

# Angel\_CY

## UMA Schematics Document

### IVY Bridge

### Intel PCH

*DY :None Installed*  
*DIS:DIS installed*  
*DIS\_Muxless :BOTH DIS or Muxless installed*  
*DIS\_PX:BOTH DIS or PX installed*  
*DIS\_PX\_Muxless:DIS or PX or Muxless installed.*  
*Muxless: Muxless installed.(PX4.0)*  
*PX:MUX installed.(PX3.0)*  
*PX\_Muxless:BOTH PX or Muxless installed.*  
*UMA:UMA installed*  
*UMA\_Muxless:BOTH UMA or Muxless installed*  
*UMA\_PX\_Muxless:UMA or PX or Muxless installed*

*ANNIE: ONLY FOR ANNIE solution.*  
*PSL: KBC795 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*65W: for 65W adaptor installed.*  
*90W: for 90W adaptor installed.*

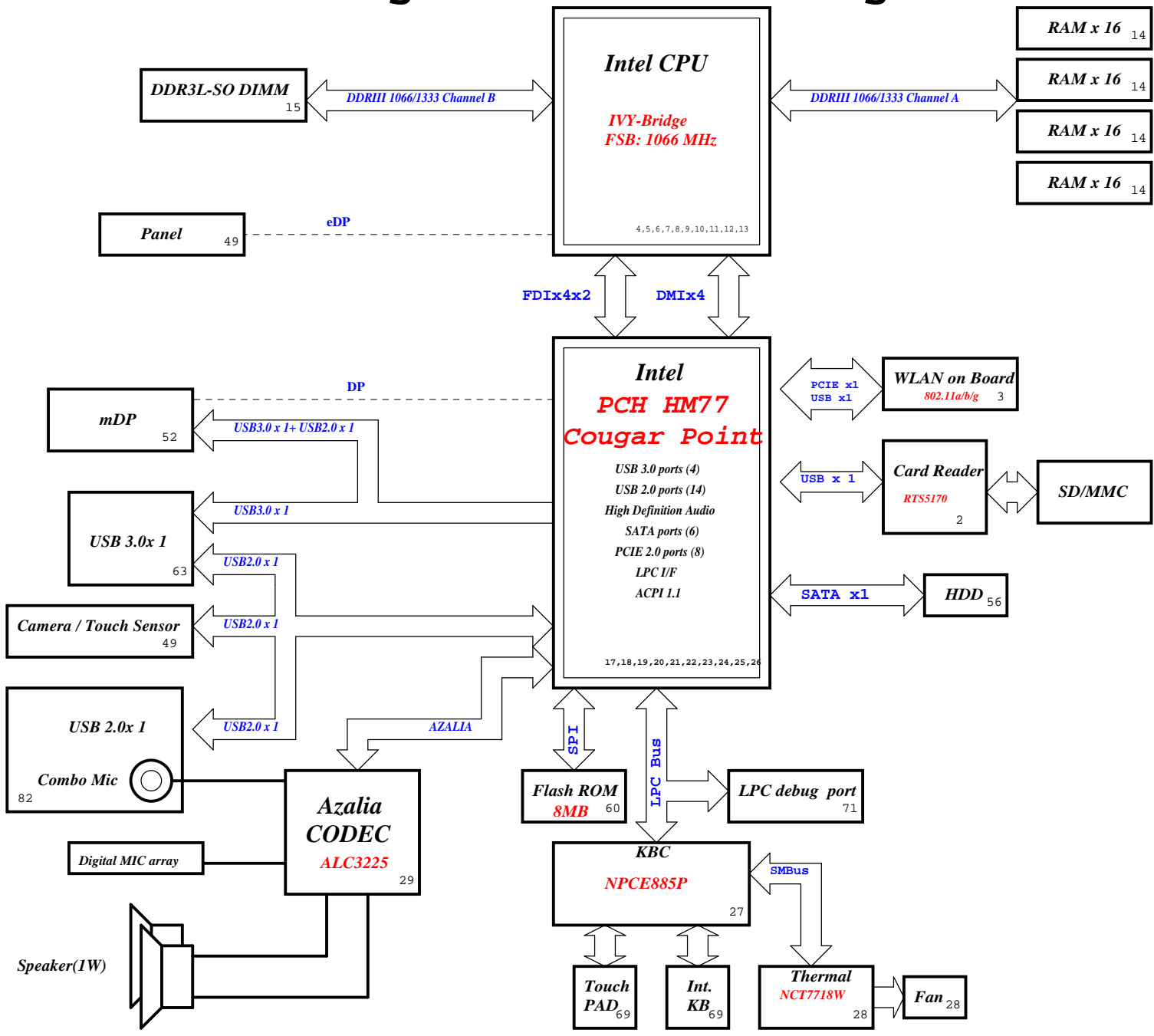
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Title <b>Cover Page</b>		
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Project code : 91.4LJ01.001  
 PCB P/N :  
 Revision : 12313-1

# Angel-CY Block Diagram



SYSTEM DC/DC BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
CPU DC/DC TPS51640 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE VCC_GFXCORE
SYSTEM DC/DC TPS51363 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3
SYSTEM DC/DC SYW232 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
SYSTEM LOD S-1339D 47	
INPUTS	OUTPUTS
1D8V_S0	1D5V_S0
SYSTEM DC/DC SY8037 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0
<b>PCB LAYER</b>	
L1:Top	L5:Signal
L2:VCC	L6:Signal
L3:Signal	L7:GND
L4:GND	L8:Bottom

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Title: **Block Diagram**

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Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> Default Mode: Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Leave floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0: connect to the EMBEDDED display Port	0
CFG[6:5]	<b>PCI-Express Port Bifurcation Straps</b>	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	<b>PEG DEFER TRAINING</b>	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

**USB Table**

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

**PCIE Routing**

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

**SATA Table**

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

**SMBus ADDRESSES**

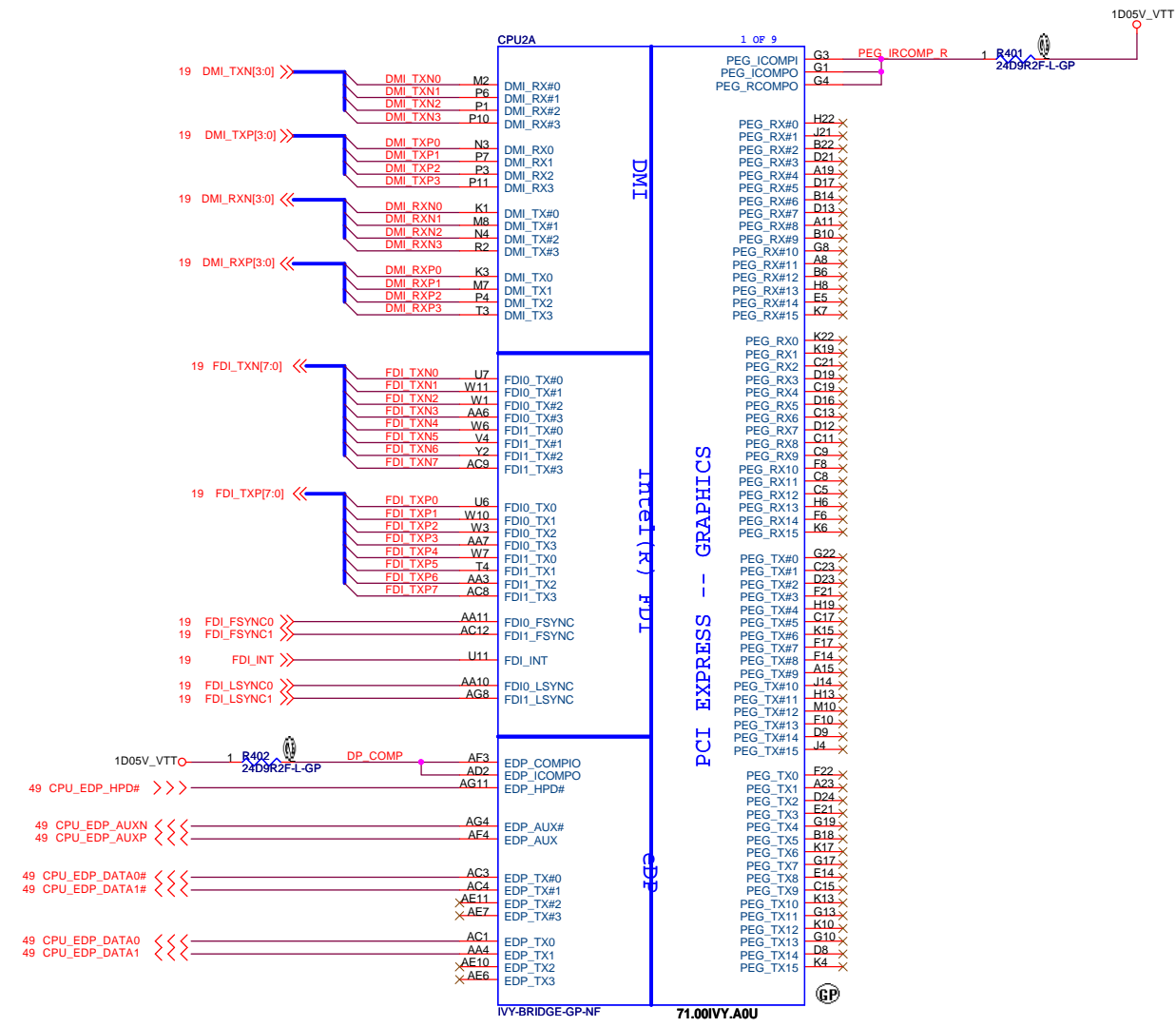
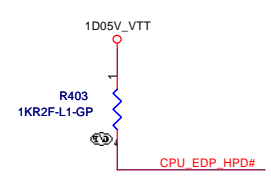
I <sup>2</sup> C / SMBus Addresses	Ref Des	HURON RIVER ORB	
		Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

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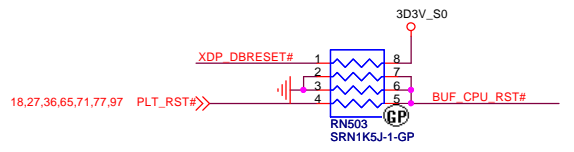
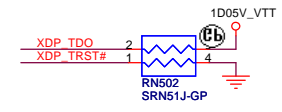
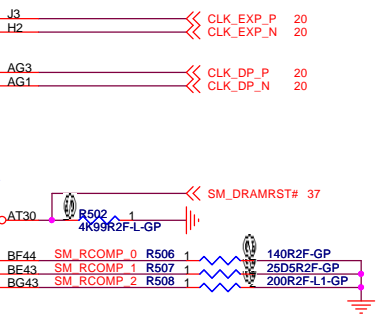
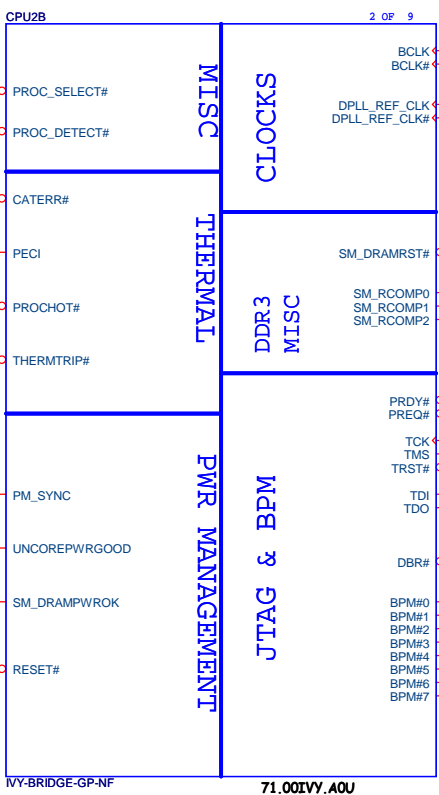
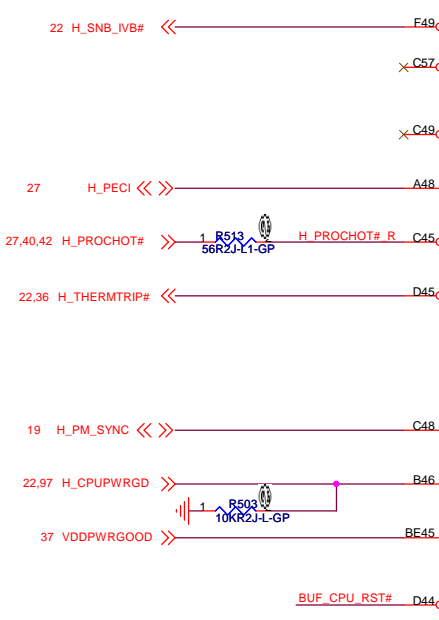
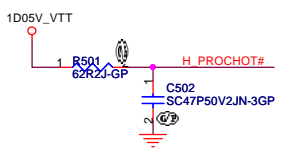


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<b>CPU (PCIE/DMI/FDI)</b>	
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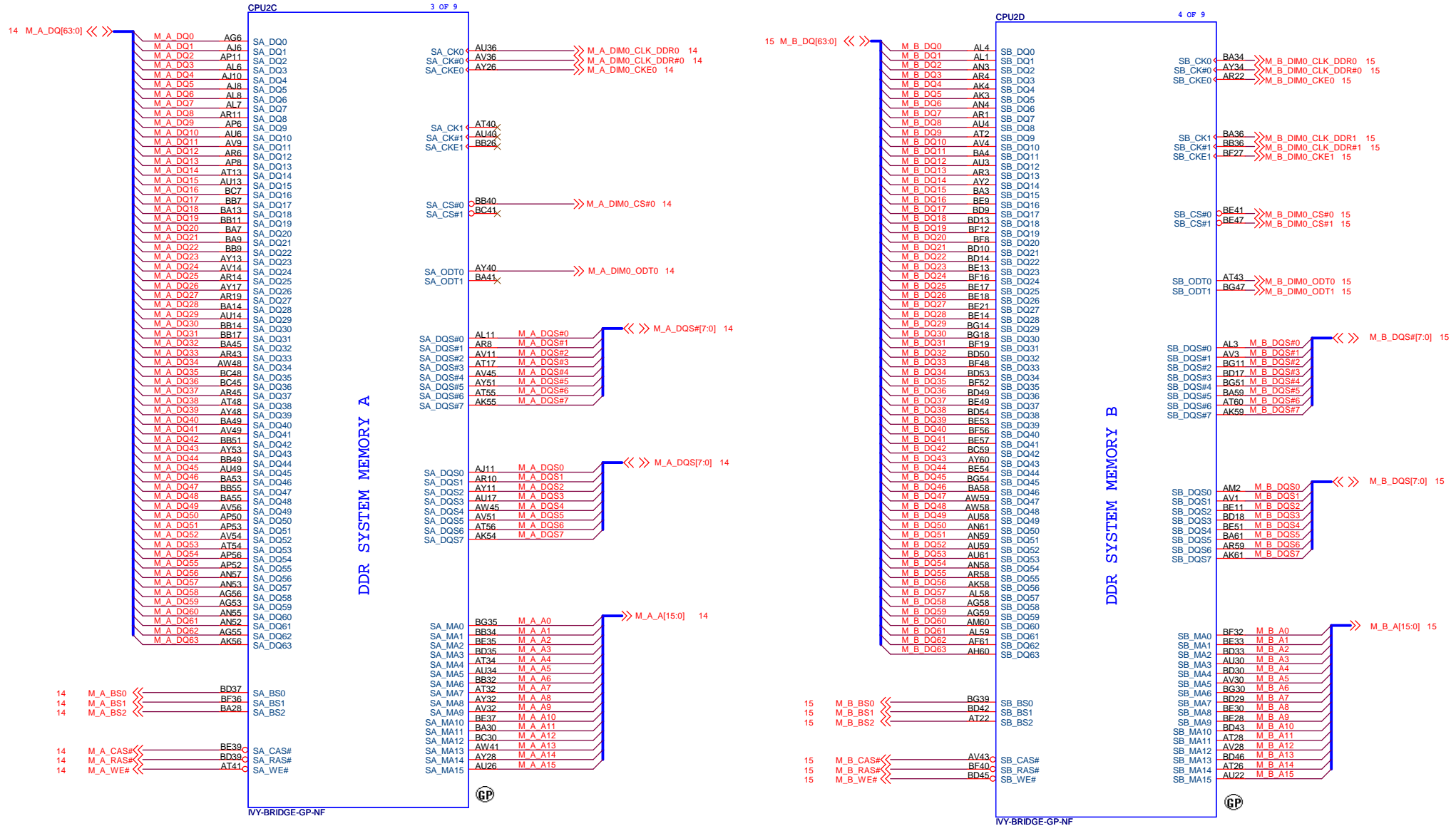
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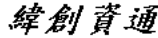
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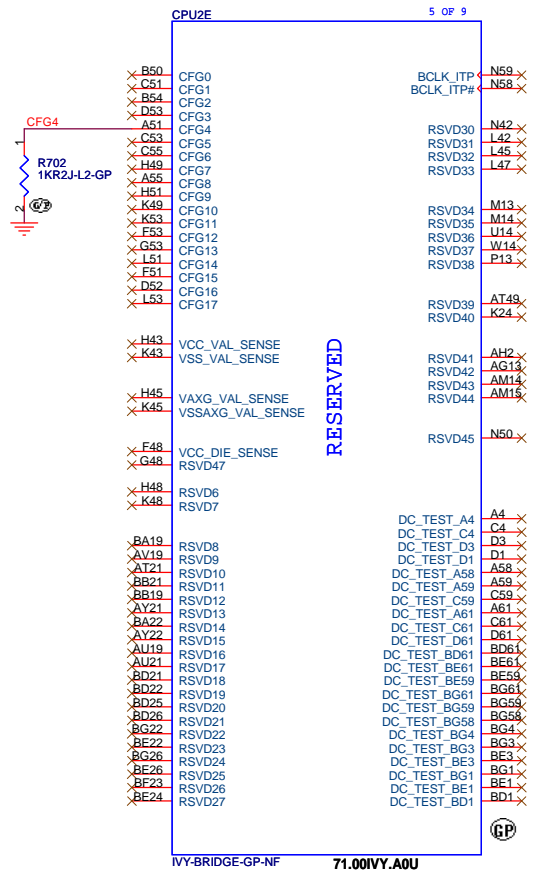
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<b>CPU (THERMAL/CLOCK/PM )</b>			
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<b>CPU (DDR)</b>	
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Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition  0: Lane Reversed	0
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable  0: Enabled - An external Display Port device is connected to the Embedded Display Port  Pull-down to GND through a 1KΩ ± 5% resistor to enable port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	00
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

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<b>CPU (RESERVED)</b>			
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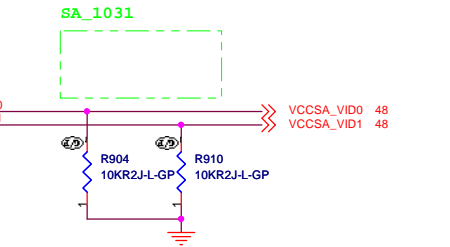
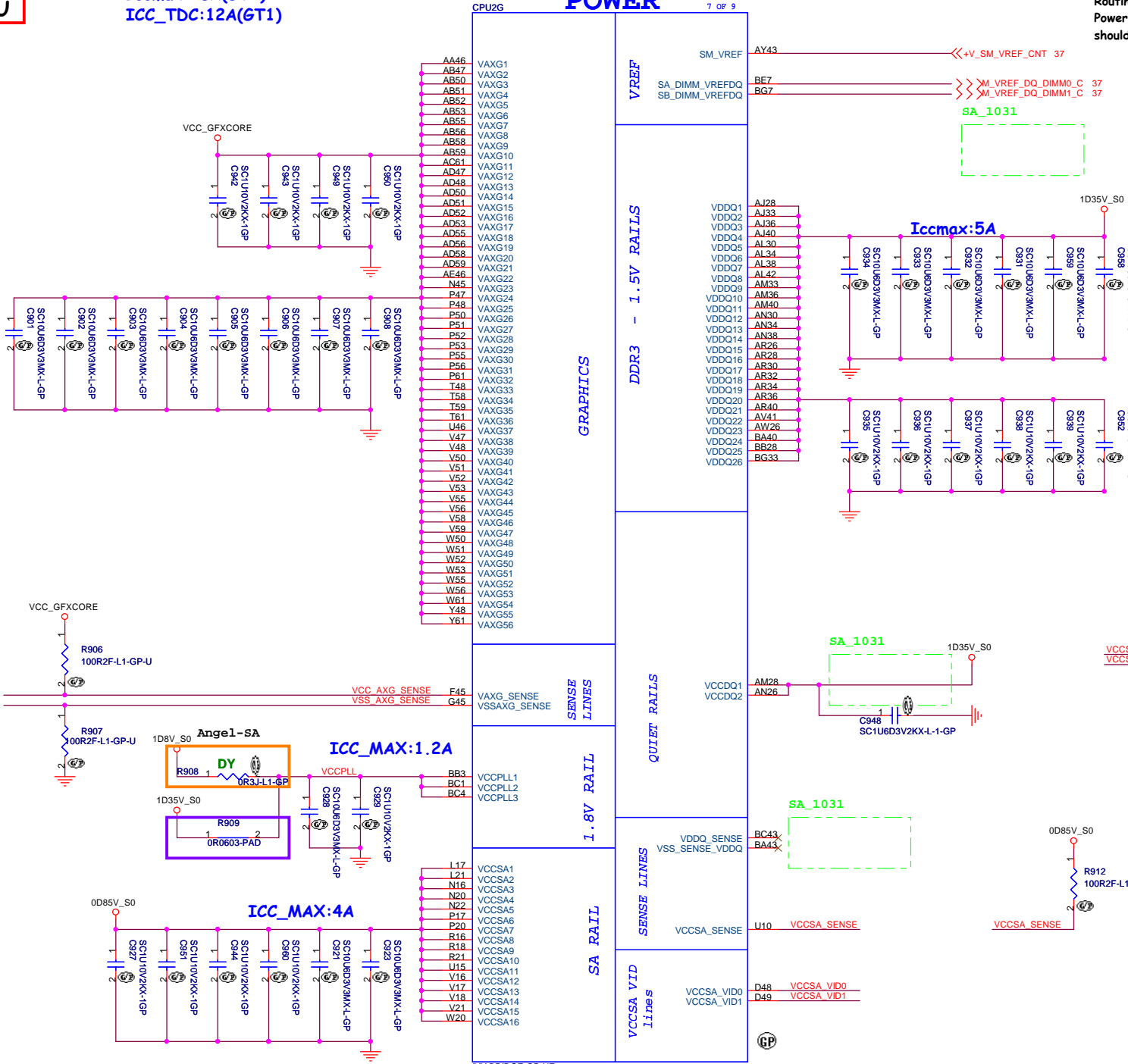


SSID = CPU

Iccmax:18A(GT1)  
ICC\_TDC:12A(GT1)

POWER

Routing Guideline:  
Power from DDR\_VREF\_S3 and +V\_SM\_VREF\_CNT  
should have 10 mils trace width.



VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

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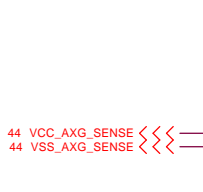
Title: **CPU (VCC\_GFXCORE)**

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- GRAPHICS**
- VAXG1-VAXG56
  - TS48-TS59
  - W50-W59
  - W61-W68
  - Y48-Y61
- SENSE LINES**
- VAXG\_SENSE F45
  - VSS\_AXG\_SENSE G45
  - VCCPLL1-VCCPLL3 BB3-BC4
  - VCCSA1-VCCSA16 L17-W20
  - VCCSA\_VID0, VCCSA\_VID1 D48-D49
- QUIET RAILS**
- VCCDQ1, VCCDQ2 AM28, AN26
- 1.8V RAIL**
- VCCPLL1-VCCPLL3 BB3-BC4
- SA RAIL**
- VCCSA1-VCCSA16 L17-W20
- VY-BRIDGE-GP-NF 71.00IVY.A0U

44 VCC\_AXG\_SENSE  
44 VSS\_AXG\_SENSE



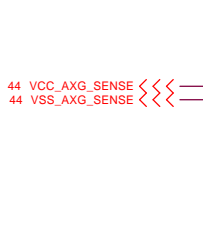
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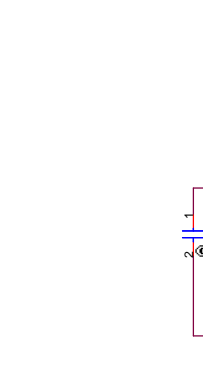
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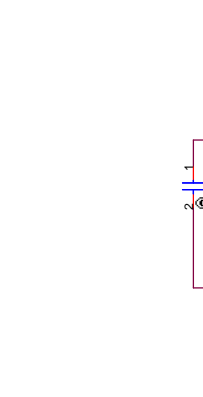
VCC\_GFXCORE



VCC\_GFXCORE



ICC\_MAX:5A



VREF



CPU2G



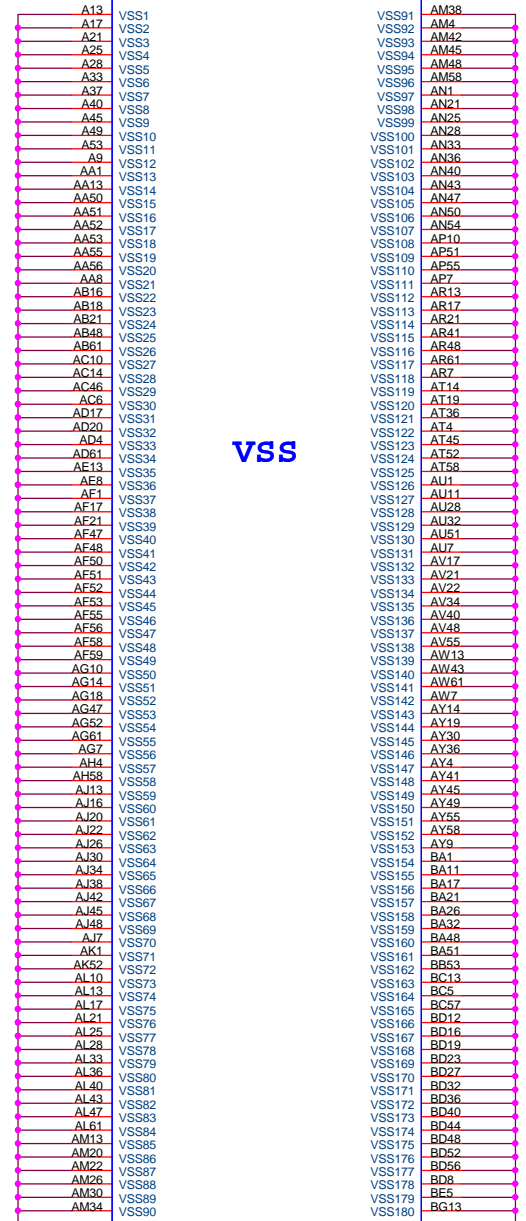
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CPU2H

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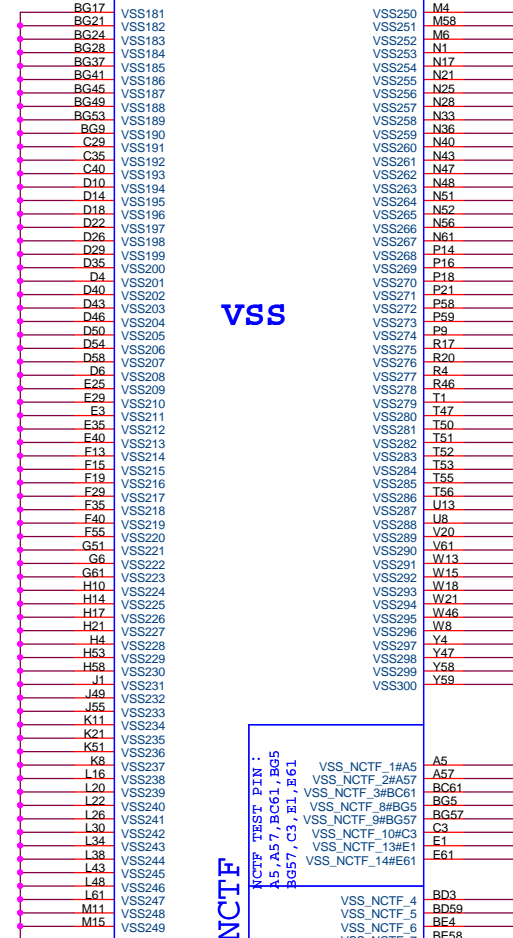


IVY-BRIDGE-GP-NF



CPU2I

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IVY-BRIDGE-GP-NF

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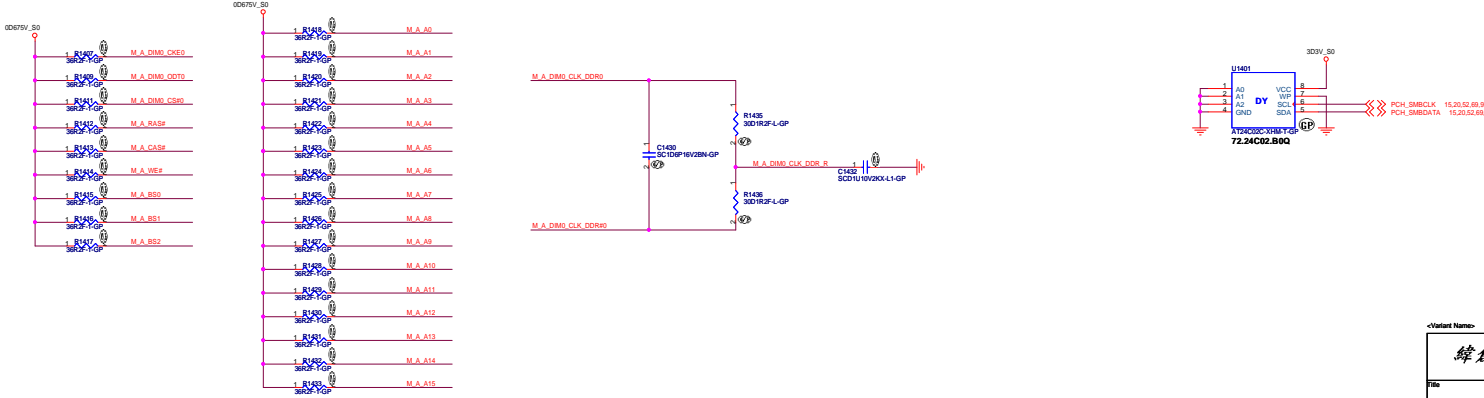
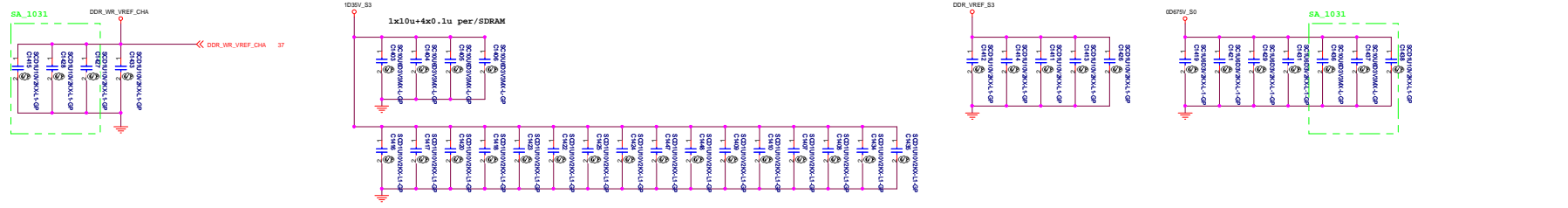
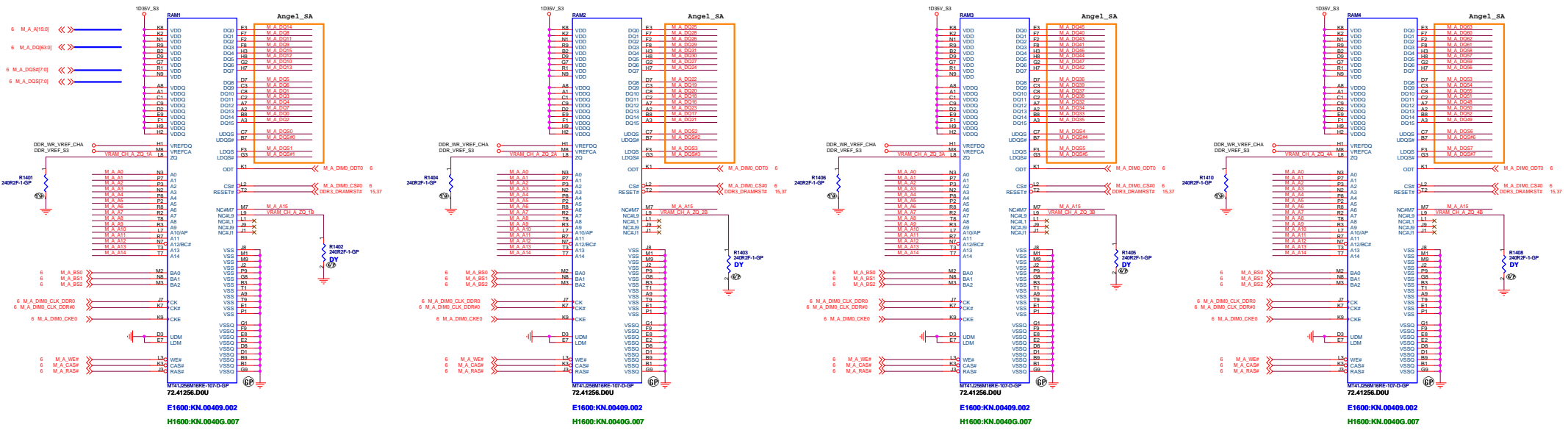
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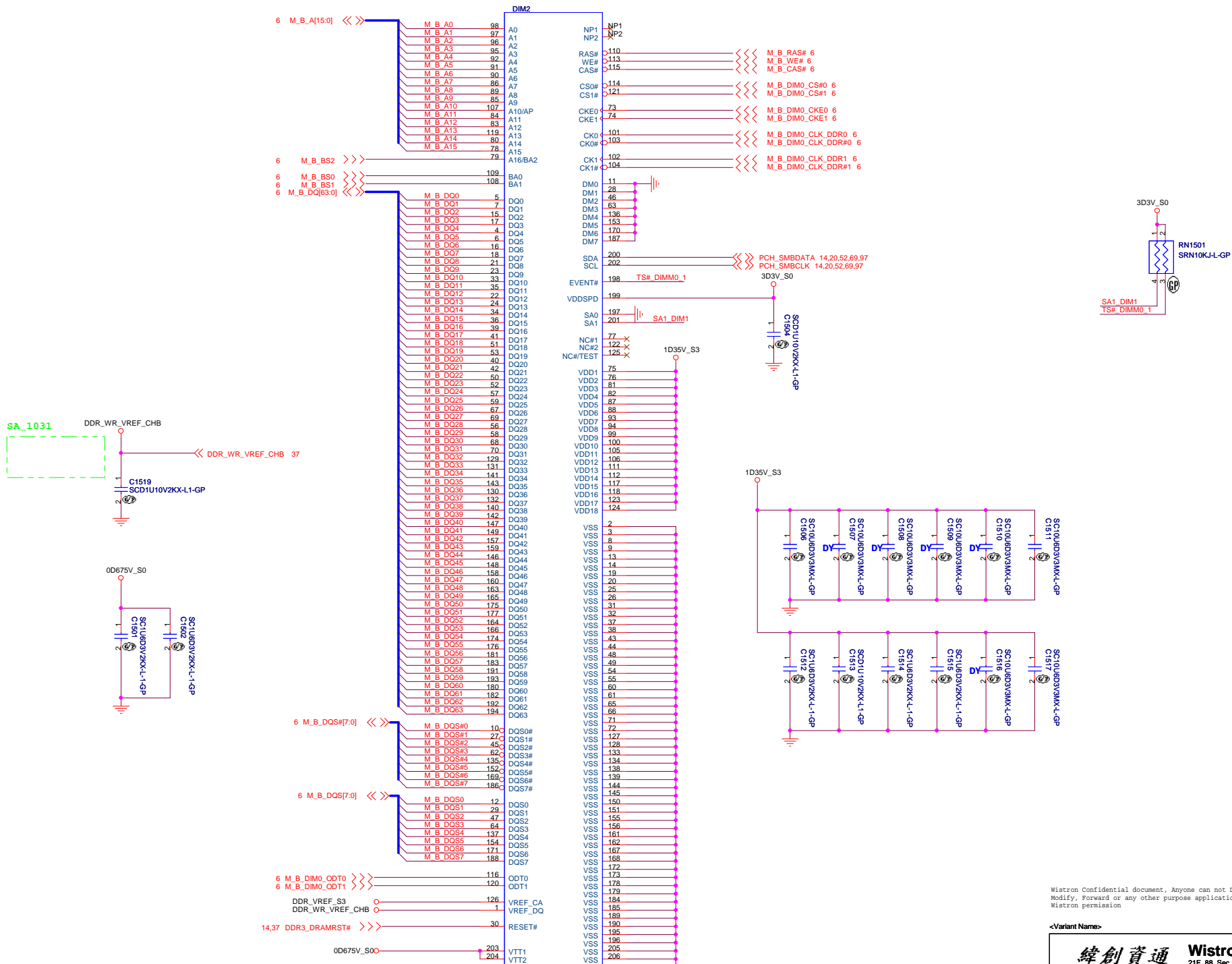
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File: DDR3-SODIMM1  
 Size: 1 Document Number: 1 Rev: 1  
 Custom: Ange1-CY  
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 3RD = 62.10024.S11  
 4th = 62.10017.X31

1st = 62.10024.M51

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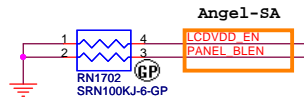
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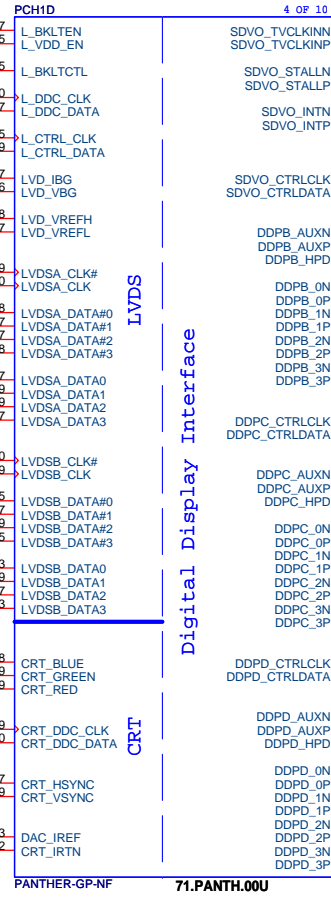
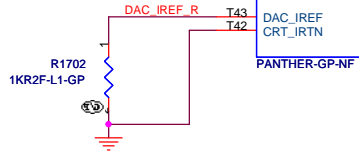
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A4	<b>Angel-CY</b>		<b>1</b>
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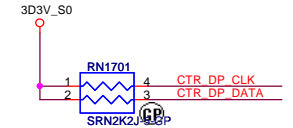




27 PANEL\_BLEN  
49 LCDVDD\_EN  
49 PCH\_BKLT\_CTL



Digital Display Interface



CTR\_DP\_CLK  
CTR\_DP\_DATA

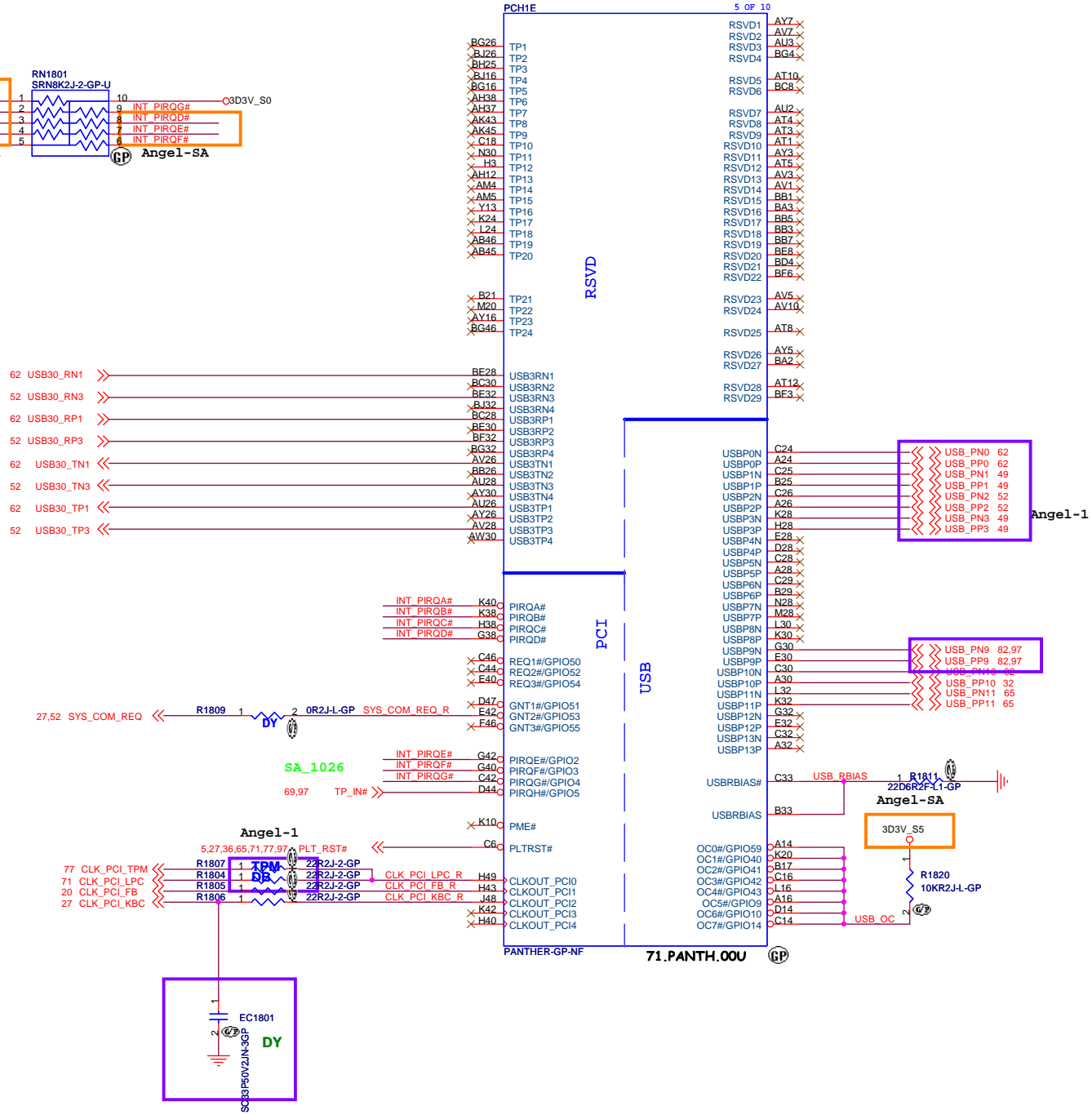
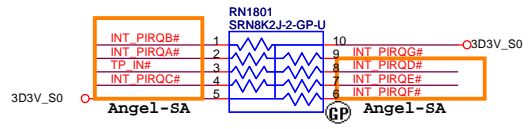
CTR\_DP\_CLK 52  
CTR\_DP\_DATA 52  
PCH\_DP\_AUXN 52  
PCH\_DP\_AUXP 52  
PCH\_DP\_HPD 52  
PCH\_DP\_DATA0# 52  
PCH\_DP\_DATA0 52  
PCH\_DP\_DATA1# 52  
PCH\_DP\_DATA1 52  
PCH\_DP\_DATA2# 52  
PCH\_DP\_DATA2 52  
PCH\_DP\_DATA3# 52  
PCH\_DP\_DATA3 52

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<b>PCH (LVDS/CRT/DDI)</b>		
Title		
Size A3	Document Number	Rev
	<b>Angel-CY</b>	<b>1</b>
Date: Monday, April 22, 2013	Sheet 17 of	102

**SSID = PCH**



**USB Table**

Pair	Device
0	USB3.0 Ext. port 1
1	TOUCH PANEL
2	mDP
3	CCD
4	NC
5	NC
6	X
7	X
8	NC
9	USB2.0 Ext. port 1
10	Card Reader
11	Mini Card1 (BT)
12	NC

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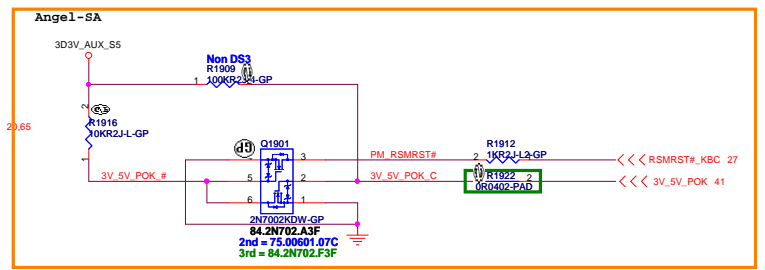
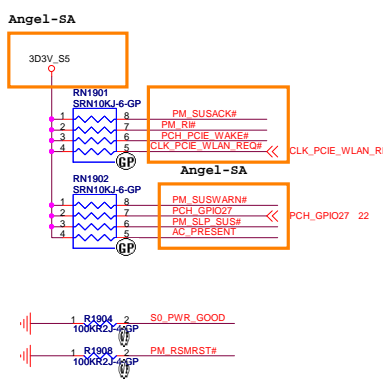
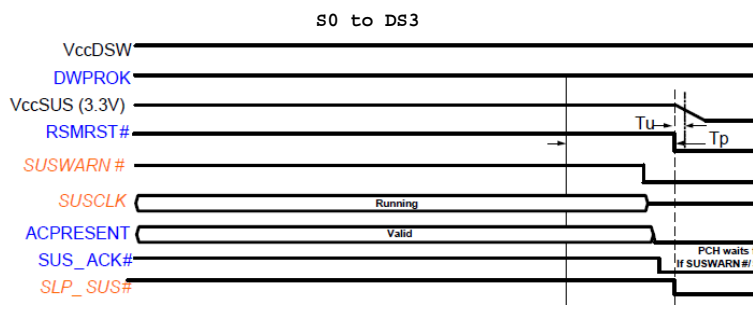
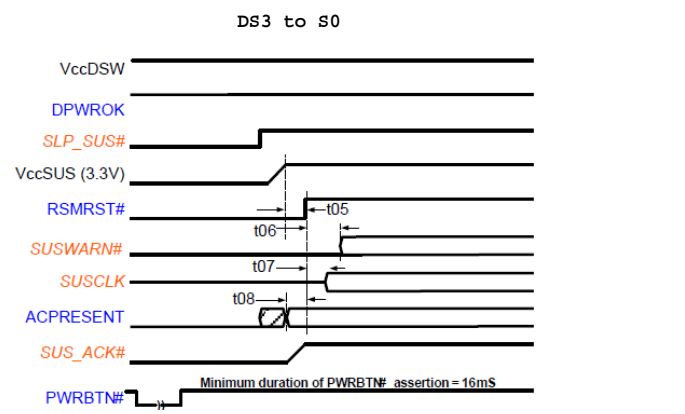
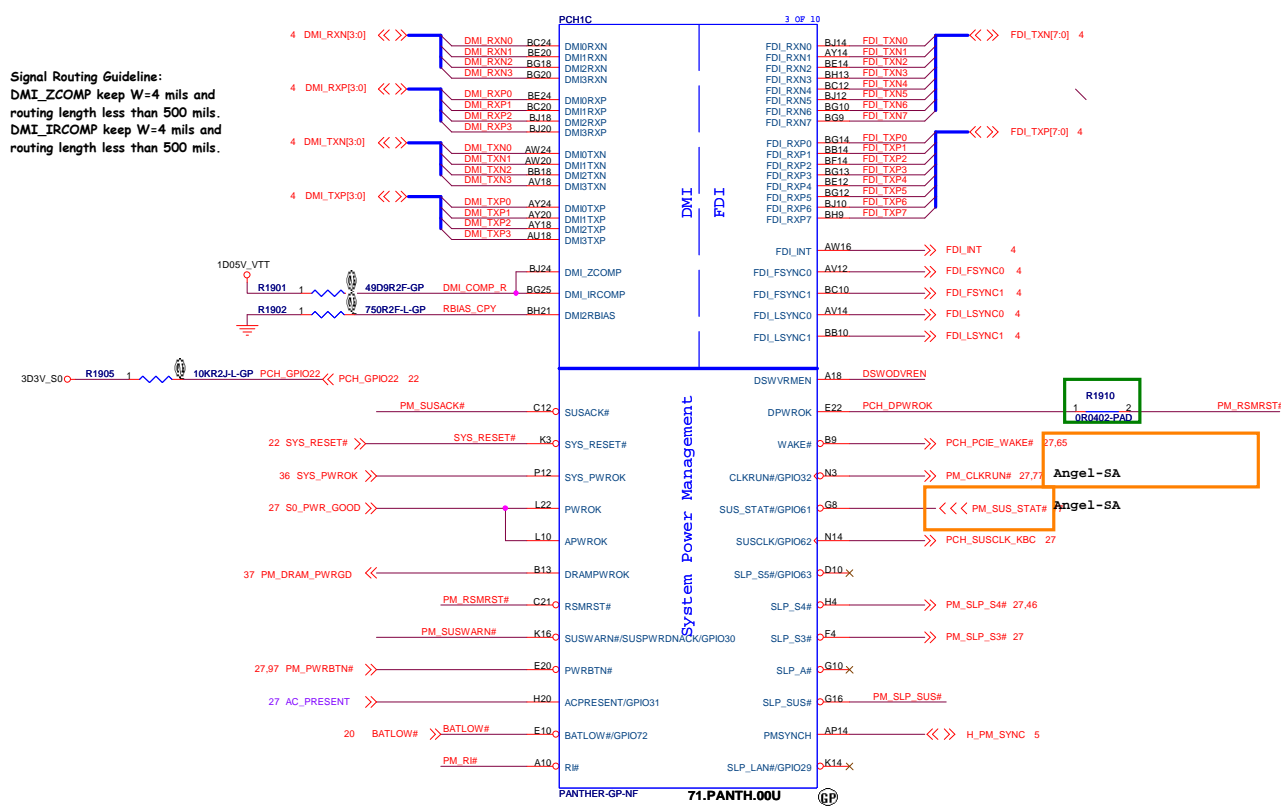
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Title: **PCH (PCI/USB/NVRAM)**

Size: A3 Document Number: **Angel-CY** Rev: **1**

Date: Monday, April 22, 2013 Sheet 18 of 102

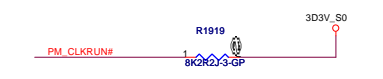
Signal Routing Guideline:  
 DMI\_ZCOMP keep W=4 mils and routing length less than 500 mils.  
 DMI\_IRCOMP keep W=4 mils and routing length less than 500 mils.



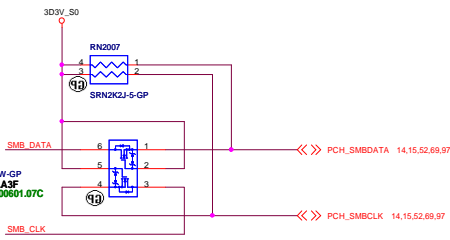
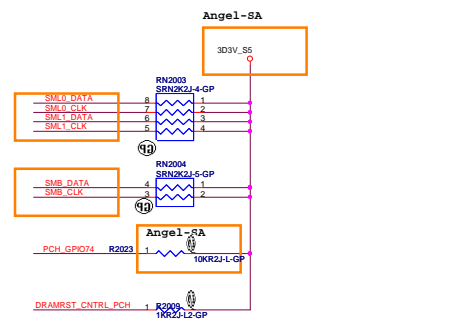
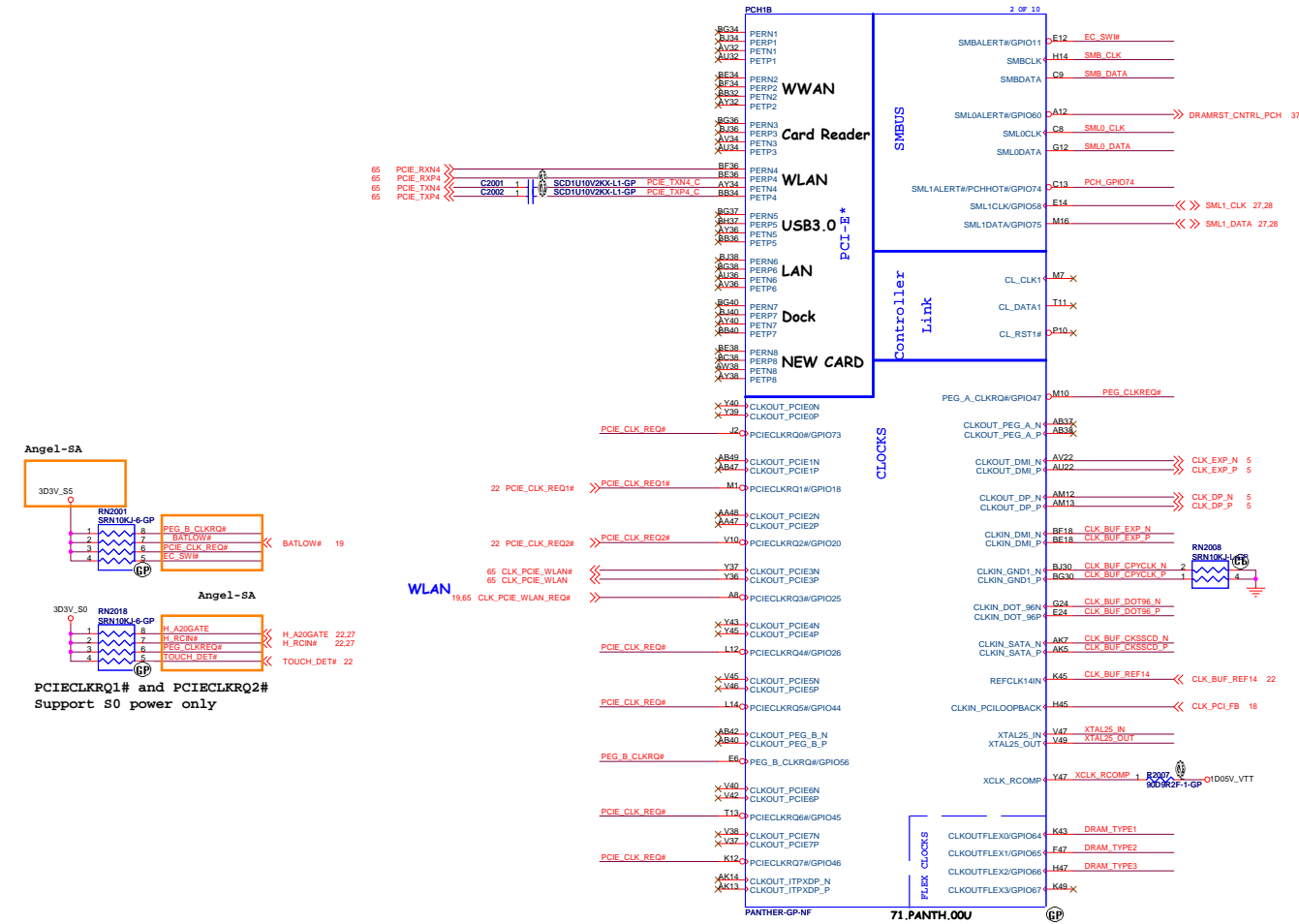
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC\_AUX\_S5

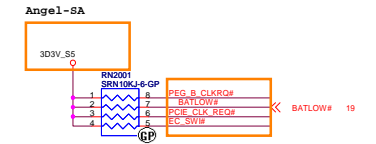
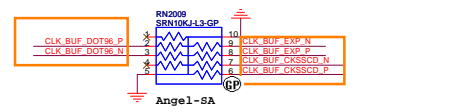
DSWODVREN R1917, 1 330KR2F1-GP



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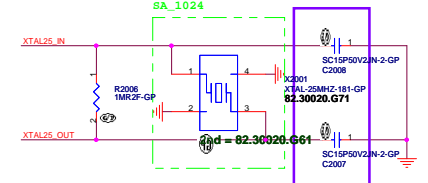
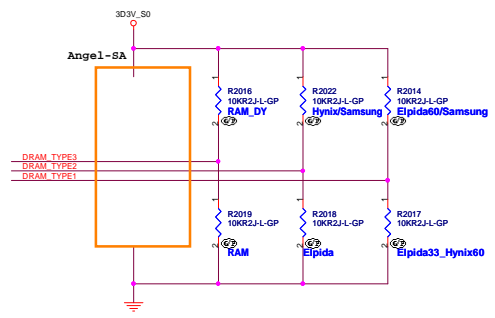


UMA\_DIS# : DGPU\_PRSNNT#  
 UMA : 1 1  
 DIS : 0 1  
 SG(PX) : 0 0  
 Optimus(Muxless) : 1 0



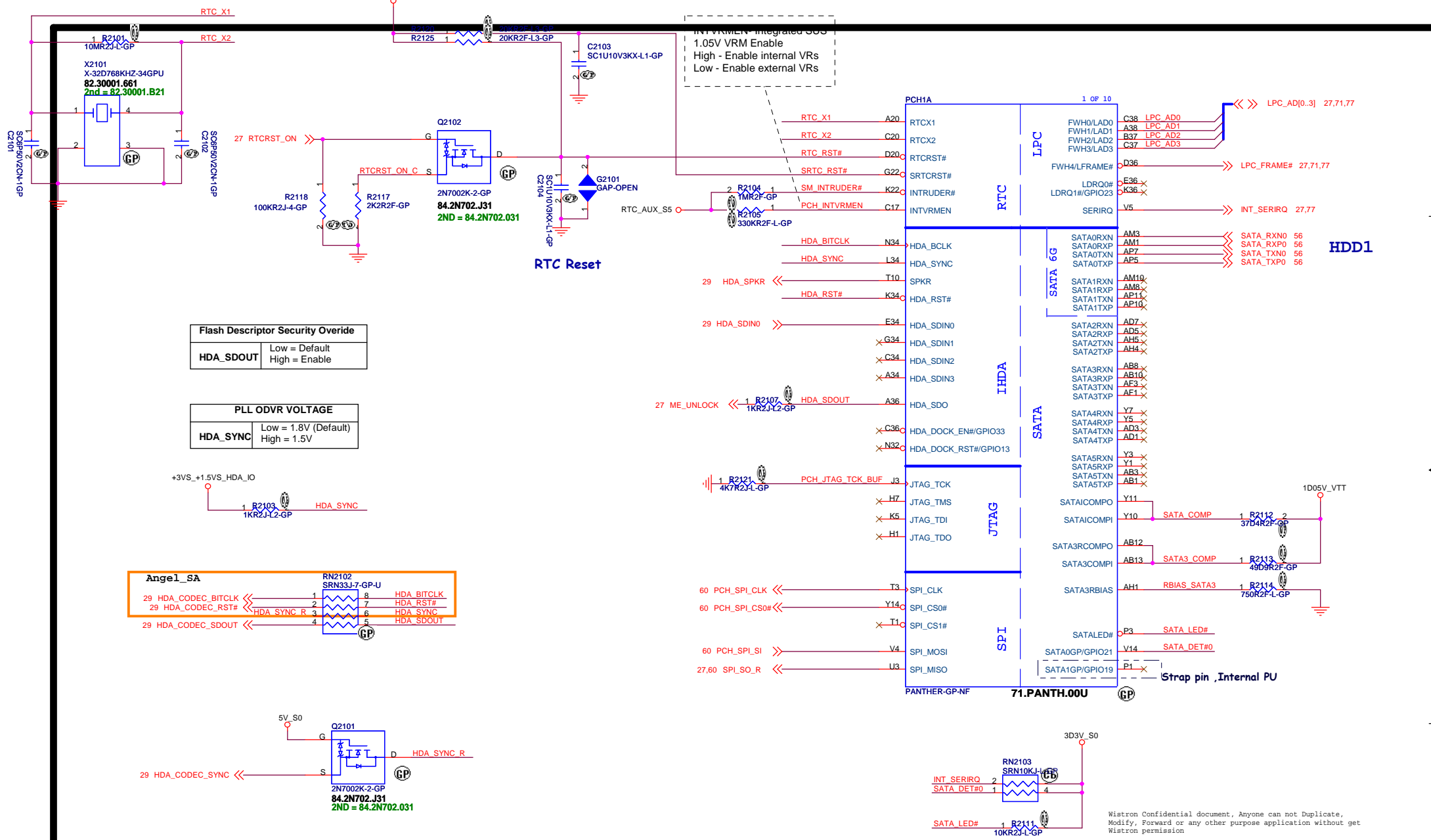
PCIECLKRQ1# and PCIECLKRQ2#  
 Support S0 power only

GPIC06	GPIC05	GPIC04	Status
DRAM_Type3	DRAM_Type2	DRAM_Type1	
0	0	0	ELPIDA_KM.00409.003 ELPIDA DDR3L 1333 4Gb EDJ4216EBBG-D1-F
0	0	1	ELPIDA_KN.00409.002 ELPIDA DDR3L 1600 4Gb EDJ4216EFBG-GNL-F
0	1	0	Hymix_KN.0040G.007 HYNIX DDR3L 1600 4Gb H5TC4G63AFR-PBA LF+HF 256*16 29nm



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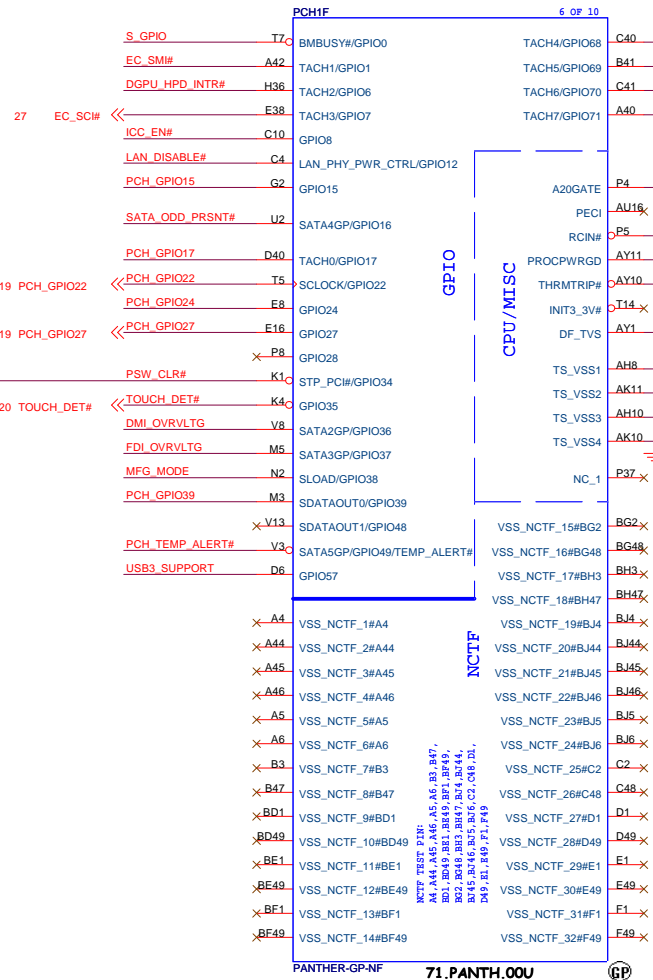
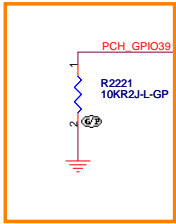
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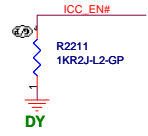
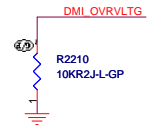
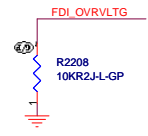
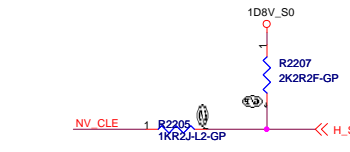
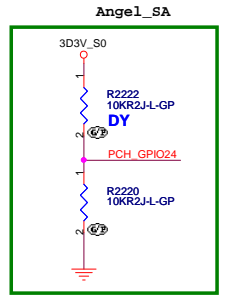
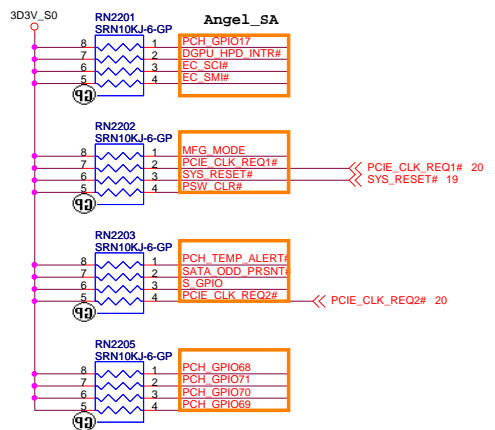
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

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SSID = PCH



Pass Word Clear



FDI TERMINATION VOLTAGE OVERRIDE(Reserved)	
FDI_OVRVLTG (GPIO37)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE(Reserved)	
DMI_OVRVLTG (GPIO36)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable(Reserved)	
ICC_EN# (GPIO8)	HIGH- DISABLED [DEFAULT]
	LOW - ENABLED

NCTF Pin:  
A1, A4, A45, A46, A5, A6, B3, B47, B01, B049, B81, B849, B81, B849, B02, B049, B83, B847, B04, B044, B45, B046, B05, B06, C2, C48, D1, D49, E1, F49

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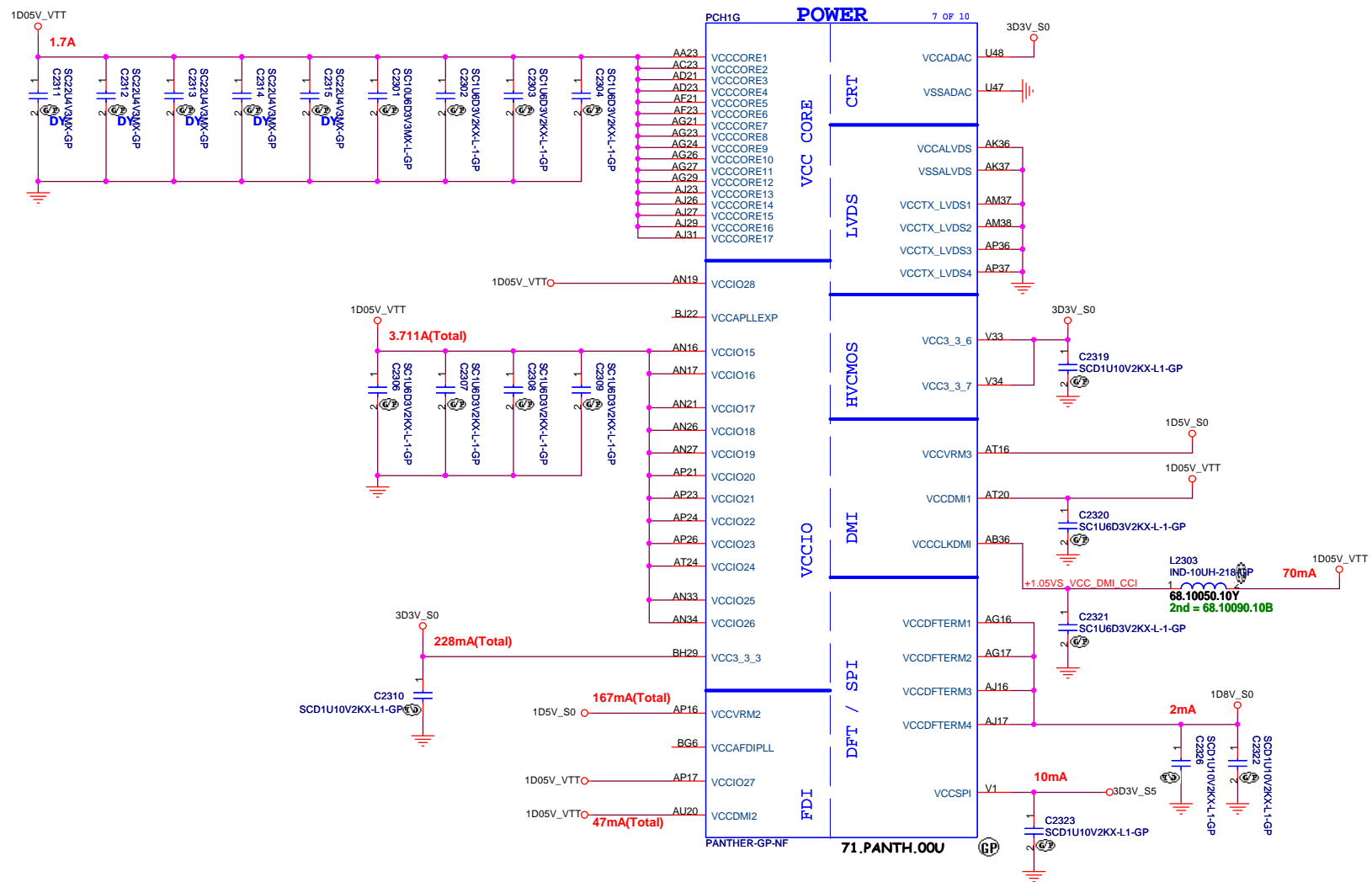
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Size: Custom Document Number: **Angel-CY** Rev: **1**

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<b>Title</b> <b>PCH (POWER1)</b>		
<b>Size</b> A3	<b>Document Number</b> <b>Angel-CY</b>	<b>Rev</b> <b>1</b>
<b>Date:</b> Monday, April 22, 2013		
Sheet 23 of 102		

SSID = PCH

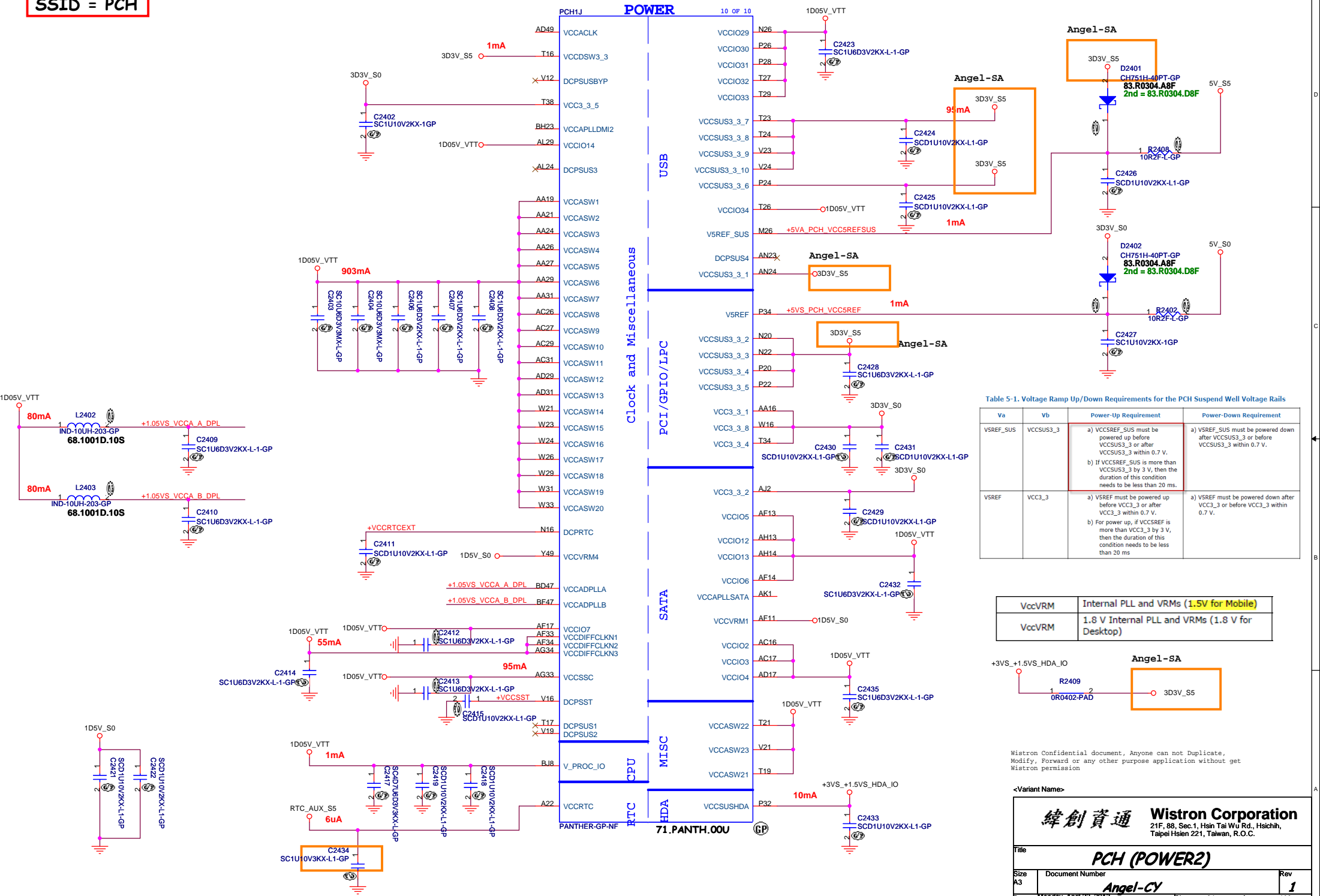
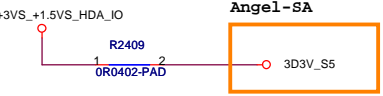


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
V5REF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) V5REF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
V5REF	VCC3_3	a) V5REF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) V5REF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)



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SSID = PCH

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H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK4
AA3	VSS3	VSS82	AK42
AA33	VSS4	VSS83	AK46
AA34	VSS5	VSS84	AK9
AB11	VSS6	VSS85	AL16
AB14	VSS7	VSS86	AL17
AB39	VSS8	VSS87	AL19
AB4	VSS9	VSS88	AL2
AB43	VSS10	VSS89	AL21
AB5	VSS11	VSS90	AL23
AB7	VSS12	VSS91	AL26
AC19	VSS13	VSS92	AL27
AC2	VSS14	VSS93	AL31
AC21	VSS15	VSS94	AL33
AC24	VSS16	VSS95	AL34
AC33	VSS17	VSS96	AL48
AC34	VSS18	VSS97	AM11
AC48	VSS19	VSS98	AM14
AD10	VSS20	VSS99	AM36
AD11	VSS21	VSS100	AM39
AD12	VSS22	VSS101	AM43
AD13	VSS23	VSS102	AM45
AD19	VSS24	VSS103	AM46
AD24	VSS25	AM7	AN2
AD26	VSS26	VSS104	AN2
AD27	VSS27	VSS105	AN29
AD33	VSS28	VSS106	AN29
AD34	VSS29	VSS107	AN3
AD36	VSS30	VSS108	AN31
AD37	VSS31	VSS109	AP12
AD38	VSS32	VSS110	AP19
AD39	VSS33	VSS111	AP28
AD4	VSS34	VSS112	AP30
AD40	VSS35	VSS113	AP32
AD42	VSS36	VSS114	AP38
AD43	VSS37	VSS115	AP4
AD45	VSS38	VSS116	AP42
AD46	VSS39	VSS117	AP46
AD8	VSS40	VSS118	AP8
AE2	VSS41	VSS119	AR2
AE3	VSS42	VSS120	AR48
AE10	VSS43	VSS121	AT11
AE12	VSS44	VSS122	AT13
AD14	VSS45	VSS123	AT18
AD16	VSS46	VSS124	AT22
AE16	VSS47	VSS125	AT26
AF19	VSS48	VSS126	AT28
AF24	VSS49	VSS127	AT30
AF26	VSS50	VSS128	AT32
AF27	VSS51	VSS129	AT34
AF29	VSS52	VSS130	AT39
AF31	VSS53	VSS131	AT42
AF38	VSS54	VSS132	AT46
AF4	VSS55	VSS133	AT7
AF42	VSS56	VSS134	AU24
AF46	VSS57	VSS135	AU30
AF5	VSS58	VSS136	AU36
AF7	VSS59	VSS137	AV20
AF8	VSS60	VSS138	AV24
AG19	VSS61	VSS139	AV30
AG2	VSS62	VSS140	AV38
AG31	VSS63	VSS141	AV4
AG48	VSS64	VSS142	AV43
AH11	VSS65	VSS143	AV8
AH3	VSS66	VSS144	AW14
AH36	VSS67	VSS145	AW18
AH39	VSS68	VSS146	AW2
AH40	VSS69	VSS147	AW22
AH42	VSS70	VSS148	AW26
AH46	VSS71	VSS149	AW28
AH7	VSS72	VSS150	AW32
AJ19	VSS73	VSS151	AW34
AJ21	VSS74	VSS152	AW36
AJ24	VSS75	VSS153	AW40
AJ33	VSS76	VSS154	AW48
AJ34	VSS77	VSS155	AV11
AK12	VSS78	VSS156	AY12
AK3	VSS79	VSS157	AY22
		VSS158	AY28

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PCH1I 9 OF 10

AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY8	VSS162	VSS262	K39
B11	VSS163	VSS263	K46
B19	VSS164	VSS264	K7
B23	VSS165	VSS265	L18
B27	VSS166	VSS266	L2
B31	VSS167	VSS267	L20
B35	VSS168	VSS268	L26
B39	VSS169	VSS269	L28
B7	VSS170	VSS270	L48
F45	VSS171	VSS271	L48
BB12	VSS172	VSS272	M12
BB16	VSS173	VSS273	M16
BB20	VSS174	VSS274	M18
BB22	VSS175	VSS275	M22
BB24	VSS176	VSS276	M24
BB28	VSS177	VSS277	M30
BB30	VSS178	VSS278	M32
BB38	VSS179	VSS279	M34
BB4	VSS180	VSS280	M38
BB46	VSS181	VSS281	M4
BC14	VSS182	VSS282	M42
BC18	VSS183	VSS283	M46
BC2	VSS184	VSS284	M6
BC22	VSS185	VSS285	M18
BC26	VSS186	VSS286	M24
BC32	VSS187	VSS287	M30
BC34	VSS188	VSS288	M32
BC36	VSS189	VSS289	M34
BC40	VSS190	VSS290	M38
BC42	VSS191	VSS291	M4
BC48	VSS192	VSS292	M42
BD46	VSS193	VSS293	M46
BD5	VSS194	VSS294	M6
BE22	VSS195	VSS295	N18
BE26	VSS196	VSS296	P30
BE40	VSS197	VSS297	N47
BF10	VSS198	VSS298	N47
BF12	VSS199	VSS299	P11
BF16	VSS200	VSS300	P18
BF20	VSS201	VSS301	T33
BF22	VSS202	VSS302	P40
BF24	VSS203	VSS303	P43
BF26	VSS204	VSS304	P47
BF28	VSS205	VSS305	P7
BD3	VSS206	VSS306	R2
BF30	VSS207	VSS307	R48
BF38	VSS208	VSS308	T12
BF40	VSS209	VSS309	T31
BF8	VSS210	VSS310	T37
BG17	VSS211	VSS311	T4
BG21	VSS212	VSS312	W34
BG33	VSS213	VSS313	T46
BG44	VSS214	VSS314	T47
BG8	VSS215	VSS315	T8
BH11	VSS216	VSS316	V11
BH15	VSS217	VSS317	V17
BH17	VSS218	VSS318	V26
BH19	VSS219	VSS319	V27
H10	VSS220	VSS320	V29
BH27	VSS221	VSS321	V31
BH31	VSS222	VSS322	V36
BH33	VSS223	VSS323	V39
BH35	VSS224	VSS324	V43
BH39	VSS225	VSS325	V7
BH43	VSS226	VSS326	W17
BH7	VSS227	VSS327	W19
D1	VSS228	VSS328	W2
D12	VSS229	VSS329	W27
D16	VSS230	VSS330	W48
D18	VSS231	VSS331	Y12
D22	VSS232	VSS332	Y4
D24	VSS233	VSS333	Y42
D26	VSS234	VSS334	Y46
D30	VSS235	VSS335	Y8
D32	VSS236	VSS336	BG29
D34	VSS237	VSS337	N24
D38	VSS238	VSS338	AJ3
D42	VSS239	VSS339	AD47
D6	VSS240	VSS340	B43
E18	VSS241	VSS341	BE10
E26	VSS242	VSS342	BG41
G18	VSS243	VSS343	G14
G20	VSS244	VSS344	H16
G26	VSS245	VSS345	T36
G28	VSS246	VSS346	BG22
G36	VSS247	VSS347	BG24
G48	VSS248	VSS348	C22
H12	VSS249	VSS349	AP13
H18	VSS250	VSS350	M14
H22	VSS251	VSS351	AF3
H24	VSS252	VSS352	AF1
H26	VSS253	VSS353	BE16
H30	VSS254	VSS354	BC16
H32	VSS255	VSS355	BG28
H34	VSS256	VSS356	BJ28
H36	VSS257		
H38	VSS258		

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Size A3	Document Number Angel-CY
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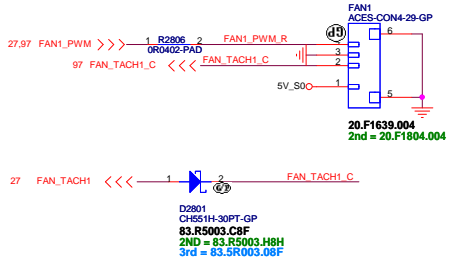
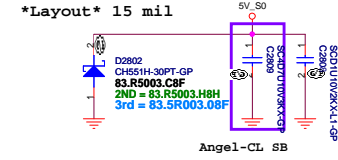
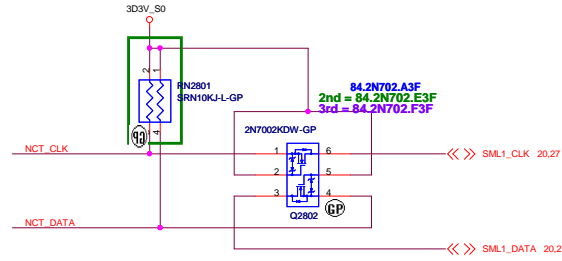
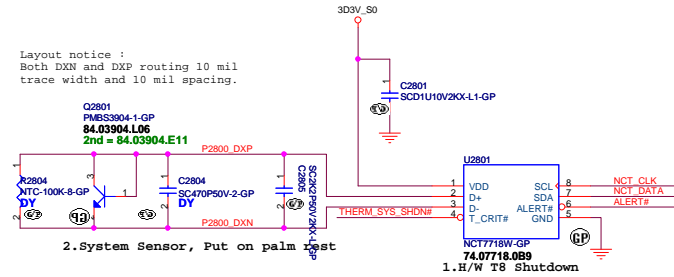
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Title			
<b><i>Clock(colay)</i></b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013		Sheet 26 of 102



# Thermal sensor NCT 7718W

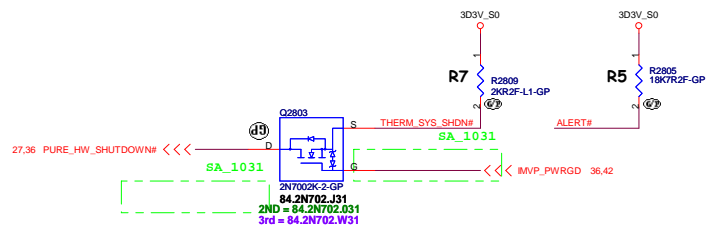
Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.



## ALERT# /T CRIT# Pull-up Resistor

R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	87°C	97°C	107°C	117°C	
79°C	89°C	99°C	109°C	119°C	
81°C	91°C	101°C	111°C	121°C	
83°C	93°C	103°C	113°C	123°C	
85°C	95°C	105°C	115°C	125°C	

T\_CRIT temperature strapping point





# AUDIO OP AMPLIFIER

# Blanking

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<Variant Name>

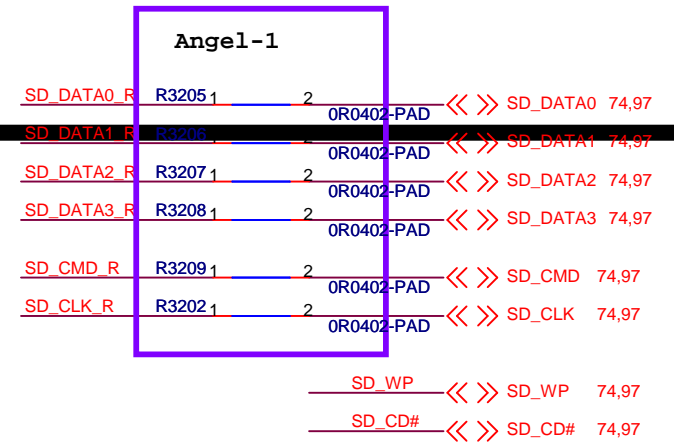
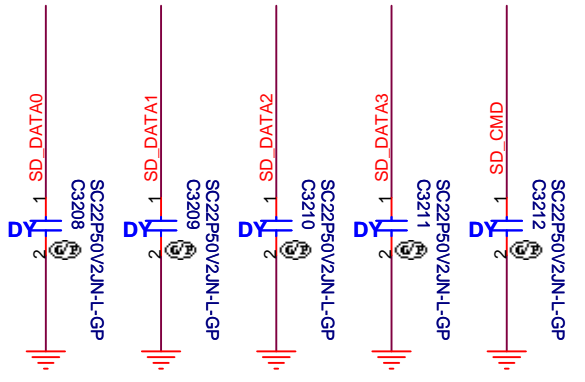
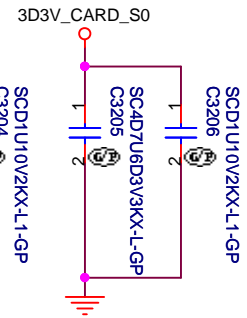
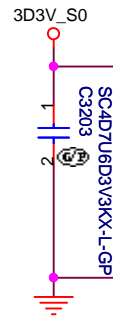
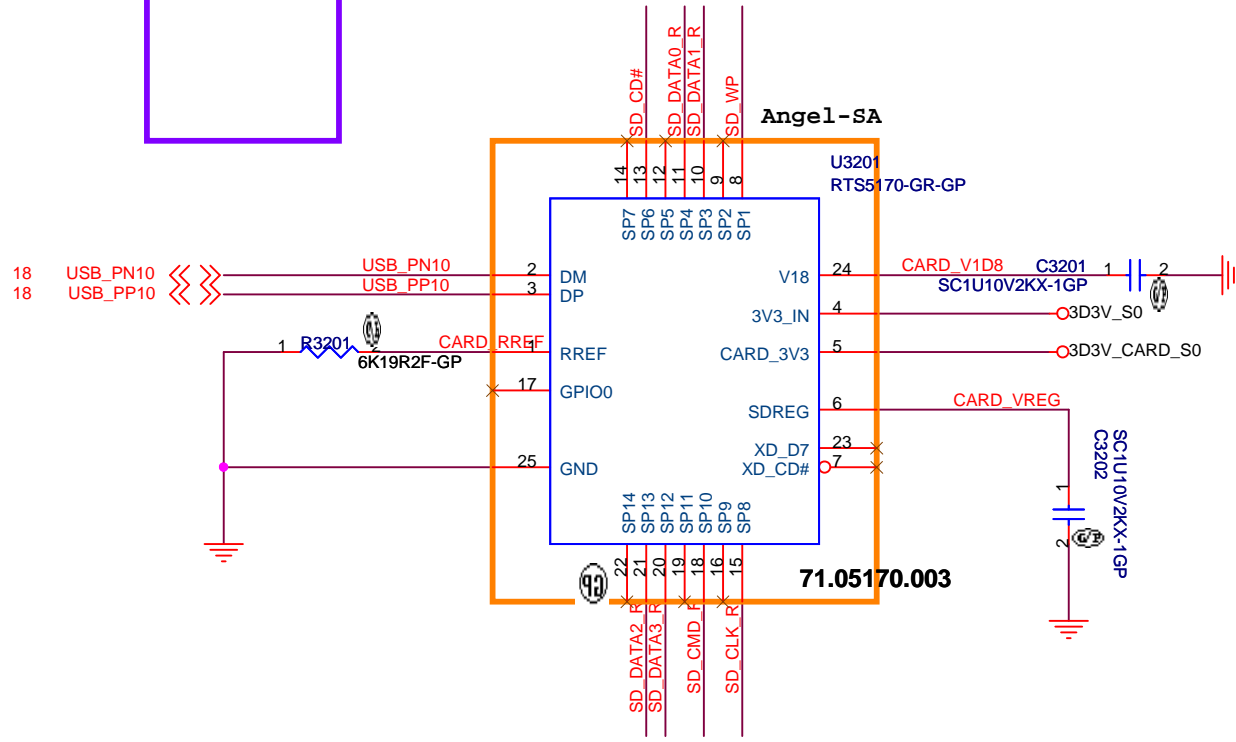
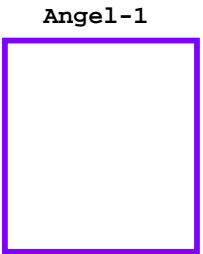
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Audio AMP</b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013		Sheet 30 of 102

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Title			
<b>AR8158</b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
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<b>RTS5159 (CARD READER)</b>			
Title <b>RTS5159 (CARD READER)</b>	Document Number <b>Angel-CY</b>		Rev <b>1</b>
Date Monday, April 22, 2013	Sheet 32	of 102	



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Title			
<b>Reserved</b>			
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A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013	Sheet 33 of	102

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Title			
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Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013	Sheet 34 of	102

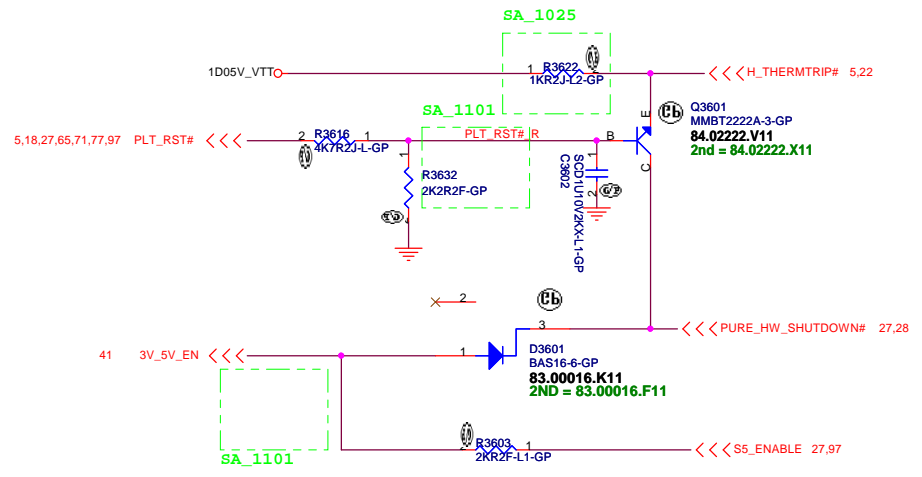
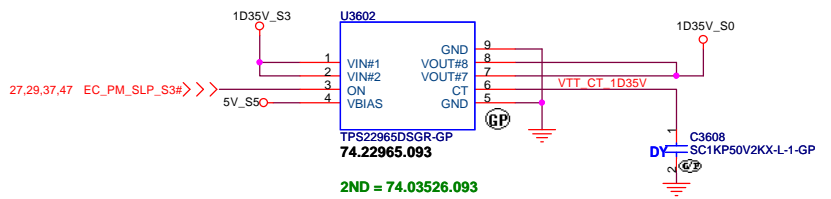
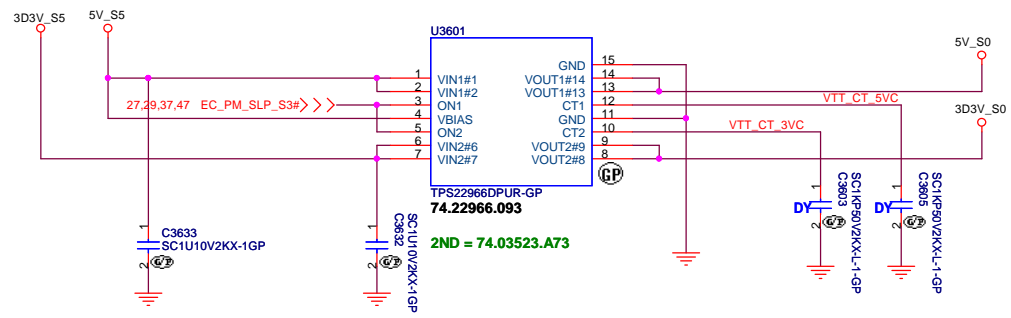
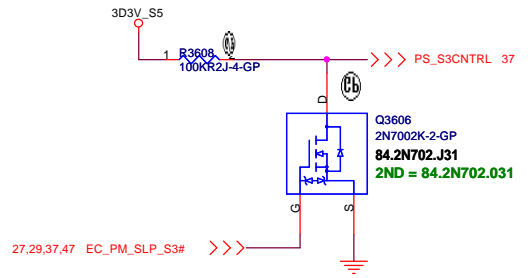
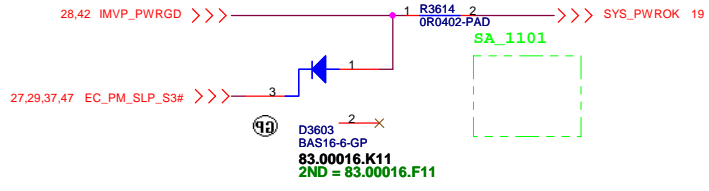
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<b>Title</b>			
<b>USB 3.0 Controller</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
A4	<b>Angel-CY</b>		<b>1</b>
<b>Date:</b> Monday, April 22, 2013		<b>Sheet</b> 35	<b>of</b> 102

# Power Sequence



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<Variant Name>

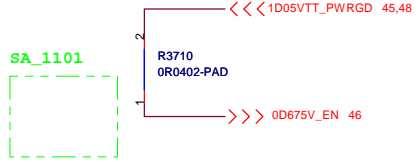
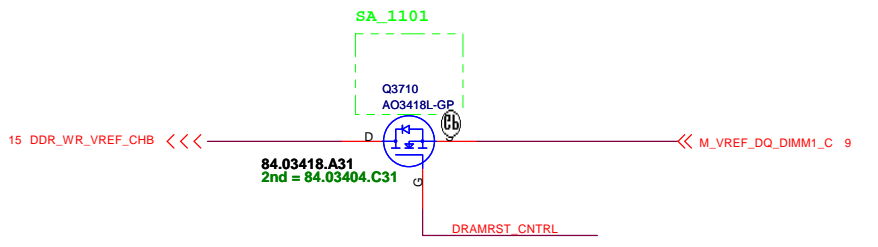
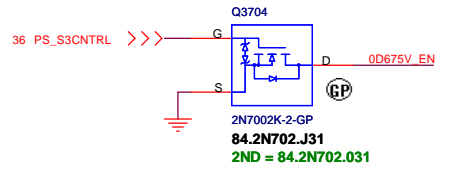
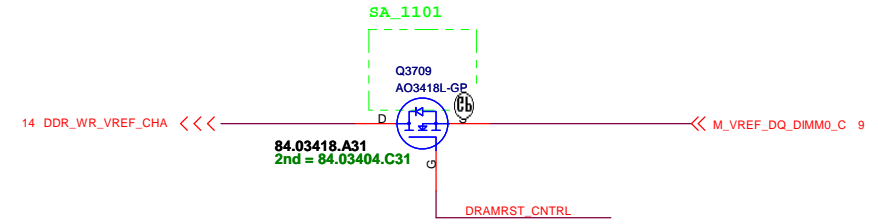
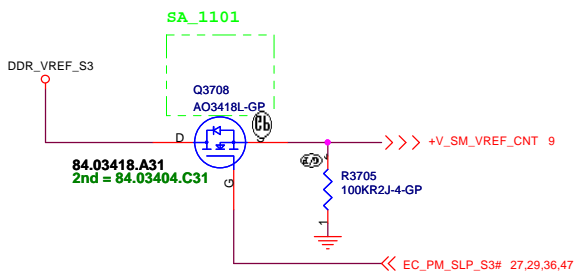
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

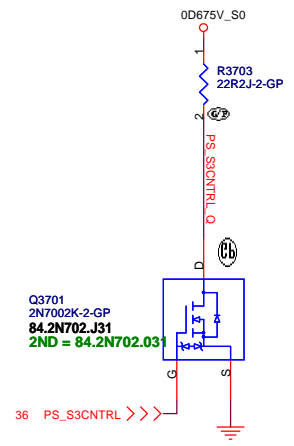
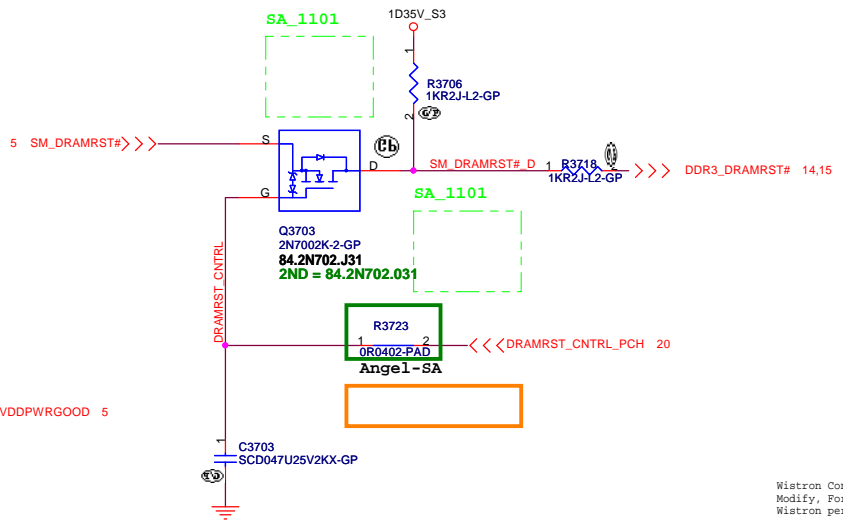
Size A3 Document Number: **Angel-CY** Rev: **1**

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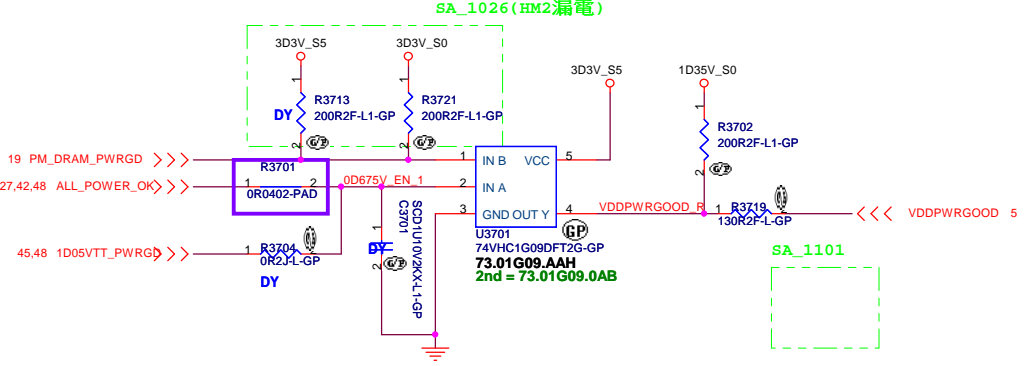
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation



S3 Power Reduction Circuit  
SM\_DRAMRST#



Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



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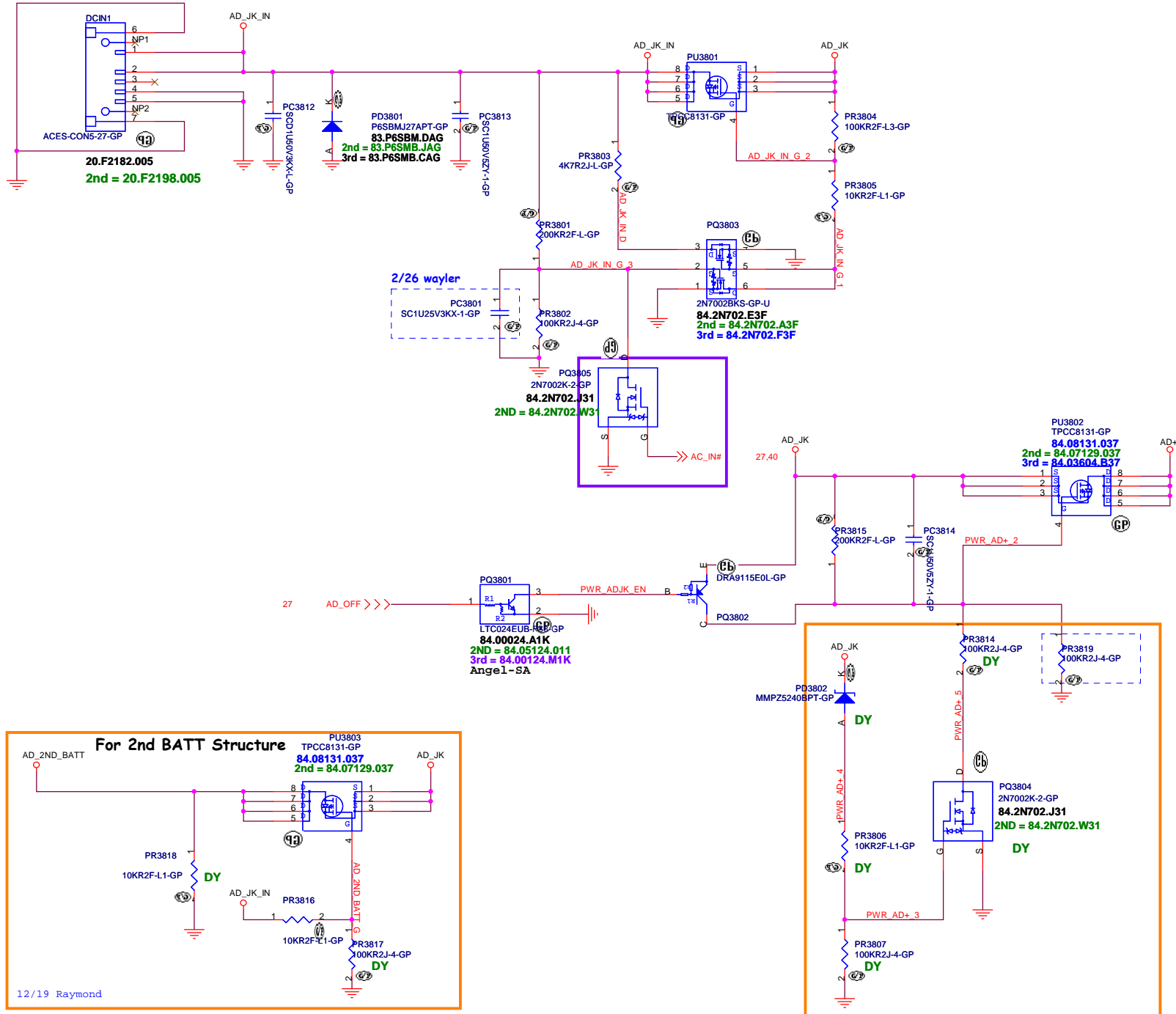
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Title		
<b>ADAPTER</b>		
Size A3	Document Number	Rev
	<b>Angel-CY</b>	<b>1</b>
Date: Monday, April 22, 2013	Sheet 37	of 102

# ANNIE solution

remember to check pin define

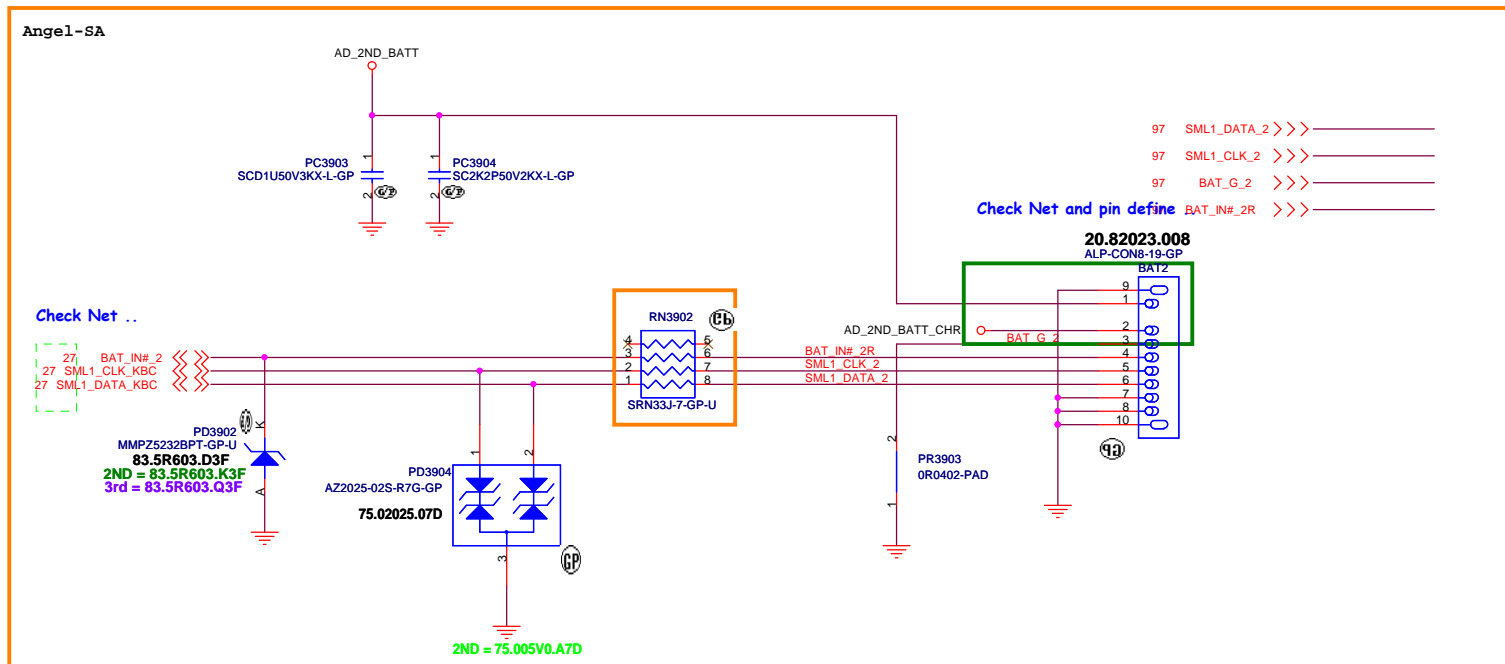
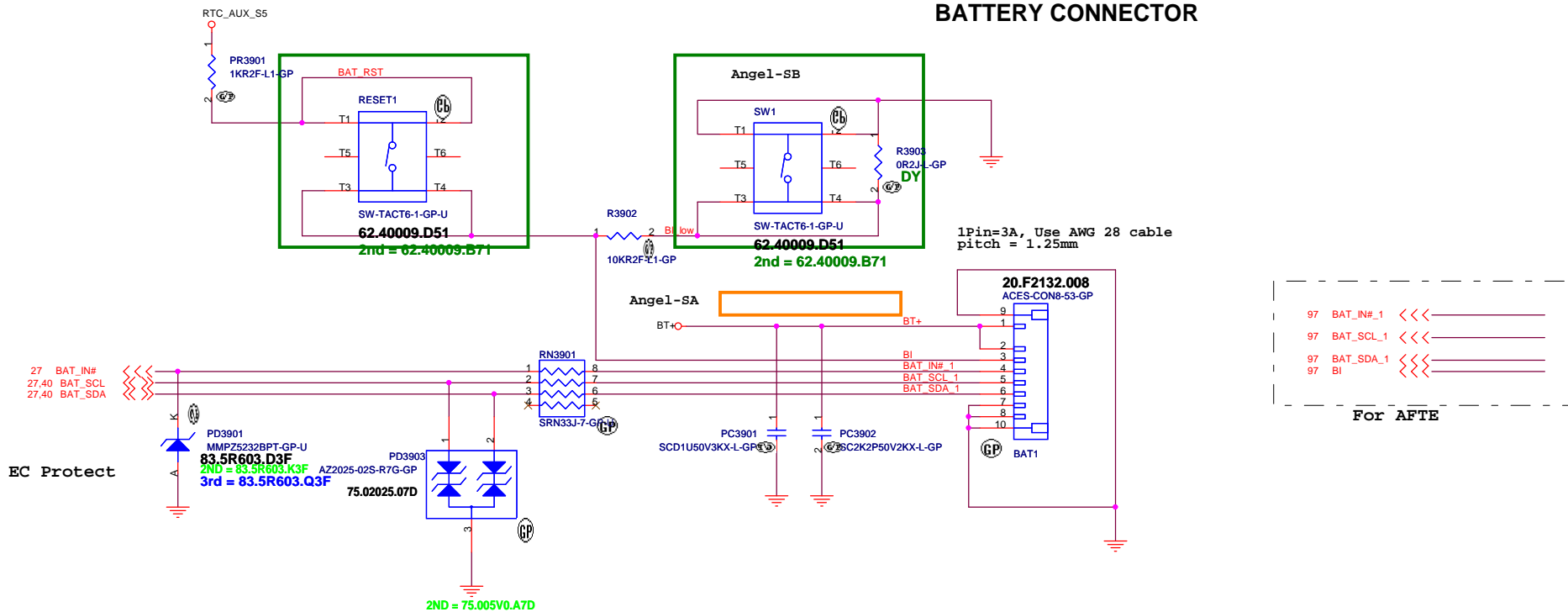
pitch = 2mm



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<b>DCIN JACK</b>	
Title <b>DCIN JACK</b>	Document Number <b>Angel-CY</b>
Size A3	Rev <b>1</b>
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# BATTERY CONNECTOR



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<Variant Name>

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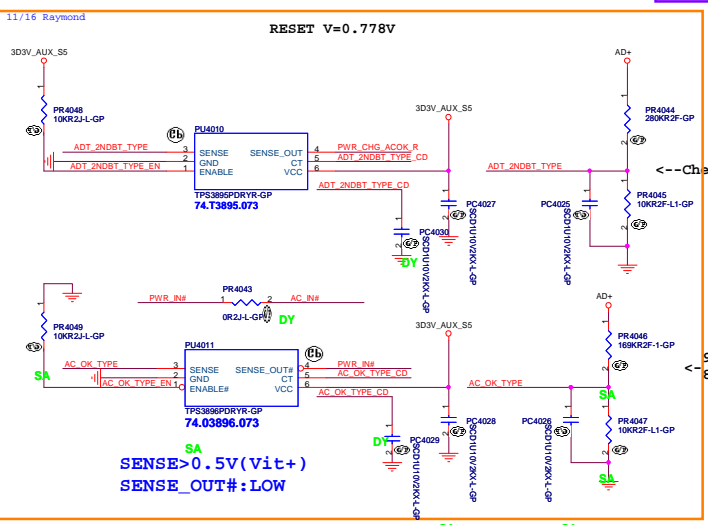
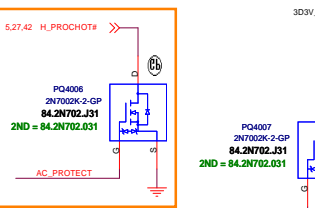
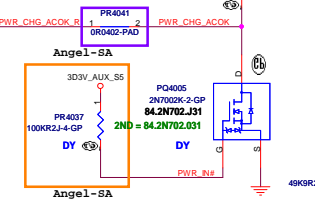
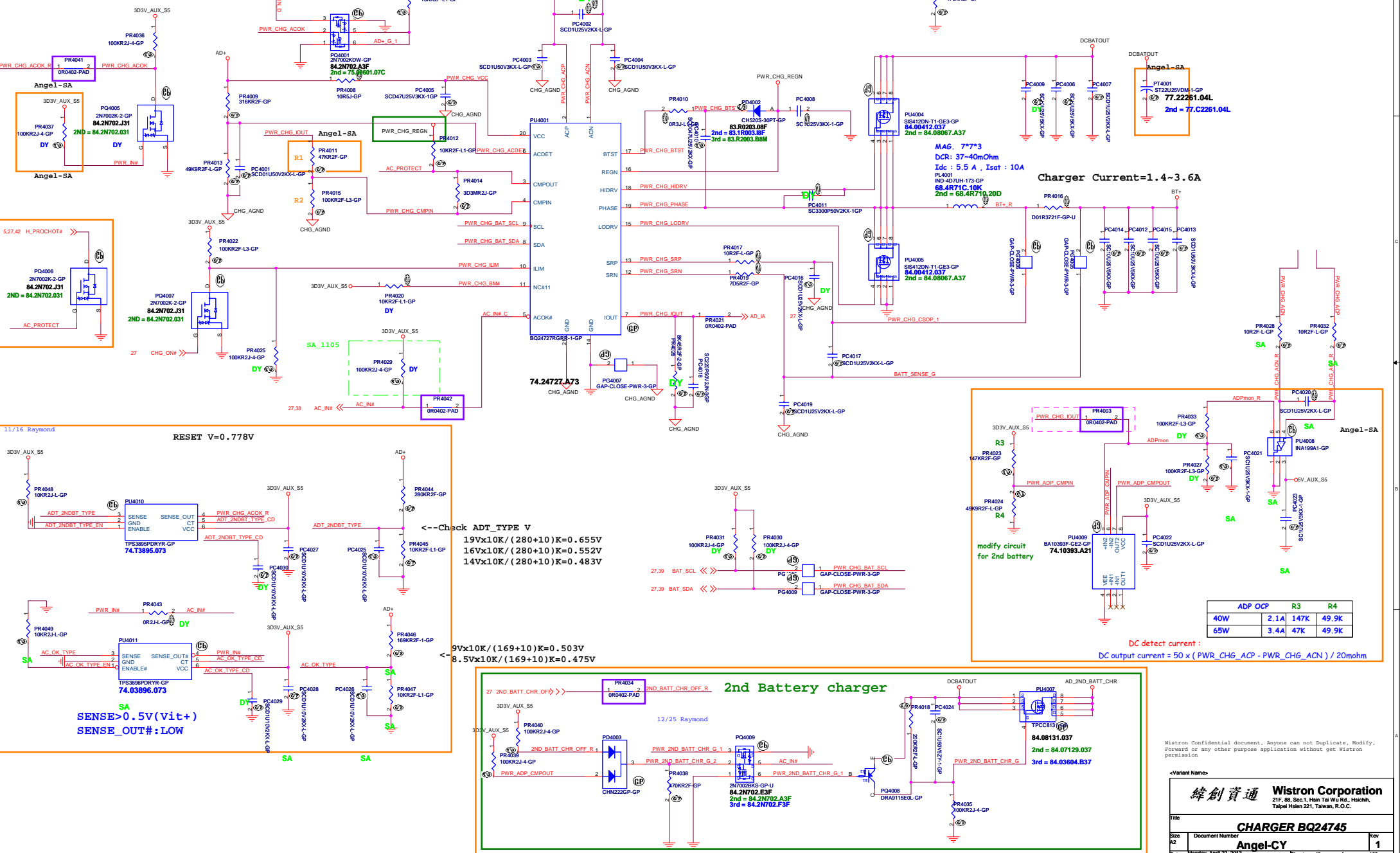
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Size: A3 Document Number: **Angel-CY** Rev: **1**

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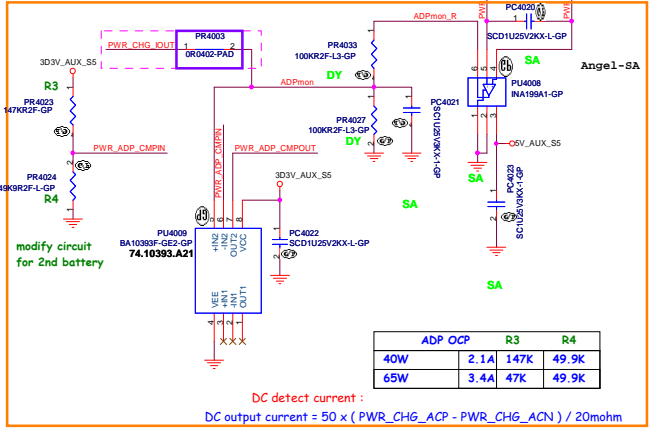
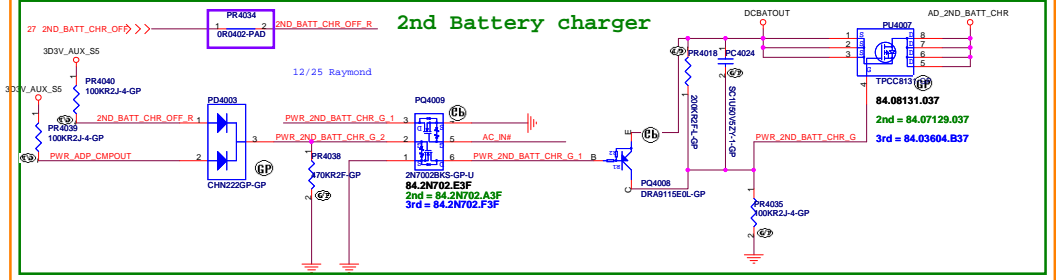
# SSID = Charger

AD+ total power	R1	R2
40w	47K	100K
65w	137K	100K



---Check ADT\_TYPE V  
 $19V \times 10K / (280+10)K = 0.655V$   
 $16V \times 10K / (280+10)K = 0.552V$   
 $14V \times 10K / (280+10)K = 0.483V$

$9V \times 10K / (169+10)K = 0.503V$   
 $8.5V \times 10K / (169+10)K = 0.475V$



ADP OCP	R3	R4
40W	2.1A	47K
65W	3.4A	47K

DC detect current :  
 DC output current =  $50 \times (PWR\_CHG\_ACP - PWR\_CHG\_ACN) / 20m\Omega$

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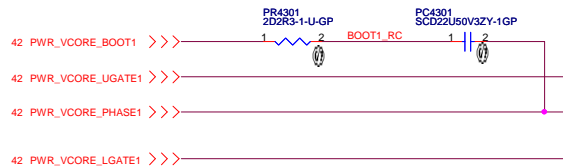
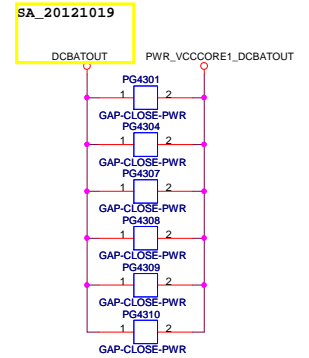
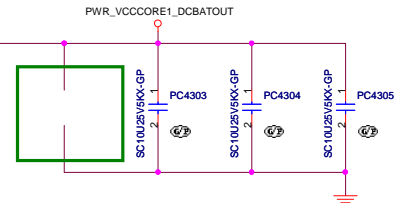
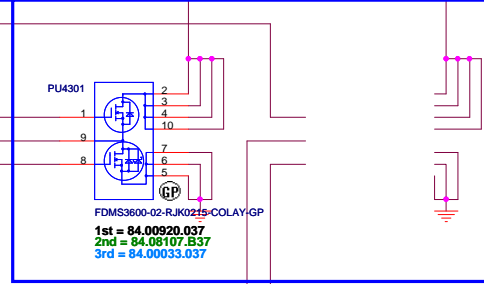




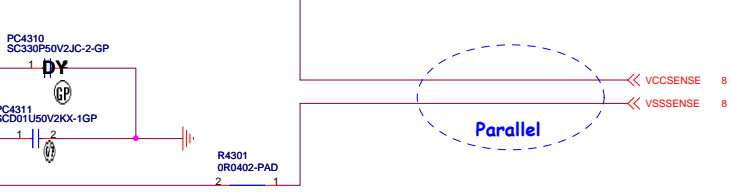
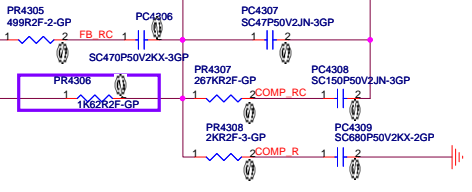
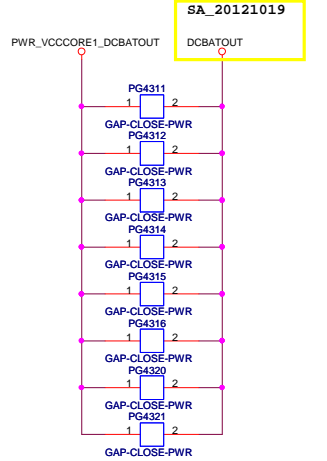
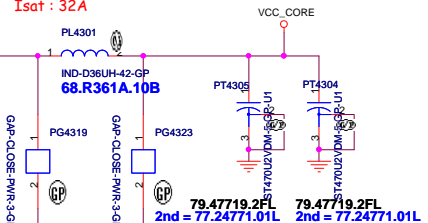
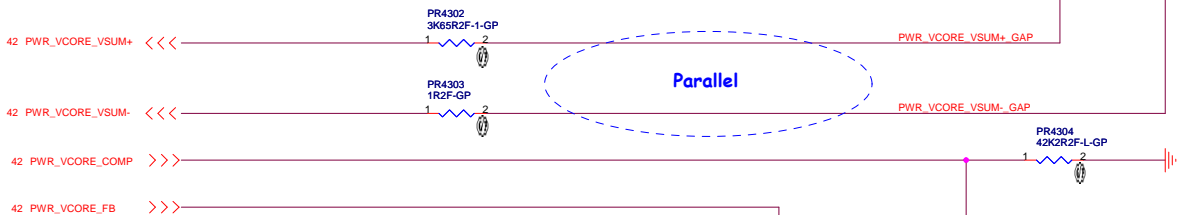
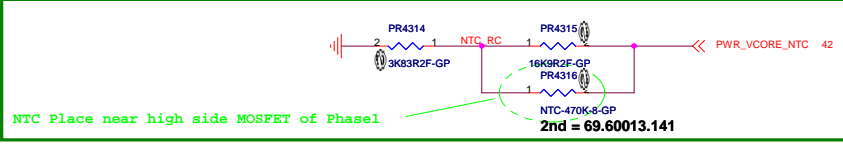
BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S)	Mount
PU4302	84.03664.037 (FDMS3664S)	DY

BOM control



Pana . 7 x 7 x 4  
DCR 1.8~2.3 mOhm  
Isat : 32A



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UMA C

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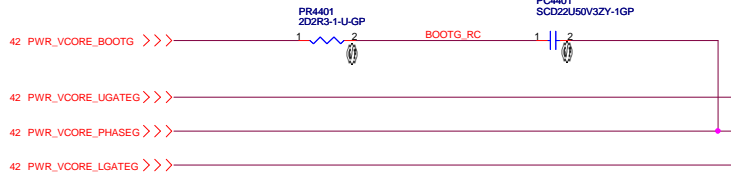
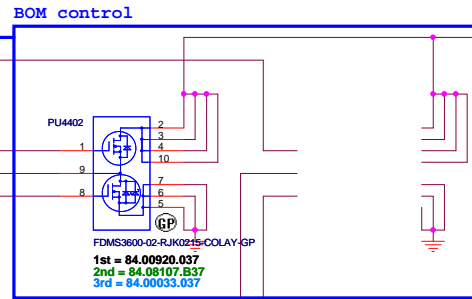
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Size: Custom Document Number Rev: 1

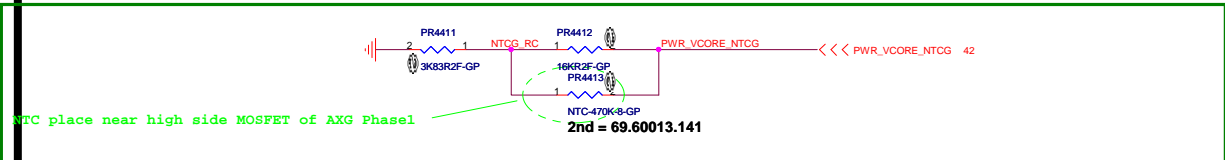
Date: Monday, April 22, 2013 Sheet: 43 of 103

**BOM control**

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S)	<b>Mount</b>
PU4402	84.03664.037 (FDMS3664S)	<b>DY</b>



Pana : 7 x 7 x 4  
DCR 1.8~2.3 mOhm  
Isat : 32A



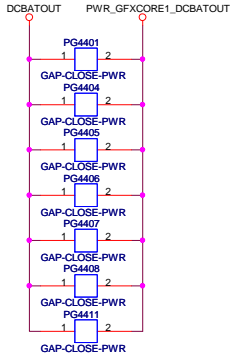
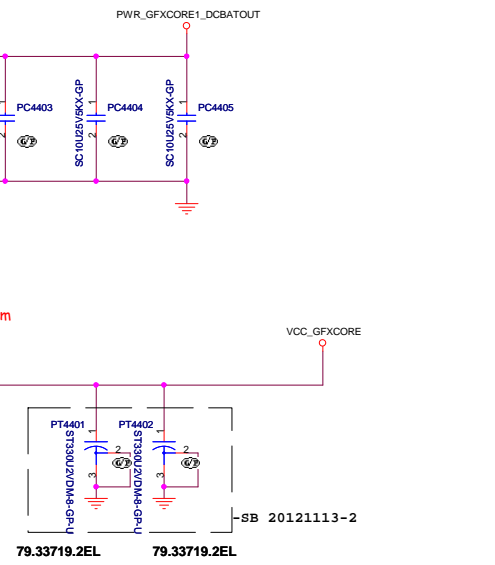
Parallel



AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

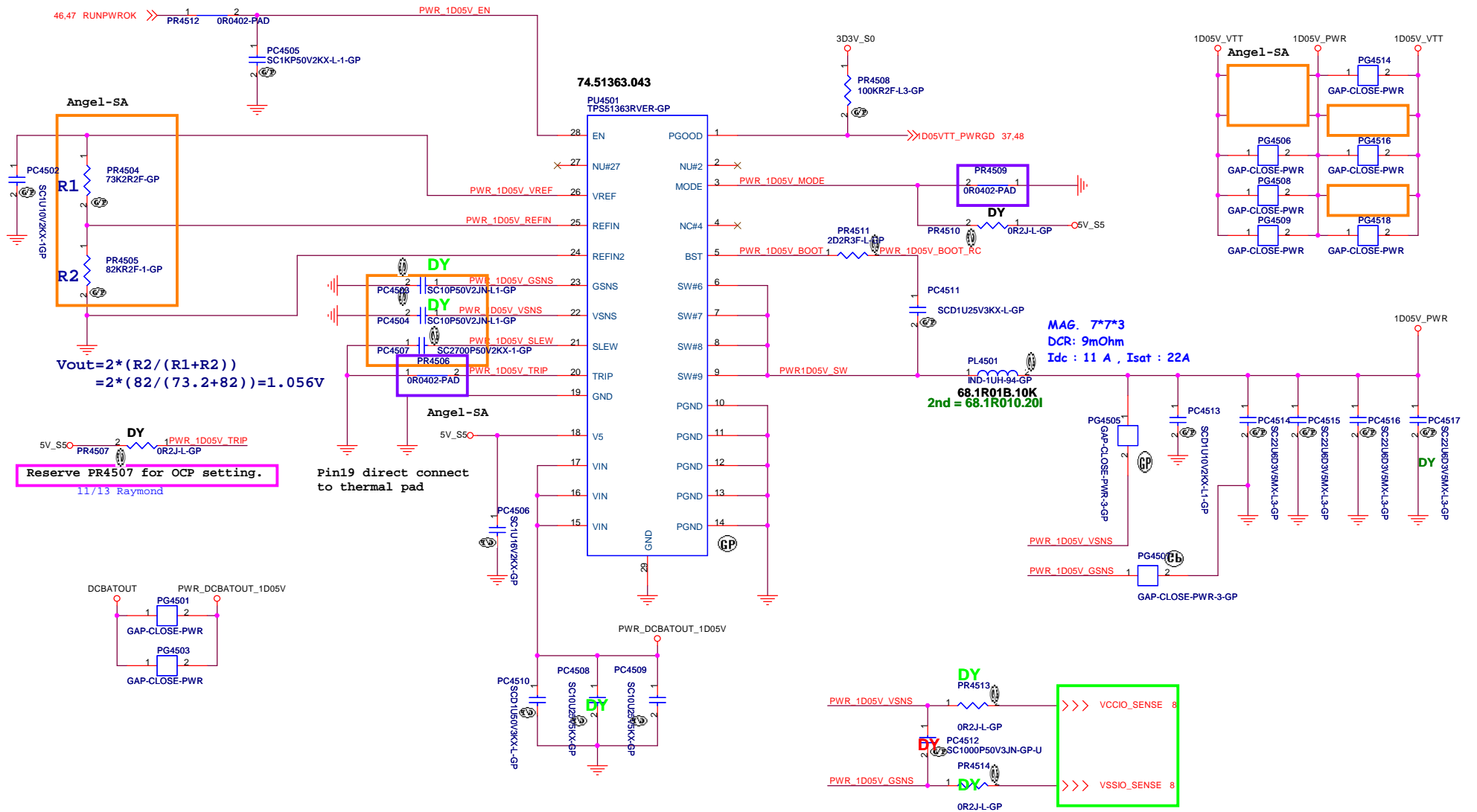


Parallel



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# TPS51363 for 1D05V

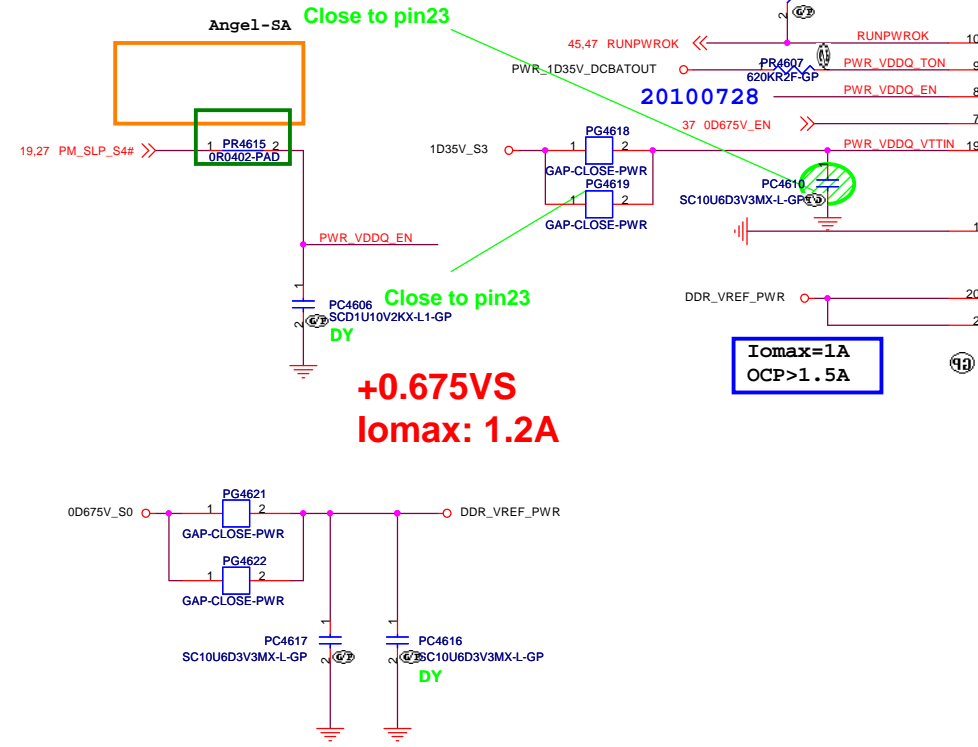
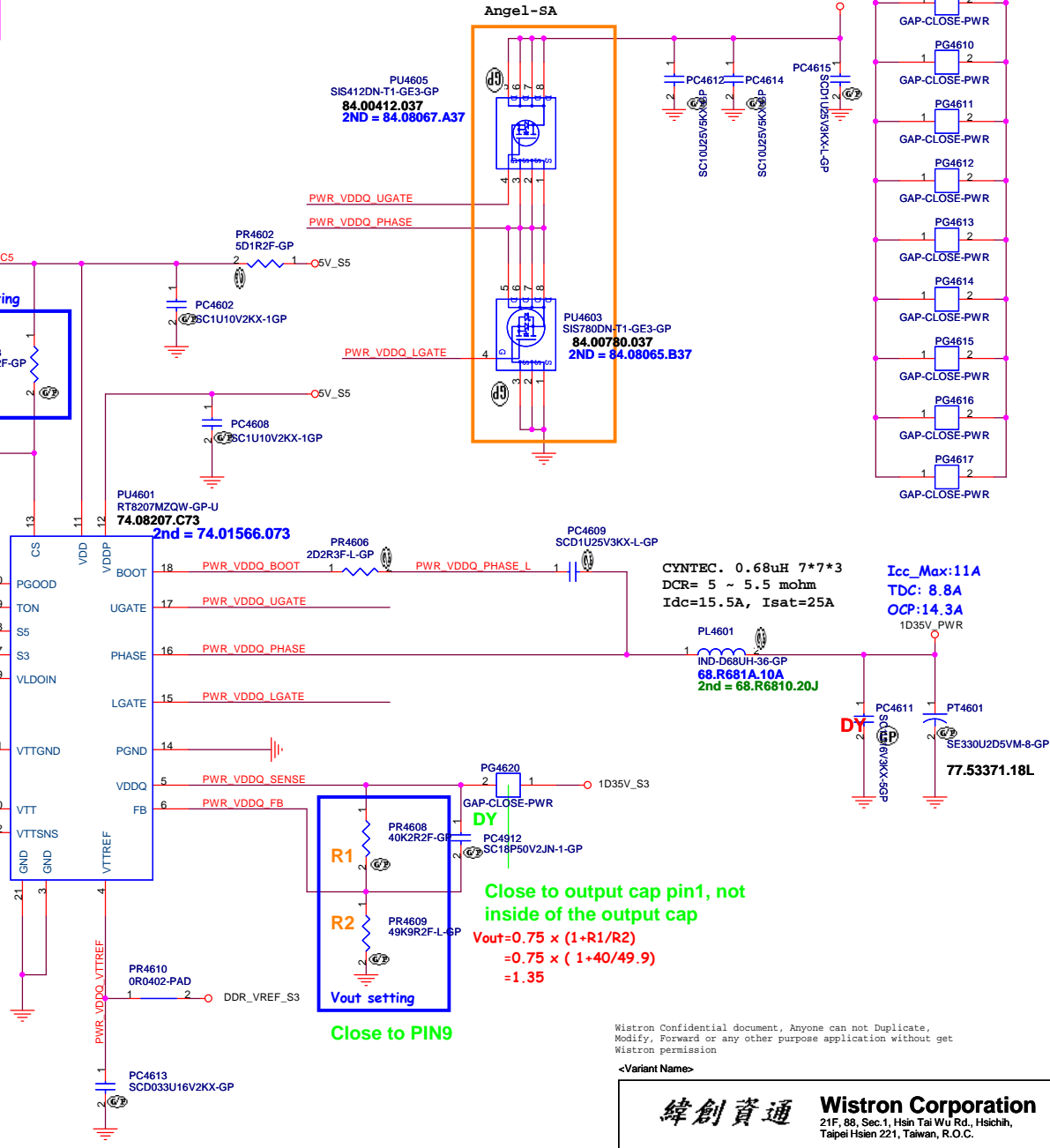
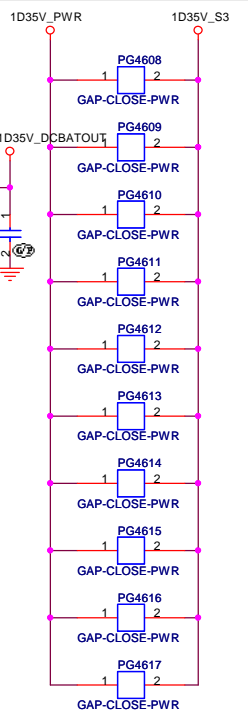
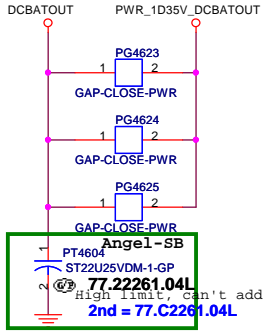


HR PX

緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

SSID = PWR.Plane.Regulator\_lp35v0p675v

# RT8207L for VDDQ



**+0.675VS**  
**Iomax: 1.2A**

**Iomax=1A**  
**OCP>1.5A**

**Close to output cap pin1, not inside of the output cap**  
 $V_{out} = 0.75 \times (1 + R1/R2)$   
 $= 0.75 \times (1 + 40/49.9)$   
 $= 1.35$

**CYNTEC. 0.68uH 7\*7\*3**  
**DCR= 5 ~ 5.5 mohm**  
**Idc=15.5A, Isat=25A**

**Icc\_Max:11A**  
**TDC: 8.8A**  
**OCP:14.3A**

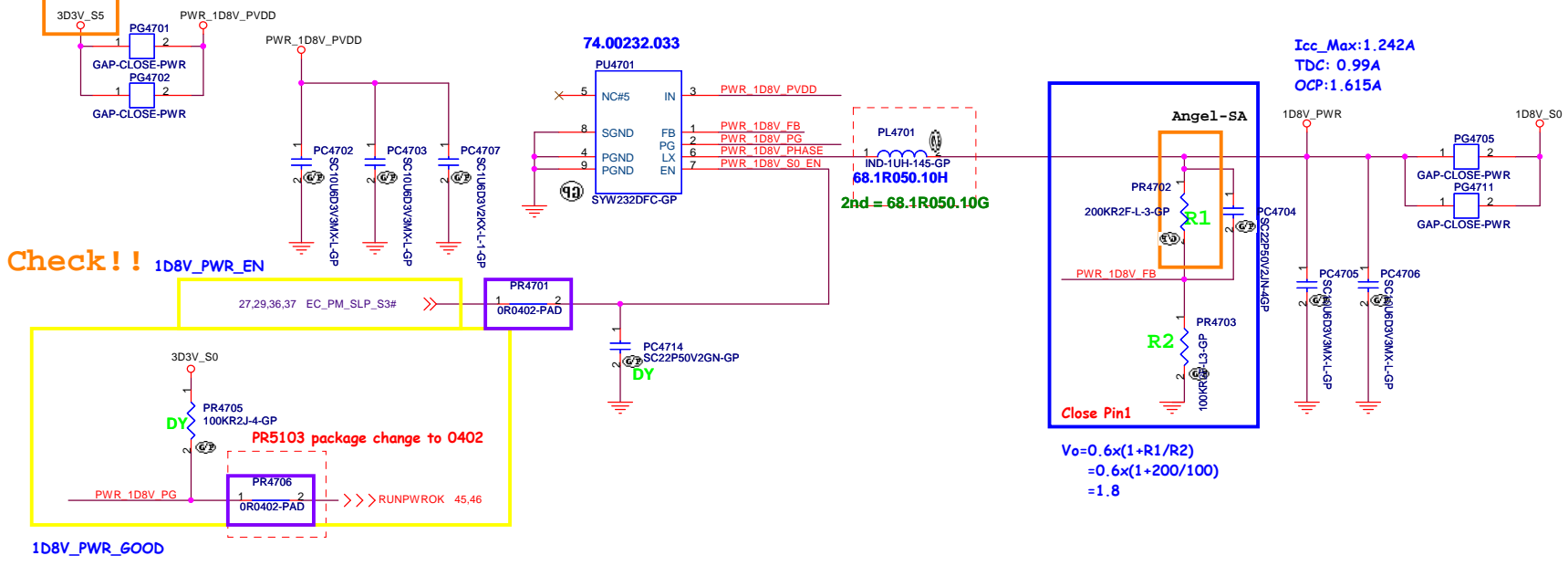
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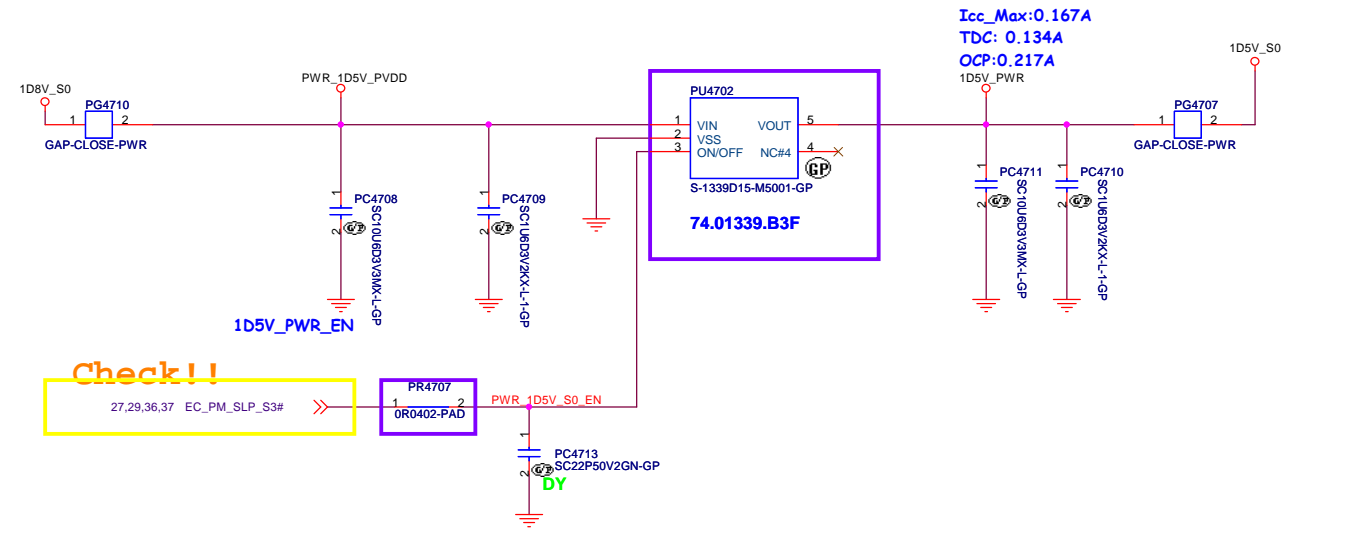
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>TPS51116 +1.5V SUS</b>		
Title	Document Number	Rev
	<b>Angel-CY</b>	<b>1</b>
Date: Monday, April 22, 2013	Sheet 46 of 102	

**SSID = PWR.Plane.Regulator\_1p8v**

Check!!



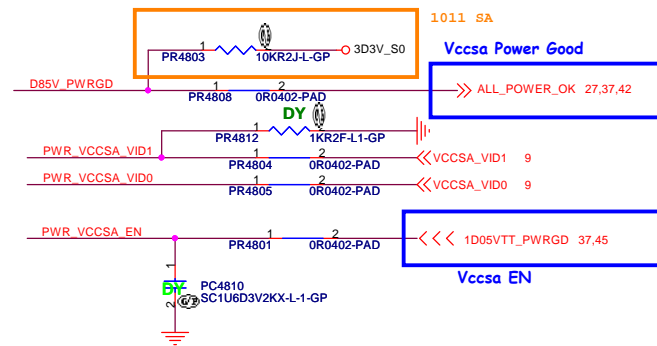
**S-1339D15 for +1.5V**



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Variant Name		
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<b>DC CONVERTER_1D8V&amp;1D5V</b>		
Title	Document Number	Rev
	<b>Angel-CY</b>	<b>1</b>
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# LDO G978 for VCCSA



D0, D1 V<sub>0</sub> Selection Table

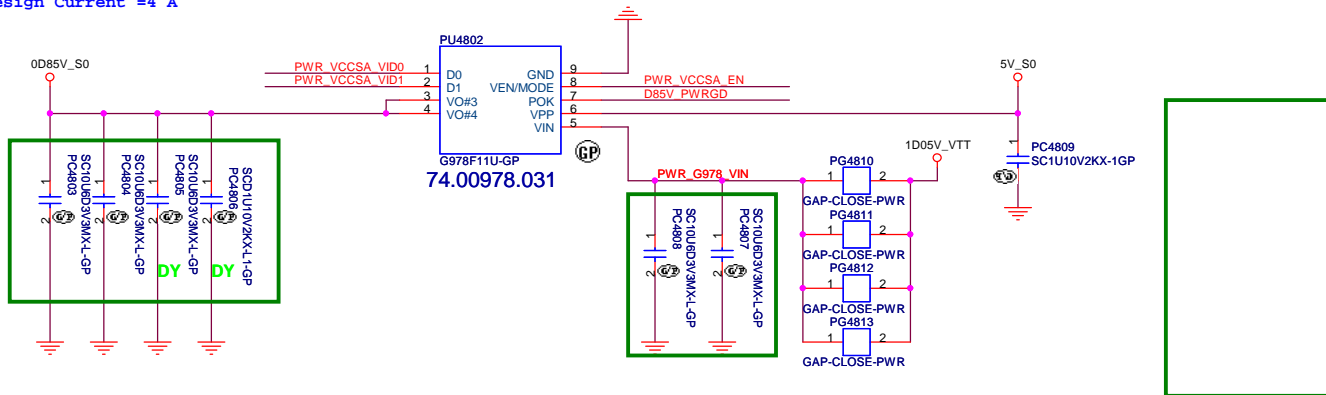
D0	D1	V <sub>0</sub> MODE=0	V <sub>0</sub> MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"x" means "don't care".

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

Design Current = 4 A



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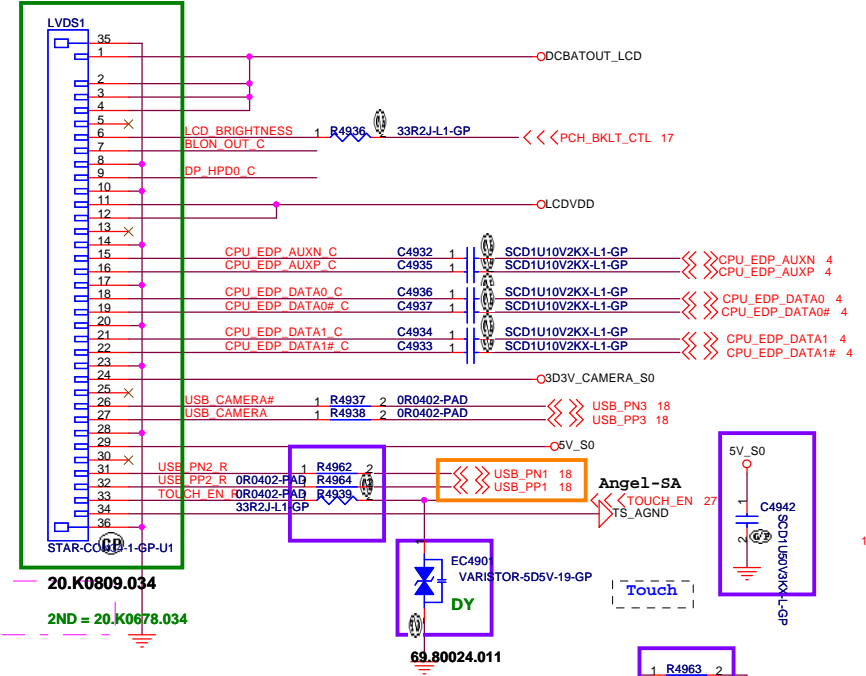
UMA C

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<b>VCCSA LDO G978</b>	
Size A3	Document Number <b>Angel-CY</b>
Date: Monday, April 22, 2013	Sheet 48 of 103



**SSID = VIDEO**

Angel-SA



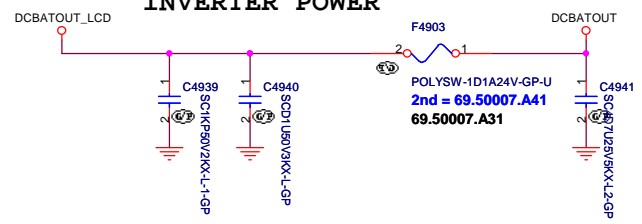
**J1 Pin Assignment**

1	USB5V
2	D-
3	D+
4	GND
5	GND
6	INT

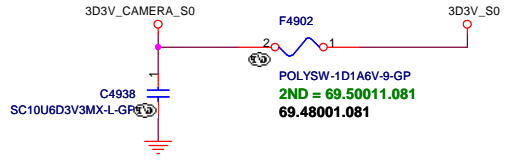
- 97 DP\_HPD0\_C >>> \_\_\_\_\_
- 97 BLON\_OUT\_C >>> \_\_\_\_\_
- 97 LCD\_BRIGHTNESS >>> \_\_\_\_\_
- 97 CPU\_EDP\_DATA1\_C >>> \_\_\_\_\_
- 97 CPU\_EDP\_DATA1#\_C >>> \_\_\_\_\_
- 97 CPU\_EDP\_DATA0\_C >>> \_\_\_\_\_
- 97 CPU\_EDP\_DATA0#\_C >>> \_\_\_\_\_
- 97 CPU\_EDP\_AUXP\_C >>> \_\_\_\_\_
- 97 CPU\_EDP\_AUXN\_C >>> \_\_\_\_\_

For AFTE

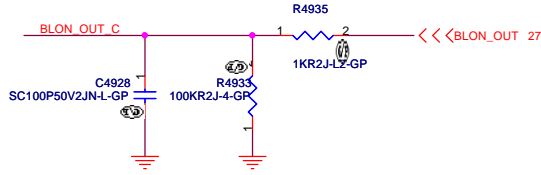
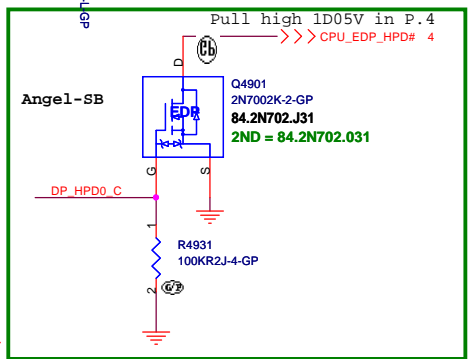
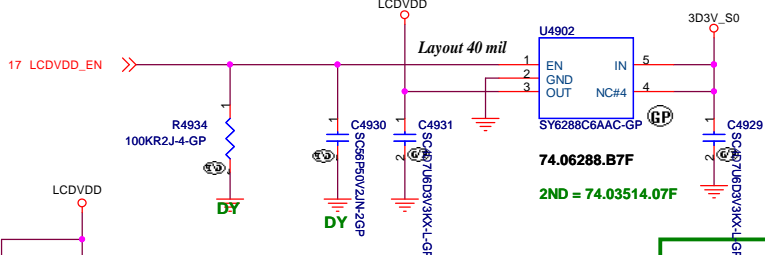
**INVERTER POWER**



**Camera Power**



Layout 40 mil



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<-Variant Name>

<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>LCD Connector</b>	
File	Rev 1
Size A3	Document Number
<b>Angel-CY</b>	
Date: Monday, April 22, 2013	Sheet 49 of 102

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<Variant Name>

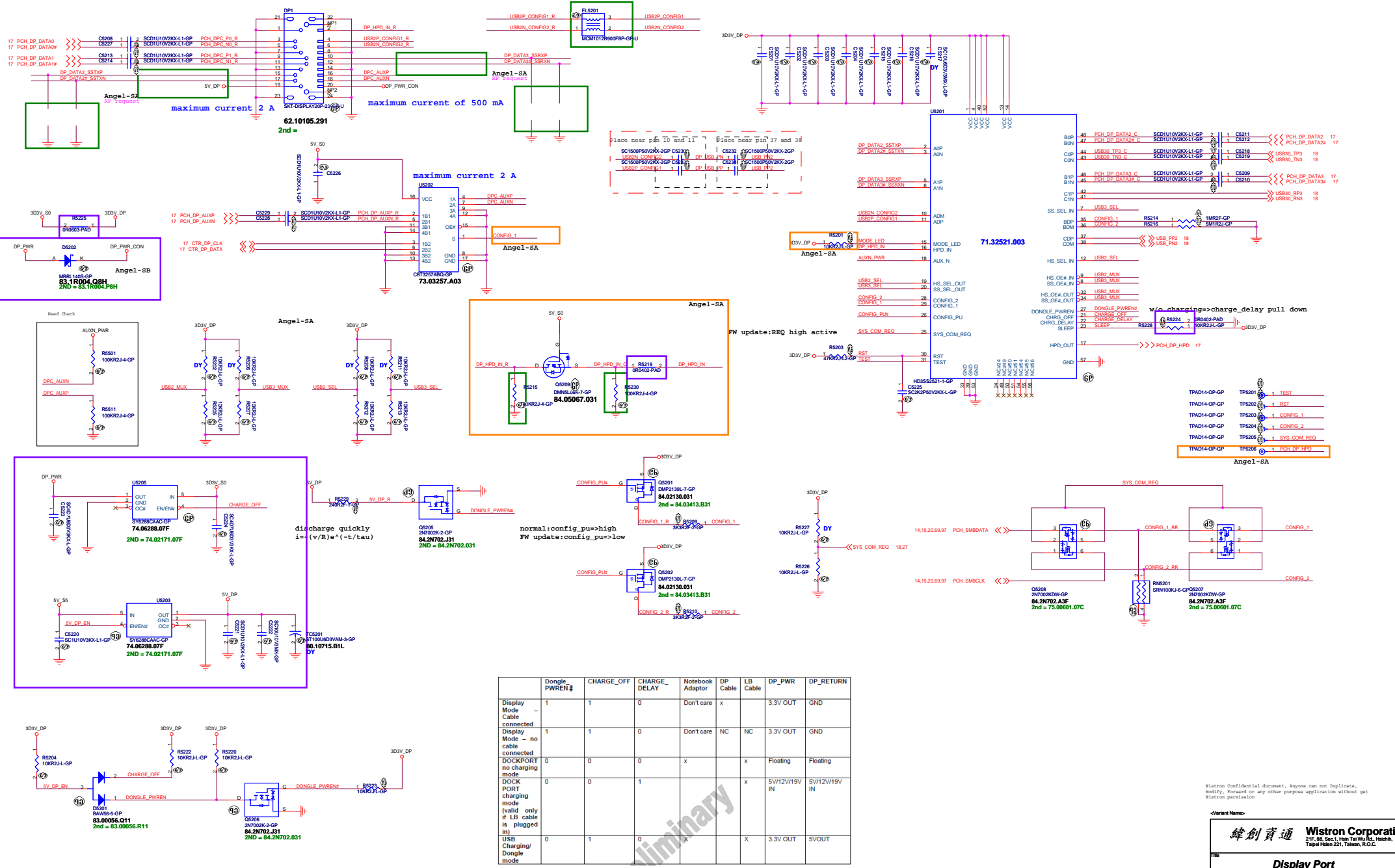
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>CRT Connector</b>			
<b>Size</b> A4	<b>Document Number</b> <b>Angel-CY</b>		<b>Rev</b> <b>1</b>
<b>Date:</b> Monday, April 22, 2013		<b>Sheet</b> 50	<b>of</b> 102

# HDMI Level Shifter & CONNECTOR

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Title					
<b>HDMI Level Shifter/Connector</b>					
Size	Document Number				Rev
A3	<b>Angel-CY</b>				<b>1</b>
Date:	Monday, April 22, 2013	Sheet	51	of	102



	Dongle PWREN#	CHARGE_OFF	CHARGE_DELAY	Notebook Adaptor	DP Cable	LB Cable	DP_PWR	DP_RETURN
Display Mode - Cable connected	1	1	0	Don't care	x	NC	3.3V OUT	GND
Display Mode - no cable connected	1	1	0	Don't care	NC	NC	3.3V OUT	GND
DOCKPORT no charging mode	0	0	0	x	x	Floating	Floating	Floating
DOCK PORT charging mode (valid only if LB cable is plugged in)	0	0	1		x	5V/12V/19V IN	5V/12V/19V IN	
USB Charging/ Dongle mode	0	1	0		X	3.3V OUT	5VOUT	

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Title			
<b>S-VIDEO</b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013	Sheet 54 of	102

SSID = User.Interface

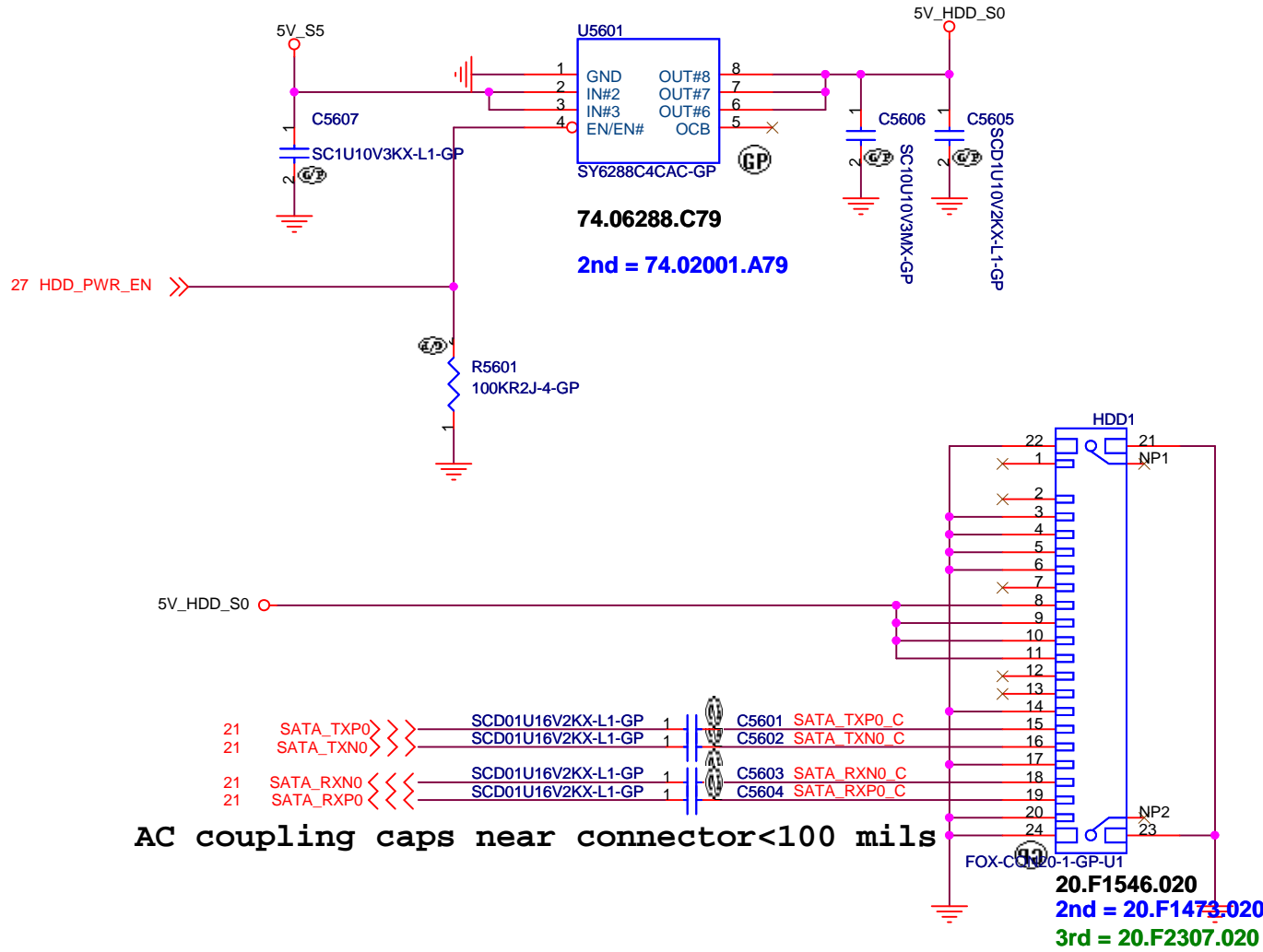
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Title			
<b>ITP</b>			
Size A4	Document Number <b>Angel-CY</b>		Rev <b>1</b>
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# SATA HDD Connector



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Title <b>HDD</b>		
Size A4	Document Number <b>Angel-CY</b>	Rev <b>1</b>
Date: Monday, April 22, 2013	Sheet 56 of	102



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Title			
<b>E-SATA/USB CHARGER</b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013		Sheet 57 of 102

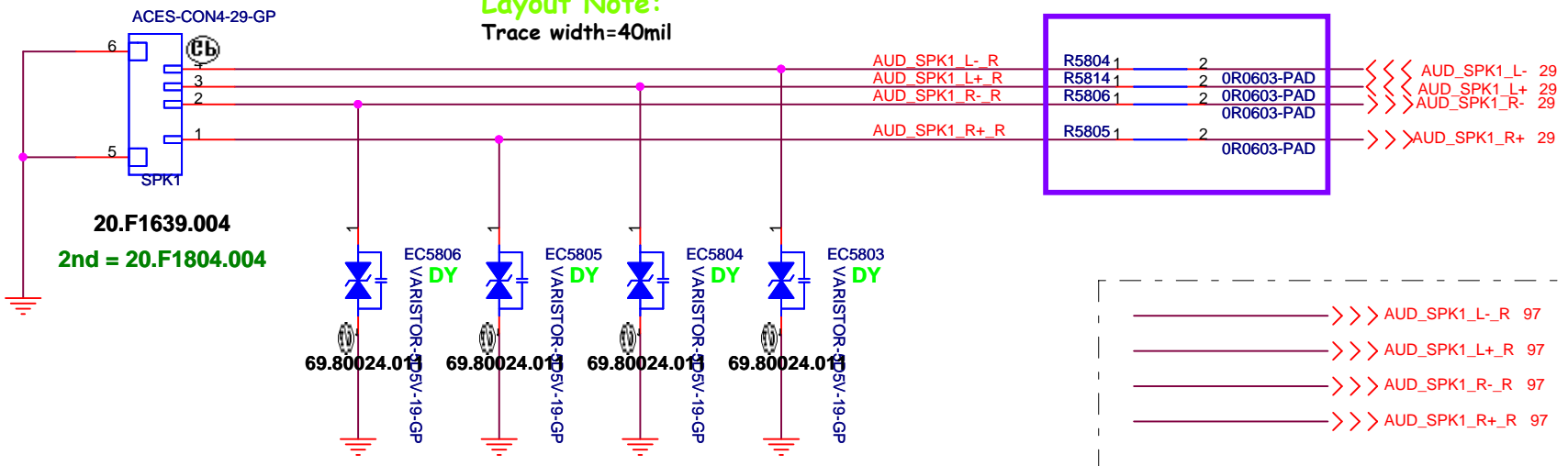
**SSID = AUDIO**

**SSID = AUDIO**

*Speaker*

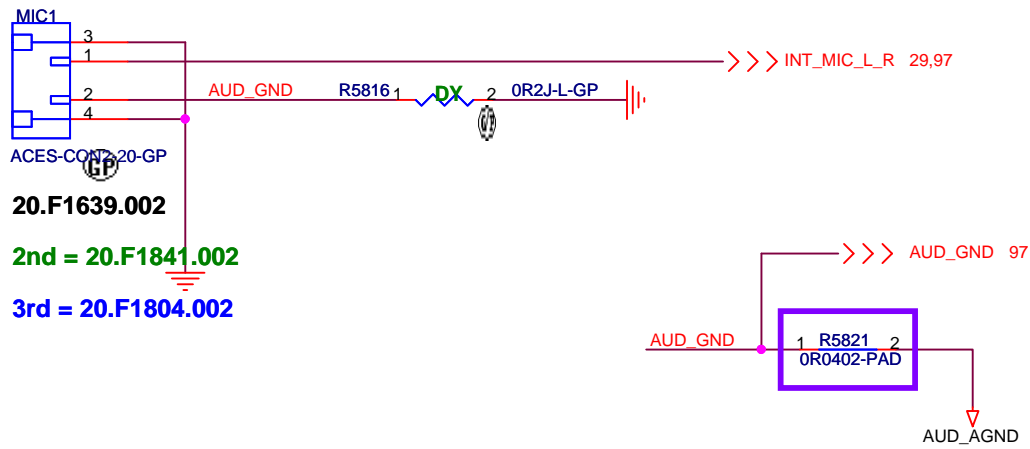
SA  
10/22 change by Edwin  
Pin Define SWAP

**Layout Note:**  
Trace width=40mil



For AFTE

*Combo Jack on Small Board*



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<b>MIC/SPEAKER/JACK</b>			
Size A4	Document Number		Rev
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

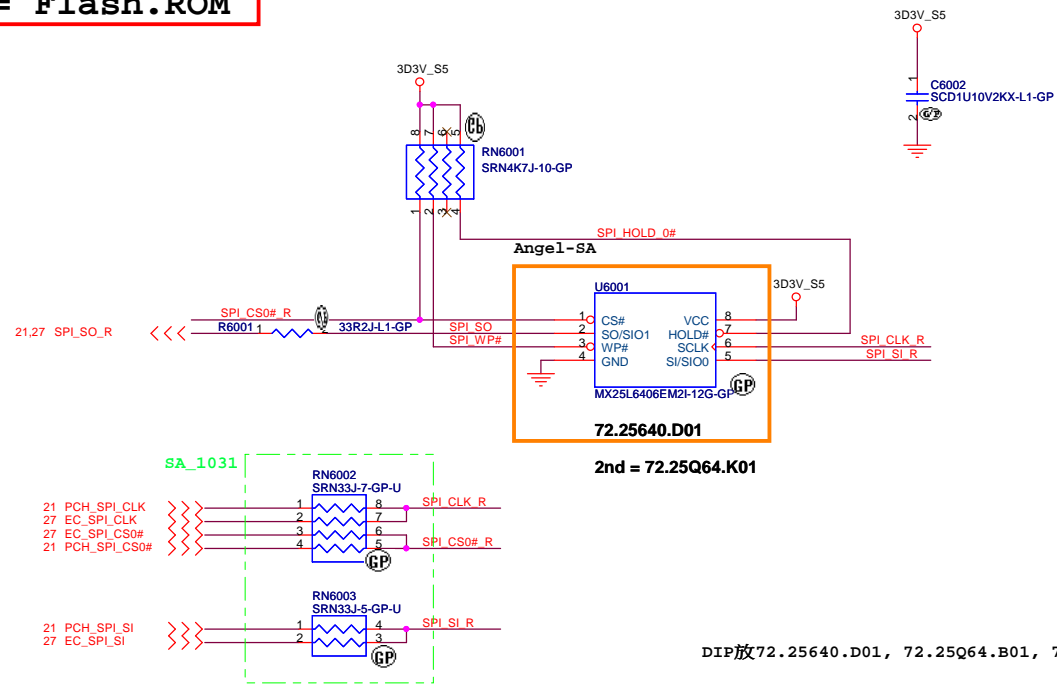
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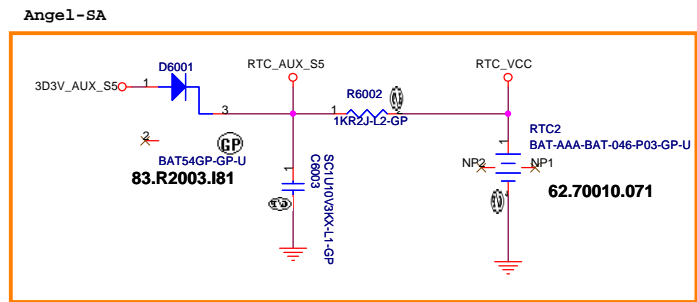
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
<b>LAN CONNECTOR</b>		
Size A4	Document Number <b>Angel-CY</b>	Rev <b>1</b>
Date: Monday, April 22, 2013		Sheet 59 of 102

**SSID = Flash.ROM**



**SSID = RBATT**



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<Variant Name>

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<p>Title <b>Flash/RTC</b></p>	
Size	Document Number
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Rev	<b>1</b>

**SSID = USB**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB Power SW**

Size  
A4

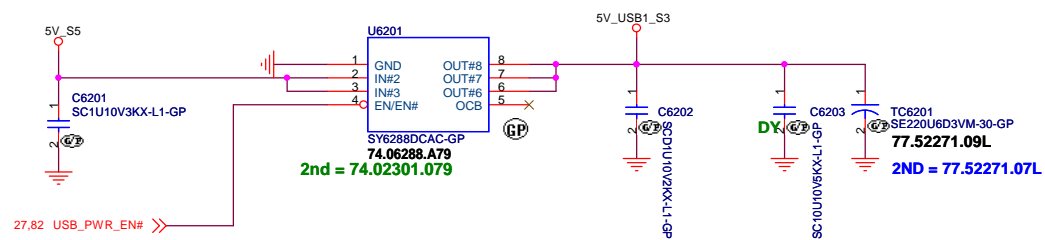
Document Number

**Angel-CY**

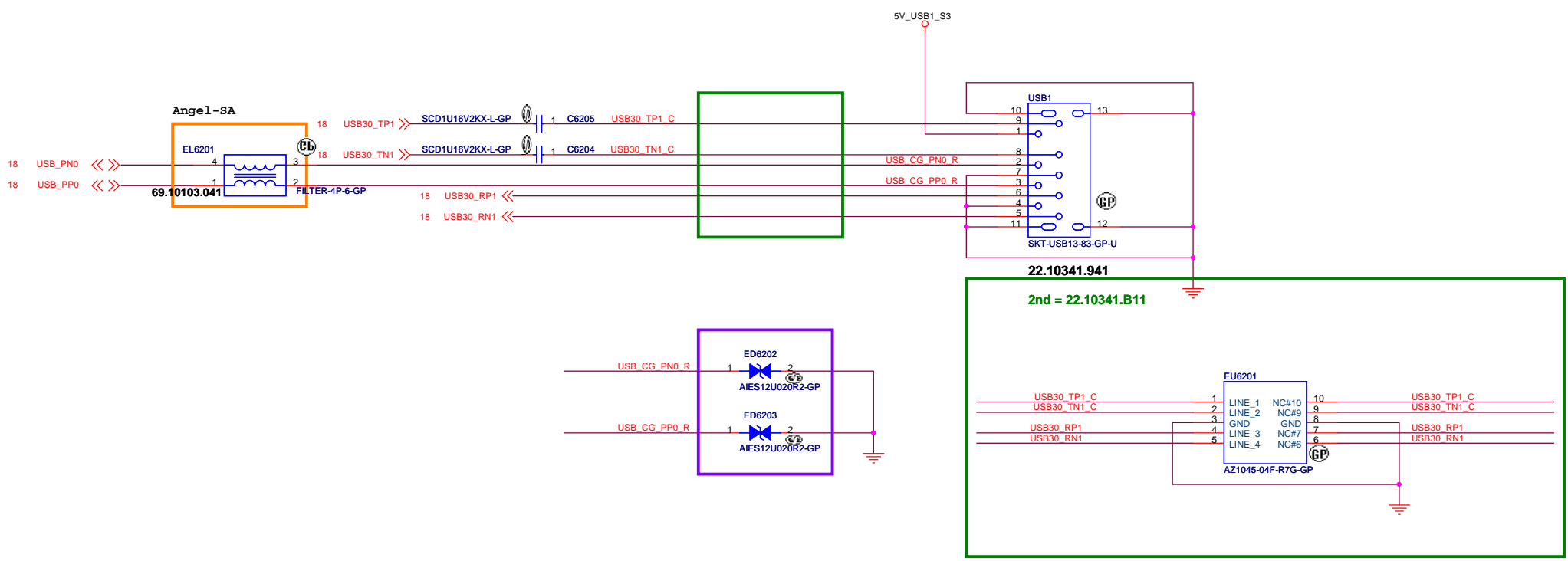
Rev  
**1**

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USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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<b>USB 3.0 Port</b>	
Title	Rev
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5 4 3 2 1

**SSID = User.Interface**  
Bluetooth Module conn.

Without BT

Blanking

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Title <b>Bluetooth</b>		
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<b>RESERVED</b>			
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SSID = Wireless

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<b>Title</b>			
<b>WWAN Connector</b>			
<b>Size</b> A4	<b>Document Number</b> <b>Angel-CY</b>		<b>Rev</b> <b>1</b>
<b>Date:</b> Monday, April 22, 2013		<b>Sheet</b> 66	<b>of</b> 102

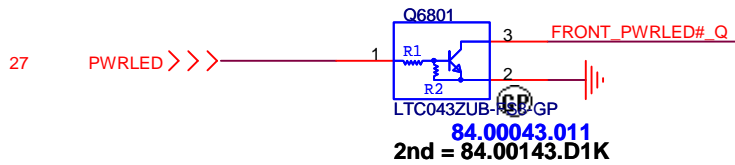
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<Variant Name>

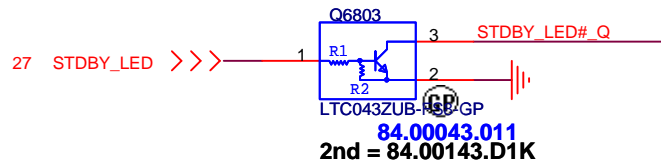
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Title</b> <b>M-SATA</b>		
<b>Size</b> A4	<b>Document Number</b> <b>Angel-CY</b>	<b>Rev</b> <b>1</b>
<b>Date:</b> Monday, April 22, 2013		<b>Sheet</b> 67 <b>of</b> 102

**SSID = User.Interface**

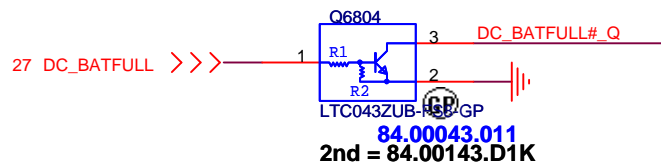
## Power button LED



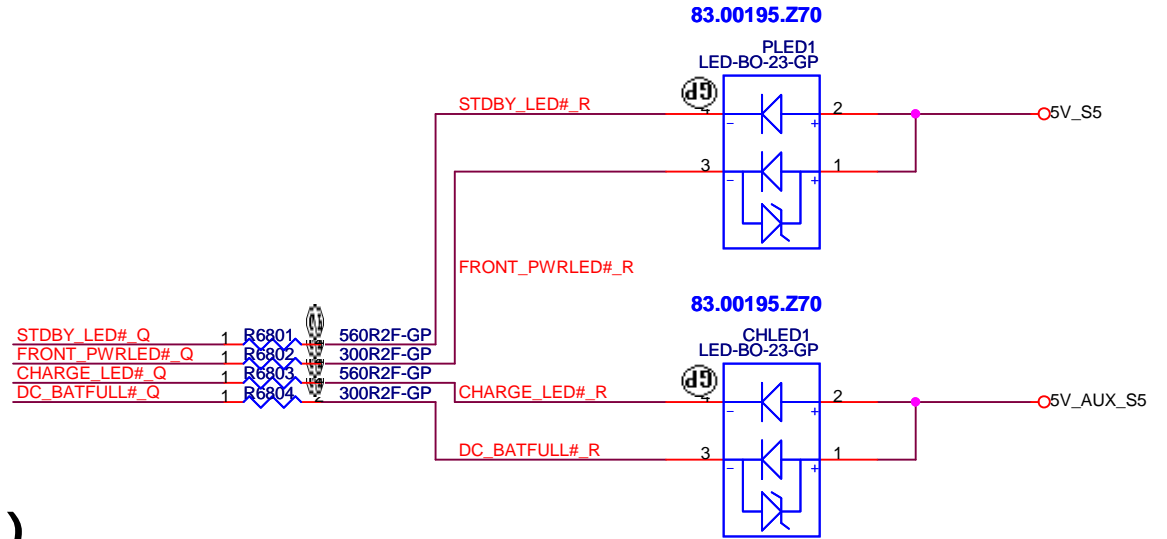
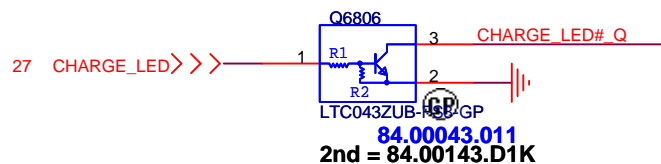
## Power STDBY\_LED



## Battery LED2 (DC\_BATFULL)



## Battery LED1 (CHARGE)



### Devices

Part No.	Lens	Source Color	Pin Assignment
LTST-C195ZBKFKT	Water Clear	InGaN Blue	1,3
		AllnGaP Orange	2,4

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<Variant Name>

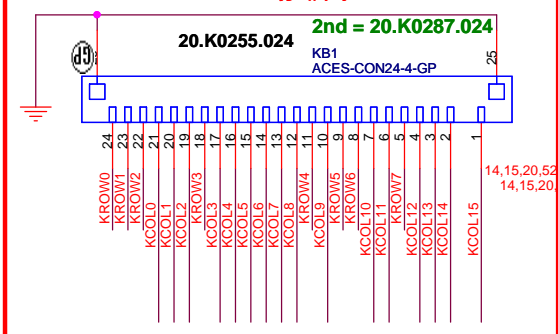
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>LED Bard/Power Button</b>			
Size A4	Document Number <b>Angel-CY</b>		Rev <b>1</b>
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# TOUCH PAD

D = KBC

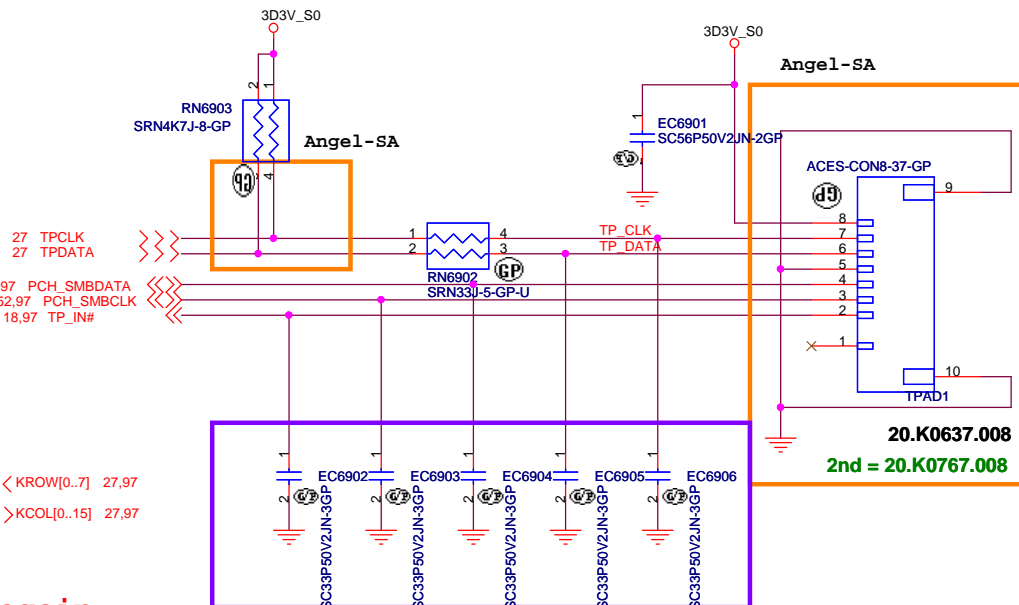
## Internal KeyBoard Connector

上接觸



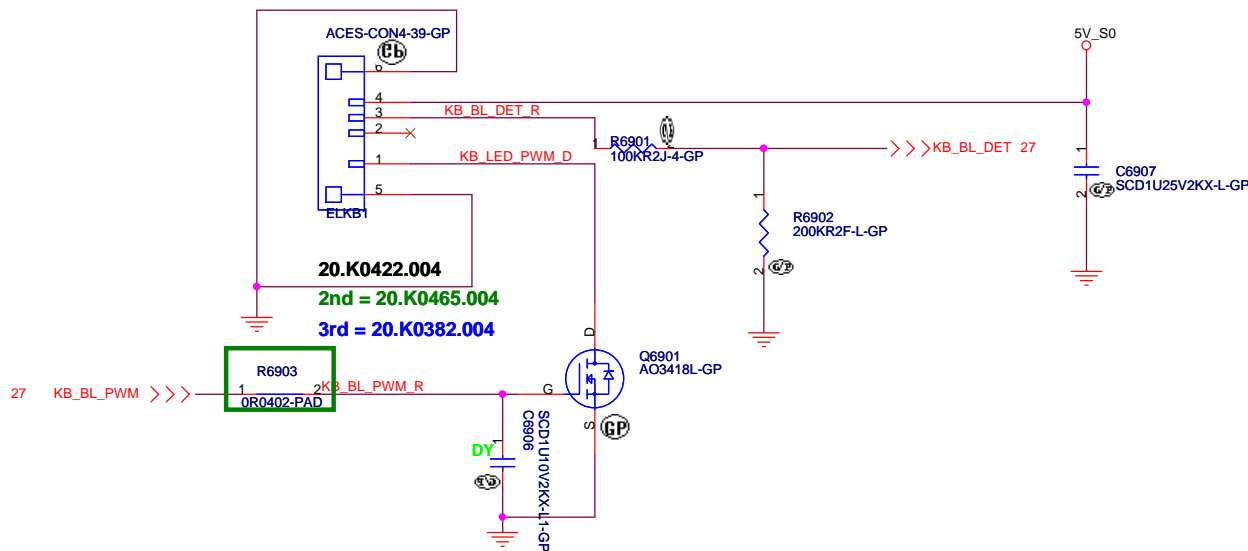
<<< KROW[0..7] 27,97  
>>> KCOL[0..15] 27,97

KB Pin define need to check again



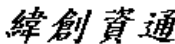
- 27,97 KCOL0 >>>
- 27,97 KCOL1 >>>
- 27,97 KCOL2 >>>
- 27,97 KCOL3 >>>
- 27,97 KCOL4 >>>
- 27,97 KCOL5 >>>
- 27,97 KCOL6 >>>
- 27,97 KCOL7 >>>
- 27,97 KCOL8 >>>
- 27,97 KCOL9 >>>
- 27,97 KCOL10 >>>
- 27,97 KCOL11 >>>
- 27,97 KCOL12 >>>
- 27,97 KCOL13 >>>
- 27,97 KCOL14 >>>
- 27,97 KCOL15 >>>
  
- 27,97 KROW0 >>>
- 27,97 KROW1 >>>
- 27,97 KROW2 >>>
- 27,97 KROW3 >>>
- 27,97 KROW4 >>>
- 27,97 KROW5 >>>
- 27,97 KROW6 >>>
- 27,97 KROW7 >>>
- 97 TP\_DATA >>>
- 97 TP\_CLK >>>

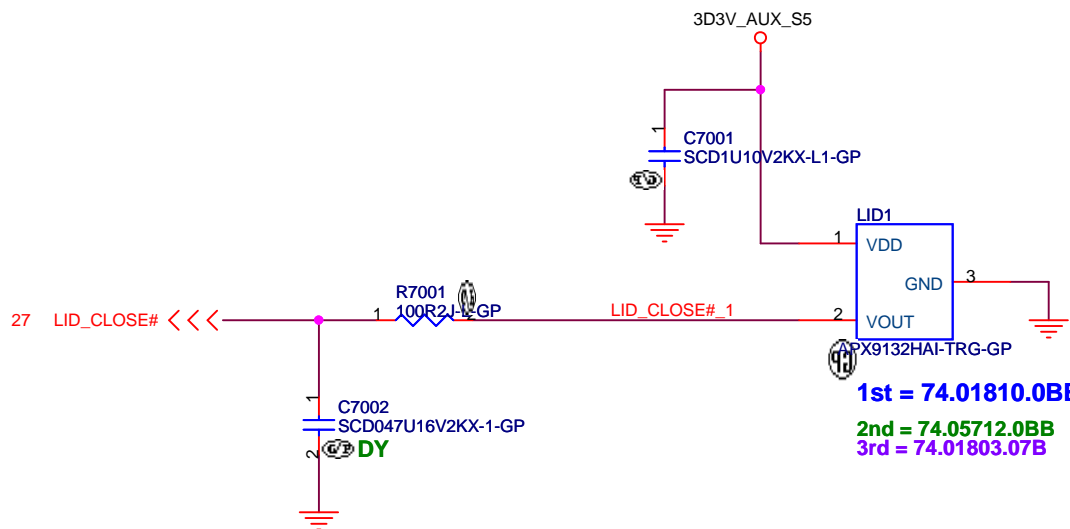
For AFTE



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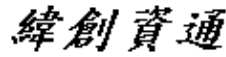
<Variant Name>

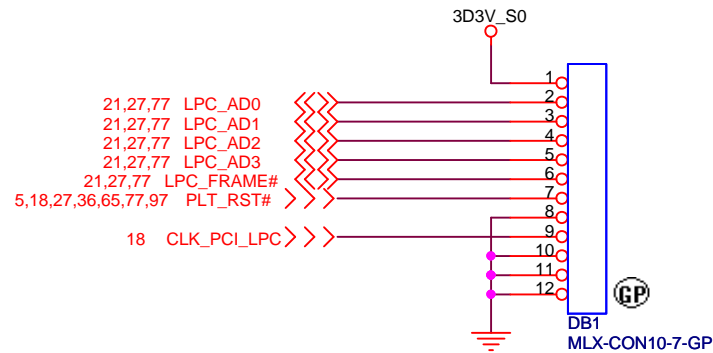
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Key Board/Touch Pad</b>		
Size	Document Number	Rev
Custom	<b>Angel-CY</b>	<b>1</b>
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<Variant Name>

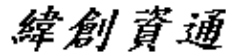
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Hall Sensor</b>		
Size A4	Document Number <b>Angel-CY</b>	Rev <b>1</b>
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**DB**  
**1st = 20.F0714.010**

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<b>Title</b> <i>Dubug connector</i>		
<b>Size</b> A4	<b>Document Number</b> <b>Angel-CY</b>	<b>Rev</b> <b>1</b>
<b>Date:</b> Monday, April 22, 2013		<b>Sheet</b> 71 <b>of</b> 102

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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013	Sheet 72 of	102



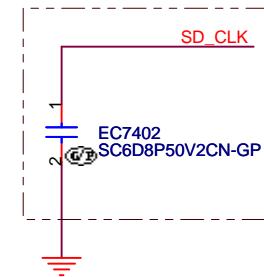
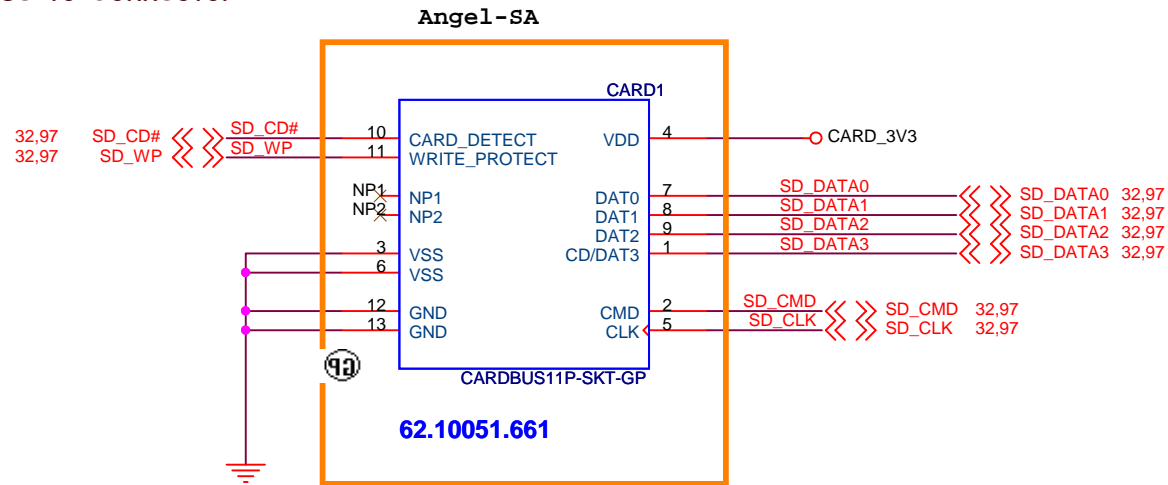
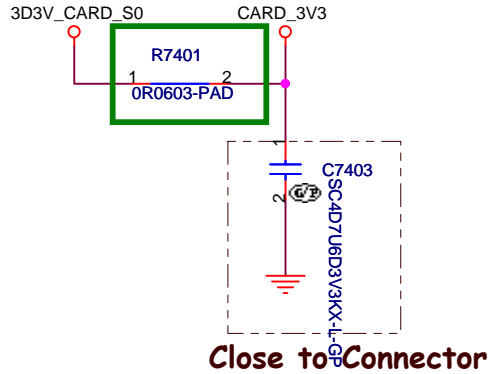
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<Variant Name>

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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>Angel-CY</b>		<b>1</b>
Date:	Monday, April 22, 2013		Sheet 73 of 102

# SD/XD/MS Card Reader



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<Variant Name>

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<b>Card Reader CONN</b>		
Size A4	Document Number <b>Angel-CY</b>	Rev <b>1</b>
Date: Monday, April 22, 2013		Sheet 74 of 102

SSID = ExpressCard

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<Variant Name>

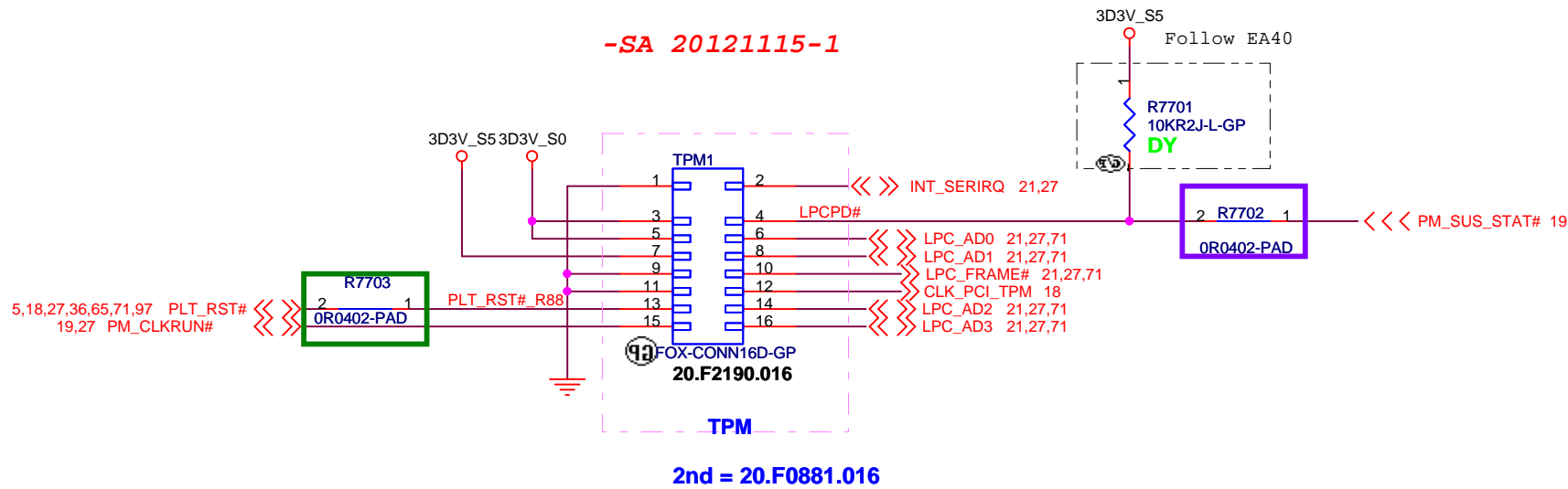
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>New Card</b>			
Size	Document Number	Rev	
A4	<b>Angel-CY</b>	<b>1</b>	
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Title <b>Reserved</b>		
Size A4	Document Number <b>Angel-CY</b>	Rev <b>1</b>
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**SSID - User Interface**

**Free Fall Sensor**

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Note

- no via trace under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

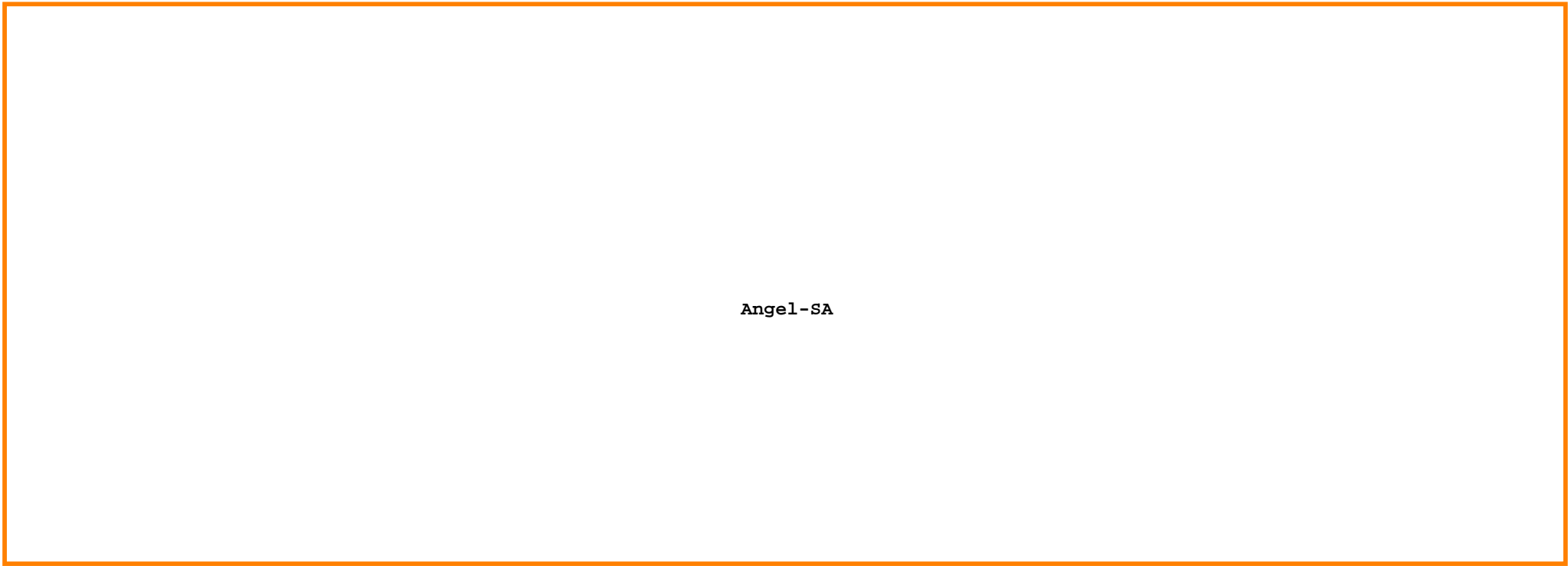
Note

- 1) Keep all signals are the same trace width. (included VDD, GND).
- 2) No VIA under IC bottom.

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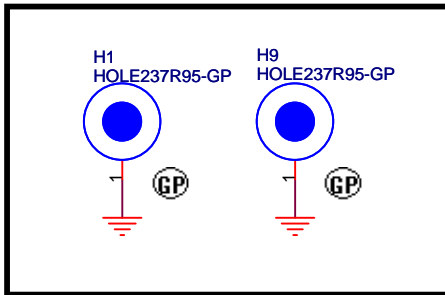
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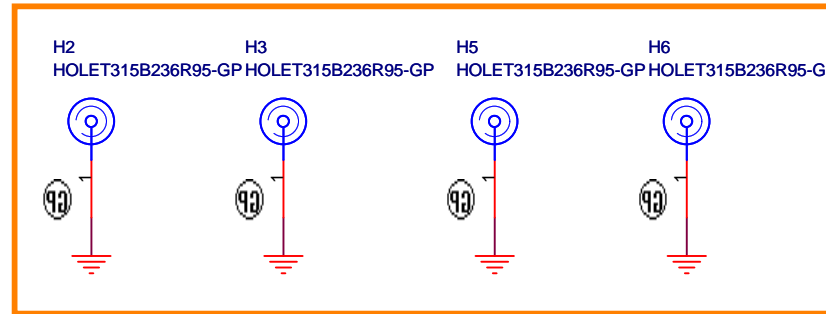
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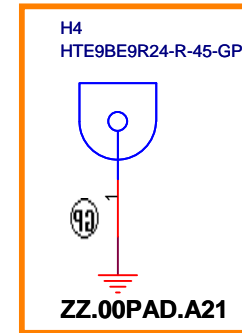
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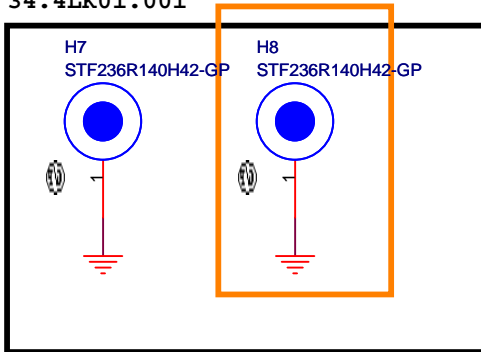


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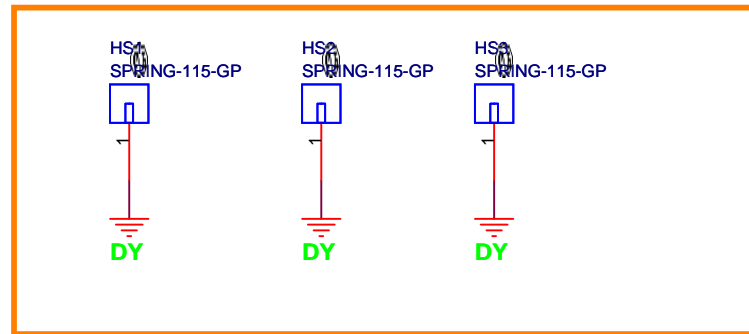
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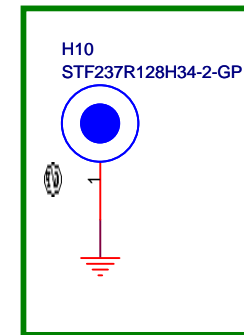


34.4PT16.001

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H10  
STF237R128H34-2-GP



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Title

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Size  
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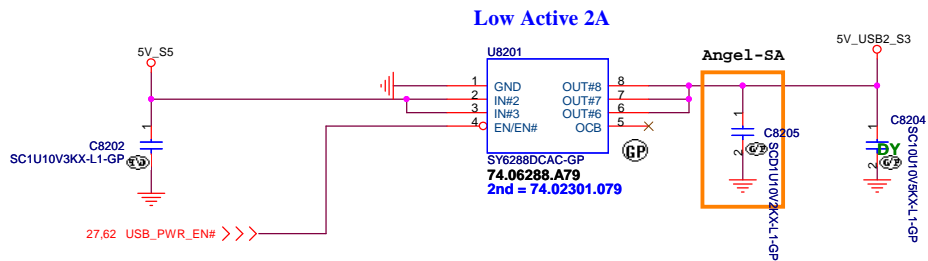
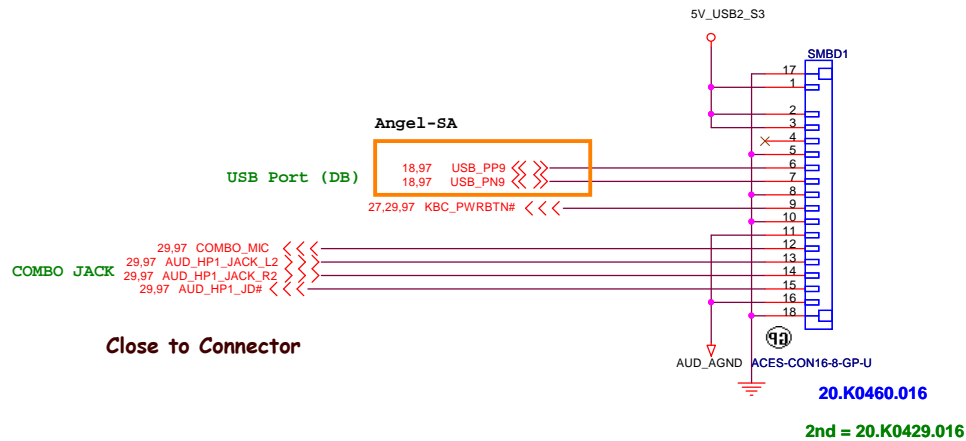
Document Number

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Title			
<b>GPU(PEG)</b>			
Size A2	Document Number	Rev	
<b>Angel-CY</b>		<b>1</b>	
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Title		
<b>GPU (DIGITALOUT)</b>		
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Title			
<b>GPU (VRAM I/F)</b>			
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Title			
<b>GPU (POWER/GND)</b>			
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Title					
<b>GPU-VRAM1,2 (1/4)</b>					
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Size A3	Document Number <b>Angel-CY</b>	Rev <b>1</b>
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Title			
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Title			
<b>GPU-VRAM7,8 (4/4)</b>			
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<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	<b>1</b>
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Title			
<b>LVDS Switch</b>			
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<b>Title</b>			
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<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
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SSID = SDIO

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Title

**TOUCH PANEL**

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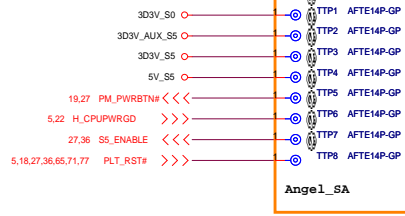
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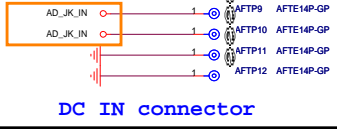


### Check test point

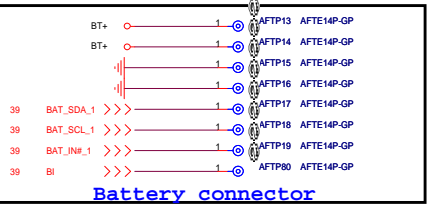


Test Point放在Dimm Door打開可量測處

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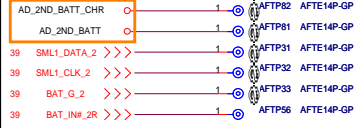


DC IN connector

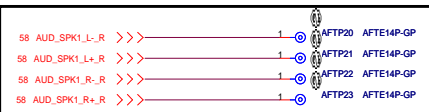


Battery connector

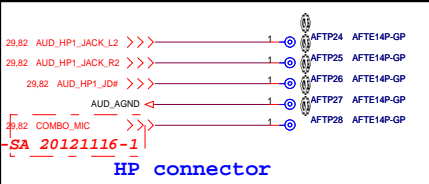
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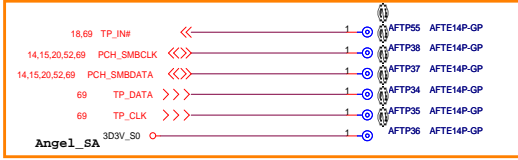
Second Battery connector



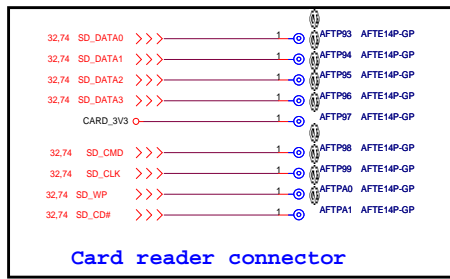
Speaker connector



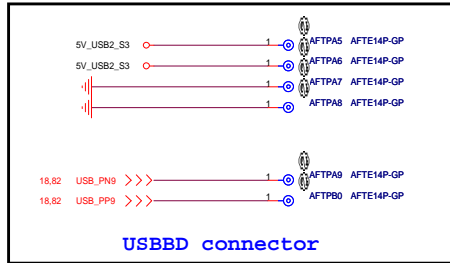
HP connector



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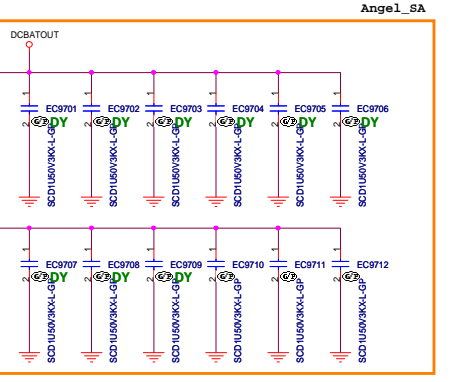
Card reader connector



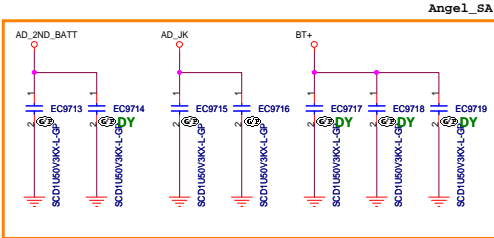
USBBD connector



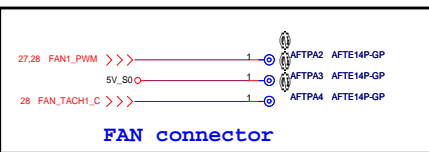
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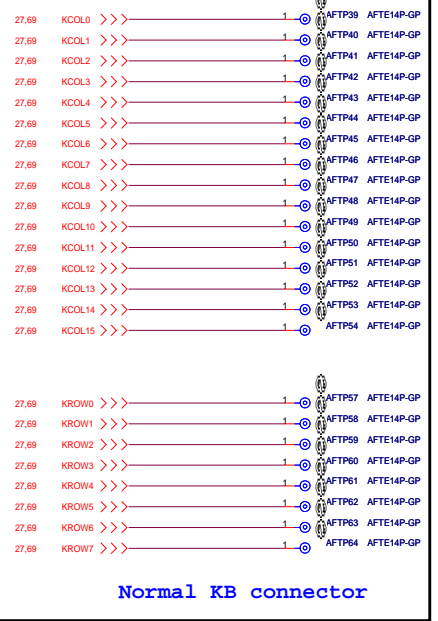
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FAN connector



Normal KB connector

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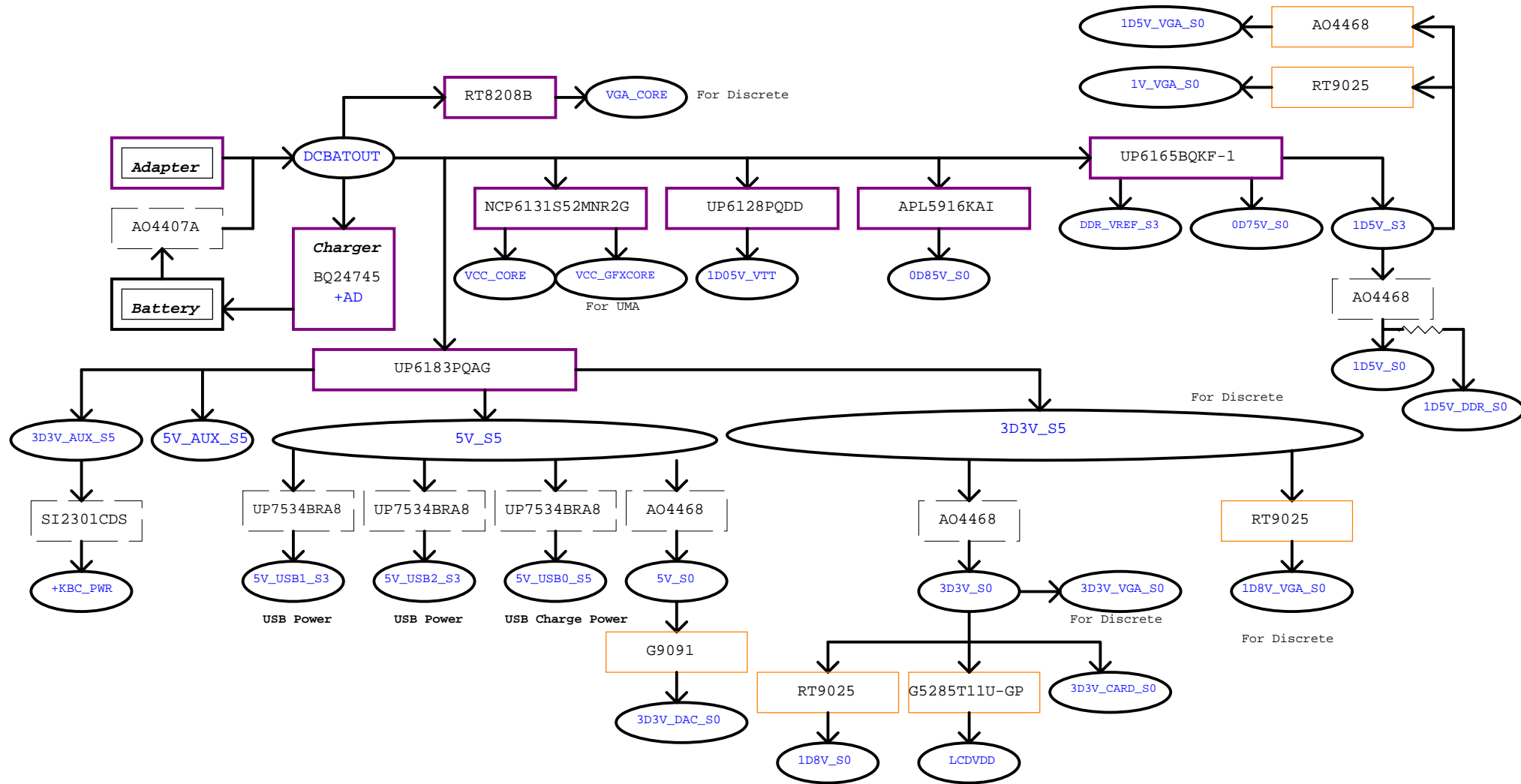
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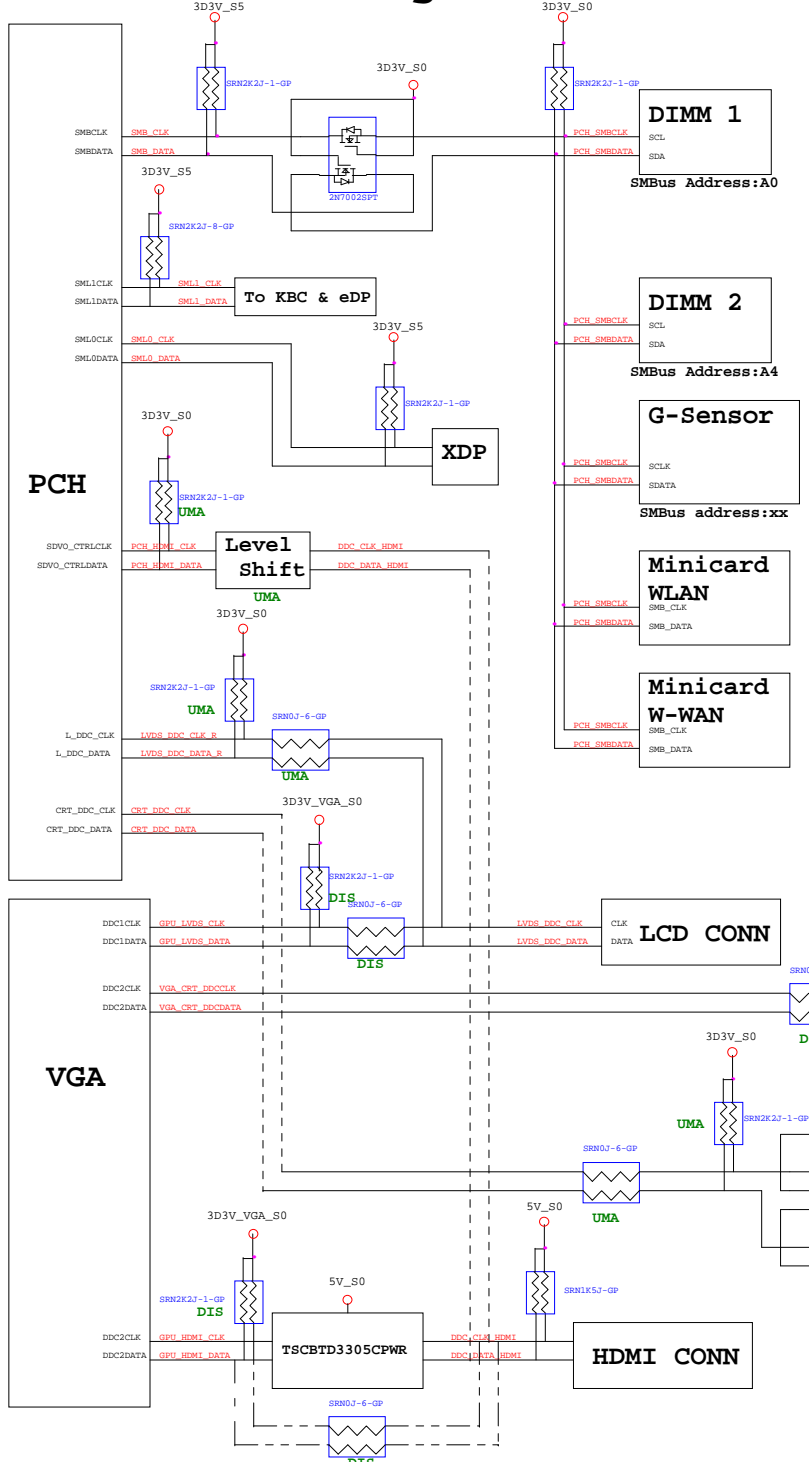
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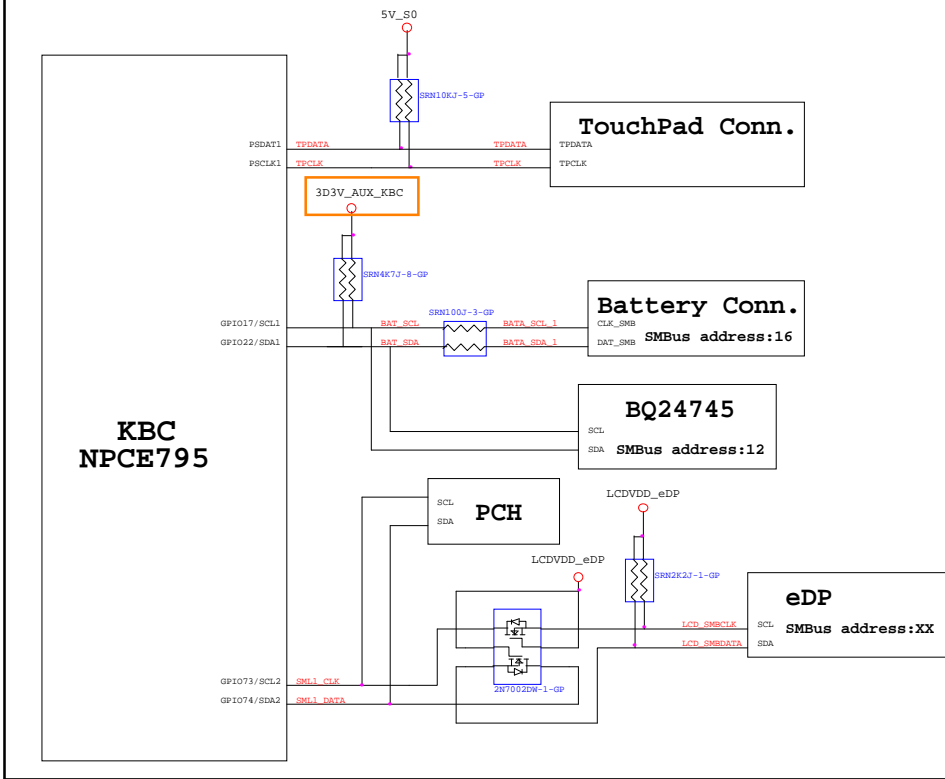




# PCH SMBus Block Diagram

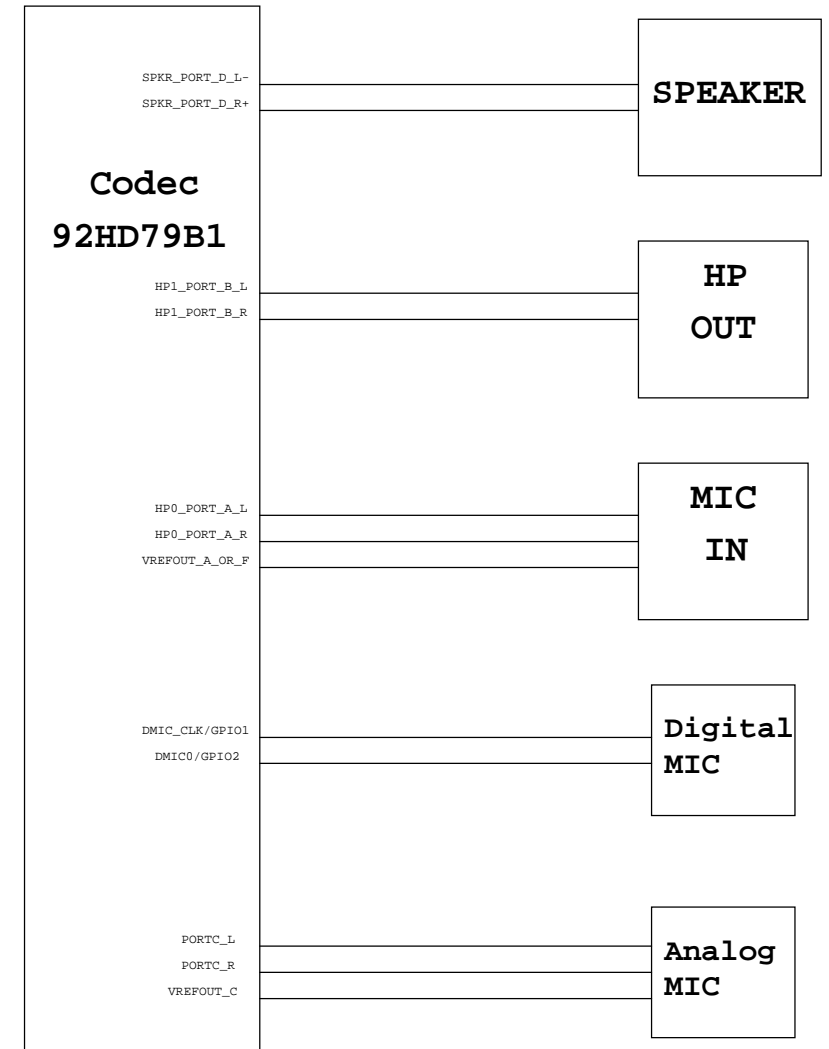
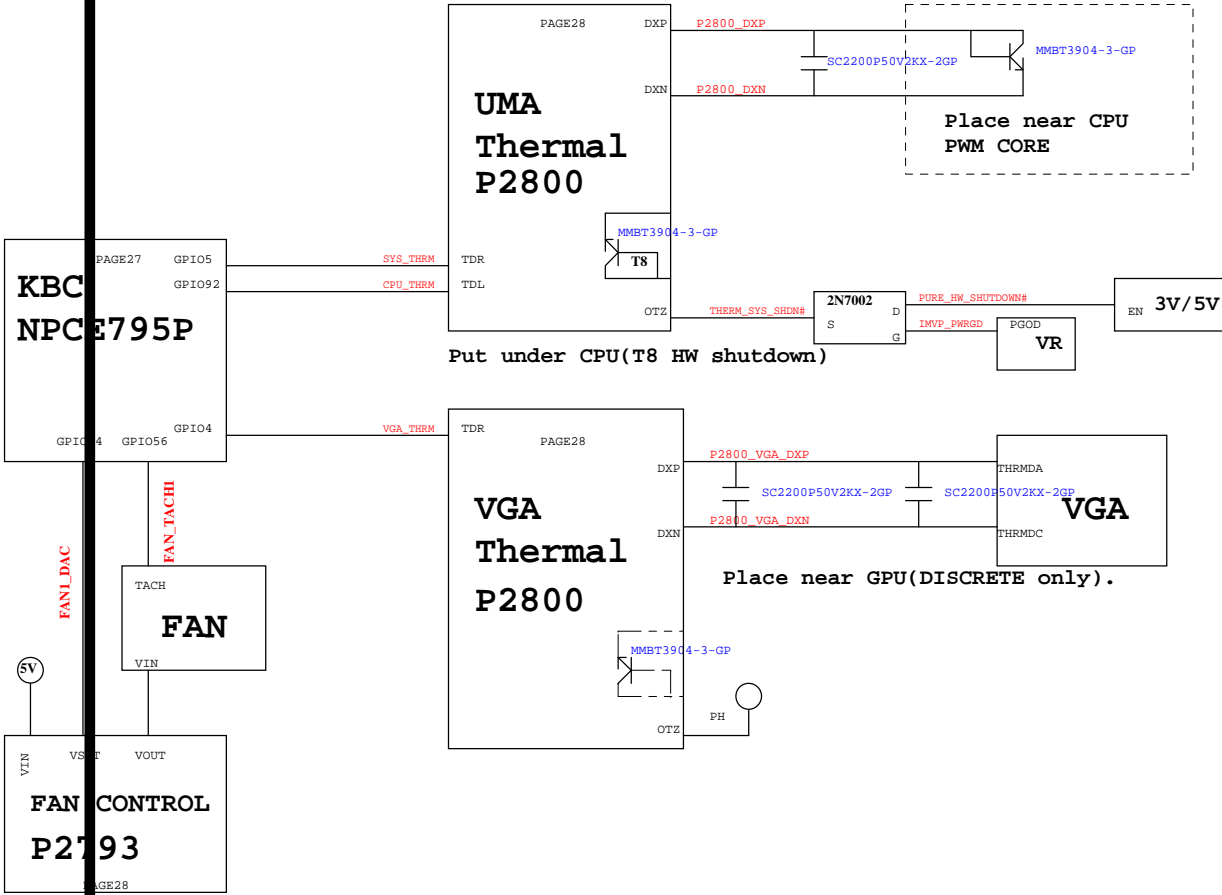


# KBC SMBus Block Diagram



# Thermal Block Diagram

# Audio Block Diagram



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<b>Title Thermal/Audio Block Diagram</b>			
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