

DQDN15 AMD QUEEN M12

Muxless /UMA Schematics Document

AMD LIANO APU FS1

AMD GPU Seymour XT

FCH HUDSON M3


PCB 10246-1

2011-05-28

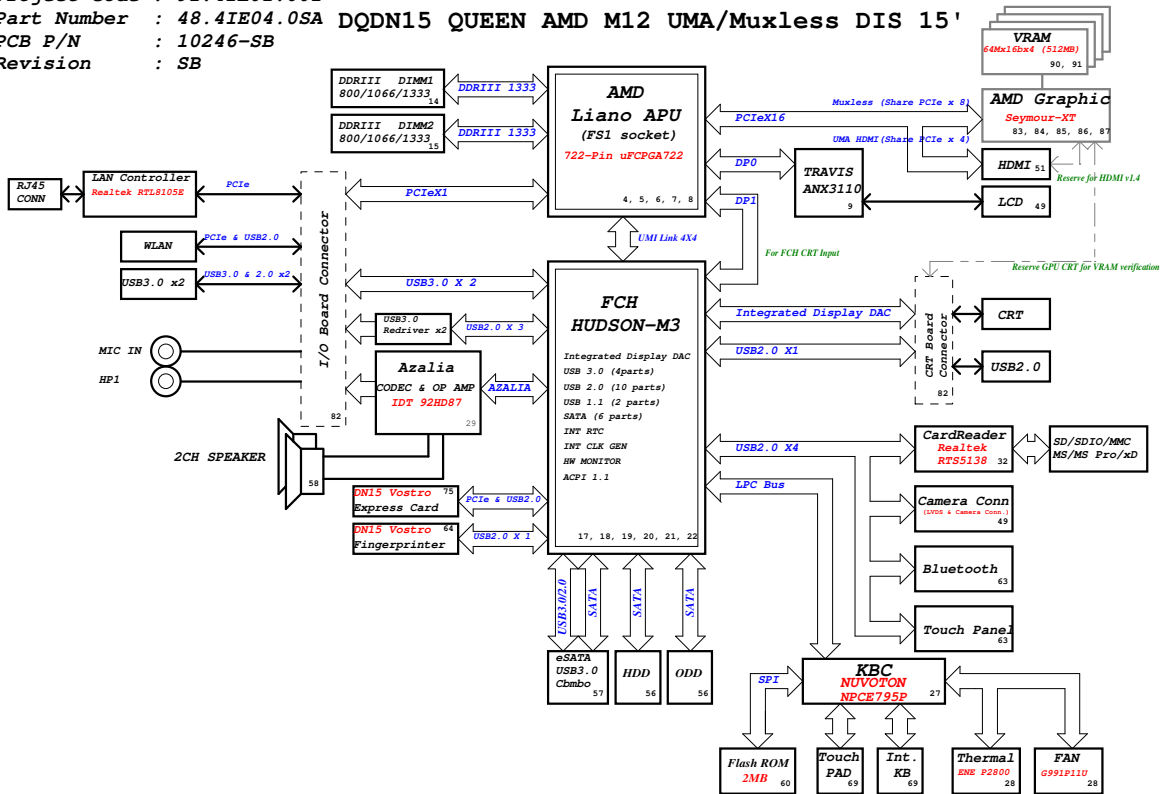
REV : A00

DY :None Installed
UMA_PX:UMA and Muxless platform installed
DIS_PX:DIS and Muxless platform installed
PX:Muxless platform installed
FCH_UMA_PX:UMA_PX CRT FCH output
Whistler: For 8 X Vram
DN15: For DN15

DQ15 AMD DIS SAMSUNG TI

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Title		Cover Page
Size	Document Number	Rev
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Project code : 91.4IE01.001
 Part Number : 48.4IE04.0SA DQDN15 QUEEN AMD M12 UMA/Muxless DIS 15'
 PCB P/N : 10246-SB
 Revision : SB



CHARGER BQ24745		40
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC TP551123		41
INPUTS	OUTPUTS	
DCBATOUT	3D3V AUX S5 5V AUX S5 5V S5 3D3V S5	
APU Core/NB Power ISL6267HRTZ-T		42, 43
INPUTS	OUTPUTS	
DCBATOUT	APU VDD APU VDDNB	
DDRIII SUS TP55116RGER		44
INPUTS	OUTPUTS	
DCBATOUT	1D5V S3	
DDRIII VTT TP55116RGER		44
INPUTS	OUTPUTS	
DCBATOUT	0D75V S0	
APU VDDR/VDDP RT8209		46
INPUTS	OUTPUTS	
DCBATOUT	1D2V S0	
AMD FCH CORE Power RT8209		46
INPUTS	OUTPUTS	
DCBATOUT	1D1V S5	
AMD GPU CORE RT8208B		92
INPUTS	OUTPUTS	
DCBATOUT	VGA CORE PWR	
PCB LAYER		
L1: Top		
L2: VCC		
L3: Signal		
L4: Signal		
L5: GND		
L6: Bottom		

0015 AMD DIS SAMSUNG TI

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File: **Block Diagram** Rev: **X00**
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Strapping

No Fusion Config, Strap Not needed, but reserve

REQUIRED SYSTEM STRAPS

	EC_PWM2 PCH GP0199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM	Allow PCI GEN2 DEFAULT	SS_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM DEFAULT	Force PCI GEN1	SS_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB Debug Port / CRT USB 2.0
1	Mini Card (WLAN)
2	Fingerprint
3	WWAN
4	Bluetooth
5	Touch Panel
6	eSATA/USB Charger
7	CCD Camera
8	New Card
9	CardReader
10	USB 3.0 port 1
11	USB 3.0 port 2
12	USB 3.0 port 3
13	USB 3.0 port 4

PCIe Routing

	APU
LANE0	LAN
LANE1	—WWAN—
LANE2	WLAN
LANE3	—CardReader—

	FCH
LANE0	
LANE1	—Express Card—
LANE2	
LANE3	

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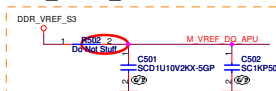
APUIA MEMORY CHANNEL 1 OF 8

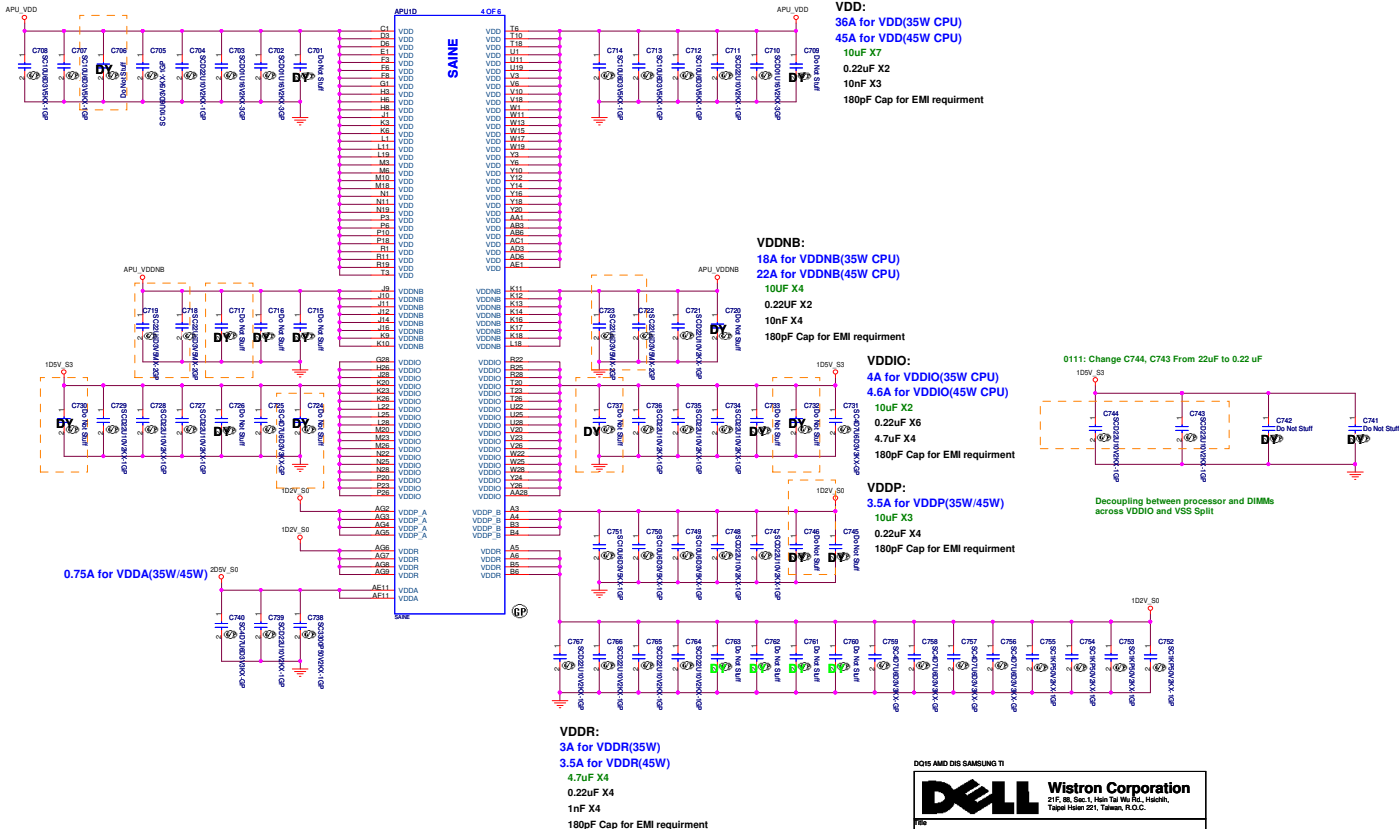
14 M_A_A0	U20	MA_ADD0	E13	MA_DATA0	M_A_D00_14
14 M_A_A1	B20	MA_ADD1	J13	MA_DATA1	M_A_D01_14
14 M_A_A2	B21	MA_ADD2	H13	MA_DATA2	M_A_D02_14
14 M_A_A3	F21	MA_ADD3	J13	MA_DATA3	M_A_D03_14
14 M_A_A4	N21	MA_ADD4	H13	MA_DATA4	M_A_D04_14
14 M_A_A5	N24	MA_ADD5	F13	MA_DATA5	M_A_D05_14
14 M_A_A6	N20	MA_ADD6	M_A_DAT6	MA_DATA6	M_A_D06_14
14 M_A_A7	N21	MA_ADD7	M_A_DAT7	MA_DATA7	M_A_D07_14
14 M_A_A8	M21	MA_ADD8	H17	M_A_D08_14	
14 M_A_A9	M24	MA_ADD9	F17	M_A_D09_14	
14 M_A_A10	M21	MA_ADD10	H17	M_A_D10_14	
14 M_A_A11	M24	MA_ADD11	J19	M_A_D11_14	
14 M_A_A12	L24	MA_ADD12	G19	M_A_D12_14	
14 M_A_A13	L21	MA_ADD13	H19	M_A_D13_14	
14 M_A_A14	L20	MA_ADD14	H19	M_A_D14_14	
14 M_A_A15	L20	MA_ADD15	F19	M_A_D15_14	
14 M_A_B50	U24	MA_BANK0	H20	M_A_D016_14	
14 M_A_B51	U21	MA_BANK1	F21	M_A_D017_14	
14 M_A_B52	L23	MA_BANK2	G21	M_A_D018_14	
14 M_A_DM0	E14	MA_DM0	H23	M_A_D019_14	
14 M_A_DM1	A17	MA_DM1	G20	M_A_D020_14	
14 M_A_DM2	E21	MA_DM2	F20	M_A_D021_14	
14 M_A_DM3	F25	MA_DM3	G29	M_A_D022_14	
14 M_A_DM4	AC23	MA_DM4	H22	M_A_D023_14	
14 M_A_DM5	AD27	MA_DM5	G24	M_A_D024_14	
14 M_A_DM6	AD19	MA_DM6	MA_DAT5	MA_DATA5	
14 M_A_DM7	AD15	MA_DM7	MA_DAT6	MA_DATA6	
14 M_A_D0S0	G14	MA_DQS_L0	G26	M_A_D026_14	
14 M_A_D0S1	H14	MA_DQS_H0	F23	M_A_D027_14	
14 M_A_D0S2	H18	MA_DQS_H1	H24	M_A_D028_14	
14 M_A_D0S3	H18	MA_DQS_L1	E28	M_A_D029_14	
14 M_A_D0S4	H21	MA_DQS_H2	MA_DAT0	M_A_D030_14	
14 M_A_D0S5	H21	MA_DQS_H2	MA_DATA31	M_A_D031_14	
14 M_A_D0S6	E27	MA_DQS_L2	AB28	M_A_D032_14	
14 M_A_D0S7	C26	MA_DQS_H3	AD25	M_A_D033_14	
14 M_A_D0S8	AE28	MA_DQS_H4	MA_DAT3	M_A_D034_14	
14 M_A_D0S9	AD26	MA_DQS_L4	AA24	M_A_D035_14	
14 M_A_D0S10	AE22	MA_DQS_H5	AC26	M_A_D036_14	
14 M_A_D0S11	AA22	MA_DQS_L5	AD28	M_A_D037_14	
14 M_A_D0S12	AB18	MA_DQS_H6	AB26	M_A_D038_14	
14 M_A_D0S13	AA18	MA_DQS_L6	AC25	M_A_D039_14	
14 M_A_D0S14	AA14	MA_DQS_H7	MA_DAT8	MA_DATA8	
14 M_A_D0S15	AA15	MA_DQS_L7	MA_DAT9	MA_DATA9	
14 M_A_DM0_CLK_DDR0	T21	MA_CLK_H0	AA23	M_A_D040_14	
14 M_A_DM0_CLK_DDR1	122	MA_CLK_L0	MA_DAT2	M_A_D041_14	
14 M_A_DM0_CLK_DDR2	R21	MA_CLK_H1	AA20	M_A_D042_14	
14 M_A_DM0_CLK_DDR3	R24	MA_CLK_L1	AB24	M_A_D043_14	
14 M_A_DM0_CLK_DDR4	R24	MA_CLK_L1	AD24	M_A_D044_14	
14 M_A_DM0_CLK_DDR5	R24	MA_CLK_L1	AA21	M_A_D045_14	
14 M_A_DM0_CKE0	H28	MA_CKE0	AC21	M_A_D046_14	
14 M_A_DM0_CKE1	H27	MA_CKE1	MA_DAT47	M_A_D047_14	
14 M_A_DM0_ODT0	Y25	MA_ODT0	AA19	M_A_D048_14	
14 M_A_DM0_ODT1	AA27	MA_ODT1	AC17	M_A_D049_14	
14 M_A_DM0_CS#0	Y22	MA_CS#0	MA_DAT50	M_A_D050_14	
14 M_A_DM0_CS#1	AA26	MA_CS#1	MA_DAT51	M_A_D051_14	
14 M_A_RAS#	W24	MA_RAS#	MA_DAT52	M_A_D052_14	
14 M_A_WE#	W24	MA_WE#	MA_DAT53	M_A_D053_14	
14 M_A_RST#	H25	MA_RESET#	MA_DAT54	M_A_D054_14	
		MA_EVENT#	MA_DAT55	M_A_D055_14	
		M_VREF_DQ_APU	MA_DAT56	M_A_D056_14	
		M_VREF_DQ_APU	MA_DAT57	M_A_D057_14	
		M_VREF_DQ_APU	MA_DAT58	M_A_D058_14	
		M_VREF_DQ_APU	MA_DAT59	M_A_D059_14	
		M_VREF_DQ_APU	MA_DAT60	M_A_D060_14	
		M_VREF_DQ_APU	MA_DAT61	M_A_D061_14	
		M_VREF_DQ_APU	MA_DAT62	M_A_D062_14	
		M_VREF_DQ_APU	MA_DAT63	M_A_D063_14	

APUIB MEMORY CHANNEL 2 OF 8

T27	MB_ADD0	M_B_D00_15
P24	MB_ADD1	M_B_D01_15
F25	MB_ADD2	M_B_D02_15
N27	MB_ADD3	M_B_D03_15
M27	MB_ADD4	M_B_D04_15
M27	MB_ADD5	M_B_D05_15
M27	MB_ADD6	M_B_D06_15
M27	MB_ADD7	M_B_D07_15
M25	MB_ADD8	
L26	MB_ADD9	
L26	MB_ADD10	
L27	MB_ADD11	
K27	MB_ADD12	
W26	MB_ADD13	
K25	MB_ADD14	
K24	MB_ADD15	
I27	MB_BANK0	
T28	MB_BANK1	
S28	MB_BANK2	
D14	MB_DM0	
A18	MB_DM1	
A22	MB_DM2	
M2	MB_DM3	
AF26	MB_DM4	
AC26	MB_DM5	
AD14	MB_DM6	
AD14	MB_DM7	
C15	MB_DQS_0	
E18	MB_DQS_L0	
H18	MB_DQS_H1	
D18	MB_DQS_L1	
E22	MB_DQS_H2	
D22	MB_DQS_L2	
S26	MB_DQS_H3	
AE26	MB_DQS_L3	
AG24	MB_DQS_H4	
AG26	MB_DQS_L4	
AG21	MB_DQS_H5	
AG17	MB_DQS_L5	
AG16	MB_DQS_H6	
AH14	MB_DQS_L6	
AG14	MB_DQS_H7	
AG14	MB_DQS_L7	
R26	MB_CLK_H0	
P27	MB_CLK_L0	
P28	MB_CLK_H1	
P28	MB_CLK_L1	
J26	MB_CKE0	
J27	MB_CKE1	
W26	MB_ODT0	
Y26	MB_ODT1	
Y25	MB_CS#0	
Y27	MB_CS#1	
Y24	MB_RAS#	
W25	MB_CAS#	
W25	MB_WE#	
J25	MB_RESET#	
T28	MB_EVENT#	
B14	MB_DATA0	
B14	MB_DATA1	
D16	MB_DATA2	
E16	MB_DATA3	
C13	MB_DATA4	
B16	MB_DATA5	
B16	MB_DATA6	
A17	MB_DATA7	
C18	MB_DATA8	
B18	MB_DATA9	
B20	MB_DATA10	
E17	MB_DATA11	
E16	MB_DATA12	
B17	MB_DATA13	
B18	MB_DATA14	
C19	MB_DATA15	
C21	MB_DATA16	
S22	MB_DATA17	
A24	MB_DATA19	
D20	MB_DATA20	
B21	MB_DATA21	
E22	MB_DATA22	
B23	MB_DATA23	
E24	MB_DATA24	
B25	MB_DATA25	
D28	MB_DATA26	
S24	MB_DATA27	
D24	MB_DATA28	
D27	MB_DATA29	
C27	MB_DATA30	
C27	MB_DATA31	
AG26	MB_DATA32	
AG23	MB_DATA33	
AG23	MB_DATA34	
AG27	MB_DATA35	
AG27	MB_DATA36	
AG27	MB_DATA37	
AG24	MB_DATA38	
AG24	MB_DATA39	
AE22	MB_DATA40	
AE20	MB_DATA41	
AD23	MB_DATA43	
AD23	MB_DATA44	
AD21	MB_DATA45	
AD20	MB_DATA46	
AD20	MB_DATA47	
AE19	MB_DATA48	
AE16	MB_DATA49	
AE16	MB_DATA50	
AE16	MB_DATA51	
AG20	MB_DATA52	
AG19	MB_DATA53	
AG17	MB_DATA54	
AG16	MB_DATA55	
AG15	MB_DATA56	
AG13	MB_DATA57	
AG13	MB_DATA58	
AG13	MB_DATA59	
AG13	MB_DATA60	
AG13	MB_DATA61	
AG13	MB_DATA62	
AG13	MB_DATA63	

APU VREF_DQ





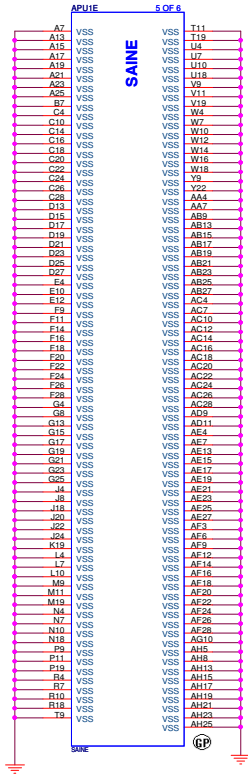
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Rev **APU Power(4/5)**

Doc Number **QUEEN AMD Muxless/UMA**

Rev **X00**

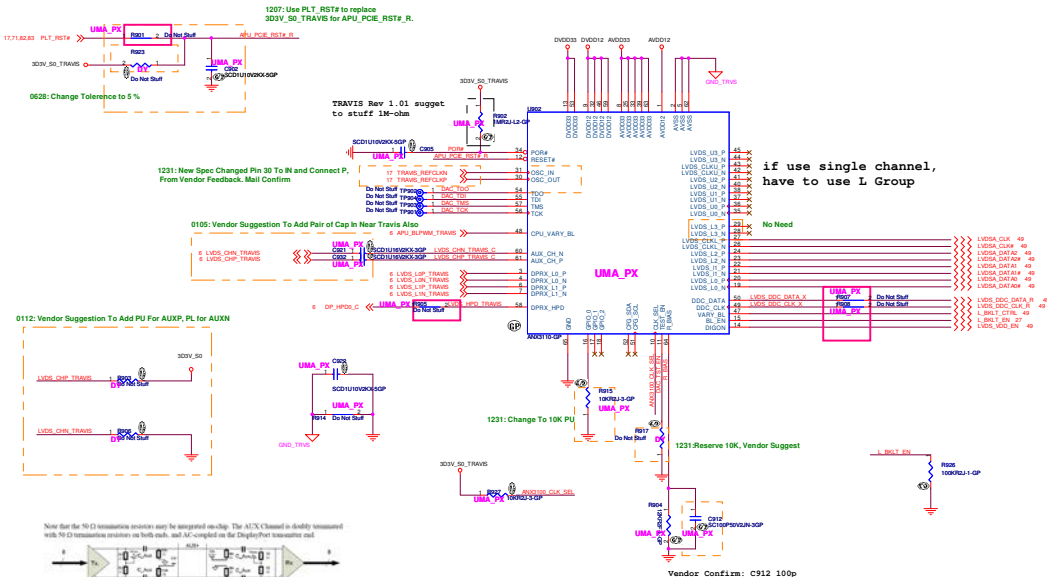
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APU VSS(5/5)		
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if use single channel,
have to use L Group

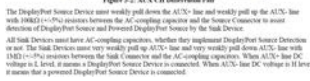
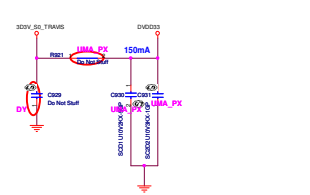
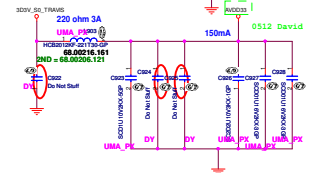
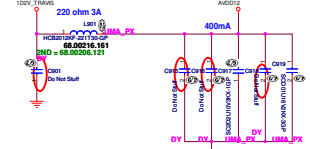
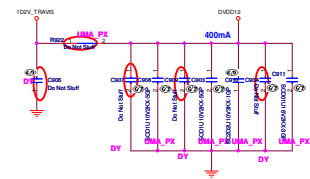


Figure 3-2 ANX CH Differential Pair

The DisplayPort Sense Device must weakly pull-down the ANX+ line and weakly pull-up the ANX- line with 10kΩ ± 1% resistors between the AC-coupling capacitor and the Sense Connector to assist detection of DisplayPort Sense and prevent DisplayPort Sense by the Sink Device.

All Sink Devices must have AC-coupling capacitors, whether they implement DisplayPort Sense Detection or not. The Sink Devices must very weakly pull-up ANX+ line and very weakly pull-down ANX- line with 10kΩ ± 1% resistors between the Sink Connector and the AC-coupling capacitors. When ANX+ line DC voltage is 0V, Sink CH assumes a DisplayPort Sense Device is connected. When ANX- line DC voltage is 10V, it means that a powered DisplayPort Sense Device is connected.

ANX9834 power on delay time For ANX3100 ALSO

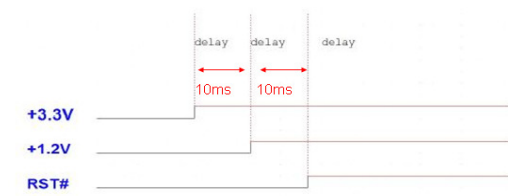
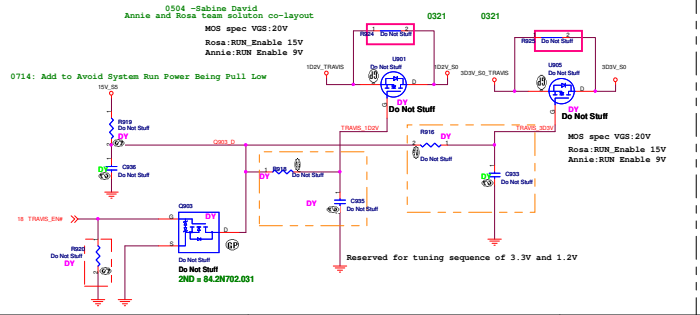
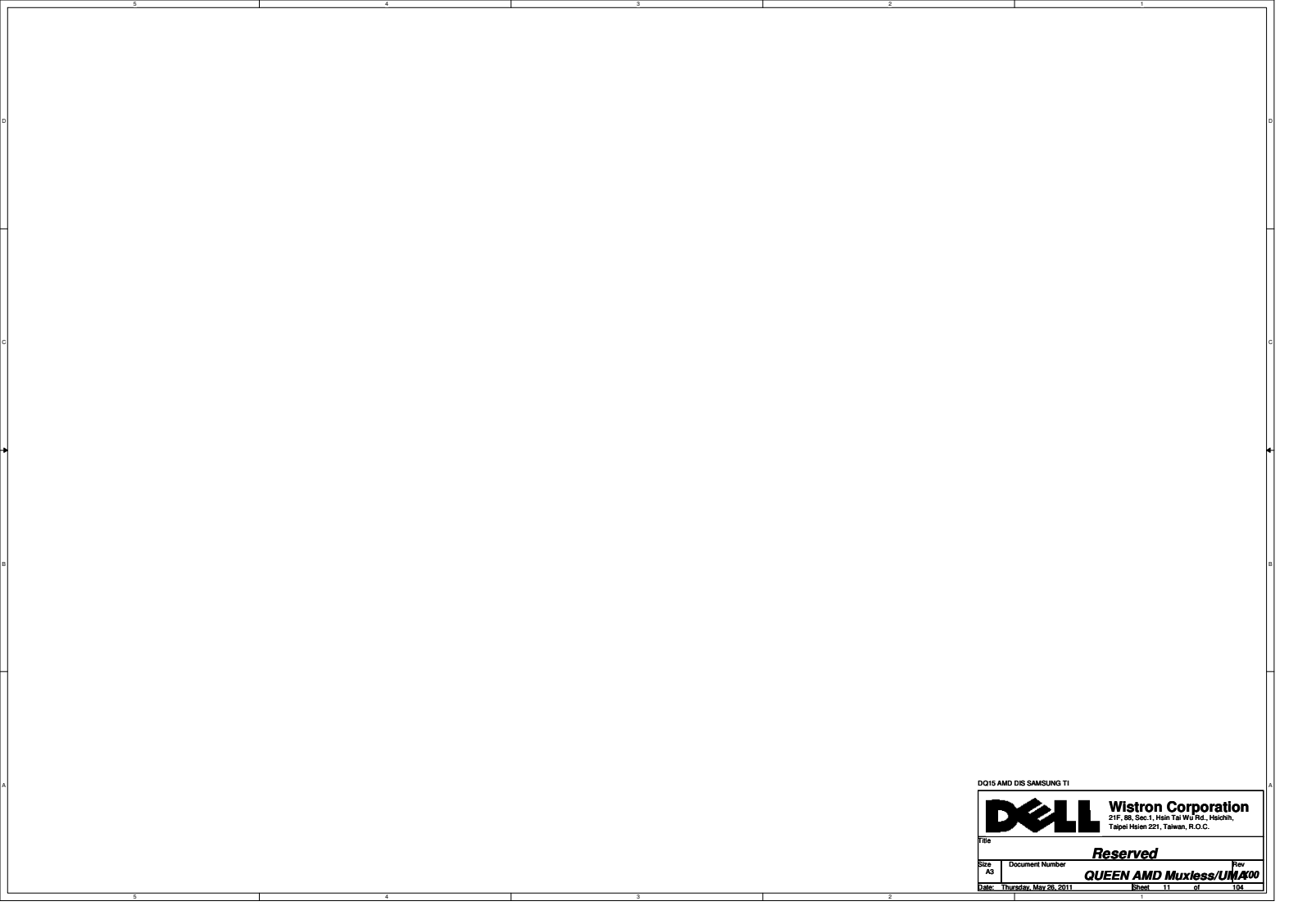


Figure 2 power supply sequencing

0015 AMD DDL SAMUNG TI

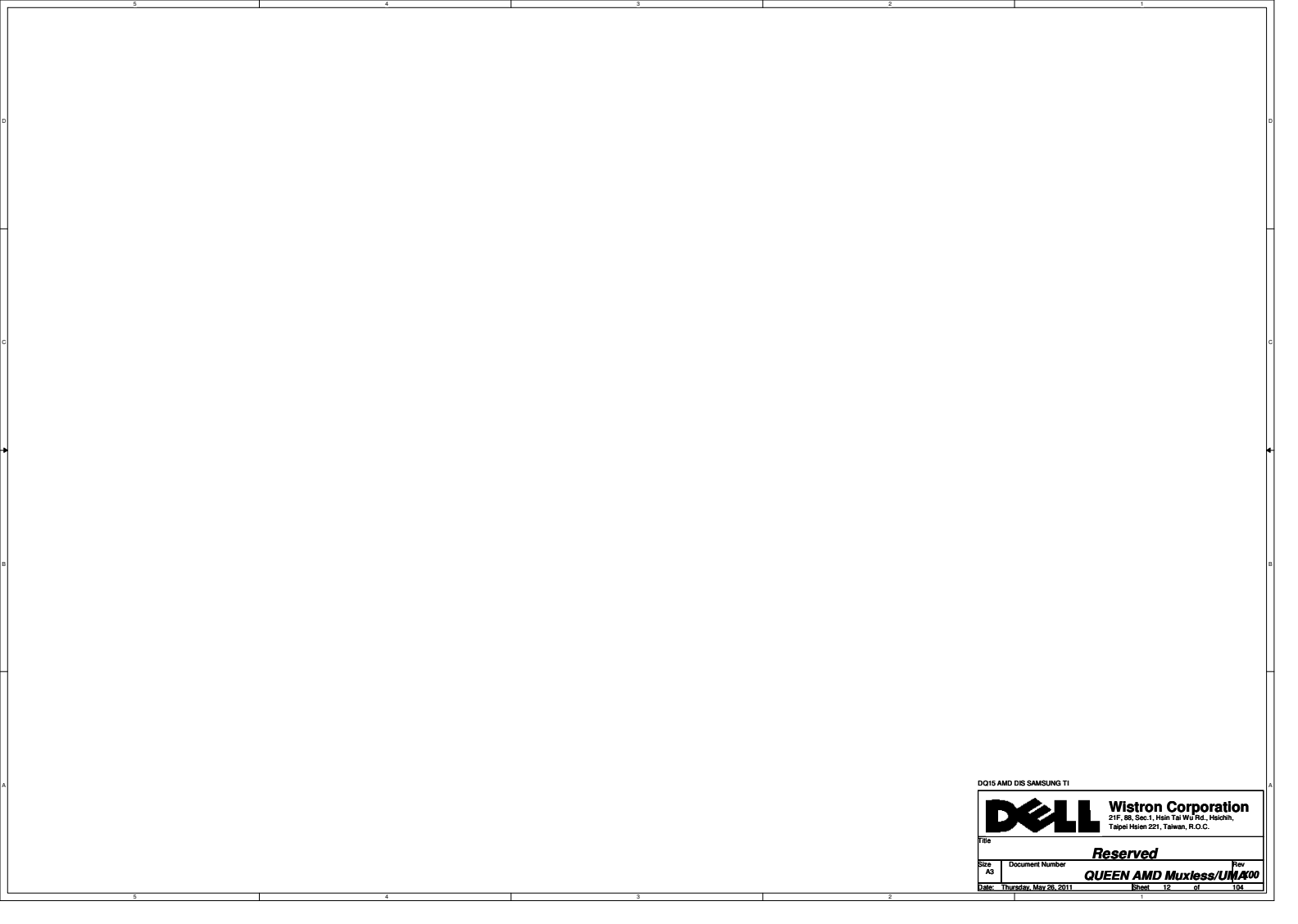
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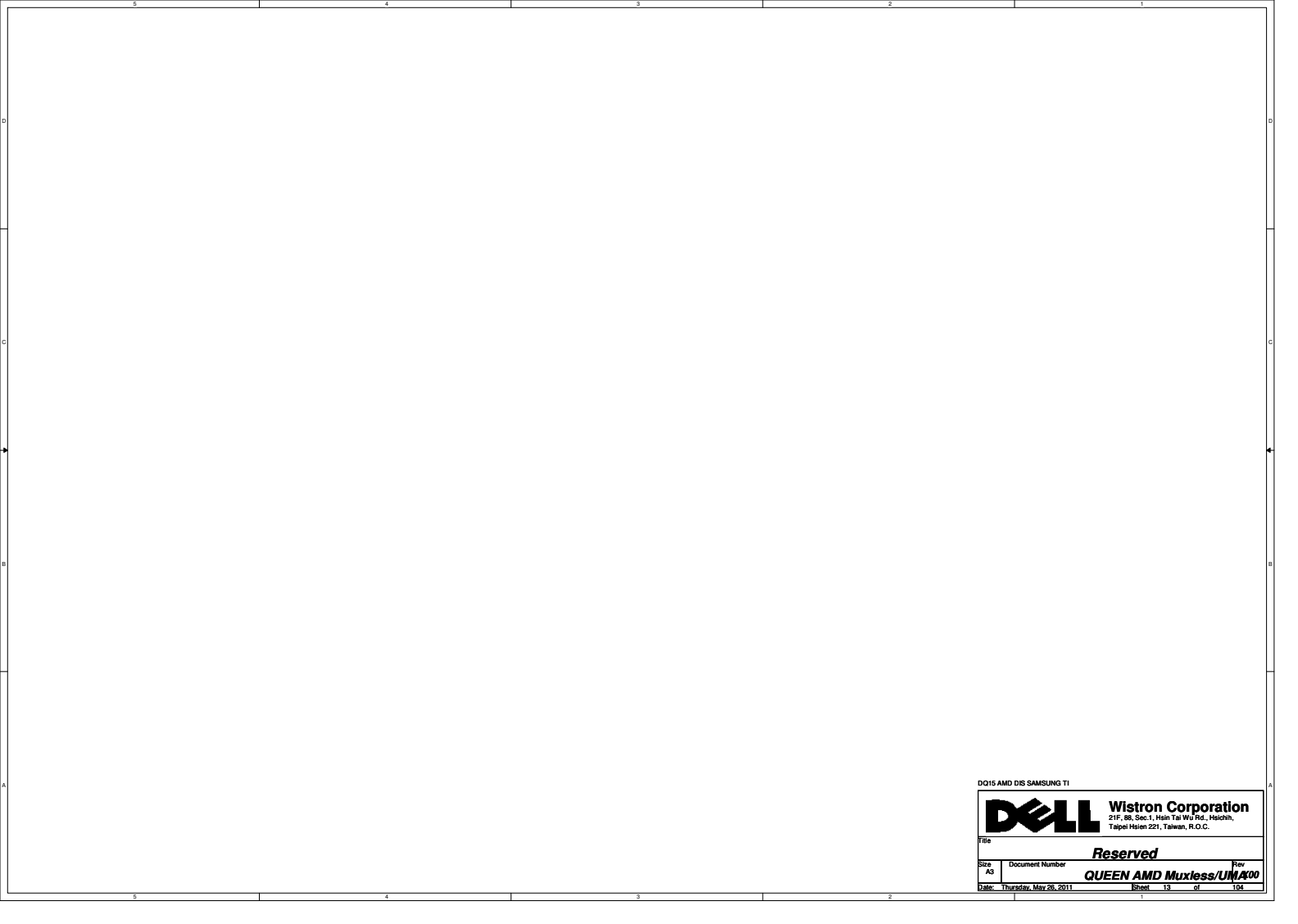


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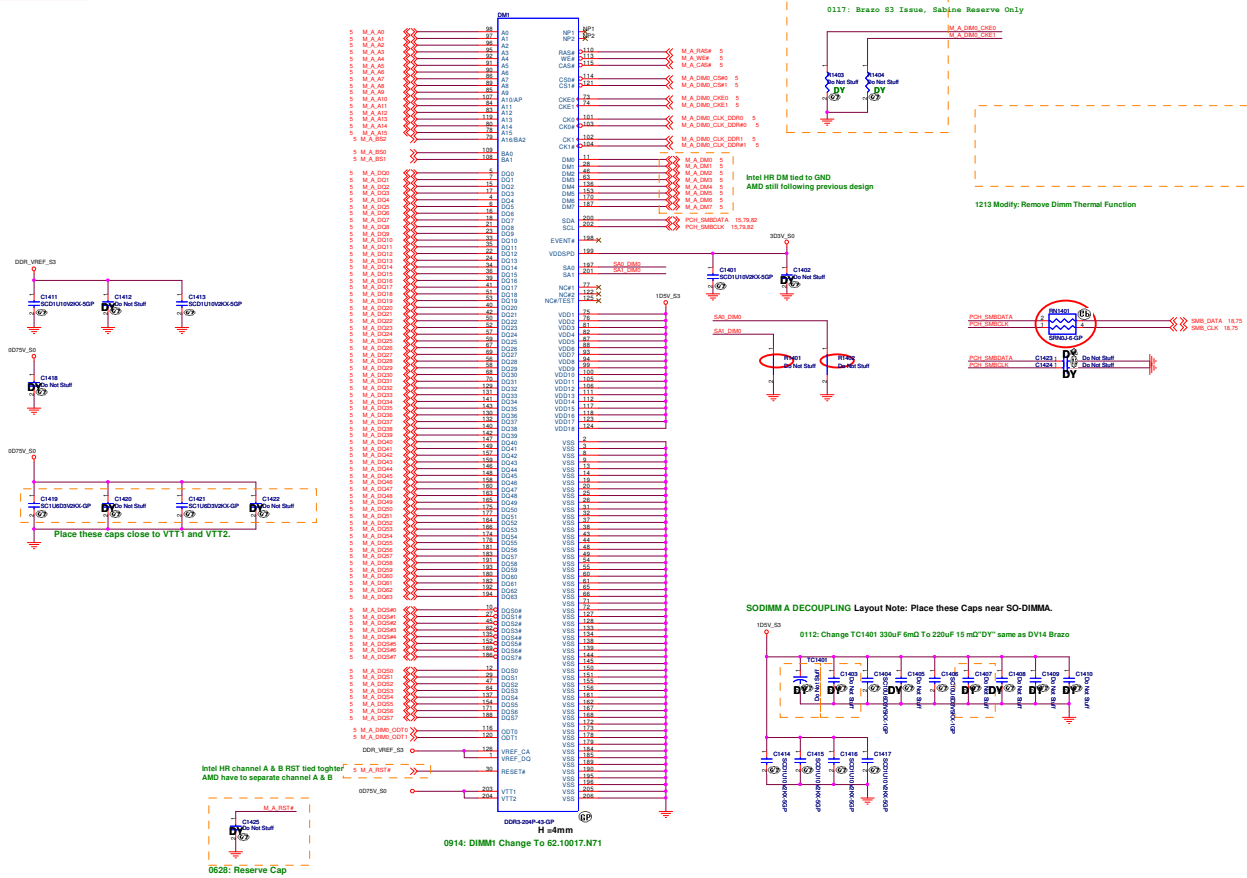
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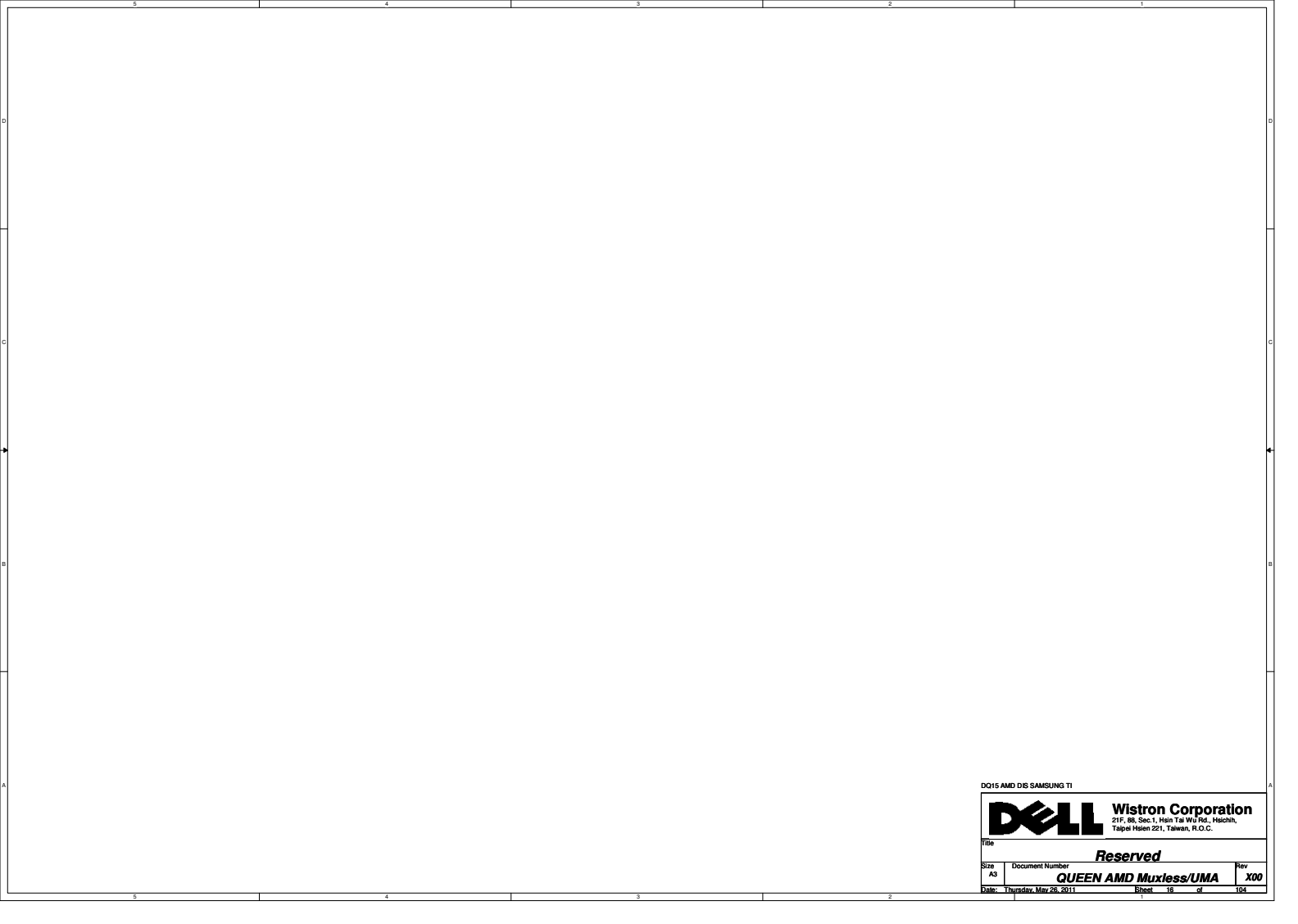


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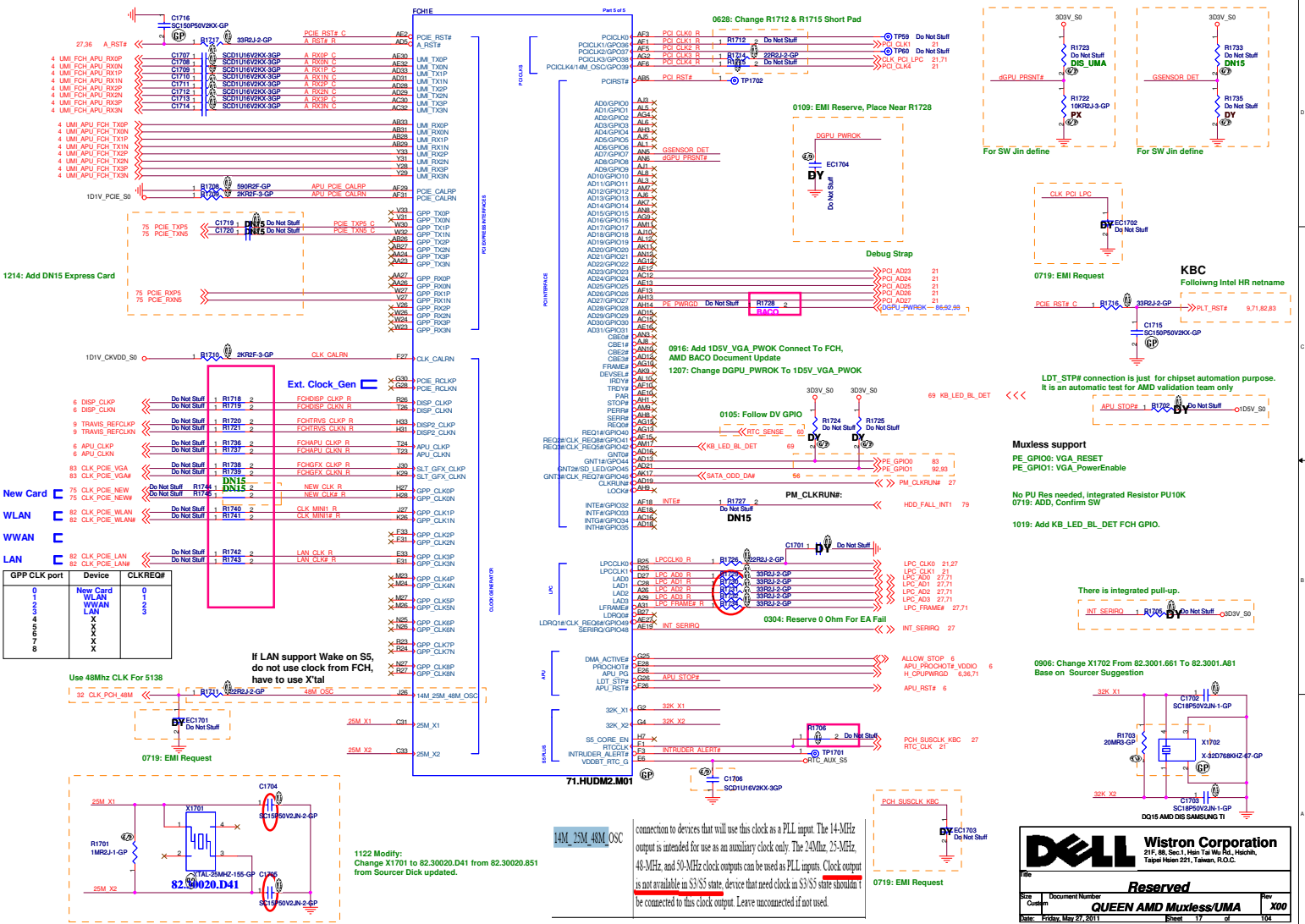
SSID = MEMORY





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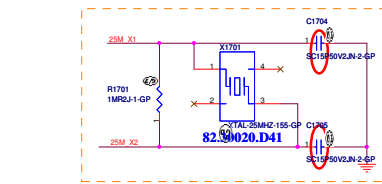


1214: Add DN15 Express Card

- New Card
- WLAN
- WWAN
- LAN

GPP CLK port	Device	CLKREQ#
0	New Card	0
1	WLAN	1
2	WLAN	2
3	WLAN	3
4	X	X
5	X	X
6	X	X
7	X	X
8	X	X

Use 48MHz CLK For 5138



1122 Modify: Change X1701 to 82.30020.D41 from 82.30020.851 from Sourcer Direct updated.

14M_25M_48M_OSC

connection to devices that will use this clock as a PLL input. The 14-MHz output is intended for use as an auxiliary clock only. The 24.0MHz, 25.0MHz, 48.0MHz, and 50.0MHz clock outputs can be used as PLL inputs. Clock output is not available in S3/S5 state, device that need clock in S3/S5 state should not be connected to this clock output. Leave unconnected if not used.

If LAN support Wake on S5, do not use clock from FCH, have to use X'tal

0719: EMI Request

0719: EMI Request

0719: EMI Request

0719: EMI Request

0719: EMI Request

0719: EMI Request

0719: EMI Request

0719: EMI Request

0719: EMI Request

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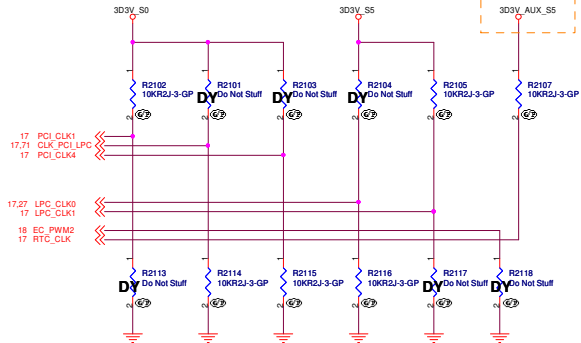
0719: EMI Request

0719: EMI Request

SSID = S.B

REQUIRED STRAPS

CRB: PU to 3.3V_AUX_S5
 Checklist: PU to 3.3V_S5
 Confirm with AMD, follow CRB suggestion



REQUIRED SYSTEM STRAPS

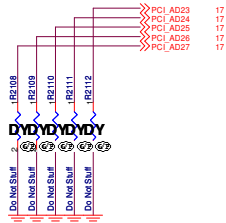
Use this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal)
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

No Fusion Config, Strap Not needed, but reserve

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS

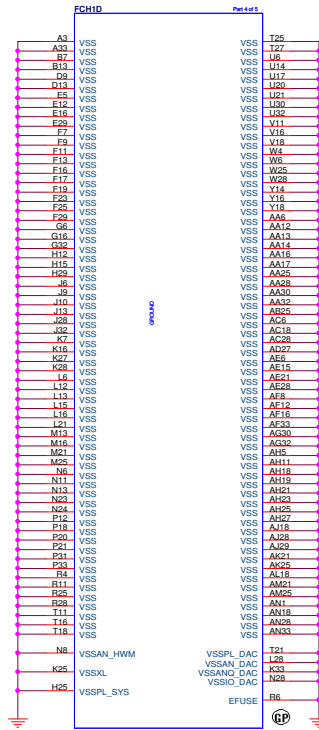


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

DQ15 AMD DIS SAMSUNG T1

DELL		Wistron Corporation	
21F, 8B, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsin 221, Taiwan, R.O.C.			
Title SB820M_STRAPPING_(5/5)			
Size A3	Document Number	Rev	
	QUEEN AMD Muxless/UMA	X00	
Date: Thursday, Mar 28, 2011	Sheet 21	of	104



71.HUDM2.M01

DQ15 AMD DIS SAMSUNG TI



217, 8th, Sec.1, Hsin Tai Wu Rd., Hsuehshin,
Taipei Hsien 221, Taiwan, R.O.C.

File

Reserved

Doc

Document Number

Rev

QUEEN AMD Muxless/UMA00

Date

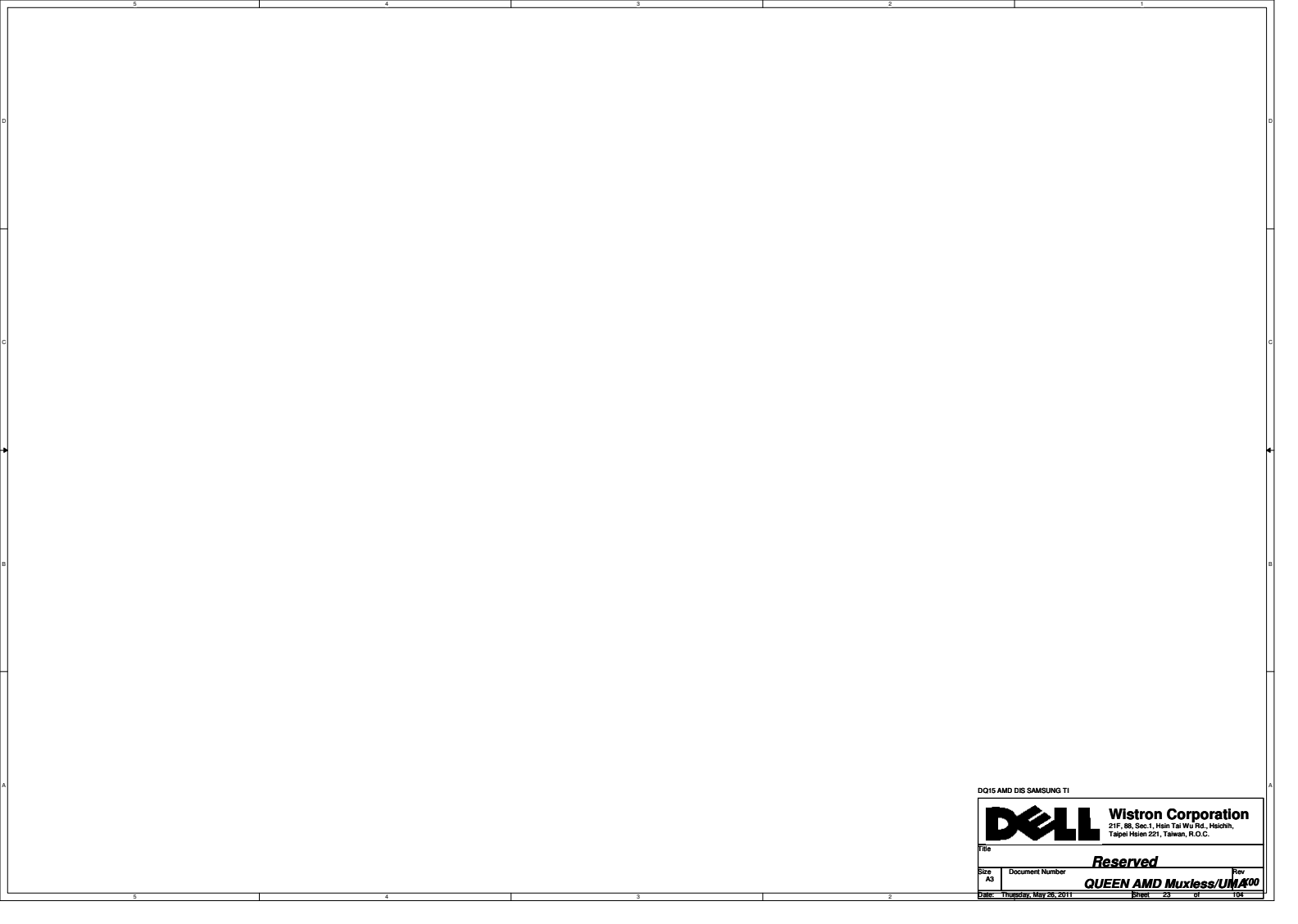
Thursday, May 26, 2011

Sheet

22

of

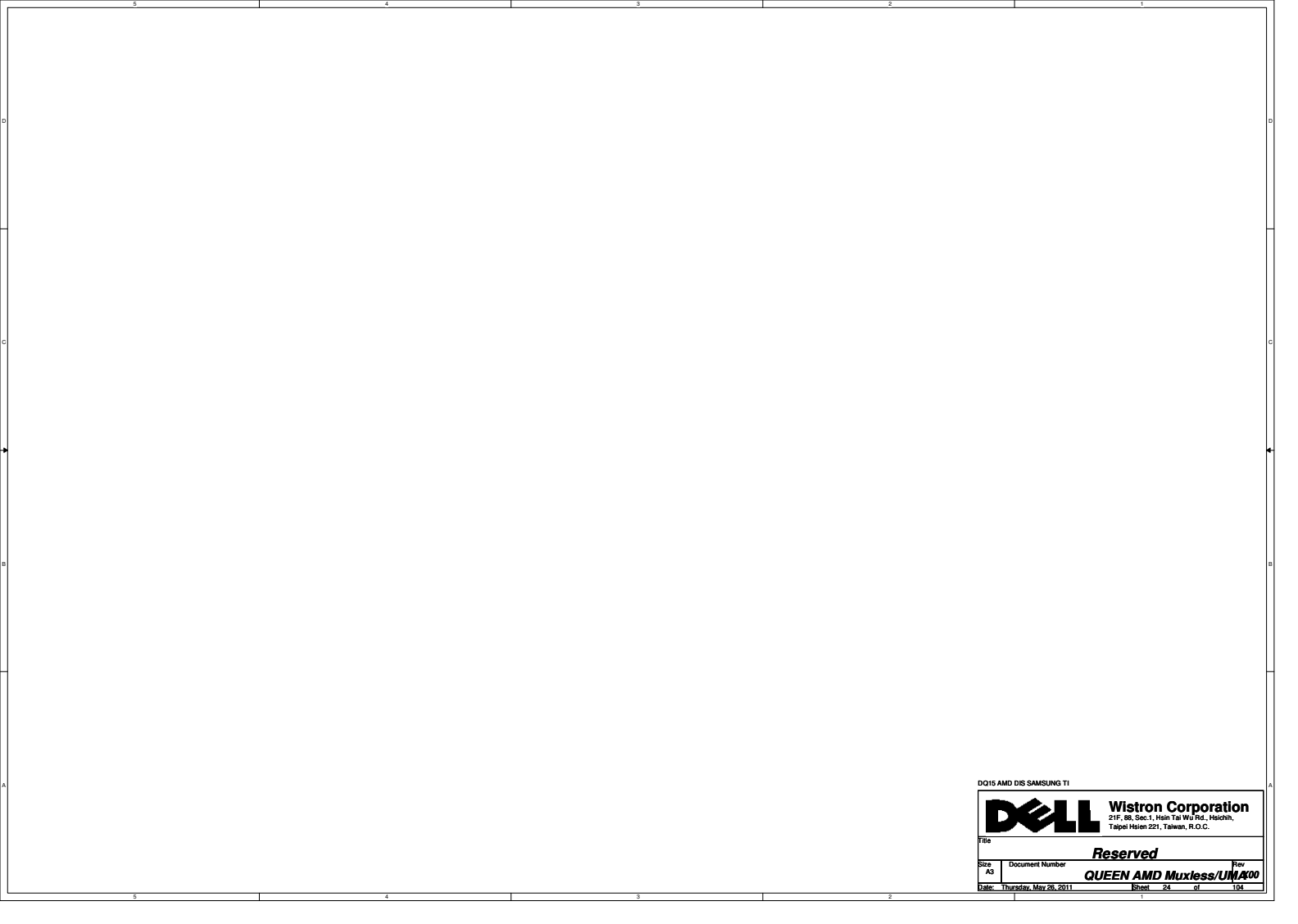
104




DQ15 AMD DIS SAMSUNG TI

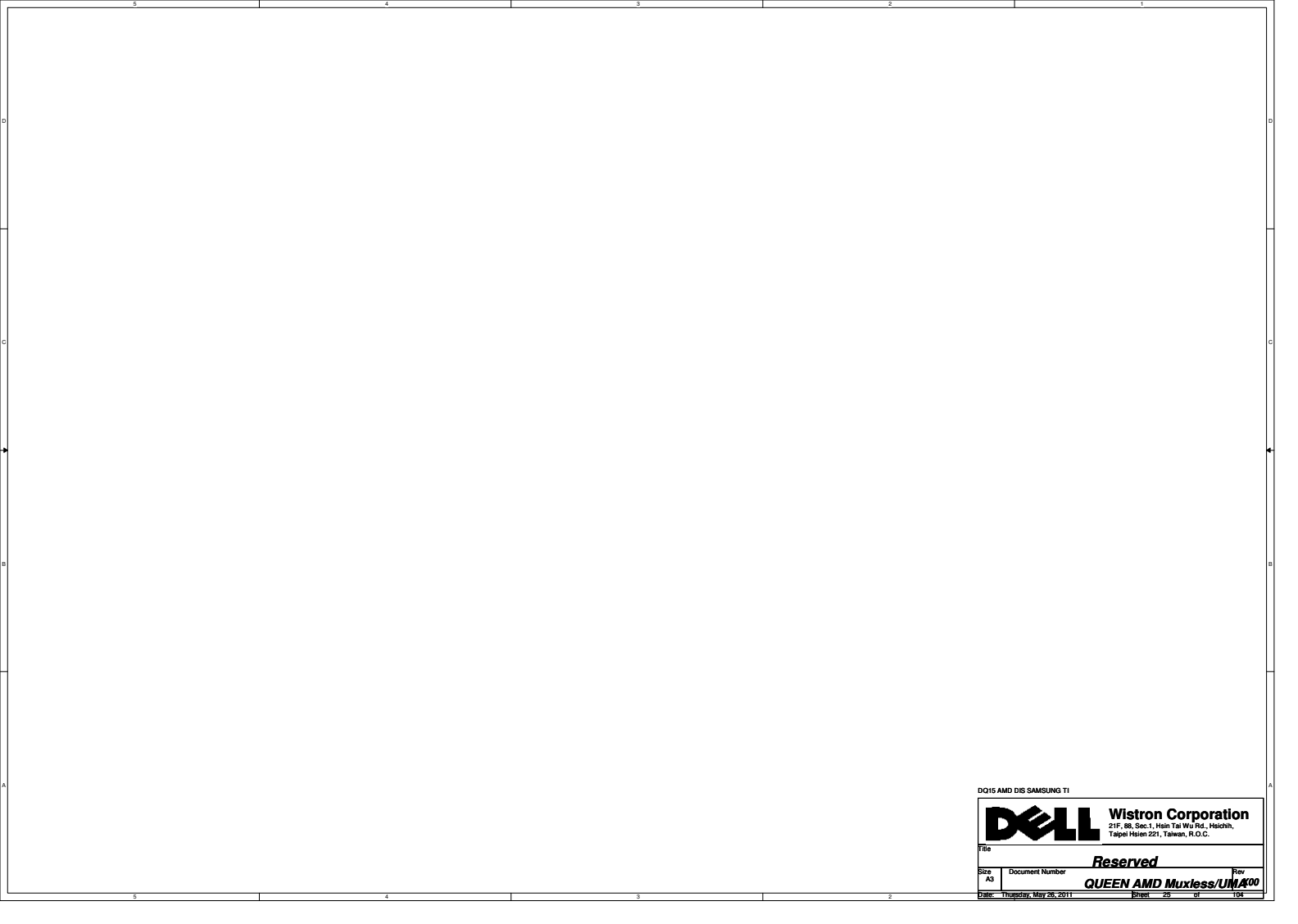
	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

File		
Reserved		
Size	Document Number	Rev
A3		
QUEEN AMD Muxless/UMA00		
Date: Thursday, May 26, 2011	Sheet 23	of 104



DQ15 AMD DIS SAMSUNG TI

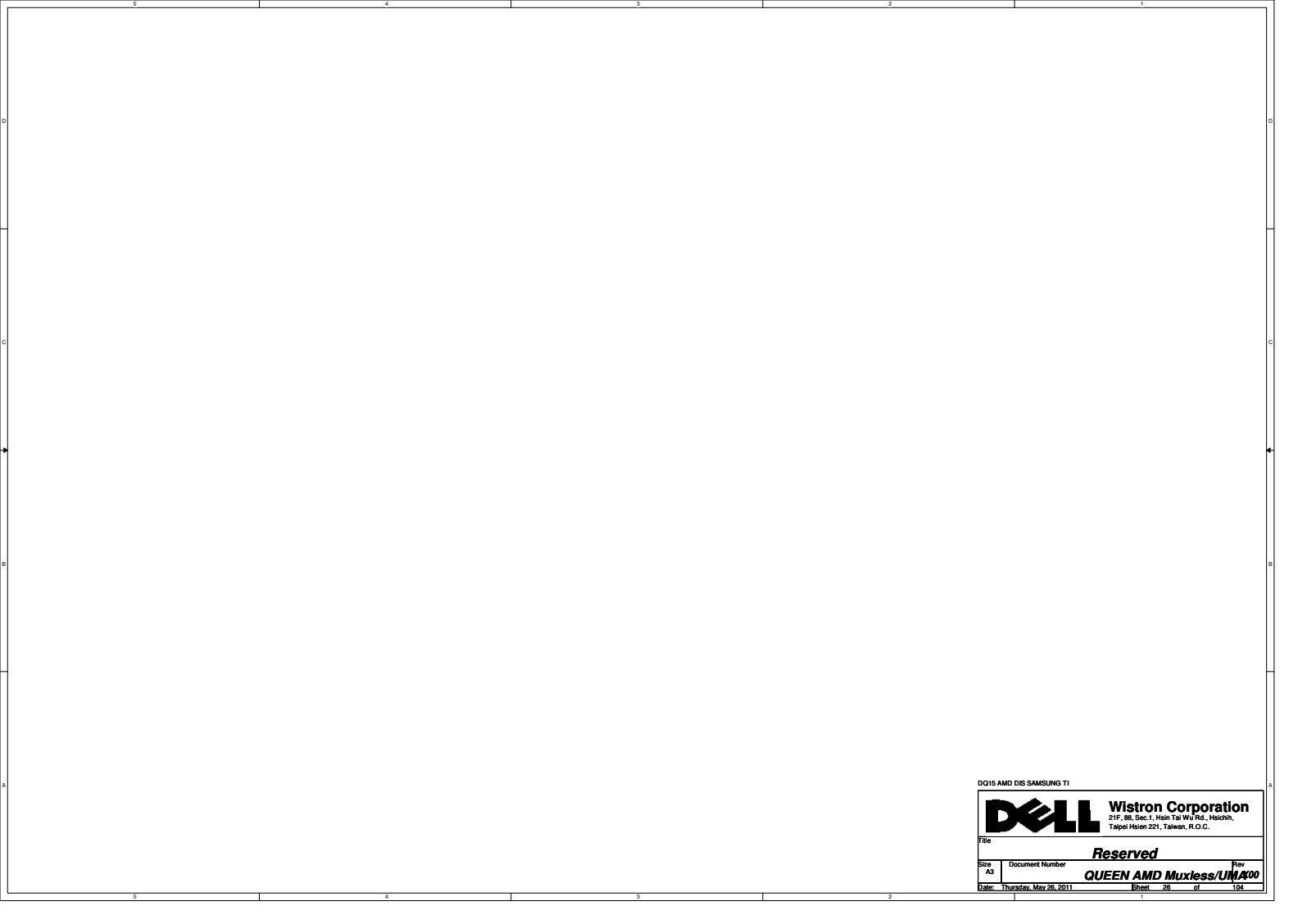
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Reserved			
Size A3	Document Number	Rev	
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Reserved		
Size	Document Number	Rev
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Reserved			
Size A3	Document Number QUEEN AMD Muxless/UMA00	Rev	
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9913 BSI Modify:
 Add R206 (R207) and reserved EC206/EC207 on
 AUD_DMIC_CLK & AUD_DMIC_JM0 for EMC suggestion.

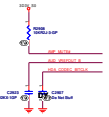
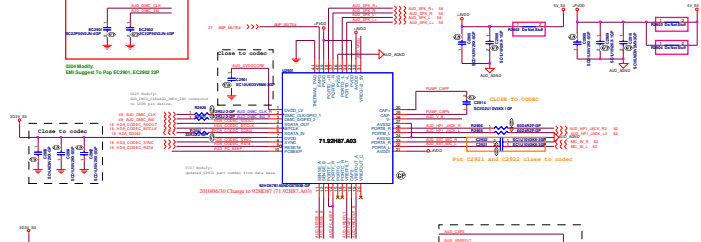
9915 Modify:
 EMU Request R203, R201 Place Near LCD1 Connector.
 Move EC201 - EC203 to P-49 and place after R202, R201

9916 Modify:
 Vendor Suggest To Change R202 To 22 Ohm

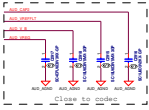
For EMI



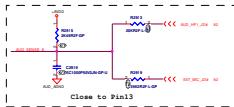
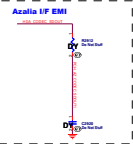
9204 Modify:
 EMU Suggest To Pop EC201, EC202 ZDP



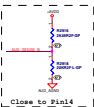
AUD_PC_BEEP
 Trace width=15 mils



9701 Modify:
 Change R201, R202, R207 to 22 Ohm for CODEC driver output.



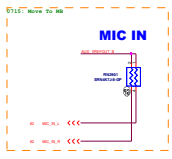
Close to Pin13



Close to Pin14



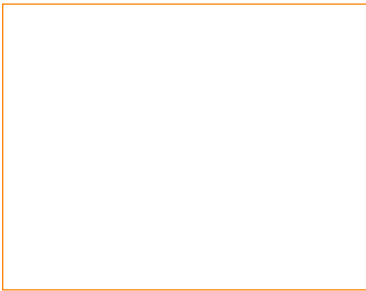
0206 EMU Reserve, Place Near R202



MIC IN


ANNIE Audio solution

Remove Annie Audio

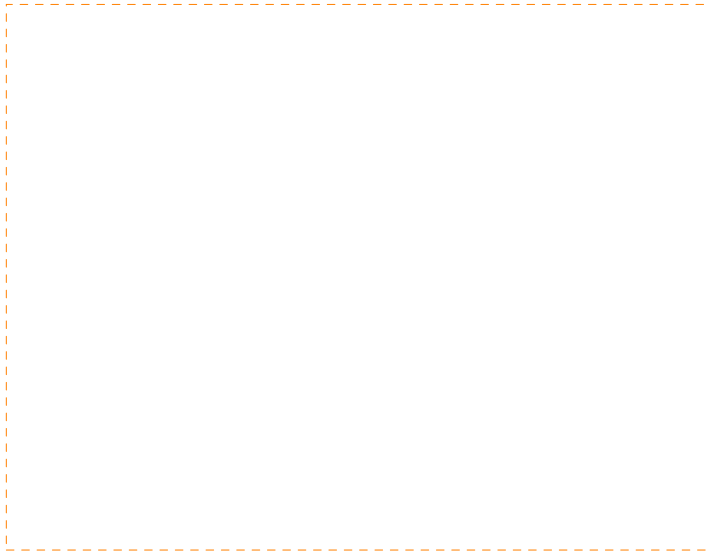


AUDIO OP AMPLIFIER


DQ15 AMD DIS SAMSUNG T1

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		AMP	
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA00		
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DG15 M12 In Daughter BD



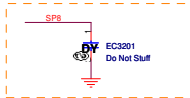
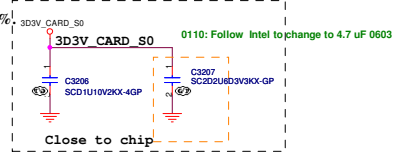
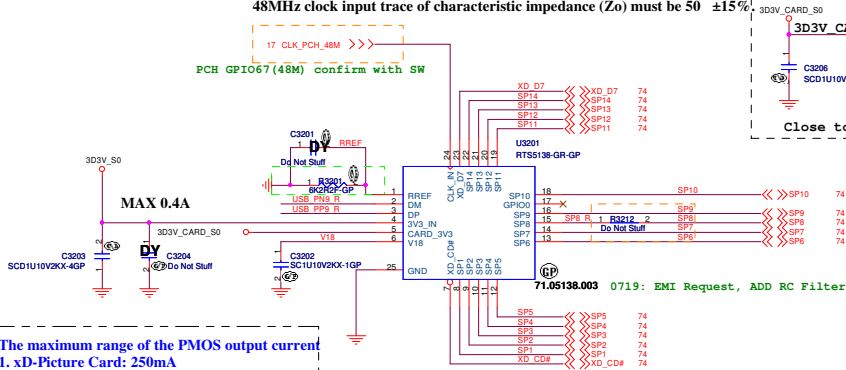
DG15 AMD DE SAMSUNG TI

		Wistron Corporation 21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
Title		LOM	
Size A3	Document Number	Rev X00	
Date: Thursday, May 28, 2011		Sheet	31 of 104

SSID = SDIO

48MHz clock input trace of characteristic impedance (Z_0) must be $50 \pm 15\%$

FCH GPIO67(48M) confirm with SW



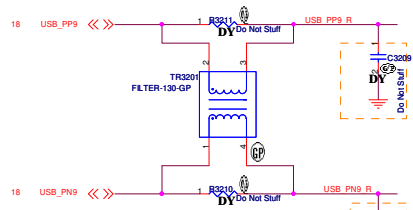
The maximum range of the PMOS output current

1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

The pin2 / pin3 (DM/DP) of RTSS138 chip trace layout with differential characteristic impedance (Z_{diff}) is $90\Omega \pm 10\%$

POWER TRACE

1. RTSS138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2. RTSS138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3. RTSS138: pin 6 (V18) trace fixed width is 12 mils (minimum). Keep the trace routing lengths as short as possible.
4. RTSS138: pin 1 (RREF) trace fixed width is 12 mils (minimum).
5. RTSS138: pin 1 (RREF) trace must far away 48MHz clock trace.
6. De-coupling and Bulk capacitor should place near to RTSS138 chip and Combo Socket.
7. It is recommended that use of ferrites bead on power trace.
8. Via size: Pad>=32 mils, Finished hole>=16 mils.



0103 Modify:
AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

0118 Modify:
Change TR3201 To 69.10118.001 due to layout limitation

D015 AMD DISAMSUNG T1

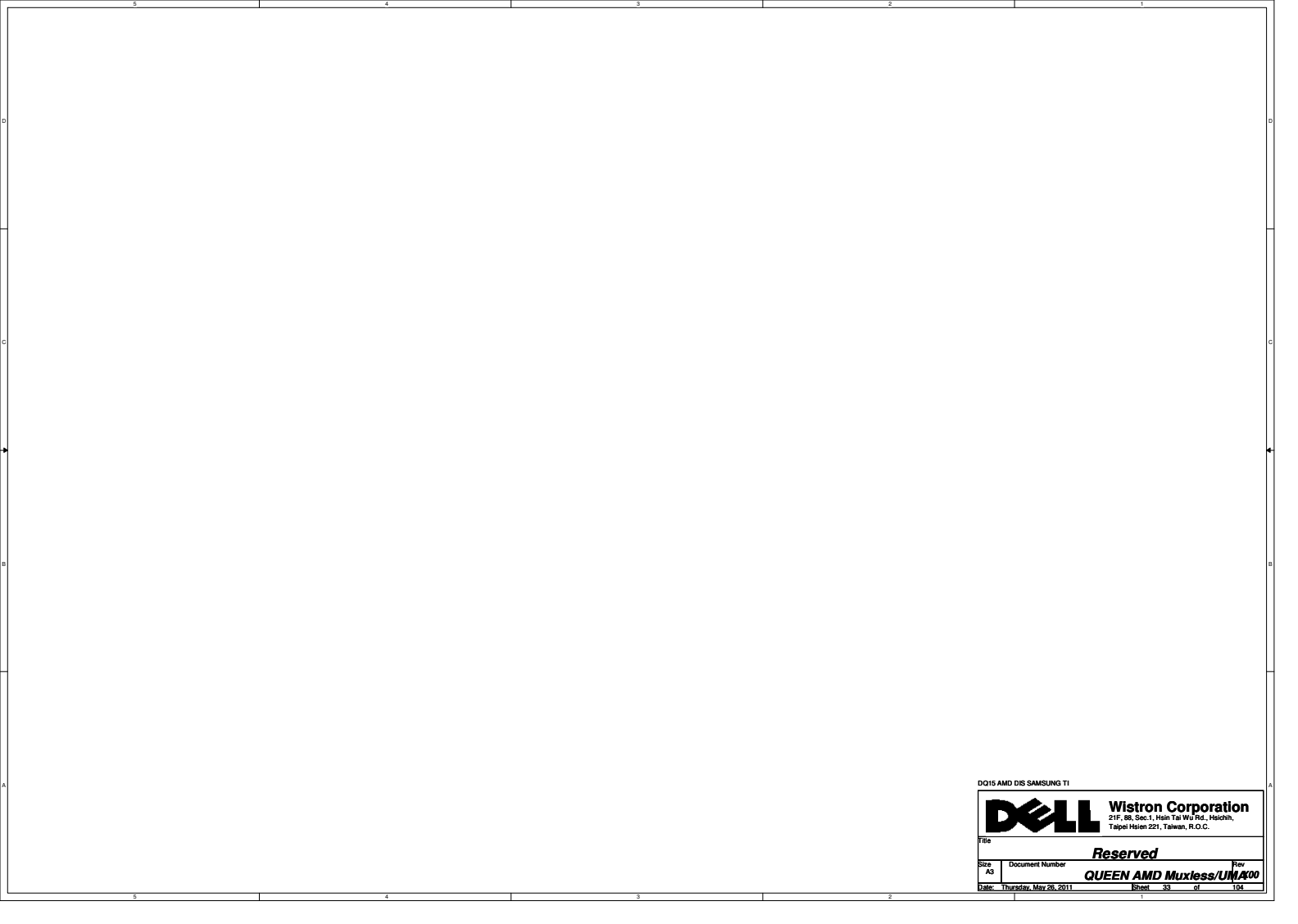
DELL Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C.

Reserved


File: _____
Rev: _____

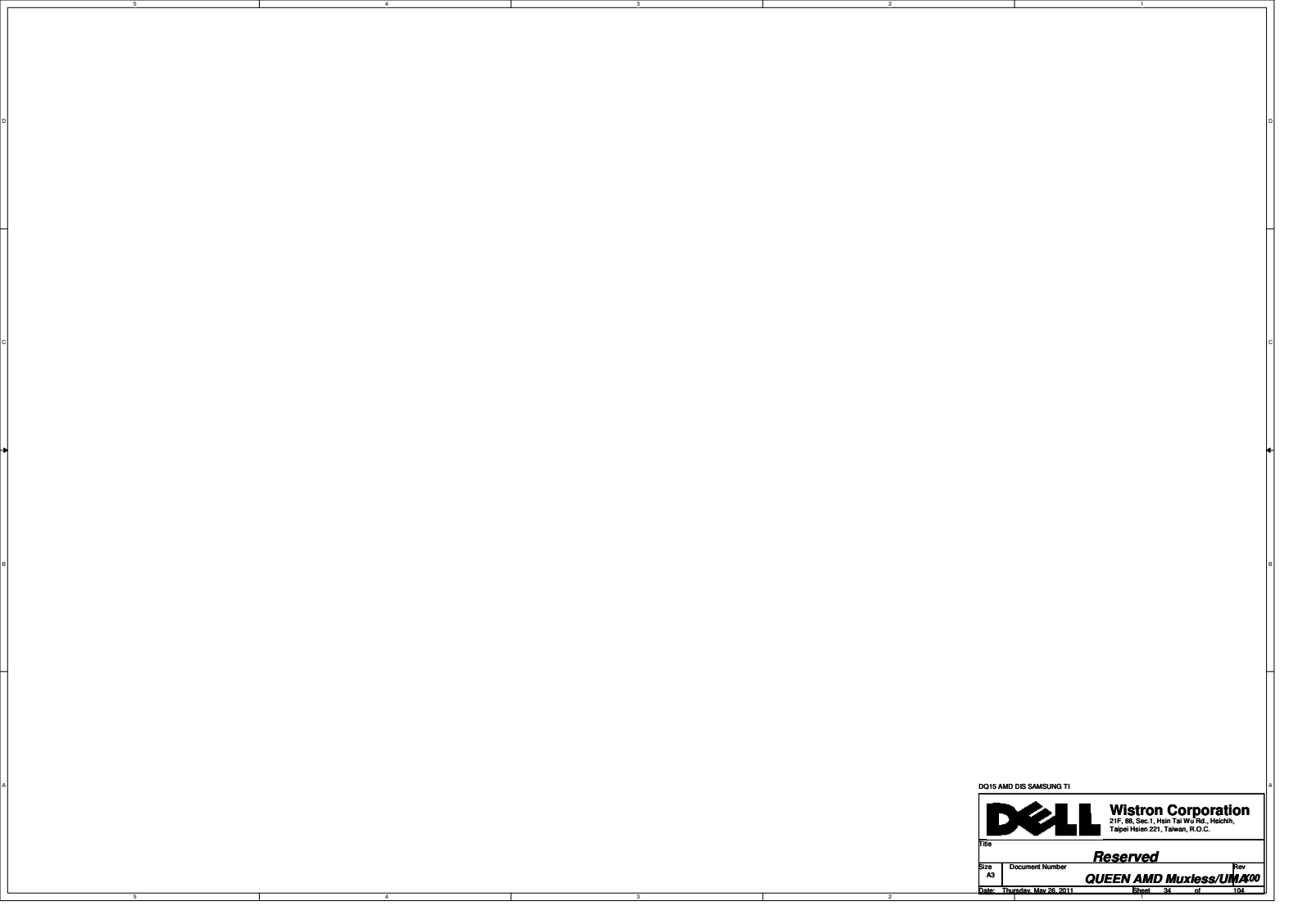
Doc No: _____ Document Number: _____
QUEEN AMD Muxless/UMA00

Date: Friday, May 27, 2011 Sheet: 32 of 104



DQ15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Hsien Tai Wu Rd., Hsuehlin, Taipei Hsien 221, Taiwan, R.O.C.	
File			
Reserved			
Size AS	Document Number QUEEN AMD Muxless/UMA00		Rev
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DQ15 AMD DIS SAMSUNG T1

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reserved			
File			Rev
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA00		
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A

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C

D

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DQ15 AMD DE SAMSUNG TI

		Wistron Corporation <small>21F, 8F, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.</small>	
		Reserved	
Title			
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA	X00	
Date: Thursday, May 28, 2011		Sheet	of
		35	104

A

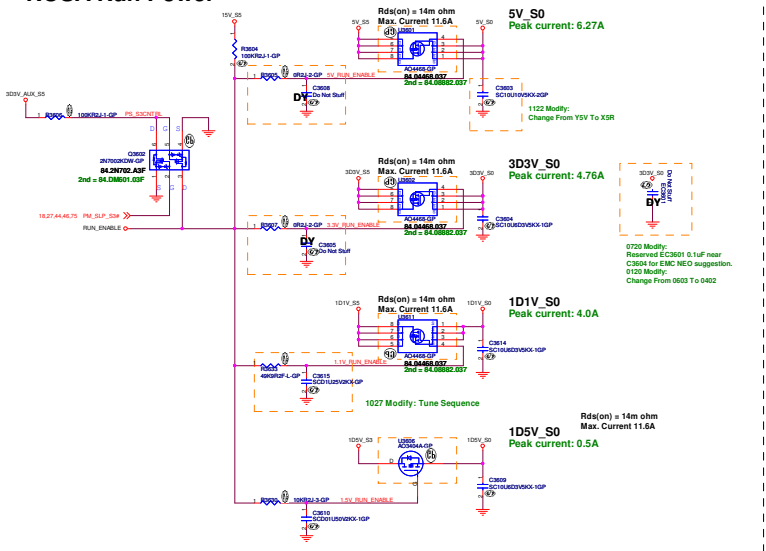
B

C

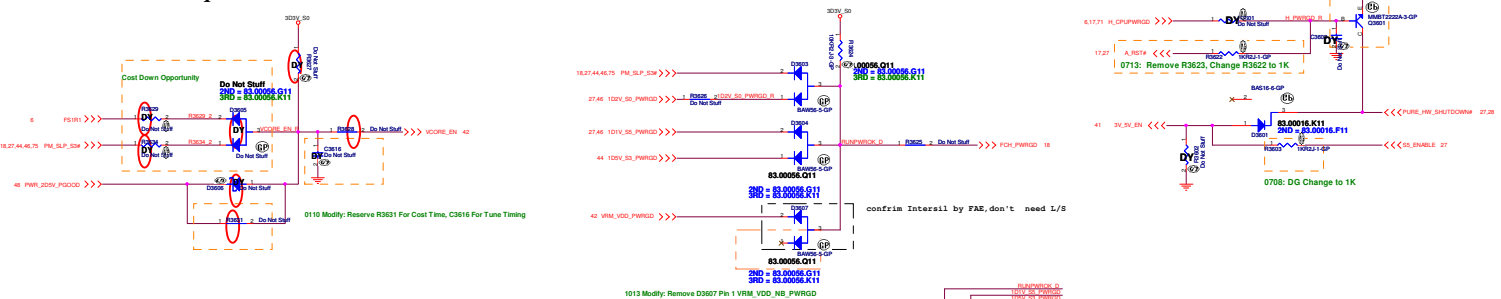
D

E

ROSA Run Power



Power Sequence



0109: EM Reserve, EC3602 Place Near P3625
0105: EM Reserve, EC3603 Place Near P3626
0106: EM Reserve, EC3604 Place Near D3601

0013: Add DS: SAMUNG T1

DELL Wistron Corporation
77E St. S&C1, Hua Tu, Hsinchu, Hsinchu, R.O.C.
Tapeel Hsien 221, Tainan, R.O.C.

Power On Logic

Document Number: QUEEN AMD Muxless/UMA X09

Rev: 1.00
Date: 1/26/2011
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5

4

3

2

1

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D

C

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A

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1

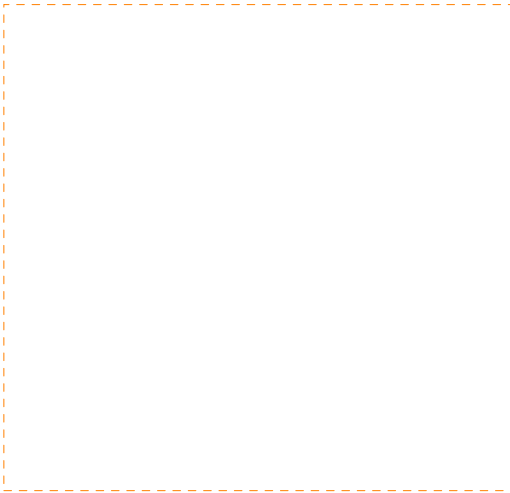
DQ15 AMD DIS SAMSUNG TI



Wistron Corporation
21F, 88, Sec.1, Main Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Plane Enable		
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00
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Thursday, May 26, 2011	37	104

Move To CRT BD



DD15 AMD DIS SAMSUNG TI



Wistron Corporation
21F, Sec. 1, Hsin Tai Wu Rd., Hsinshu,
Taipai Hsien 221, Taiwan, R.O.C.

File

DCIN JACK

Size Document Number

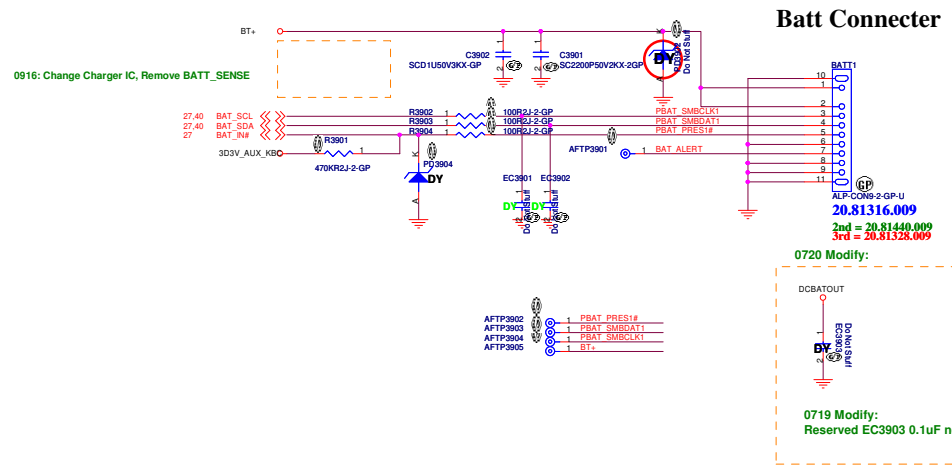
Custom

QUEEN AMD Muxless/UM100

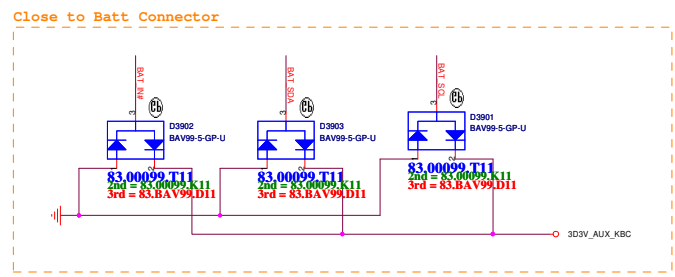
Date: Thursday, May 26, 2011

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SSID = BATT CONN



For actual location, need to be swap all pin



DQ15 AMD DIS SAMSUNG TI

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Taipei Hsien 221, Taiwan, P.R.O.C.

File **BATT CONN**

Size A3	Document Number QUEEN AMD Muxless/UMA	Rev X00
Date: Thursday, Mar 26, 2011	Sheet 39	of 104

SSID = Charger

EE need pull high and net name
0802 Rename H_PROCHOT#

627_H_PROCHOT#

X00 0415

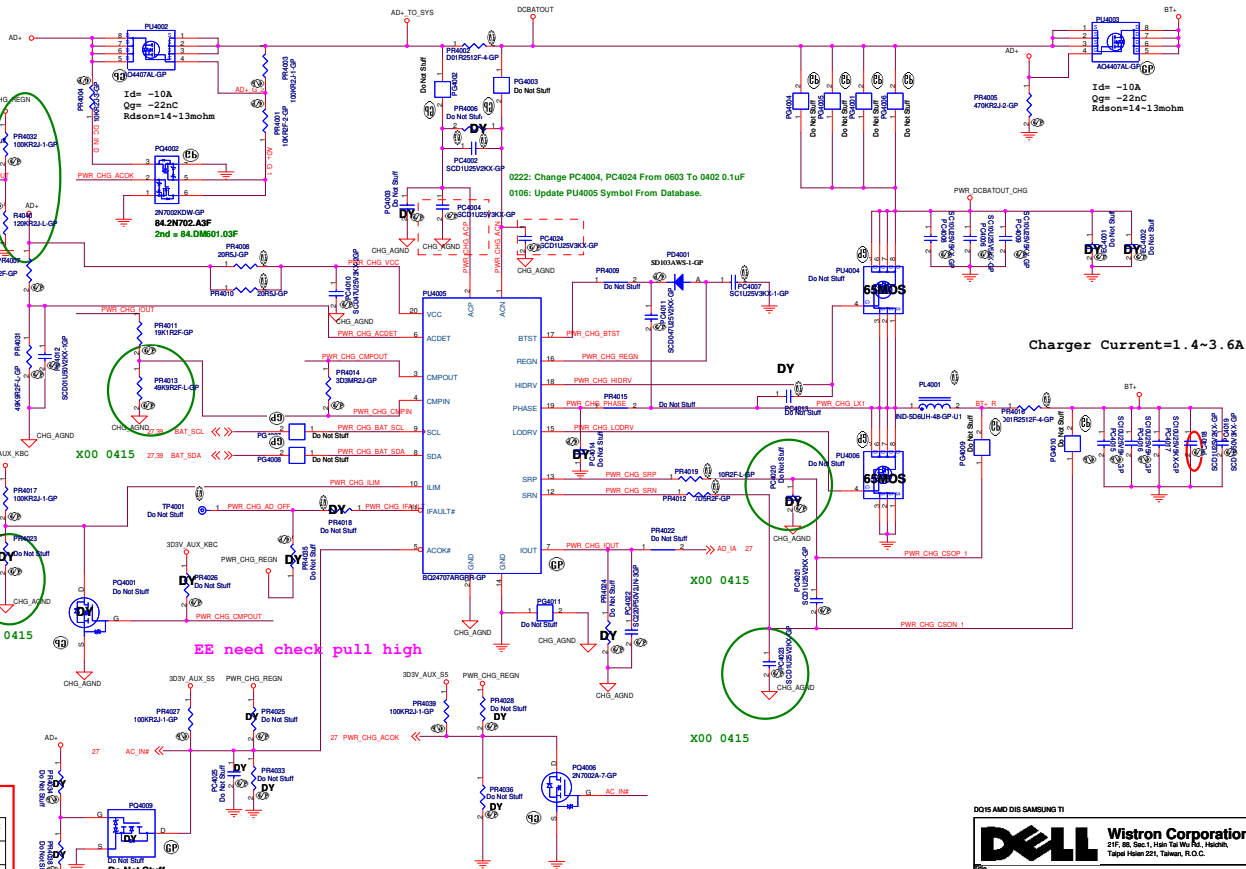
X00 0415

X00 0415

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

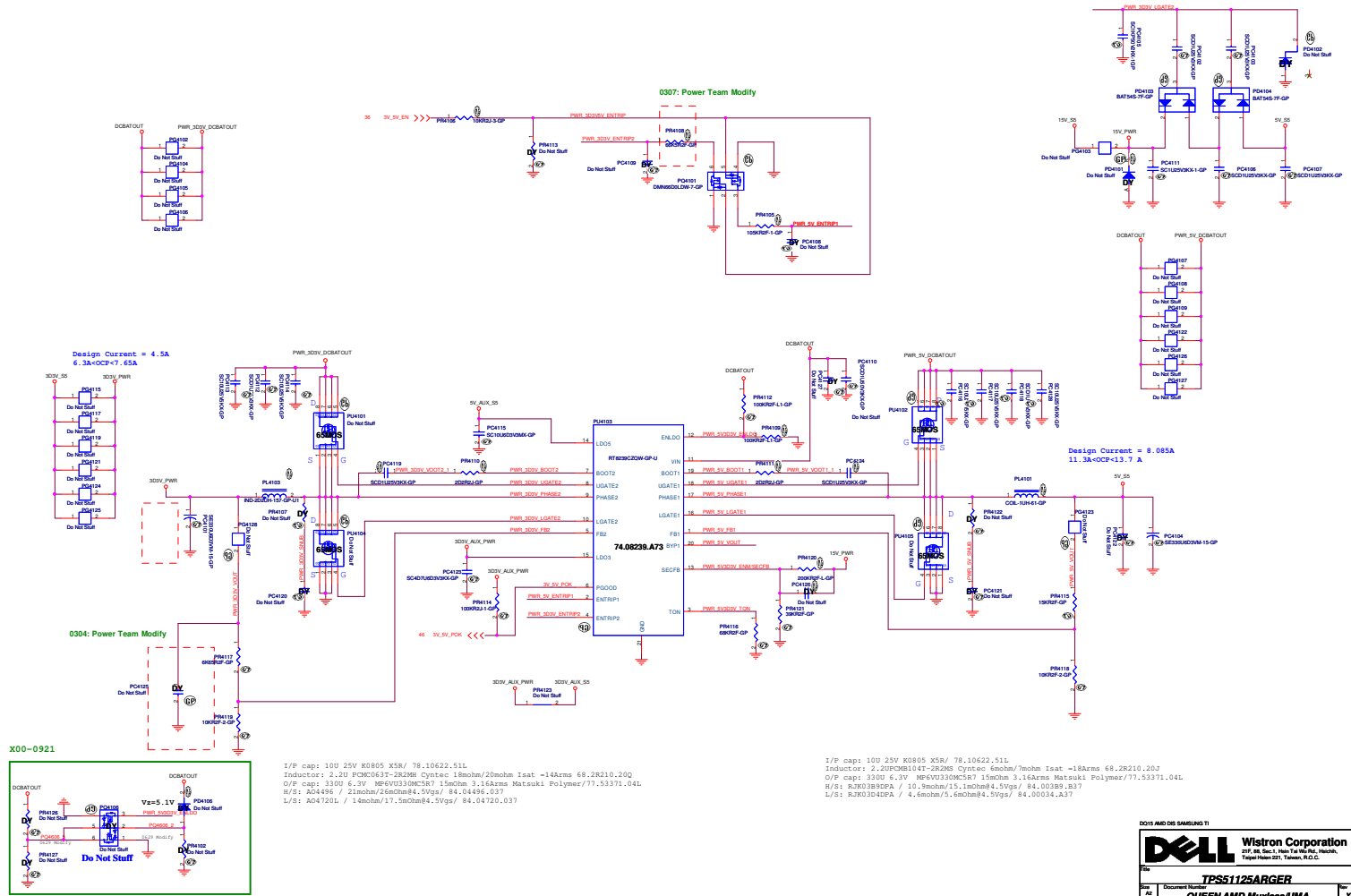
0120 Modify



DQ15 AMD DIS SAMPLING TI

Wistron Corporation
21F, 88, Sec. 1, Hsin Tu Wu Rd, Hsueh-Tai, Hsinchu City, Taiwan, R.O.C.

BQ24707RGRG4
Rev. 1.0
Date: 10/29/2011
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Design Current = 4.5A
6.3A@OCP+7.65A

Design Current = 8.085A
11.3A@OCP+13.7A

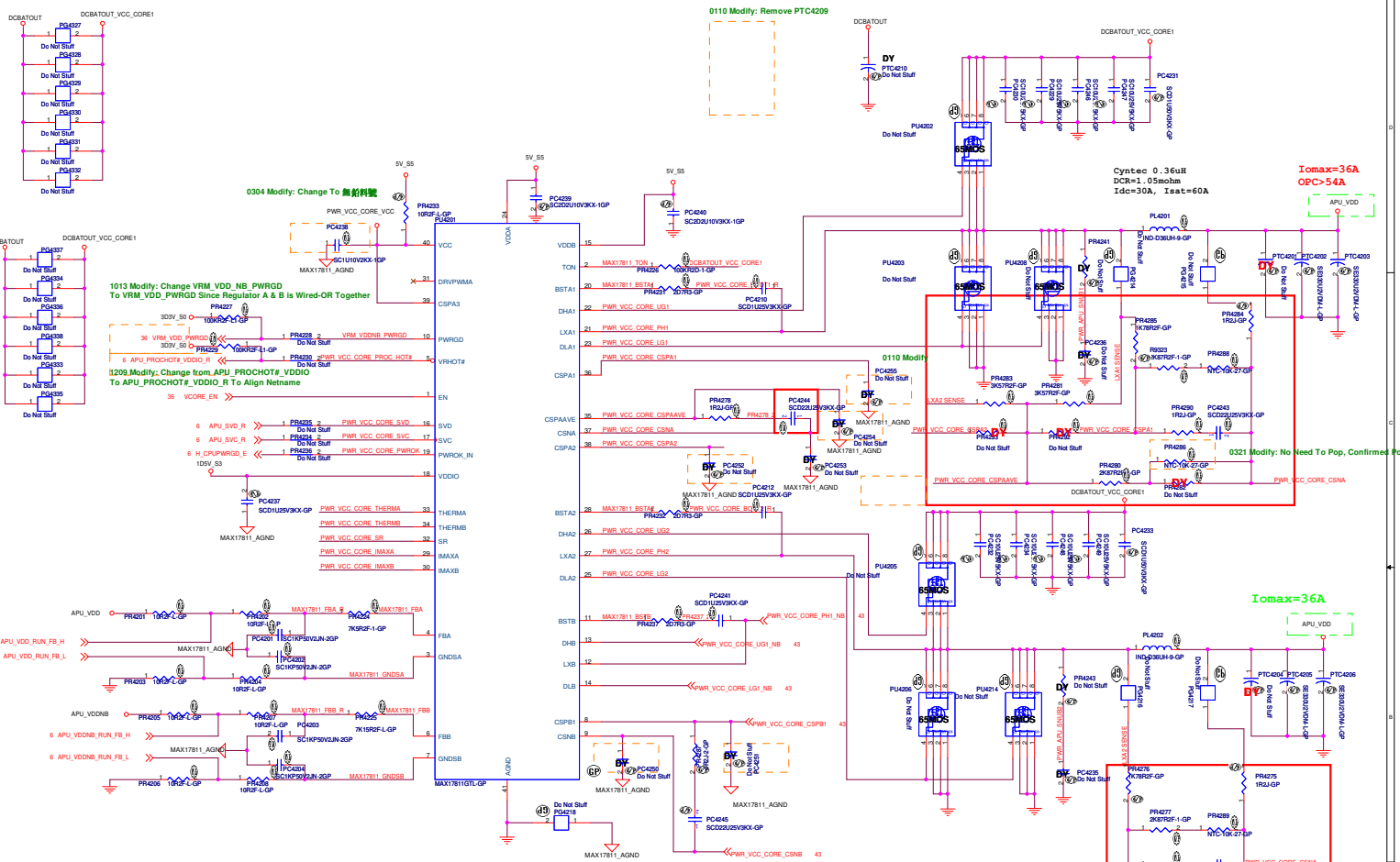
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC0437-2R2MH Cyntec 180ohm/20mhm Isat =14Arms 68.2R210.200
O/P cap: 3300 6.3V MP6V0330MC5R7 15ohm 3.14Arms Matsuki Polymer/77.53371.04L
H/S: AD4496 / 210ohm/26mOhm/4.5Vgs/ 84.04496.037
L/S: AD4720L / 14mhm/17.5mOhm/4.5Vgs/ 84.04720.037

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U P0801247-2R2MH Cyntec 6mhm/7mhm Isat =18Arms 68.2R210.200
O/P cap: 3300 6.3V MP6V0330MC5R7 15mhm 3.16Arms Matsuki Polymer/77.53371.04L
H/S: R2R0389DPA / 10.9mhm/15.1mOhm/4.5Vgs/ 84.00389.037
L/S: R2R0324DPA / 4.6mhm/9.6mOhm/4.5Vgs/ 84.00034.037

0319 PWR DS SAMSUNG TI

Wistron Corporation
 2/F, 88, Sec. 1, Hsin-Tai Rd., Hsinchu, Taiwan, R.O.C.

Part		TPSS112SARGER	
Doc. No.	Doc. Name	QUEEN AMD Mxless/UMA	
Rev.	Rev. No.	Rev. 1	Rev. 1



- 1 NTC**
 PR4280=2.87K
 PR4282=2.21K (DY)
 PR4281, PR4283=3.57K
 PC4244=0.22UF
 PR4285, PR4276=1.5K
 PR4279, PR4277=2K (DY)
 PR4286=NTC 10K
 PR4288, PR4289=NTC 10K (DY)
 PR4290, PR4291=0 ohm
 PR4292, PR4393=100ohm (DY)
- 2 NTC**
 PR4280=DY
 PR4282=DY
 PR4281, PR4283=DY
 PC4244=1nF
 PR4285, PR4276=1.78K
 PR4279, PR4277=2.78K
 PR4286=NTC 10K (DY)
 PR4288, PR4289=NTC 10K
 PR4290, PR4291=1 ohm
 PR4292, PR4393=100 ohm

DD19 AMD OS Samsung TI

		Wistron Corporation <small>23F, Sec. 1, Hsin-Tai Rd, Hsinchu, Taiwan, R.O.C.</small>
Title		VDDR & VDDP
A1	Document Number	QUEEN AMD Muxless UM & x90
Date	Revised	Mar 26, 2011
Rev#		01

OO15 AMD DS SAMUNG TI

DELL **Wistron Corporation**
23F, 8th, Sec. 1, Hsin-Tai Rd, Hsin-Tai, Hsinchu,
Taiwan 30511, Taiwan, R.O.C.

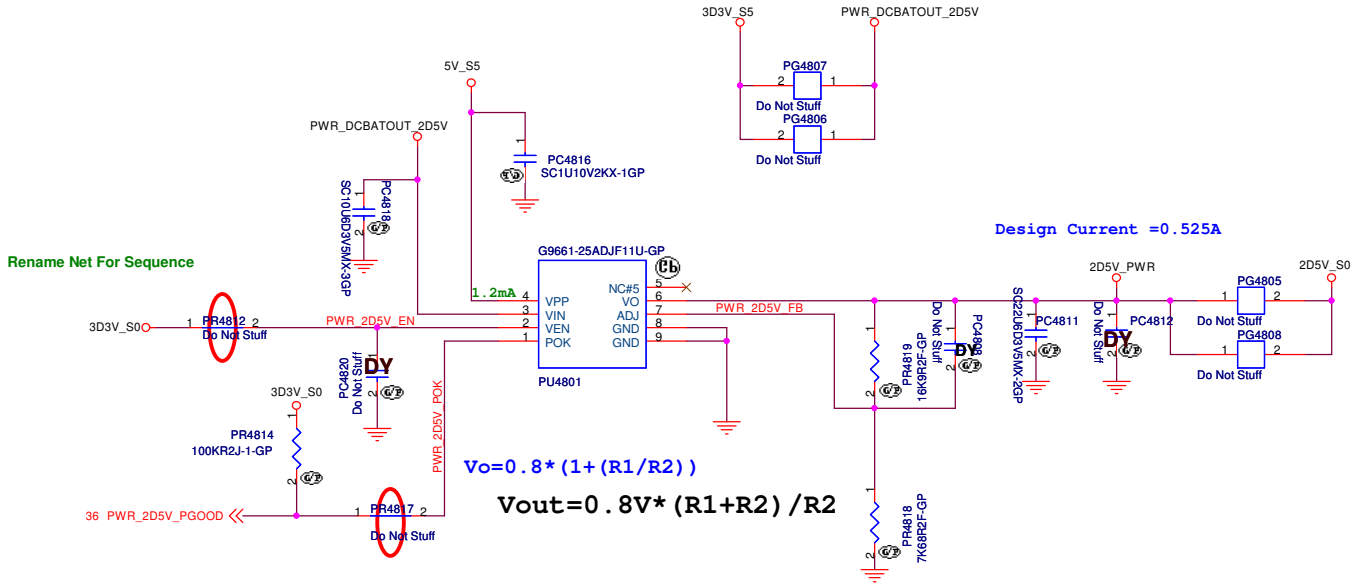
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Part **QUEEN AMD Muxless/UMA X00**

Date: Thursday, March 26, 2014 Page: 02 of 02

SSID = PWR.Plane.Regulator_2p5v VGA 1V

G9661 for 2D5V_S0



DQ15 AMD DIS SAMSUNG TI



Title		
2D5V_S0		
Size	Document Number	Rev
A4		
QUEEN AMD Muxless/UMA00		
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Remove For M12 Spec & Put In Daughter BD




Remove For M12 Spec & Put In Daughter BD



Remove For M12 Spec & Put In Daughter BD



DQ15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taippei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Board Connector			
Size	Document Number	Rev	
Custom	QUEEN AMD Muxless/UMA	X00	
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Remove EDP



LCD POWER CIRCUIT

Remove EDP



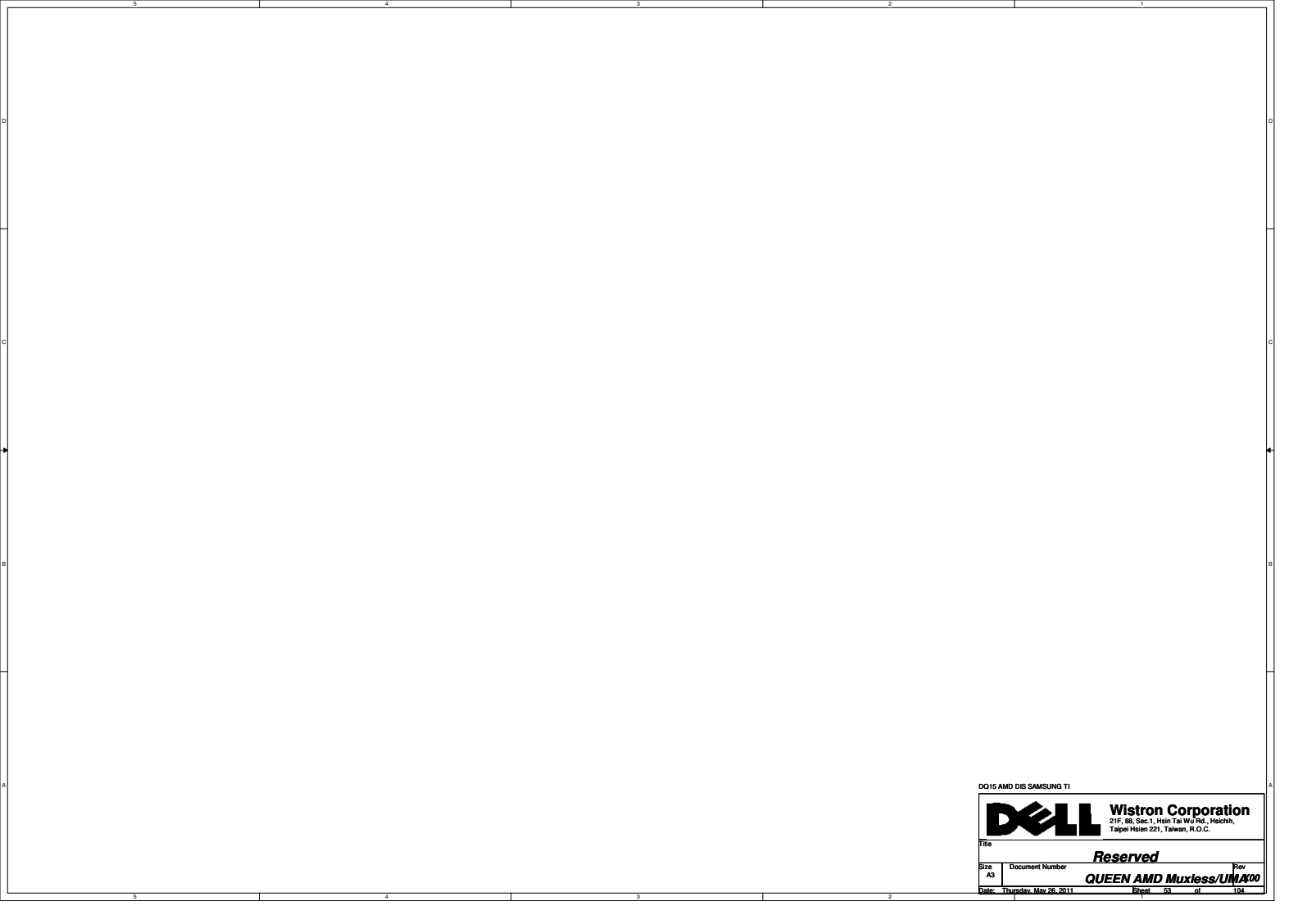
Rosa team

Remove EDP




DQ15 AMD D15 SAMSUNG TI

DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File		eDP	
Size	Document Number	Rev	
Custom			
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DQ15 AMD DIS SAMSUNG T1

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Reserved	
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA00		
Date:	Thursday, Mar 26, 2011	Sheet	53 of 104

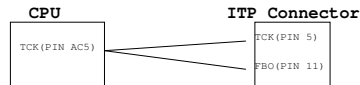
DO15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Main Tai Wu Rd., Hsiehshih, Taippei Hsien 221, Taiwan, R.O.C.
Title		Reserved
Size	Document Number	Rev
A3		
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



DQ15 AMD DE SAMSUNG TI

		Wistron Corporation <small>21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taippei Hsien 301, Taiwan, R.O.C.</small>	
Title ITP			
Size A3	Document Number QUEEN AMD Muxless/UMA		Rev X00
Date: Thursday, May 28, 2011		Sheet 55	of 104

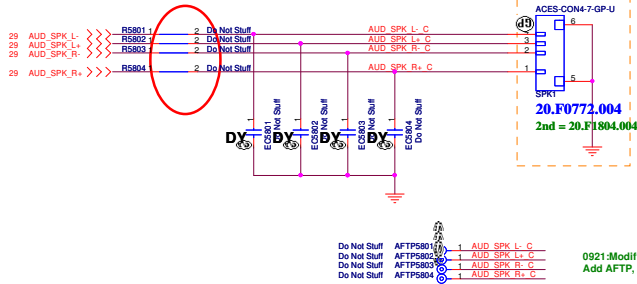
0715 Modify:
 Change ECS801-EC5804 to 100p 0402
 and default un-stuff.
 Add R5801-R5804 between SPK signal and connector
 for EMC NEO suggest.

0914 Modify:
 Change SPK1 to 20.F0772.004 from
 20.F1647.004 from Double updated.

0921 Modify:
 Modify Pin Define Base On DQ15 Intel

1110 X02 Modify:
 Add 2nd 20.F1804.004 on SPK1 from
 ME updated connector list.

Speaker Connector



MB CONN. (WIRE)

Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

DQ15 AMD DE SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichm, Taipei Hsein 221, Taiwan, R.O.C.	
		Audio Jack	
File			
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA	X00	
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LAN CONN in Daughter BD

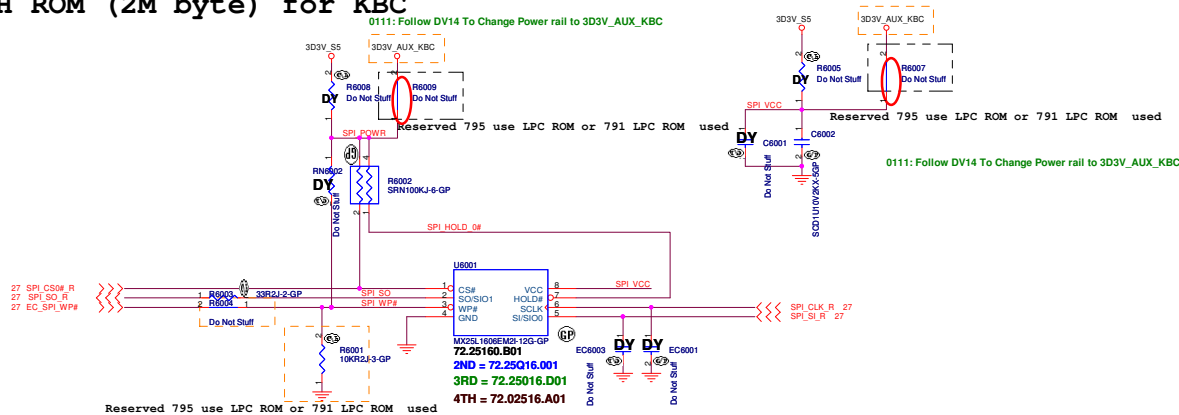


DQ15 AMD DIS SAMSUNG TI

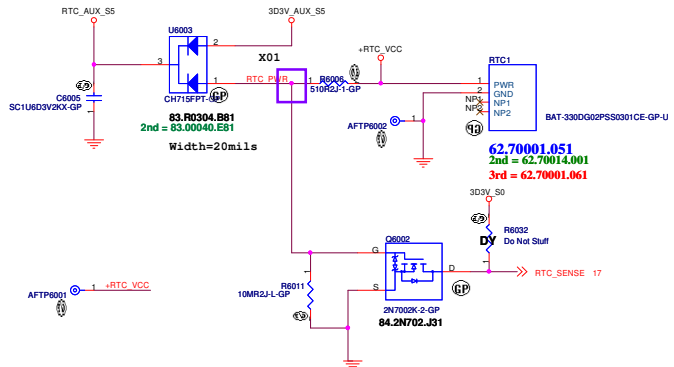
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		LAN CONN	
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA00		
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SSID = Flash.ROM

SPI FLASH ROM (2M byte) for KBC



SSID = RBATT



0105 Modify:
updated RTC1 symbol and footprint from
data base:
1122 Modify:
Add O6002, R6010, R6011 for FACTORY RTC detect function.
0111: Change RTC Schematic As DV14 Brazo, SW Suggest.

DQ15 AMD DE SAMSUNG T1

		21F, 8F, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 301, Taiwan, R.O.C.	
		Flash/RTC	
File	Document Number	Rev	
Size	QUEEN AMD Muxless/UMA	X00	
Date: Thursday, May 28, 2011	Sheet	60	of 104

SSID = USB

DQ15 AMD DIS SAMSUNG T1



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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size

Document Number

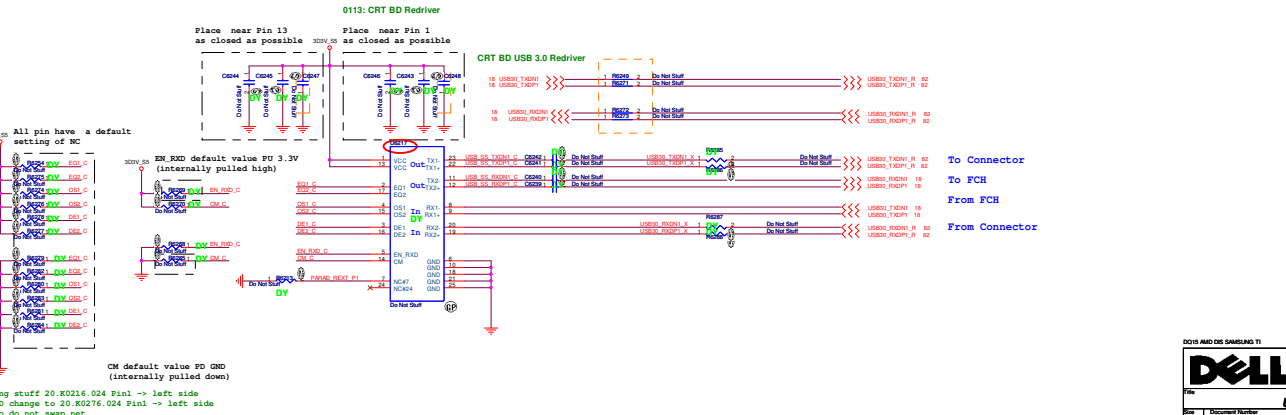
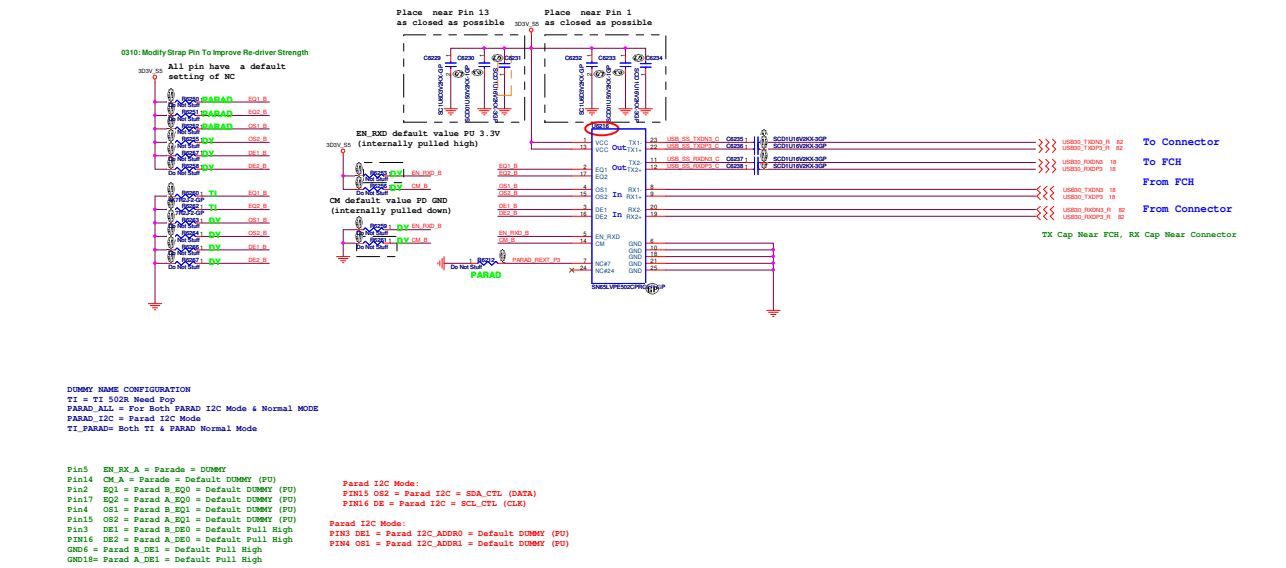
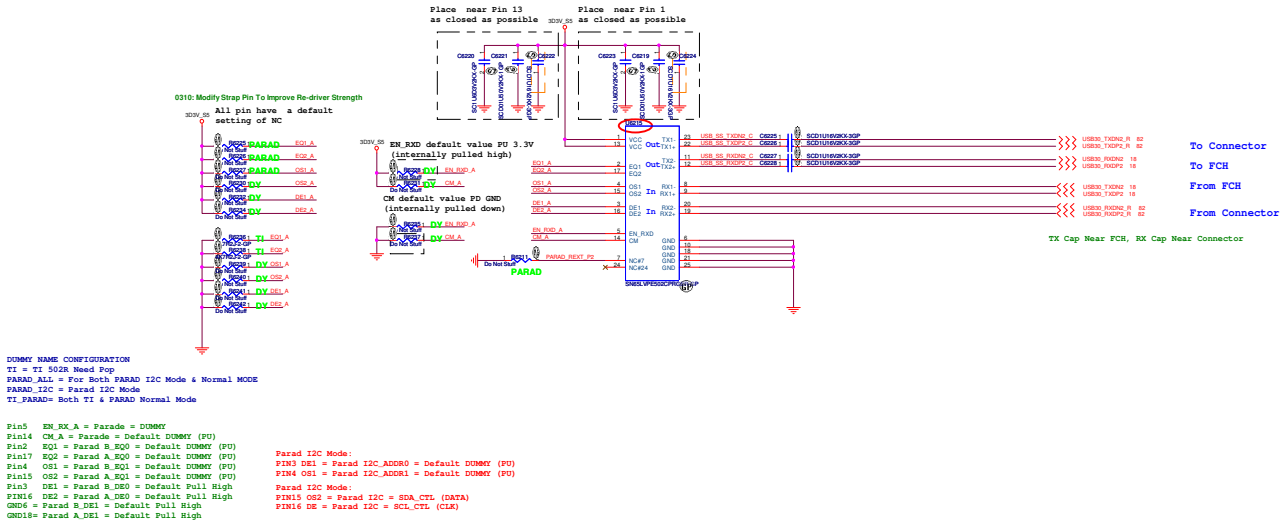
Rev

QUEEN AMD Muxless/UMA

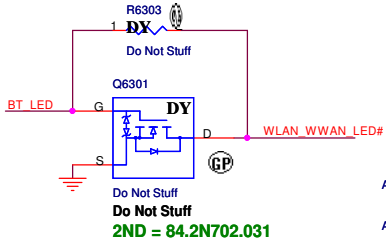
X00

Date: Thursday, May 26, 2011

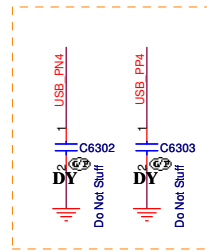
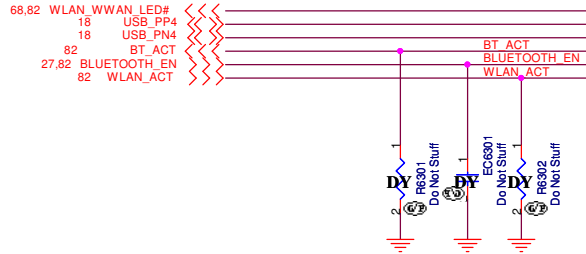
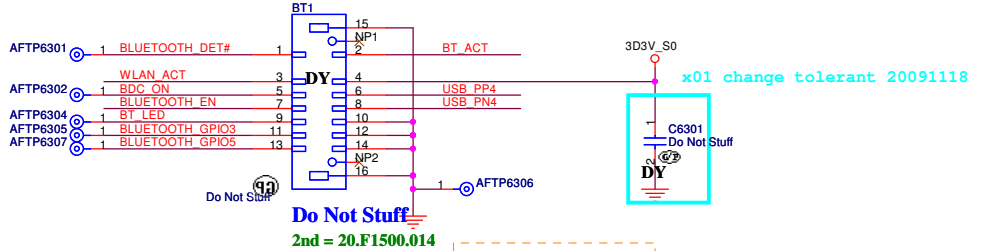
Sheet 61 of 104



SSID = User.Interface



Bluetooth Module conn.



- AFTP6309 1 WLAN_ACT
- AFTP6310 1 BLUETOOTH_EN
- AFTP6308 1 BT_ACT
- AFTP6311 1 3D3V_S0
- AFTP6312 1 USB_PP4
- AFTP6313 1 USB_PN4

0906 Modify:
 Dell Peter already confirmed DQ15 and DN15 will not support Bluetooth BT365, only support combo Wireless+BT. Please DUMMY Bluetooth connector(BT1) and stand off (HBT1) and related components.

0103 Modify:
 AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

DQ15 AMD DIS SAMSUNG T1

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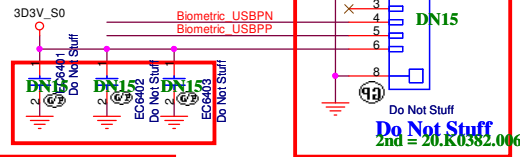
Title: **Bluetooth**

Size A4	Document Number QUEEN AMD Muxless/UMA	Rev X00
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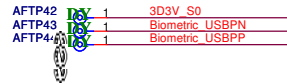
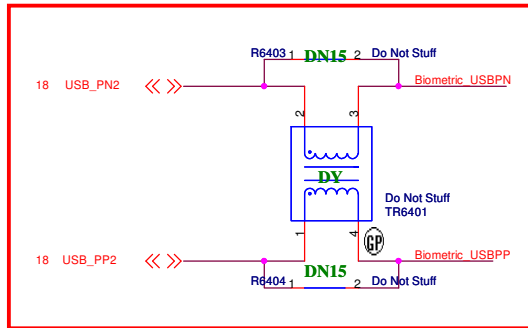
Finger Printer Connector

Finger Printer Connector

1124 X02 Modify:
 Add EC6402 0.1uF, EC6403 180pF and stuff EC6401
 47pF from RP fine tune result.



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0



DQ15 AMD DIS SAMSUNG T1



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A4		QUEEN AMD Muxless/UMAX00	
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WLAN CONN In Daughter BD




DQ15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File		WLAN	
Size	Document Number	Rev	
A3			QUEEN AMD Muxless/UMA00
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Remove For DG12 M12 SPEC



DG15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Hsien Tsa Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C.	
File		WWAN	
Size AS	Document Number	Rev	
QUEEN AMD Muxless/UMA00			
Date: Thursday, May 26, 2011	Sheet 66	of 104	

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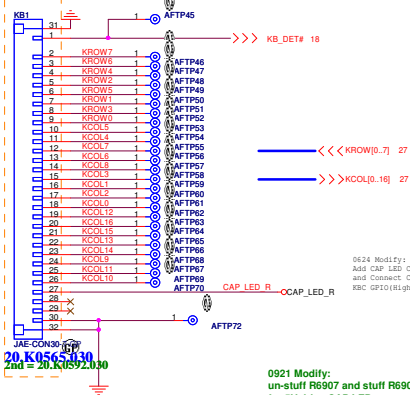
DQ15 AMD DE SAMSUNG TI

		Wistron Corporation <small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
Reserved			
Size A3	Document Number QUEEN AMD Muxless/UMA		Rev X00
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1122 Modify:
Add 2nd 20.K0592.030 on KB1 from ME updated connector list.

Internal KeyBoard Connector

0630 Modify:
Change KB1 part number to 20.K0565.030 base on ME updated BOM and GSP.



SSID = Touch.Pad

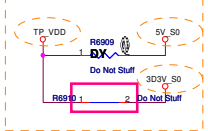
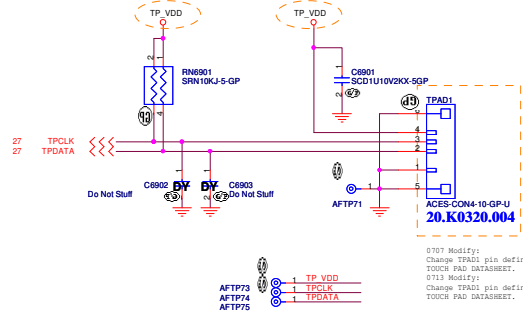
0715 Modify:
Add R6908,R6909 for TPAD1 co-layer power option.

0109 Modify:
Change TP_VDD To 3D3V_S0, Follow Intel

0624 Modify:
Removed TP LOCKED CONTROL combin with KEYBOARD Function Key.

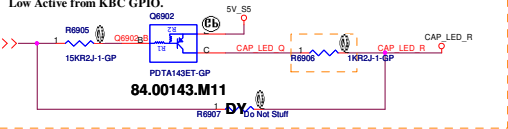
0713 Modify:
Change TPAD1 power source to 3D3V_S0 from 5V_S0 base on DELL latest spec A92.

TouchPad Connector



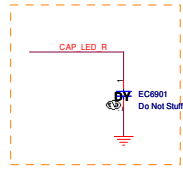
MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

CAP LED CONTROL

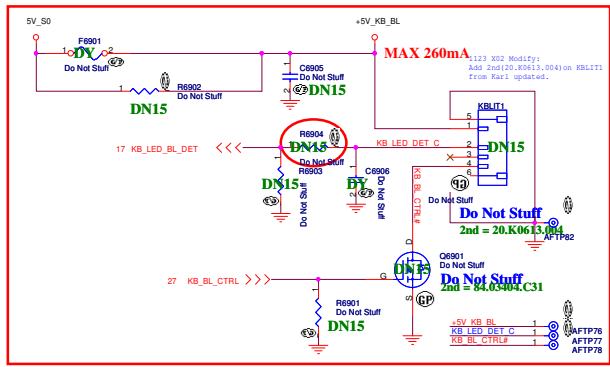


MB CONN. (FFC)
Pin1 +5V_KB_BL
Pin2 KB_LED_DET_C
Pin3 NC
Pin4 KB_BL_CTRL#

0719: EMI Request



KB Backlight Connector



DC15 AMD DIS SAMSUNG T1

DELL Wistron Corporation
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File: **Key Board/Touch Pad**

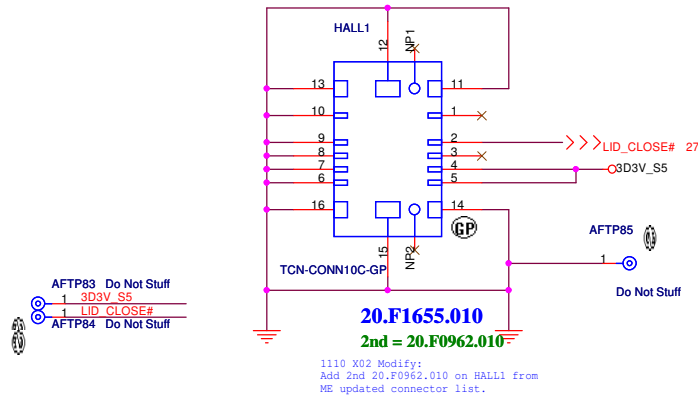
Size: Document Number
Customer: **QUEEN AMD Muxless/UMA** Rev: **X00**

Date: Thursday, May 26, 2011 Sheet: 60 of 104

SSID = Hall.Sensor

0906 Modify:
HALL SENSOR move to small board at X01 stage,so
Removed HALLSW1 related circuit and add HALL1
connector.

1122 Modify:
Add 2nd 20.F0962.010 on HALL1 from
ME updated connector list.



DQ15 AMD DIS SAMSUNG T1

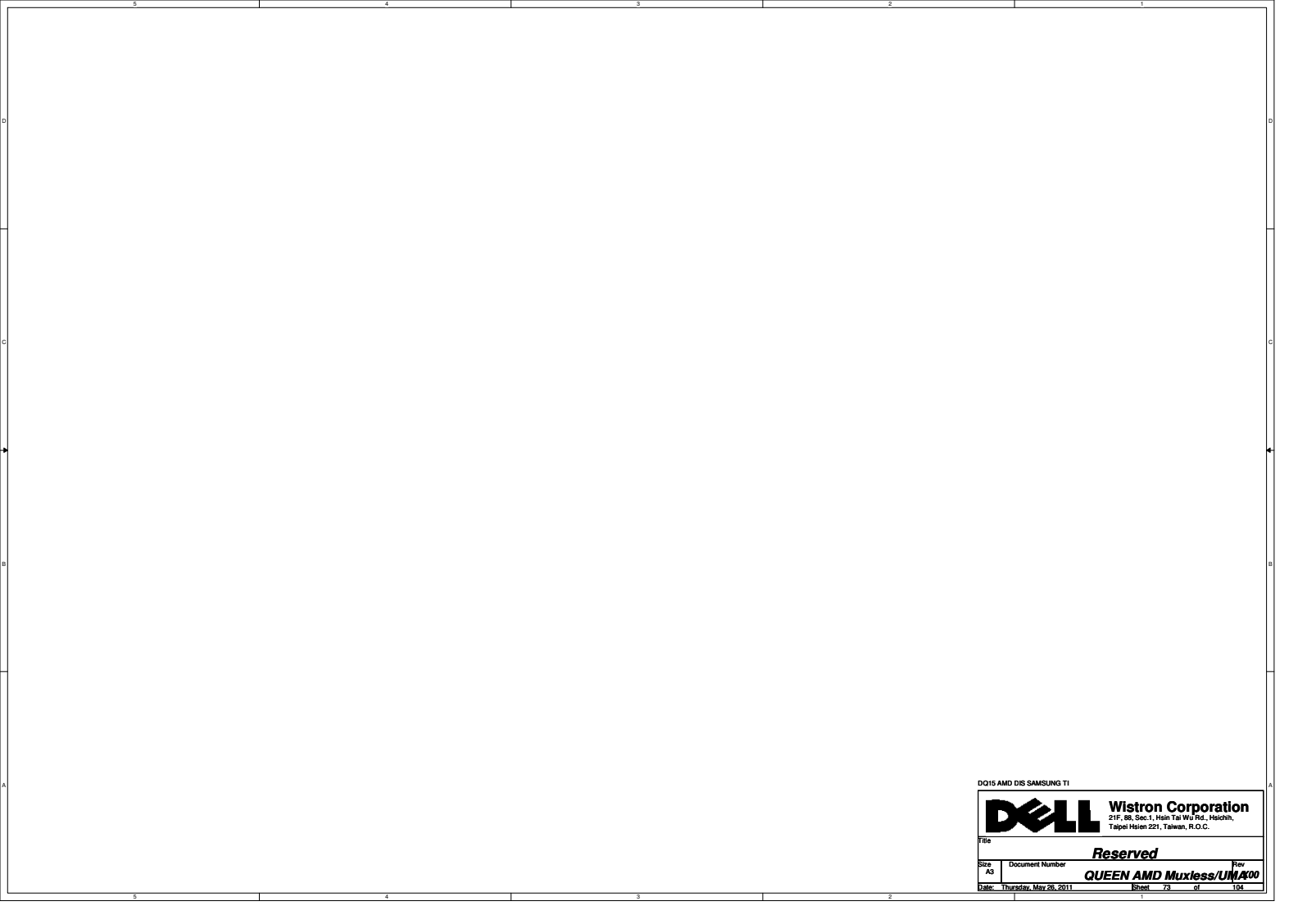


Title		
Hall Effect Sensor		
Size	Document Number	Rev
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DQ15 AMD DE SAMSUNG TI

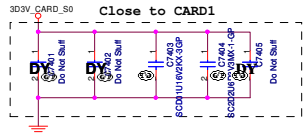
		Wistron Corporation <small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.</small>
RESERVED		
Title		
Size A3	Document Number QUEEN AMD Muxless/UMA	Rev X00
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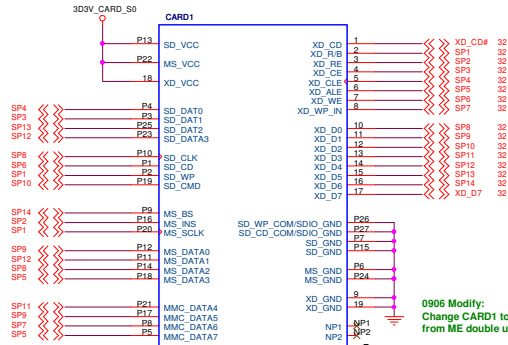
DQ15 AMD DIS SAMSUNG TI

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Reserved			
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SSID = SDIO



SD/XD/MS/MMC+ Card Reader

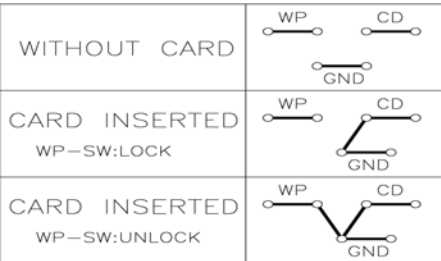


0906 Modify:
Change CARD1 to 20.I0129.001 from ME double updated latest DXF&EMN on X01.

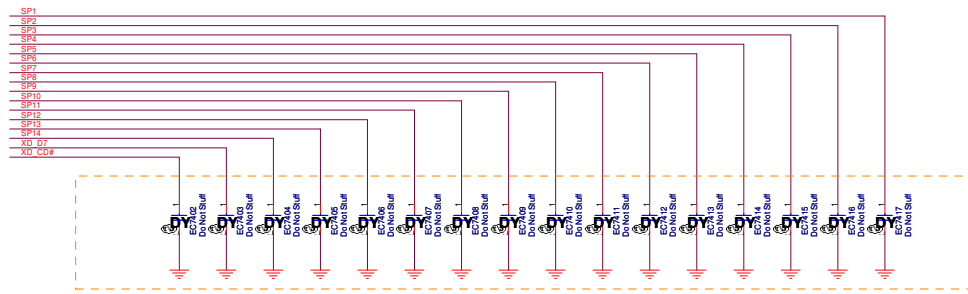
0928 Modify:
Updated CARD1 footprint to R013-P12-HM-1 from data base updated footprint.

1122 Modify:
Add 2nd 20.I0135.001 on CARD1 from ME updated latest connector list.

CARD-PUSH-46P-1-GP-U
20.I0129.001
2nd = 20.I0135.001
PCB Footprint = R013-P12-HM-1



For EMI Reserved



0913: Schematic Score Card Suggest Cap Less Than 10P

20.I0129.001			
Pin	TYPE	FUNCTION	RTSS138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT1	SP13
P26	SD	SD-WP COM	GND
		SDIO GND	GND
P27	SD	SD-CD COM	GND
		SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R#B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

D015 AMD DE SAMSUNG TI

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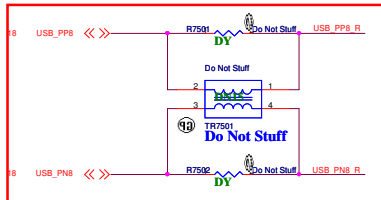
File: **CARD Reader CONN**

Size A3 Document Number **QUEEN AMD Muxless/UMA** Rev **X00**

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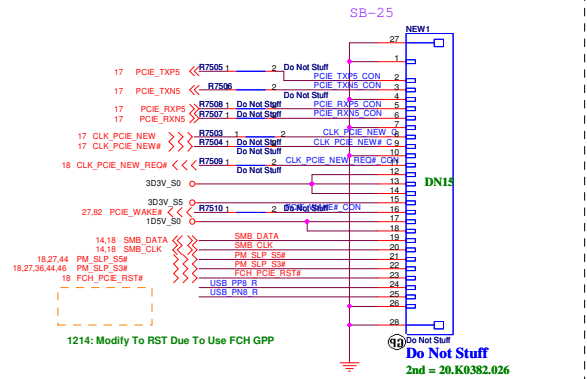
SSID = ExpressCard

1123 X02 Modify:
 Change TR7501 OH choke to 49.15103.041
 and un-stuff R7501, R7502 from EMC Req Suggestion.
 Change R7501, R7502 to 0603 from 9402.
 1123 X02 Modify:
 SMD TR7501 pin14 and pin24 each other
 base on Connce swap report.



Do Not Stuff	AFTT107	1	3D3V_S5
Do Not Stuff	AFTT126	1	3D3V_S6
Do Not Stuff	AFTT130	1	1D5V_S0
Do Not Stuff	AFTT138	1	USB_PNB_R
Do Not Stuff	AFTT139	1	USB_PPB_R
Do Not Stuff	AFTT140	1	CLK_PCIE_NEW_REDM_CON
Do Not Stuff	AFTT141	1	SMB_CLK
Do Not Stuff	AFTT142	1	SMB_DATA
Do Not Stuff	AFTT143	1	PM_SLP_S3#
Do Not Stuff	AFTT144	1	PM_SLP_S5#
Do Not Stuff	AFTT145	1	FCH_PCIE_RST#
Do Not Stuff	AFTT146	1	CLK_PCIE_NEW#_C
Do Not Stuff	AFTT147	1	CLK_PCIE_NEW#_N
Do Not Stuff	AFTT148	1	PCIE_TXNS_CON
Do Not Stuff	AFTT149	1	PCIE_RXNS_CON
Do Not Stuff	AFTT150	1	PCIE_TXNS_CON
Do Not Stuff	AFTT151	1	PCIE_RXNS_CON
Do Not Stuff	AFTT152	1	PCIE_WAKE#_CON

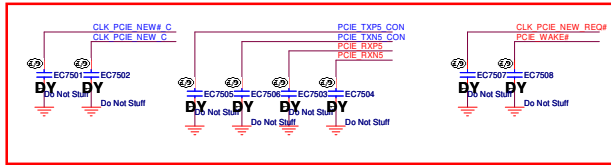
1D5V_S0_CARD Max. 650mA, Average 500mA.
 3D3V_S0_CARD Max. 1300mA, Average 1000mA
 3D3V_S5_CARDAUX Max. 275mA



1214: Modify To RST Due To Use FCH GPP

Do Not Stuff
 2nd = 20.K0382.026

For EMI



DG15 AMD DIS SAMSUNG TI

DELL Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

File: **ExpressCard**

Rev A3 Document Number: **QUEEN AMD Muxless/UMA** Rev X00

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DQ15 AMD DIS SAMSUNG T1



Wistron Corporation
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Title

Reserved

Size
A4

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Rev

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DQ15 AMD DIS SAMSUNG TI



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DQ15 AMD DIS SAMSUNG T1



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Rev

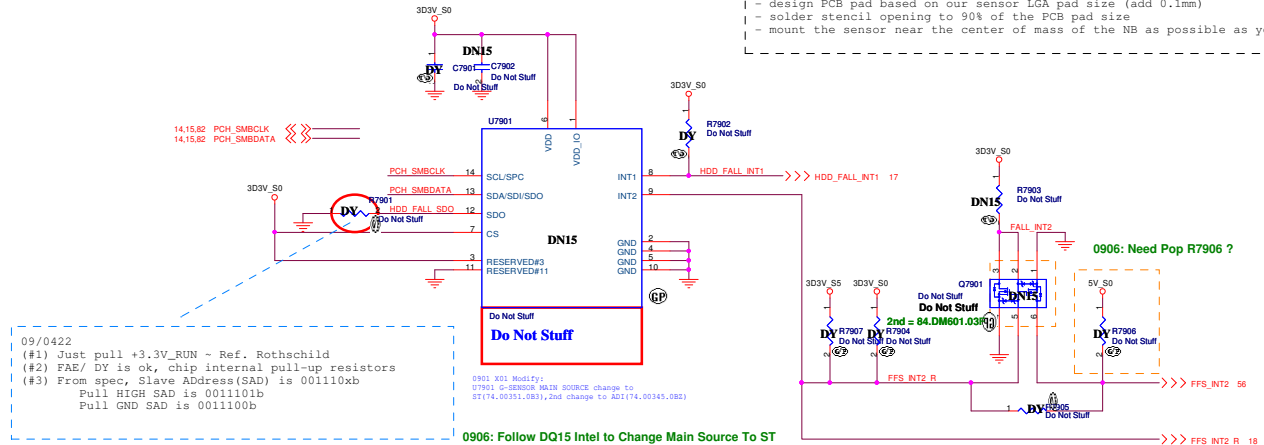
QUEEN AMD Muxless/UMA00

Date: Thursday, May 26, 2011

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SSID = User.Interface

Free Fall Sensor



Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

5

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3

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D

C

C

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B

A

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DQ15 AMD DIS SAMSUNG TI



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Title		Reserved	
Size	Document Number	Rev	
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DQ15 AMD DIS SAMSUNG TI



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Title

UNUSED PARTS/EMI Capacitors

Size

A4

Document Number

QUEEN AMD Muxless/UMA

Rev

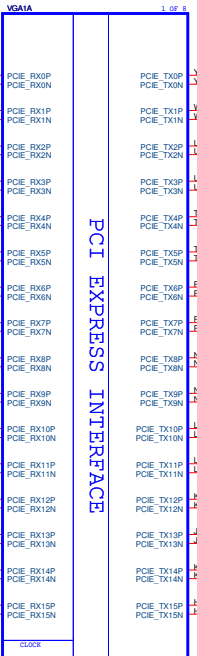
X00

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4 PEG_TXP[8..15] >>>
4 PEG_TXN[8..15] >>>

>>> PEG_RXP[8..15] 4
>>> PEG_RXN[8..15] 4



PCI EXPRESS INTERFACE

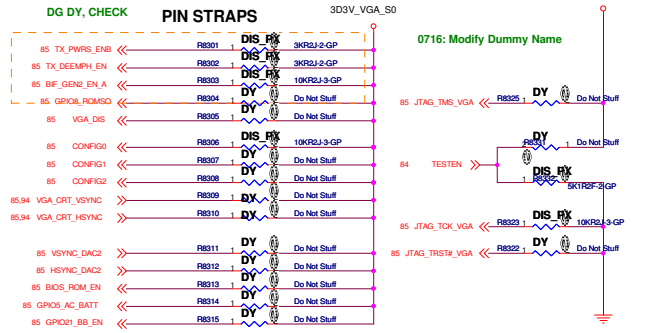
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	X	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSNC		X	1

RECOMMENDED SETTINGS
(#-DO NOT INSTALL RESISTOR
X-INSTALL 3K RESISTOR
- DESIGN DEPENDANT
NA=NOT APPLICABLE)

Full Tx output swing. Must be pulled to 3.3 V at reset using ~3-K (5%) resistor.



PE_GP100	FX3_0	FX4_0
IGPU	L	H
DGPU	H	H

JTAG SIGNAL OPTION - for option2

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

0113: Remove APU_RST# Level Shift

1008: Add Level Shift For APU_RST# To 3.3V

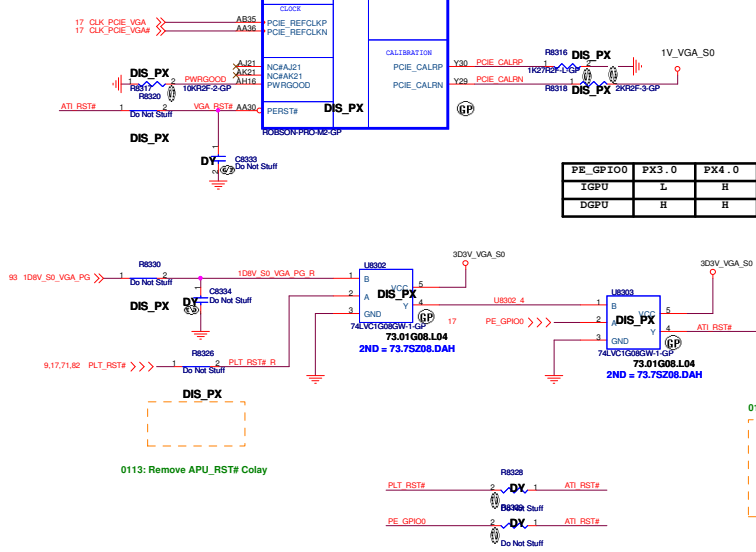
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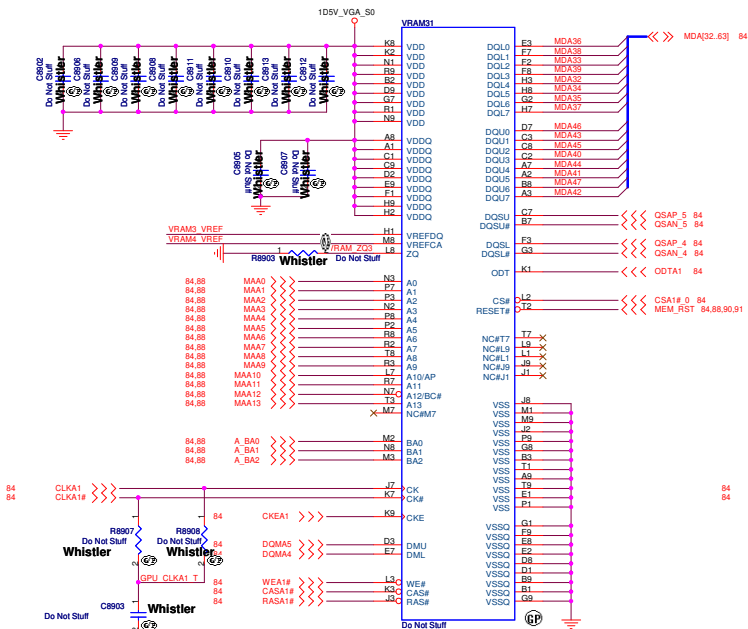
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Docu: **GPU_PCIE/STRAPPING(1/5)**

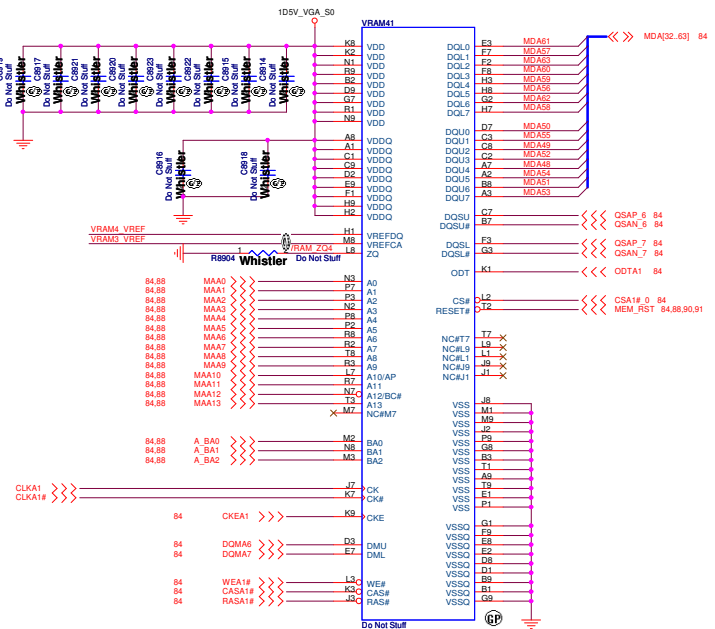
Rev: **Custom** Part: **QUEEN AMD Muxless/UMA** Rev: **X00**

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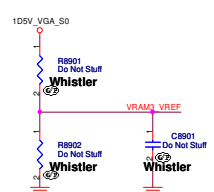




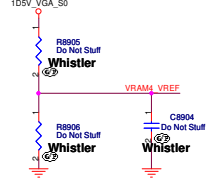
Whistler



Whistler



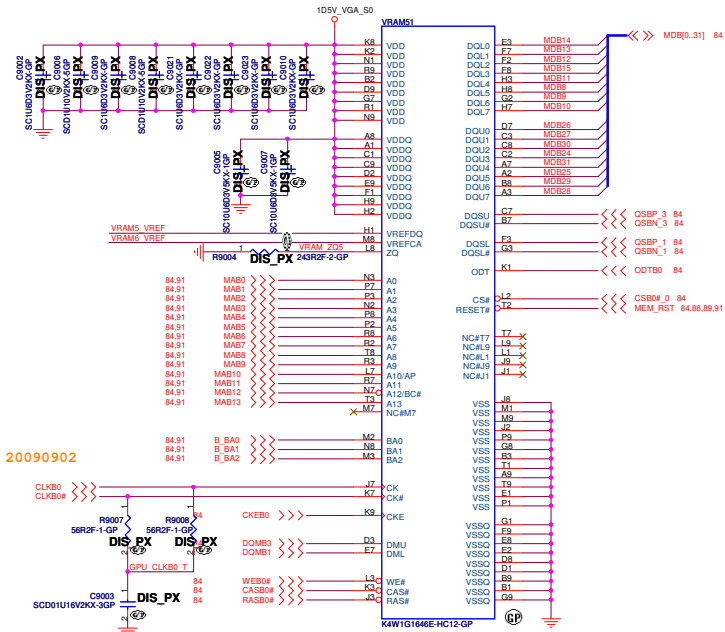
Whistler



Whistler

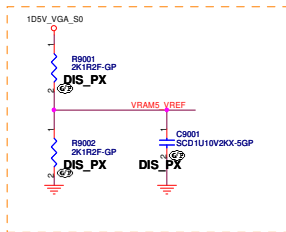
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 File: **GPU-VRAM3,4 (2/4)**
 Size A3 Document Number **QUEEN AMD Muxless/UMA** Rev **X00**
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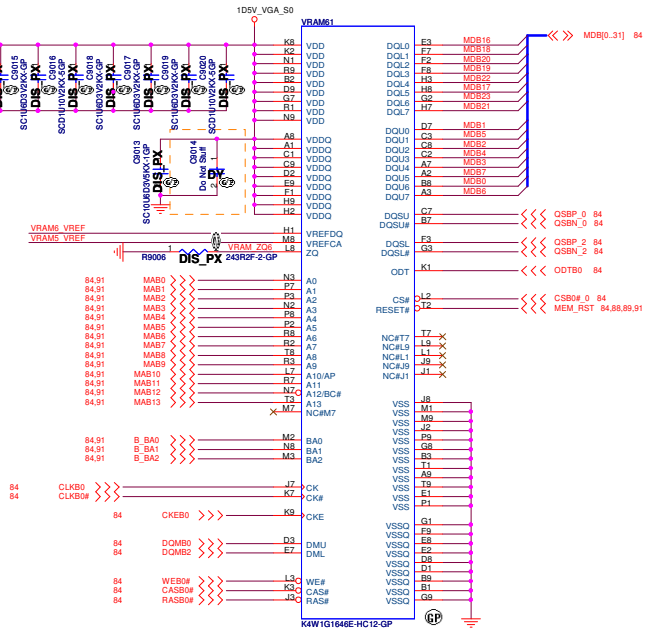


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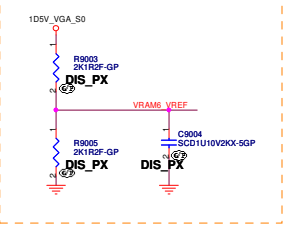
DIS_PX



Check R9001 & R9002 Change to 4.99K or no difference?



DIS_PX



Check R9001 & R9002 Change to 4.99K or no difference?

DDI5 AMD DE SAMSUNG T1

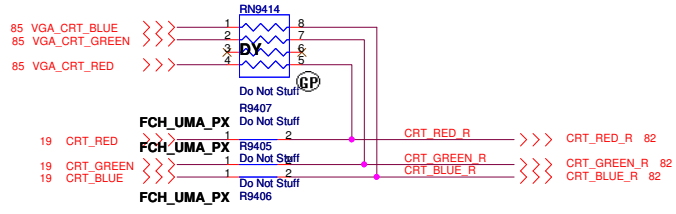
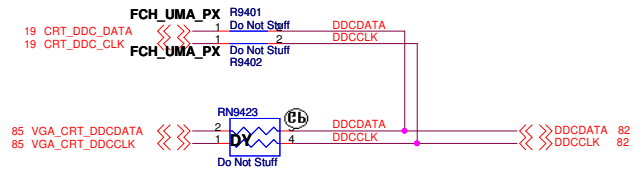
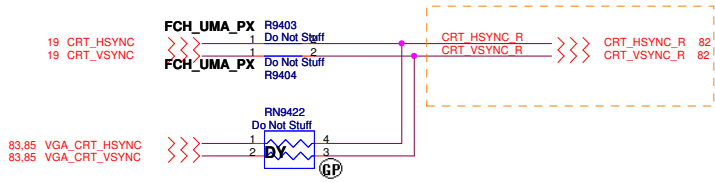
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SSID = VIDEO



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LVDS VGA Switch			
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TOUCH PANEL connector



0707: Move To Page 49, Touch Panel Combine With LVDS

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Touch Panel

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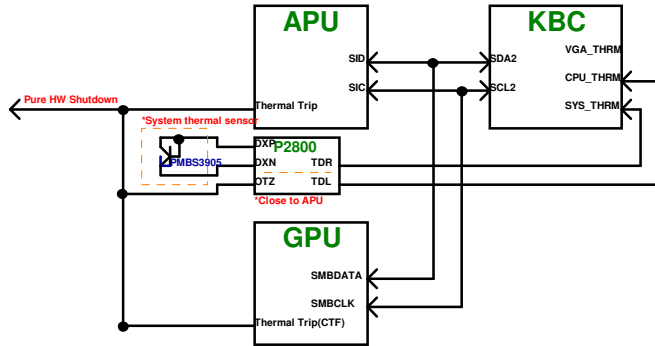
Rev

QUEEN AMD Muxless/UMAX00

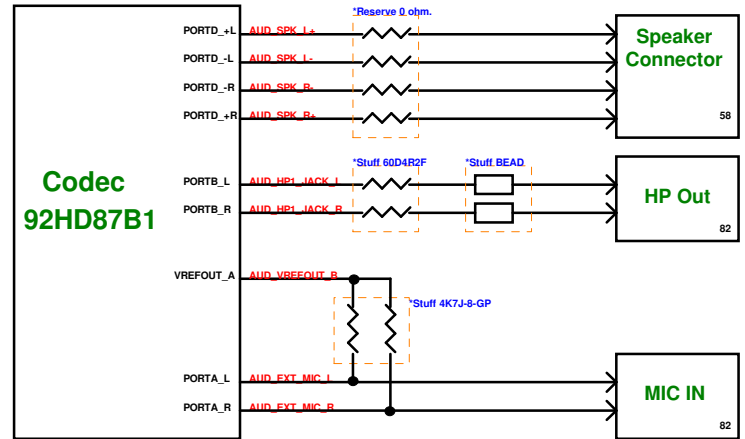
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Thermal Block Diagram



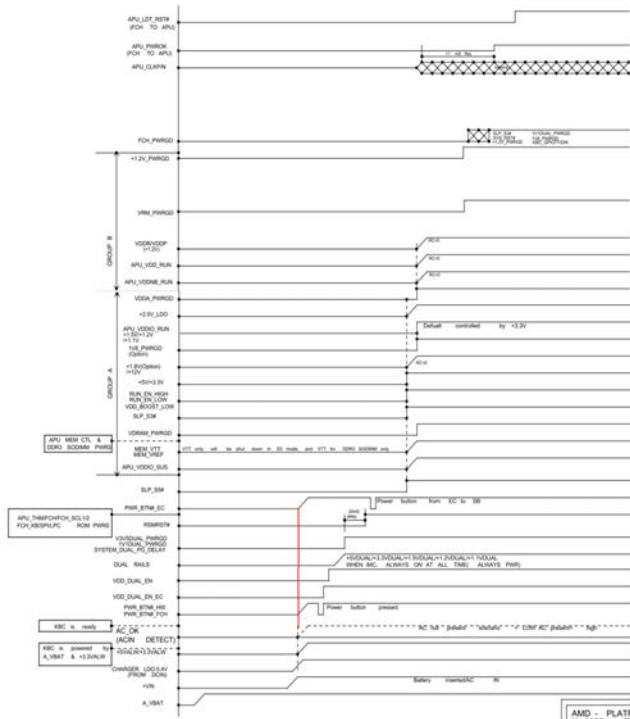
Audio Block Diagram



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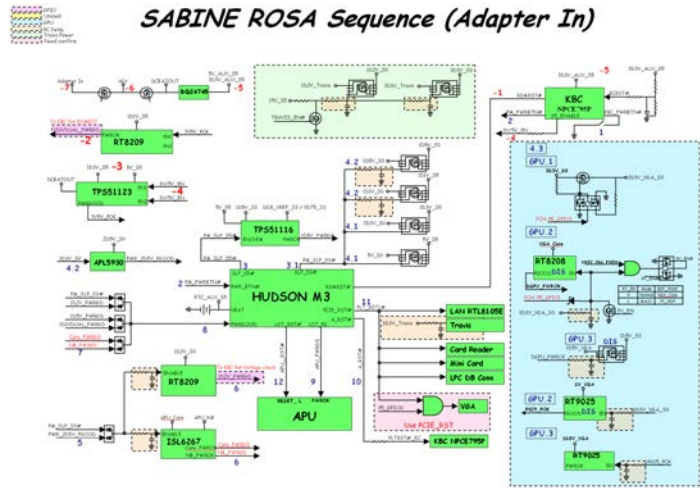
		Wistron Corporation <small>21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.</small>	
		THERMAL/AUDIO BLOCK DIAGRAM	
Title	Document Number		Rev
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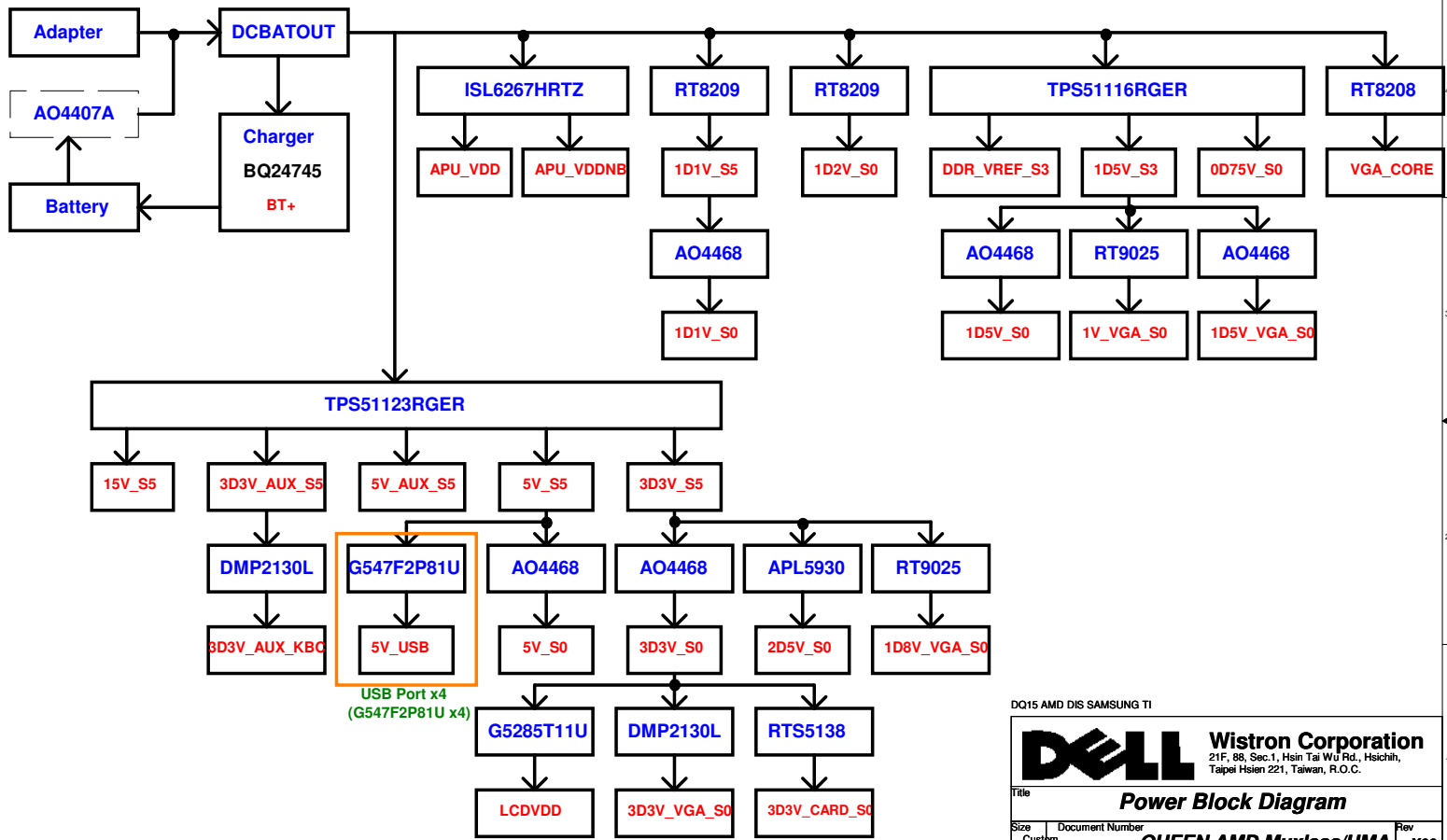
POWER SEQUENCE



AMD - PLATI


SABINE ROSA Sequence (Adapter In)



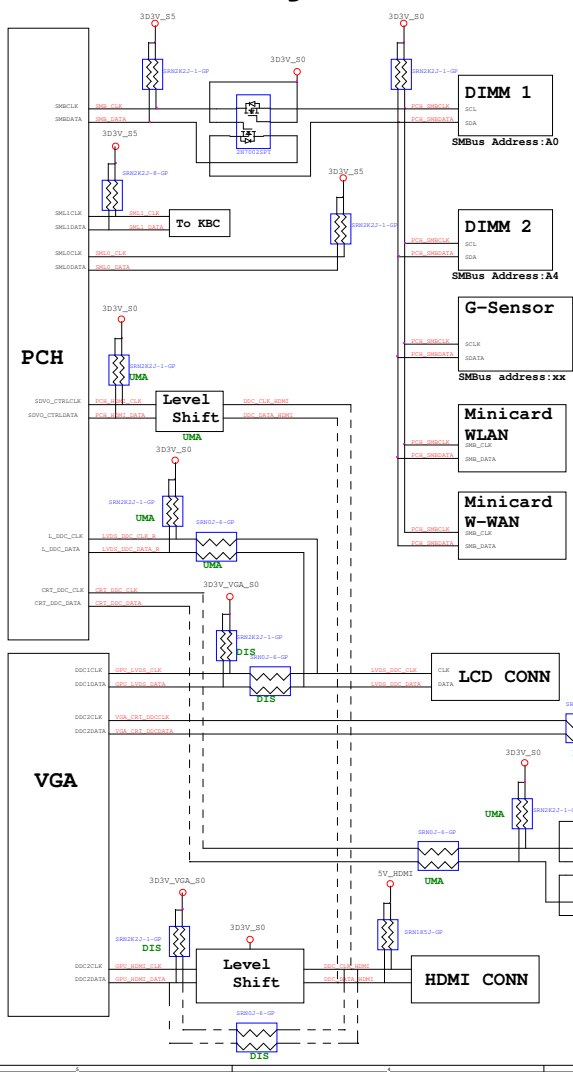


USB Port x4
(G547F2P81U x4)

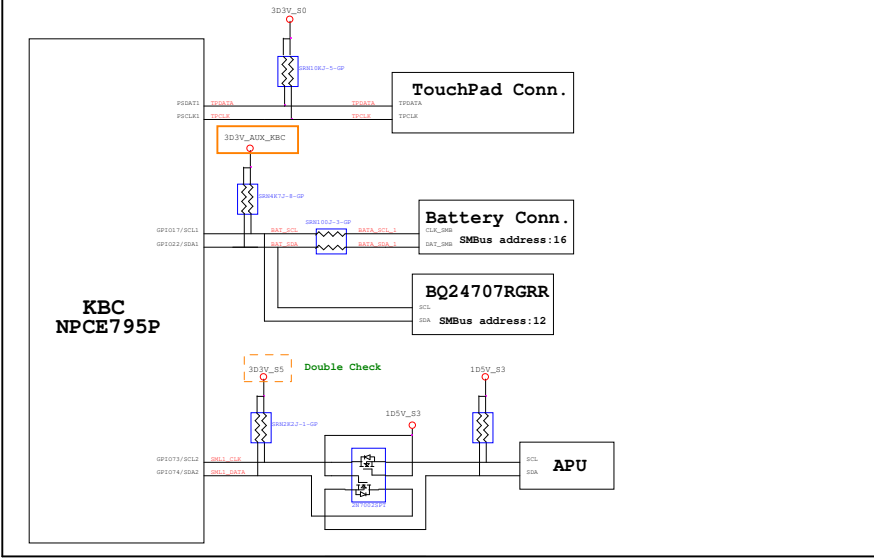
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		Power Block Diagram	
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PCH SMBus Block Diagram



KBC SMBus Block Diagram



Change notes -

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Title

Change notes

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A3

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VERSION	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	01/08	3	18,19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	According ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 OR.	Add OR for level shift off.	EE
	01/13	1	21,37	Add C3725, C2105.	Reserve for signal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory request.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
		1	13	Add TP1309.	As factory request to add.	Factory
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE
		3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
	02/25	5	79	Remove EC7928.	Layout space limitation.	EE
		1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE	

0303-1

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