

Enrico/Caruso 15" UMA Schematics Document

rPGA988A Mobile Arrandale

Intel IbeX Peak-M

2011-04-22

REV : A00

DY : Nopop Component
HDMI : Pop for HDMI function
No_HDMI : Pop for NO HDMI function
10/100 : Pop for 10/100 LAN
GIGA : Pop for GIGA LAN
Surge : Pop for surge option
G709 : Pop G709 thermal solution
INS : Pop for Inspiron series ID
VOS : Pop for Vostro series ID
S3 : Pop for S3 power reduction
Normal : Pop for NO S3 power reduction

DV15 CP UMA second



Title		
Cover Page		
Size	Document Number	Rev
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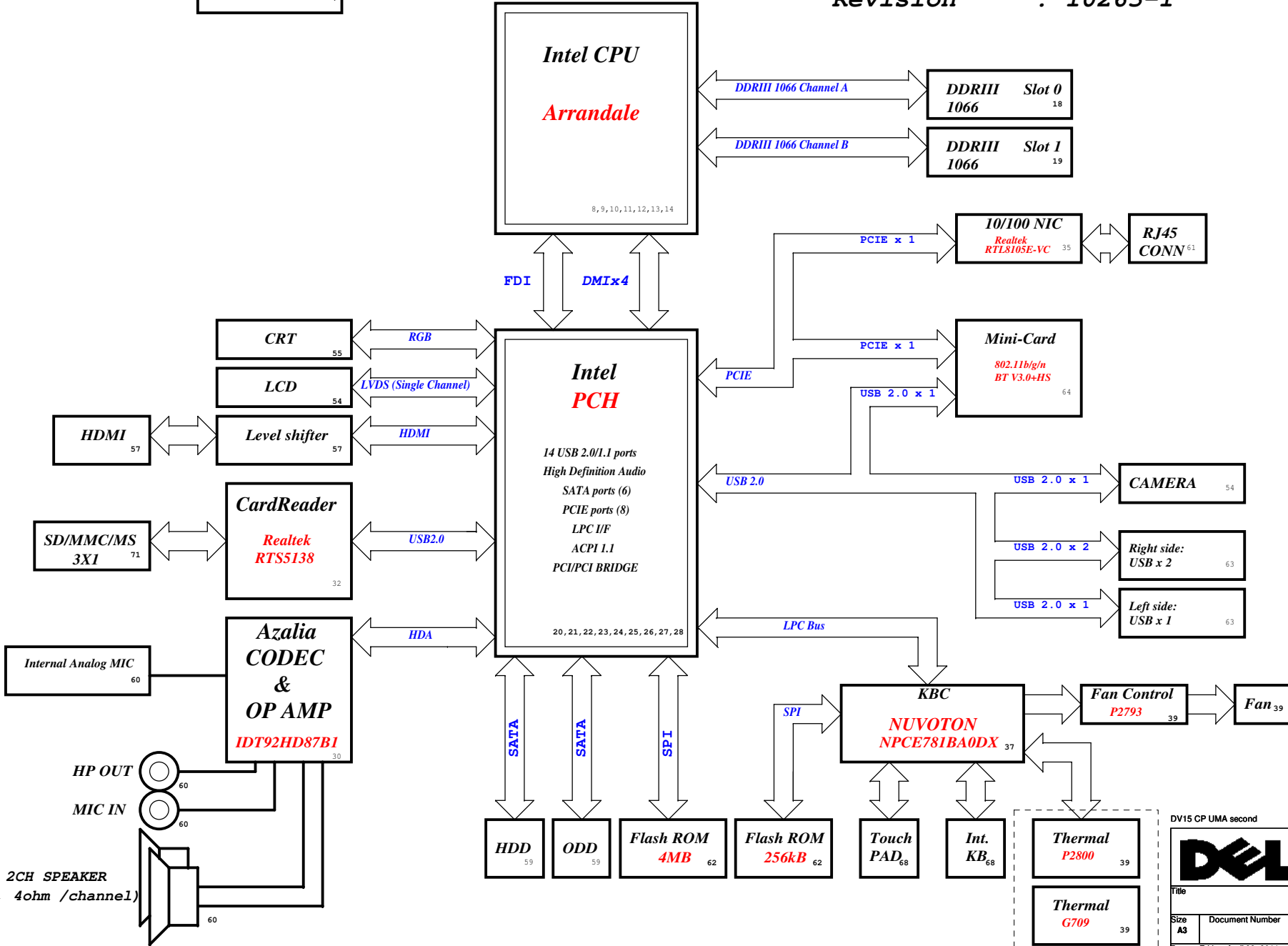
DV15 Calpella UMA Block Diagram

Project code : 91.4IP01.001
 PCB P/N : 48.4IP01.011
 Revision : 10263-1

Clock Generator
SLG8SP595
 7

Intel CPU
Arrandale
 8, 9, 10, 11, 12, 13, 14

Intel PCH
 14 USB 2.0/1.1 ports
 High Definition Audio
 SATA ports (6)
 PCIE ports (8)
 LPC I/F
 ACPI 1.1
 PCI/PCI BRIDGE
 20, 21, 22, 23, 24, 25, 26, 27, 28



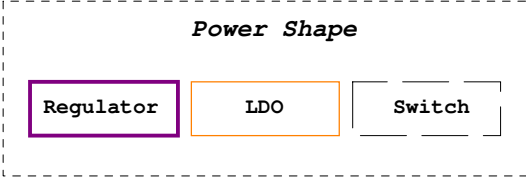
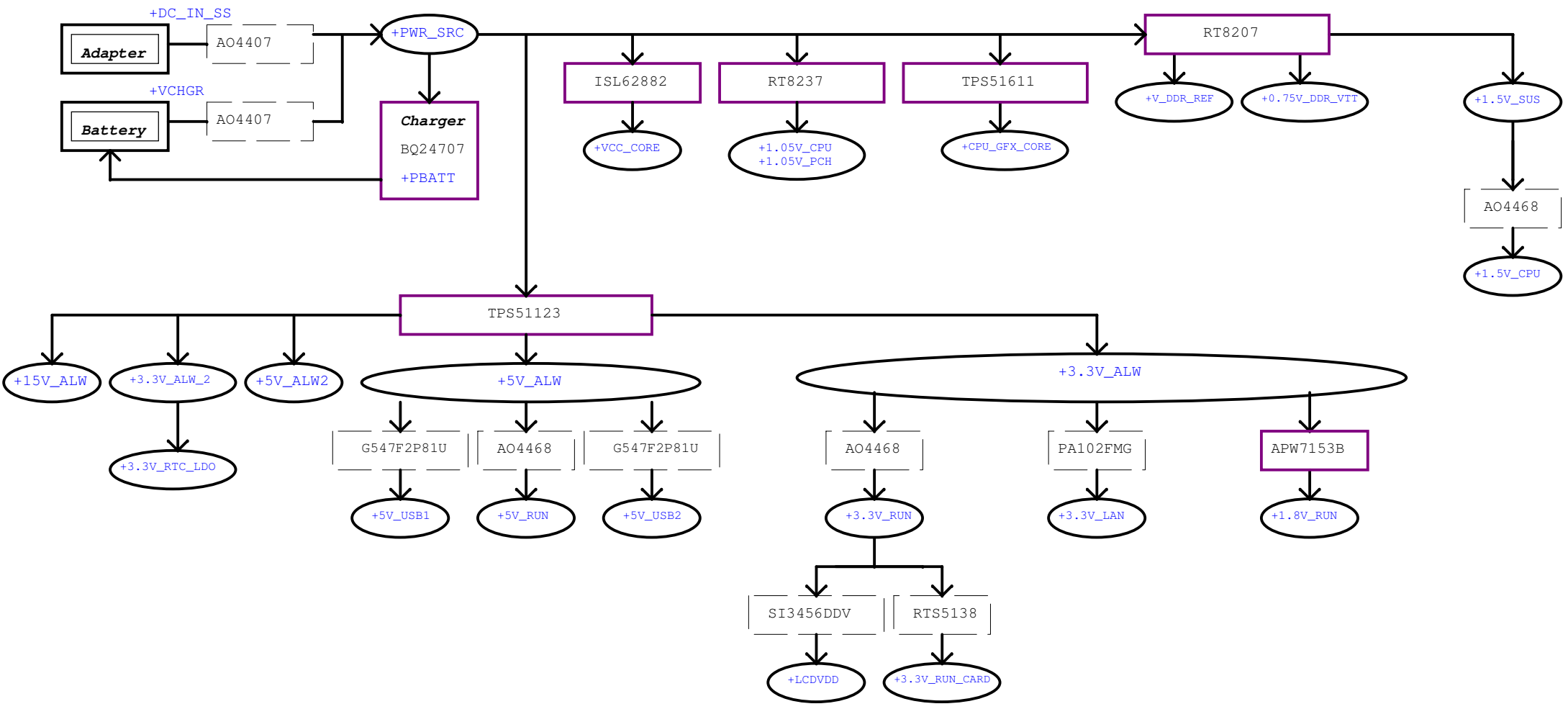
MAXIM CHARGER BQ24707 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC TPS51123 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +3.3V_ALW +5V_ALW +15V_ALW
CPU DC/DC ISL62882 47, 48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC RT8237A 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_CPU +1.05V_PCH
SYSTEM DC/DC RT8207 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +V_DDR_REF +0.75V_DDR_VTT
SYSTEM DC/DC APW7153B 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE
SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_CPU +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Bottom	

DV15 CP UMA second

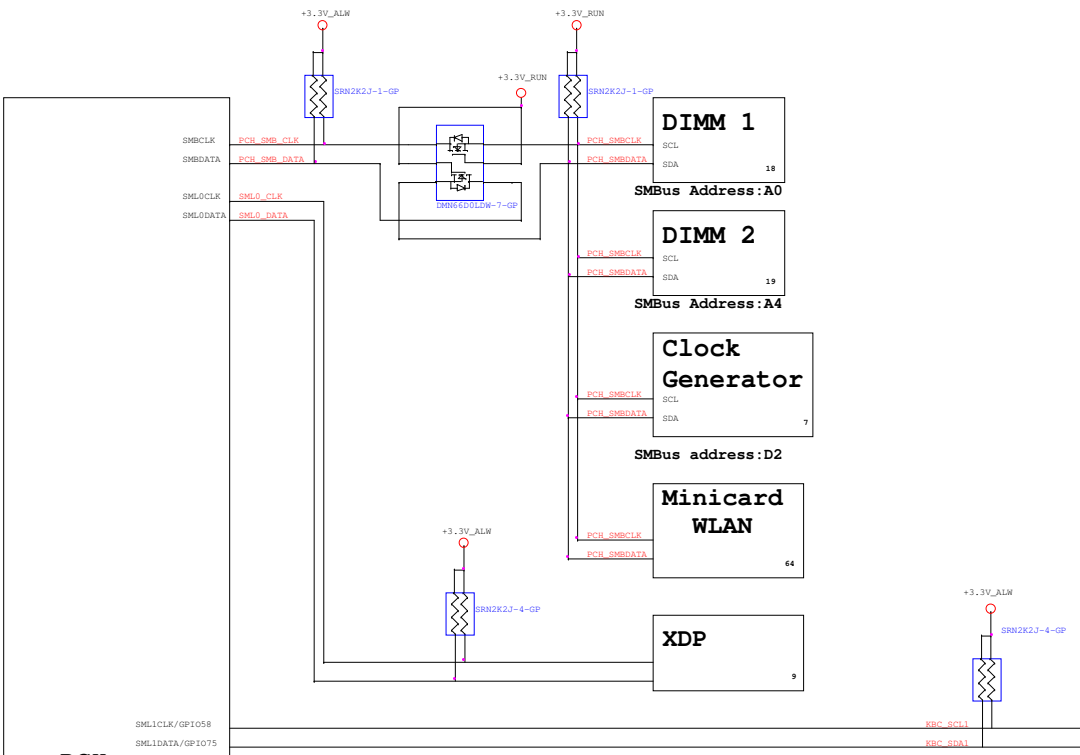
Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

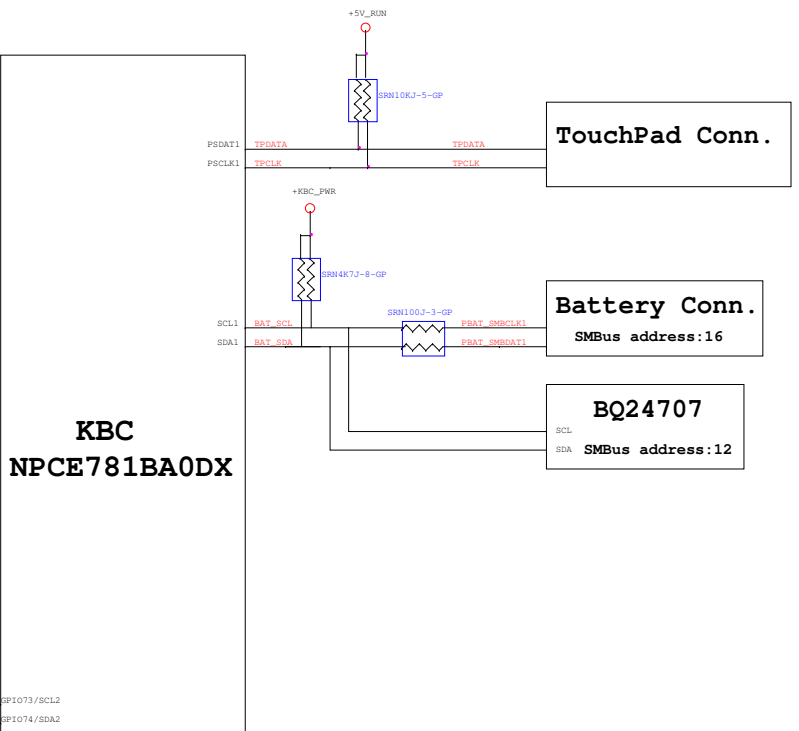
Size A3	Document Number Enrico/Caruso 15 CP	Rev A00
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PCH SMBus Block Diagram

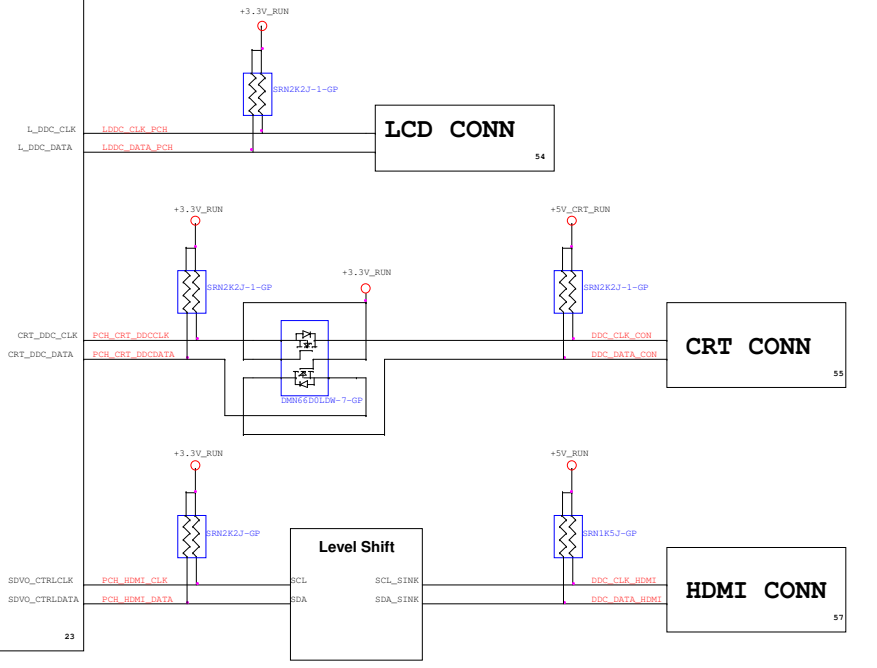


KBC SMBus Block Diagram

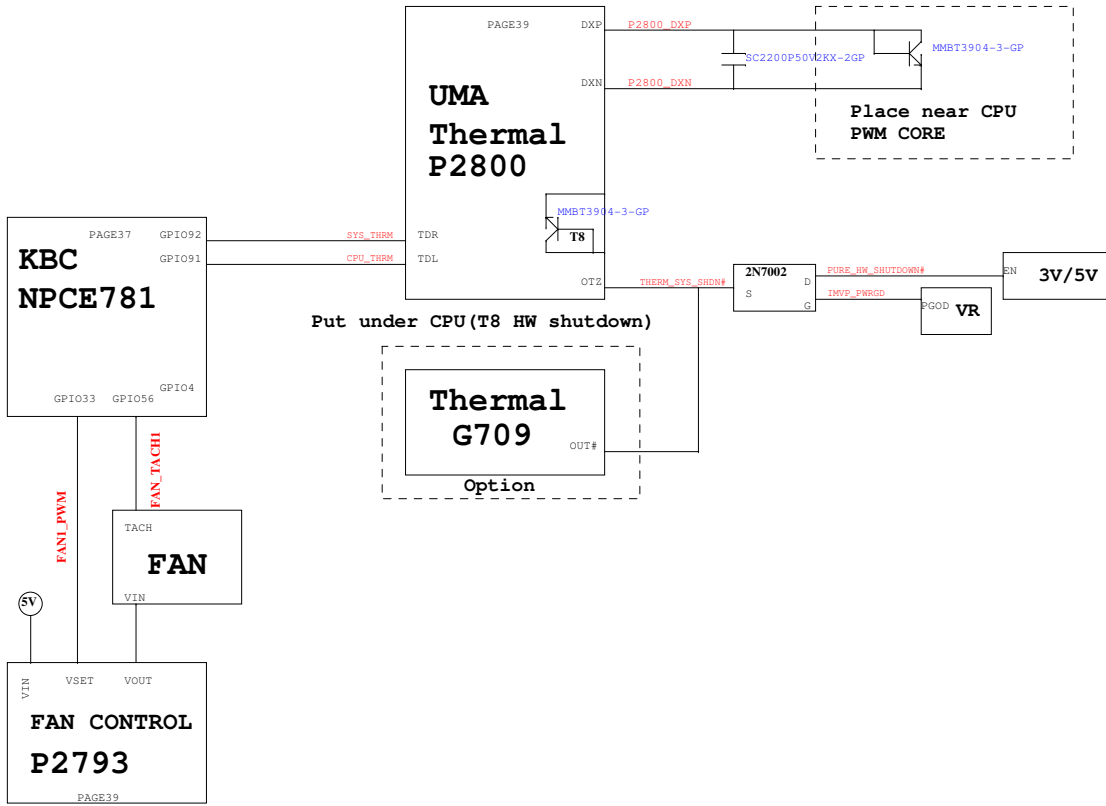


PCH

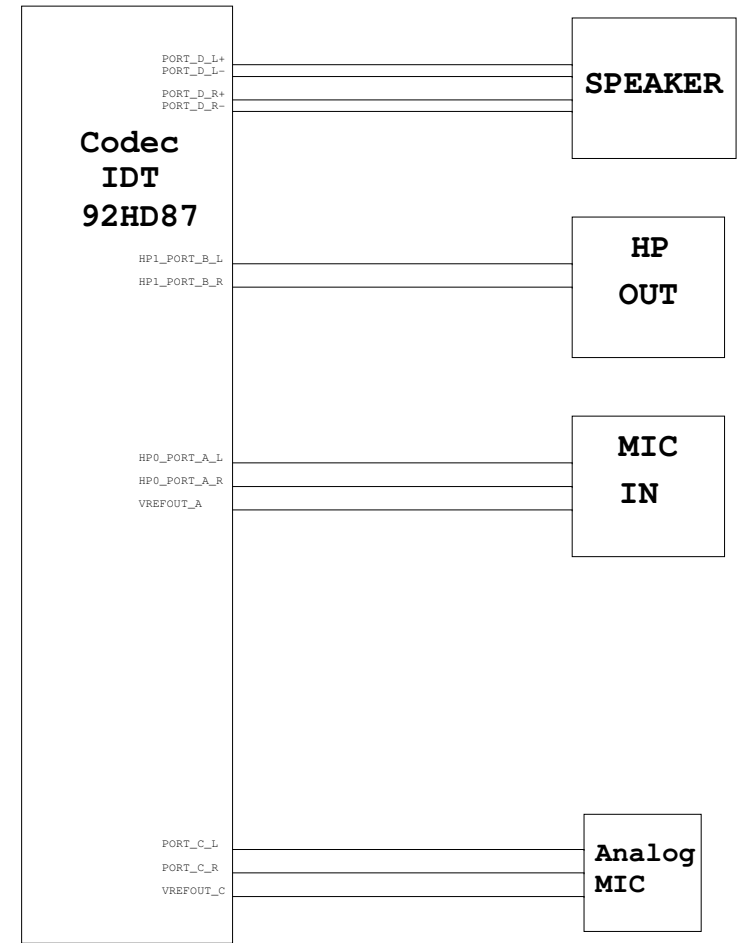
KBC
NPCE781BA0DX



Thermal Block Diagram



Audio Block Diagram



DV15 CP UMA second

DELL		Wistron Corporation	
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Title			
Thermal/Audio Block Diagram			
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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	X
1	USB1
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X

Processor Strapping

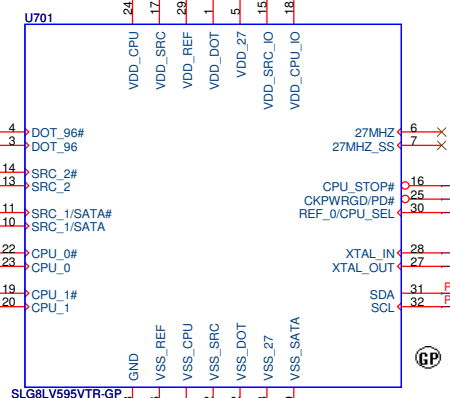
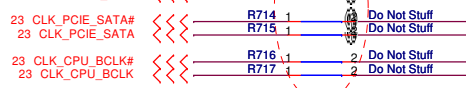
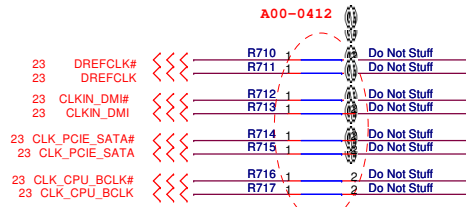
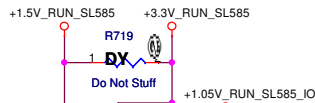
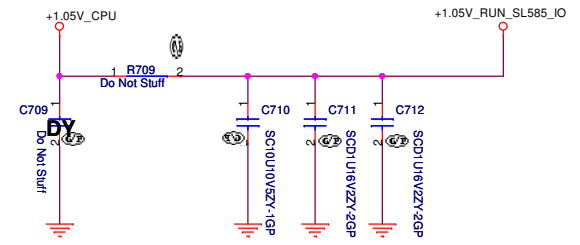
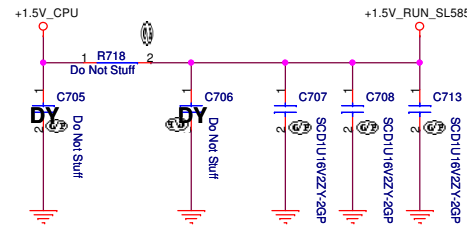
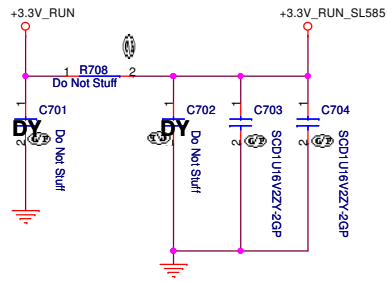
Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

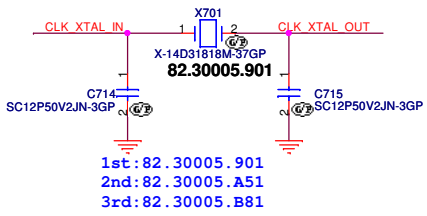
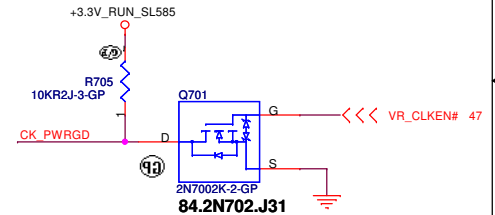
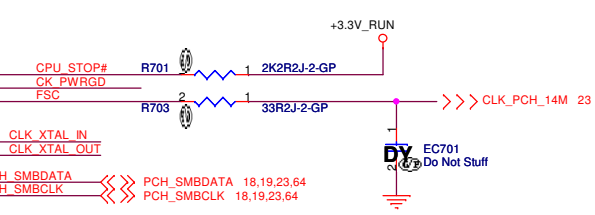
DV15 CP UMA second

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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SSID = CLOCK

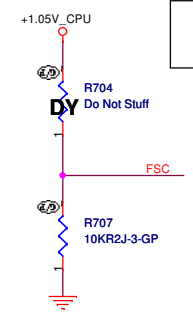


1st Silego : 71.08595.003
2nd IDT : 71.93197.B03



1st: 82.30005.901
2nd: 82.30005.A51
3rd: 82.30005.B81

FSC	0	1
SPEED	133MHz (Default)	100MHz



DV15 CP UMA second

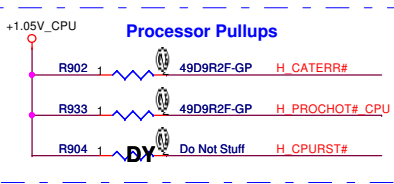
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator SLG8LV595**

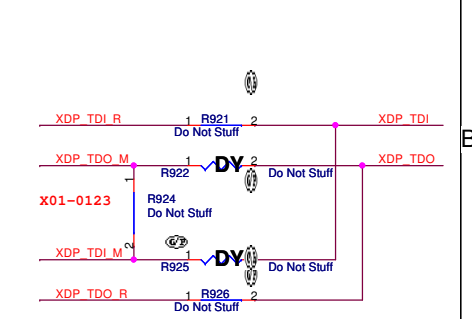
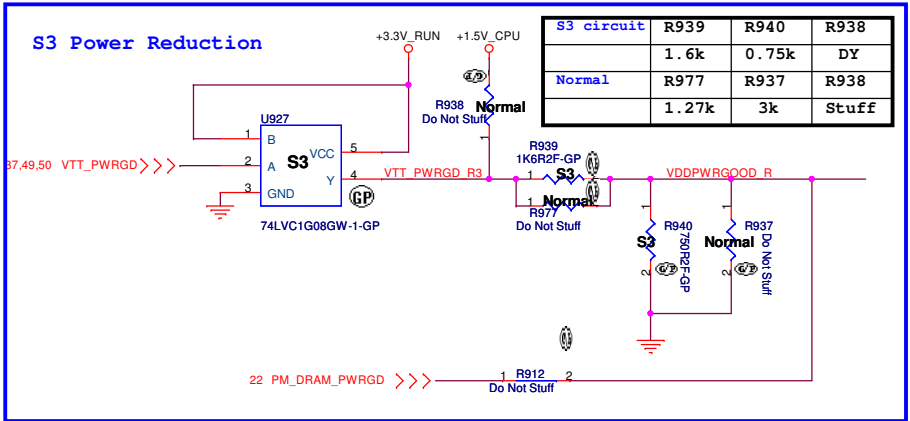
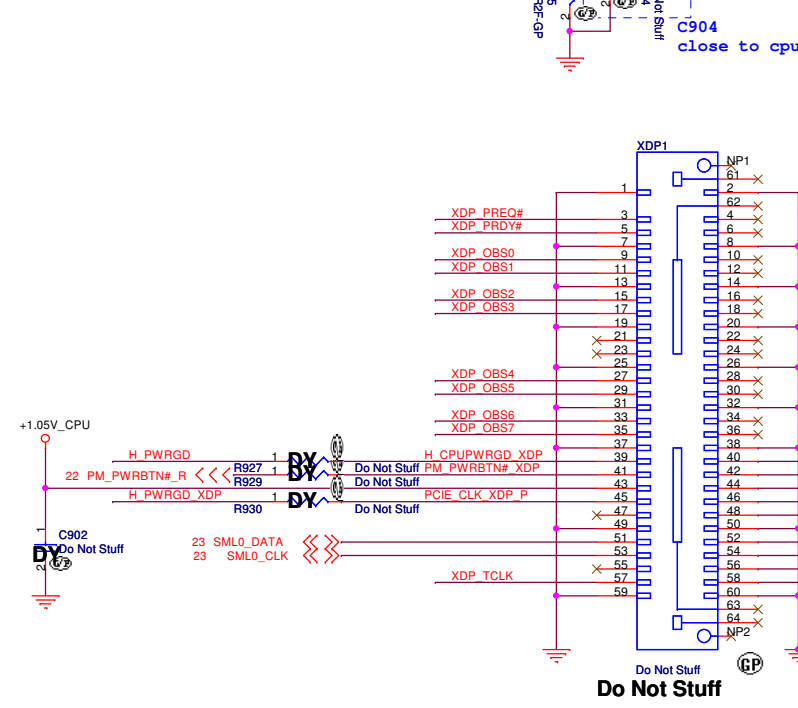
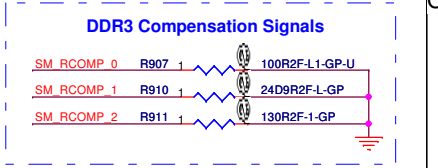
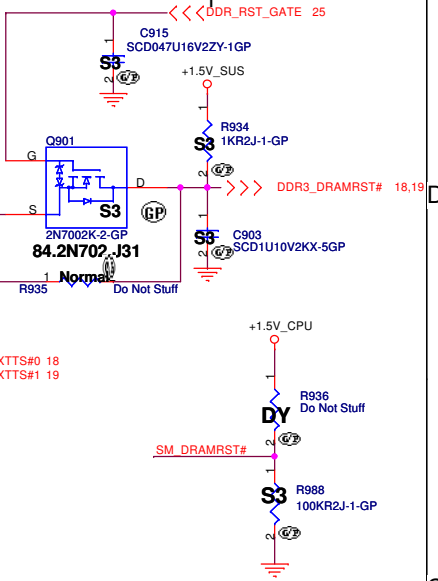
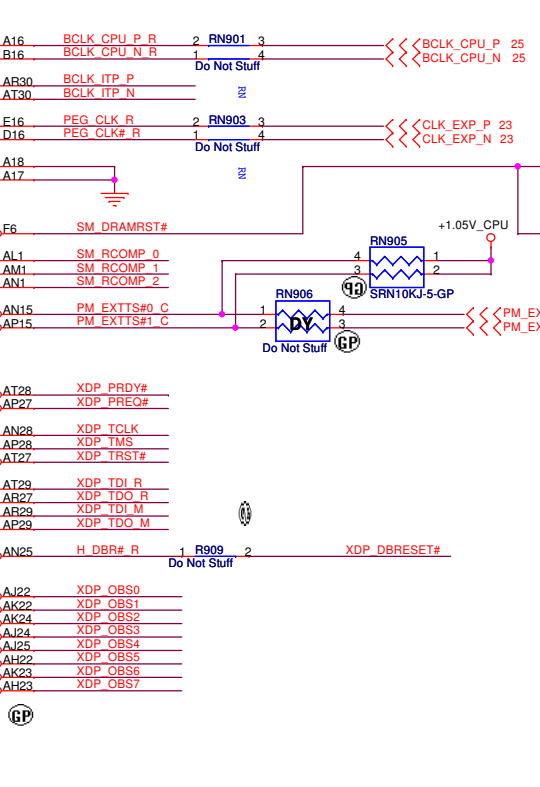
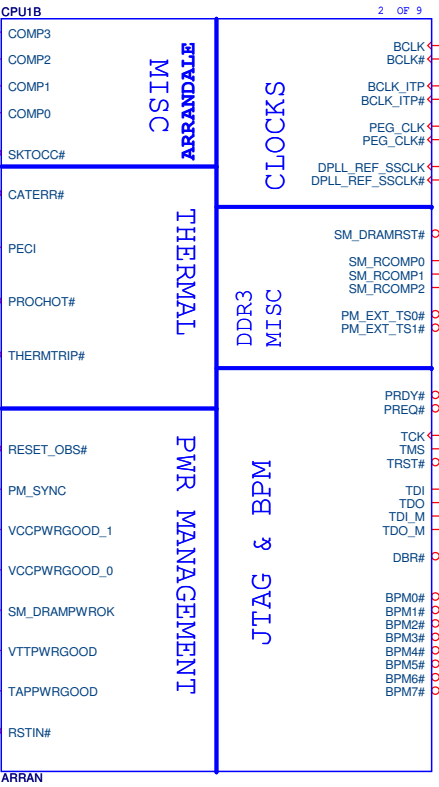
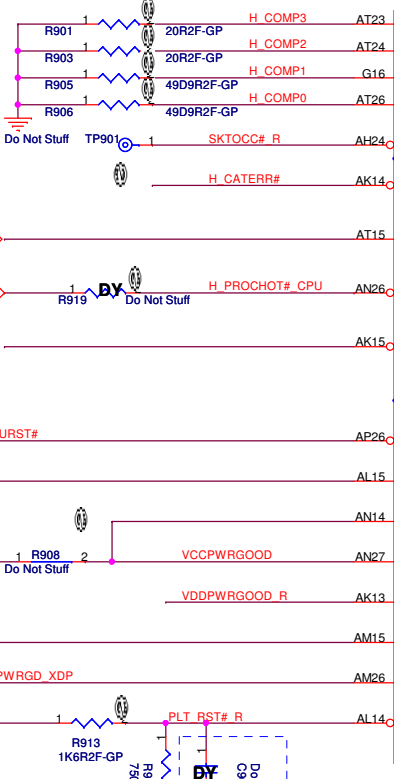
Size: Document Number: **Enrico/Caruso 15 CP** Rev: **A00**

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SSID = CPU

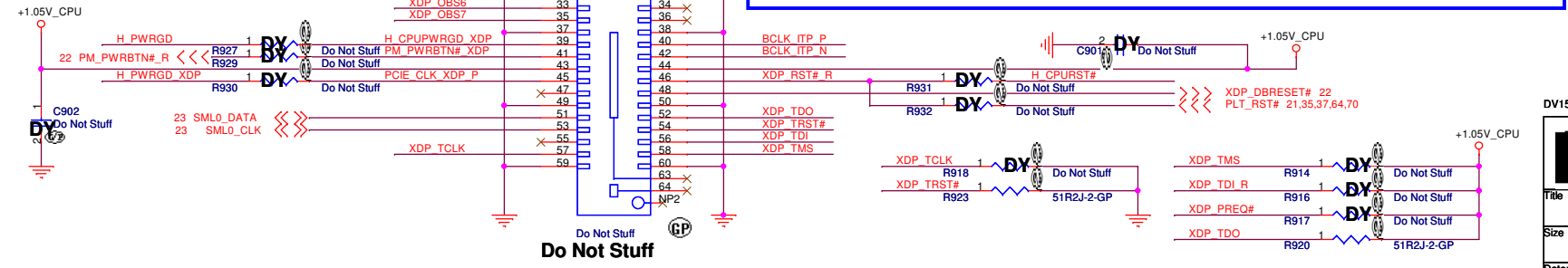


Processor Compensation Signals



JTAG MAPPING

Scan Chain (Default)	Stuff --> R921, R924, R926
CPU Only	Stuff --> R921, R922
GMCH Only	Stuff --> R924, R926, R925
	No Stuff --> R921, R922, R924, R925



DV15 CPU UMA second

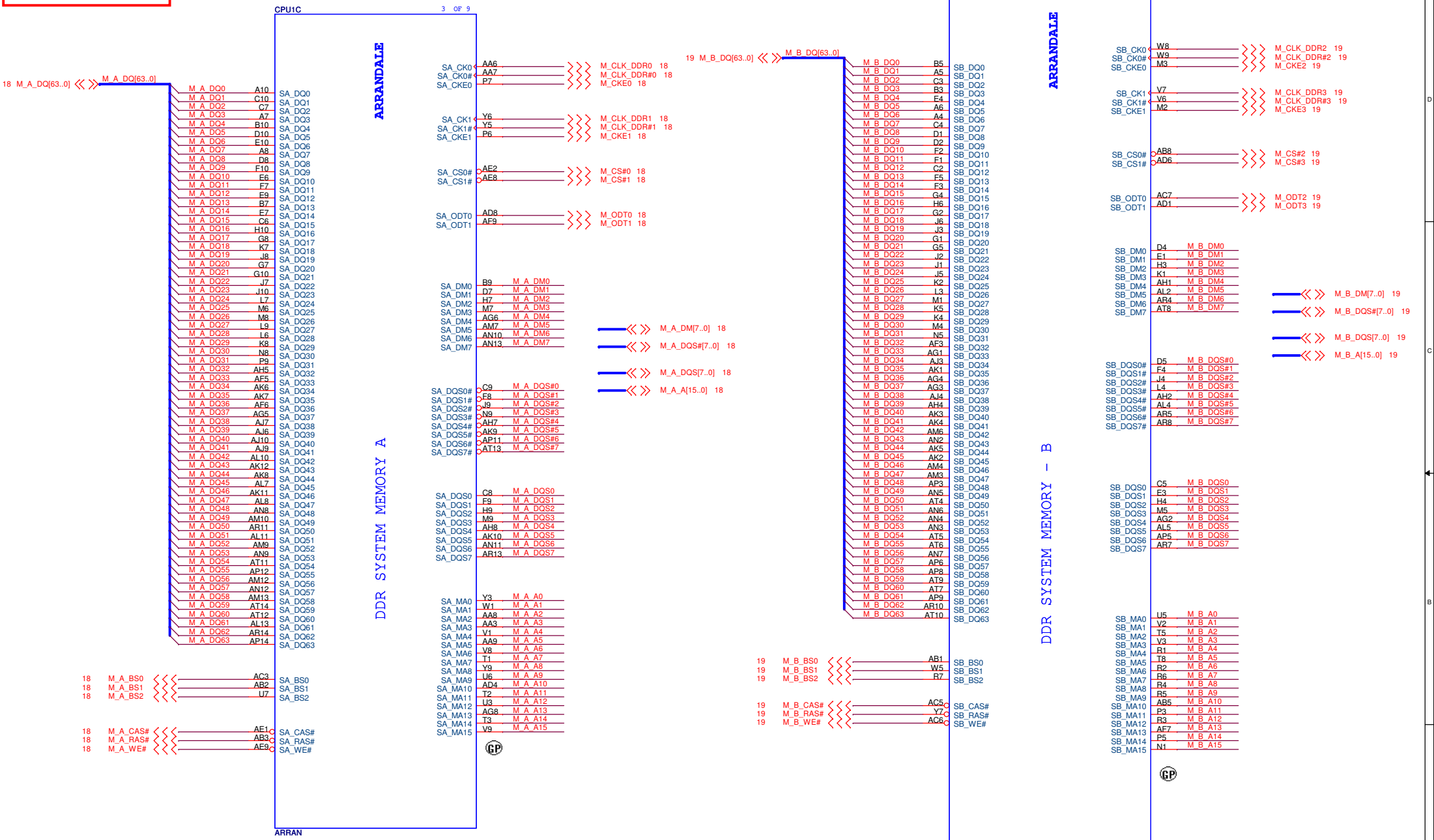
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CPU (THERMAL/CLOCK/PM)

Size: Document Number: **Enrico/Caruso 15 CP** Rev: **A00**

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SSID = CPU



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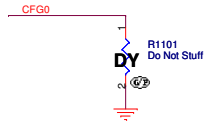
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR)**

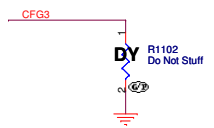
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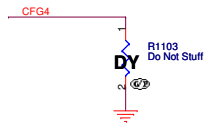
SSID = CPU



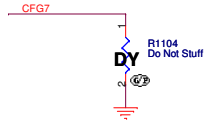
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



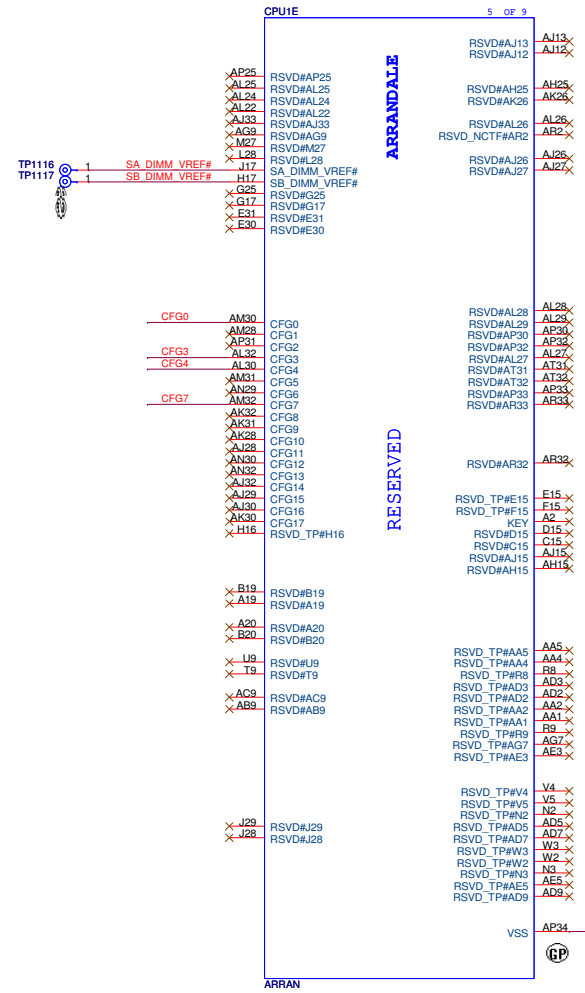
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

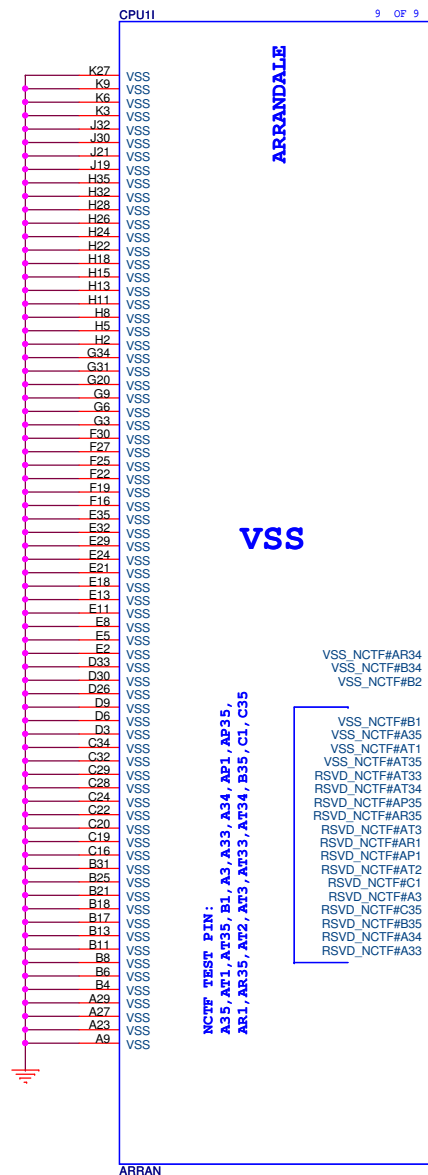
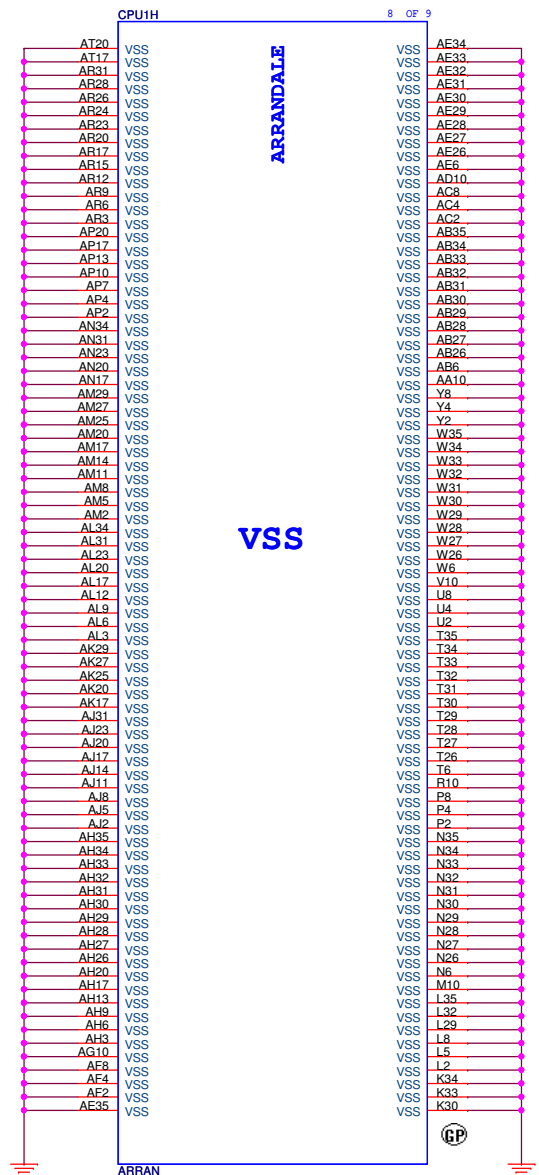


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

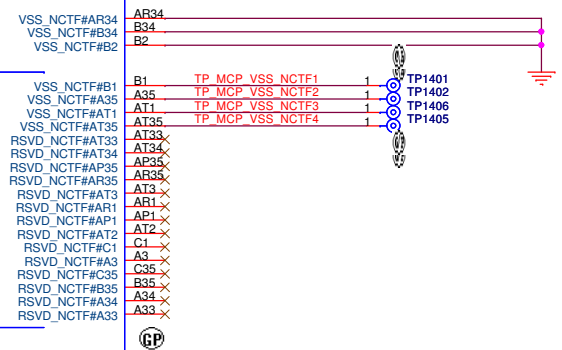


VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

SSID = CPU



NCTF TEST PIN :
 A35, AT1, AT35, B1, A3, A33, A34, AP1, AP35,
 AR1, AR35, AT2, AT3, AT33, AT34, B35, C1, C35



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Title		
CPU (VSS)		
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Reserved		
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DV15 CP UMA second



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Reserved		
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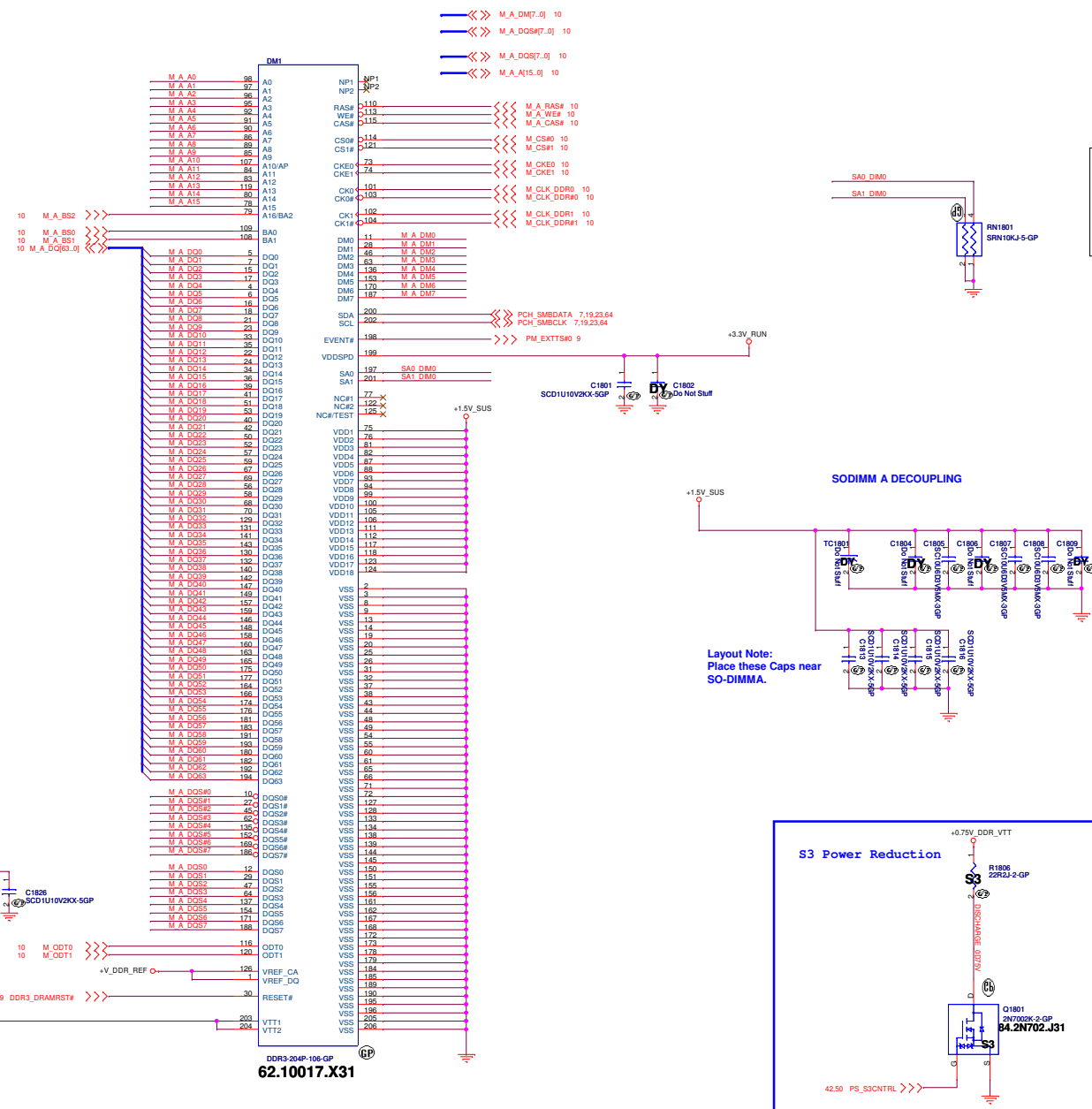
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DV15 CP UMA second



Title		
Reserved		
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SSID = MEMORY

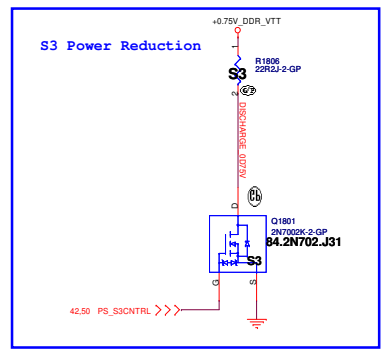


Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30

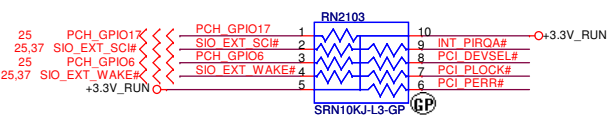
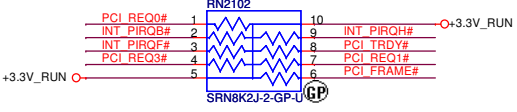
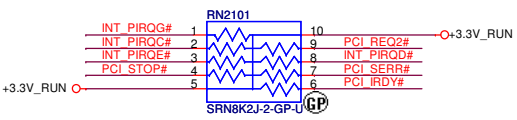
 If SA0_DIM0 = 0, SA1_DIM0 = 1
 SO-DIMMA SPD Address is 0xA4
 SO-DIMMA TS Address is 0x34

Layout Note:
 Place these Caps near
 SO-DIMMA.

Place these caps
 close to VTT1 and
 VTT2.



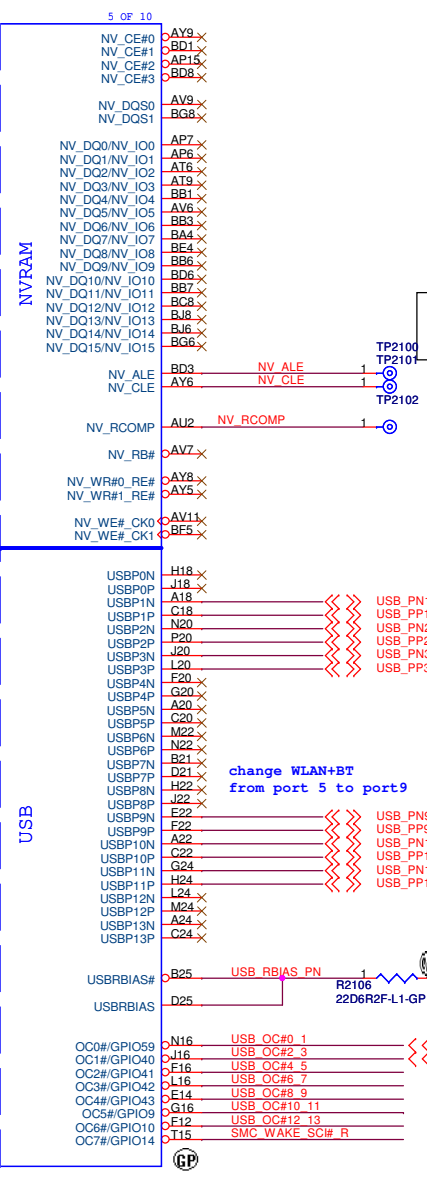
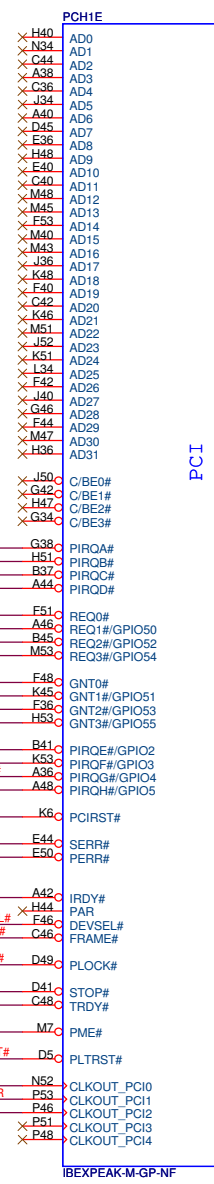
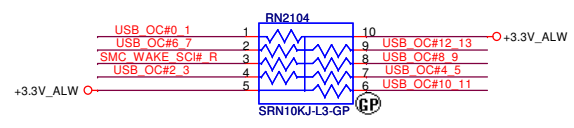
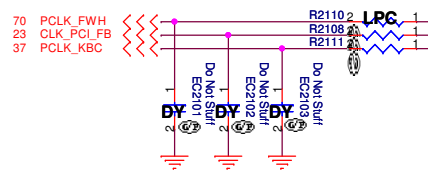
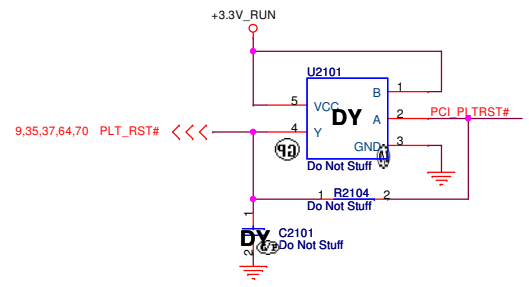
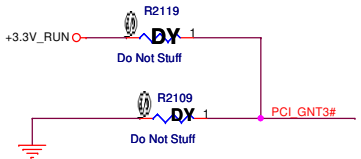
SSID = PCH



PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
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Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	X
1	USB1 (Debug Port)
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X

DV15 CP UMA second



SSID = PCH

3 OF 10

- 8 DML_CTX_PRXN0 >>> BC24
- 8 DML_CTX_PRXN1 >>> BJ22
- 8 DML_CTX_PRXN2 >>> AW20
- 8 DML_CTX_PRXN3 >>> BJ20
- 8 DML_CTX_PRPX0 >>> BD24
- 8 DML_CTX_PRPX1 >>> BG22
- 8 DML_CTX_PRPX2 >>> BA20
- 8 DML_CTX_PRPX3 >>> BG20
- 8 DML_PTX_CRXN0 >>> BE22
- 8 DML_PTX_CRXN1 >>> BF21
- 8 DML_PTX_CRXN2 >>> BD20
- 8 DML_PTX_CRXN3 >>> BE18
- 8 DML_PTX_CRXP0 >>> BD22
- 8 DML_PTX_CRXP1 >>> BH21
- 8 DML_PTX_CRXP2 >>> BC20
- 8 DML_PTX_CRXP3 >>> BD18

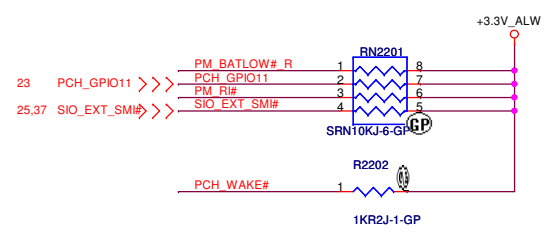
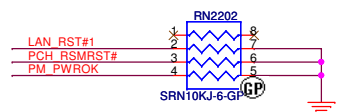
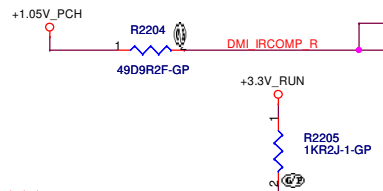
PCH1C
 DMIORXN
 DMI1RXN
 DMI2RXN
 DMI3RXN
 DMIORXP
 DMI1RXP
 DMI2RXP
 DMI3RXP
 DMIOTXN
 DMI1TXN
 DMI2TXN
 DMI3TXN
 DMIOTXP
 DMI1TXP
 DMI2TXP
 DMI3TXP
 DMI_ZCOMP
 DMI_IRCOMP
 SYS_RESET#
 SYS_PWROK
 MEPWROK
 LAN_RST#
 DRAMPWROK
 RSMRST#
 SUS_PWR_DN_ACK/GPIO30
 PWRBTN#
 ACPRESENT/GPIO31
 BATLOW#/GPIO72
 RI#
 IBEXPEAK-M-GP-NF

System Power Management

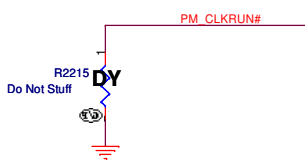
FDI_RXN0
 FDI_RXN1
 FDI_RXN2
 FDI_RXN3
 FDI_RXN4
 FDI_RXN5
 FDI_RXN6
 FDI_RXN7
 FDI_RXP0
 FDI_RXP1
 FDI_RXP2
 FDI_RXP3
 FDI_RXP4
 FDI_RXP5
 FDI_RXP6
 FDI_RXP7
 FDI_INT
 FDI_FSYNC0
 FDI_FSYNC1
 FDI_LSYNC0
 FDI_LSYNC1
 WAKE#
 CLKRUN#/GPIO2
 SUS_STAT#/GPIO6
 SUSCLK#/GPIO62
 SLP_S5#/GPIO63
 SLP_S4#
 SLP_S3#
 SLP_M#
 TP23
 PMSYNCH
 SLP_LAN#/GPIO29

- BA18 FDI_TXN0 <<< FDI_TXN0 8
- BH17 FDI_TXN1 <<< FDI_TXN1 8
- BD16 FDI_TXN2 <<< FDI_TXN2 8
- BJ16 FDI_TXN3 <<< FDI_TXN3 8
- BA16 FDI_TXN4 <<< FDI_TXN4 8
- BE14 FDI_TXN5 <<< FDI_TXN5 8
- BA14 FDI_TXN6 <<< FDI_TXN6 8
- BC12 FDI_TXN7 <<< FDI_TXN7 8
- BB18 FDI_TXP0 <<< FDI_TXP0 8
- BE17 FDI_TXP1 <<< FDI_TXP1 8
- BC16 FDI_TXP2 <<< FDI_TXP2 8
- BG16 FDI_TXP3 <<< FDI_TXP3 8
- AW16 FDI_TXP4 <<< FDI_TXP4 8
- BD14 FDI_TXP5 <<< FDI_TXP5 8
- BB14 FDI_TXP6 <<< FDI_TXP6 8
- BD12 FDI_TXP7 <<< FDI_TXP7 8

- BJ14 >>> FDI_INT 8
- BE13 FDI_FSYNC0 >>> FDI_FSYNC0 8
- BH13 FDI_FSYNC1 >>> FDI_FSYNC1 8
- BJ12 FDI_LSYNC0 >>> FDI_LSYNC0 8
- BG14 FDI_LSYNC1 >>> FDI_LSYNC1 8
- J12 PCH_WAKE# R 1 R2203 2 <<< PCH_WAKE# 37
- Y1 PM_CLKRUN# <<< PM_CLKRUN# 25,37
- P8 PM_SUS_STAT# 1 TP2201 Do Not Stuff
- F3 PCH_SUSCLK <<< PCH_SUSCLK_KBC 37
- E4 PCH_SLP_S5# 1 TP2202 Do Not Stuff
- H7 PM_SLP_S4# R 1 R2211 Do Not Stuff >>> PM_SLP_S4# 37,50
- E12 PM_SLP_S3# R 1 R2212 Do Not Stuff >>> PM_SLP_S3# 37,42,50,51
- K8 SIO_SLP_M# R 1 TP2203 Do Not Stuff
- N2 PM_SLP_DSW# 1 TP2204 Do Not Stuff
- BJ10 H_PM_SYNC <<< H_PM_SYNC 9
- E6 PM_SLP_LAN# 1 TP2205 Do Not Stuff



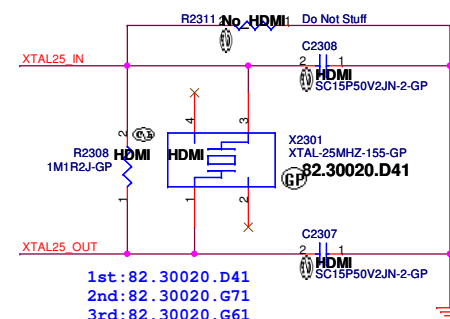
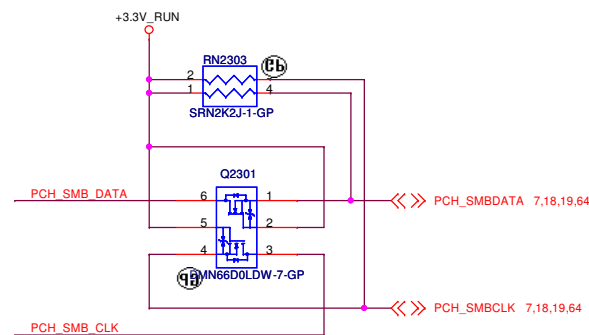
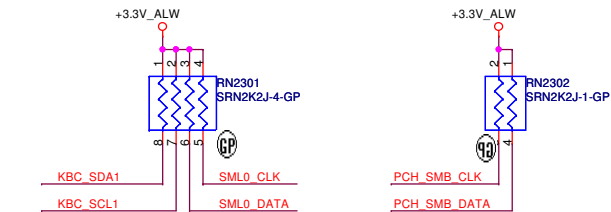
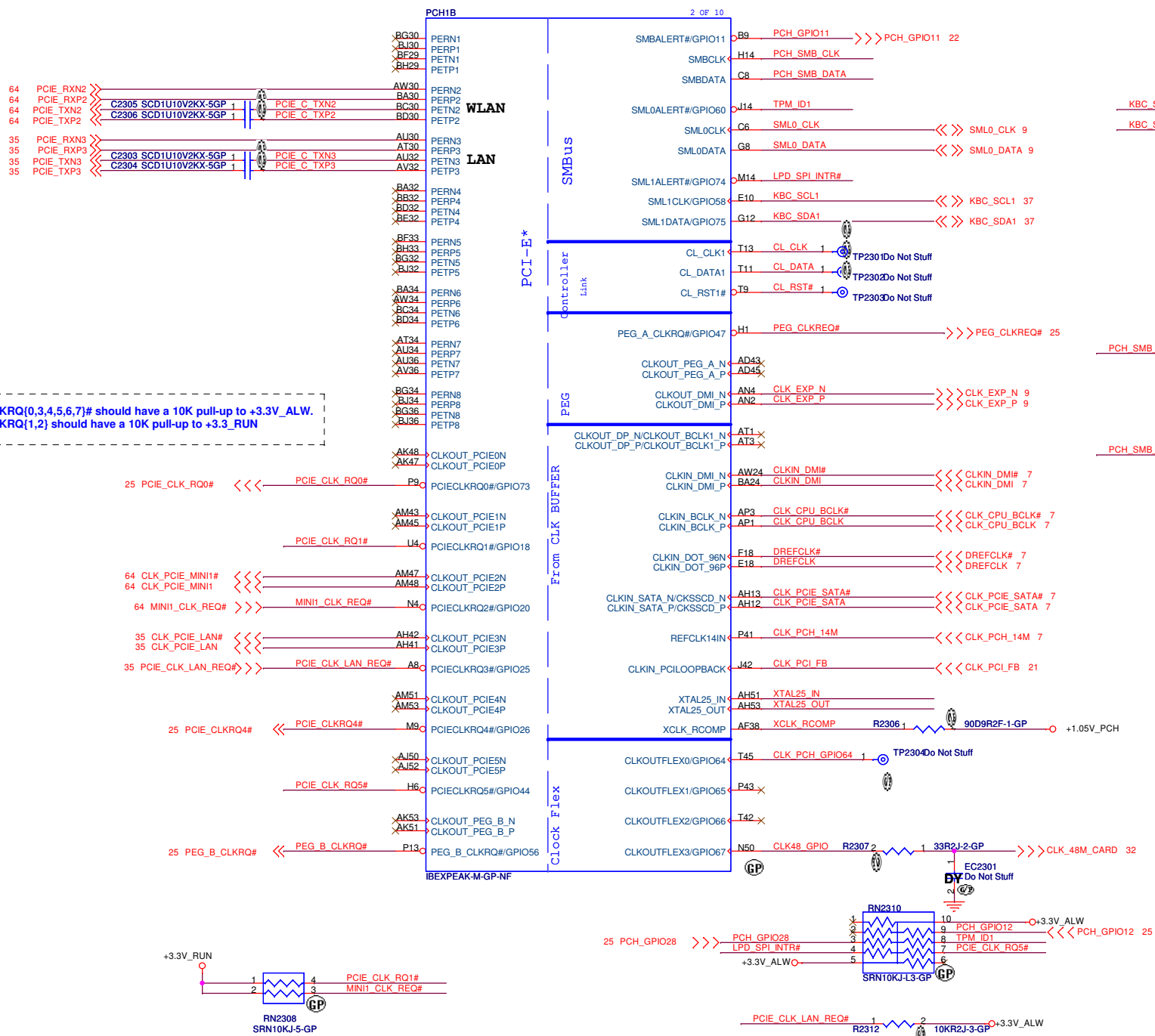
Option to "Disable" clkrun.
 Pulling it down will keep the clks running.



DV15 CP UMA second

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
		PCH (DM I/FDI/PM)		
Title	Enrico/Caruso 15 CP		Rev	A00
Size	Document Number	Date: Wednesday, April 13, 2011		Sheet 22 of 99

SSID = PCH



DV15 CP UMA second

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size: Document Number

Date: Wednesday, April 13, 2011

Sheet 23 of 99

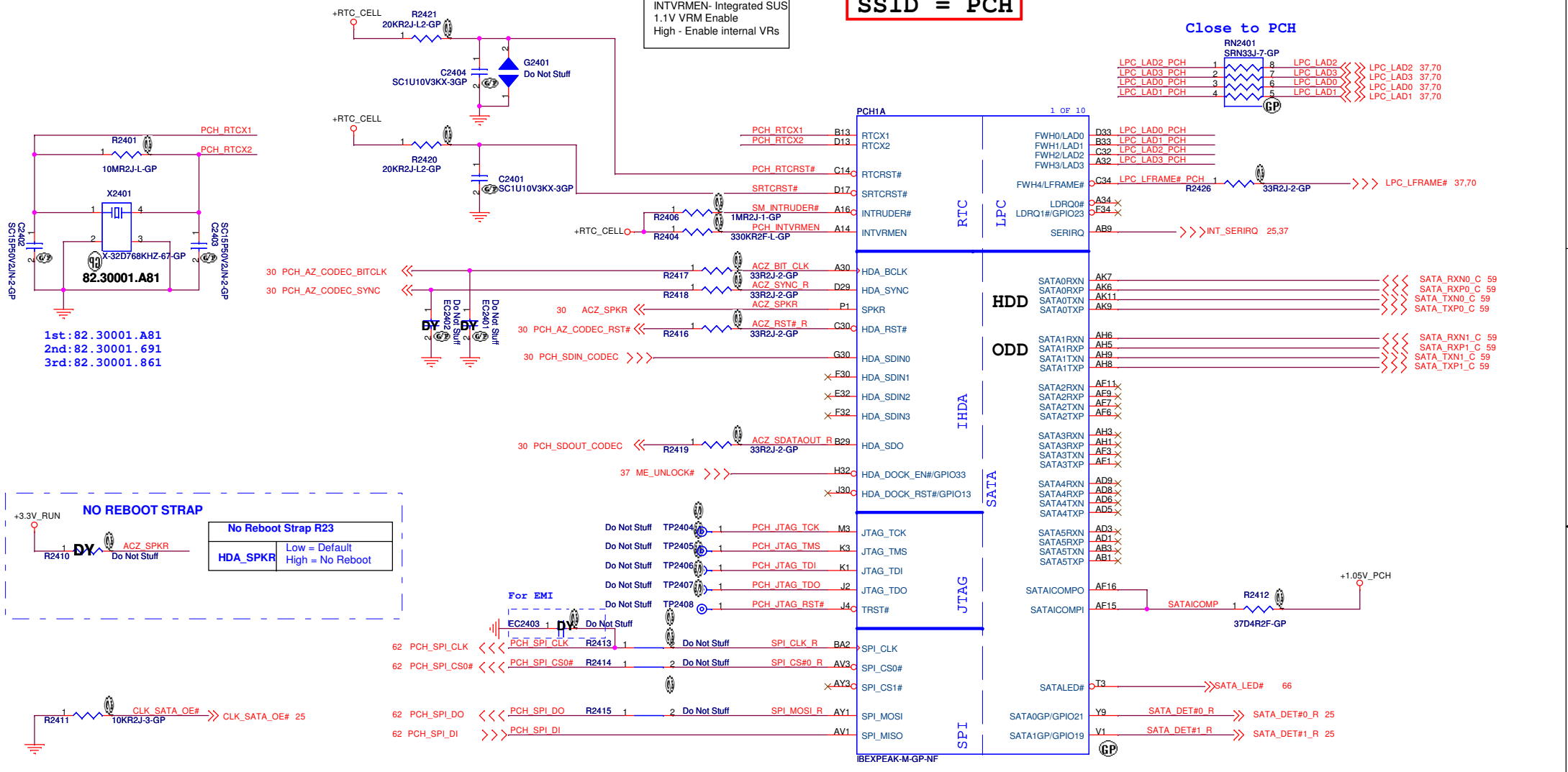
Rev: **A00**

Part Number: **Enrico/Caruso 15 CP**

SSID = PCH

INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable internal VRs

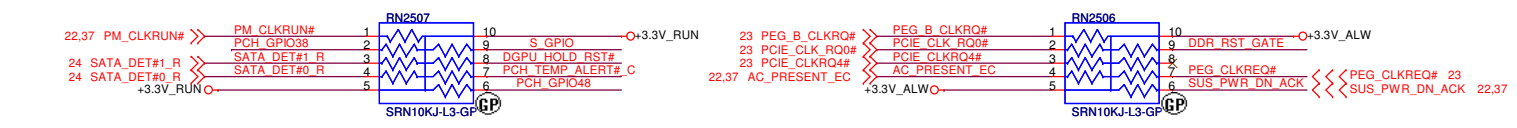
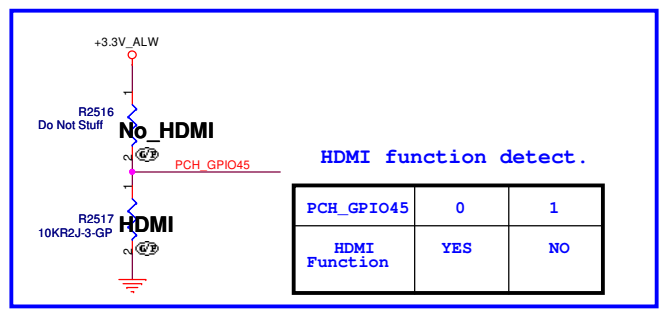
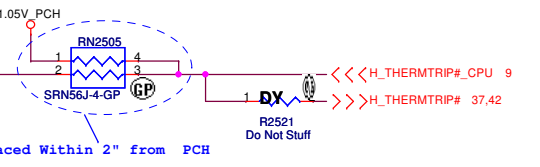
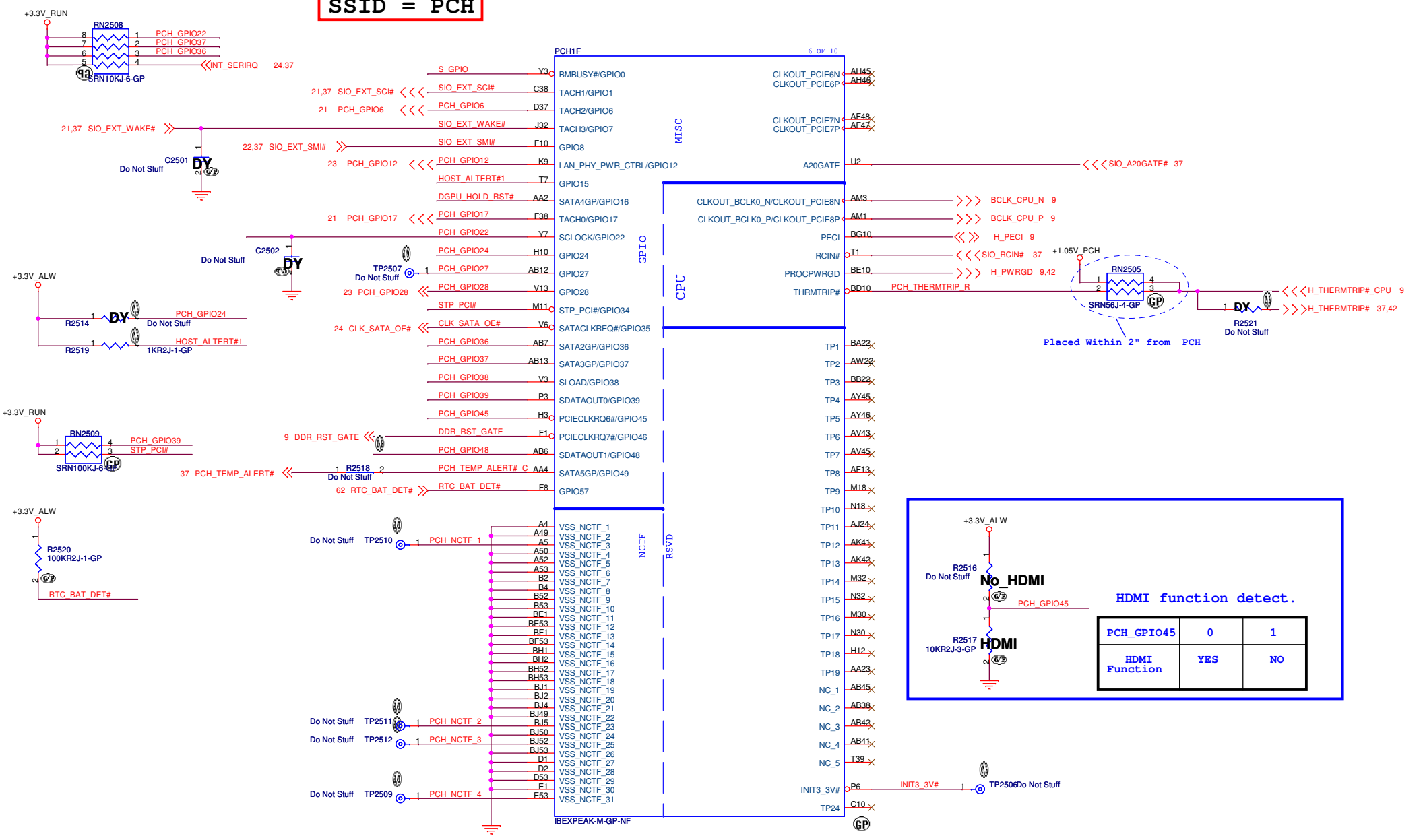
Close to PCH



DV15 CP UMA second

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title PCH (SPI/RTC/LPC/SATA/IHDA)	
Size	Document Number	Rev	
Date: Wednesday, April 13, 2011		Sheet 24 of 99	
Enrico/Caruso 15 CP		A00	

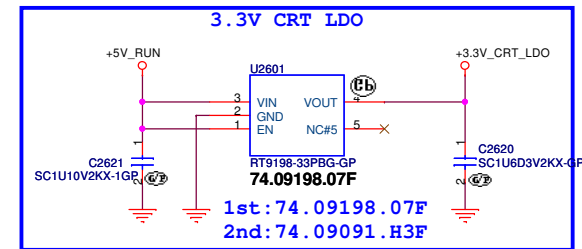
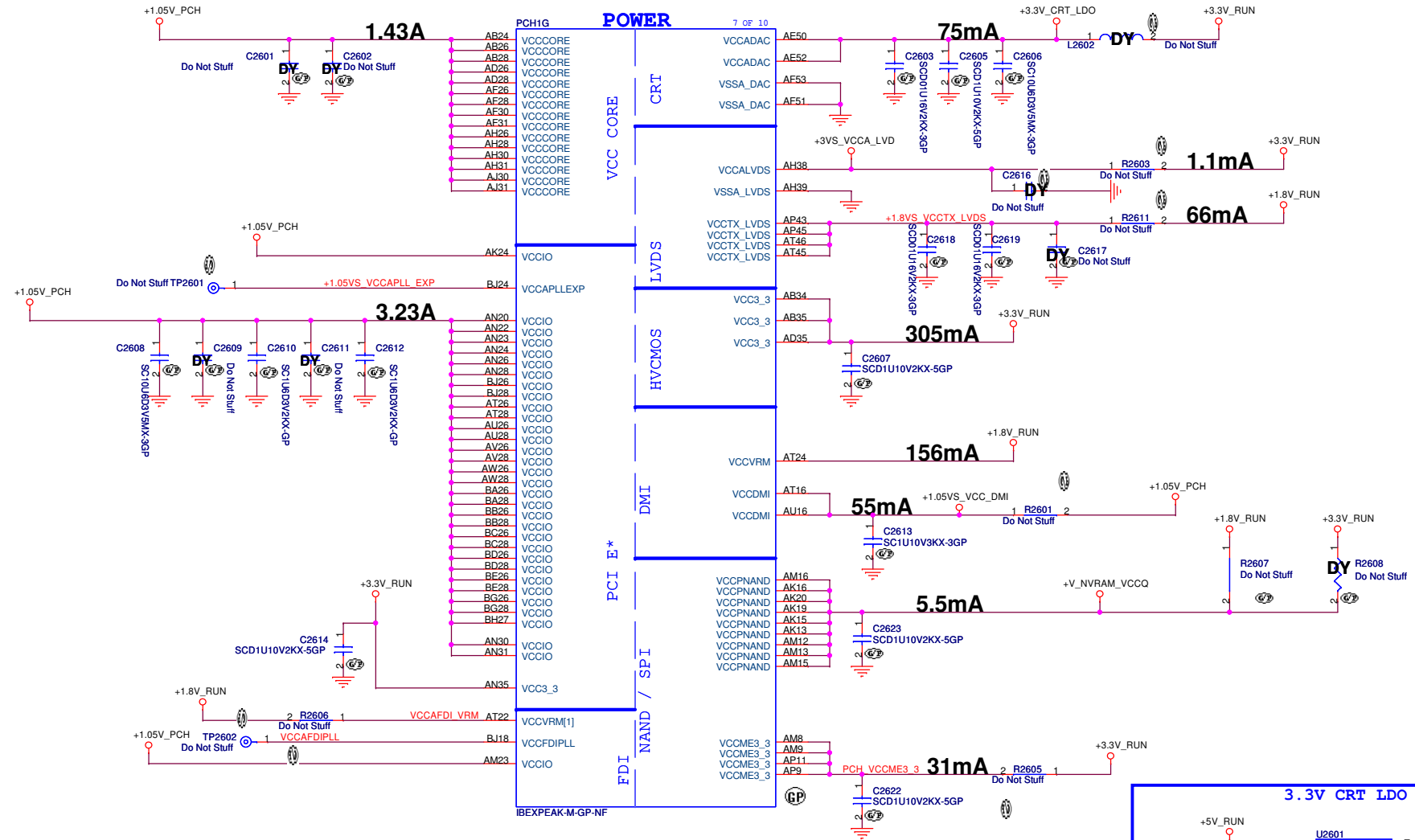
SSID = PCH



DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**
 Size: Document Number: **Enrico/Caruso 15 CP** Rev: **A00**
 Date: Wednesday, April 13, 2011 Sheet 25 of 99

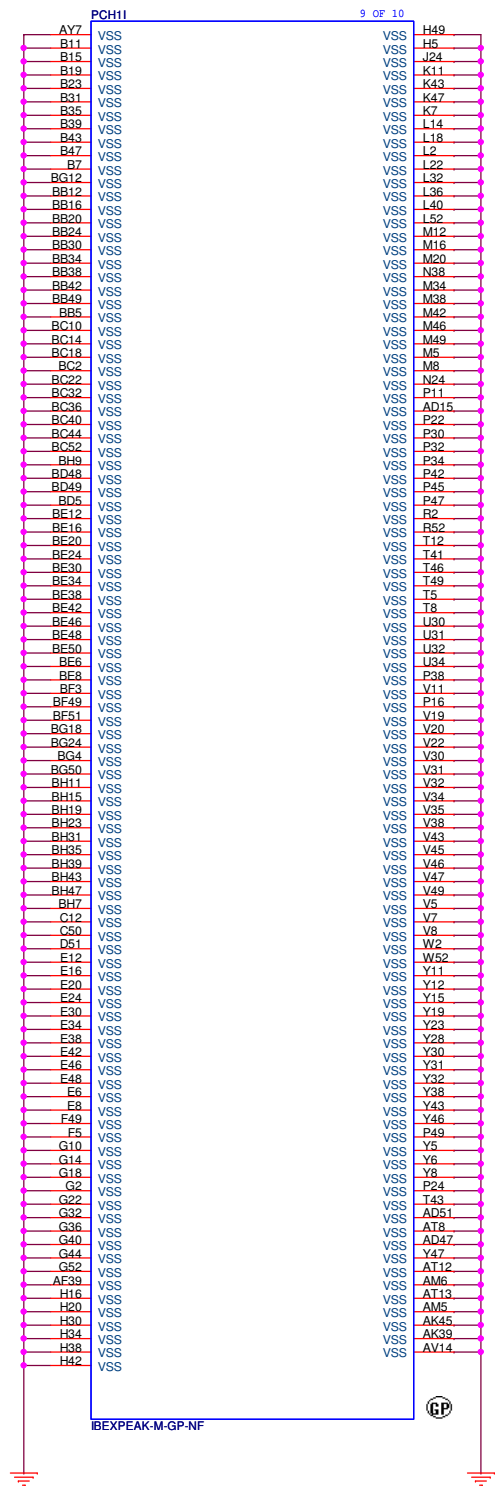
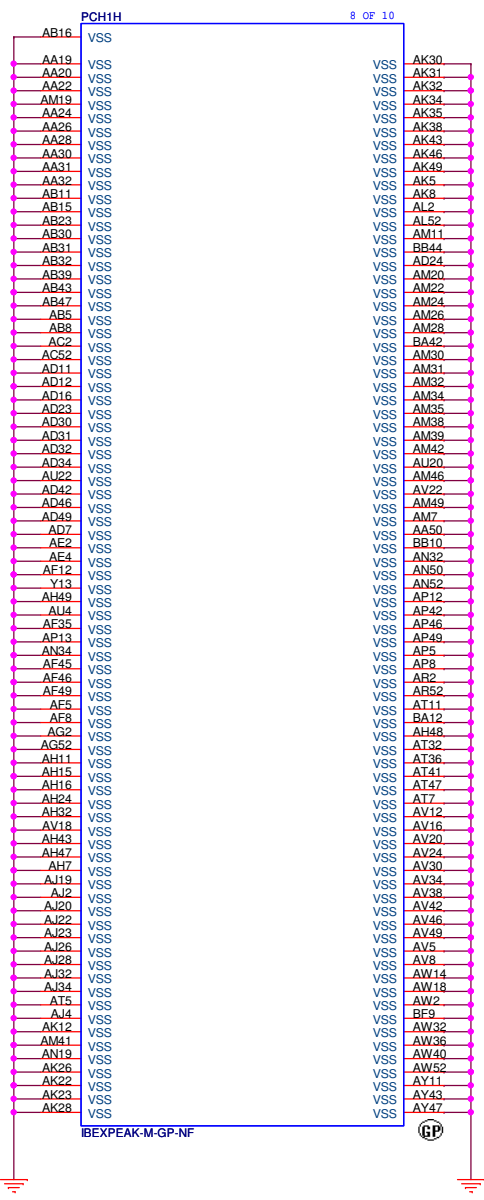
SSID = PCH



DV15 CP UMA second



SSID = PCH



DV15 CP UMA second



Title		
PCH (VSS)		
Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00
Date:	Friday, April 08, 2011	Sheet 28 of 99

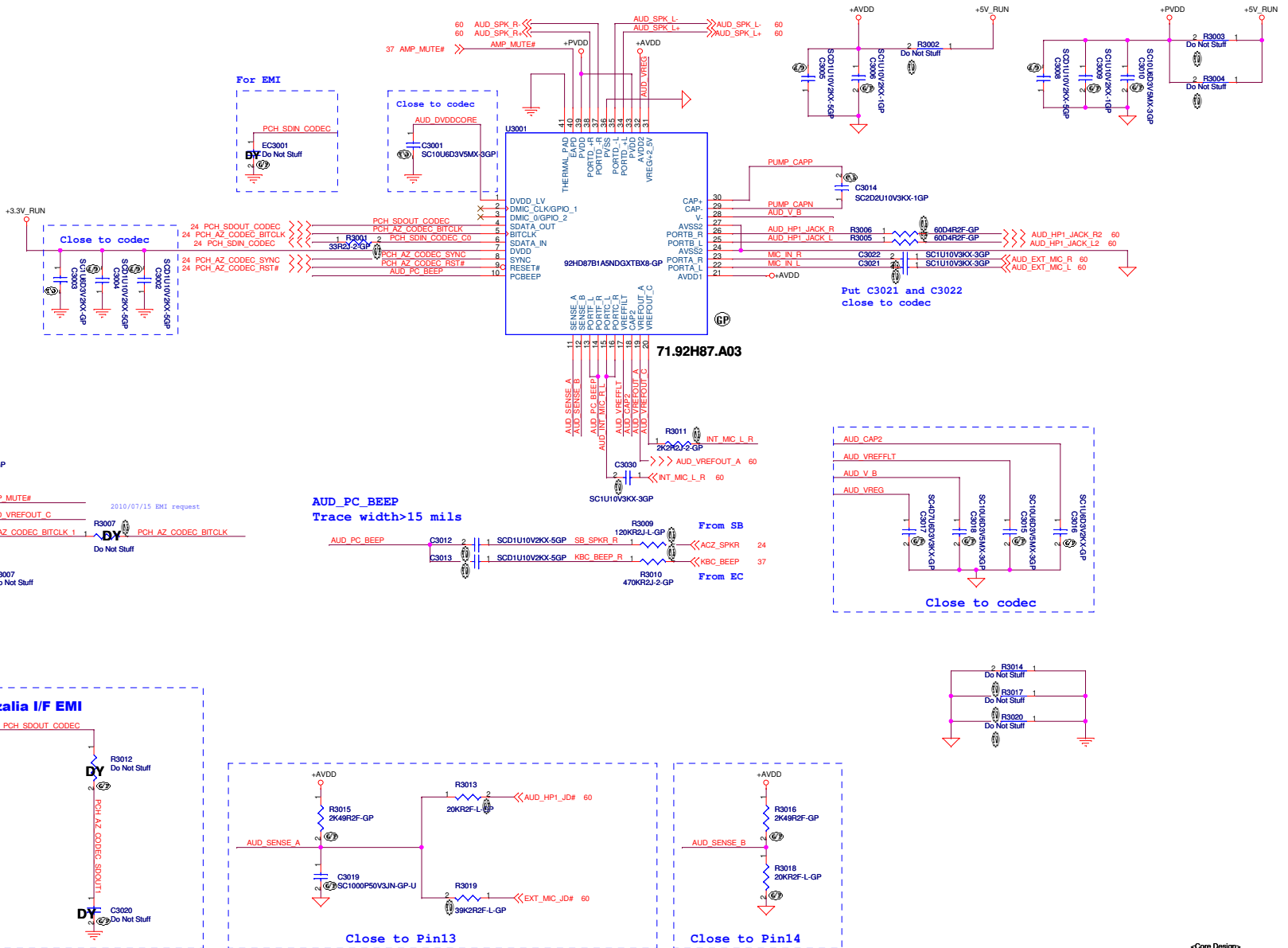
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DV15 CP UMA second



Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 29	of 99

SSID = AUDIO



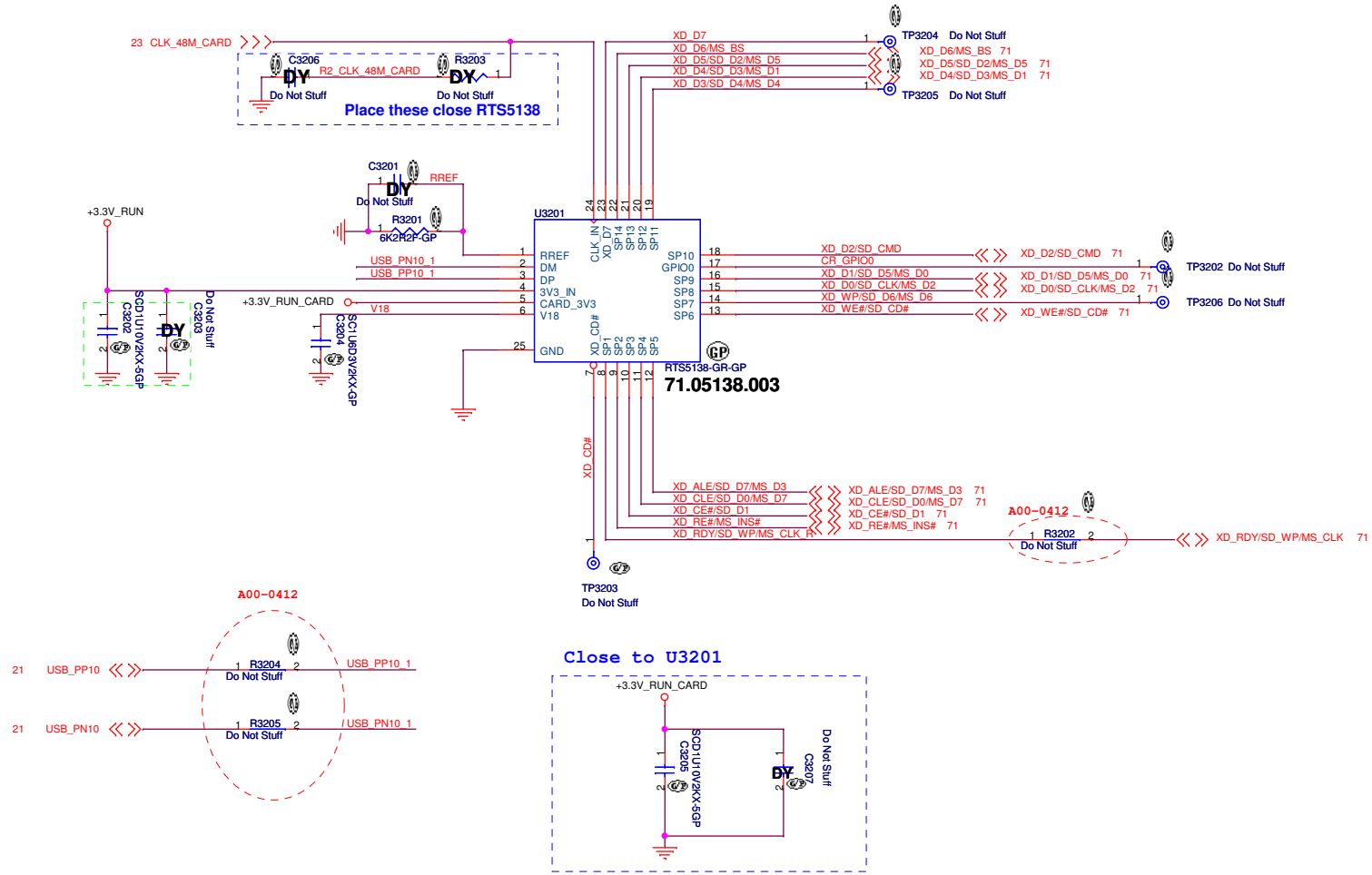
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DV15 CP UMA second



Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 31	of 99

SSID = SDIO



DV15 CP UMA second

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Card Reader-RTS5138	
Size	Document Number	Rev	
Custom	Enrico/Caruso 15 CP		A00
Date:	Wednesday, April 13, 2011	Sheet	32 of 99

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DV15 CP UMA second



Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 33 of 99	1

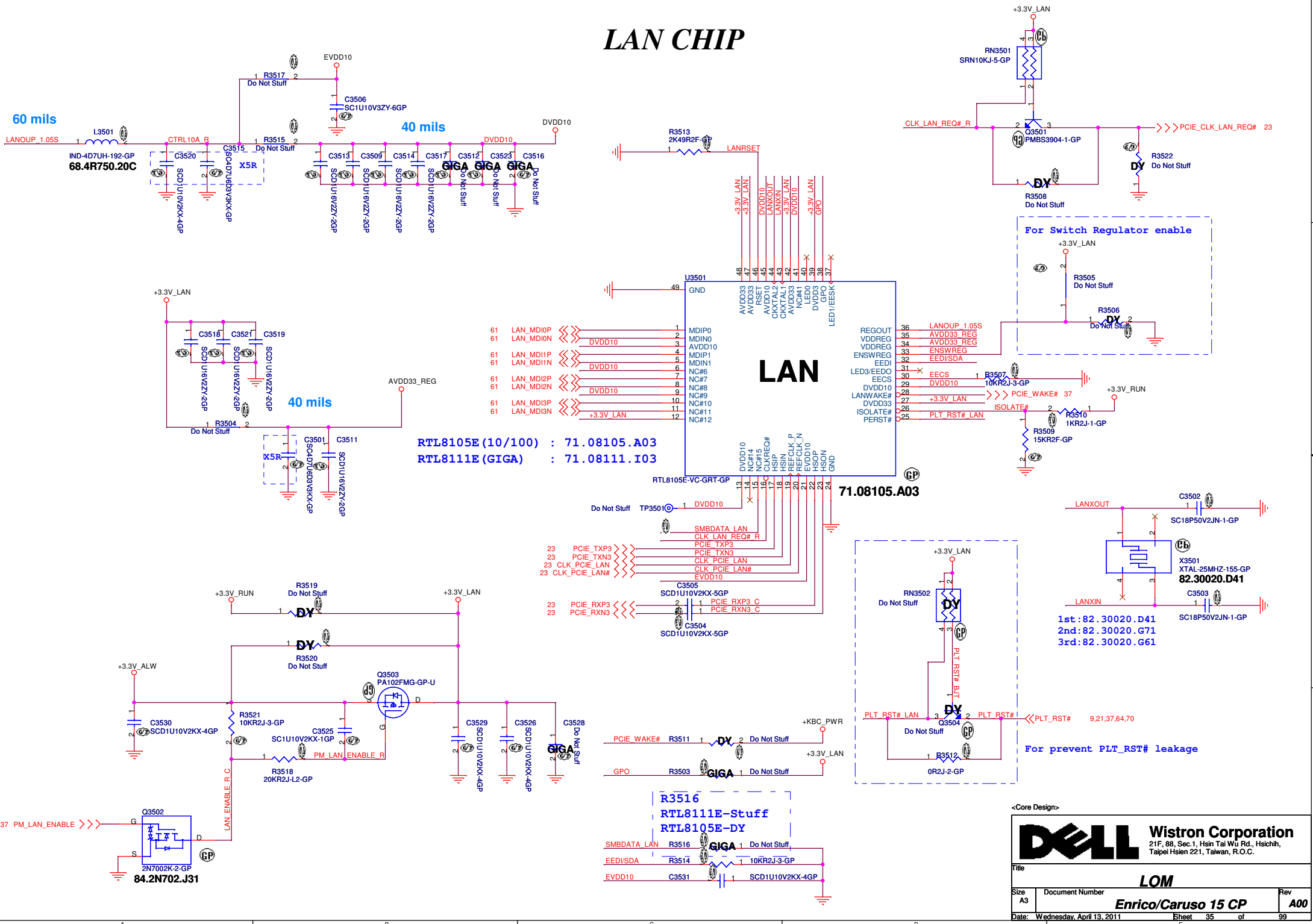
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DV15 CP UMA second



Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
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LAN CHIP



<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LOM**

Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet: 35 of 99	

(Blanking)

DV15 CP UMA second



Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 36 of 99	1

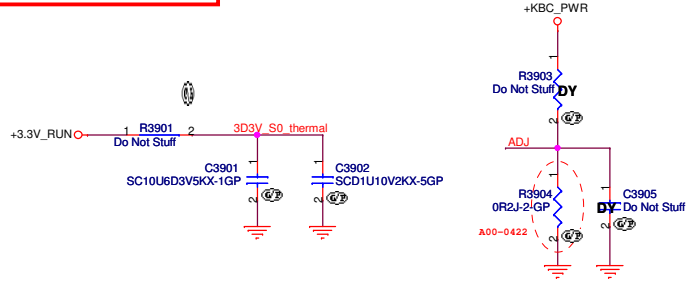
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DV15 CP UMA second



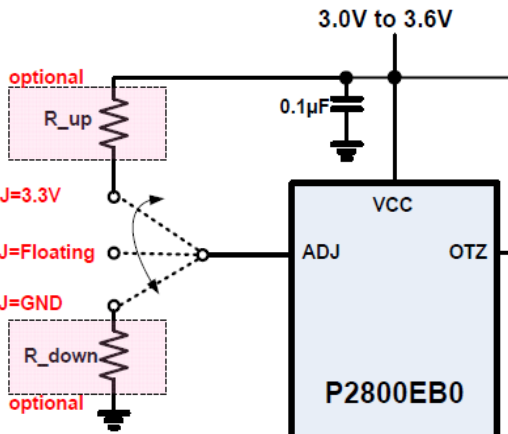
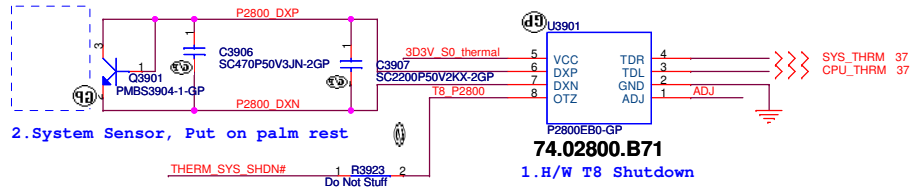
Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 38	of 99

SSID = Thermal

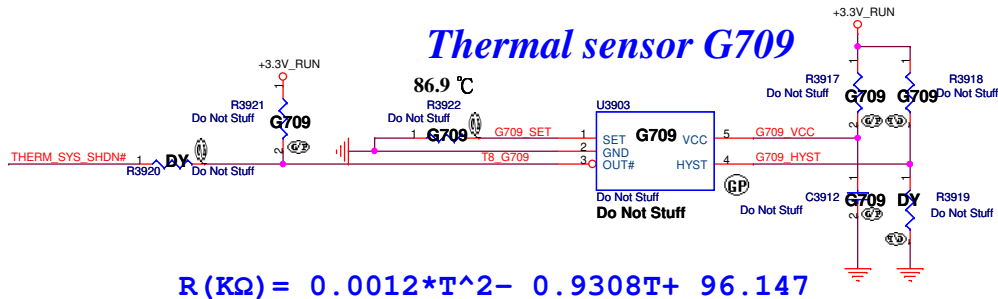


Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

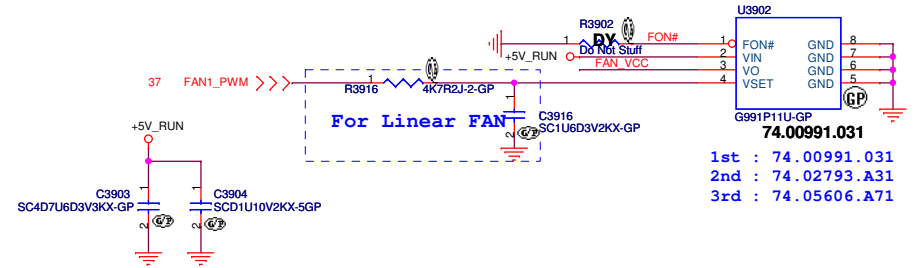
Thermal sensor P2800



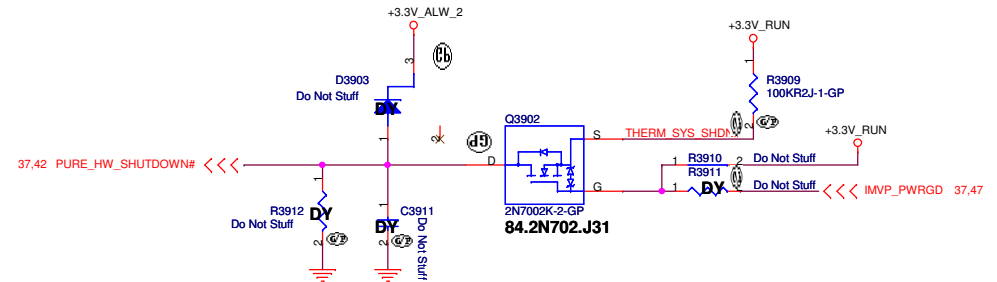
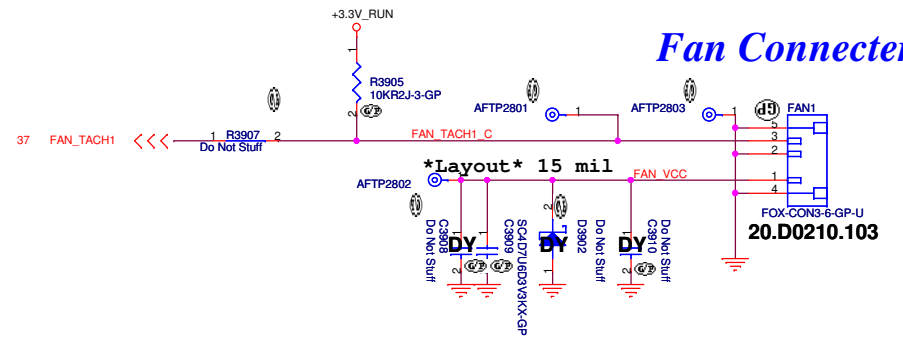
Thermal sensor G709



Fan controller



Fan Connector



DV15 CP UMA second

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Thermal sensor P2800	
Size	Document Number	Rev	
Custom	Enrico/Caruso 15 CP	A00	
Date:	Friday, April 22, 2011	Sheet	39 of 99

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DV15 CP UMA second

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 40	of 99

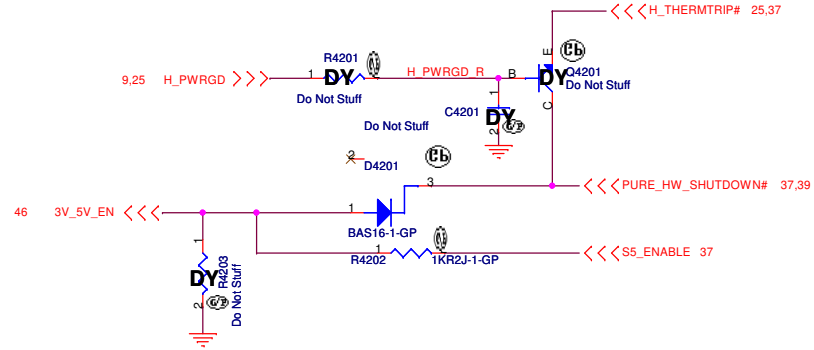
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DV15 CP UMA second

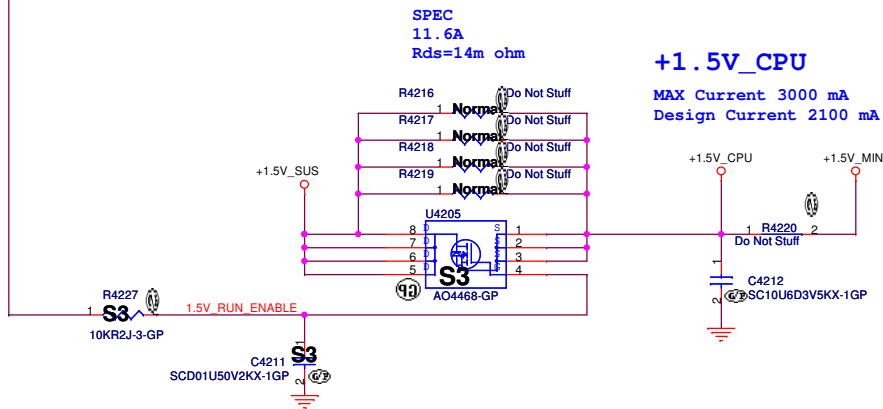
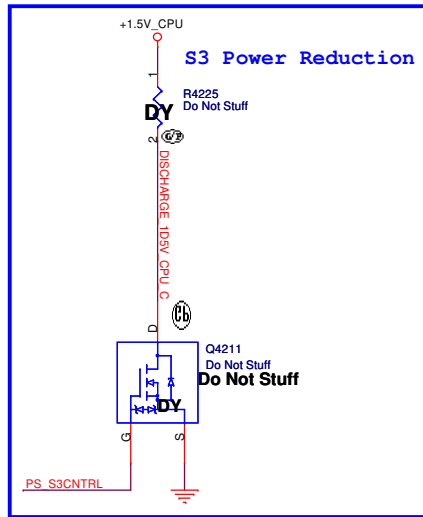
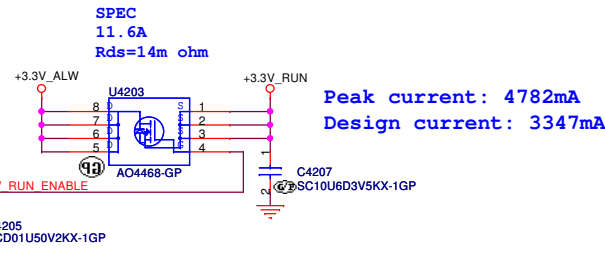
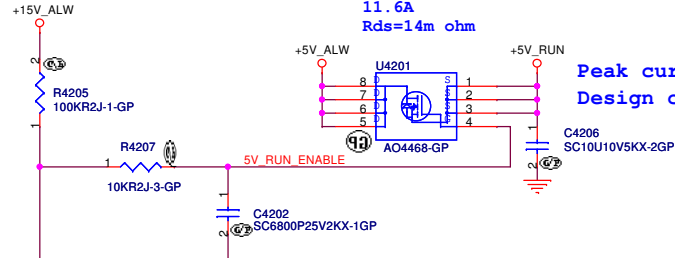
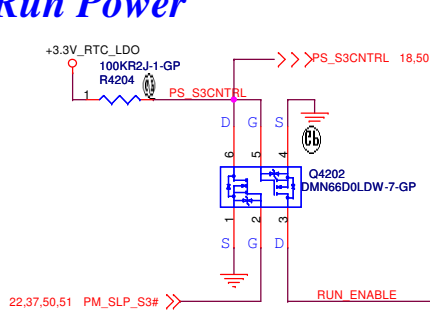


Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 41	of 99

SSID = Reset . Suspend



Run Power



+1.5V_CPU Consumption
Peak current 3A

+1.5V_MINI for Mini-Card Consumption
Peak current 1A

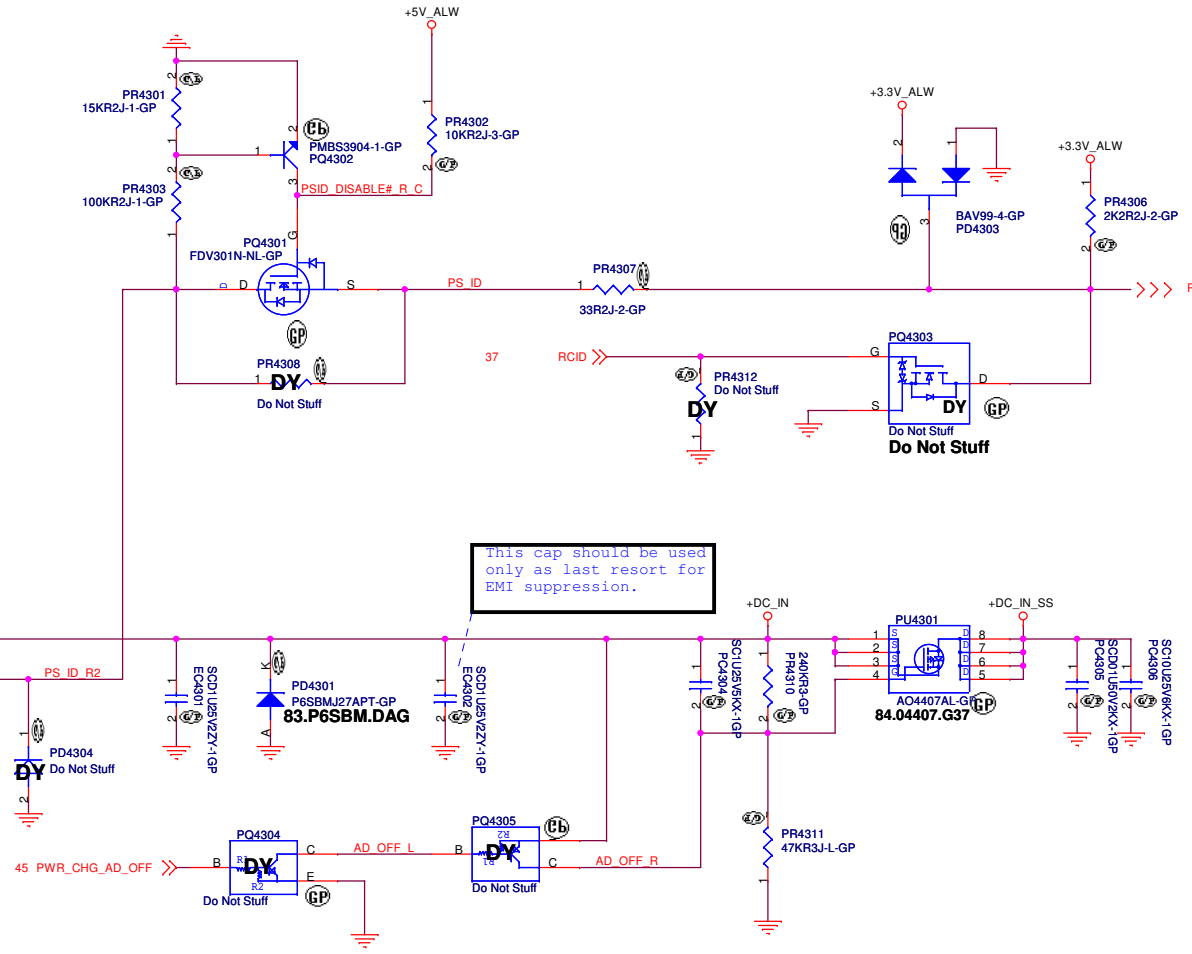
Total= 4A

SSID = PWR.Support

DCin CONN

remove EL4301 for current rating

Follow DW50

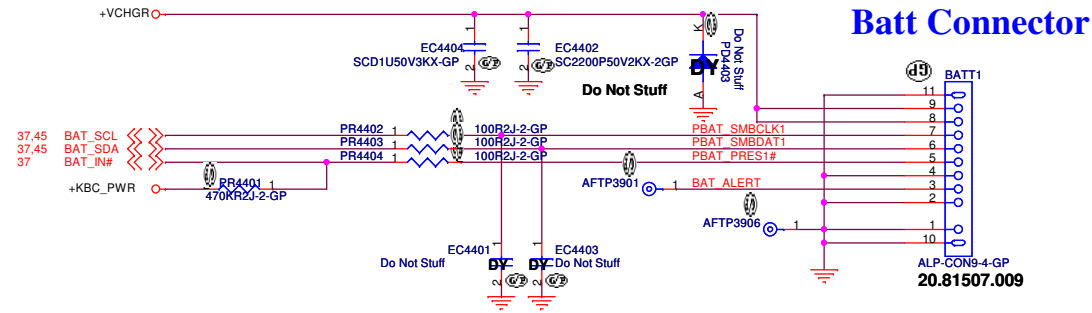


DV14 CP

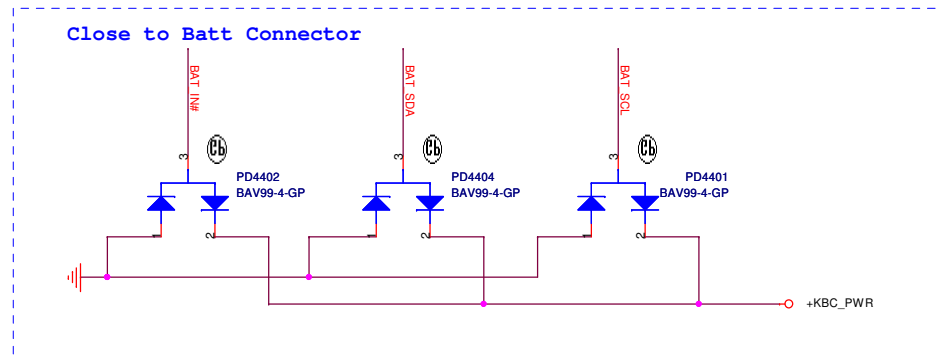


Title		
DCIN Jack		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date:	Wednesday, April 13, 2011	Sheet 43 of 99

SSID = BATT CONN



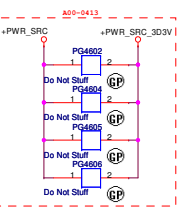
For actual location, need to be swap all pin



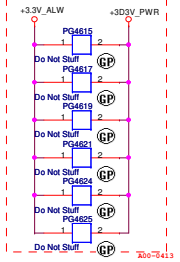
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title BATT CONN	
Size A3	Document Number Enrico/Caruso 15 CP	Rev A00	
Date: Wednesday, April 13, 2011		Sheet 44 of 99	

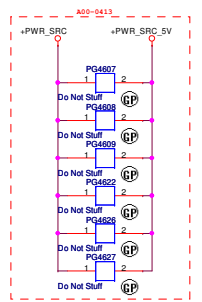
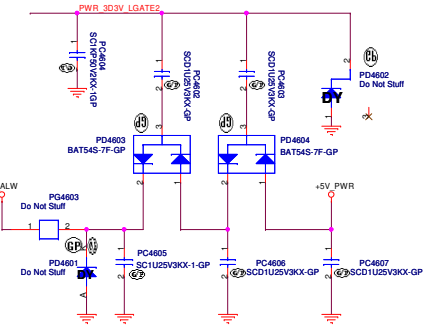
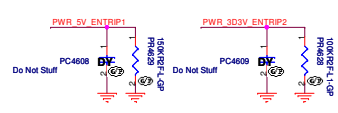
SSID = PWR.Plane.Regulator_5v3p3v



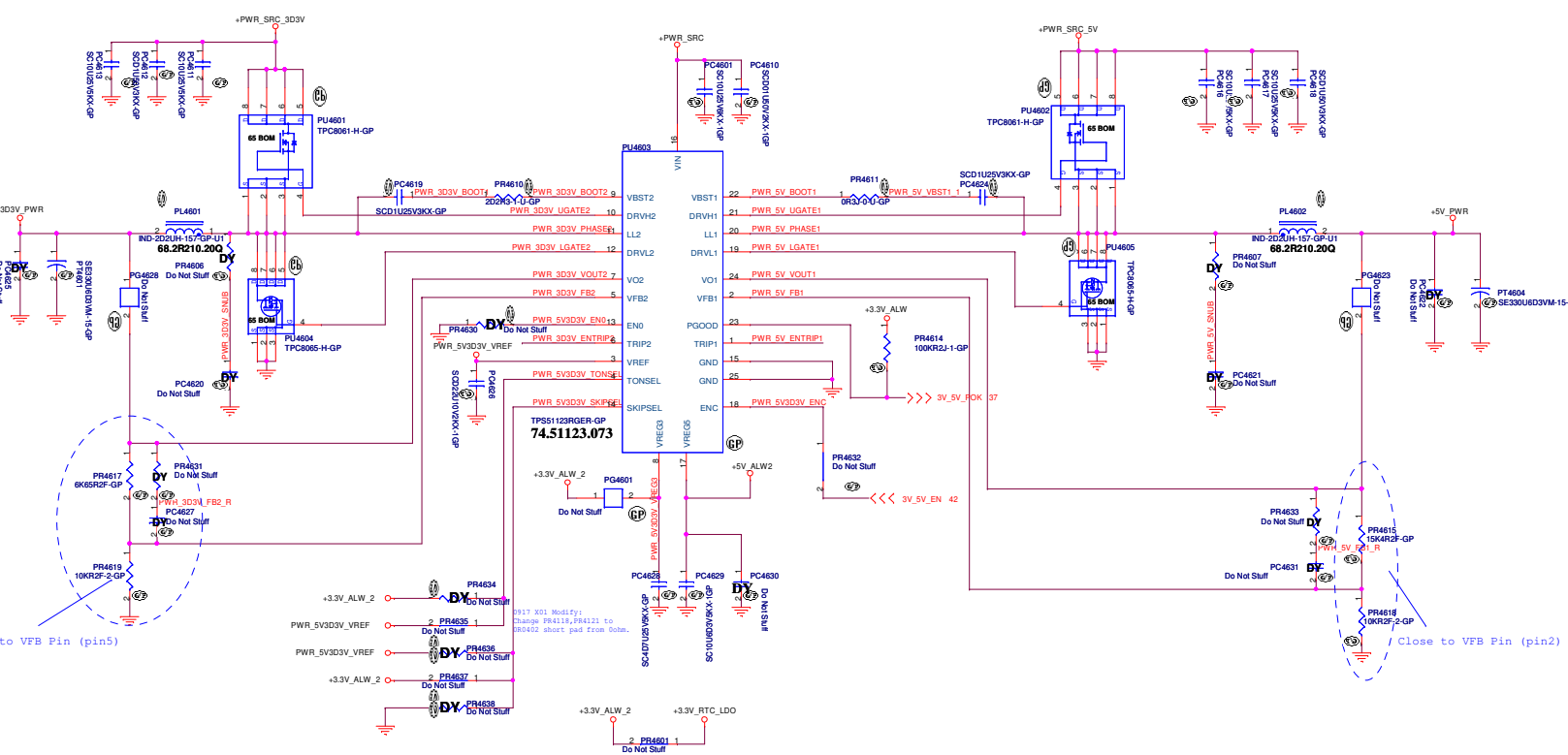
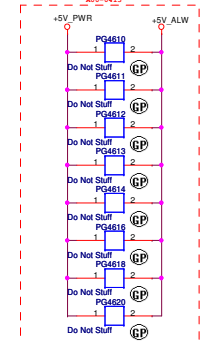
Design Current = 5.38A
8.45A < OCP < 9.98A



3007413

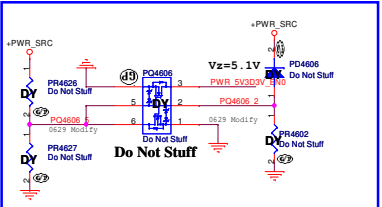


Design Current = 7.09A
11.14A < OCP < 13.17A



Close to VFB Pin (pin5)

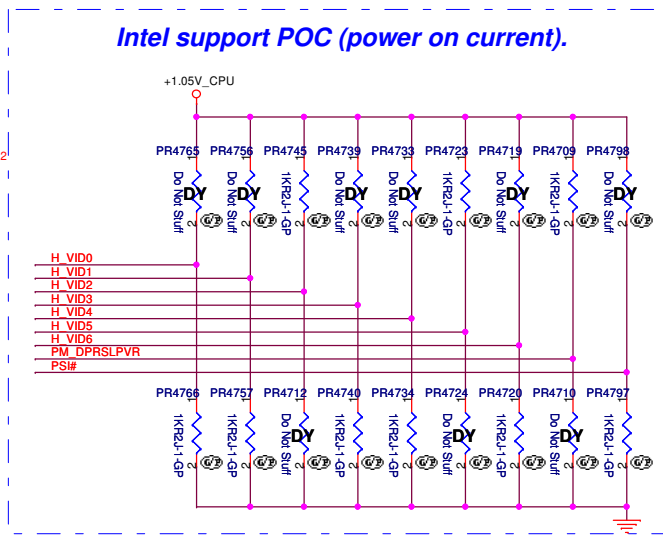
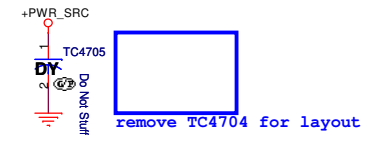
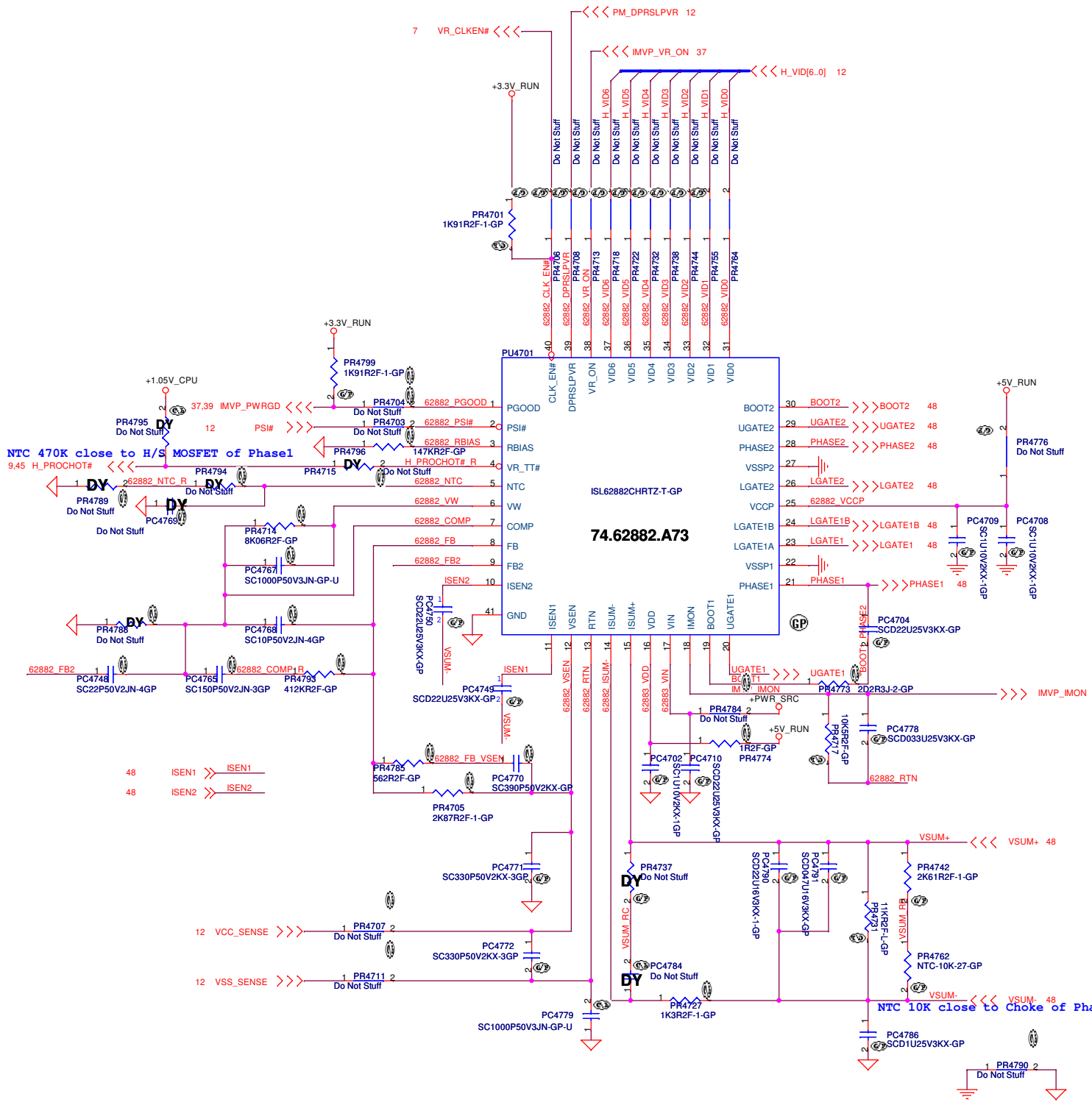
Close to VFB Pin (pin2)



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 2.2U PCMC063T-2R2MH Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.200
 O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L
 O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L
 H/S: TPC8061-H / 21mohm/30mOhm84.5Vgs/ 84.08061.037
 L/S: TPC8065-H / 12mohm/15mOhm84.5Vgs/ 84.08065.037

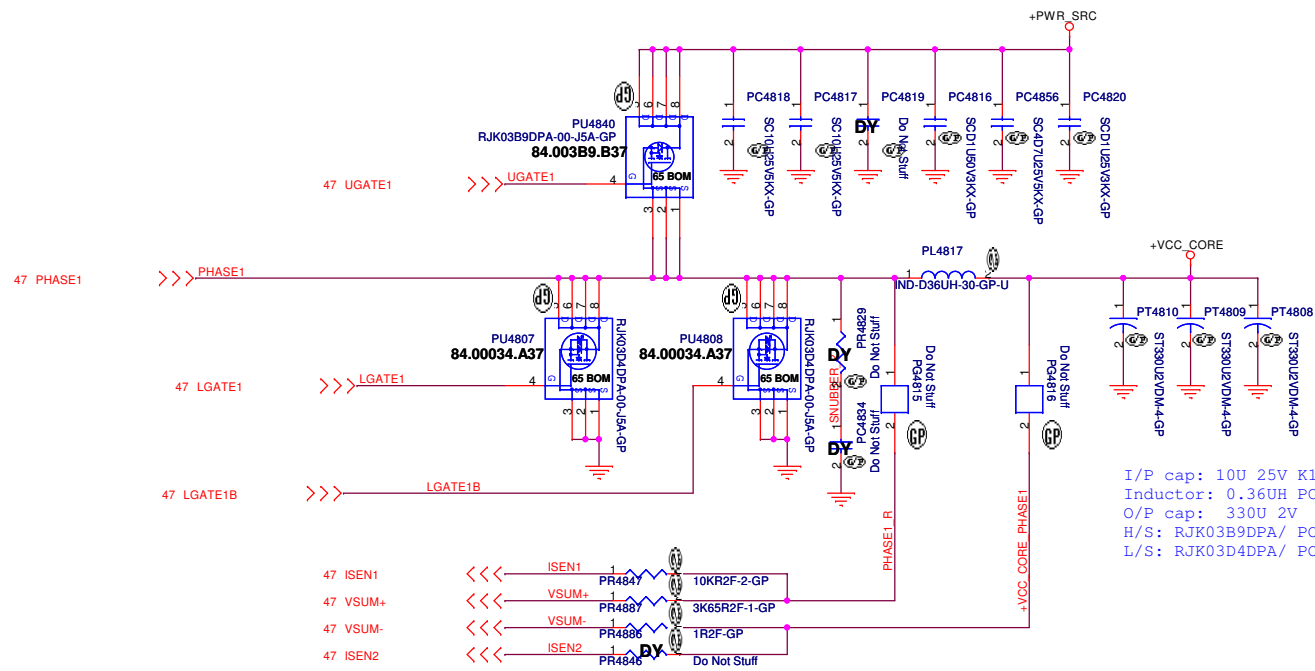
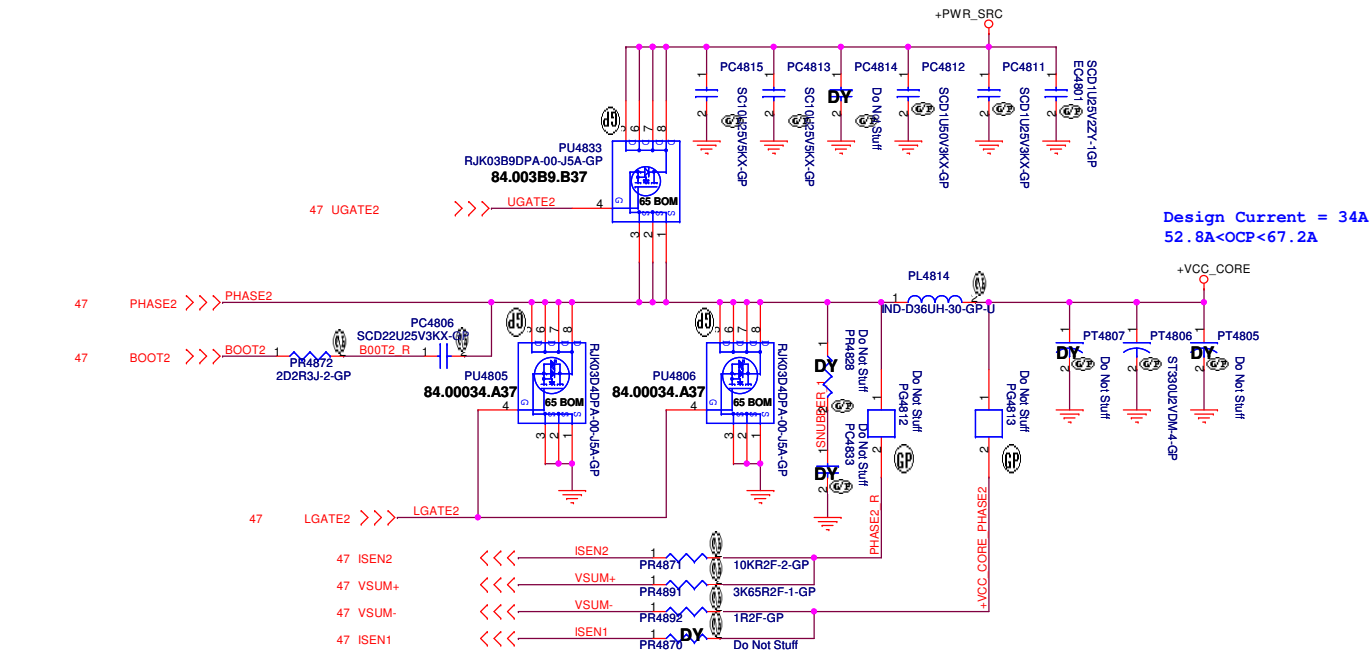


DV15 CP UMA second

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL62883 CPU CORE**

Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet: 47	of 99

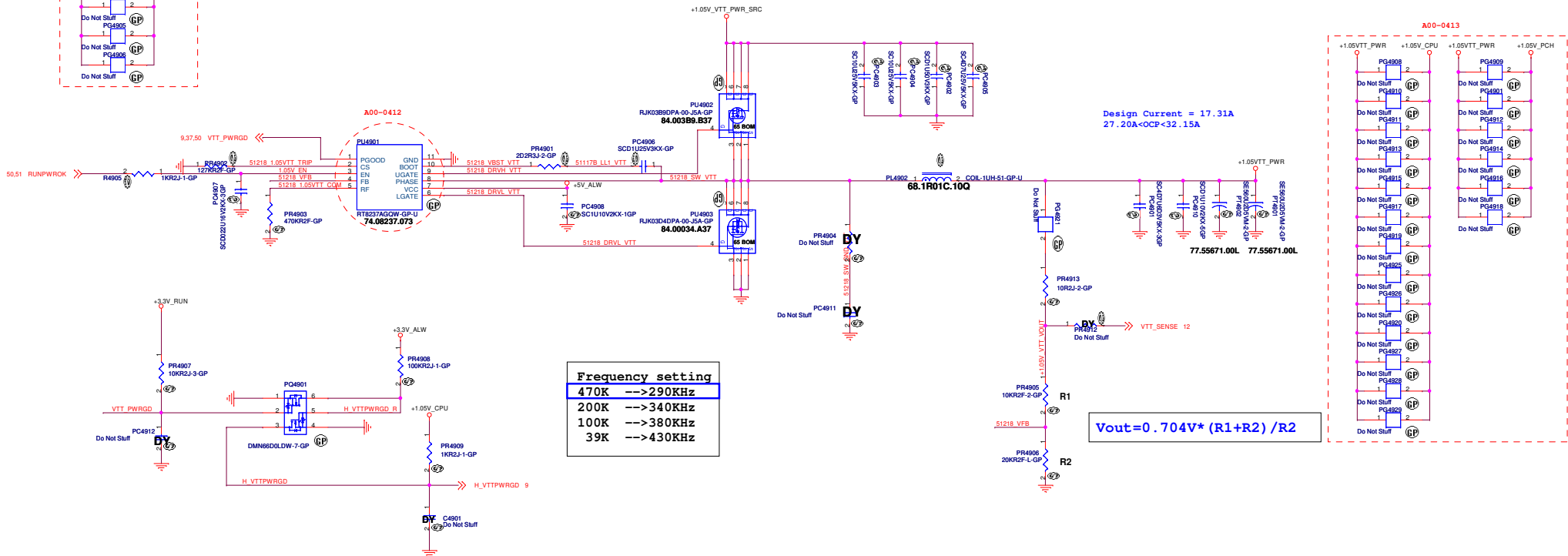


DV15 CP UMA second



Title		
ISL62883 CPU CORE		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
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RT8237A for +1.05V_VTT

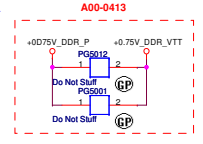
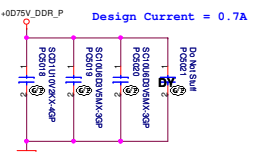
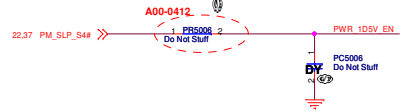
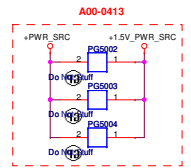
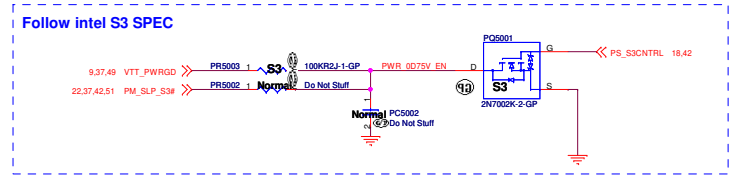
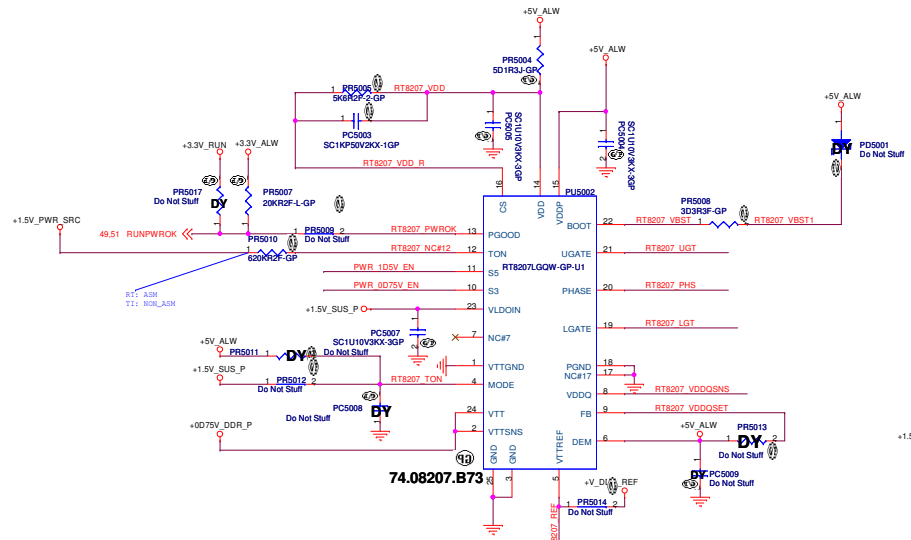


Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

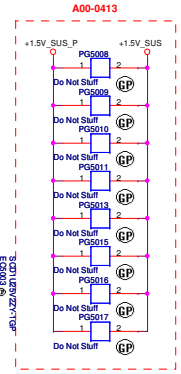
Design Current = 17.31A
27.20A<OCP<32.15A

$$V_{out} = 0.704V * (R1 + R2) / R2$$

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 1UH P06C104T-1R0MH Cynotec 3mohm/3.3mohm Isat =28Arms 68.1R01C.100
 O/P cap: CHIP CAP POL 560U 2.5V 6.3*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L
 O/P cap: CHIP CAP POL 560U 2.5V 6.3*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mOhm@4.5Vgs/ 84.00034.A37



Design Current = 7.35A
11.55A < OCP < 13.65A

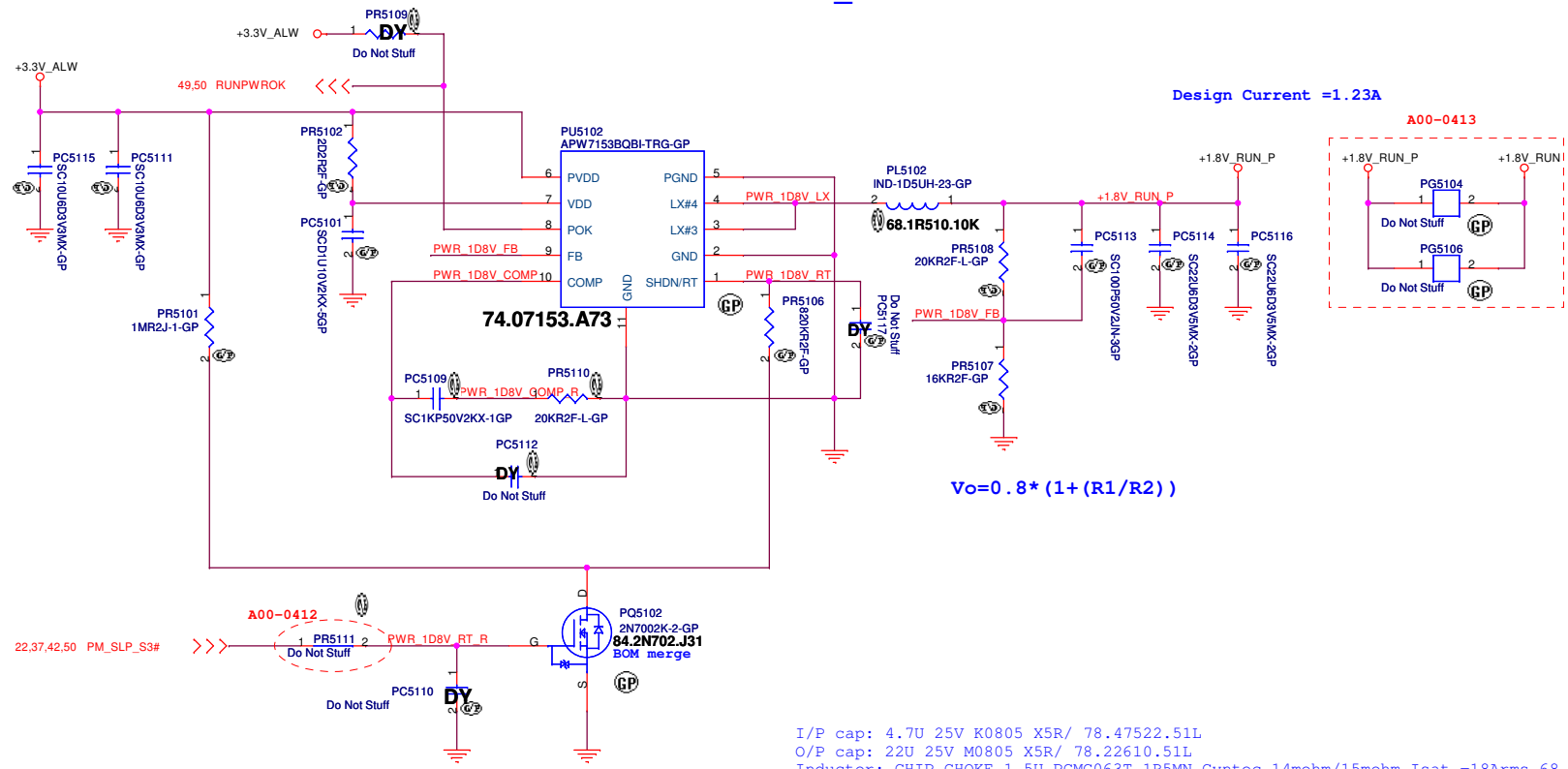


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
VSIN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 1.50 PCMC104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
 O/P cap: CHIP CAP POL 560U 2.5V 6.3*5.7 15mohm 3.5Arms Matsuki/77.55671.00L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mohm/15.1mohm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mohm/5.6mohm@4.5Vgs/ 84.00034.A37

APW7153B for 1D8V_RUN



INS 100 NONE SURGE

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			Title: APW7153B for 1D8V RUN
Size A3	Document Number Enrico/Caruso 15 CP	Rev A00	
Date: Friday, April 15, 2011	Sheet 51	of 99	

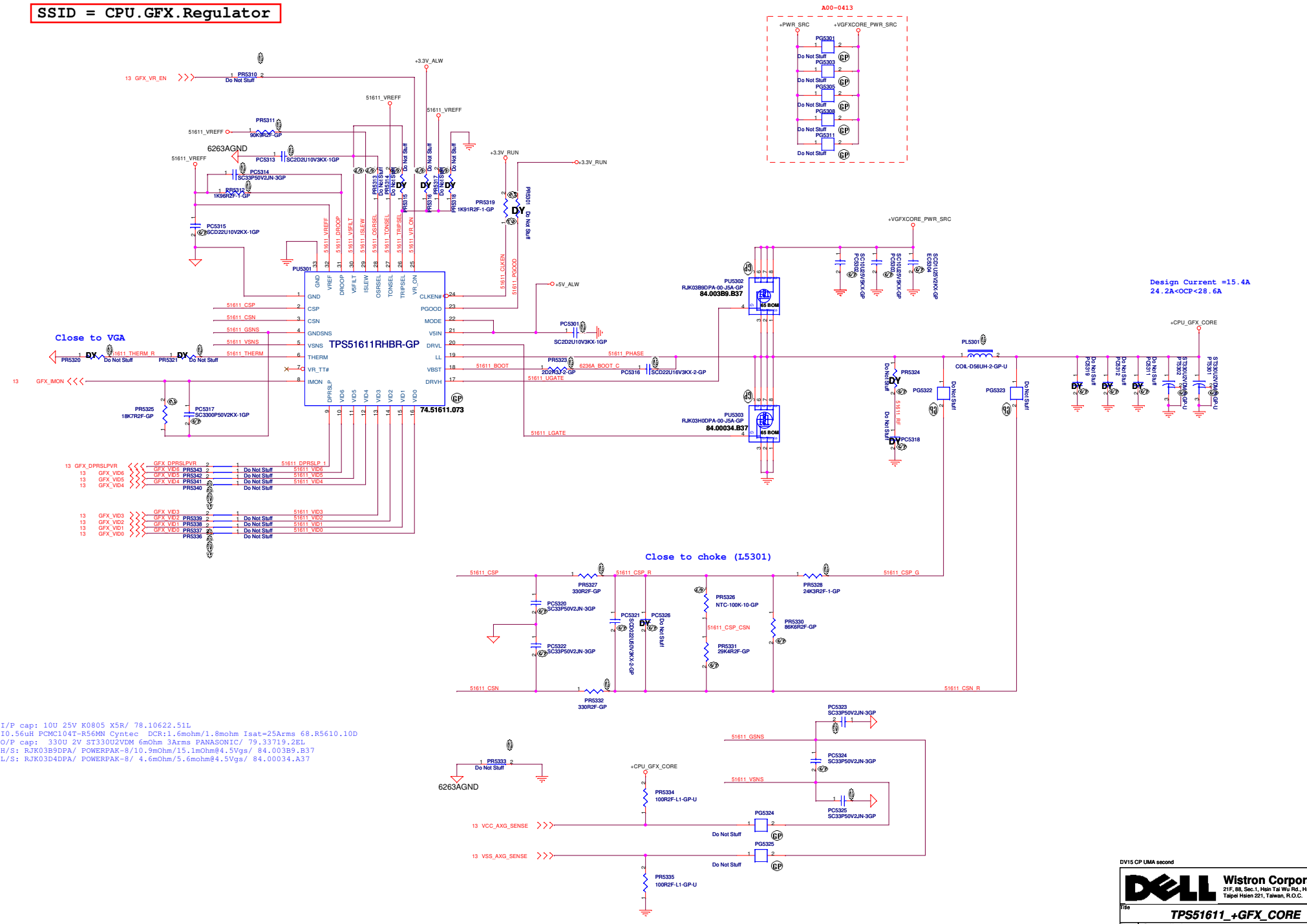
(Blanking)

DV15 CP UMA second



Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
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SSID = CPU.GFX.Regulator



Design Current =15.4A
24.2A<OCP<28.6A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
I/O.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2V ST330U2VDM 6mOhm 3Arms PANASONIC/ 79.33719.2EL
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

(Blanking)

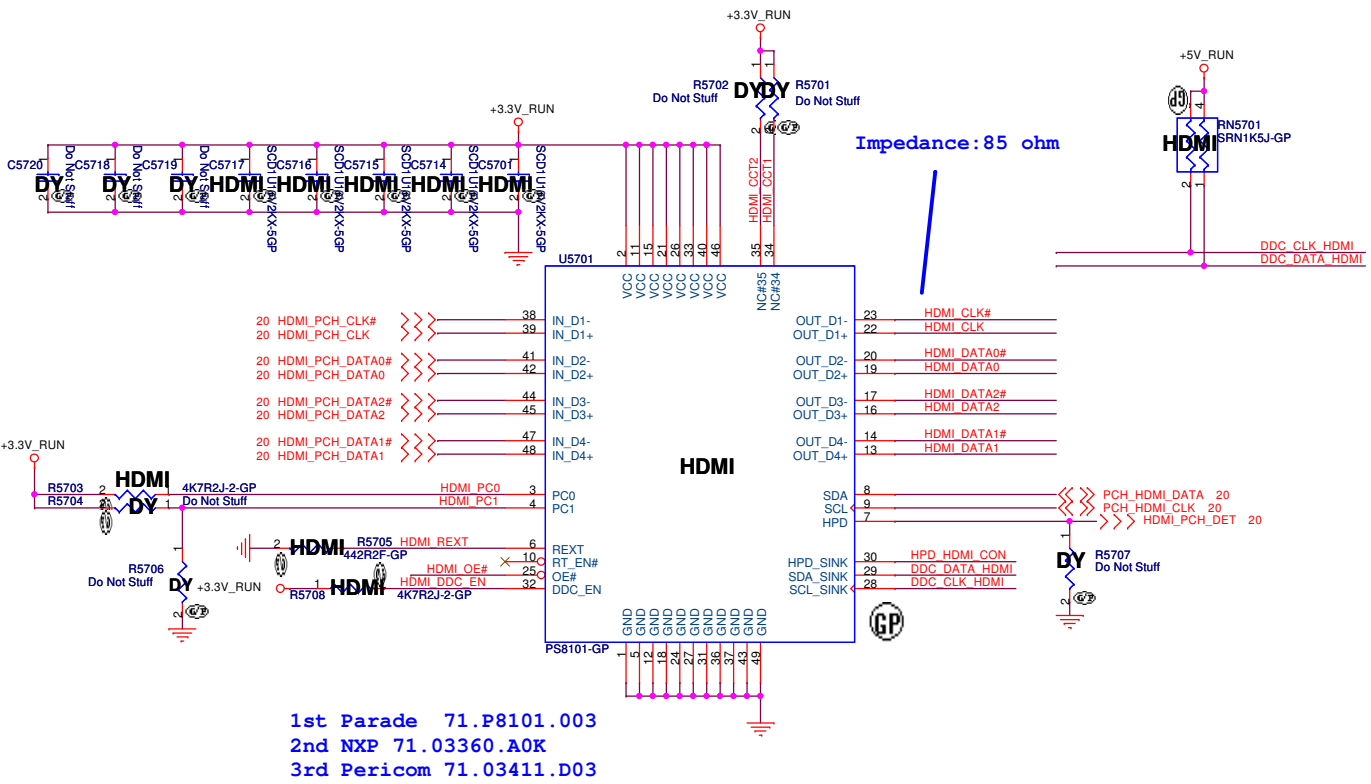
DV15 CP UMA second



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Reserved		
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SSID = VIDEO

HDMI Level Shifter & CONNECTOR

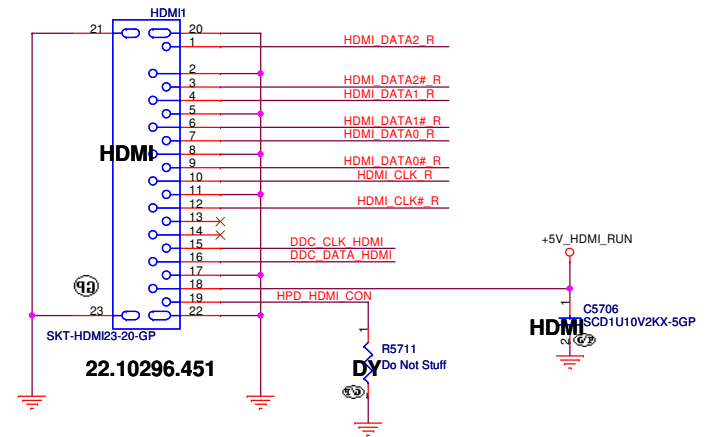


1st Parade 71.P8101.003
 2nd NXP 71.03360.A0K
 3rd Pericom 71.03411.D03

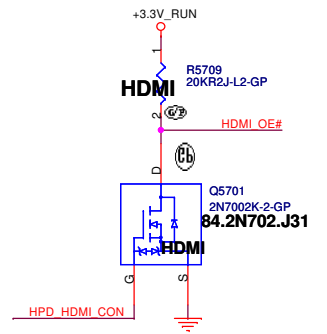
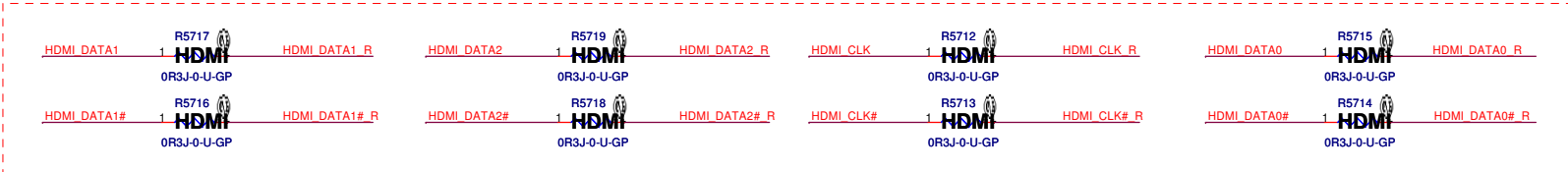
HDMI level shifter BOM controll table

		PS8101	PTN3360B	PI3VDP411LSR
PIN3	R5703	Stuff 4.7K_5%	DY	DY
PIN4	R5704	DY	DY	DY
	R5706	DY	DY	Stuff 200K_5%
PIN6	R5705	Stuff 499_1%	Stuff 10K_1%	DY
PIN10		NC	NC	NC

HDMI CONN



A00-0412



DV15 CP UMA second

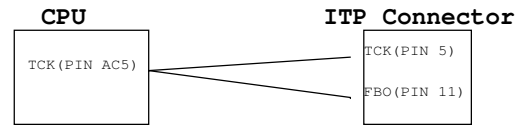
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 Taipei Hsien 221, Taiwan, R.O.C.

HDMI Level Shift/ Connector		
Size A3	Document Number	Rev
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



REMOVE FAN CONNECTOR FOR HR THERMAL SOLUTION 7/12

DV15 CP UMA second



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Title

ITP Connector

Size
A3

Document Number

Enrico/Caruso 15 CP

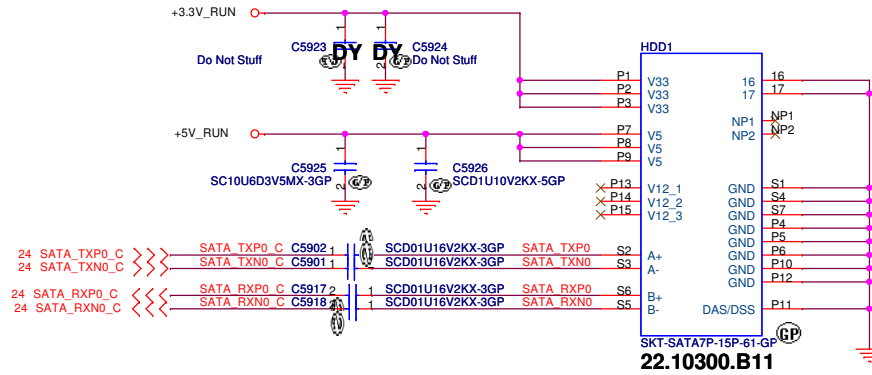
Rev

A00

Date: Friday, April 08, 2011

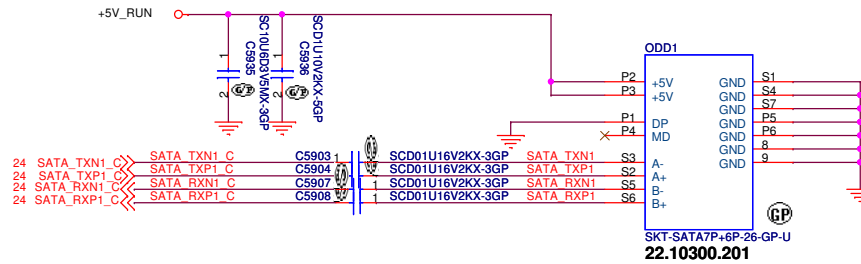
Sheet 58 of 99

SATA HDD Connector



SATA ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

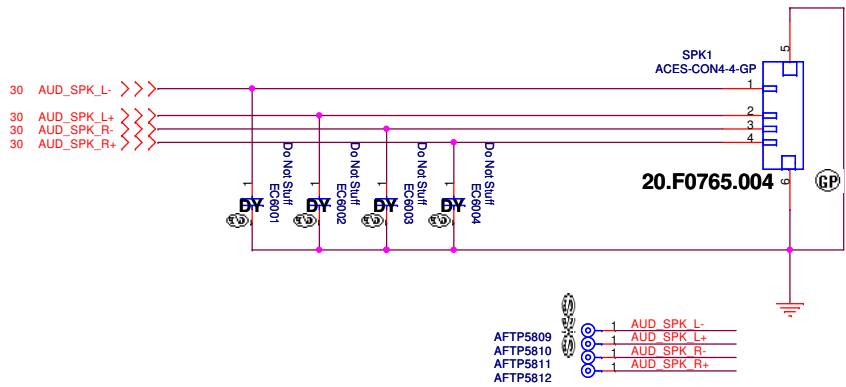


DV15 CP UMA second

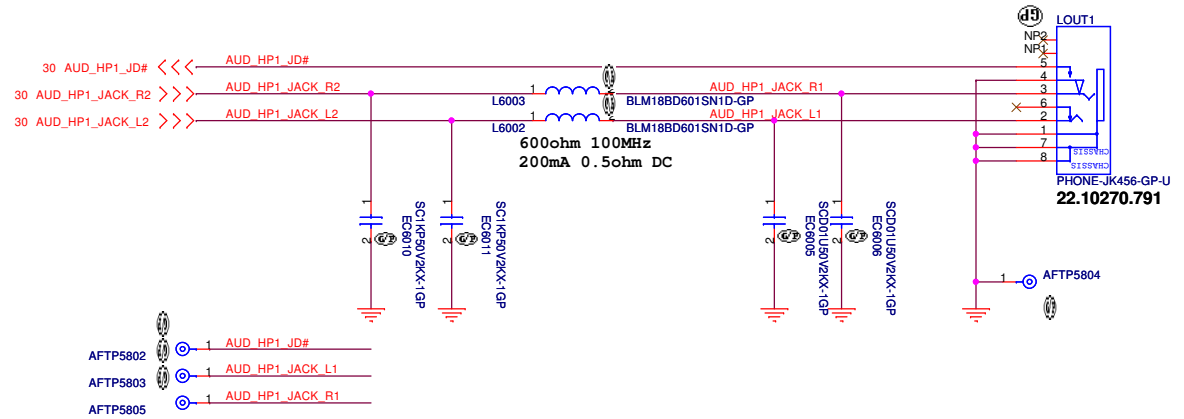


SSID = AUDIO

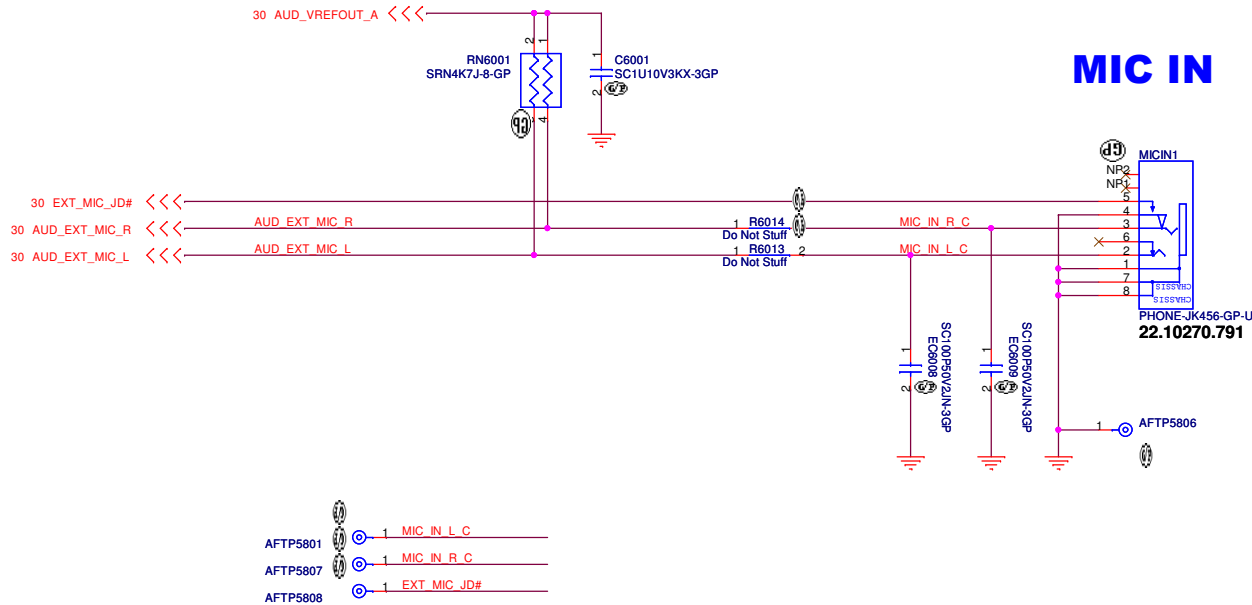
Speaker Connector



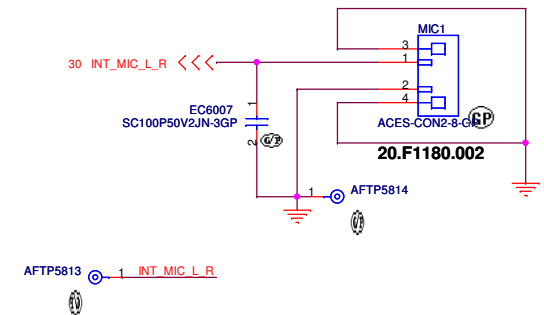
LINE1 OUT



MIC IN



Internal Microphone



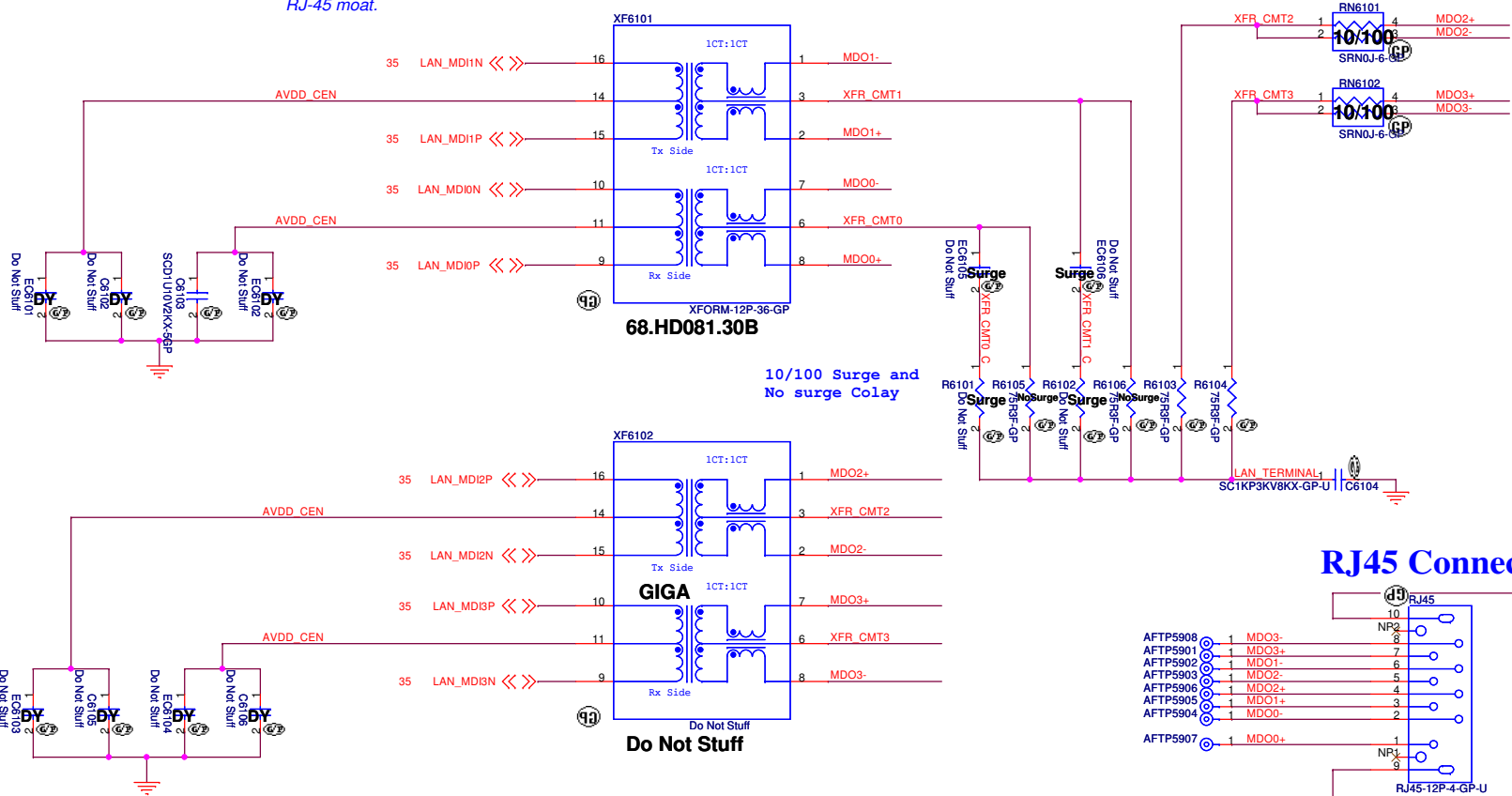
DV15 CP UMA second

DELL		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Audio Jack			
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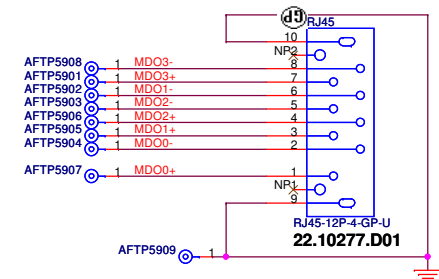
2009-10-1 Change MDI1+ (XF601.16) to MDI1+ (XF601.15)
 Change MDI1- (XF601.15) to MDI1- (XF601.16)
 Change MDI0+ (XF601.10) to MDI0+ (XF601.9)
 Change MDI0- (XF601.9) to MDI0- (XF601.10)
 Change RJ45-3 (XF601.1) to RJ45-3 (XF601.2)
 Change RJ45-6 (XF601.2) to RJ45-6 (XF601.1)
 Change RJ45-1 (XF601.7) to RJ45-1 (XF601.8)
 Change RJ45-2 (XF601.8) to RJ45-2 (XF601.7)

1. route on bottom as differential pairs.
 2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
 3. No vias, No 90 degree bends.
 4. pairs must be equal lengths.
 5. 6mil trace width, 12mil separation.
 6. 36mil between pairs and any other trace.
 7. Must not cross ground moat, except RJ-45 moat.

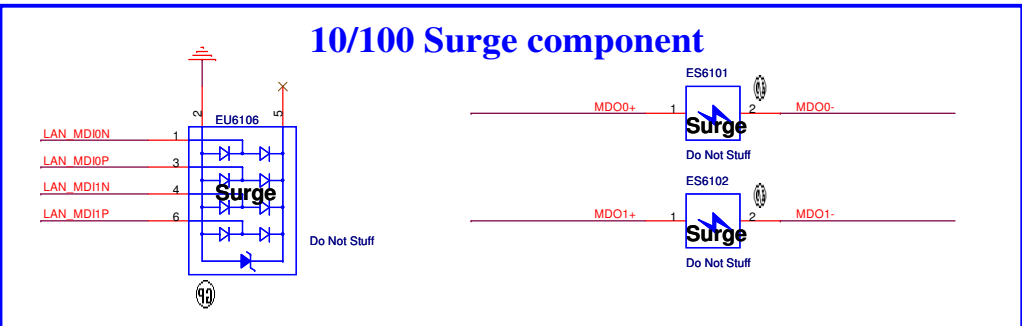
10/100M Lan Transformer



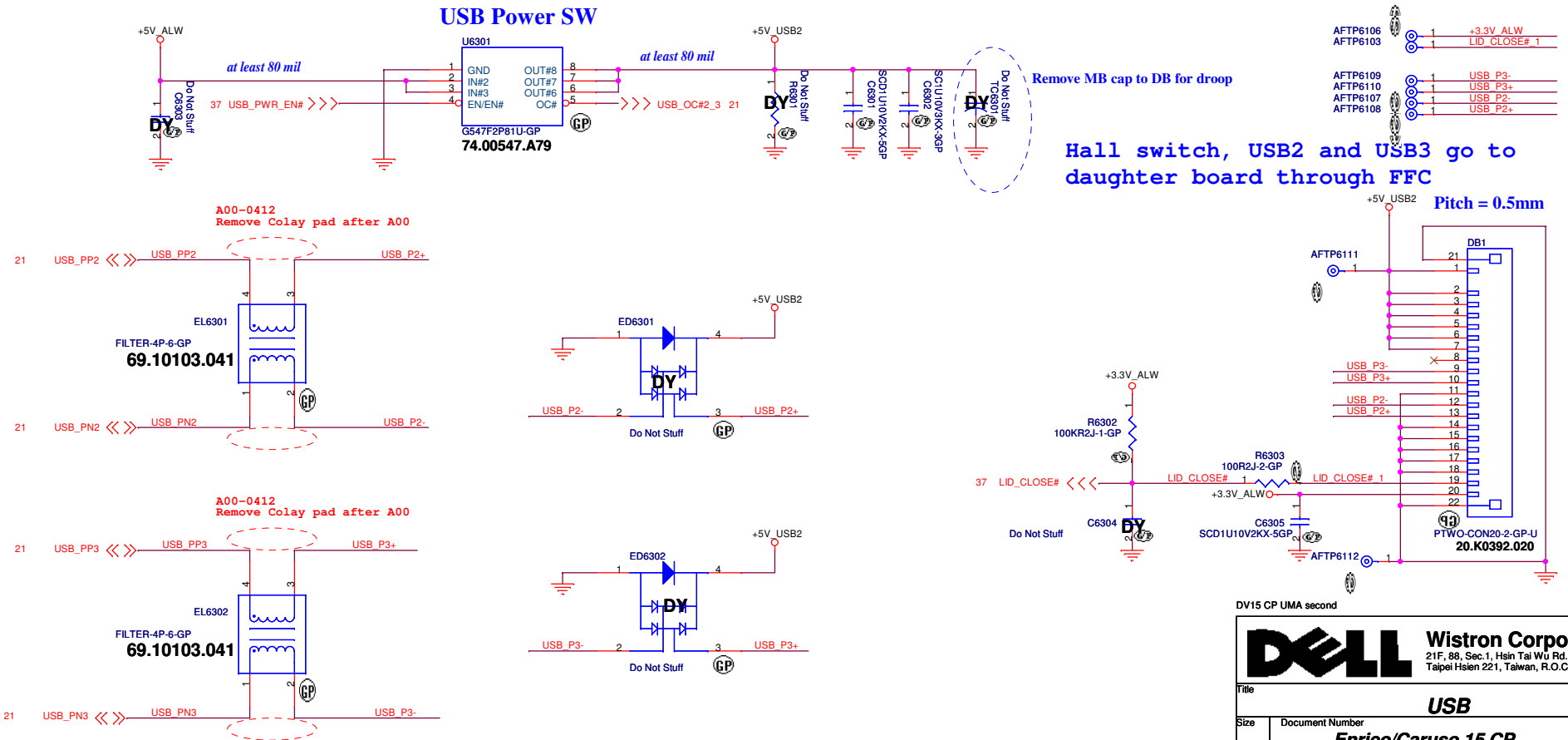
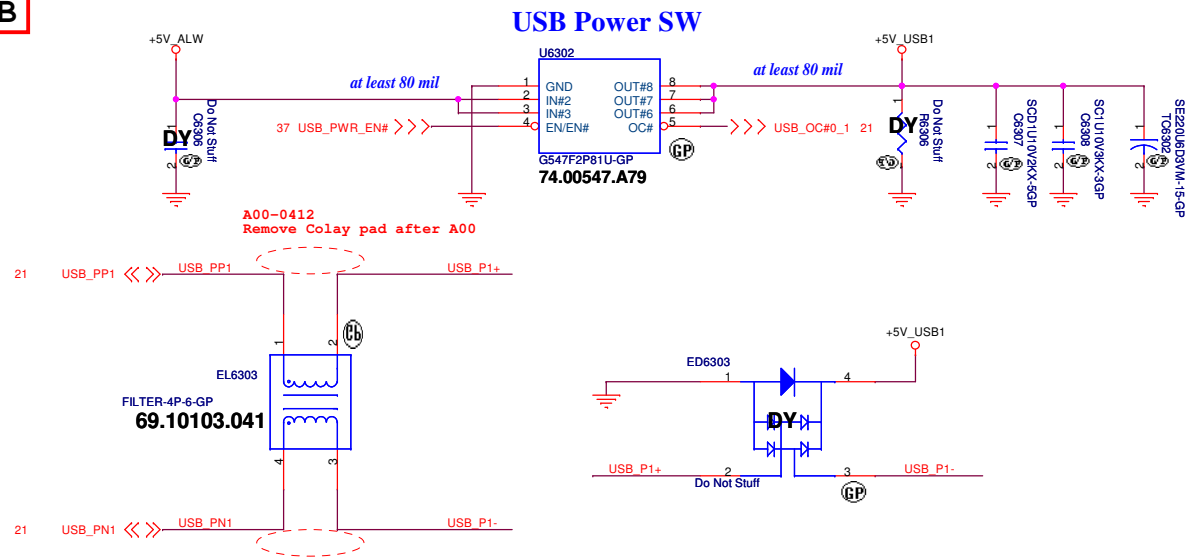
RJ45 Connector



10/100 Surge component



SSID = USB



DV15 CP UMA second

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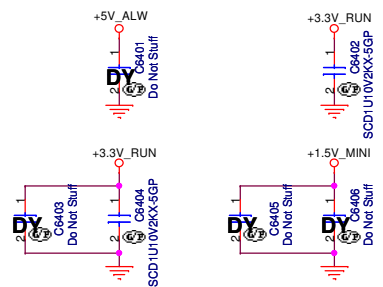
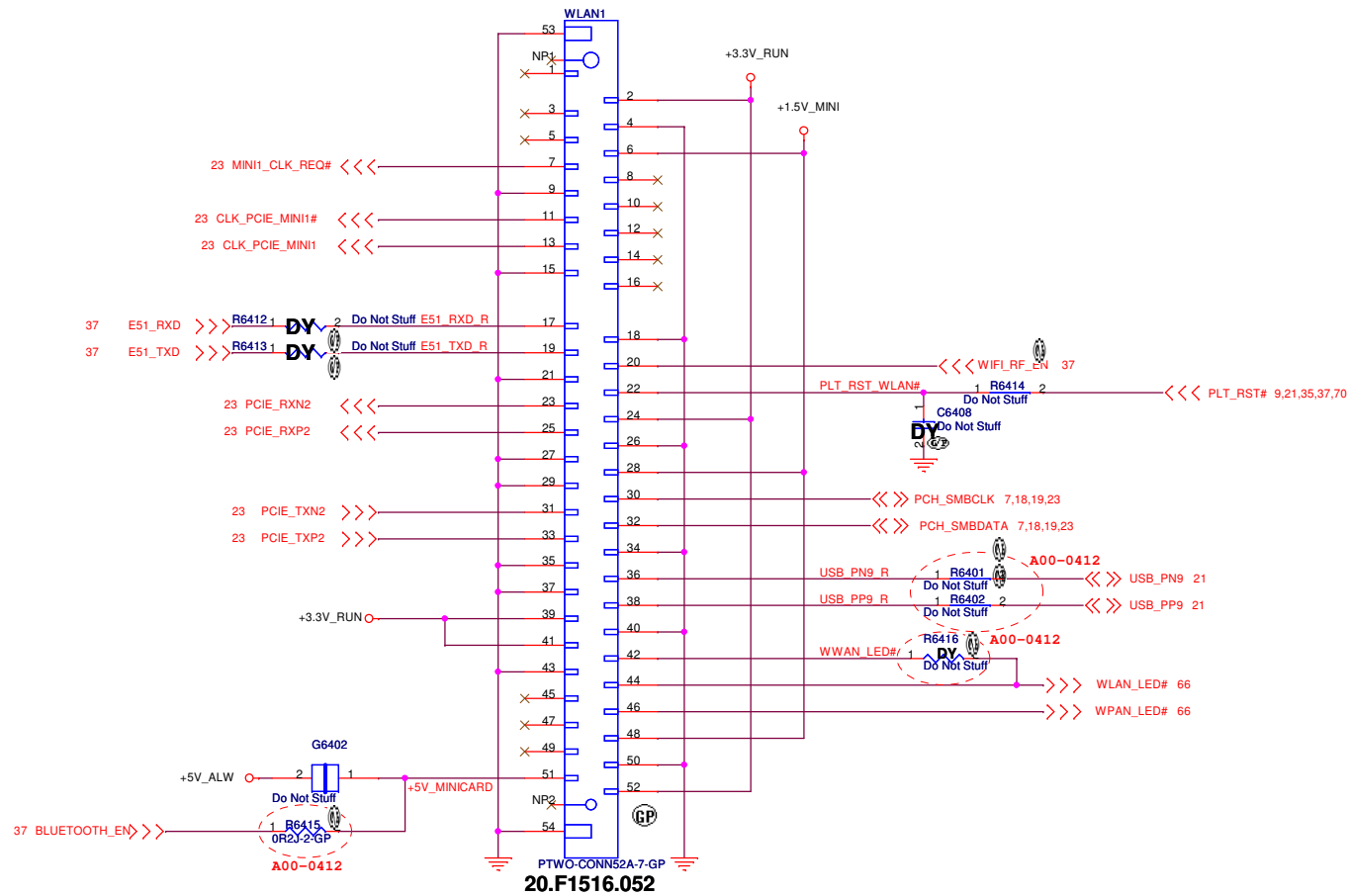
Title: **USB**

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SSID = Wireless

Mini Card Connector(802.11a/b/g)



DV15 CP UMA second

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Title: **MINICARD**

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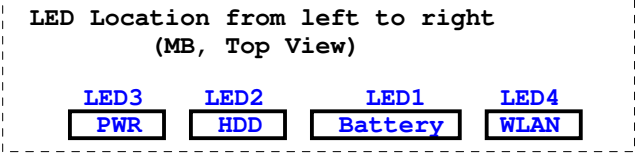
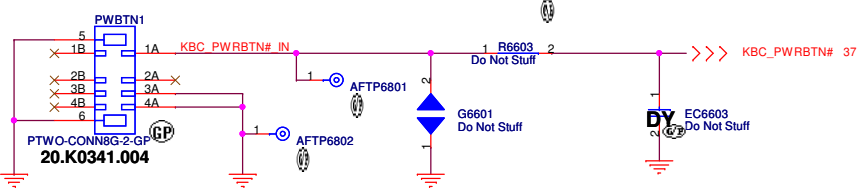
DV15 CP UMA second



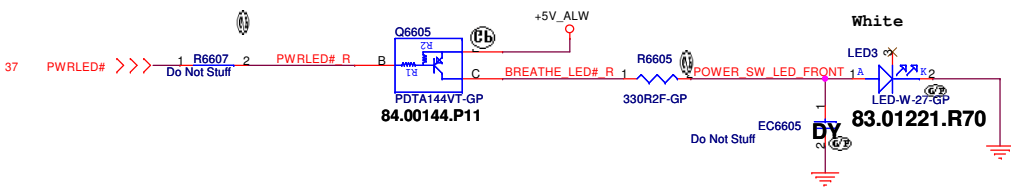
Title		
Reserved		
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SSID = User.Interface

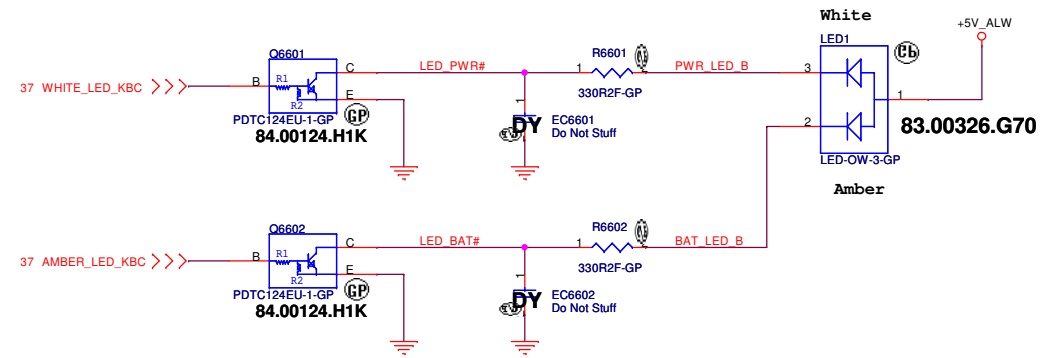
Power BTN Connector



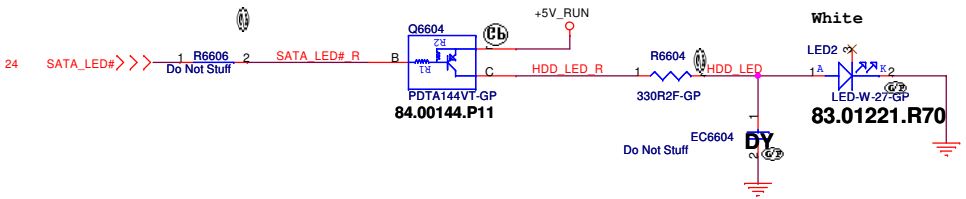
POWER LED



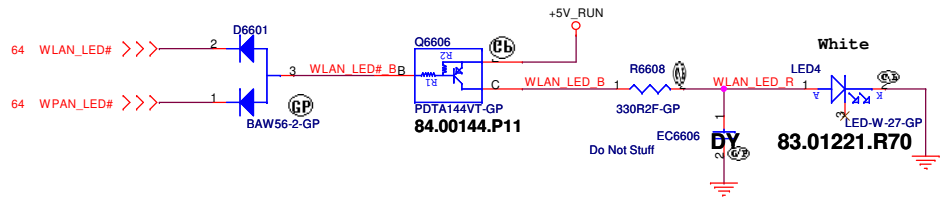
Battery LED



HDD LED



WLAN LED



DV15 CP UMA second

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED**

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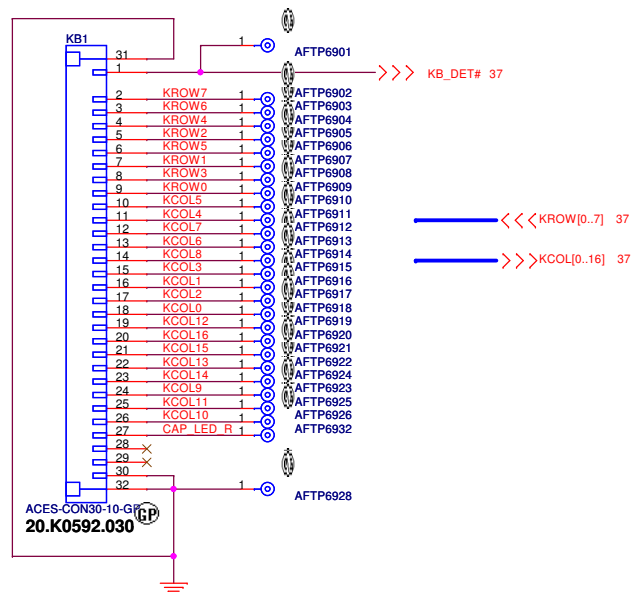
DV15 CP UMA second



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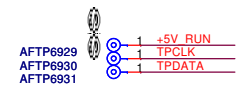
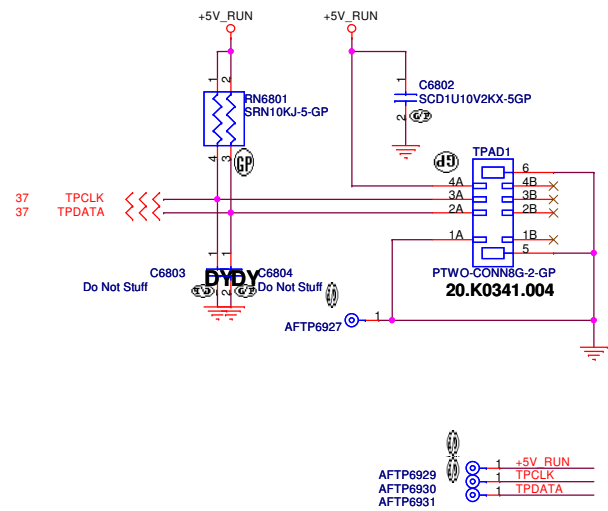
SSID = KBC

Internal KeyBoard Connector



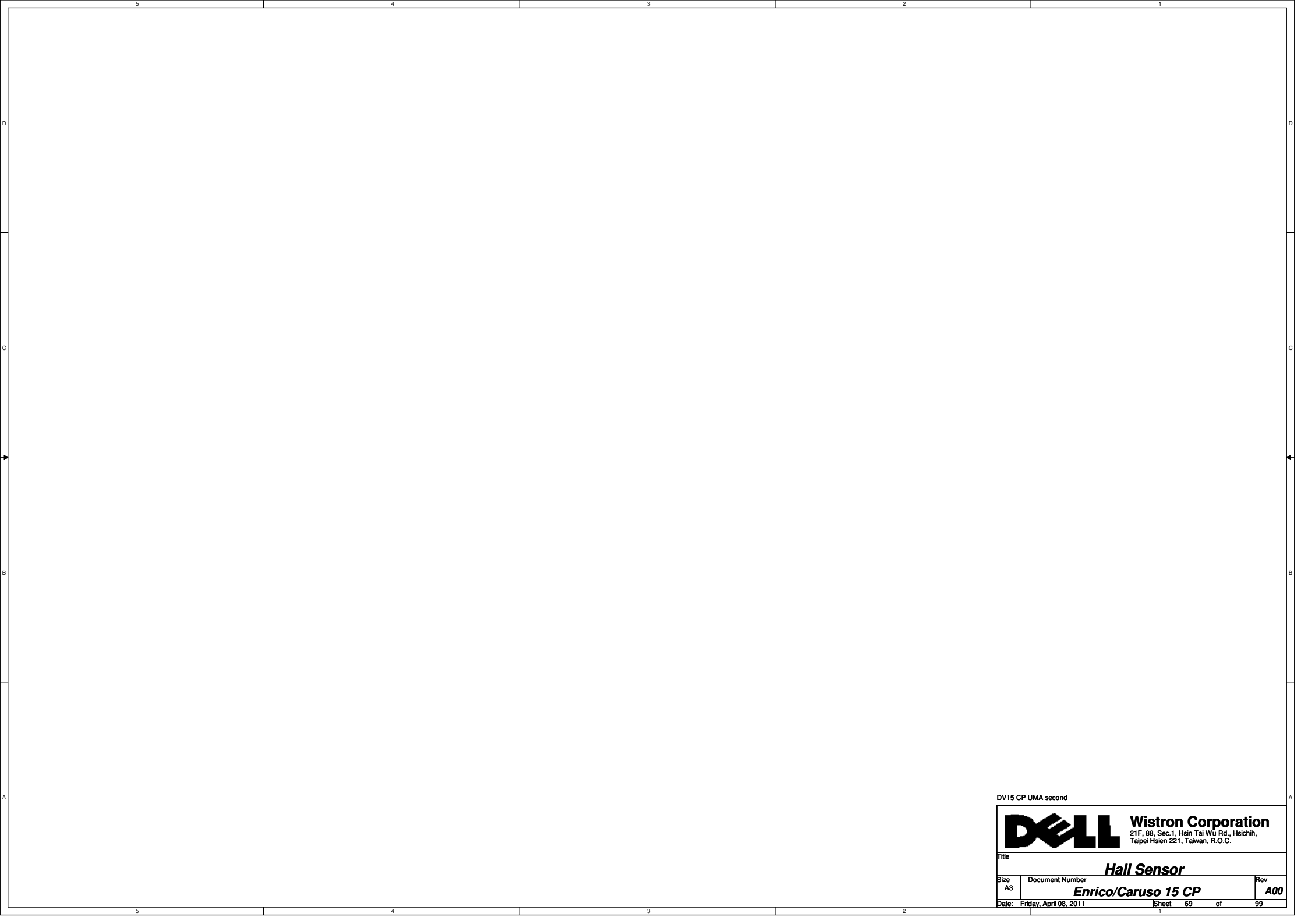
SSID = Touch.Pad

TouchPad Connector



DV15 CP UMA second

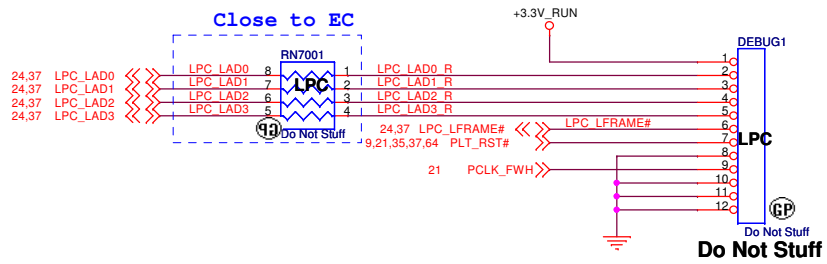
DELL		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Key Board/Touch Pad			
Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00	
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DV15 CP UMA second



Title		
Hall Sensor		
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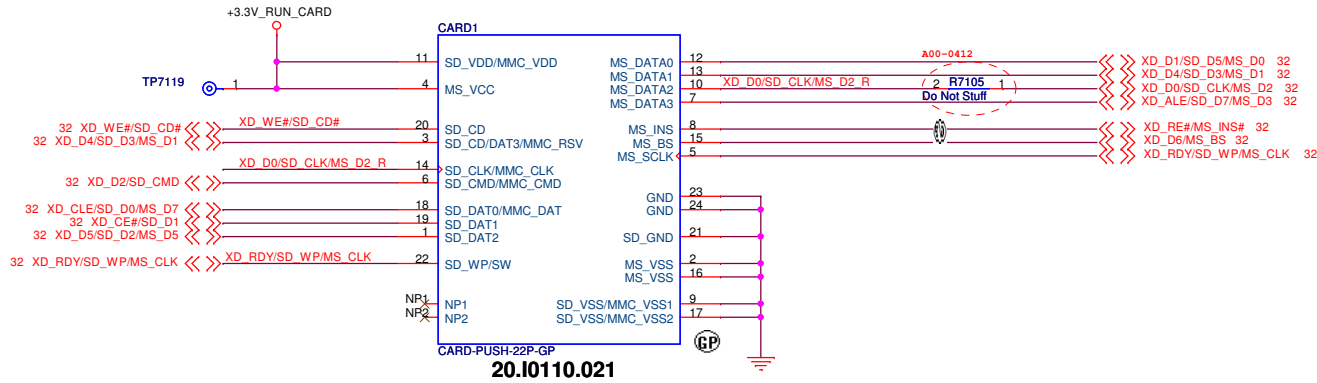
DV15 CP UMA second



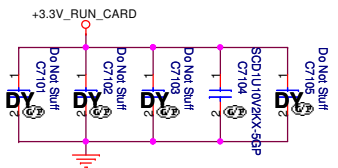
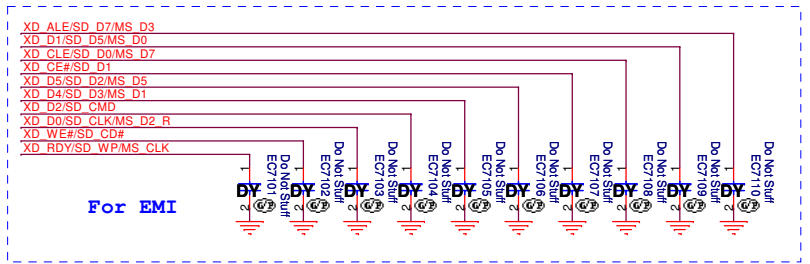
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SSID = SDIO

SD/XD/MS Card Reader



- TP7101 1 +3.3V_RUN_CARD
- TP7103 1 XD_RDY/SD_WP/MS_CLK
- TP7104 1 XD_RE#/MS_INS#
- TP7105 1 XD_CE#/SD_D1
- TP7106 1 XD_CE#/SD_D1
- TP7107 1 XD_ALE/SD_D7/MS_D3
- TP7108 1 XD_WE#/SD_CD#
- TP7110 1 XD_D0/SD_CLK/MS_D2_R
- TP7111 1 XD_D1/SD_D5/MS_D0
- TP7112 1 XD_D2/SD_CMD
- TP7114 1 XD_D4/SD_D3/MS_D1
- TP7115 1 XD_D5/SD_D2/MS_D5
- TP7116 1 XD_D6/MS_BS



DV15 CP UMA second

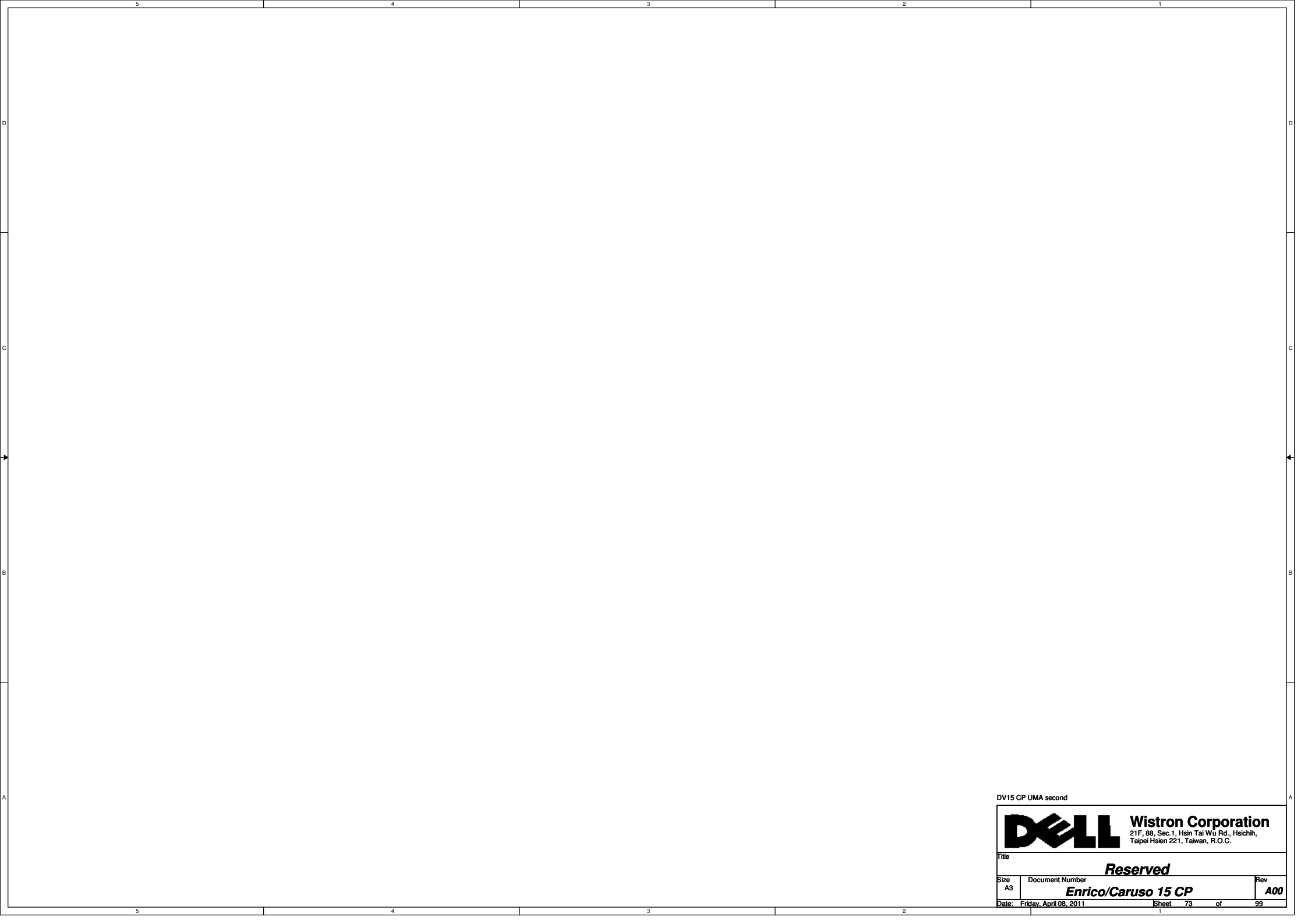


Title CARD Reader Connector		
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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RESERVED		
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DV15 CP UMA second

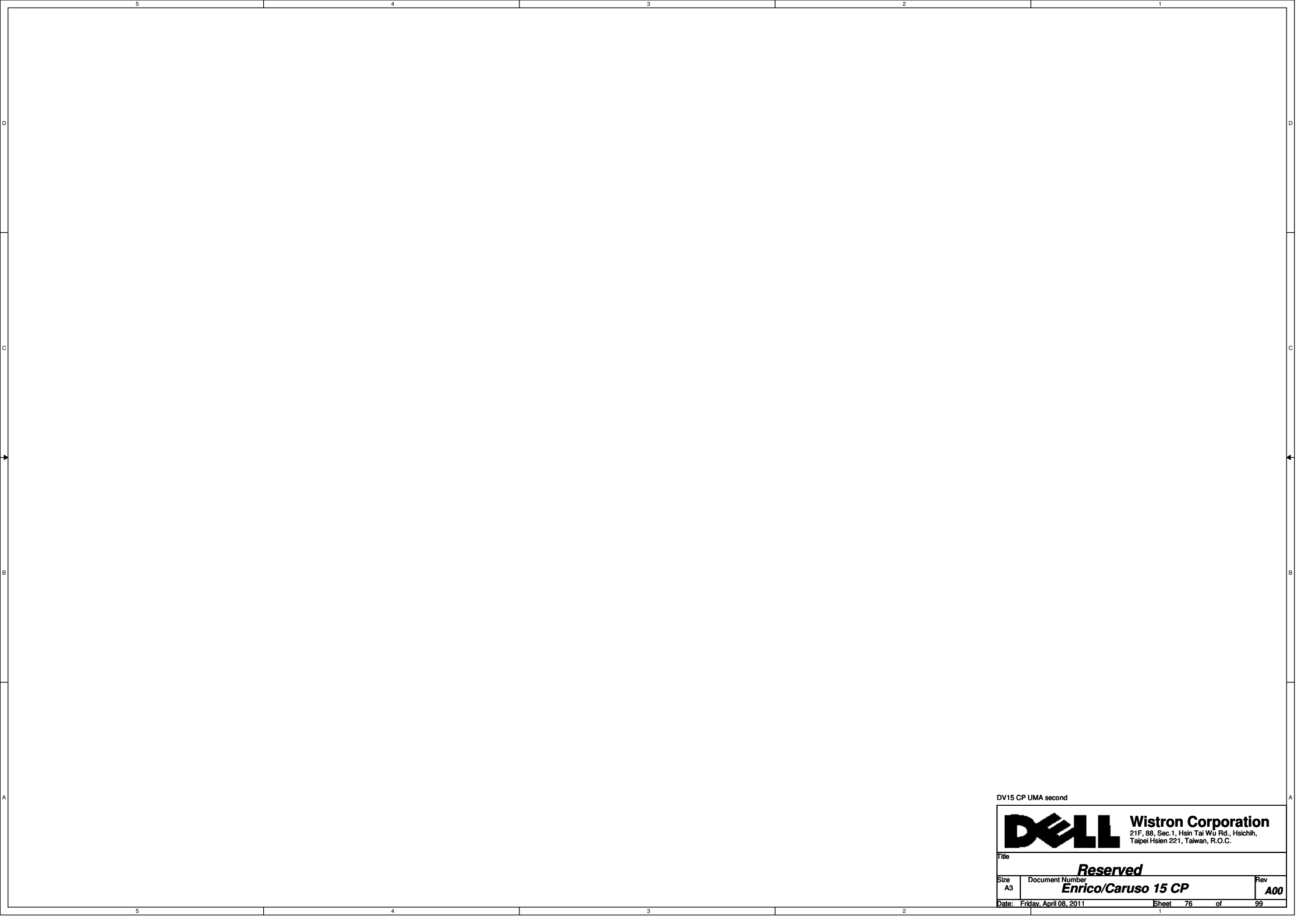


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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Reserved		
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DV15 CP UMA second



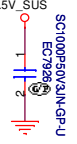
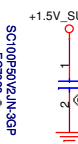
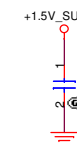
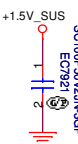
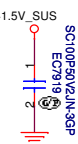
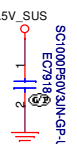
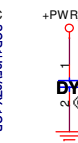
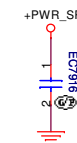
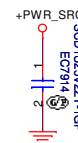
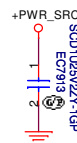
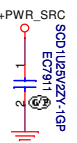
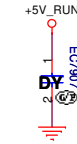
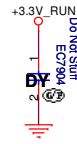
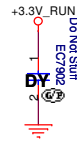
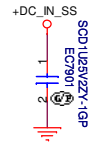
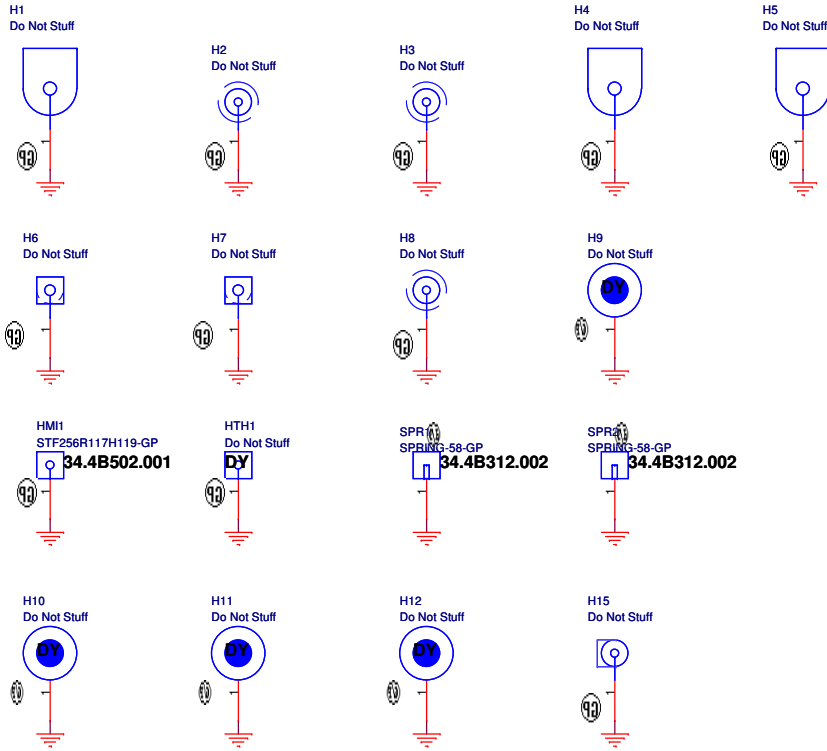
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SSID = VIDEO

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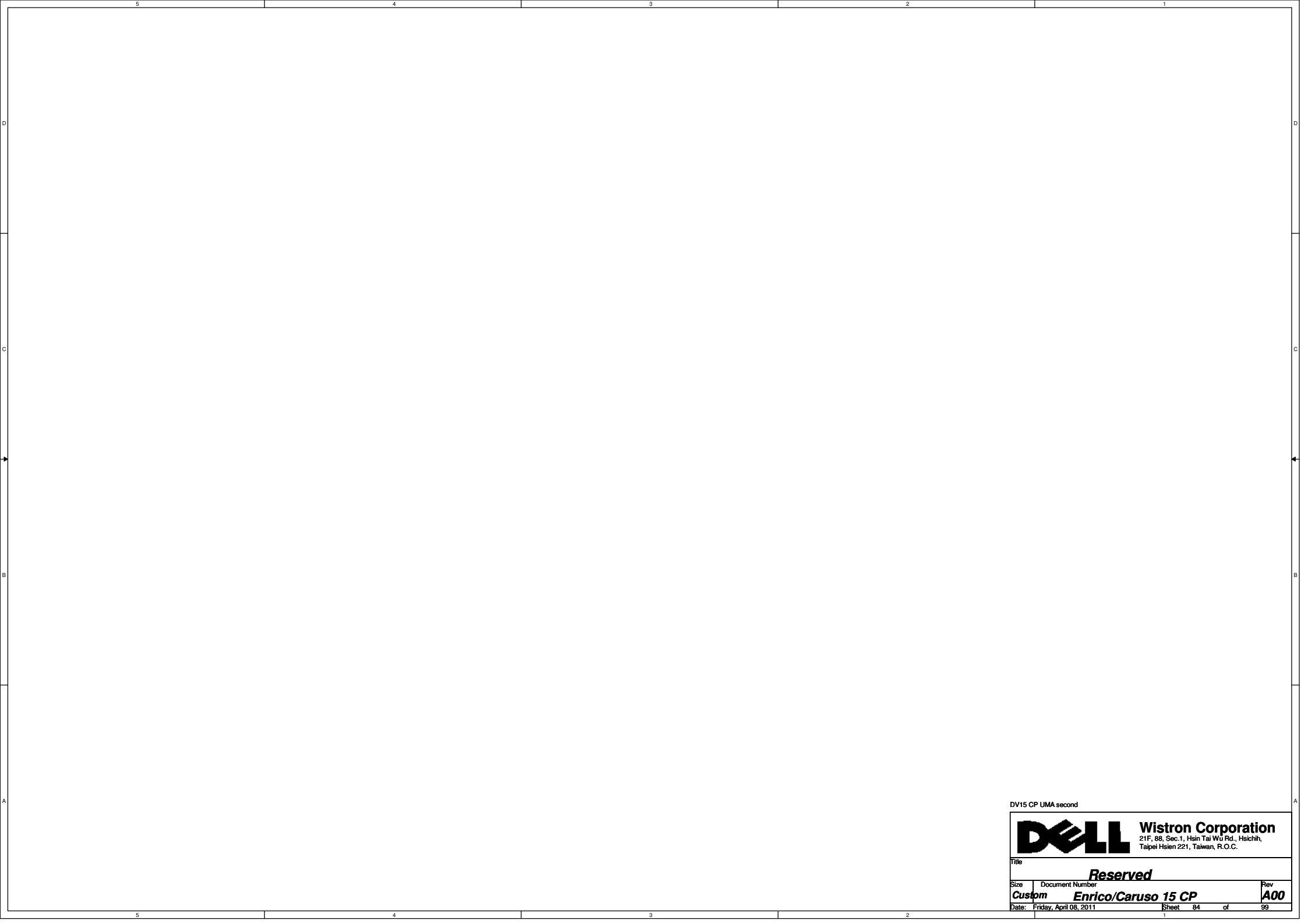
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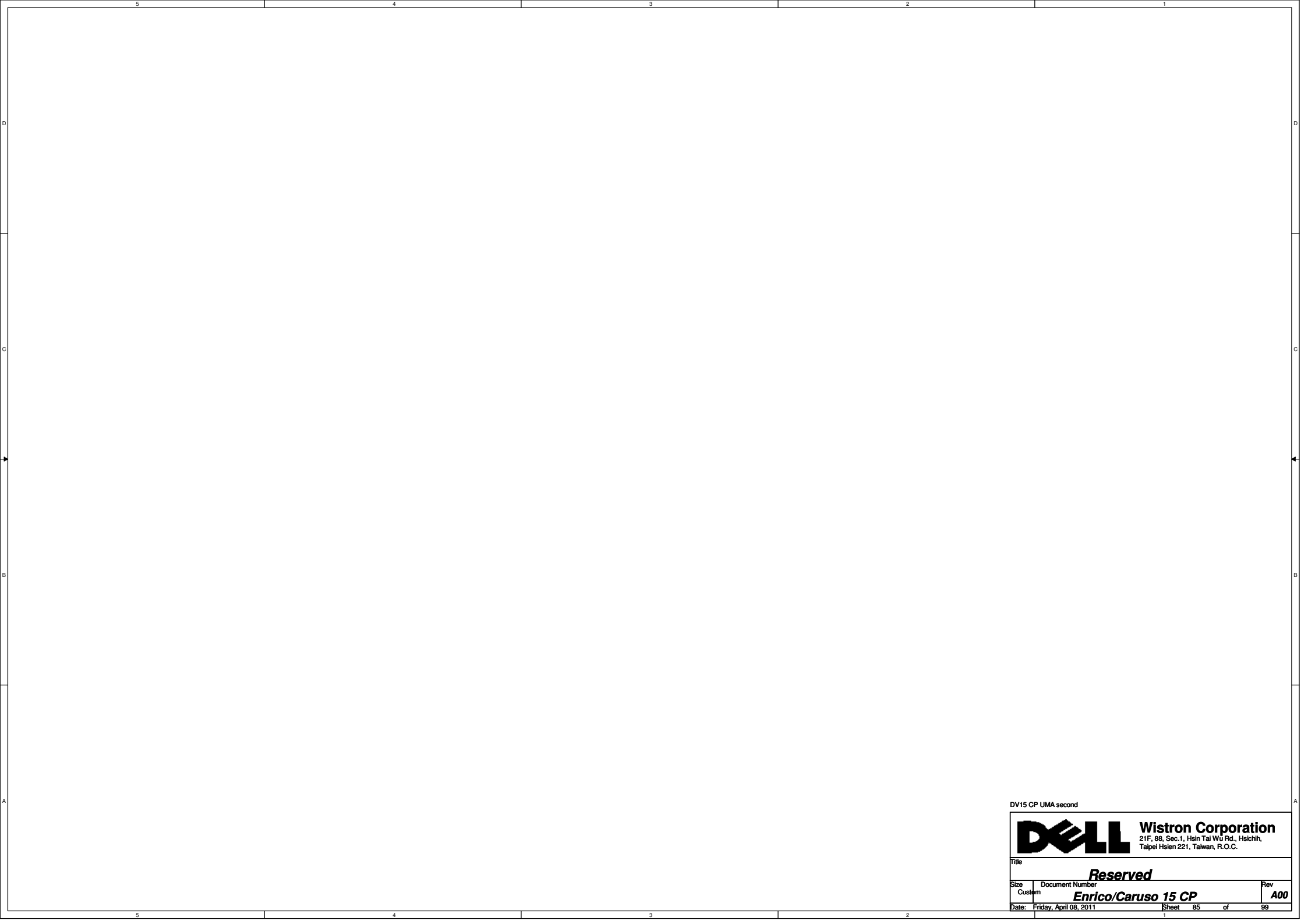
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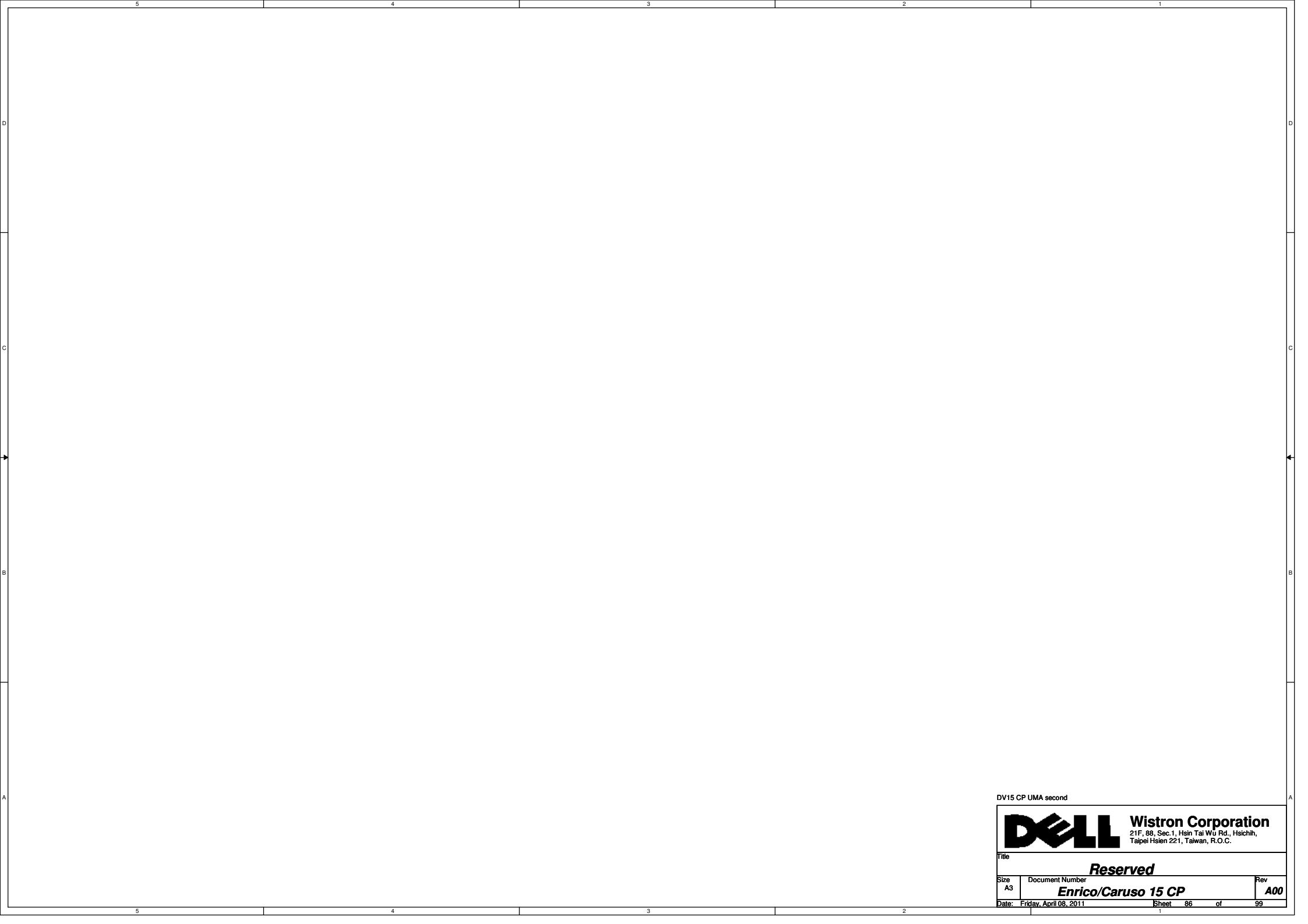
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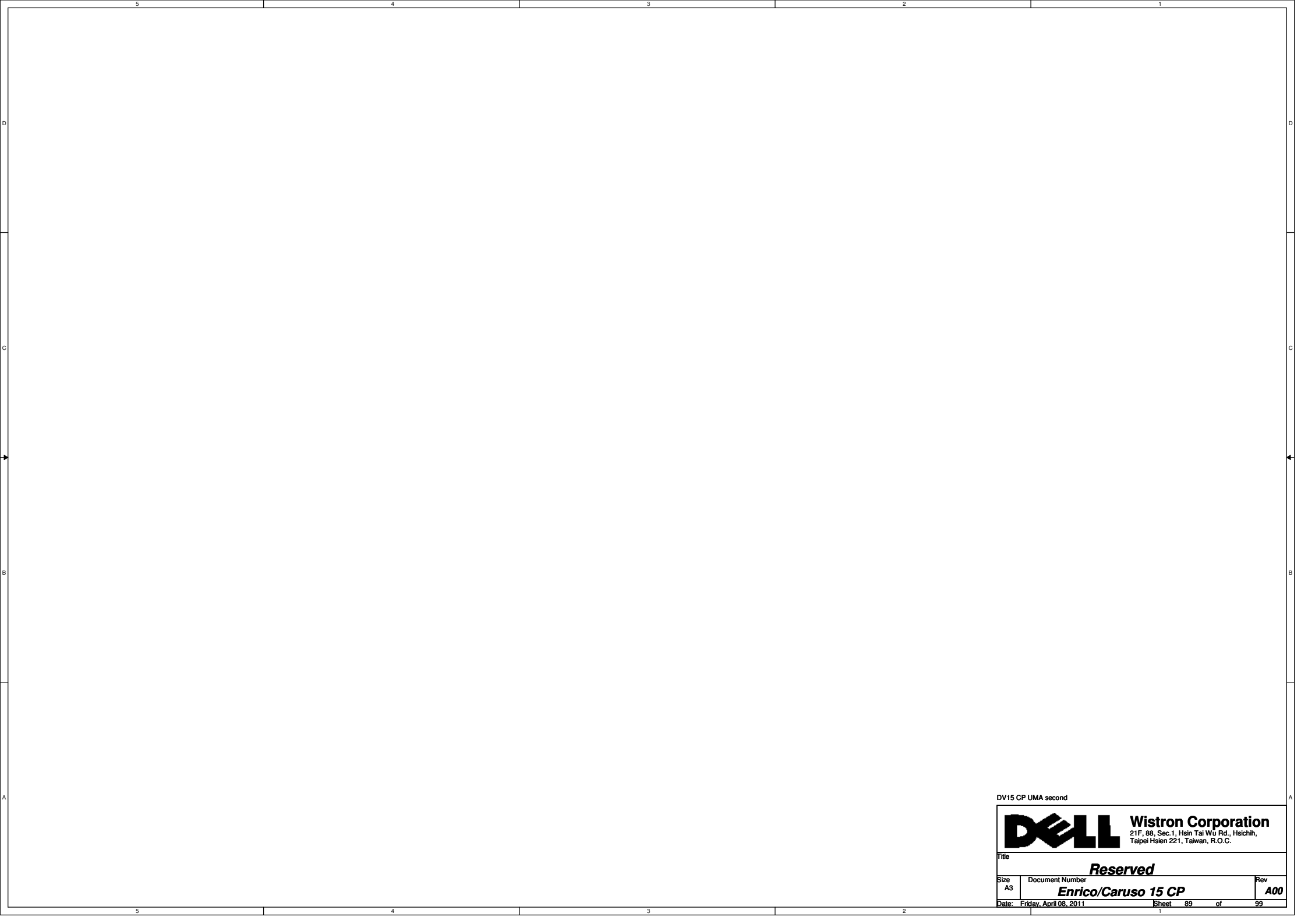
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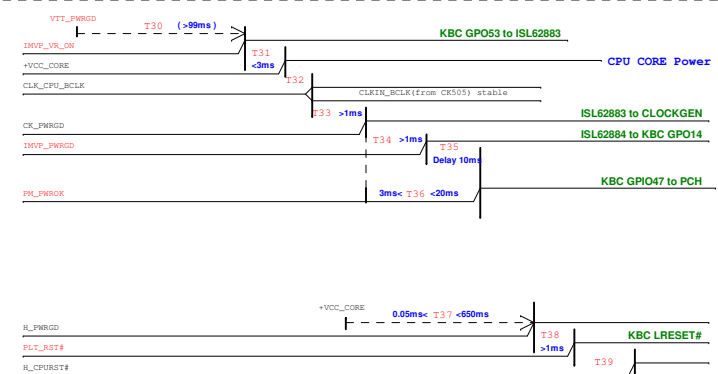
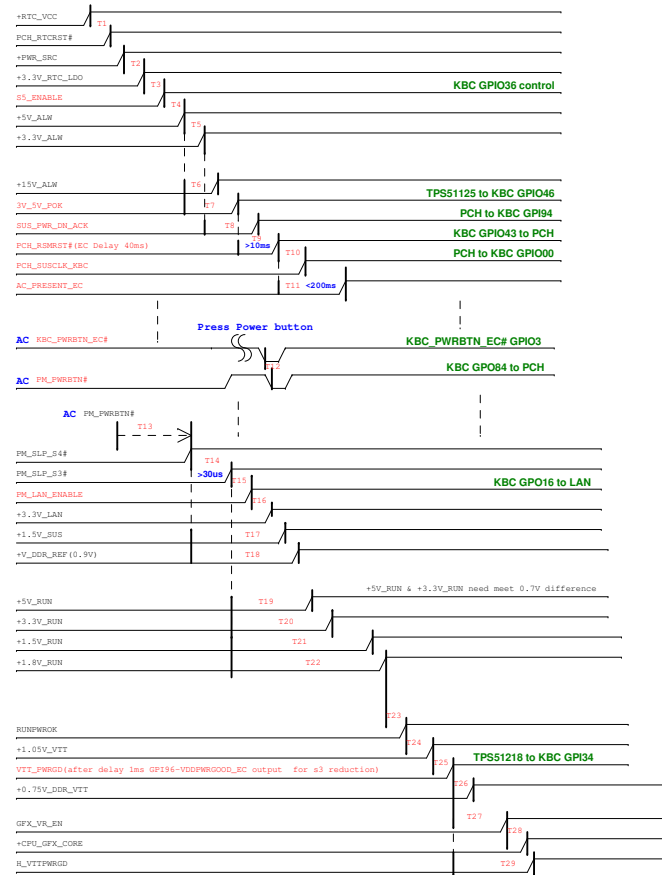


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DV15 Calpella UMA-Power Up Sequence

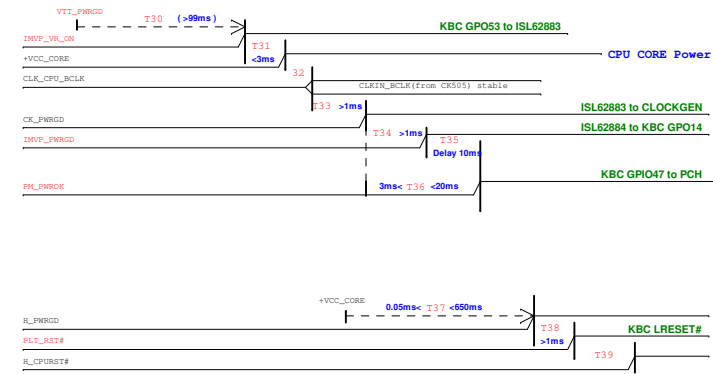
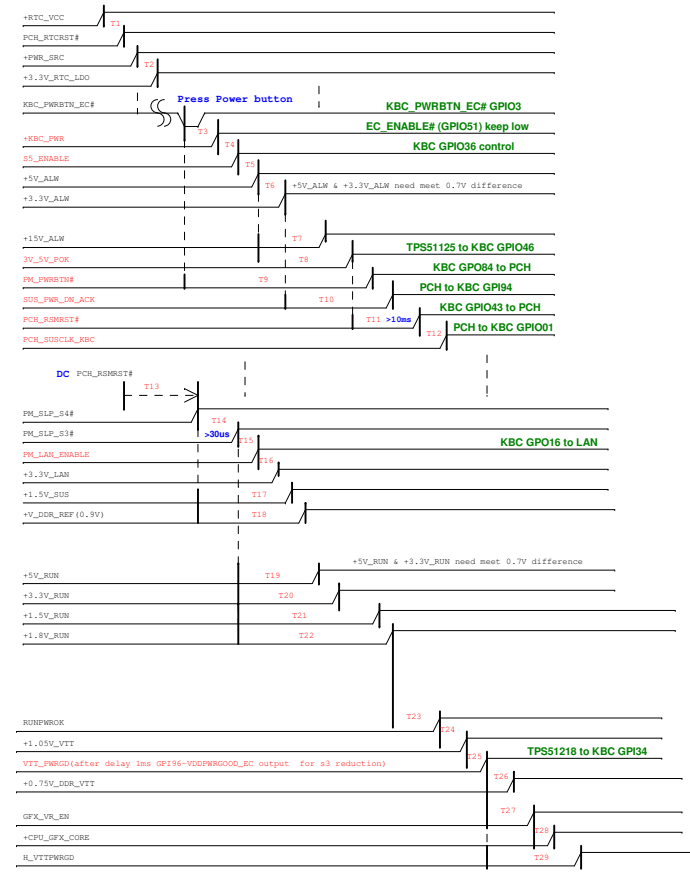
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO




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23F, 8F, 5th, 11th, 12th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st, 22nd, 23rd, 24th, 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, 41st, 42nd, 43rd, 44th, 45th, 46th, 47th, 48th, 49th, 50th, 51st, 52nd, 53rd, 54th, 55th, 56th, 57th, 58th, 59th, 60th, 61st, 62nd, 63rd, 64th, 65th, 66th, 67th, 68th, 69th, 70th, 71st, 72nd, 73rd, 74th, 75th, 76th, 77th, 78th, 79th, 80th, 81st, 82nd, 83rd, 84th, 85th, 86th, 87th, 88th, 89th, 90th, 91st, 92nd, 93rd, 94th, 95th, 96th, 97th, 98th, 99th, 100th

Item	Pg.	Date	Description	Owner
KBC	37	A00-0412	stuff R3722 and DY R3725 for change MB version from X02 to A00	EE
WLAN	64	A00-0412	change R6415 from short pad to 0 ohm for debug	EE
USB	54, 63	A00-0412	Remove colay pad(R5403,R5404,R6315,R6316,R6317,R6318,R6319,R6320) after A00	EMI
USB	32, 64	A00-0412	Remove colay pad(EL3201,EL6401) and short pad(R3204,R3205,R6401,R6402) after A00	EMI
CLK GEN	7	A00-0412	change R710~R717 from 0 ohm to short pad	EMI
HDMI	57	A00-0412	Remove colay pad(EL5701,EL5702,EL5703,EL5704) after A00	EMI
short pad	ALL	A00-0412	change PR4519,PR5006,PR5111,R3202,R3742,R3743,R3744,R7105 from 0 ohm to short pad	EE
RTC	62	A00-0412	change U6203 P/N to 83.R0304.B81 for RTC detect leakage issue	EE
RT8237A_+1.05V	49	A00-0412	update PU4901 symbol for part manager footprint change	POWER
WLAN	64	A00-0412	add and DY R6416 0 ohm for Wimax future	EE
POWER GAP	ALL	A00-0413	change power GAP (PG4511,PG4602,PG4604,PG4605,PG4606,PG4615,PG4617,PG4619,PG4621,PG4624,PG4625,PG4607,PG4608,PG4609,PG4622,PG4626,PG4627,PG4610,PG4611,PG4612,PG4613,PG4614,PG4616,PG4618,PG4620,PG4902,PG4903,PG4904,PG4905,PG4906,PG4908,PG4910,PG4911,PG4913,PG4915,PG4917,PG4919,PG4925,PG4926,PG4920,PG4927,PG4928,PG4929,PG4909,PG4901,PG4912,PG4914,PG4916,PG4918,PG5001,PG5012,PG5002,PG5003,PG5004,PG5008,PG5009,PG5010,PG5011,PG5013,PG5015,PG5016,PG5017,PG5104,PG5106,PG5301,PG5303,PG5305,PG5308,PG5311) P/N from ZZ.CON2d.XXX to ZZ.CLOSE.001 for PSE requests	POWER
Thermal	39	A00-0422	stuff R3904 to change T8 temperature setting for reliability test	EE

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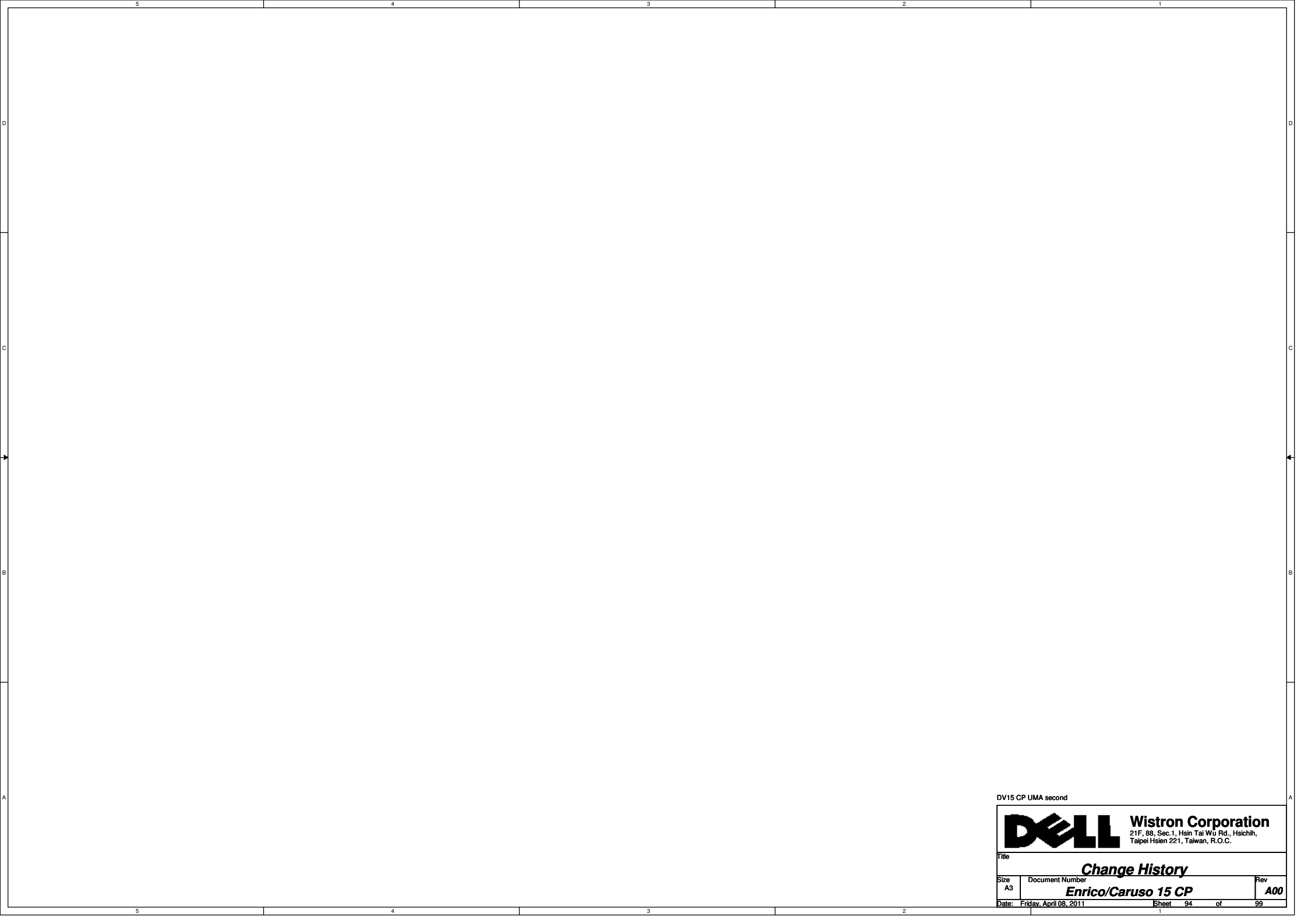
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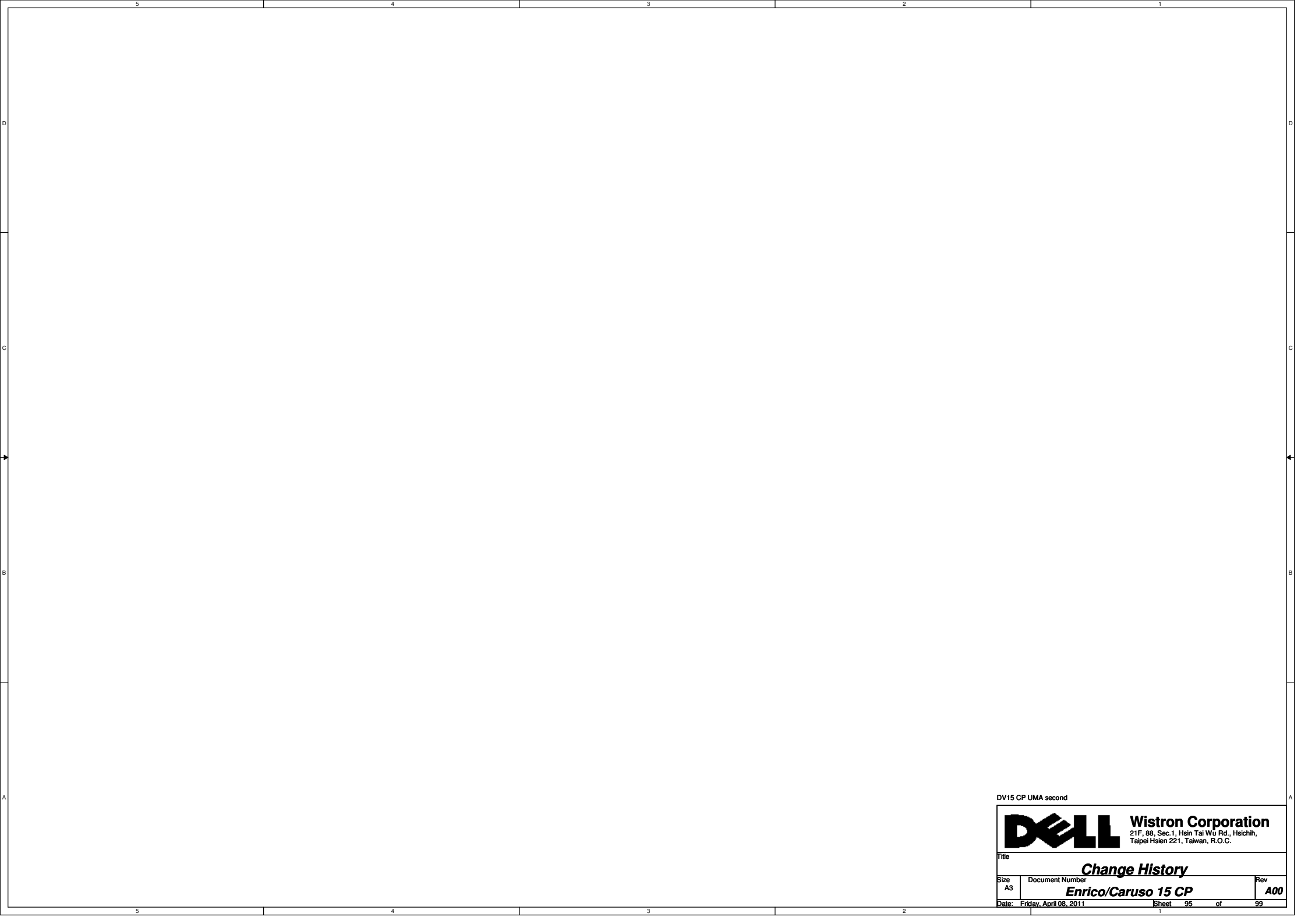
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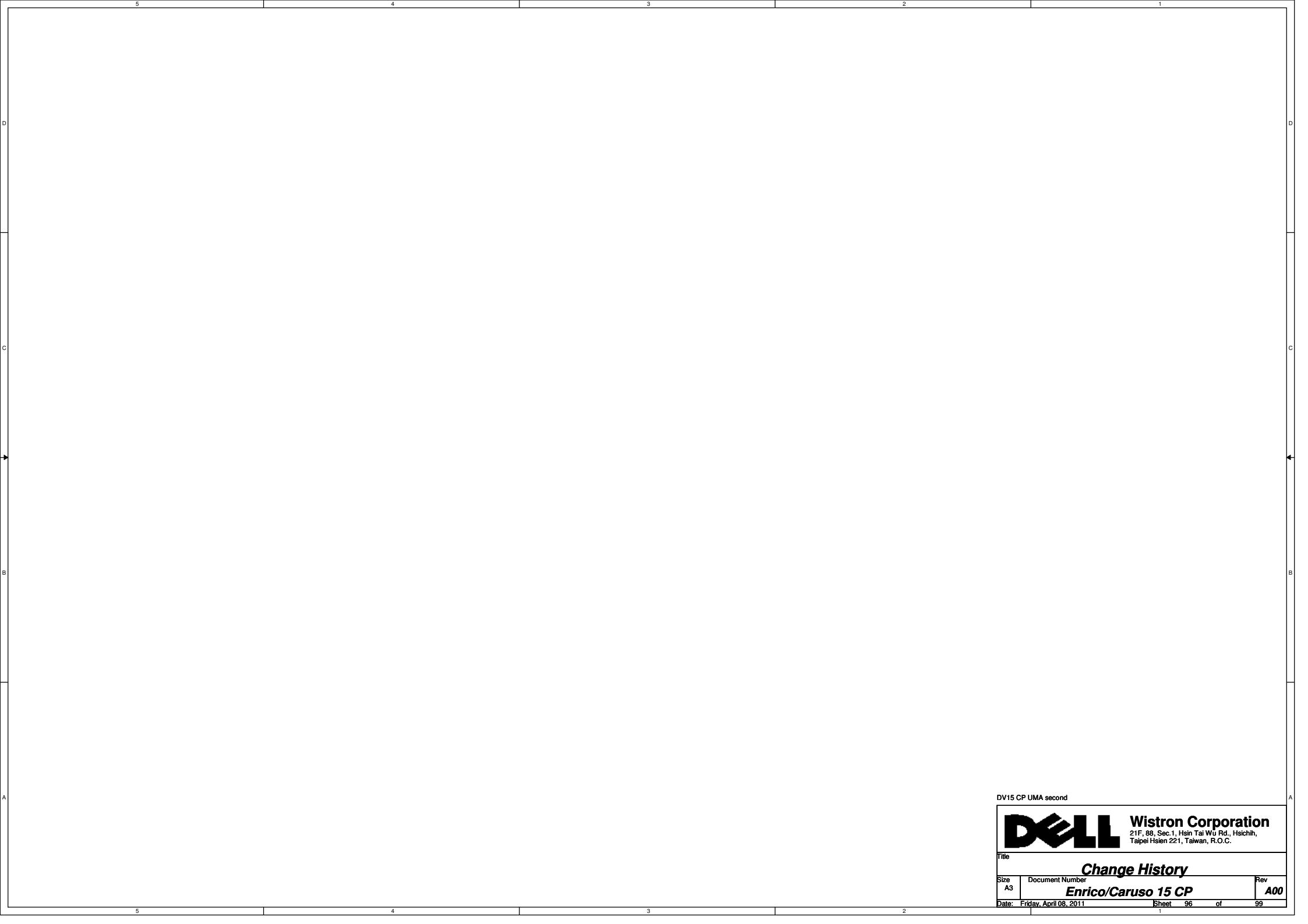
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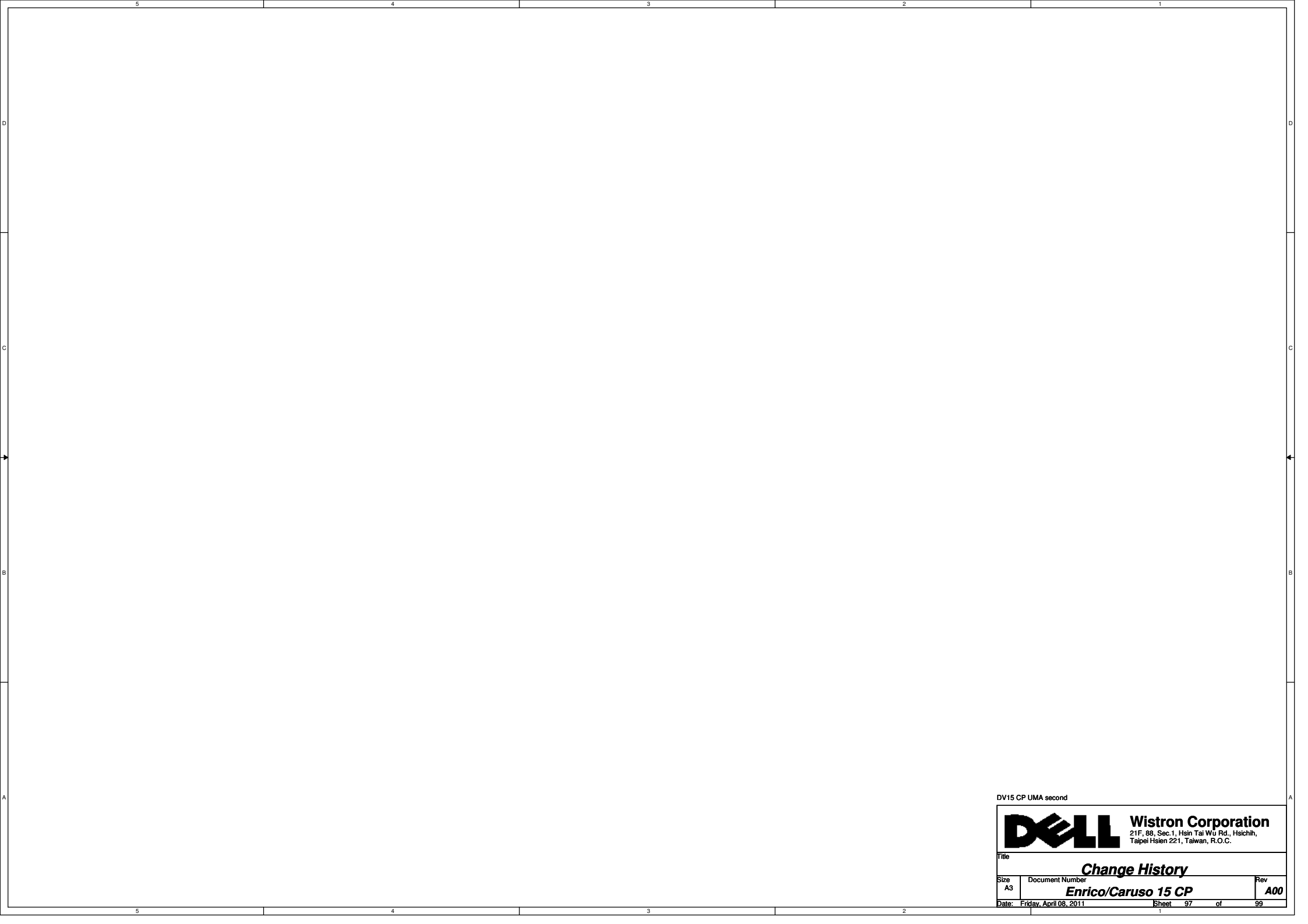
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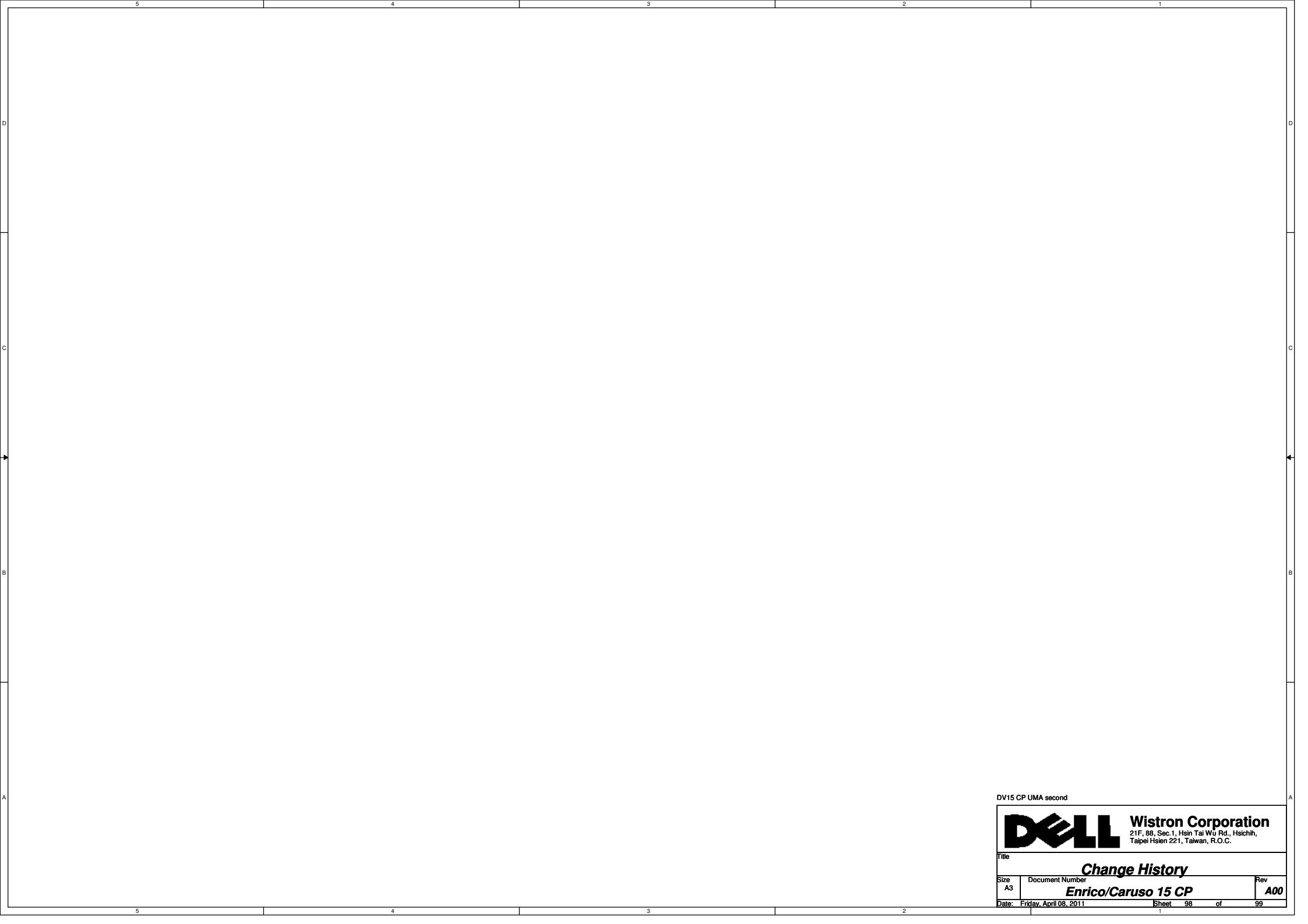
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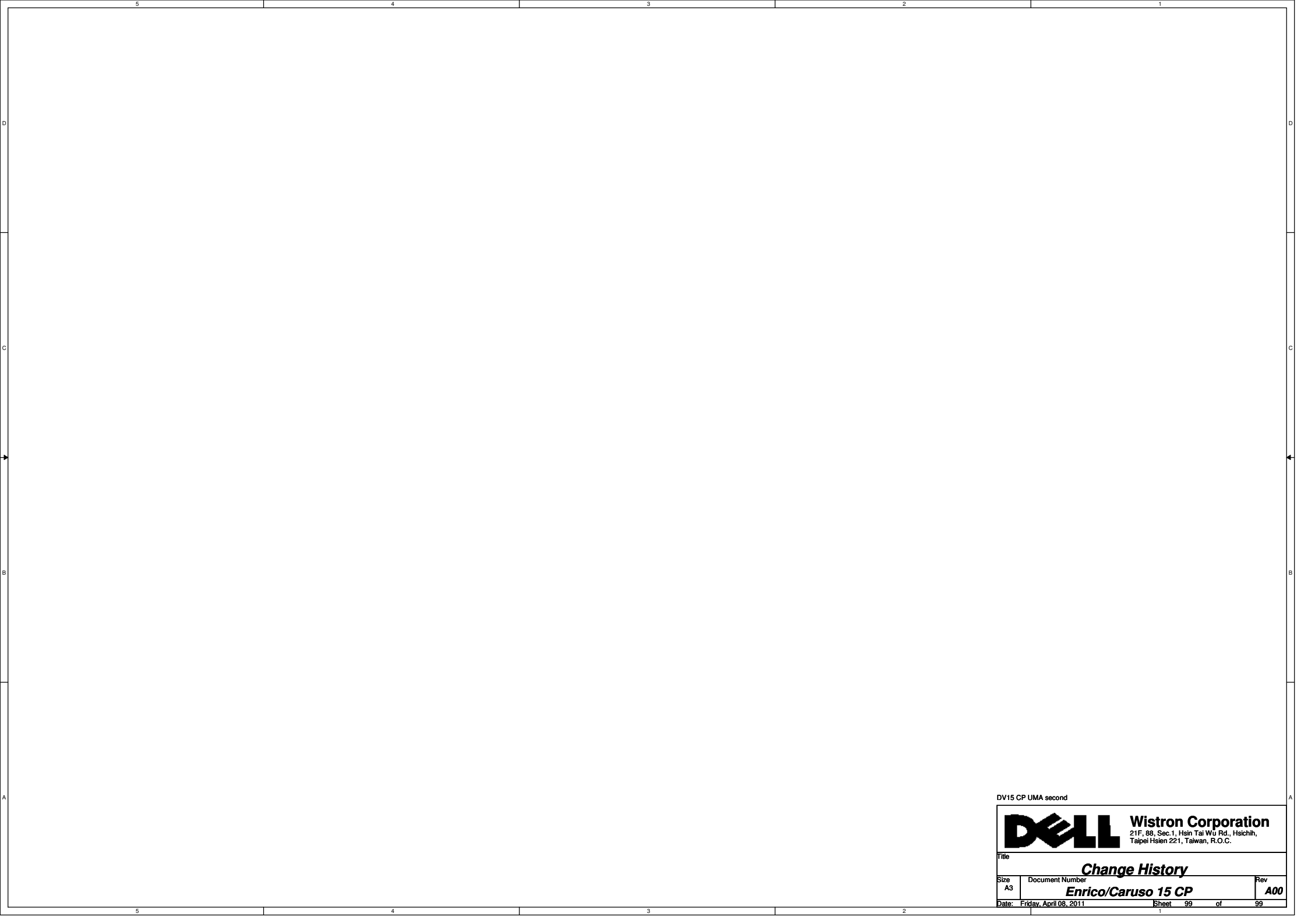
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