

# EA30\_BM

## Schematics Document

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**Cover Page**

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Document Number

**EA30 BM**

Rev

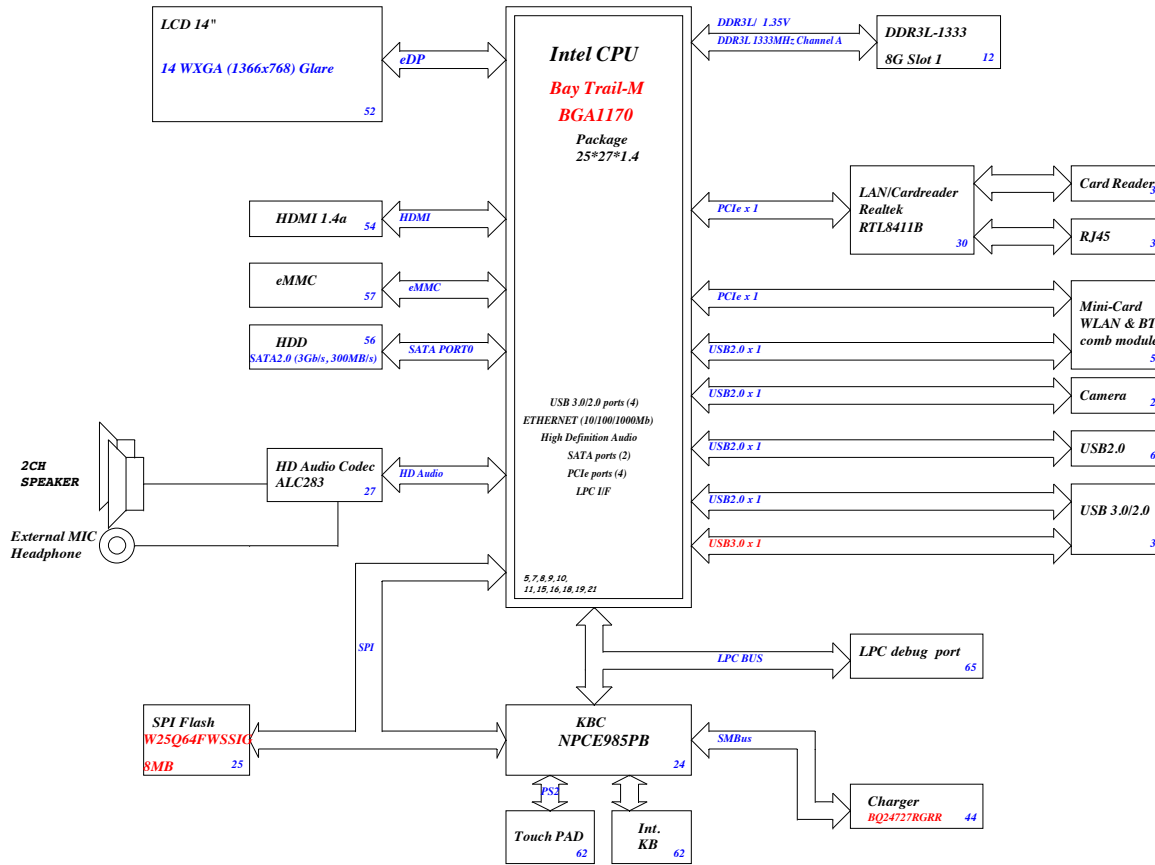
**-1**

Date: Tuesday, July 08, 2014

Sheet 1 of 102

# EA30\_BM Board Block Diagram

Project code :  
PCB P/N : 14221  
Revision : SB



<b>CHARGER</b>	
BQ24727	44
INPUTS	OUTPUTS
DCBATOUT	BT+
<b>SYSTEM DC/DC</b>	
TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_S5
	3D3V_S5
<b>CPU DC/DC</b>	
ISL95833 46-47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
<b>SYSTEM DC/DC</b>	
SY8208 50	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
<b>SYSTEM DC/DC</b>	
SY8208DQNC 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
<b>SYSTEM LDO</b>	
TLV70218 51	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
<b>SYSTEM LDO</b>	
S-1339D15 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
<b>SYSTEM LDO</b>	
TLV70012 51	
INPUTS	OUTPUTS
3D3V_S5	1D2V_S5
<b>Step Down Regulator</b>	
SYW232 51	
INPUTS	OUTPUTS
1D0V_S0_P6	1D05V_S0
<b>GPU Core</b>	
RT8812 82	
INPUTS	OUTPUTS
DCBATOUT	V6A_CORE
<b>LOAD SWITCH</b>	
TPS22966 37	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
<b>LOAD SWITCH</b>	
TPS22965 37	
INPUTS	OUTPUTS
1D0V_S5	1D0V_S0
<b>SYSTEM DC/DC</b>	
SY8208 83	
INPUTS	OUTPUTS
DCBATOUT	1D5V_V6A_S0
<b>LOAD SWITCH</b>	
TPS22966 83	
INPUTS	OUTPUTS
1D05V_S0	1D5V_V6A_S1
3D3V_S0	3D3V_V6A_S0

## PCB LAYER

L1:Top L4:Signal  
L2:VCC L5:GND  
L3:Signal L6:Bottom

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D

C

B

A

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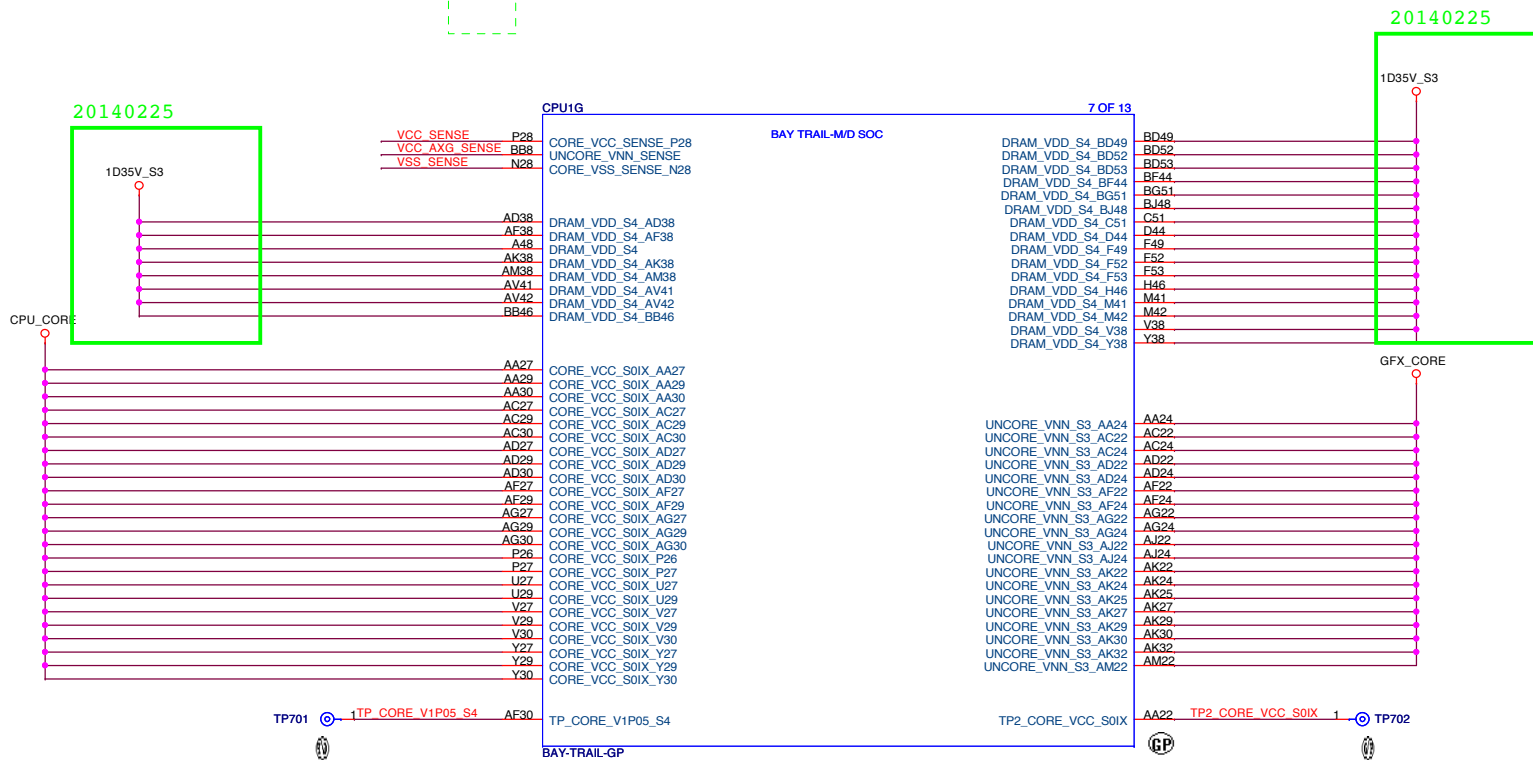
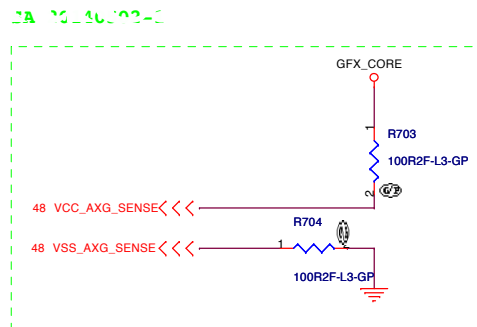
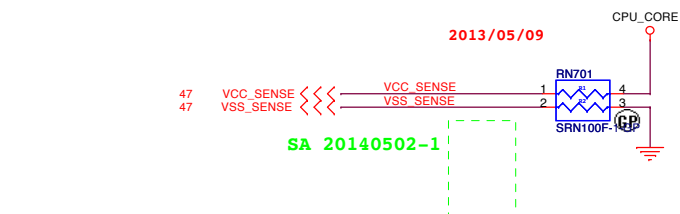
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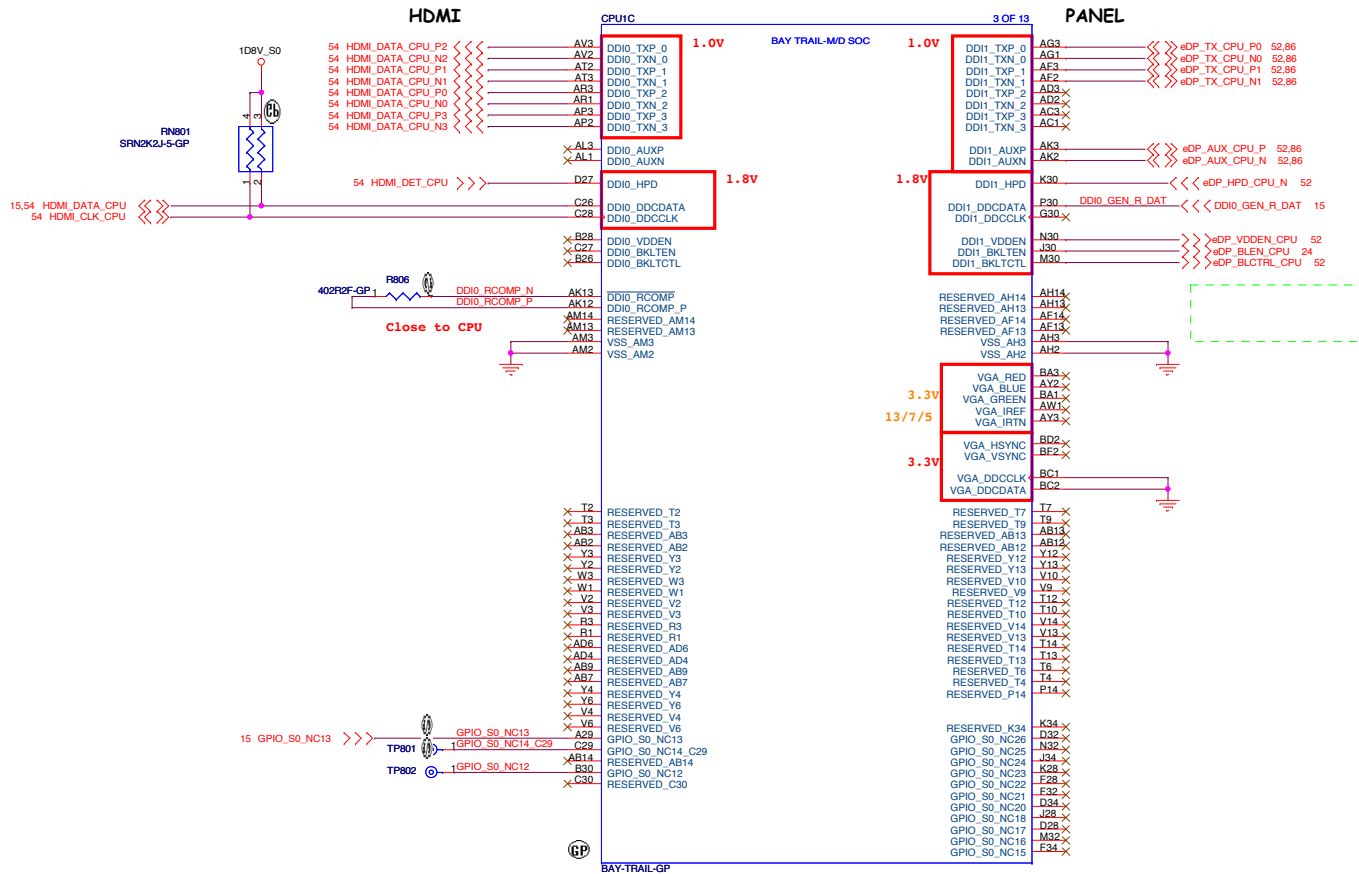
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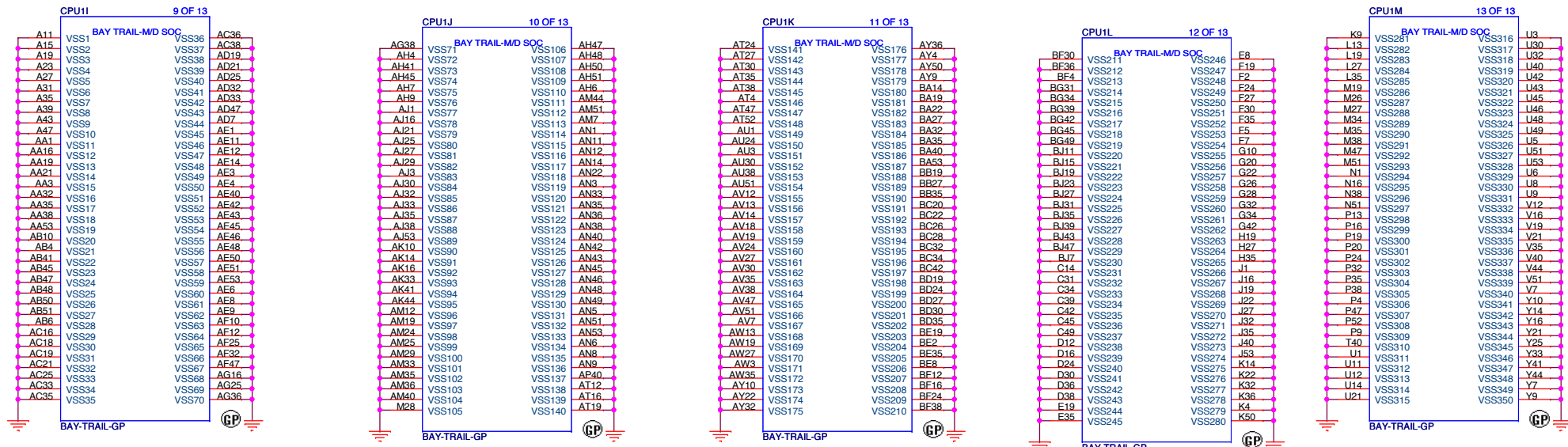
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Title CPU (DD/VE/DP/GPIO)

Size Custom Document Number EA30 BM Rev -1

Date: 108809, July 06, 2014 Sheet 8 of 102

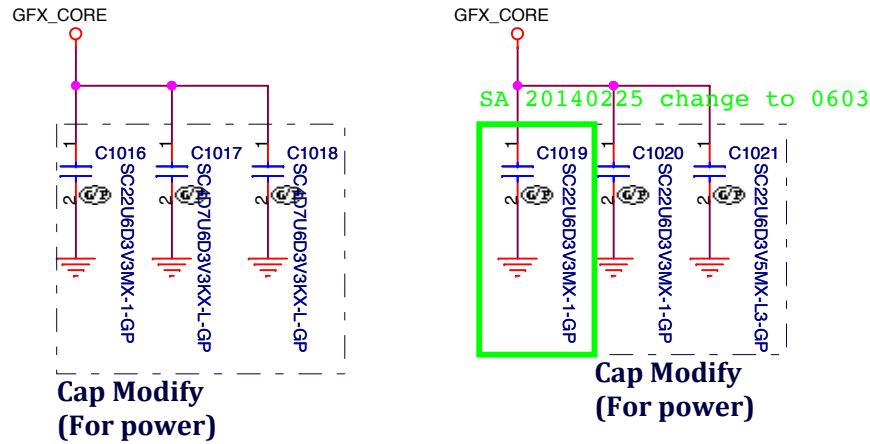
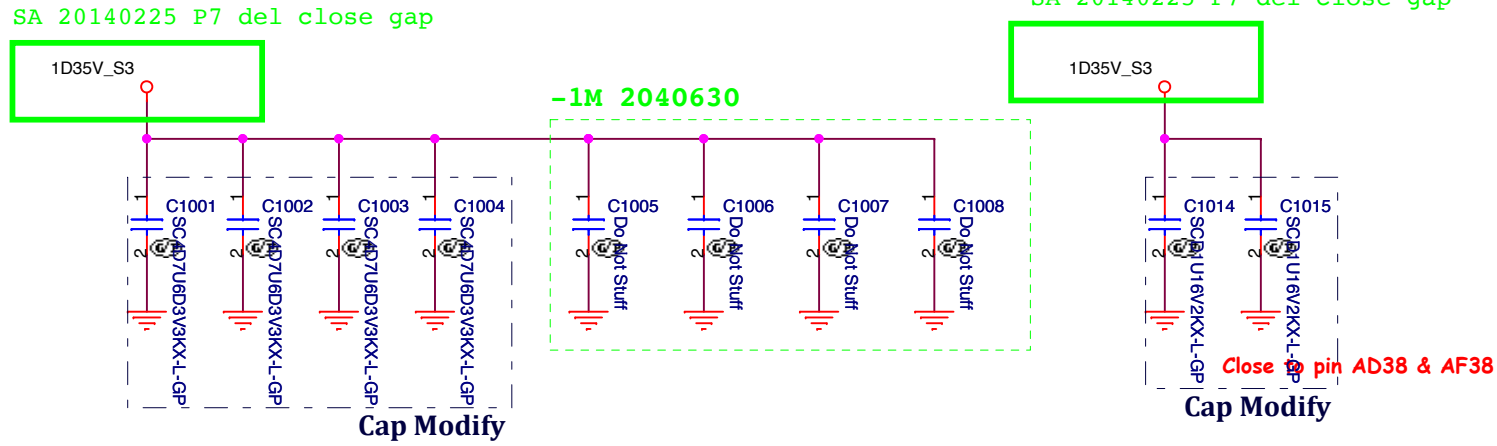
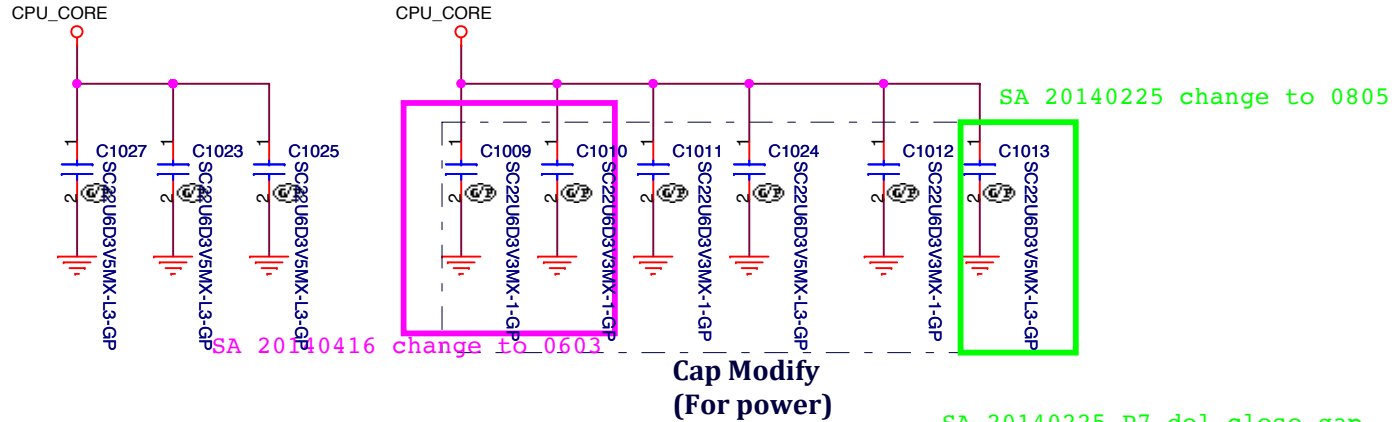


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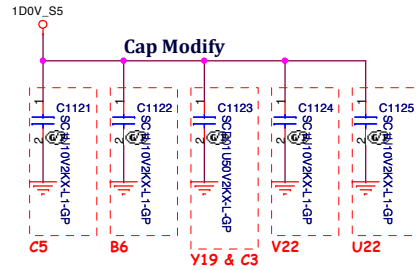
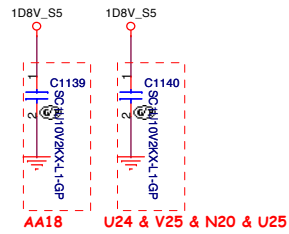
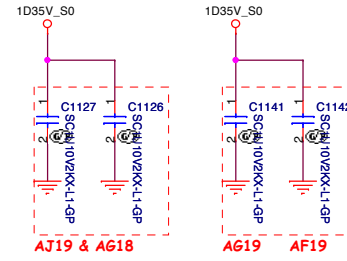
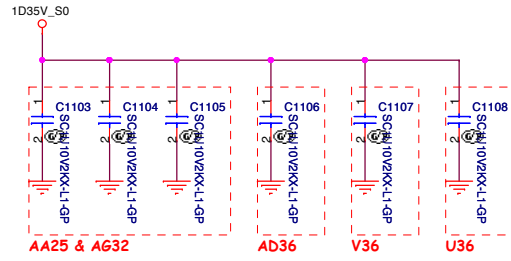
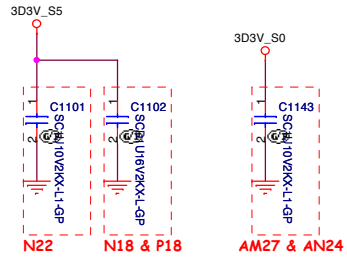
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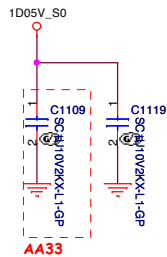
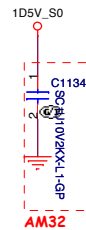
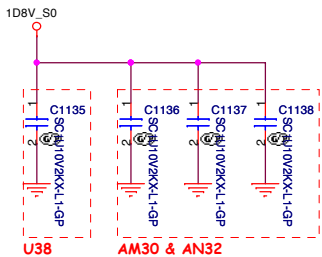
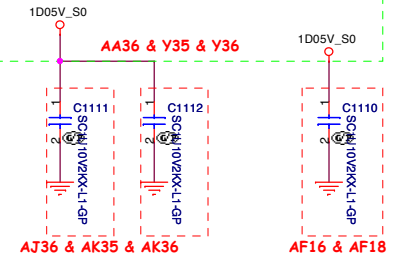
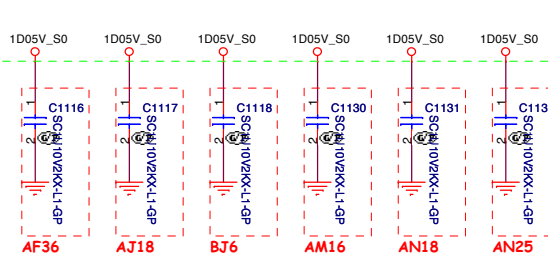
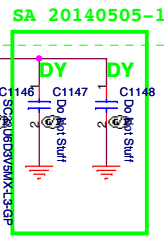
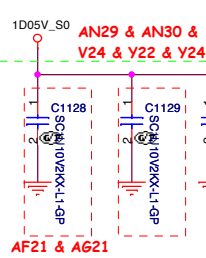
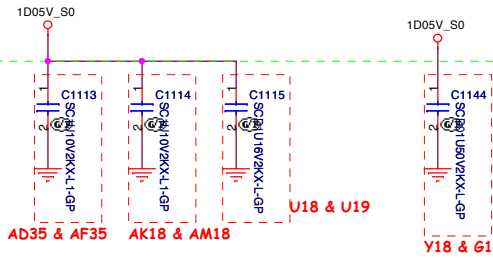
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Title <b>CPU (Power CAP1)</b>		
Size A4	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 10 of	102

# Cap Modify



SA 20140418



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CPU (Power CAP2)		
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A3	EA30 BM	-1
Date:	Tuesday, July 08, 2014	Sheet 11 of 102



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<b>DDR3-SODIMM2</b>		
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Sheet 13 of		102

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Size  
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Document Number

**EA30 BM**

Rev  
**-1**

Date: Tuesday, July 08, 2014

Sheet 14 of 102

# SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED OUTSIDE OF COZ AREA  
SHOULD BE PLACED OUTSIDE KOZ AREA

SA 20140222

Description	BIOS Boot Selection	Security Flash Descriptors	DDI1 Detect	DDI0 Detect	DDI1 Detect	Top swap
<b>GPIO</b>	<b>GPIO_S0_SC[063]</b>	<b>GPIO_S0_SC[065]</b>	<b>DDI1_DDCDATA</b>	<b>DDI0_DDCDATA</b>	<b>MDSI_DDCDATA</b>	<b>GPIO_S0_SC [56]</b>
<b>Schematic</b>						
<b>High</b>	SPI	Normal Operation	RN801 PH DDI1 detected	DDI0 detected	DDI1 detected	
<b>Low</b>	LPC	Override	DDI1 not detected	DDI0 not detected	DDI1 not detected	

## 2.25 Hardware Straps

All straps are sampled on the rising edge of PMC\_CORE\_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

## 30.2 LPE\_I2S2\_DATAOUT/ GPIO\_S0\_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO\_S0\_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

### 27.1.1.2 Hardware Controlled

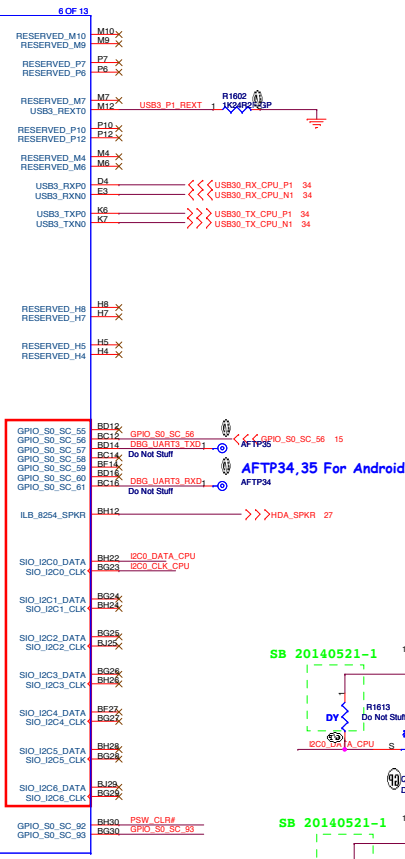
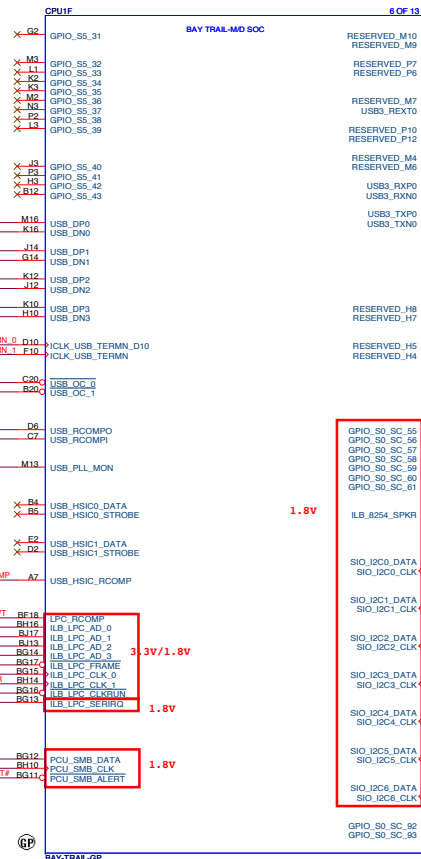
System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.

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### USB Table

Pair	Device
0	USB3.0 Port 0(USB2.0)
1	USB 2.0 (debug port)
2	Wifi + BT
3	Camera



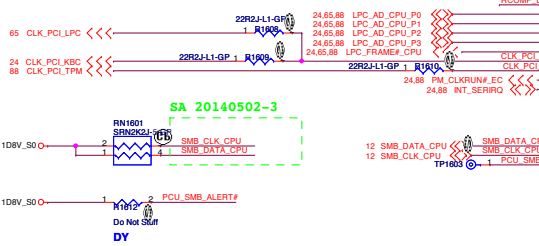
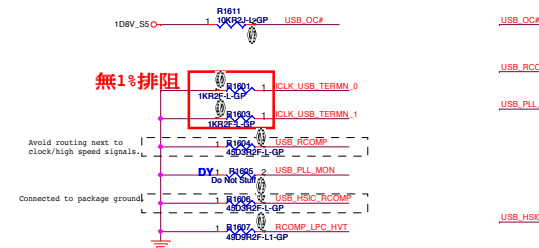
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13/7/5

**USB 3.0**  
34 USB\_CPU\_PP0 <>>> USB\_DP0  
34 USB\_CPU\_PP0 <>>> USB\_DN0  
34 USB\_CPU\_PP1 <>>> USB\_DP1  
34 USB\_CPU\_PP1 <>>> USB\_DN1

**USB 2.0**  
34 USB\_CPU\_PP1 <>>> USB\_DP1  
34 USB\_CPU\_PP1 <>>> USB\_DN1

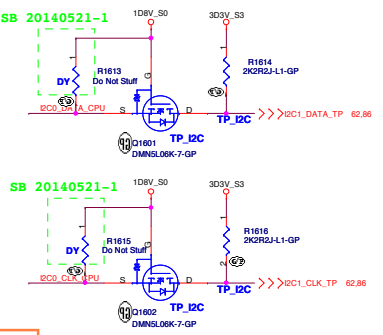
**Wifi + BT**  
58,86 USB\_CPU\_PP2 <>>> USB\_DP2  
58,86 USB\_CPU\_PP2 <>>> USB\_DN2  
13/7/5

**Camera**  
52,86 USB\_CPU\_PP3 <>>> USB\_DP3  
52,86 USB\_CPU\_PP3 <>>> USB\_DN3

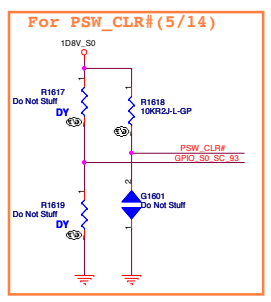


**1.8V**

GPIO\_S0\_55 <>>> USB\_DP0  
GPIO\_S0\_56 <>>> USB\_DN0  
GPIO\_S0\_57 <>>> USB\_DP1  
GPIO\_S0\_58 <>>> USB\_DN1  
GPIO\_S0\_59 <>>> USB\_DP2  
GPIO\_S0\_60 <>>> USB\_DN2  
GPIO\_S0\_61 <>>> USB\_DP3  
GPIO\_S0\_62 <>>> USB\_DN3



### USB Port Routing Guide for Bay Trail-M



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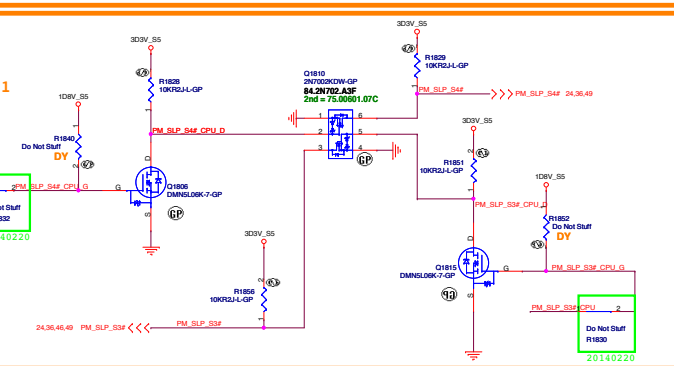
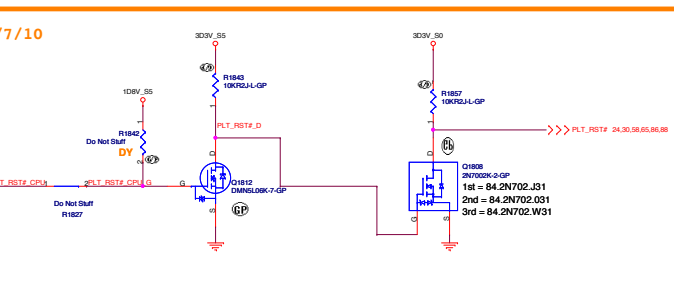
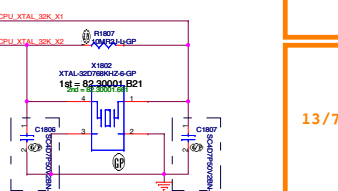
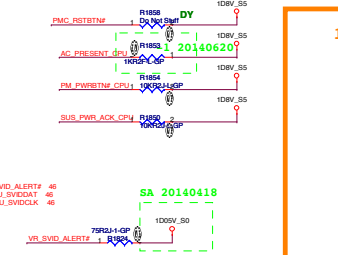
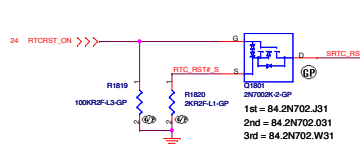
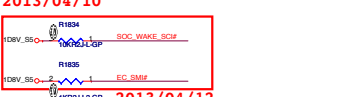
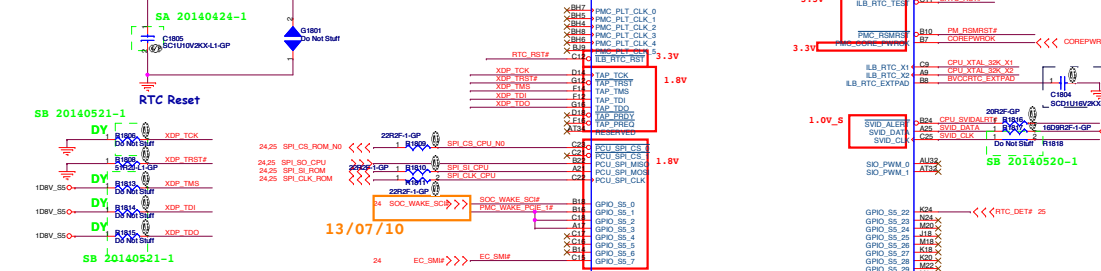
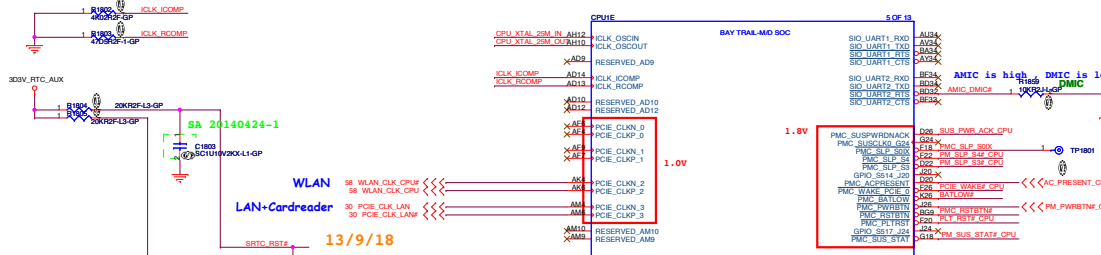
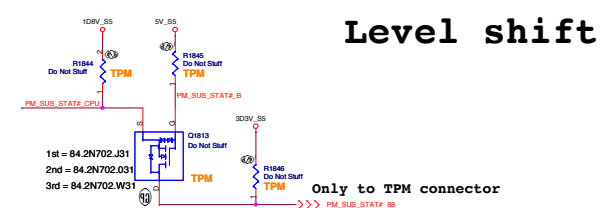
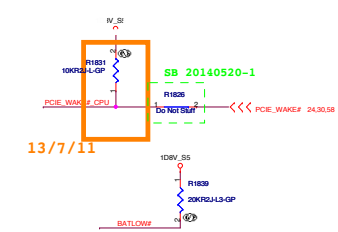
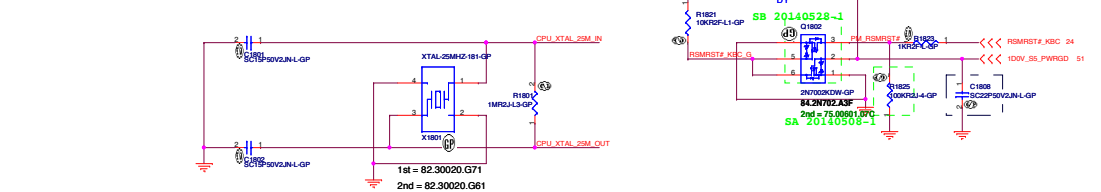
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Sheet 17 of

102





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Sheet 20 of

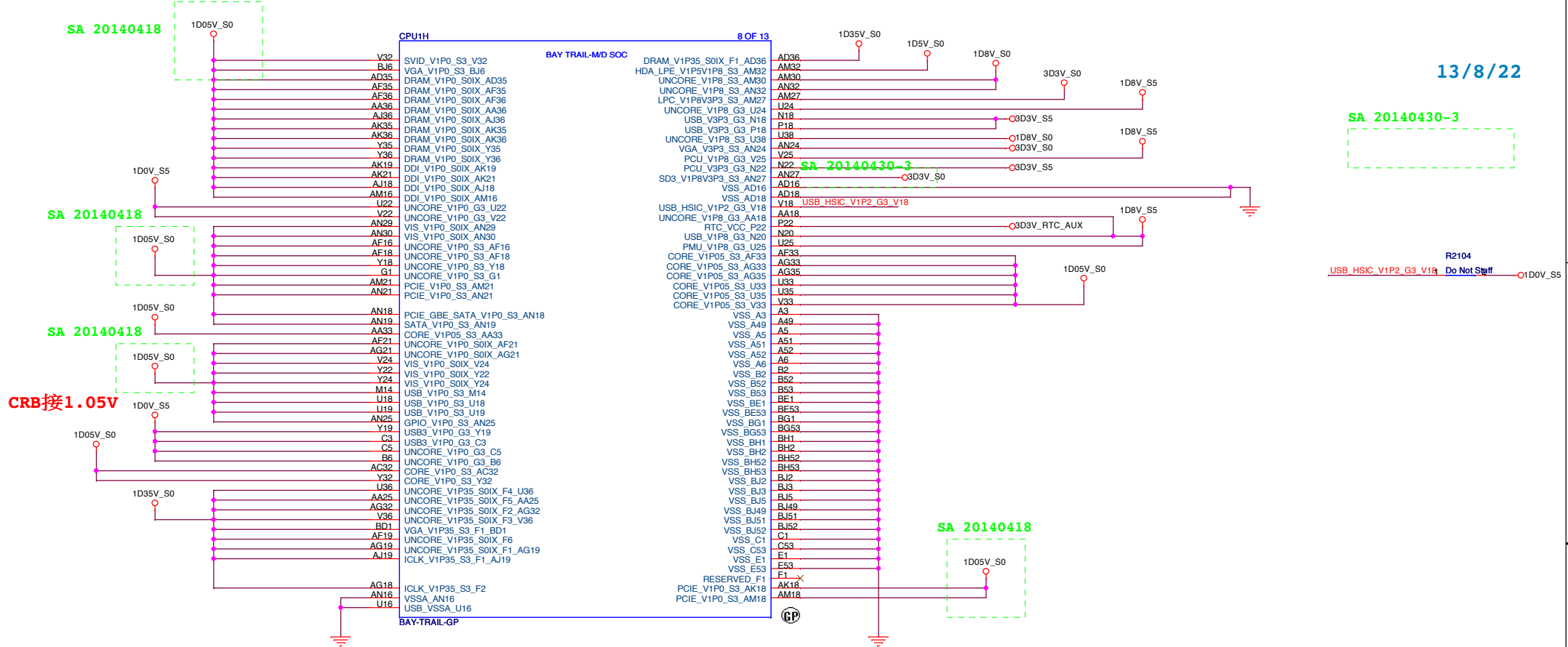
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SA 20140430-3

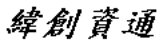
R2104  
USB\_HSIC\_V1P2\_G3\_V18 Do Not Stuff

CRB接1.05V



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Sheet 22 of 102

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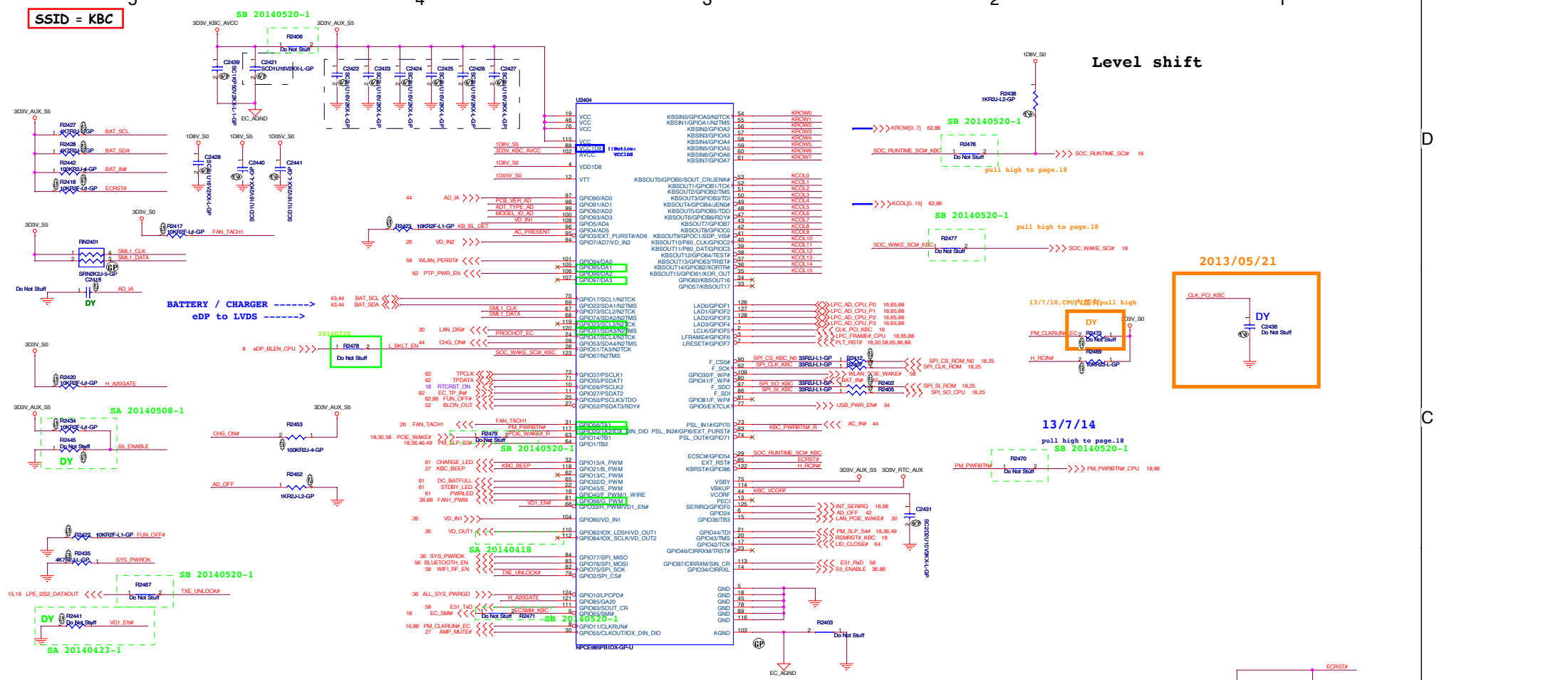
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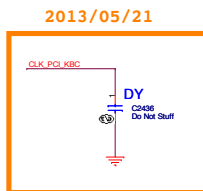
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Size Custom	Document Number		Rev
	<b>EA30 BM</b>		<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 23	of 102

SSID = KBC

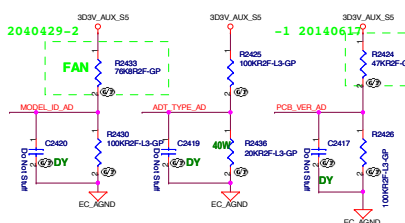
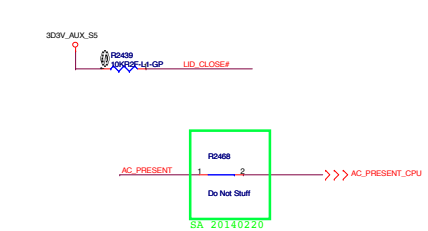
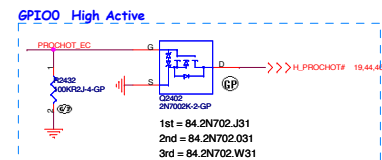
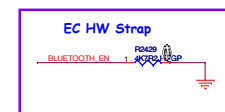
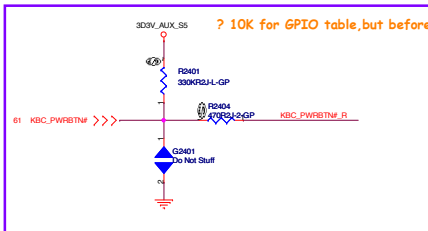


Level shift



2013/05/21

13/7/14

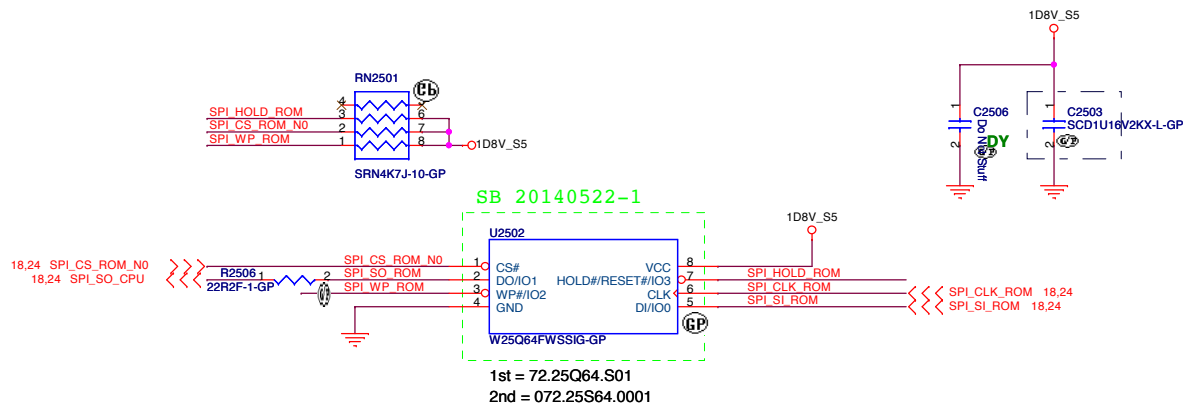


PCB_VER_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054 V	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592 V	< 2.383 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169 V	#VALUE!
ADT_TYPE_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
65W	N/A	100.0 K	3.300 V	3.3000 V	>= 3.000 V
90W	N/A	100.0 K	0.000 V	0.0000 V	< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055 V	>= 0.150 V
40W	20.0 K	100.0 K	0.550 V	0.5592 V	>= 0.425 V
MODEL_ID_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
EA30_FANLESS	100.0 K	10.0 K	3.000 V	3.0054 V	>= 2.875 V
EA30_FAN	100.0 K	20.0 K	2.750 V	2.7591 V	< 2.875 V
EA53_FANLESS	100.0 K	33.0 K	2.481 V	2.4935 V	< 2.616 V
EA53_FAN	100.0 K	47.0 K	2.245 V	2.2592 V	< 2.383 V
EA30_FANLESS_EMWG	100.0 K	64.9 K	2.001 V	2.0169 V	>= 1.122 V
EA30_FAN_EMWG	100.0 K	76.8 K	1.750 V	1.7591 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	0.000 V	0.0000 V	< 1.758 V

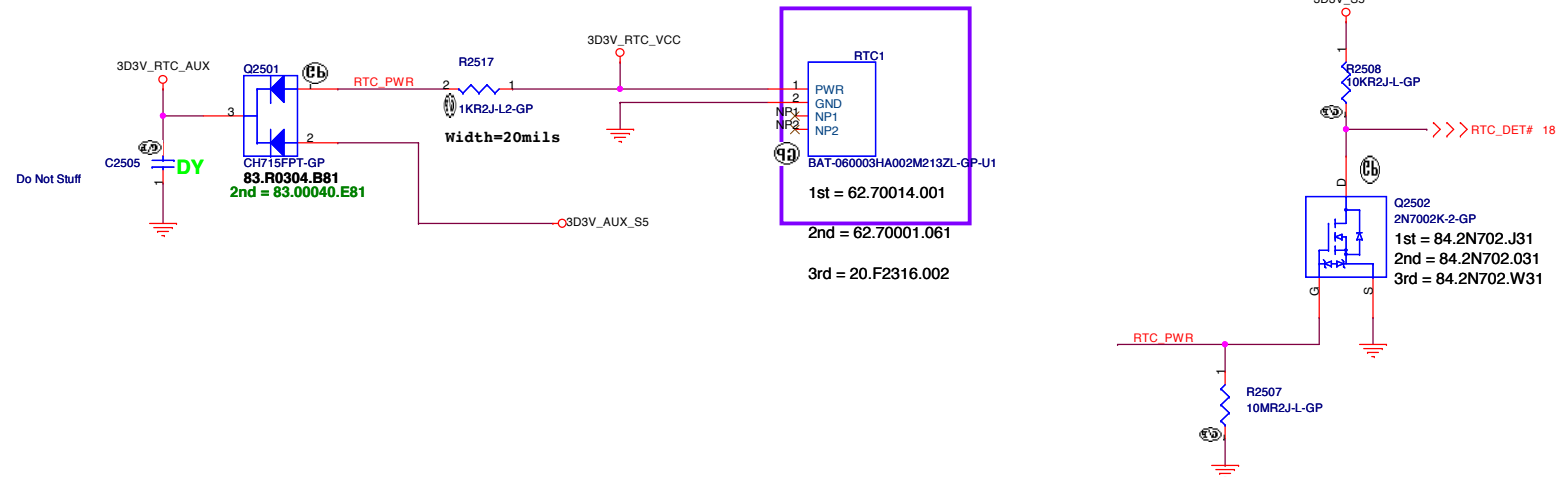
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No eMMC

**SSID = Flash.ROM**

**SPI FLASH ROM (8M BYTE) IC: PCH**



**SSID = RBAT**



**SPI FLASH ROM (128k byte) for EC**

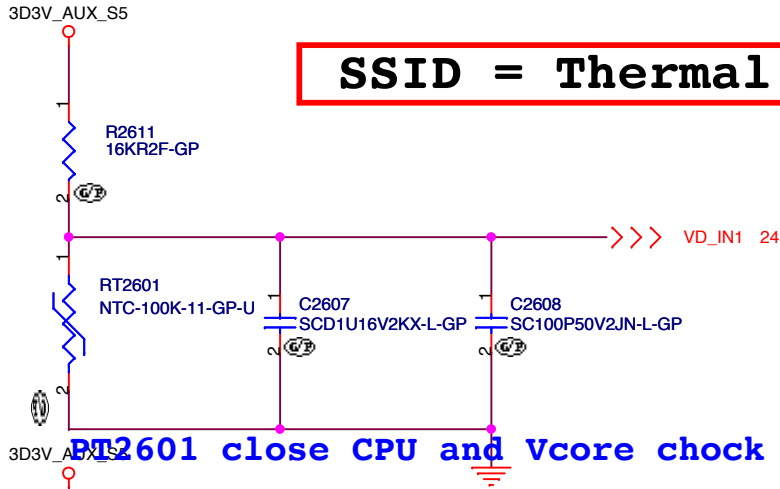
*SPI ROM Equal length need to less than 500mil*

**72.25010.N01**

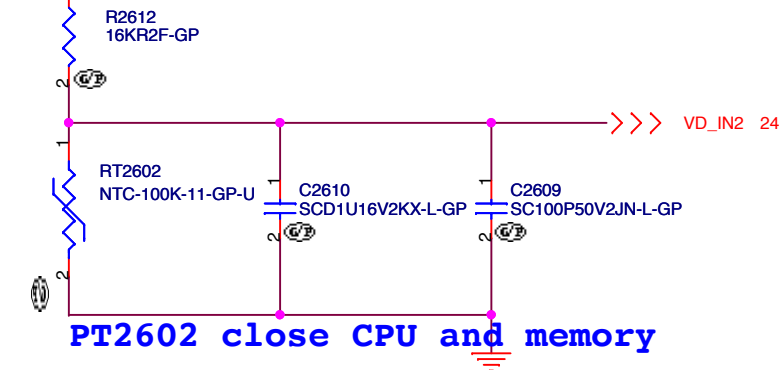
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<b>Flash(KBC+PCH)/RTC</b>	
Title	
Size A3	Document Number
Date: Tuesday, July 08, 2014	EA30 BM
Sheet 25	Rev -1

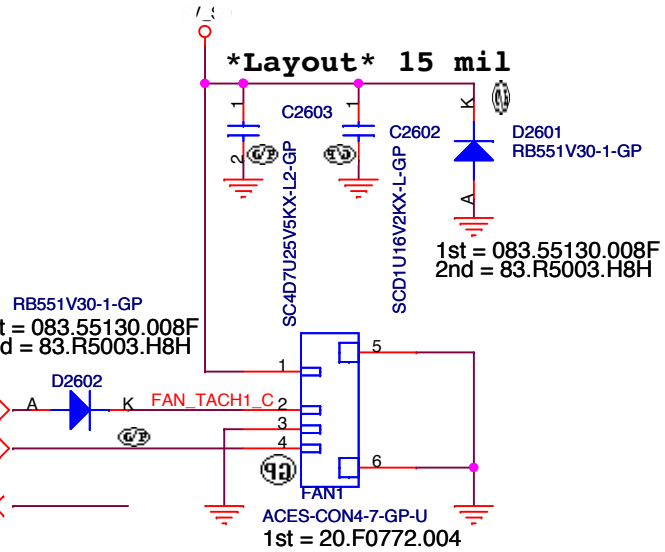
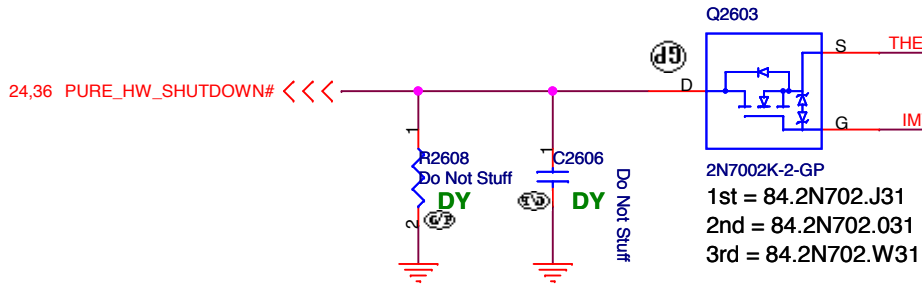
**SSID = Thermal**



**PT2601 close CPU and Vcore chock**

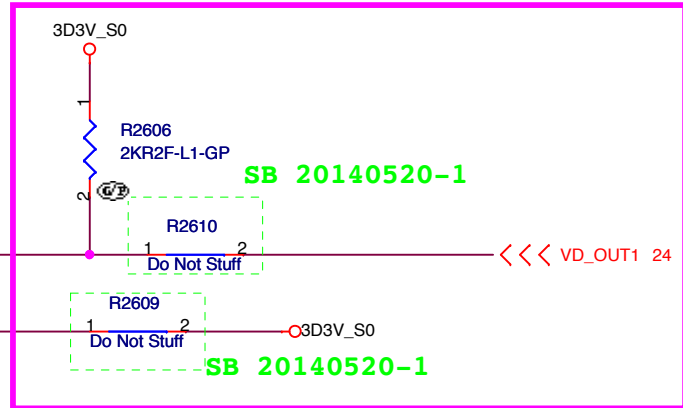


**PT2602 close CPU and memory**



RB551V30-1-GP  
1st = 083.55130.008F  
2nd = 83.R5003.H8H

24 FAN\_TACH1 >>> A  
24,86 FAN1\_PWM >>> K  
86 FAN\_TACH1\_C <<<



**SB 20140520-1**

Do Not Stuff

**SB 20140520-1**

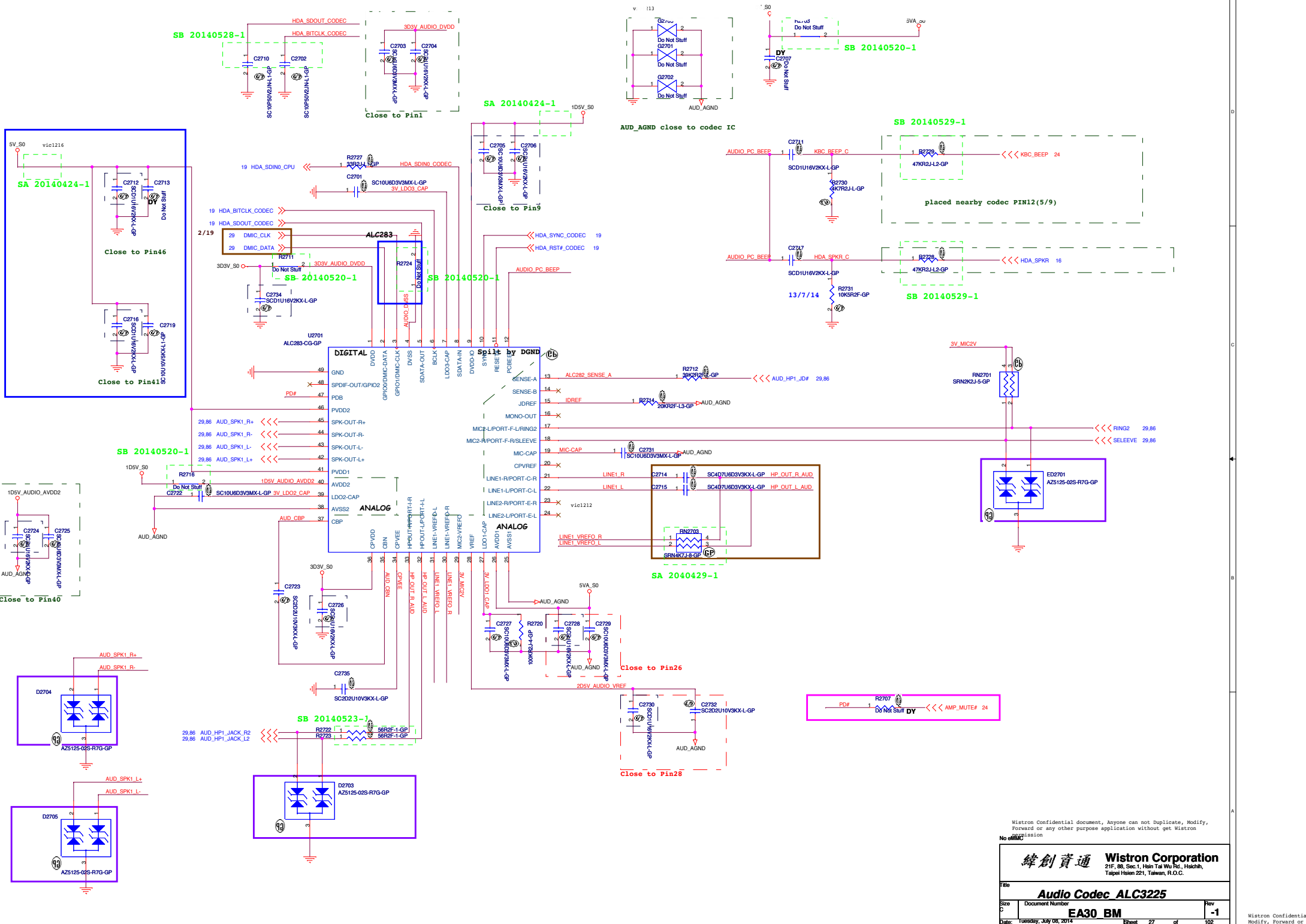
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Title: **G788P81/Fan Controller P2793**

Size A4 Document Number: **EA30 BM** Rev: **-1**

Date: Tuesday, July 08, 2014 Sheet 26 of 102



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 Taipei Hsien 221, Taiwan, R.O.C.

Title

**Audio AMP 1001**

Size  
 A4

Document Number

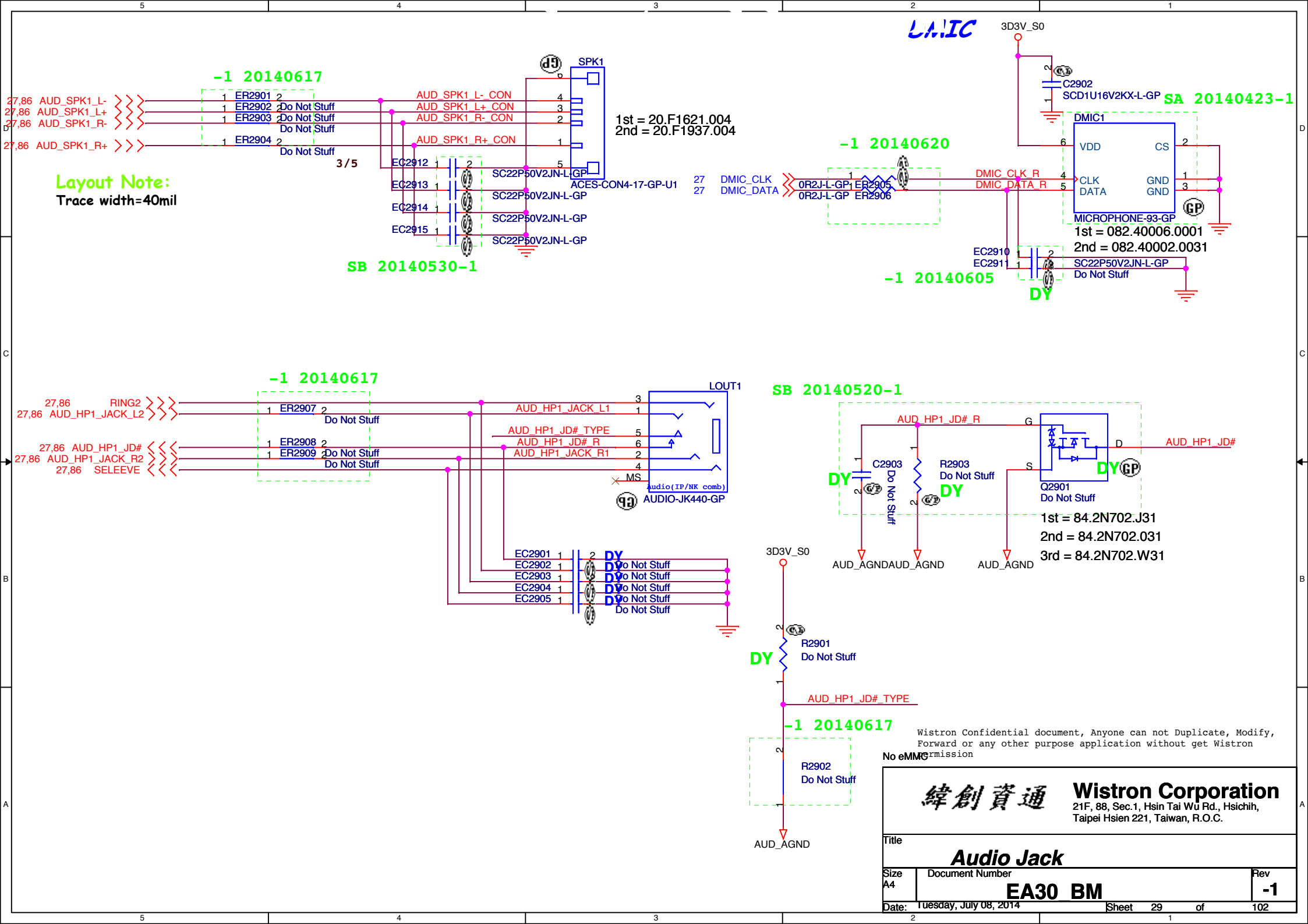
**EA30 BM**

Rev  
**-1**

Date: Tuesday, July 08, 2014

Sheet 28 of

102



**Layout Note:**  
Trace width=40mil

1st = 20.F1621.004  
2nd = 20.F1937.004

**LA.I.C**

SA 20140423-1

SB 20140530-1

-1 20140605

DY

-1 20140617

SB 20140520-1

DY

DY GP

1st = 84.2N702.J31  
2nd = 84.2N702.031  
3rd = 84.2N702.W31

DY

-1 20140617

R2902  
Do Not Stuff

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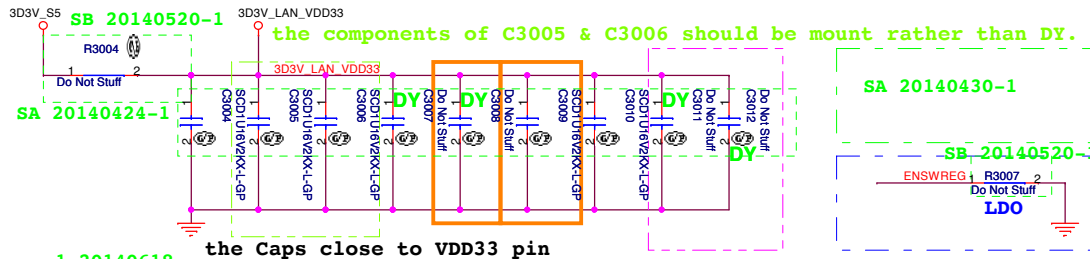
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Title **Audio Jack**

Size A4 Document Number **EA30 BM** Rev **-1**

Date: Tuesday, July 08, 2014 Sheet 29 of 102

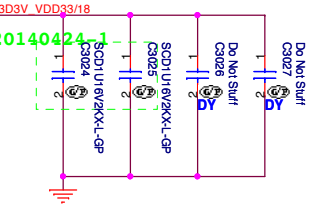


the Caps close to VDD33 pin

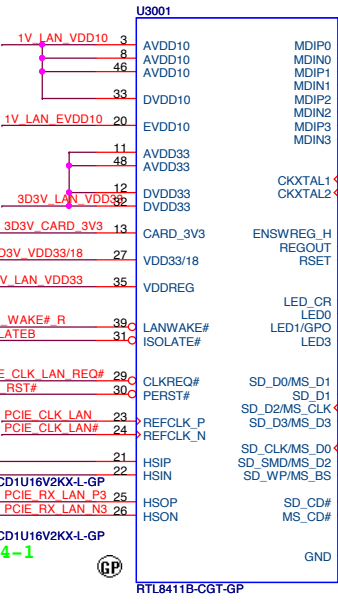
Close to VDDREG pin

SP5	2	ER3014	1	<<>>	SD_DATA1	33,86
SP6	2	ER3022	1	<<>>	SD_DATA0	33,86
SP7	2	22R2F-1-GP	ER3021	<<>>	SD_CLK	33,86
SP8	2	ER3024	1	<<>>	SD_CMD	33,86
SP9	2	ER3023	1	<<>>	SD_DATA3	33,86
SP10	2	ER3025	1	<<>>	SD_DATA2	33,86
				<<>>	SD_WP	33
				<<>>	SD_CD#	33,86

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	SD_D1	MS_CLK
SP6	SD_D0	MS_D7
SP7	SD_CLK	MS_D3
SP8	SD_CMD	MS_D6
SP9	SD_D3	MS_D2
SP10	SD_D2	MS_D1
SP11	MS_D0	XD_CLE
SP12	SD_WP	XD_WP#
SP13	SD_CD#	MS_D5
SP14	MS_D4	XD_D0
SP15	MS_D0	XD_D1
SP16		XD_CD#

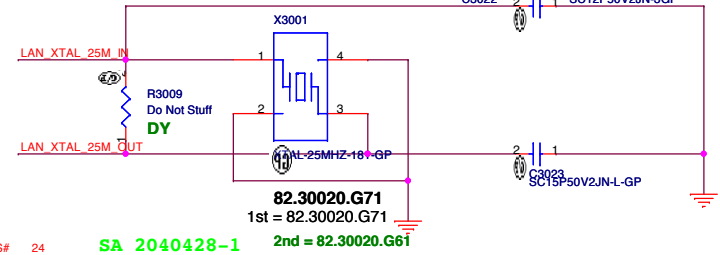
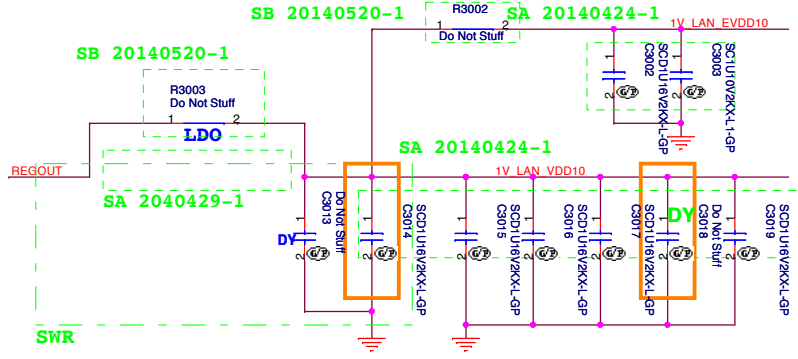
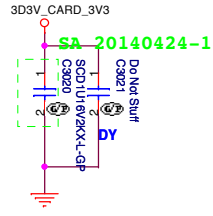


PCIE_CLK_LAN_REQ#	>>>	PCIE_CLK_LAN_REQ#	19
PCIE_CLK_LAN	<<<	PCIE_CLK_LAN	18
PCIE_CLK_LAN#	<<<	PCIE_CLK_LAN#	18
PLT_RST#	<<<	PLT_RST#	18,24,58,65,86,88

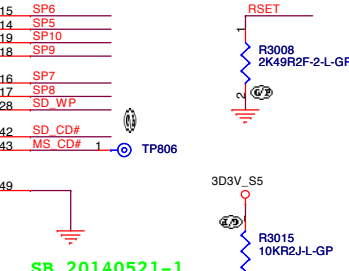
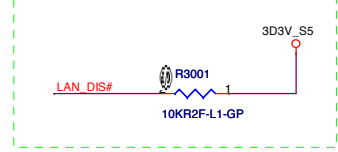


1st = 071.8411B.0003

PCIE_TX_LAN_P3	>>>	PCIE_TX_LAN_P3	19
PCIE_TX_LAN_N3	>>>	PCIE_TX_LAN_N3	19
PCIE_RX_CPU_P3	>>>	PCIE_RX_CPU_P3	19
PCIE_RX_CPU_N3	>>>	PCIE_RX_CPU_N3	19

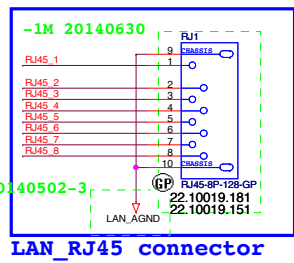
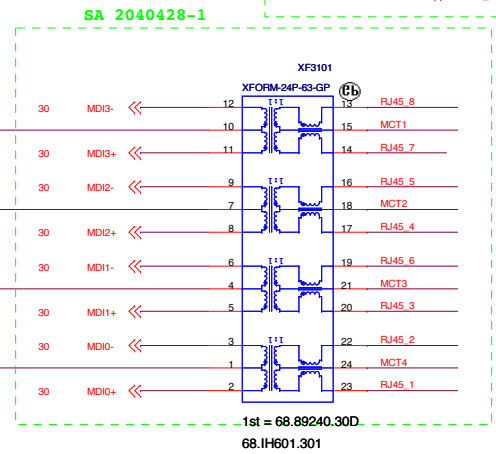
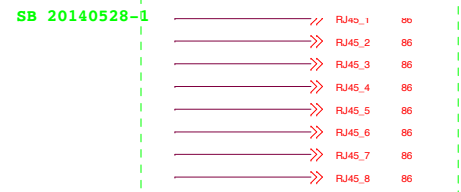


1st = 82.30020.G71  
2nd = 82.30020.G61

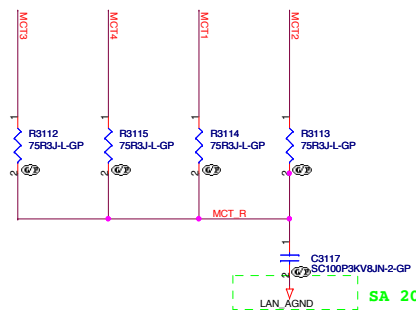
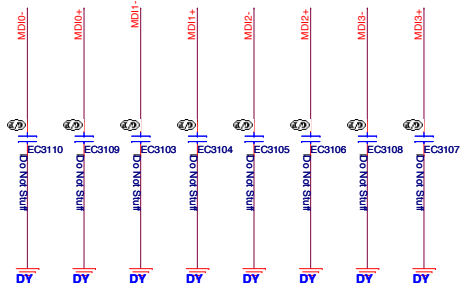
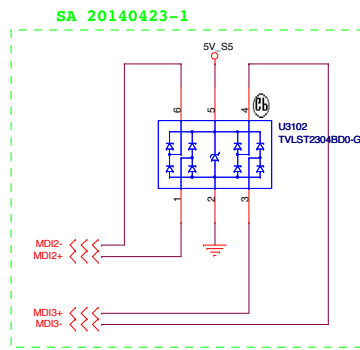
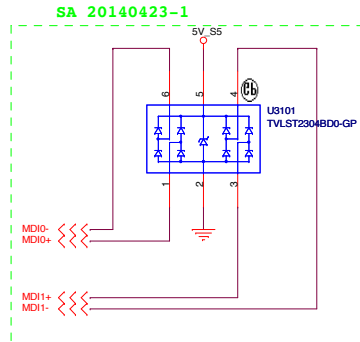
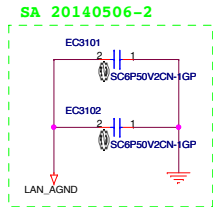


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**SSID = LAN**



SA 20140502-3



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Title

**RTS5229(CARD READER)**

Size

A4

Document Number

**EA30 BM**

Rev

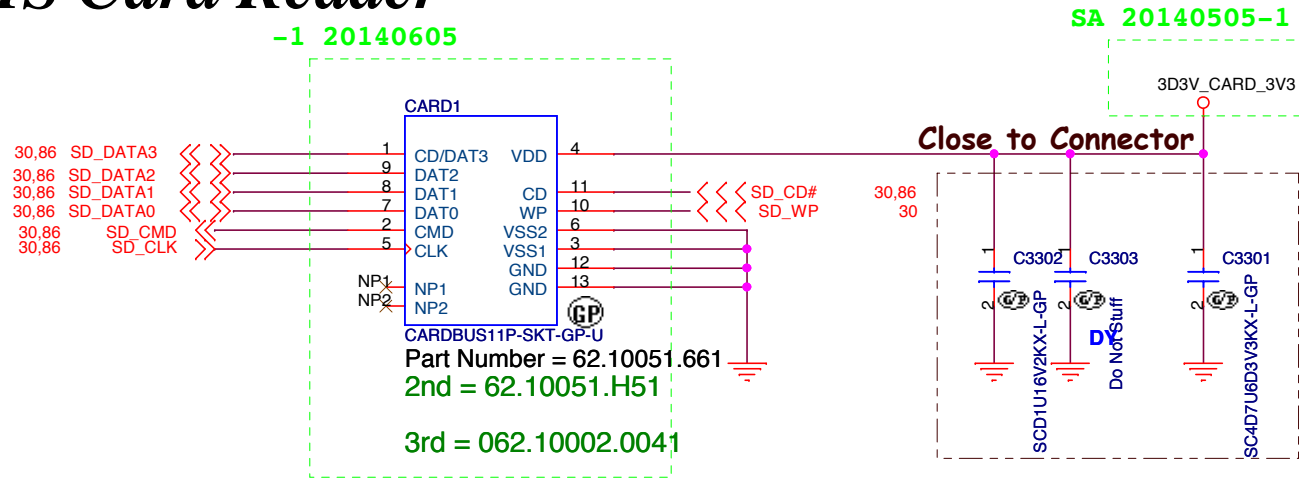
**-1**

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Sheet 32 of 102

SSID = SDIO

# SD//MS Card Reader



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Title

**CARD Reader CONN**

Size  
Custom

Document Number

**EA30 BM**

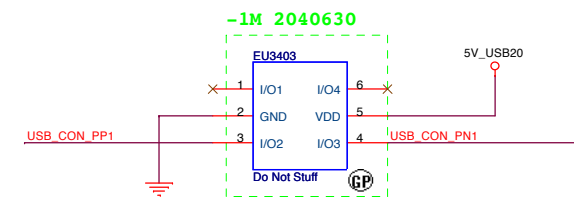
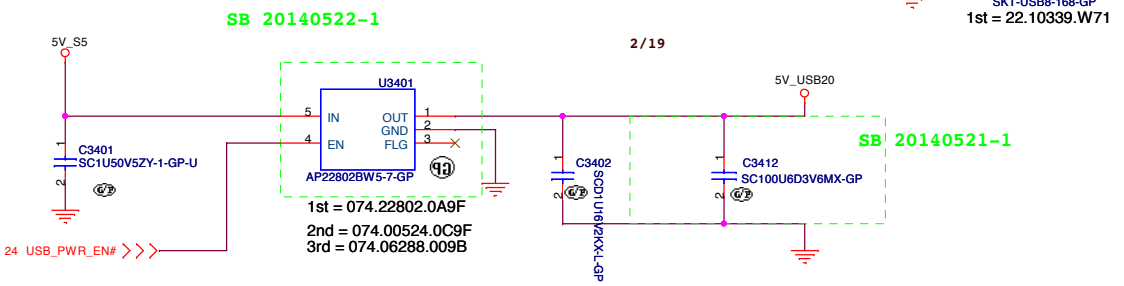
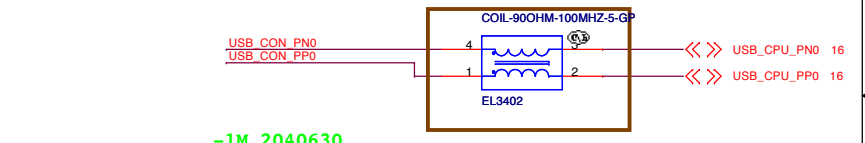
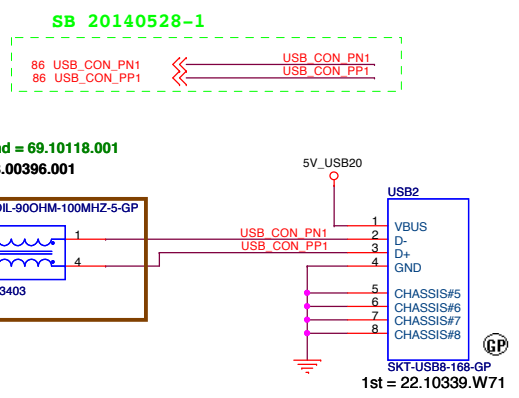
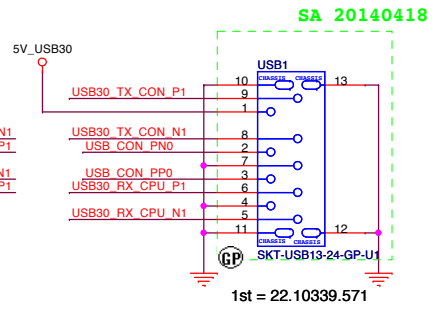
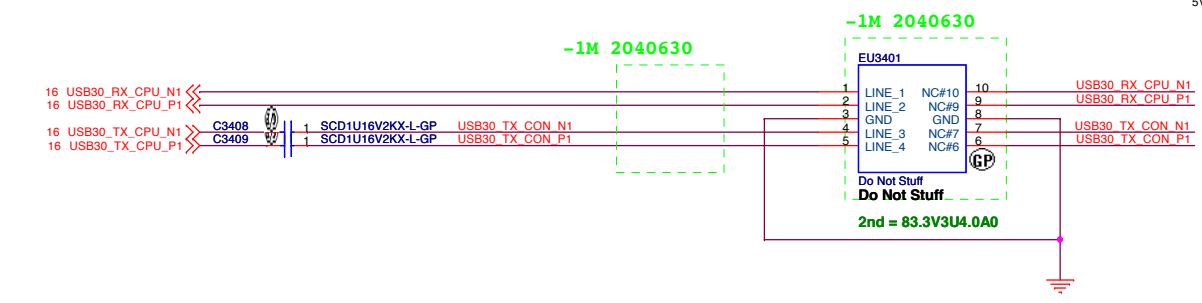
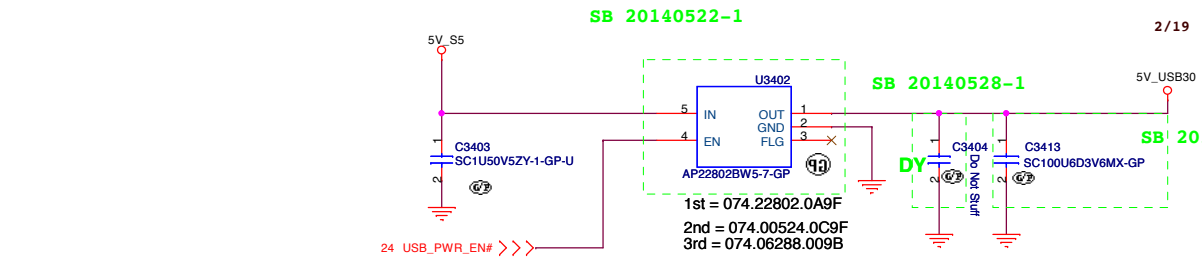
Rev

**-1**

Date: Tuesday, July 08, 2014

Sheet 33 of 102

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



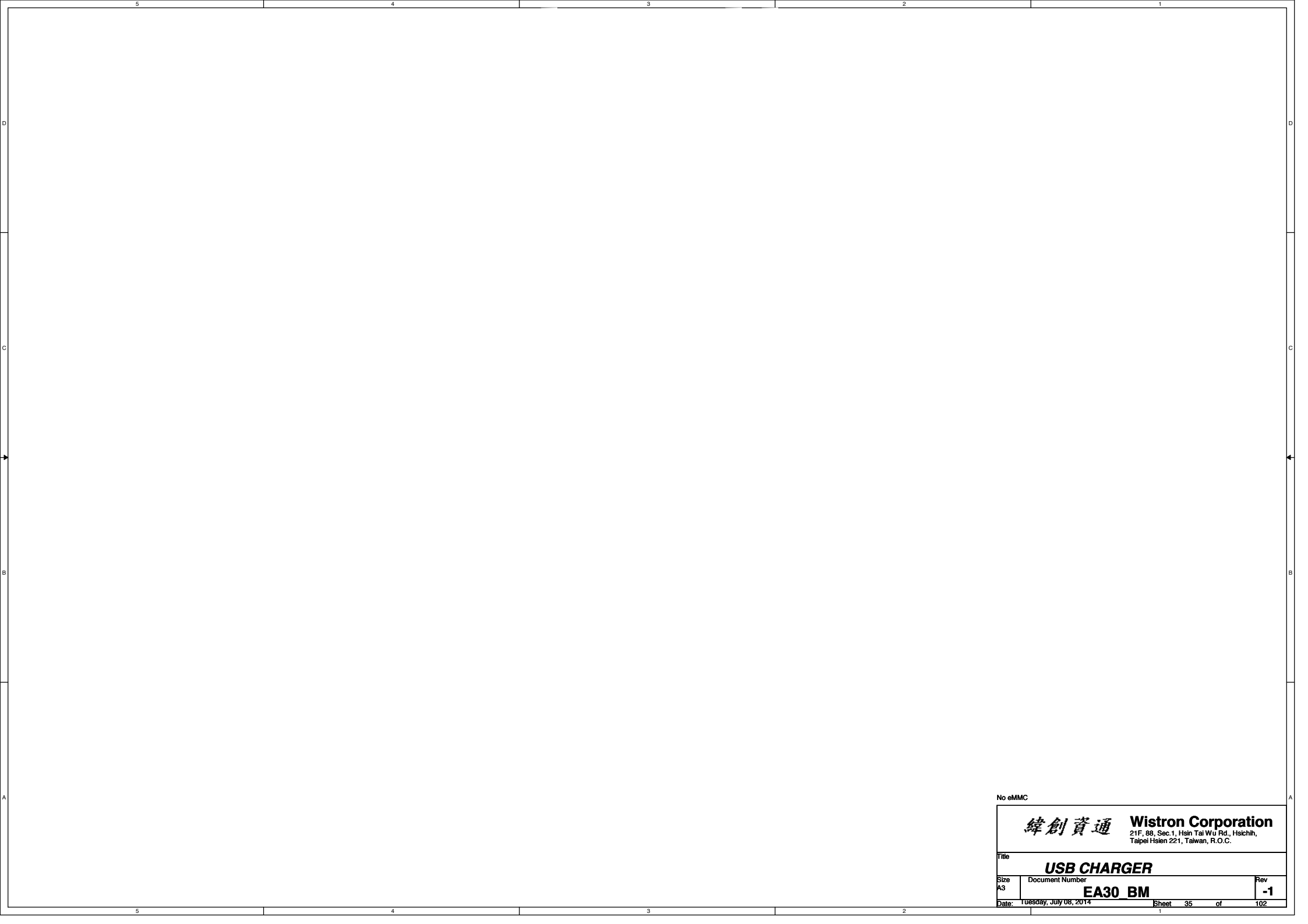
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Title: **USB 2.0/3.0 Port**

Size A3 Document Number: **EA30 BM** Rev: **-1**

Date: Tuesday, July 08, 2014 Sheet 34 of 102



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Title

**USB CHARGER**

Size

A3

Document Number

**EA30 BM**

Rev

**-1**

Date: Tuesday, July 08, 2014

Sheet 35 of 102

# Power Sequence

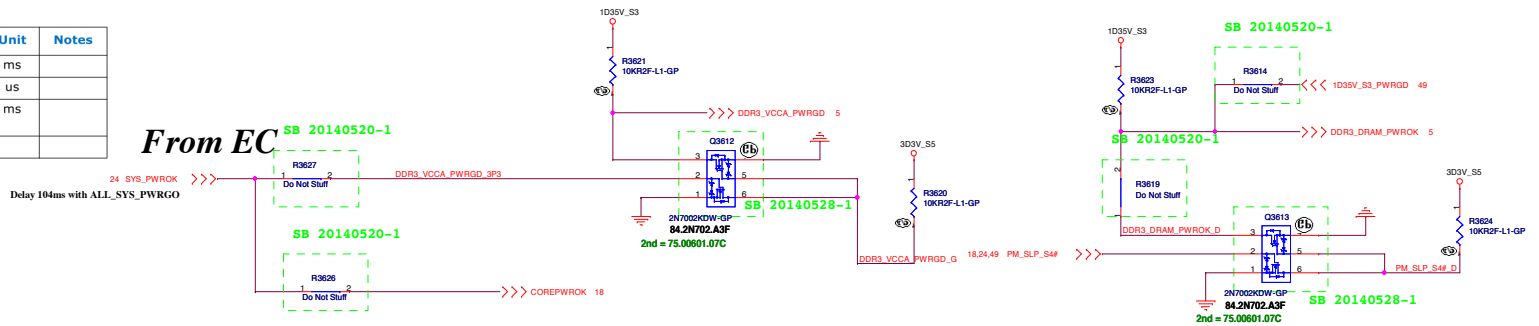
Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWR0K and PMC_CORE_PWR0K assertion	100		ms	
T3					

## DDR3\_VCCA\_PWRGD

## DDR3\_DRAM\_PWR0K

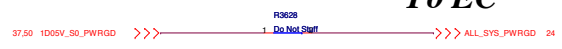
From EC SB 20140520-1



## ALL\_SYS\_PWRGD

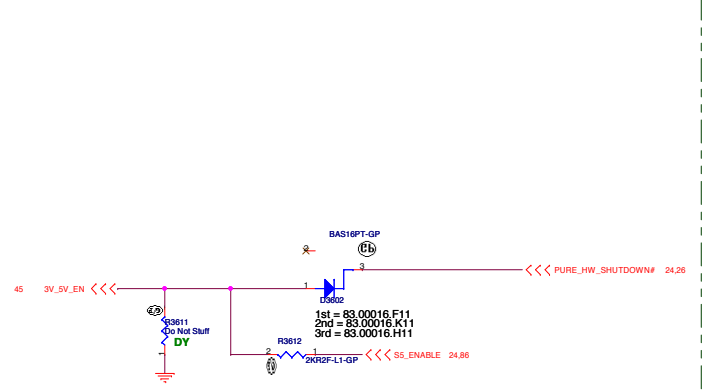
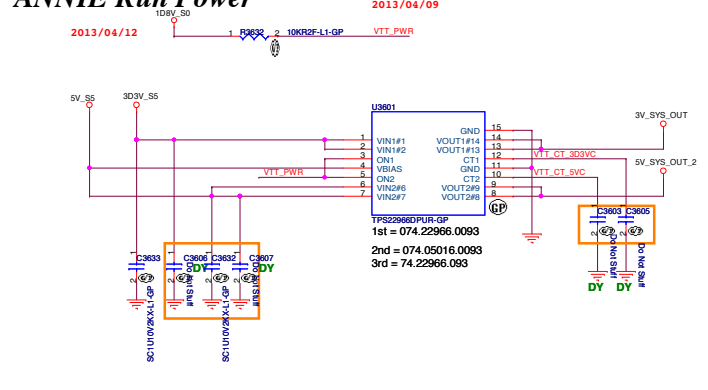
## COREPWR0K

13/8/22 To EC

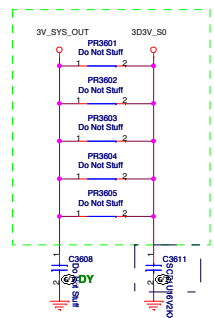


## ANNIE Run Power

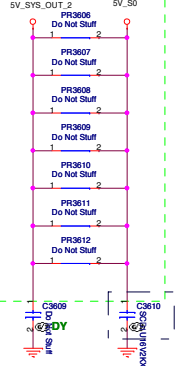
13/9/18



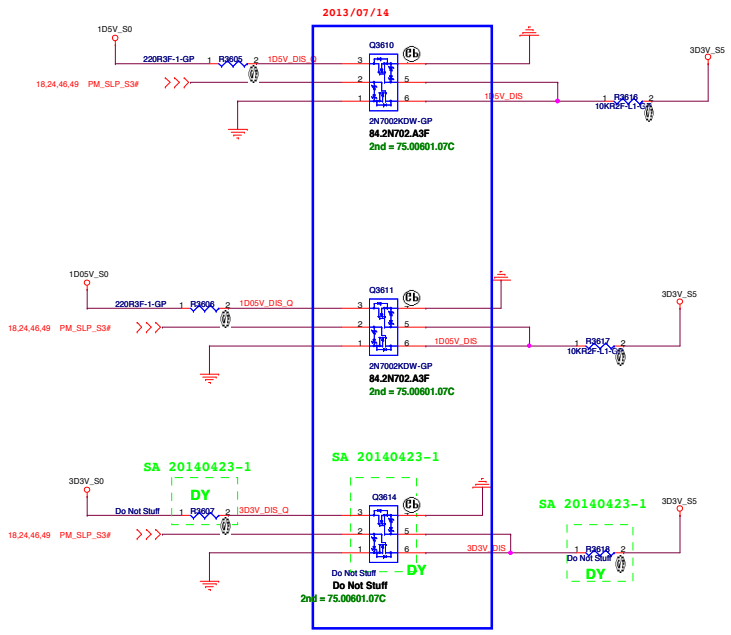
## SB 20140520-1



## SB 20140520-1



## Discharge circuit





5

4

3

2

1

D

D

C

C

B

B

A

A

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<b>Title</b>			
<b>DS3</b>			
<b>Size</b> A4	<b>Document Number</b> <b>EA30 BM</b>		<b>Rev</b> <b>-1</b>
<b>Date:</b> Tuesday, July 08, 2014		<b>Sheet</b> 38	<b>of</b> 102

5

4

3

2

1

# Power Sequence

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Title			
<b>1D05 M</b>			
Size	Document Number	Rev	
Custom	<b>EA30 BM</b>	<b>-1</b>	
Date:	Tuesday, July 08, 2014	Sheet	39 of 102

D

D

C

C

B

B

A

A

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Title  
**Connected Standby1**

Size A	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
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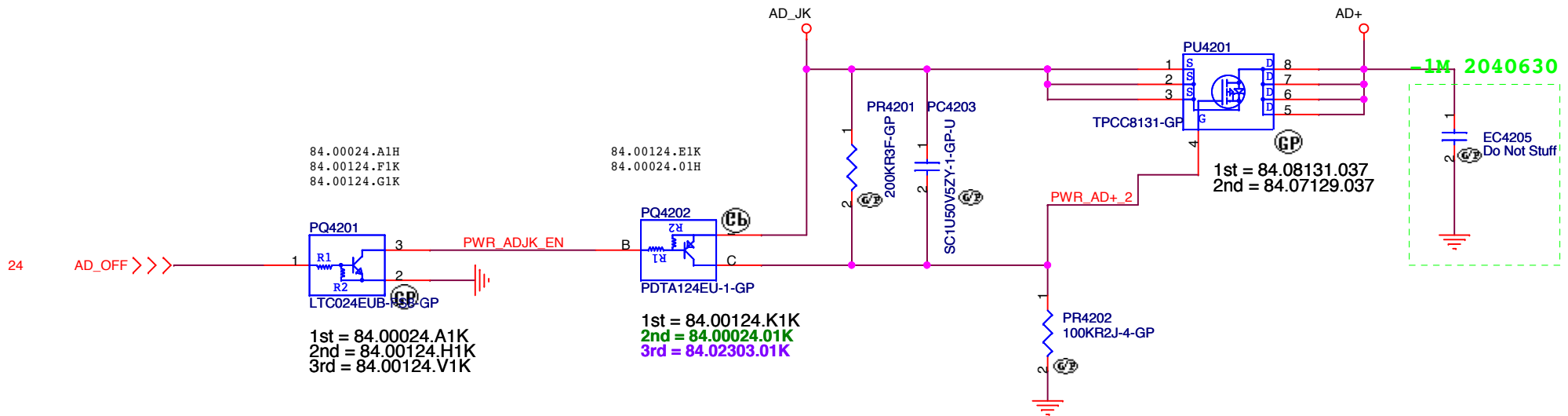
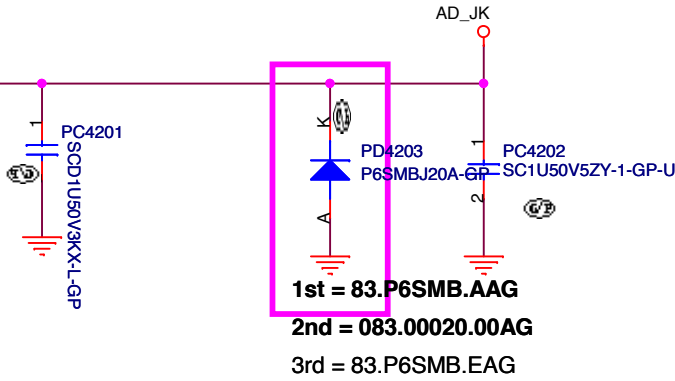
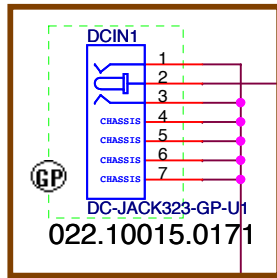
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Title		
<b>Connected Standby2</b>		
Size	Document Number	Rev
A	<b>EA30 BM</b>	<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 41 of 102

# ANNIE solution

Adaptor in to generate DCBATOUT

3/4 SA 20140418



vic0103

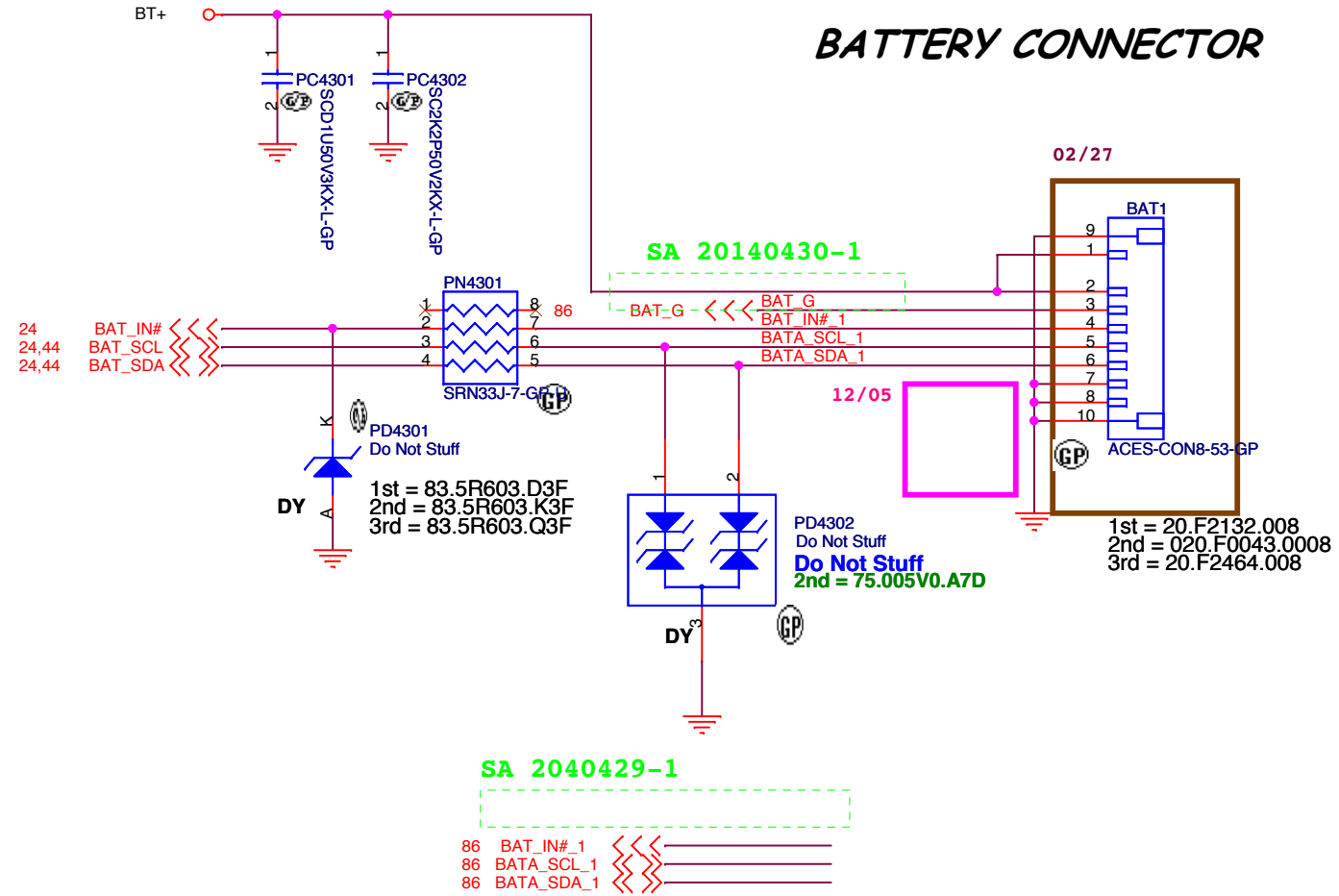
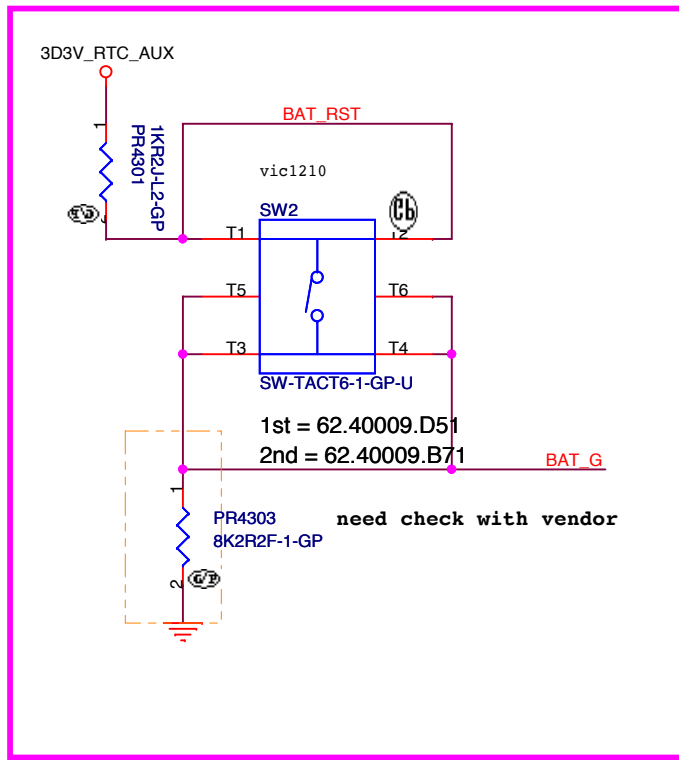


DC IN connector

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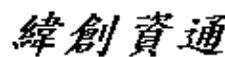
No eMMC

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>DCIN JACK</b>			
Size A4	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 42	of	102



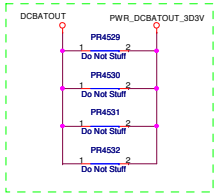
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No eMMC

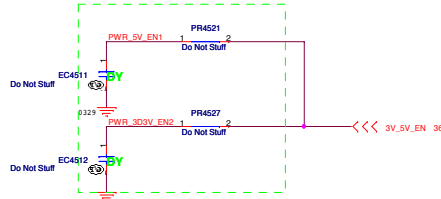
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>BATT CONN</b>	
<b>Size</b> A4	<b>Document Number</b> <b>EA30 BM</b>
<b>Date:</b> Tuesday, July 08, 2014	<b>Rev</b> <b>-1</b>
<b>Date:</b> Tuesday, July 08, 2014	<b>Sheet</b> 43 <b>of</b> 102



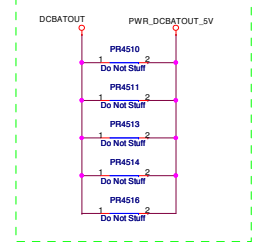
SB 20140520-1



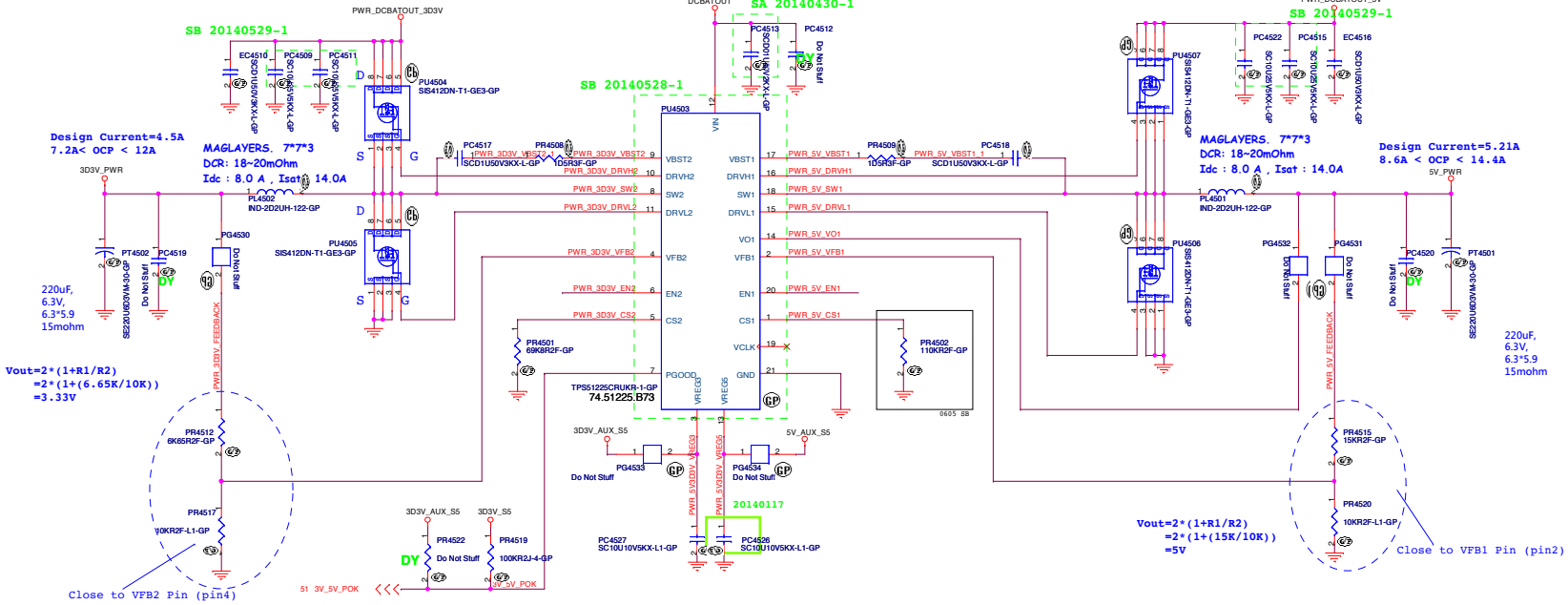
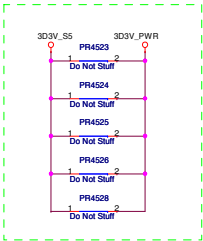
-1 20140617



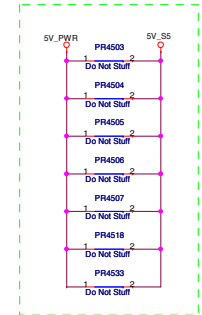
SB 20140520-1



SB 20140520-1



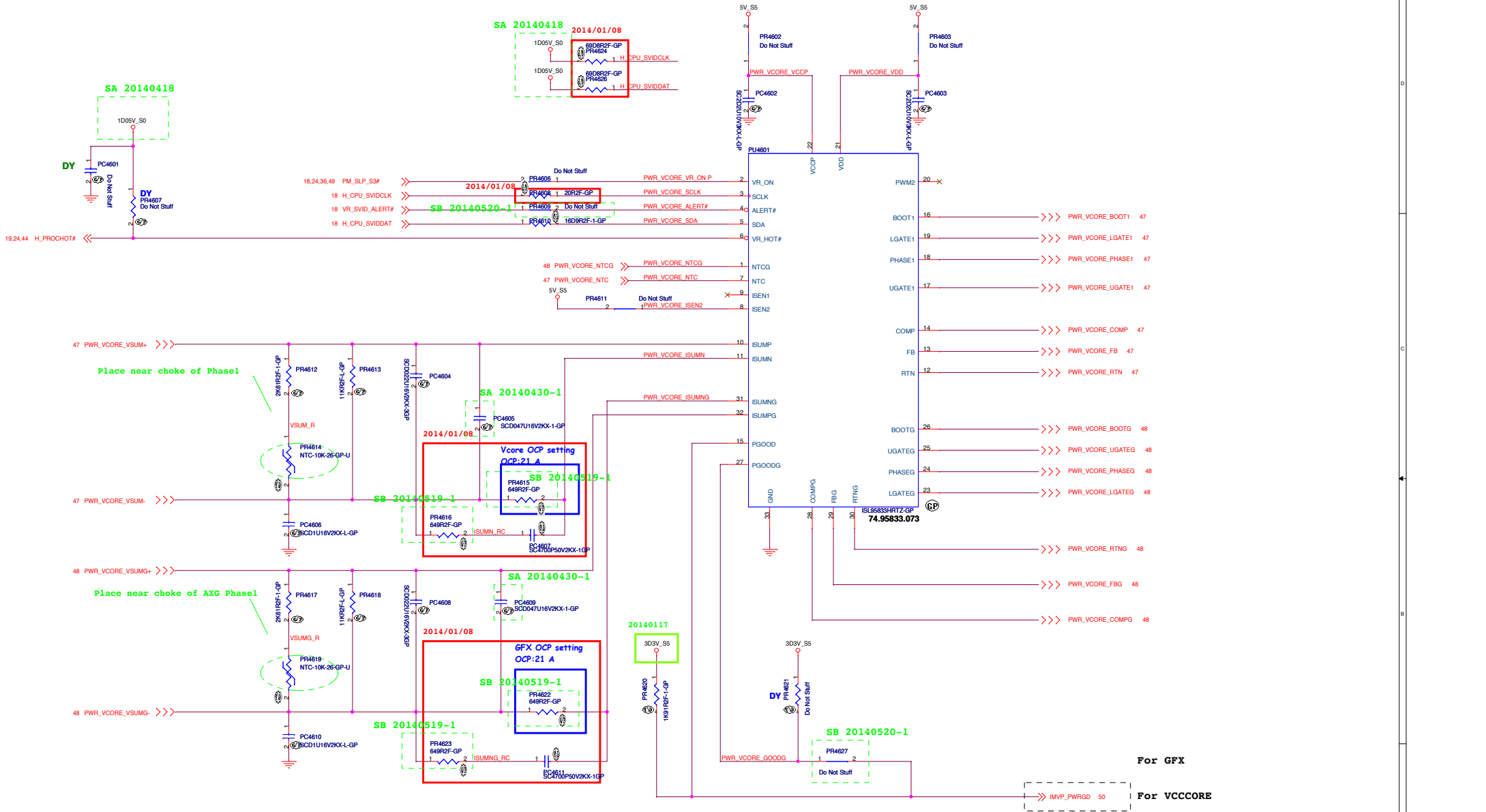
SB 20140520-1



No eMMC

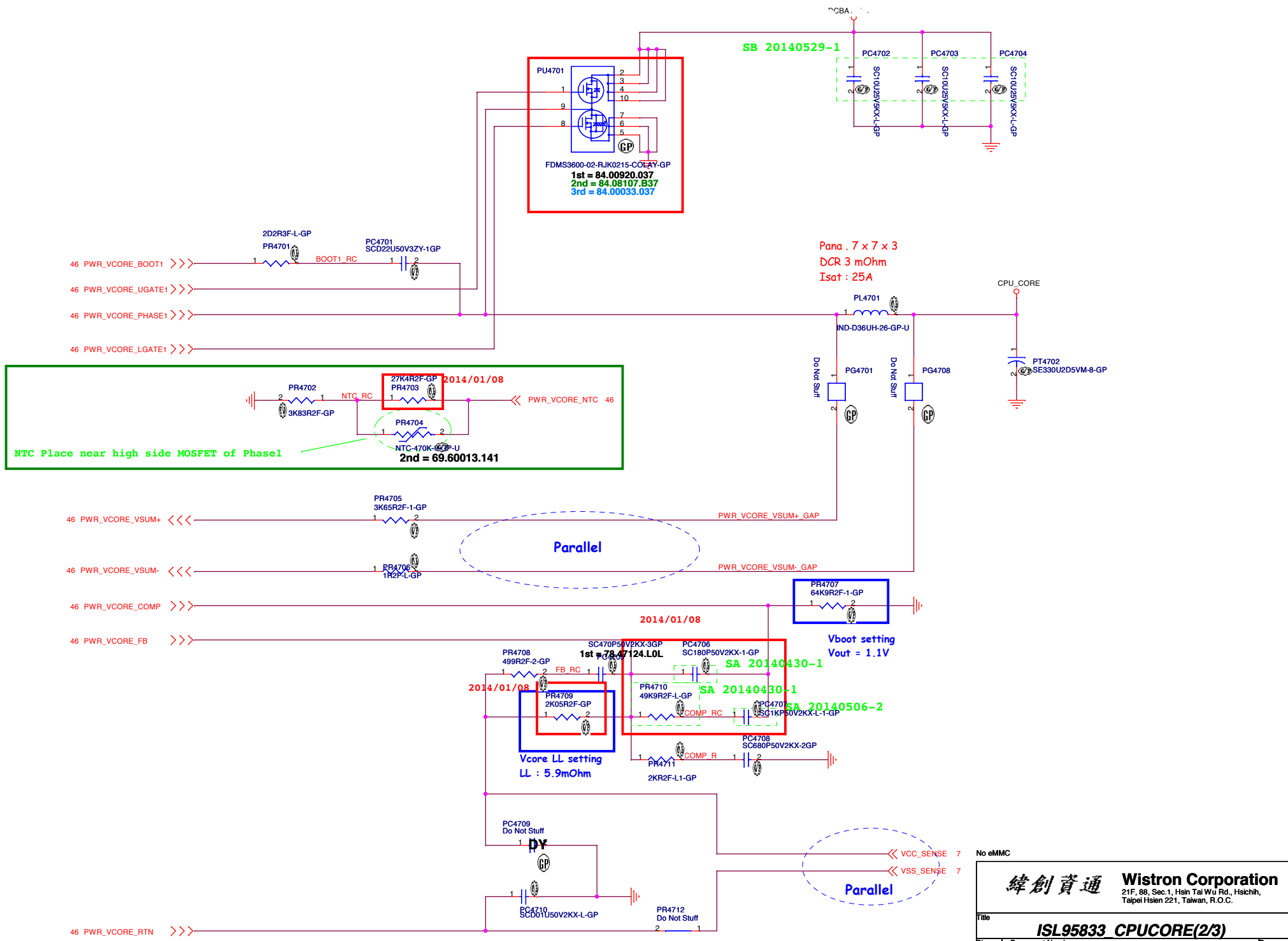
緯創資通 Wistron Corporation  
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Taipei Hsin 221, Taiwan, R.O.C.

Title			TPS51225 5V/3D3V		
Size	Document Number	Rev			
A2	EA51 BM	-1			
Date:	Tuesday, July 08, 2014	Sheet	46	of	102



For GFX

For VCCORE



PU4701  
 1 2 3 4 10  
 9 7 6 5  
 8  
 FDMS3600-02-RJK0215-COLEAY-GP  
 1st = 84.00920.037  
 2nd = 84.08107.837  
 3rd = 84.00033.037

SB 20140529-1  
 PC4702  
 PC4703  
 PC4704  
 SC10U25V9KX-L-GP  
 SC10U25V9KX-L-GP  
 SC10U25V9KX-L-GP

27K4R2F-GP 2014/01/08  
 PR4703  
 PR4704  
 NTC-470K-4GP-U  
 2nd = 69.60013.141  
 NTC Place near high side MOSFET of Phase1

Pana . 7 x 7 x 3  
 DCR 3 mOhm  
 Isat : 25A

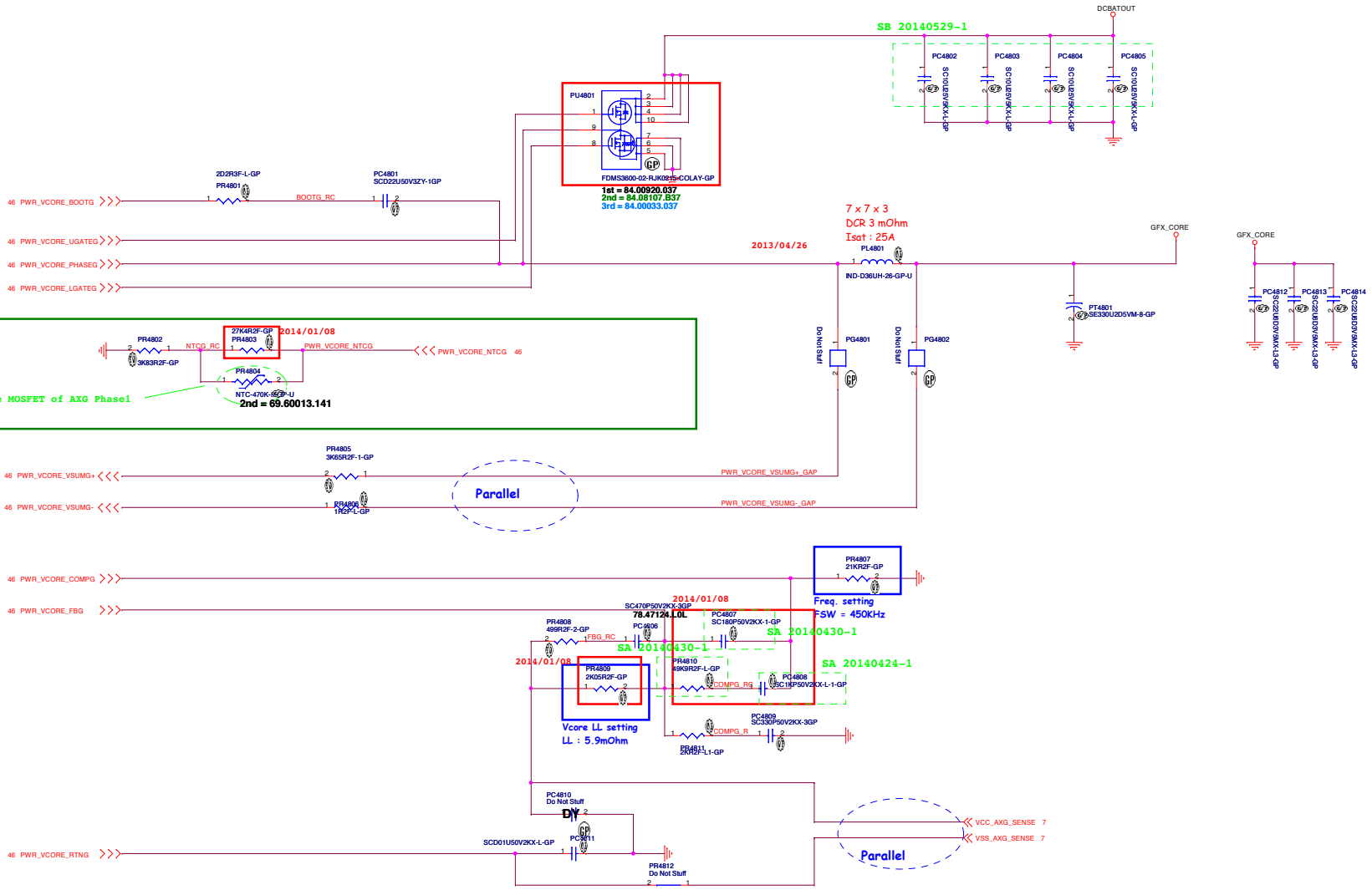
Parallel

2014/01/08  
 PR4707  
 64K9R2F-1-GP  
 Vboot setting  
 Vout = 1.1V  
 PR4709  
 2K05R2F-GP  
 Vcore LL setting  
 LL : 5.9mOhm  
 PR4710  
 49K9R2F-L-GP  
 SA 20140430-1  
 SA 20140430-1  
 SA 20140506-2  
 PR4711  
 2KR2F-L1-GP  
 PR4712  
 Do Not Stuff

Parallel  
 VCC\_SENSE 7  
 VSS\_SENSE 7

No eMMC

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Title <b>ISL95833 CPUCORE(2/3)</b>		
Size A3	Document Number <b>EA51 BM</b>	Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 47	of 102



NTC place near high side MOSFET of AXG Phase1

2014/01/08  
 2nd = 69.60013.141

SB 20140529-1

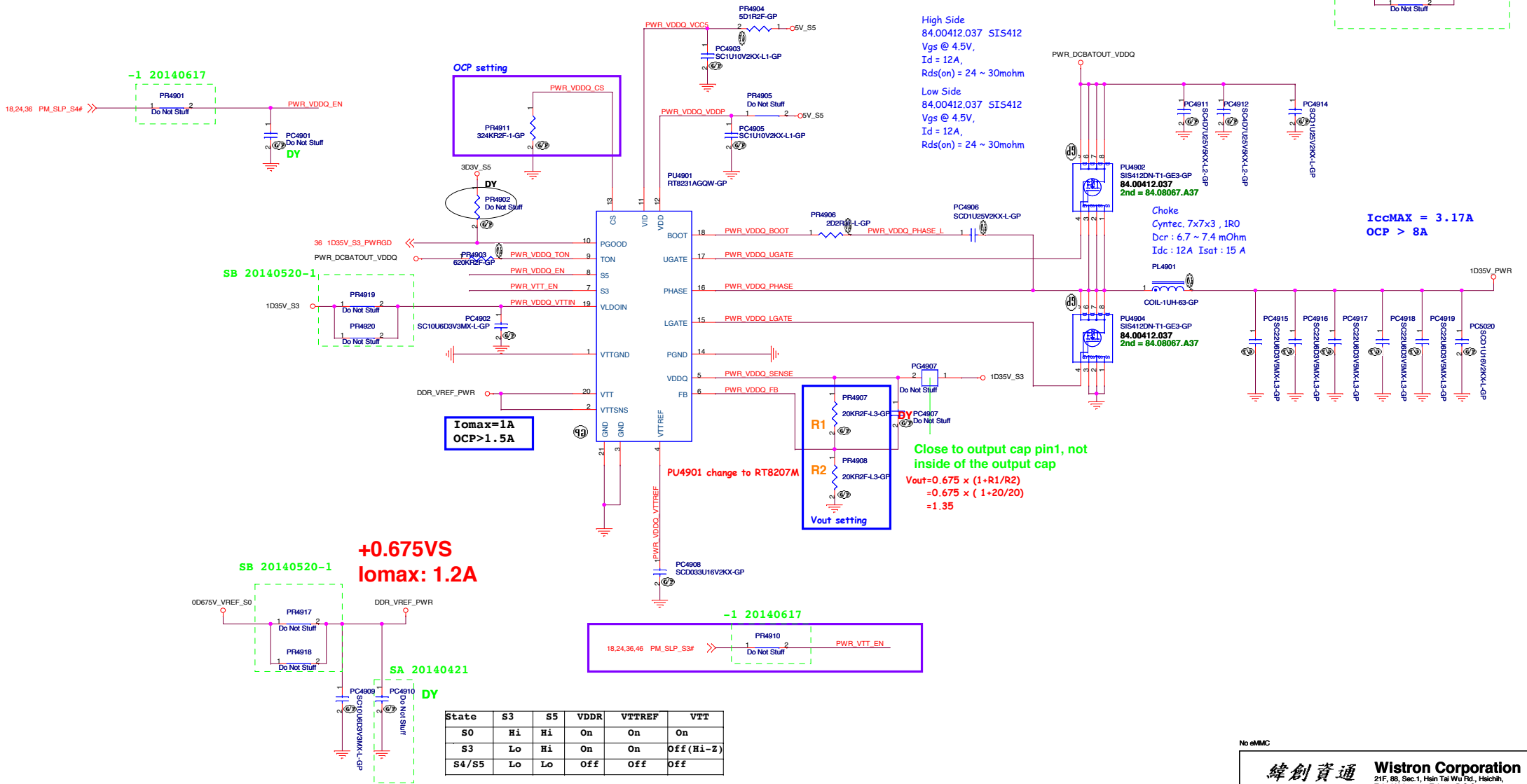
PC4802 SC1028V2KX-L-GP  
 PC4803 SC1028V2KX-L-GP  
 PC4804 SC1028V2KX-L-GP  
 PC4805 SC1028V2KX-L-GP

7 x 7 x 3  
 DCR 3 mOhm  
 Isat : 25A

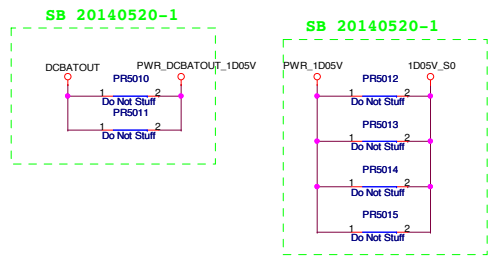
Parallele

Parallele

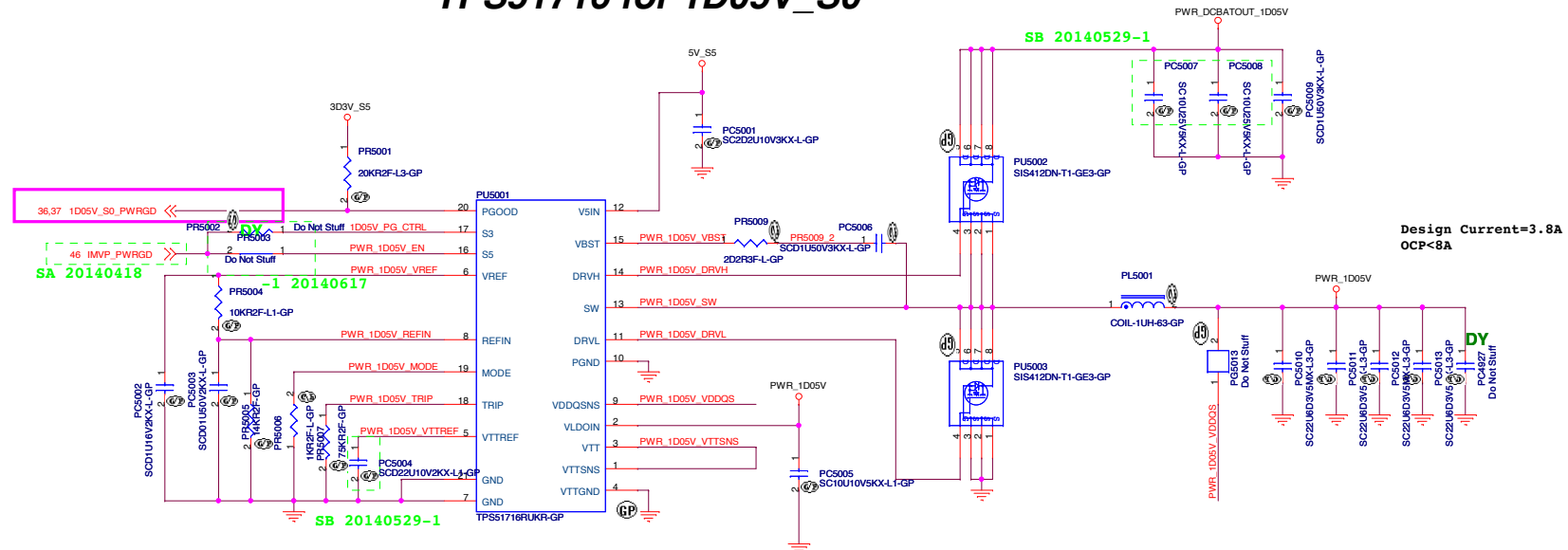
# RT8231 for VDDQ



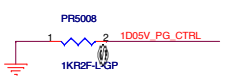
SSID = PWR.Plane.Regulator\_1p05v



### TPS51716 for 1D05V\_S0



36.37 1D05V\_S0\_PWRGD <<  
48 IMVP\_PWRGD <<  
SA 20140418



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-2)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

No eMMC

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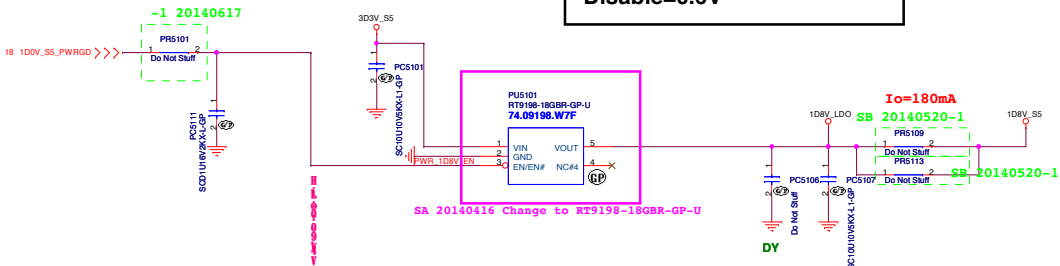
Title: **DC to DC 1D05V(RT8231A)**

Size: Custom Document Number: **EA51 BM** Rev: -1

Date: 1/26/2014, July 06, 2014 Sheet 50 of 102

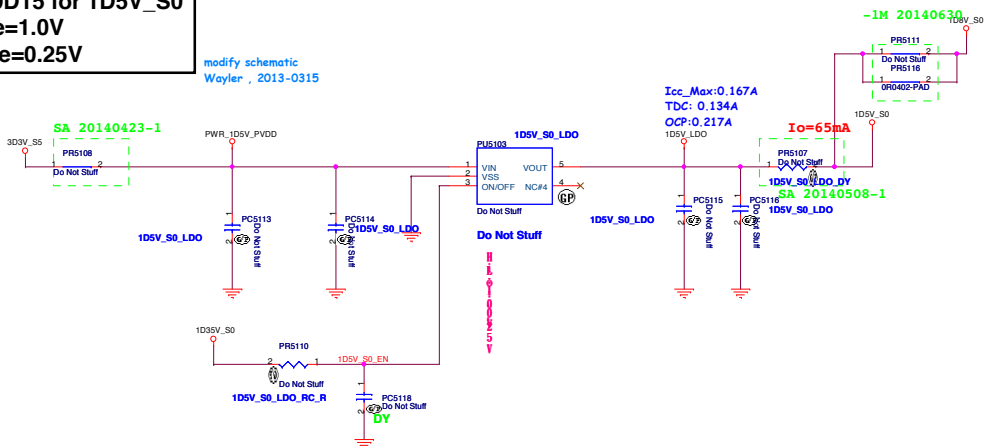
**SSID = PWR.Plane.Regulator\_1p8v**

**TLV70218DBVR for 1D8V\_S5**  
 Enable=0.9V  
 Disable=0.6V



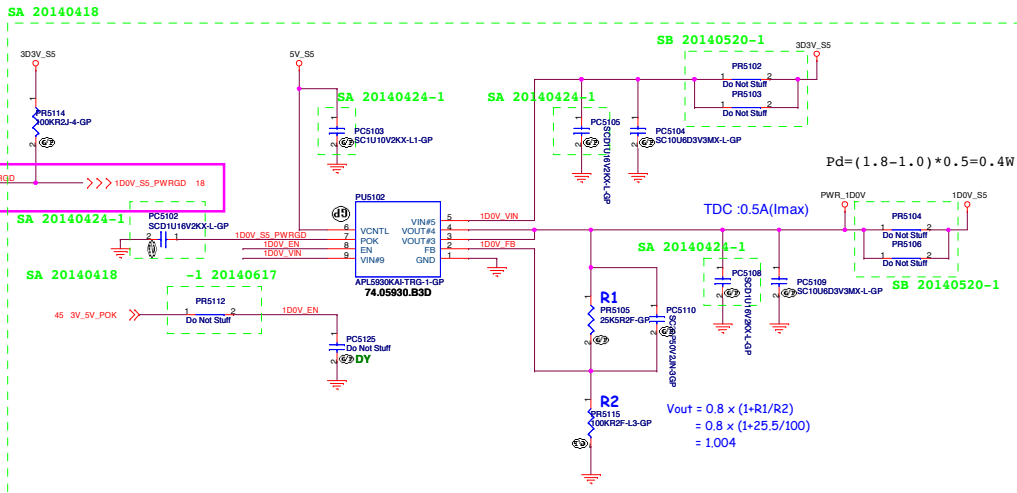
**S-1339D15 for 1D5V\_S0**  
 Enable=1.0V  
 Disable=0.25V

modify schematic  
 Wayler, 2013-0315



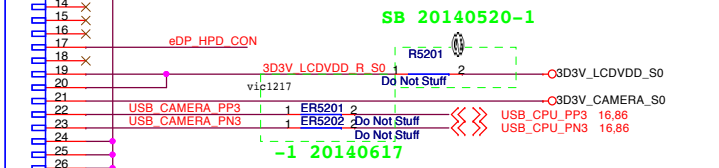
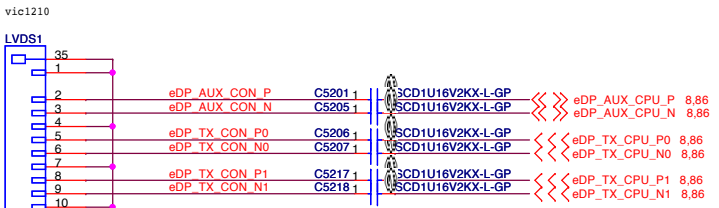
**20140418 Change to LDO**

**APL5930 for 1D0V\_S5**  
 Enable=1.1V  
 Disable=0.5V



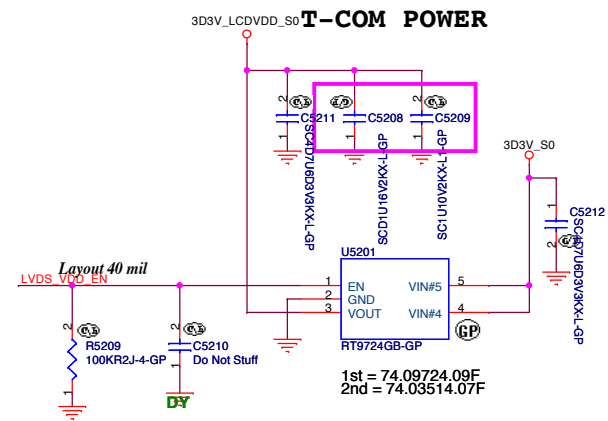
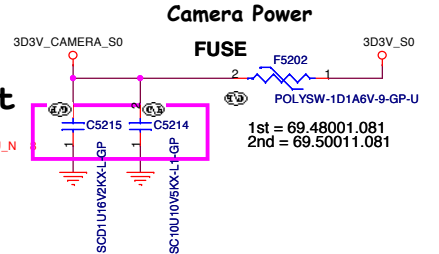
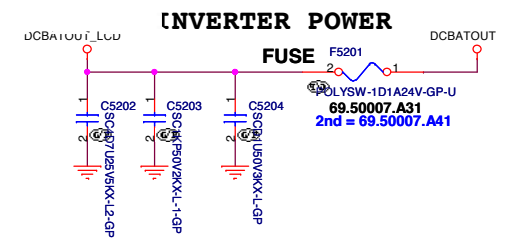
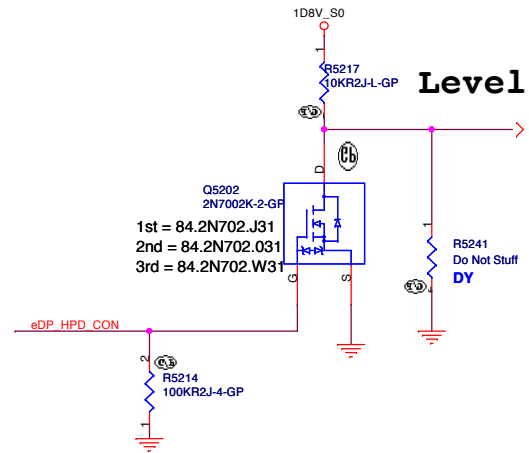
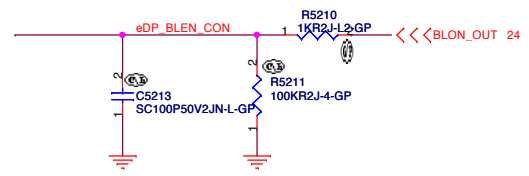
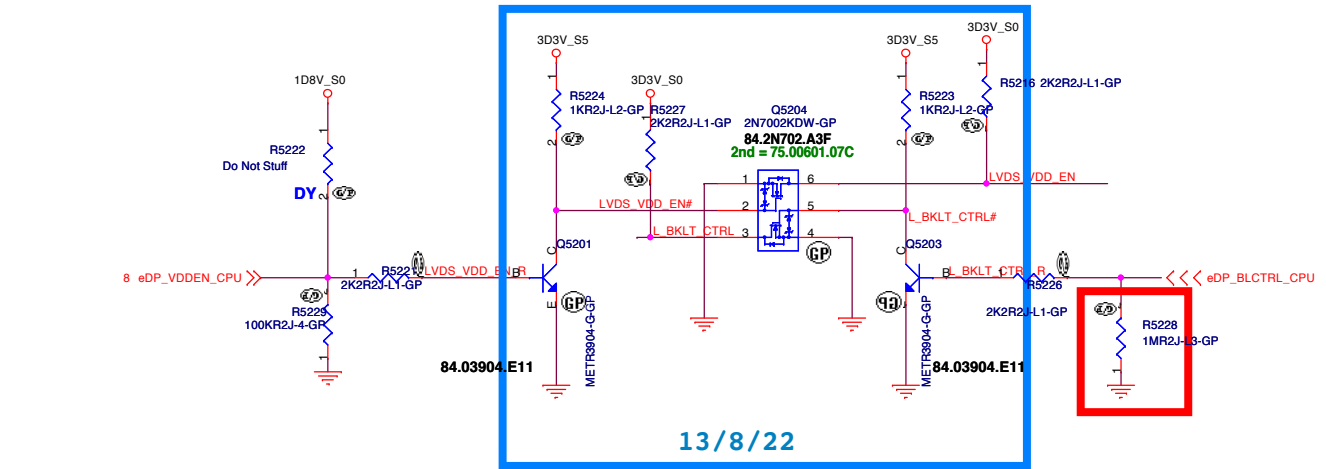
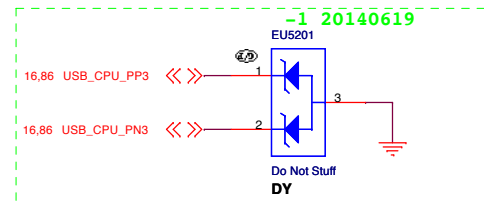
No eMMC

**SSID = VIDEO**



STAR-CONN-1-GP-U1  
 1st = 20.K0809.034  
 2nd = 20.K0678.034

**EDP connector**



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<p>File <b>EDP Connector</b></p>		
Size A3	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 52 of	102

5

4

3

2

1

D

D

C

C

B

B

A

A

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Title		
<b>CRT Board Connector</b>		
Size	Document Number	Rev
A3	<b>EA30 BM</b>	<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 53 of 102

5

4

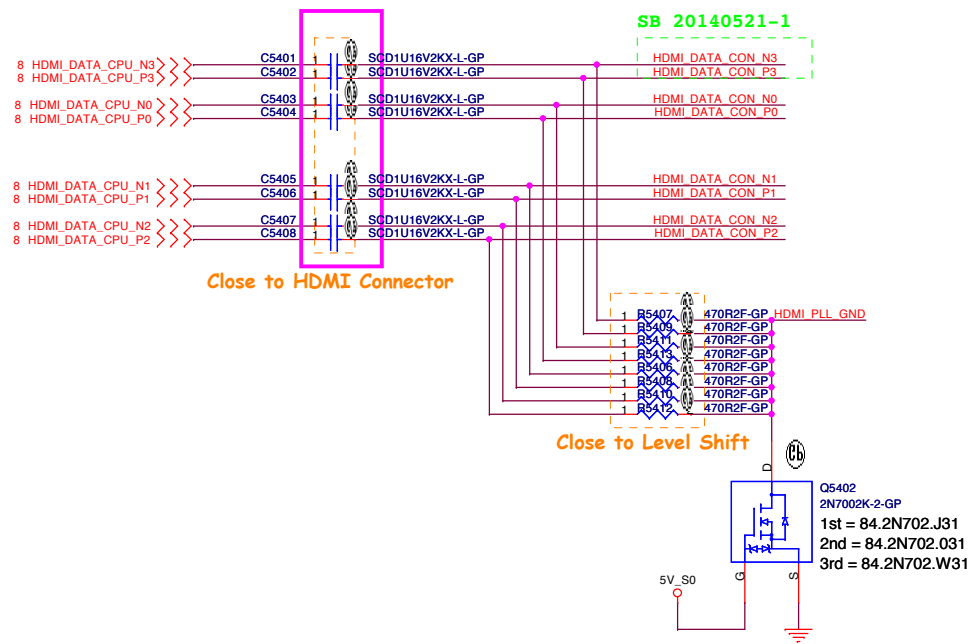
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2

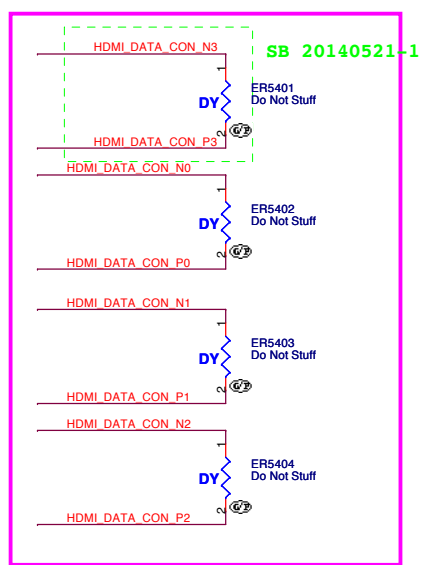
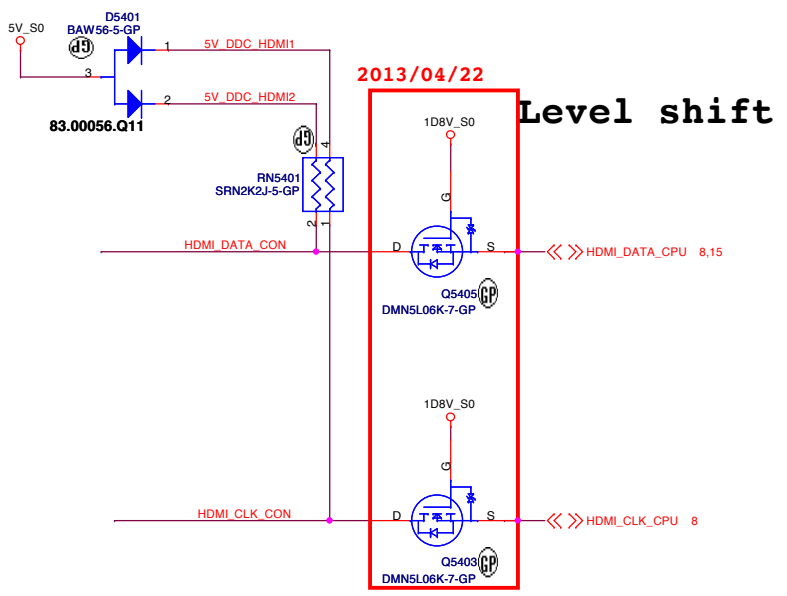
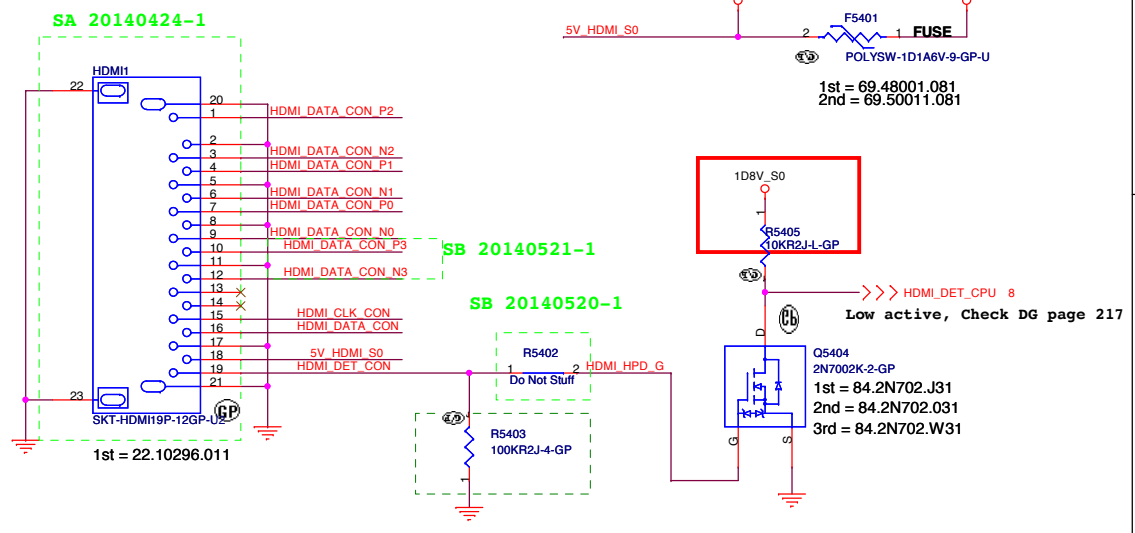
1

**SSID = VIDEO**

# HDMI Level Shifter & CONNECTOR



## HDMI CONN



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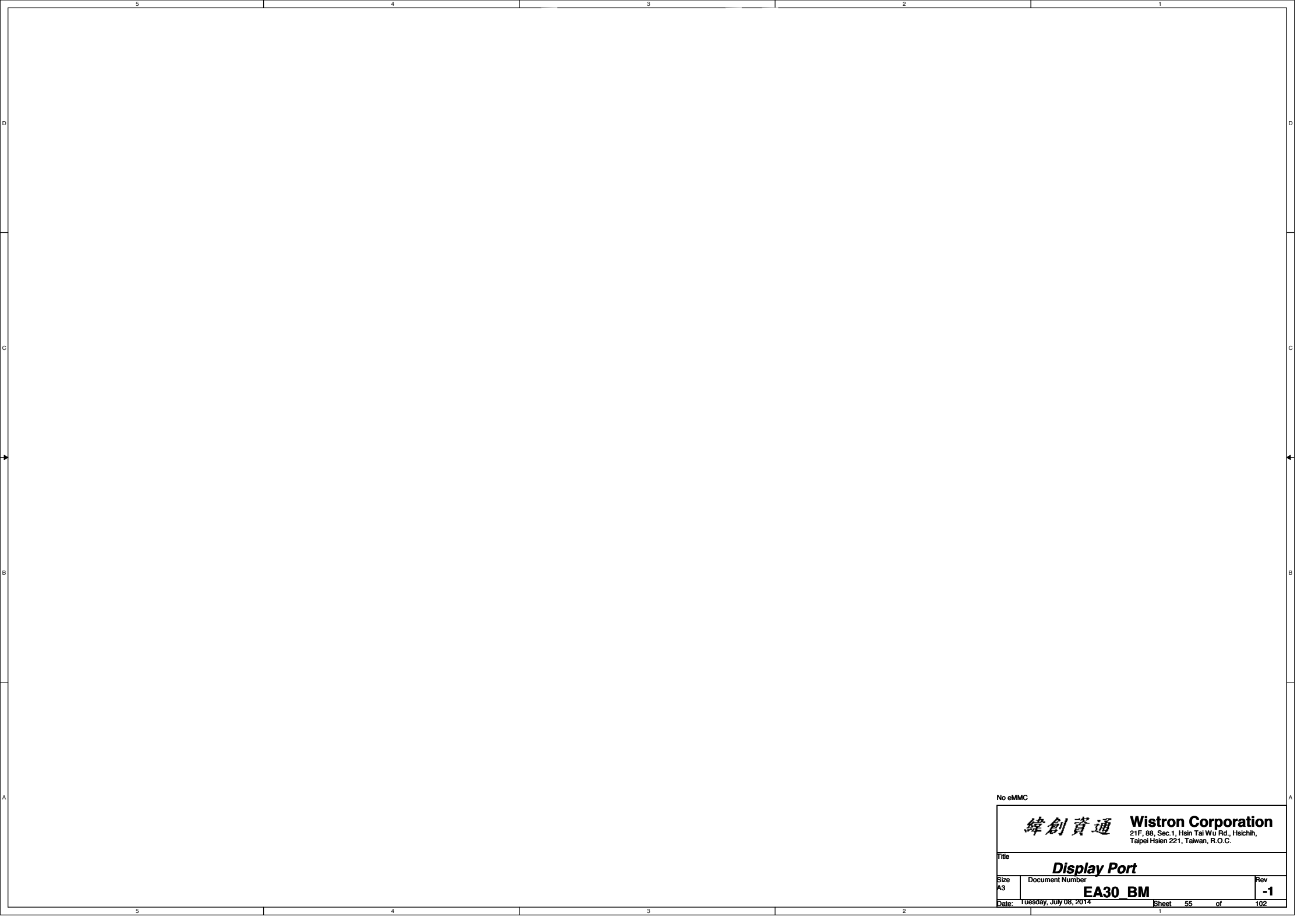
No eMMC

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Title: **HDMI Level Shifter/Connector**

Size A3 Document Number: **EA30 BM** Rev: **-1**

Date: Tuesday, July 08, 2014 Sheet 54 of 102



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Display Port**

Size

A3

Document Number

**EA30 BM**

Rev

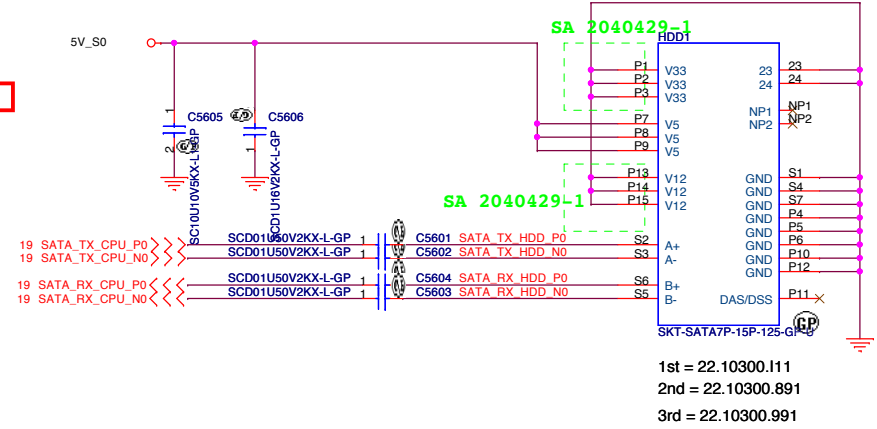
**-1**

Date: **Tuesday, July 08, 2014**

Sheet **55** of **102**

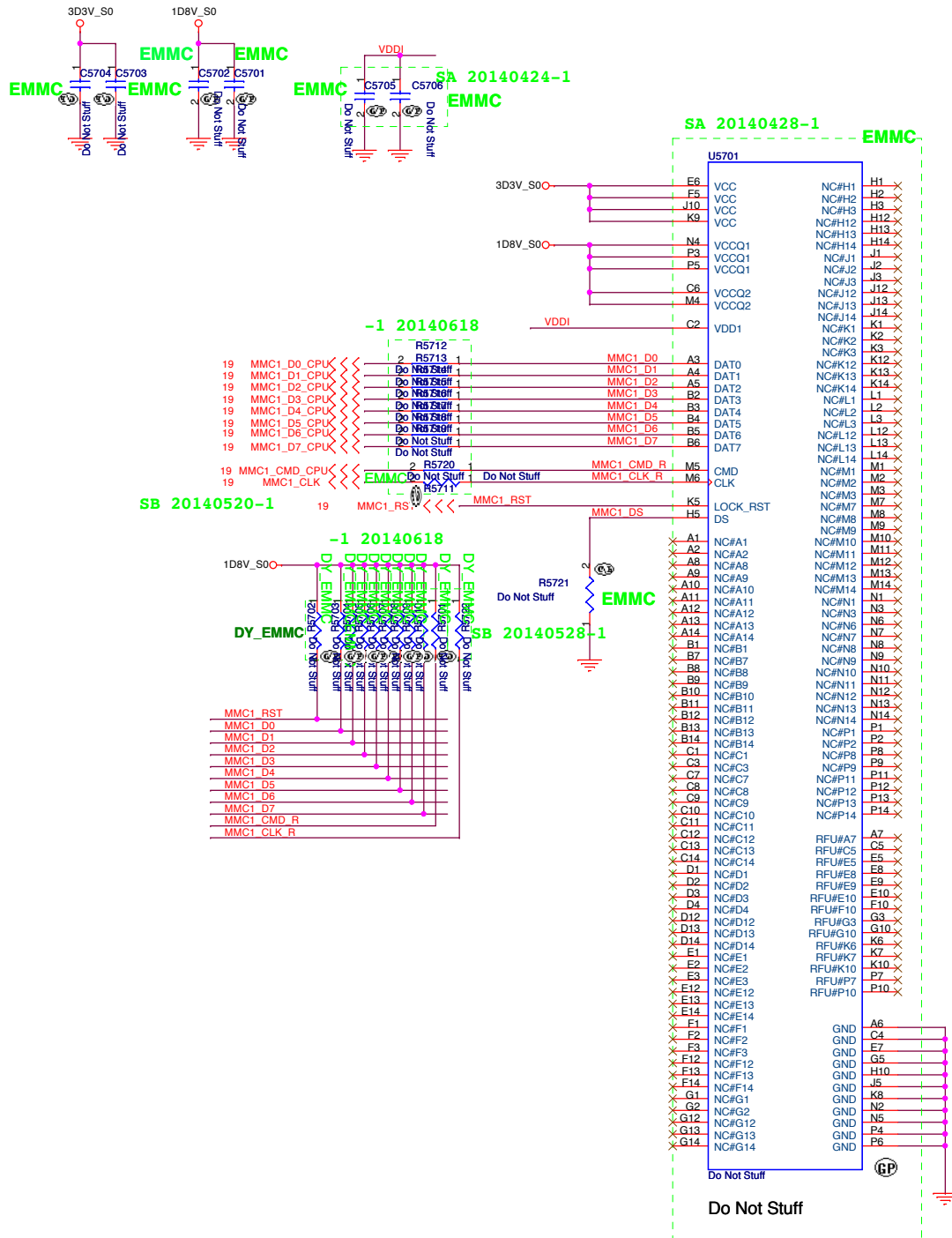
**SSID = SATA**

# SATA HDD Connector



AC coupling caps near connector < 100 mils

No eMMC



No eMMC

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Title		
<b>eMMC</b>		
Size	Document Number	Rev
A3	<b>EA30 BM</b>	<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 57 of 102



**SSID = Wireless**

# *Mini Card Connector(mSATA)*

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Title

**WWAN CONN**

Size

A4

Document Number

**EA30 BM**

Rev

**-1**

Date: Tuesday, July 08, 2014

Sheet 59 of 102

SSID = mSATA

# Mini Card Connector(mSATA)

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Title

**mSATA Connector**

Size

A4

Document Number

**EA30 BM**

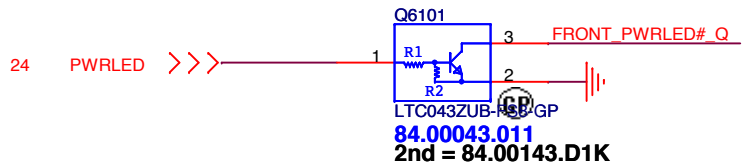
Rev

**-1**

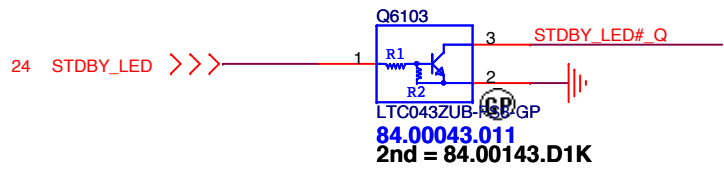
Date: Tuesday, July 08, 2014

Sheet 60 of 102

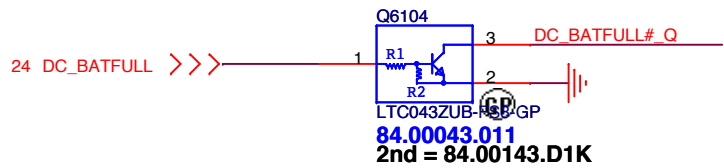
### Power button\_LED



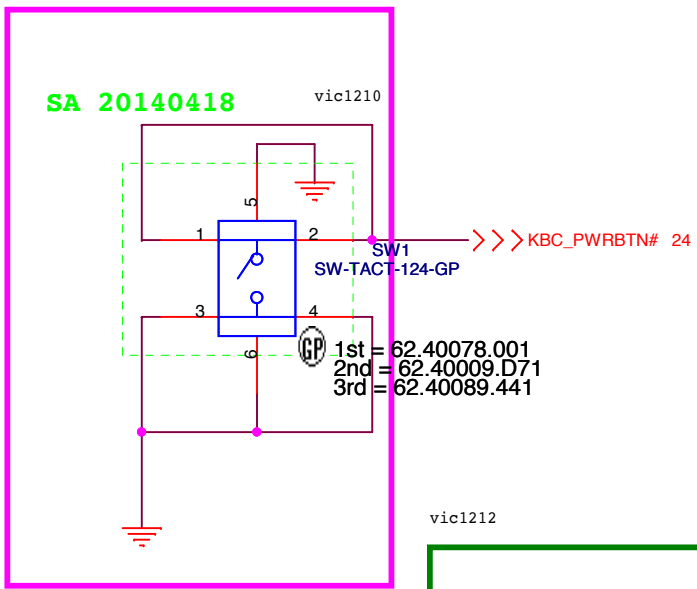
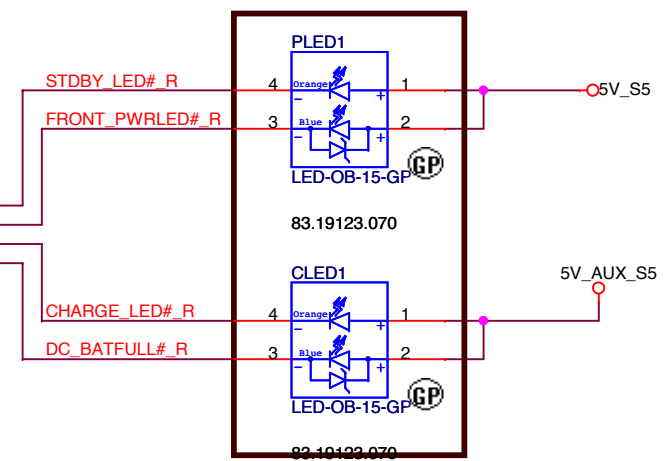
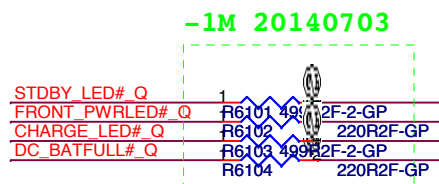
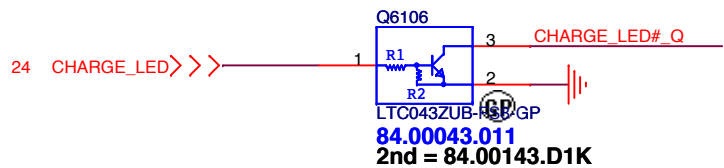
### Power STDBY\_LED



### Battery LED2 (DC\_BATFULL)



### Battery LED1 (CHARGE)



No eMMC

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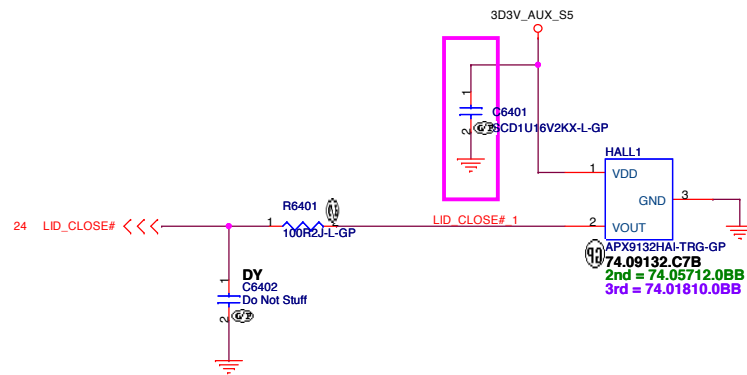
Title <b>LED Bard/Power Button</b>		
Size A4	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 61	of 102



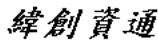
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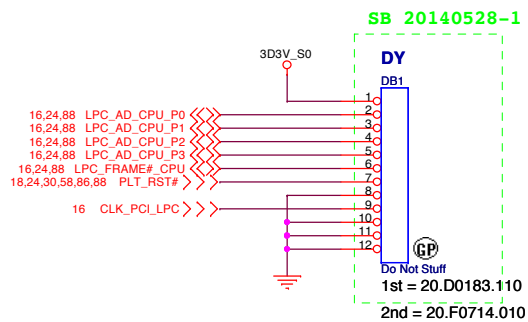
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Title		
<b>IO Board Connector</b>		
Size	Document Number	Rev
A3	<b>EA30 BM</b>	<b>-1</b>
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<b>Hall Sensor</b>		
Size A3	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 64 of 102	



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Title		
<b>Dubug connector</b>		
Size	Document Number	Rev
A3	<b>EA30 BM</b>	<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 65 of 102

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Title			
<b>SENSOR HUB</b>			
Size	Document Number	Rev	
A3	<b>EA30 BM</b>	<b>-1</b>	
Date:	Tuesday, July 08, 2014	Sheet	66 of 102

# Free Fall Sensor

## Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

**SDO="H"; address="3Ah"**  
**\*SDO="L"; address="38h"**

**\*CS="H"; mode="I2C"**  
**CS="L"; mode="SPI"**

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Title

**G Sensor**

Size

Document Number

Rev

A

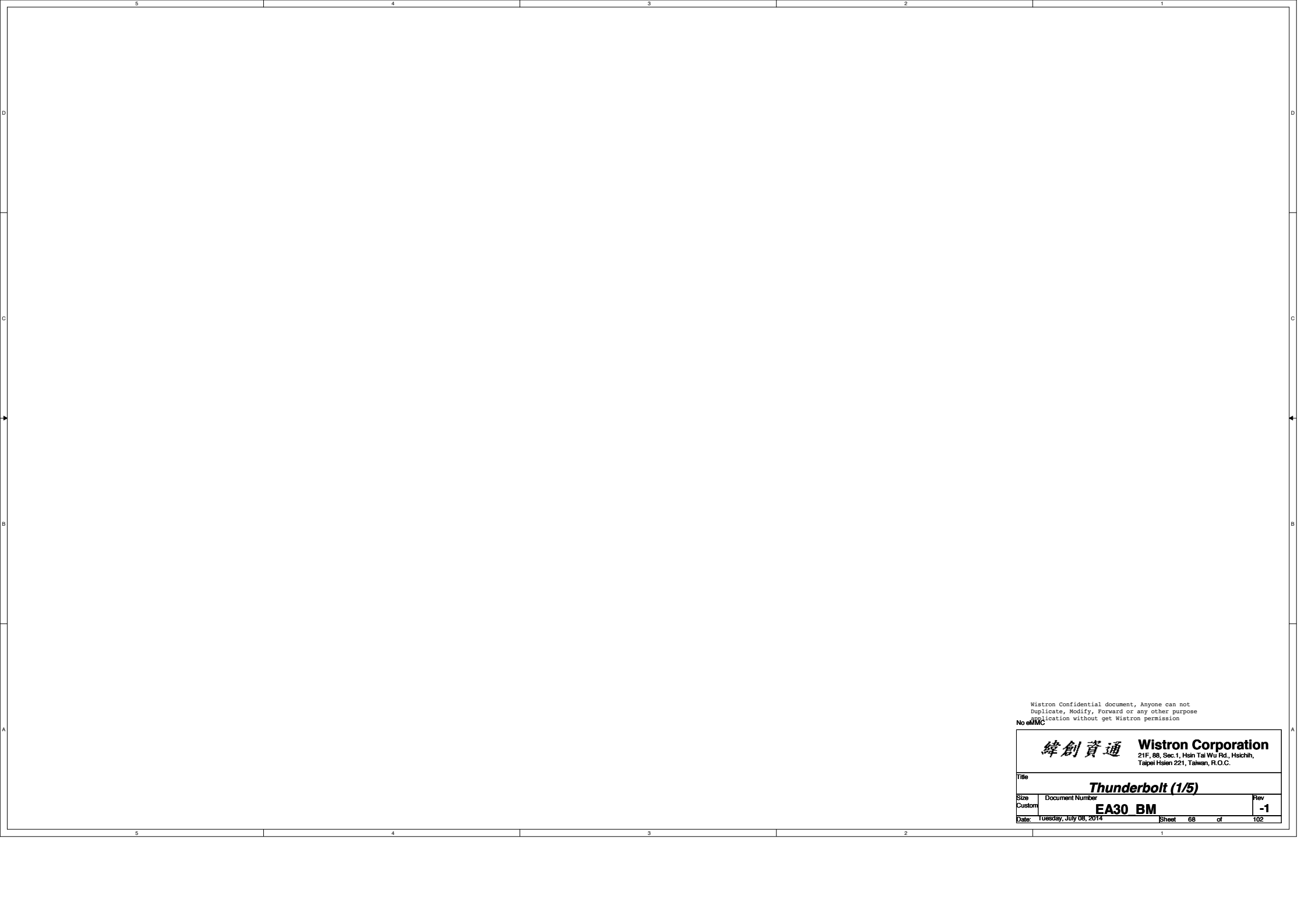
**EA30 BM**

**-1**

Date: Tuesday, July 08, 2014

Sheet 67 of

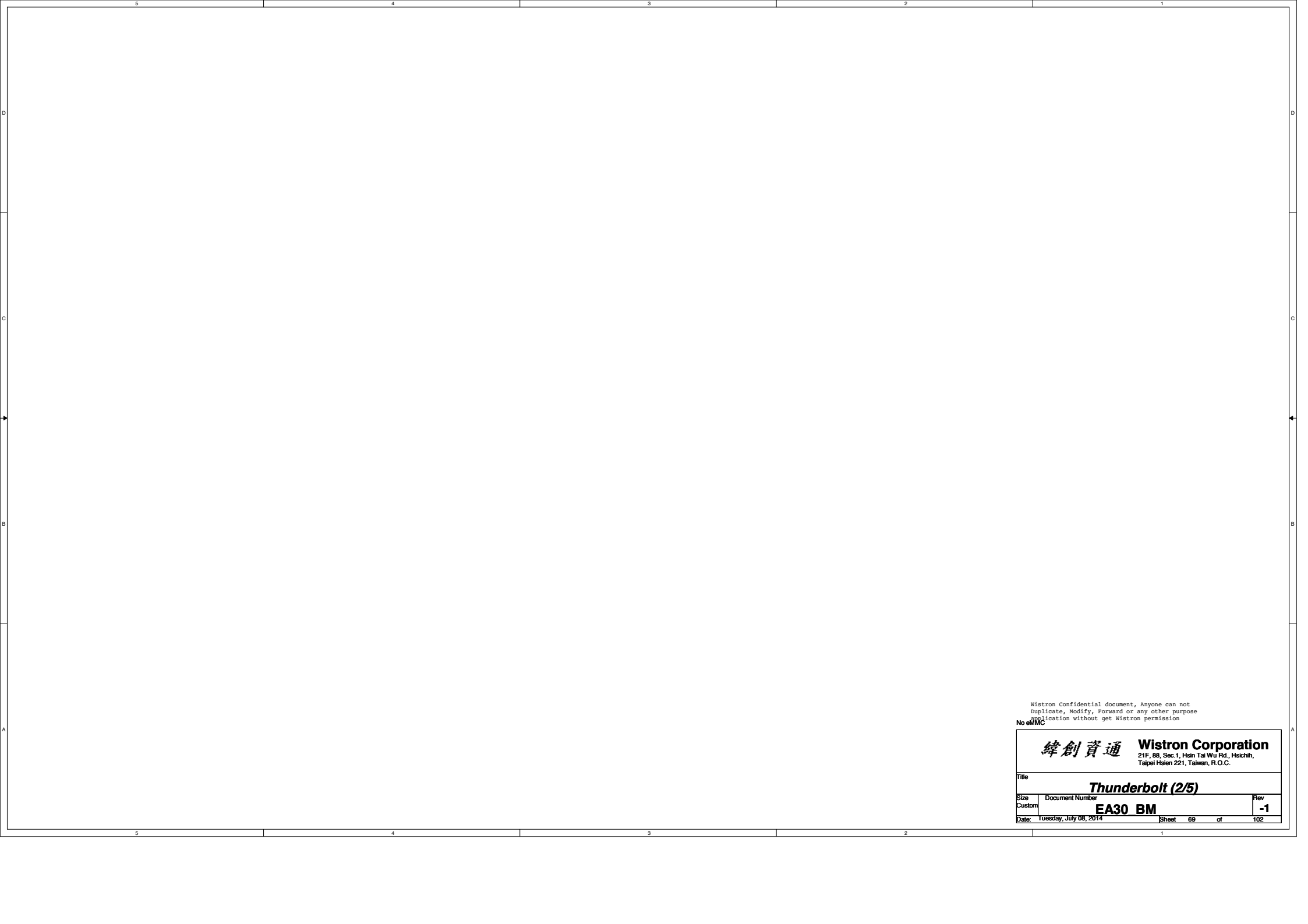
102



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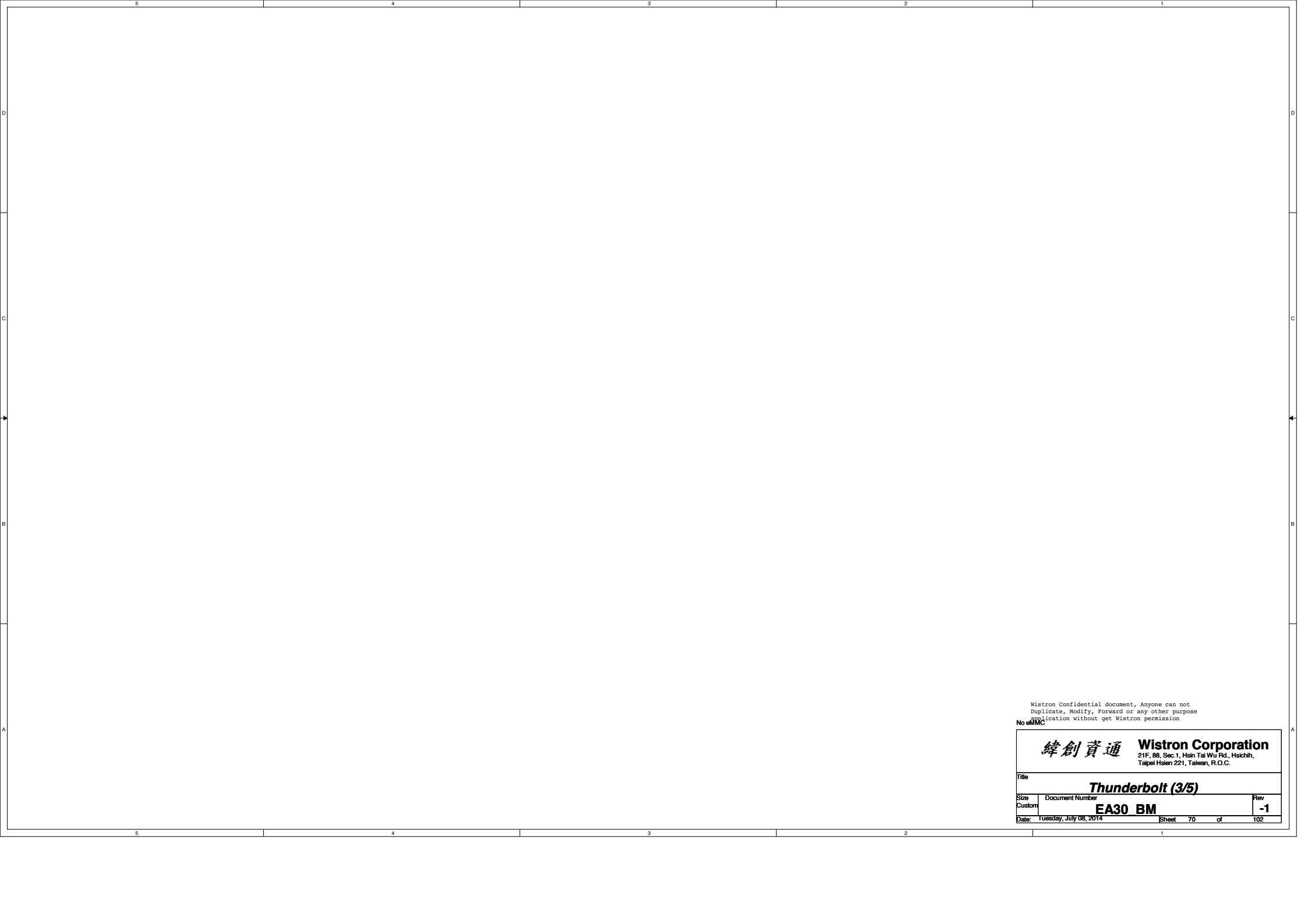
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<b>Title</b>			
<b>Thunderbolt (1/5)</b>			
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	
Custom	<b>EA30 BM</b>	<b>-1</b>	
<b>Date:</b>	Tuesday, July 08, 2014	<b>Sheet</b>	68 of 102



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<b>Title</b>			
<b>Thunderbolt (2/5)</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
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<b>Date:</b>	Tuesday, July 08, 2014	<b>Sheet</b>	<b>69 of 102</b>



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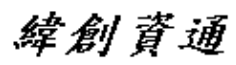
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Title			<b>Thunderbolt (3/5)</b>
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Custom	<b>EA30 BM</b>	<b>-1</b>	
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<b>Title</b> <i><b>Thunderbolt (5/5)</b></i>			
<b>Size</b> A4	<b>Document Number</b> <b>EA30 BM</b>		<b>Rev</b> <b>-1</b>
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Sheet 72		of 102	

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Title		GPU(PEG)	
Size	Document Number	Rev	
Custom	EA30 BM	-1	
Date:	Thursday, July 03, 2014	Sheet	73 of 102

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Title		
<b>GPU (DIGITALOUT)</b>		
Size	Document Number	Rev
Custom	<b>EA30 BM</b>	<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 74 of 102

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Title

**GPU (VRAM VF)**

Size A2 Document Number Row

**EA30 BM** -1

Date: Tuesday, July 08, 2014 Sheet 75 of 102

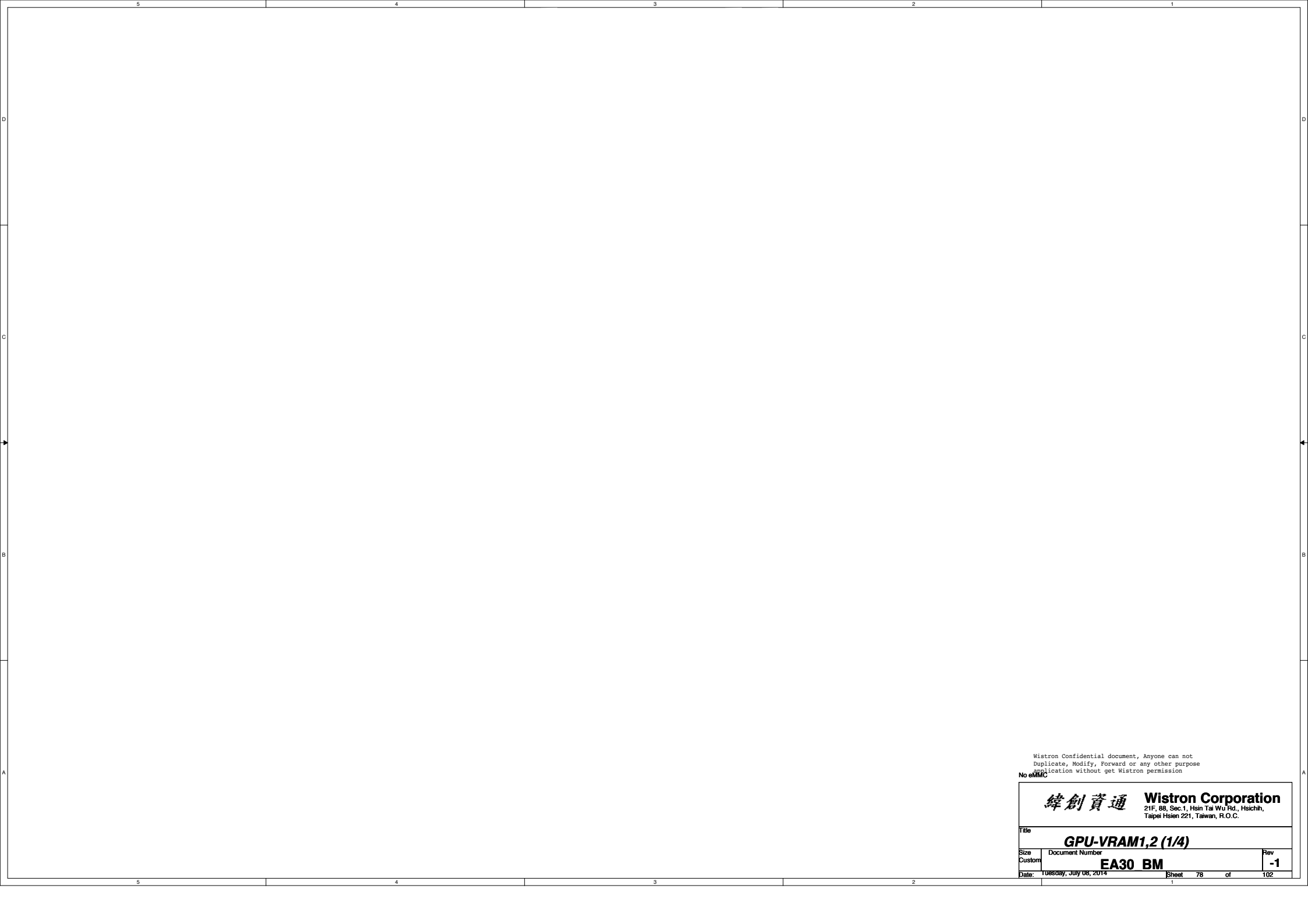
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<b>GPU (GPIO/STRAP)</b>			
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000000	EA30 BM	-1	
DATE: 2009/04/06 09:11		DESIGNER: CH	CHK: CH

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<b>GPU (POWER/GND)</b>			
Title			Rev
Size	Document Number		
Customer	<b>EA30 BM</b>	<b>-1</b>	
Date	1050505, July 05, 2014	Sheet	77 of 102



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Title			
<b>GPU-VRAM1,2 (1/4)</b>			
Size	Document Number		Rev
Custom	<b>EA30 BM</b>		<b>-1</b>
Date:	Tuesday, July 08, 2014		Sheet 78 of 102

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Title		
<b>GPU-VRAM3,4 (2/4)</b>		
Size	Document Number	Rev
Custom	<b>EA30 BM</b>	<b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 79	of 102

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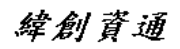
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<b>Title</b> <b>GPU-VRAM5,6 (3/4)</b>			
<b>Size</b> Custom	<b>Document Number</b> <b>EA30 BM</b>		<b>Rev</b> -1
<b>Date:</b> Tuesday, July 08, 2014		<b>Sheet</b> 80	<b>of</b> 102

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Title		
<b>GPU-VRAM7,8 (4/4)</b>		
Size	Document Number	Rev
Custom	<b>EA30 BM</b>	<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 81 of 102

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Title		
<b>RT8812A VGA CORE</b>		
Size	Document Number	Rev
Custom	<b>EA30 BM</b>	<b>-1</b>
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<b>DISCRETE VGA POWER</b>			
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Serial	<b>EA30 BM</b>		<b>-1</b>
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Title

**Switchable GFX LCD(1/2)**

Size

A4

Document Number

**EA30 BM**

Rev

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Title

**Switchable GFX LCD(2/2)**

Size

A4

Document Number

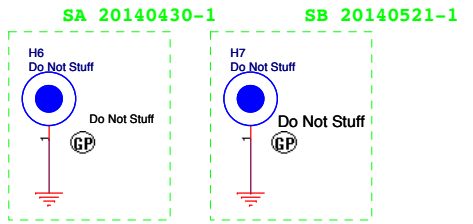
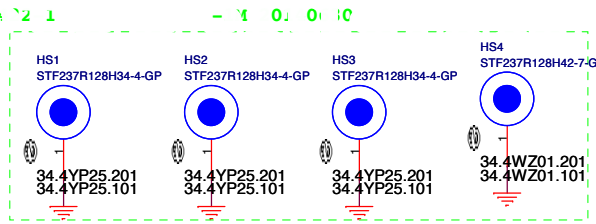
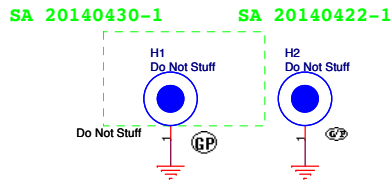
**EA30 BM**

Rev

**-1**

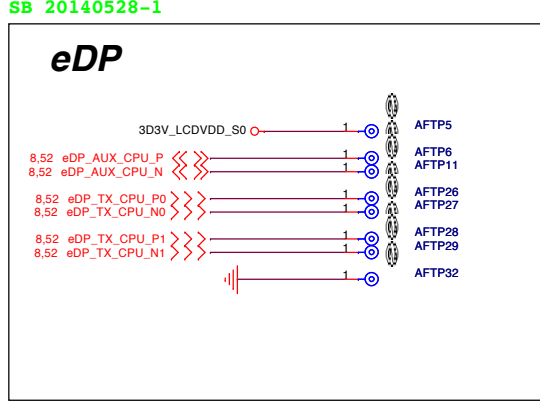
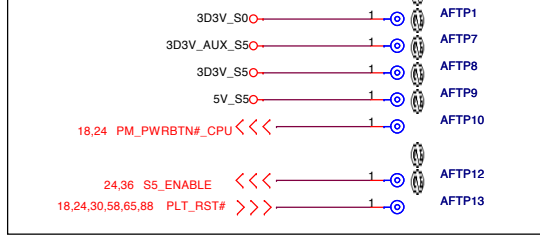
Date: Tuesday, July 08, 2014

Sheet 85 of 102

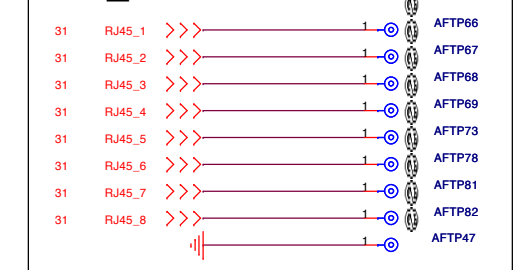


### Check test point

Test Point放在 Bottom side 可量測處



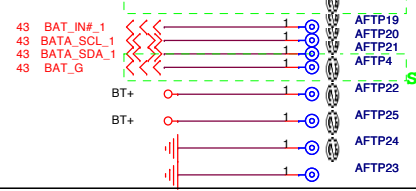
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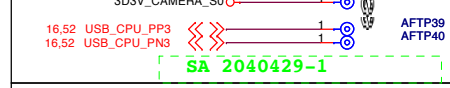
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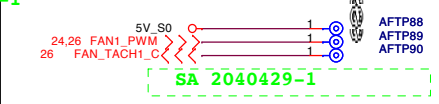
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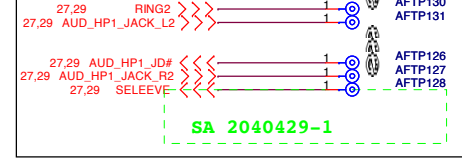
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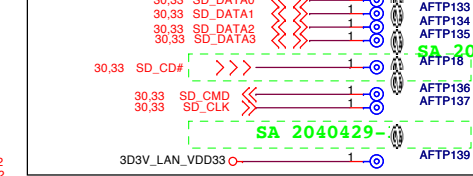
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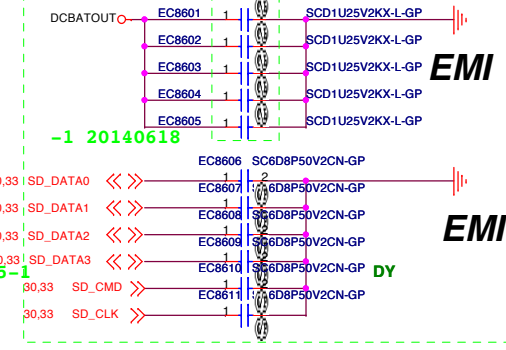
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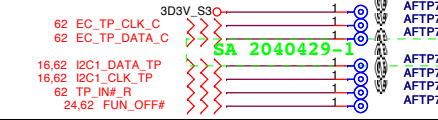
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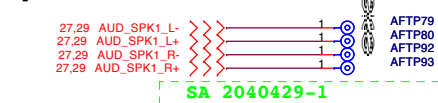
### SA 20140502-3



### Touch PAD



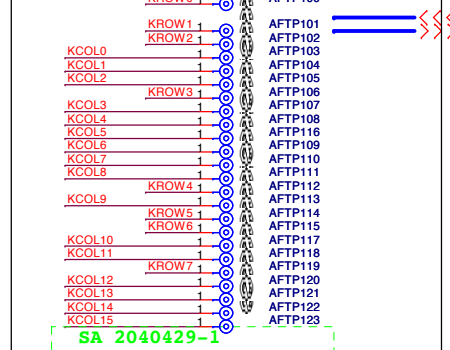
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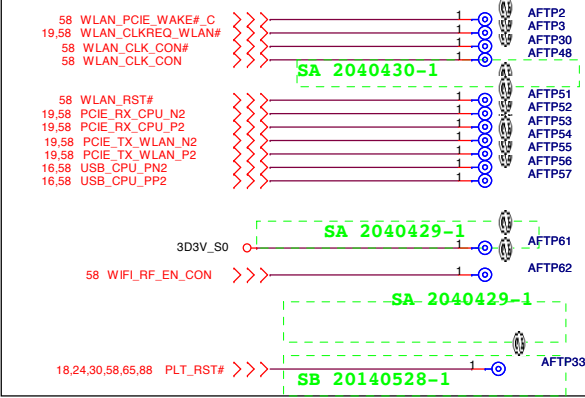
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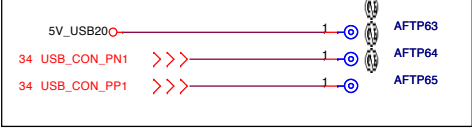
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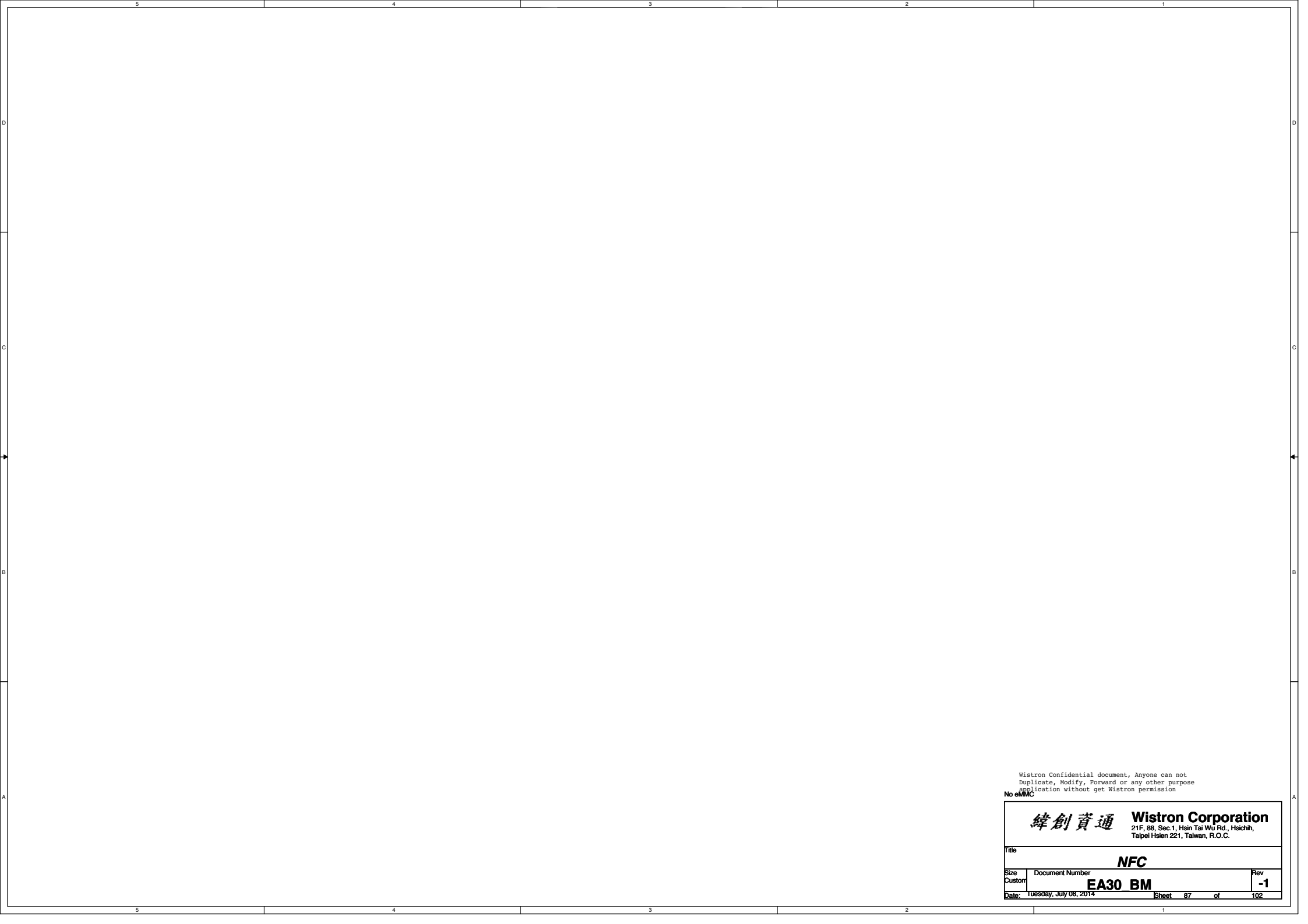
### WLAN



### USB2



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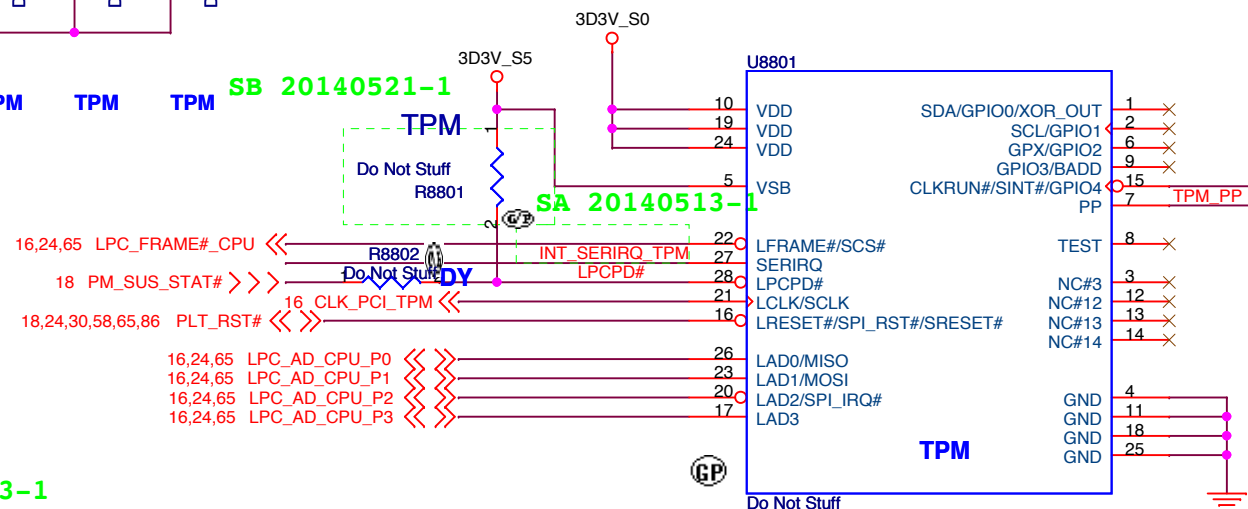
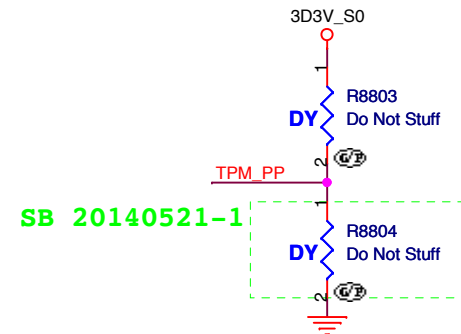
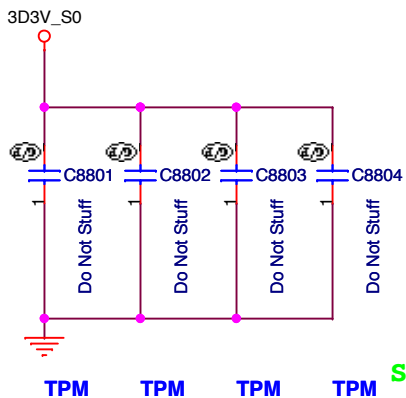


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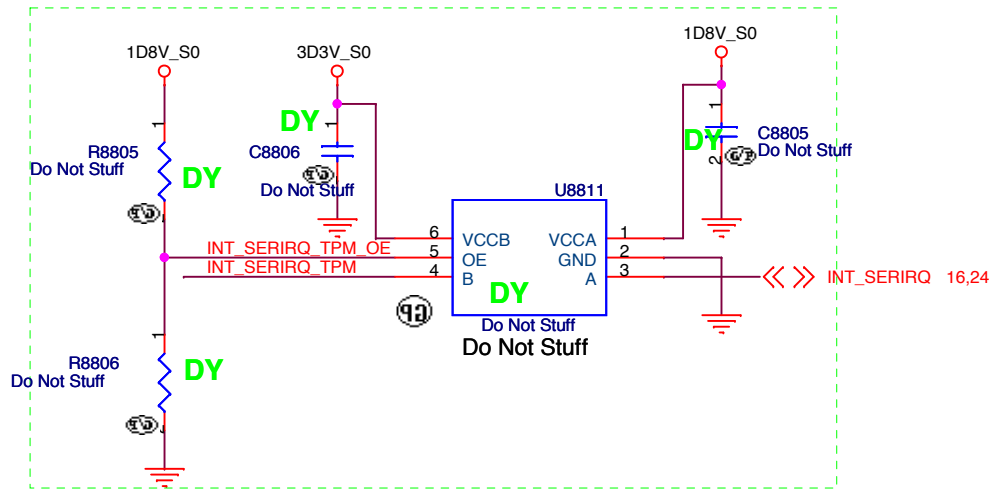
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Size	Document Number	Rev	
Custom	<b>EA30 BM</b>	<b>-1</b>	
Date:	Tuesday, July 08, 2014	Sheet	87 of 102



SB 20140513-1



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Size	Document Number	Rev
A4	<b>EA30 BM</b>	<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 88 of 102

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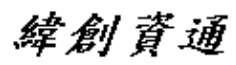
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<b>Size</b> A4	<b>Document Number</b> <b>EA30 BM</b>	<b>Rev</b> -1	
<b>Date:</b> Tuesday, July 08, 2014		Sheet 89 of	102

D

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Title **Express Card**

Size A	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
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Date: Tuesday, July 08, 2014 Sheet 90 of 102

D

D

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C

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Title **Smart Card socket**

Size A	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
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Title **Switchable GFX eDP**

Size A	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
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Title **Bottom Docking**

Size A	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
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Date: Tuesday, July 08, 2014 Sheet 93 of 102

	A	B	C	D	E
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<b>Inter LAN WG1217LM</b>			
Size A3	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet	94	of 102

D

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Title

**LAN Switch**

Size

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Document Number

**EA30 BM**

Rev

**-1**

Date: Tuesday, July 08, 2014

Sheet 95 of 102

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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<b>Title</b>			
<b>PCH_XDP</b>			
Size	Document Number	Rev	
A4	<b>EA30 BM</b>	<b>-1</b>	
Date:	Tuesday, July 08, 2014	Sheet	96 of 102

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Title		
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Size A4	Document Number <b>EA30 BM</b>	Rev <b>-1</b>
Date: Tuesday, July 08, 2014	Sheet 97 of	102

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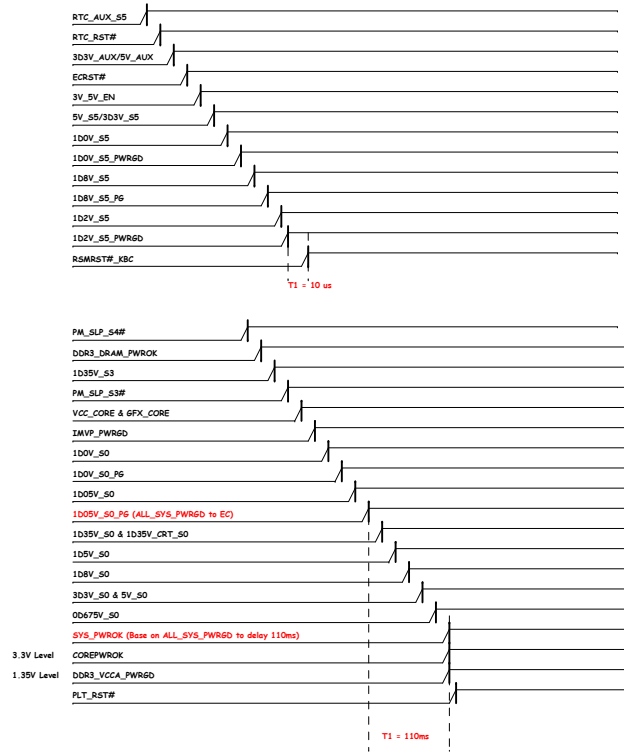
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Title

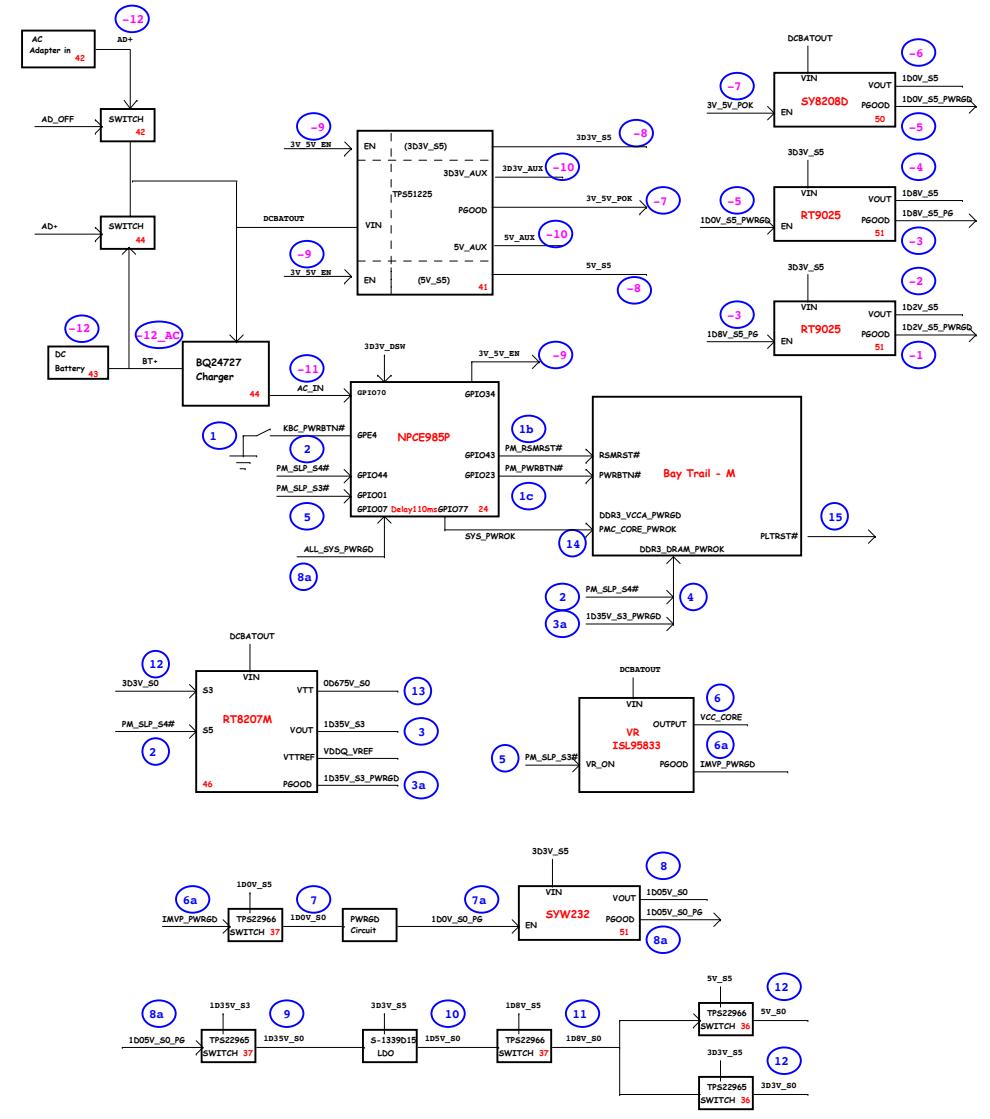
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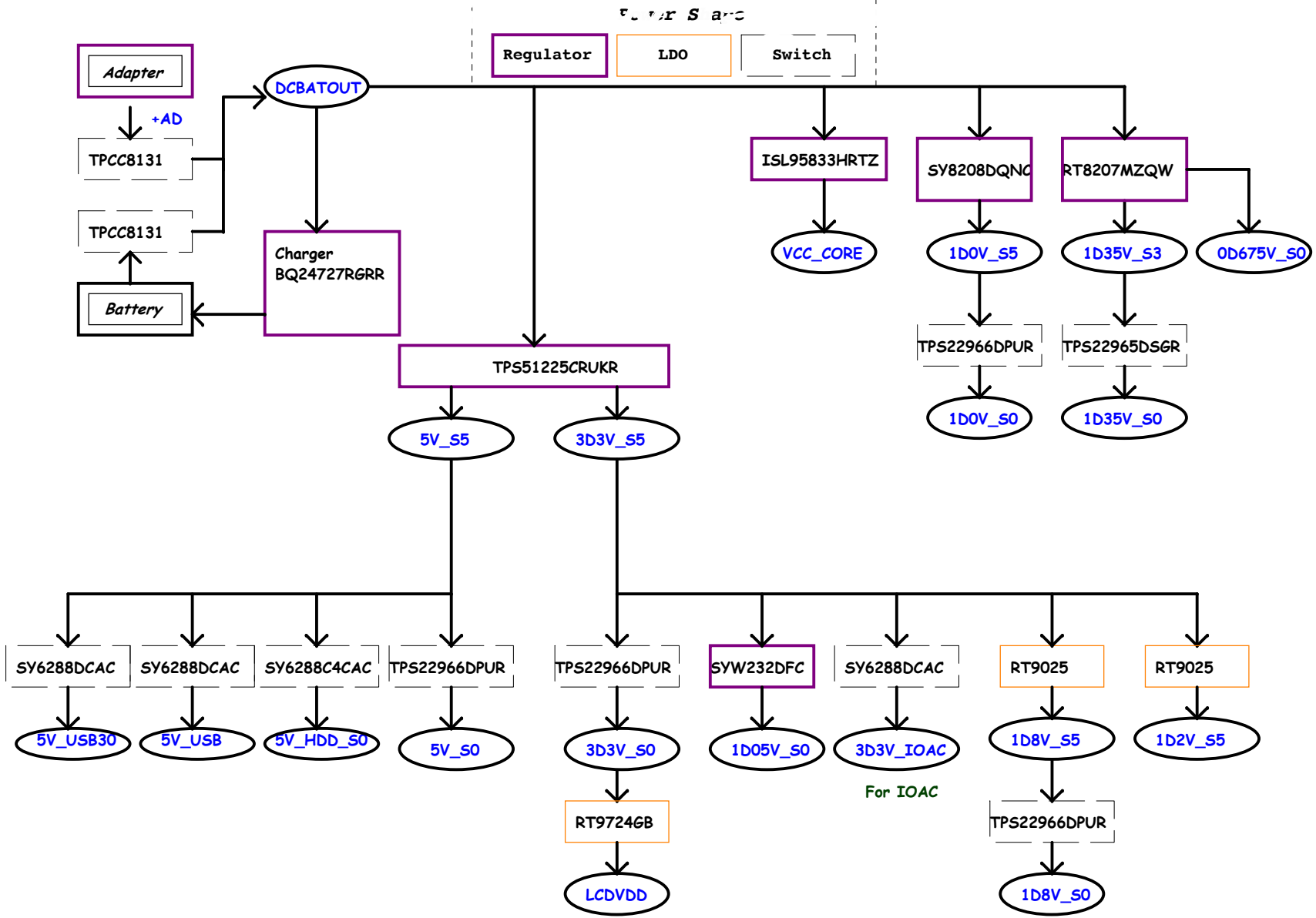
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# Intel-Power Up Sequence with non-S0ix

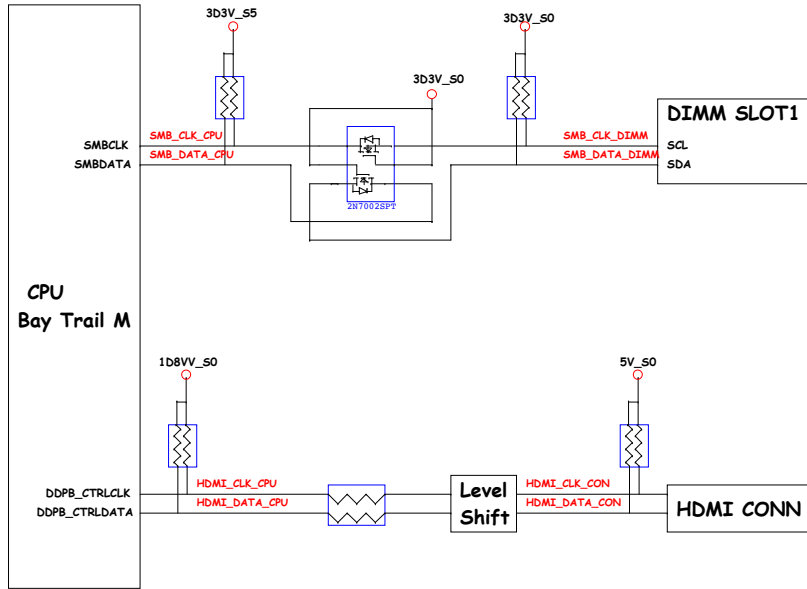


# Bay Trail - M POWER UP SEQUENCE DIAGRAM

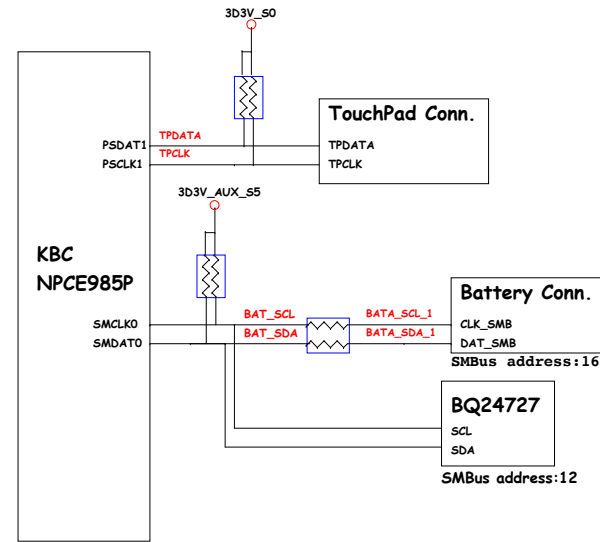




# PCH SMBus Block Diagram



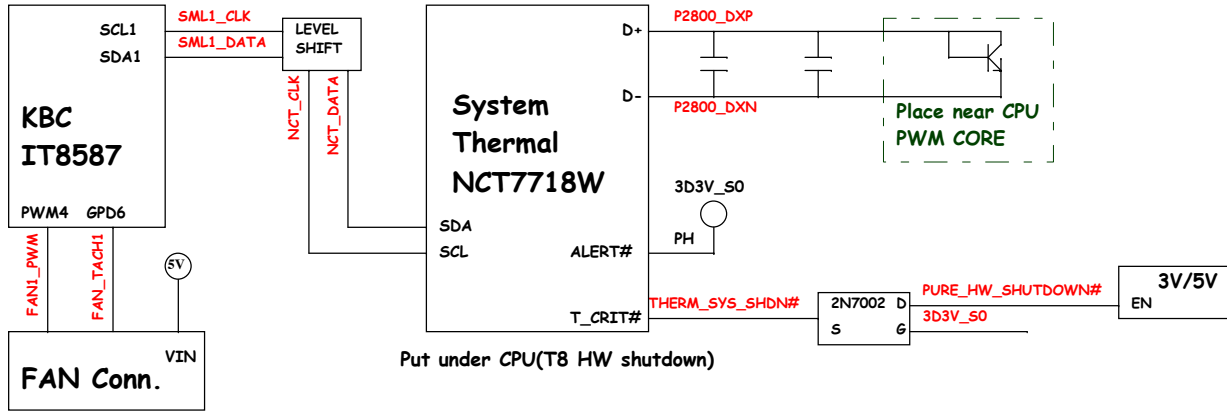
# KBC SMBus Block Diagram



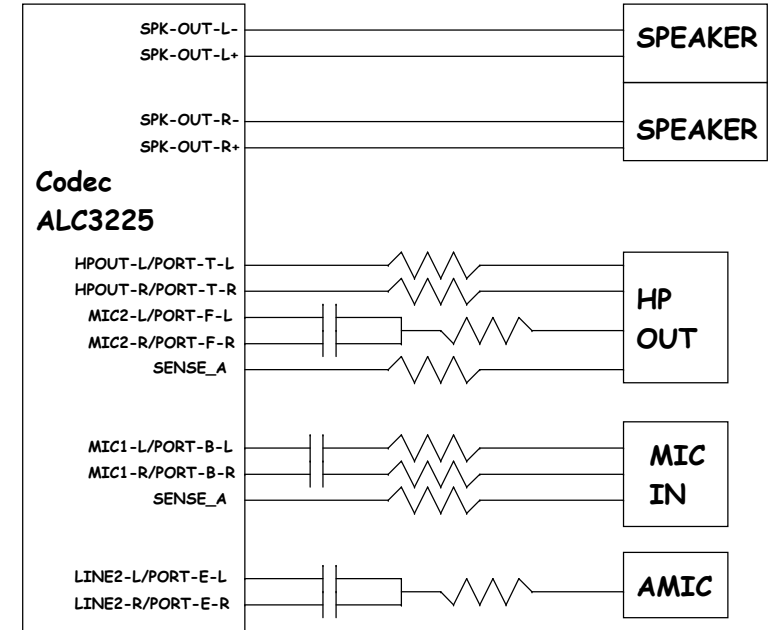
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No eMMC

# Thermal Block Diagram



# Audio Block Diagram



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