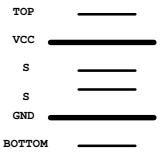
HM42-DN Block Diagram

Project code: 91.4HD01.001
PCB P/N : 48.4GX01.0SA
PCB 版號 : 09919 SA
REVISION : PCB STACKUP



DDR3 16,17 — 800/1066/1333MHz
DDR3 800/1066/1333 MHz 16,17 — 800/1066/1333MHz
AMD Champlain CPU S1G4 (45W)
638-Pin uFCPGA638 4,5,6,7
OUT / IN — HT 3.0 16X16
CRT 20
LCD 19
HDMI 21
CLK GEN. 3
ICS9LPRS480BKLFT 71.09480.A03
RTM880N-796-VB-GRT 71.00880.A03
North Bridge
AMD RS880M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
8,9,10
16X — PCI EXPRESS GRAPHIC
Madison ATI 53,54,55,56,57
DDR3 VRAM 58, 59, 60, 61
LAN Giga LAN BCM57780 26
TXFM 27
RJ45 27
INT MIC 30
Codec ALC272 28
AZALIA
A-Link 4X1
PCIex1
Mini Card WLAN 33
MIC In 30
INT.SPKR 30
OP AMP 29
Line Out
30
South Bridge
AMD SB820
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
11,12,13,14,15
LPC BUS
KBC Novoton NPCE781B 36
BIOS MXIC MX25L1605 37
LPC DEBUG CONN 37
Touch Pad 38
INT. KB 36
SATA
USB
CardReader AU6433 32
MS/MS Pro/xD /MMC/SD 5 in 1 32
HDD SATA 22
ODD SATA 23
Mini USB Blue Tooth 24
USB 3 Port 25
Camera
Daughter Board USB Board
Daughter Board PWR+LED Board

SYSTEM DC/DC RT8223 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5 (5.5A) 3D3V_S5 (5A)

SYSTEM DC/DC RT8209E 47

5V_S5	1D5V_S3 (14A)

RT9026 47

5V_S5	0D75_S3 (1.2A)

SYSTEM DC/DC RT8209E 48

INPUTS	
DCBATOUT	1D1V_S0 (11A)

RT9025 48

3D3V_S5	1D1V_S5 (1.4A)

RT9025 49

5V_S5	1D1V_VGA

RT9161 49

3D3V_S0	2D5V_S0 (200mA)

RT9025 49

1D5V_S3	1D05V_S0 (1.4A)

CHARGER BQ24745 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JE40-DN | Rev: -3
Date: Friday, March 26, 2010 | Sheet 1 of 63

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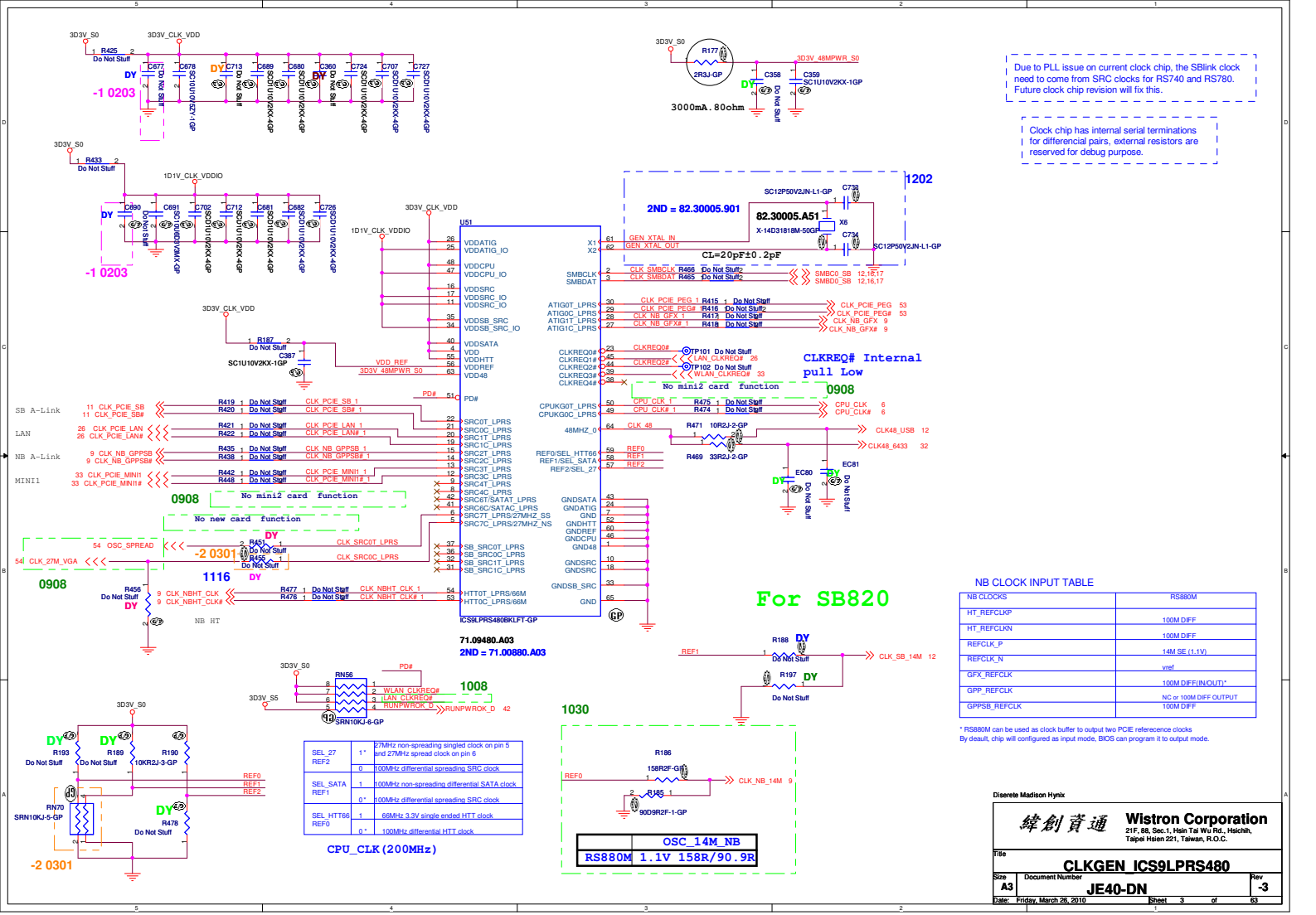
Taipei Hsien 221, Taiwan, R.O.C.

Title: **History**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 2 of 63


3D3V_S0
3D3V_CLK_VDD
R425 Do Not Stuff
C677 C678 C713 C689 C680 C360 C724 C707 C727
DY
-1 0203
SC1U10V2KX-1GP
SC1U10V2KX-4GP
R177
2R3J-GP
3D3V_48MPWR_S0
C358
C359
SC1U10V2KX-1GP
3000mA.80ohm
R433 Do Not Stuff
1D1V_CLK_VDDIO
C690 C691 C702 C712 C681 C682 C726
SC1U10V2KX-4GP
SC1U6D3V2MX-GP
U51
ICS9LPRS480BKLFT-GP
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
PD#
X1
X2
GEN_XTAL_IN
GEN_XTAL_OUT
CL=20pF±0.2pF
2ND = 82.30005.901
82.30005.A51
X-14D31818M-50GP
X8
C732
C734
SC12P50V2JN-L1-GP
1202
SMBCLK
SMBDAT
CLK_SMBCLK R466 Do Not Stuff2
CLK_SMBDAT R465 Do Not Stuff2
SMBC0_SB 12,16,17
SMBD0_SB 12,16,17
R187 Do Not Stuff
C387
SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_PCIE_PEG_1 R415 Do Not Stuff
CLK_PCIE_PEG# R416 Do Not Stuff2
CLK_NB_GFX_1 R417 Do Not Stuff
CLK_NB_GFX#_1 R418 Do Not Stuff
CLK_PCIE_PEG 53
CLK_PCIE_PEG# 53
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP101 Do Not Stuff
LAN_CLKREQ# 26
TP102 Do Not Stuff
WLAN_CLKREQ# 33
CLKREQ# Internal pull Low
No mini2 card function
0908
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK_1 R475 Do Not Stuff
CPU_CLK#_1 R474 Do Not Stuff
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
R471 10R2J-2-GP
R469 33R2J-2-GP
CLK48_USB 12
CLK48_6433 32
EC80 EC81
SB A-Link
LAN
NB A-Link
MINI1
CLK_PCIE_SB R419 Do Not Stuff
CLK_PCIE_SB# R420 Do Not Stuff
CLK_PCIE_LAN R421 Do Not Stuff
CLK_PCIE_LAN# R422 Do Not Stuff
CLK_NB_GPPSB R435 Do Not Stuff
CLK_NB_GPPSB# R438 Do Not Stuff
CLK_PCIE_MINI1 R442 Do Not Stuff
CLK_PCIE_MINI1# R448 Do Not Stuff
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
0908
No mini2 card function
No new card function
54 OSC_SPREAD
54 CLK_27M_VGA
R451 Do Not Stuff
R456 Do Not Stuff
CLK_SRC0T_LPRS
CLK_SRC0C_LPRS
-2 0301
1116
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
REF0
REF1
REF2
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSB_SRC
HTT0T_LPRS/66M
HTT0C_LPRS/66M
R456 Do Not Stuff
R477 Do Not Stuff
R476 Do Not Stuff
CLK_NBHT_CLK_1
CLK_NBHT_CLK#_1
CLK_NBHT_CLK
CLK_NBHT_CLK#
NB HT
For SB820
71.09480.A03
2ND = 71.00880.A03
R188 Do Not Stuff
R197 Do Not Stuff
REF1
CLK_SB_14M 12
3D3V_SS
RN56
SRN10KJ-6-GP
PD#
WLAN_CLKREQ#
LAN_CLKREQ#
RUNPWROK_D
RUNPWROK_D 42
1008
1030
R193 Do Not Stuff
R189 Do Not Stuff
R190 10KR2J-3-GP
RN70 SRN10KJ-5-GP
R478 Do Not Stuff
-2 0301
REF0
REF1
REF2
R186 158R2F-GP
R185 90D9R2F-1-GP
CLK_NB_14M 9
OSC_14M_NB
RS880M 1.1V 158R/90.9R
SEL_27 REF2
1 * 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0 100MHz differential spreading SRC clock
SEL_SATA REF1
1 100MHz non-spreading differential SATA clock
0 * 100MHz differential spreading SRC clock
SEL_HTT66 REF0
1 66MHz 3.3V single ended HTT clock
0 * 100MHz differential HTT clock
CPU_CLK(200MHz)
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
NB CLOCK INPUT TABLE
NB CLOCKS | RS880M
HT_REFCLKP | 100M DIFF
HT_REFCLKN | 100M DIFF
REFCLK_P | 14M SE (1.1V)
REFCLK_N | vref
GFX_REFCLK | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF
* RS880M can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
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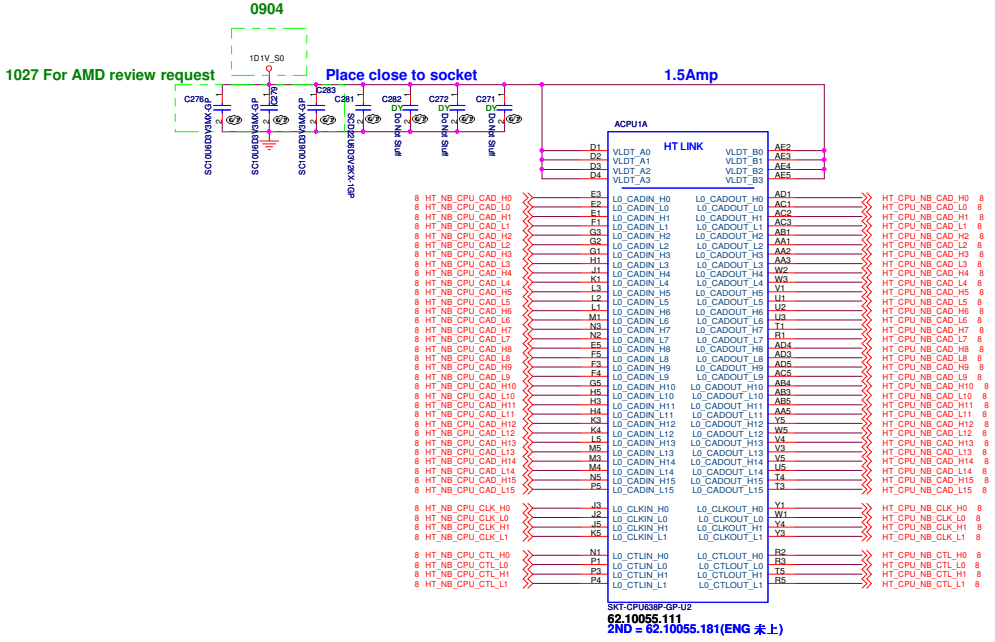
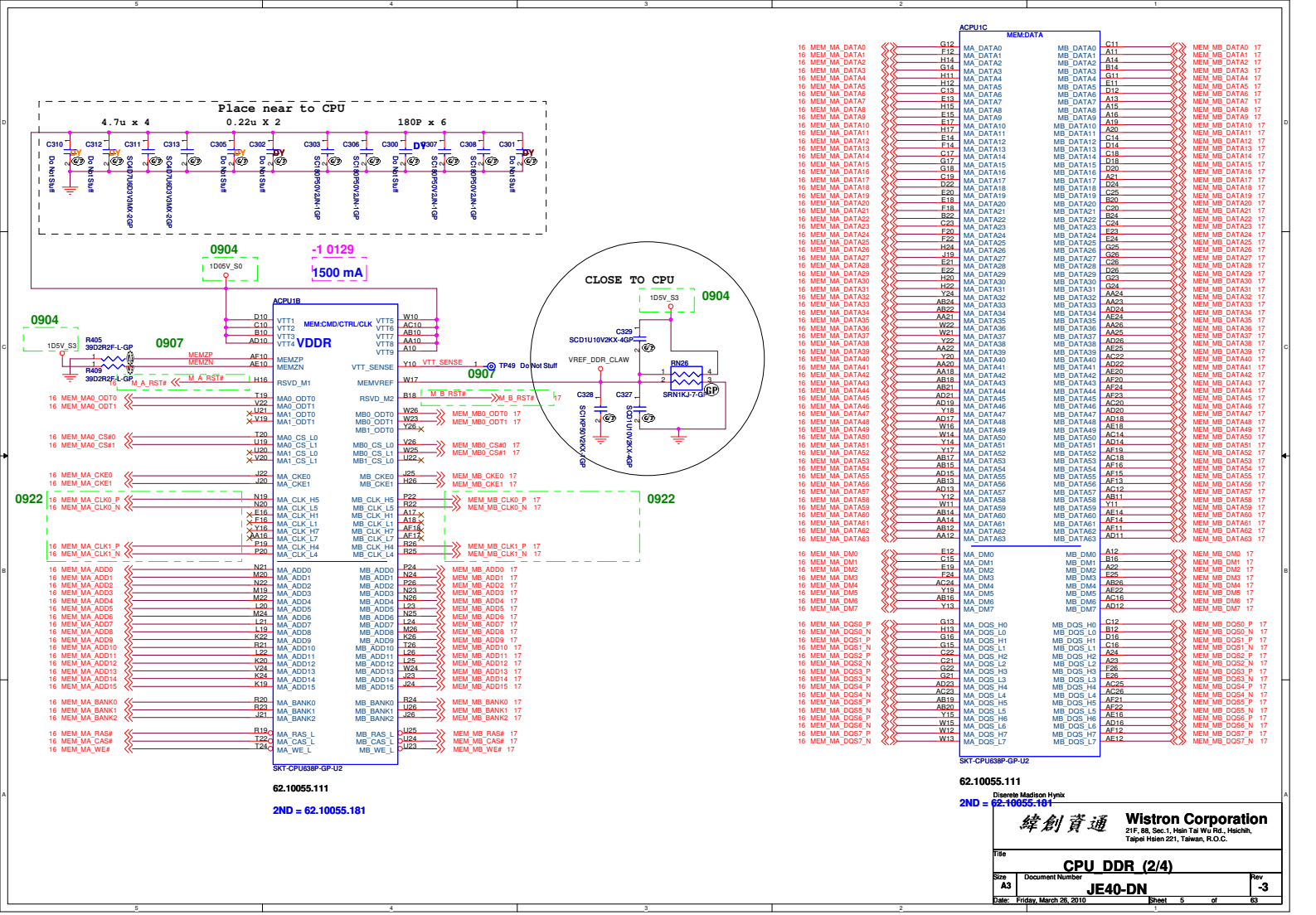
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN_ICS9LPRS480
Size A3
Document Number JE40-DN
Rev -3
Date: Friday, March 26, 2010
Sheet 3 of 63

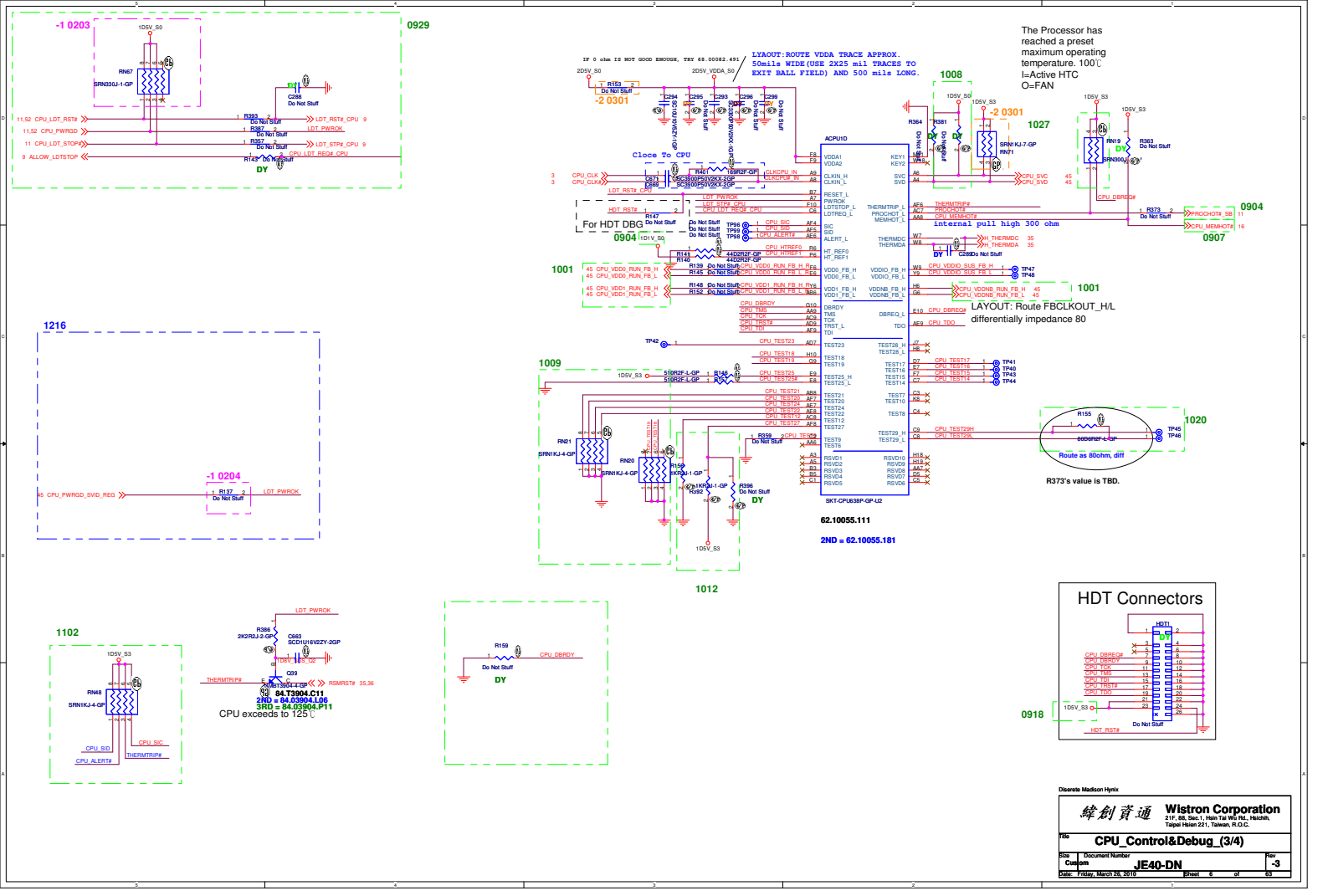


Diserete Madison Hynix

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_HT_LINK I/F_(1/4)		
Size: A3	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 4 of 63	



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_DDR_(2/4)	
Size: A3	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 5 of 63	


-1 0203
0929
RN67
SRN33U-1-GP
C288
Do Not Stuff
DY
11,52 CPU_LDT_RST#
11,52 CPU_PWRGD
11 CPU_LDT_STOP#
9 ALLOW_LDTSTOP
R383 Do Not Stuff
R387 Do Not Stuff
R357 Do Not Stuff
R143 Do Not Stuff
LDT_RST#_CPU 9
LDT_PWROK
LDT_STP#_CPU 9
LDT_CPU_REQ#_CPU
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
-2 0301
R153 Do Not Stuff
Cloce To CPU
ACPU1D
SKT-CPU838P-GP-U2
62.10055.111
2ND = 62.10055.181
The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN
1008
1027
-2 0301
SRN4KJ-7-GP
RN71
LAYOUT: Route FBCLKOUT_H/L differentially impedance 80
internal pull high 300 ohm
For HDT DBG
0904
0907
1001
1009
1012
1216
-1 0204
R137 Do Not Stuff
1102
RN48
SRN1KJ-4-GP
R386 2K2R2J-2-GP
C663 SCD1U16V2ZY-2GP
Q99
2N3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
3RD = 84.03904.P11
CPU exceeds to 125℃
R159 Do Not Stuff
DY
1020
R155
60D6R8F-L-GP
Route as 80ohm, diff
R373's value is TBD.
HDT Connectors
HDT1
0918
Do Not Stuff
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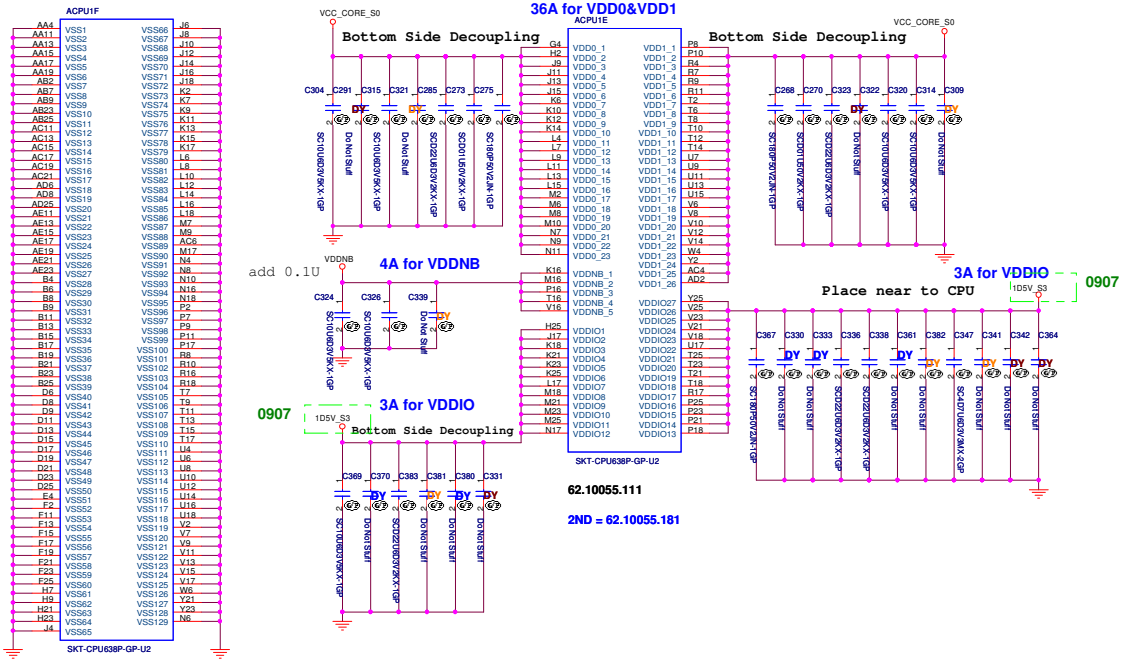
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU_Control&Debug_(3/4)
Size: Custom
Document Number: JE40-DN
Rev: -3
Date: Friday, March 26, 2010
Sheet 6 of 53



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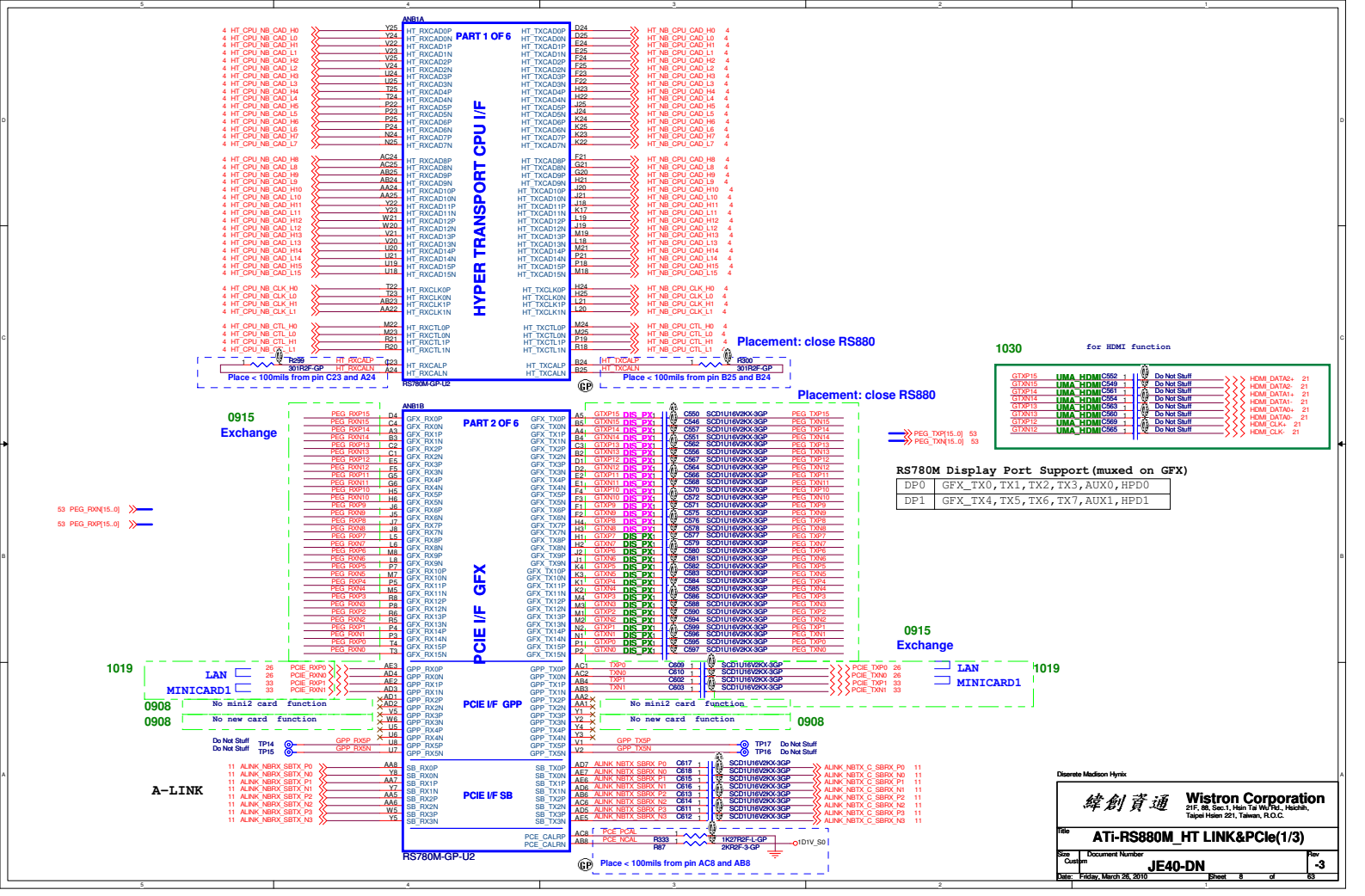
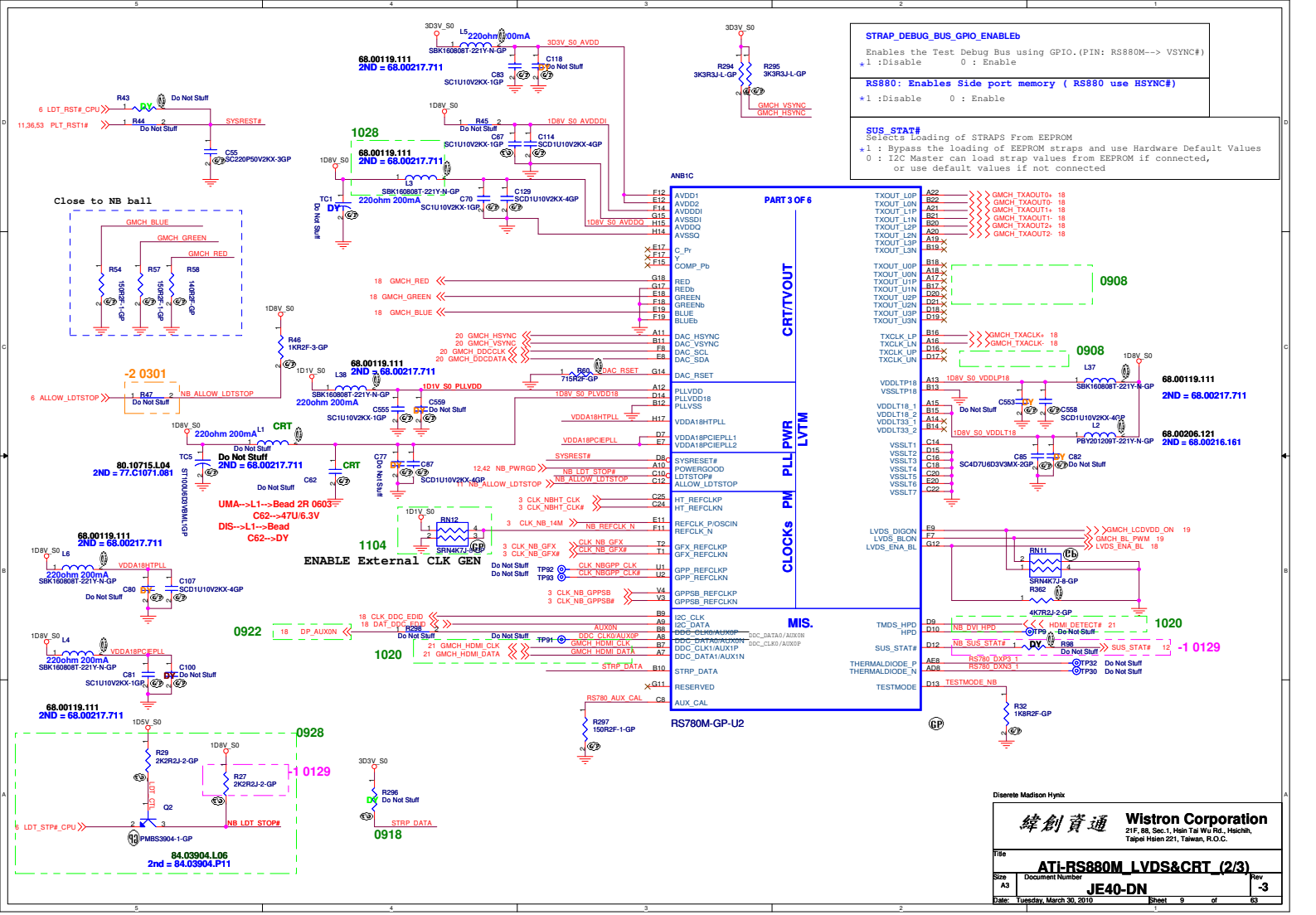
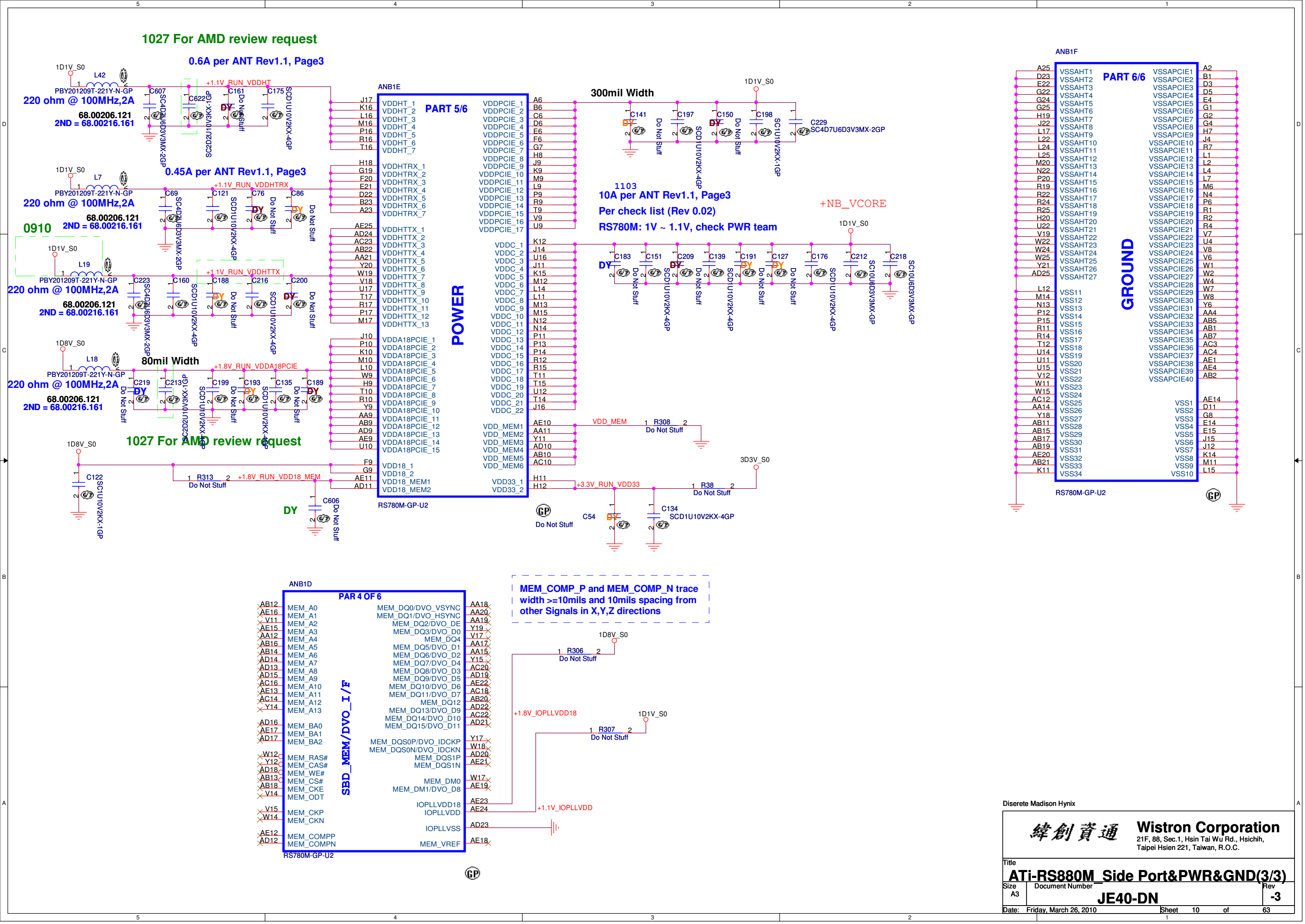
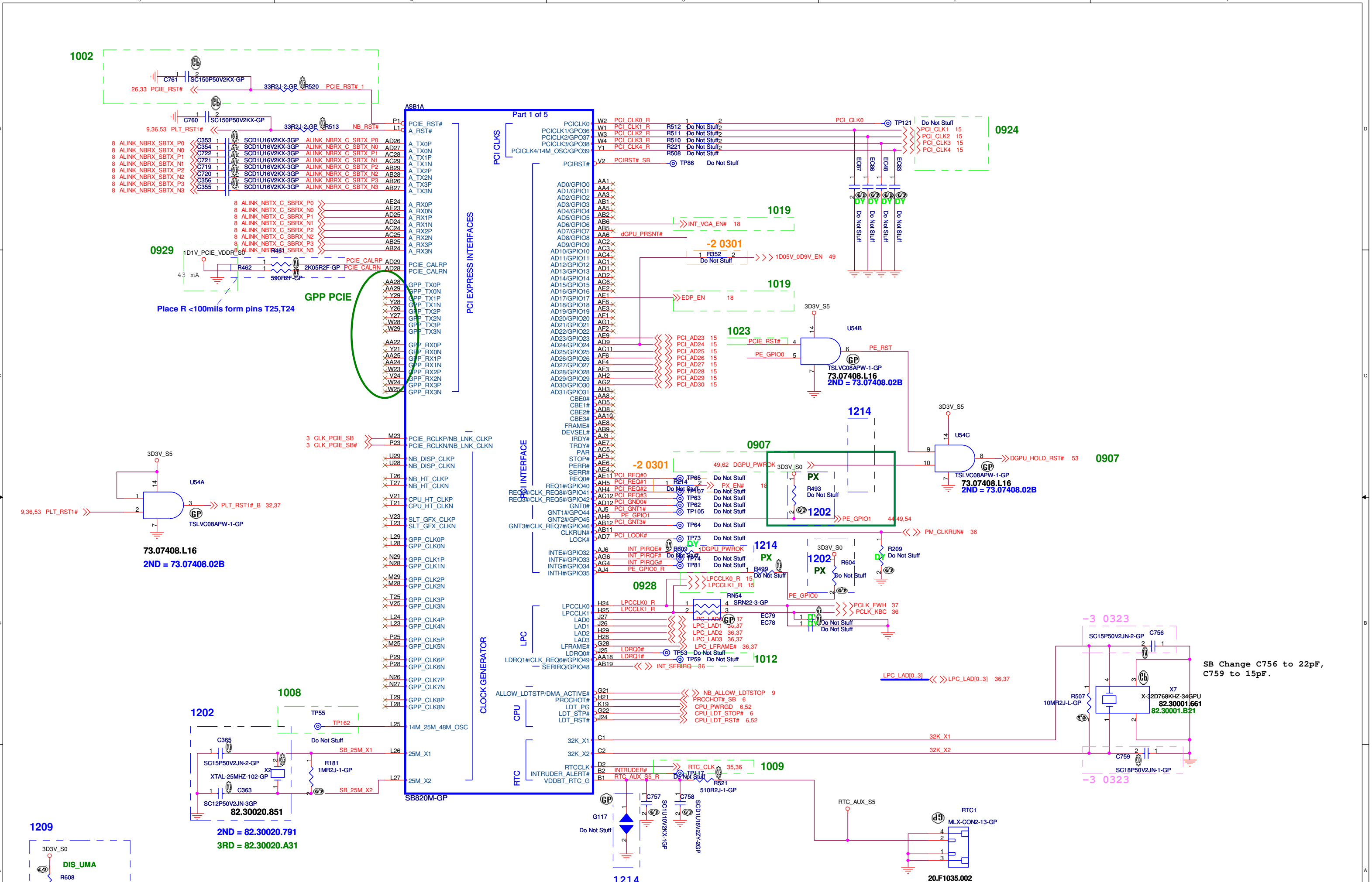
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)		
Size A3	Document Number JE40-DN		Rev -3
Date: Friday, March 26, 2010		Sheet 7 of 63	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Placement: close RS880
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Place < 100mils from pin AC8 and AB8
0915 Exchange
1030
for HDMI function
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
1019
LAN
MINICARD1
0908
No mini2 card function
No new card function
A-LINK
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M_HT LINK&PCIe(1/3)
JE40-DN
-3
Friday, March 26, 2010
Sheet 8 of 63


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC#)
*1 :Disable 0 : Enable
RS880: Enables Side port memory (RS880 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL PWR LVTM
CLOCKs PM
MIS.
RS780M-GP-U2
Close to NB ball
ENABLE External CLK GEN
UMA-->L1-->Bead 2R 0603
C62-->47U/6.3V
DIS-->L1-->Bead
C62-->DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI-RS880M_LVDS&CRT_(2/3)
JE40-DN
Date: Tuesday, March 30, 2010
Sheet 9 of 63


1027 For AMD review request
0.6A per ANT Rev1.1, Page3
220 ohm @ 100MHz,2A
68.00206.121
2ND = 68.00216.161
0.45A per ANT Rev1.1, Page3
0910
80mil Width
300mil Width
1103
10A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
Do Not Stuff
Diserete Madison Hynix
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_Side Port&PWR&GND(3/3)
Size A3
Document Number
JE40-DN
Rev -3
Date: Friday, March 26, 2010
Sheet 10 of 63



POWER EXPRESS SUPPORT

PE_GPIO0 VGA RESET	H: Enable
PE_GPIO1 VGA POWER ENABLE	H: Enable
PE_GPIO2 MODE SWITCH(BY NB)	H:VGA L:NB

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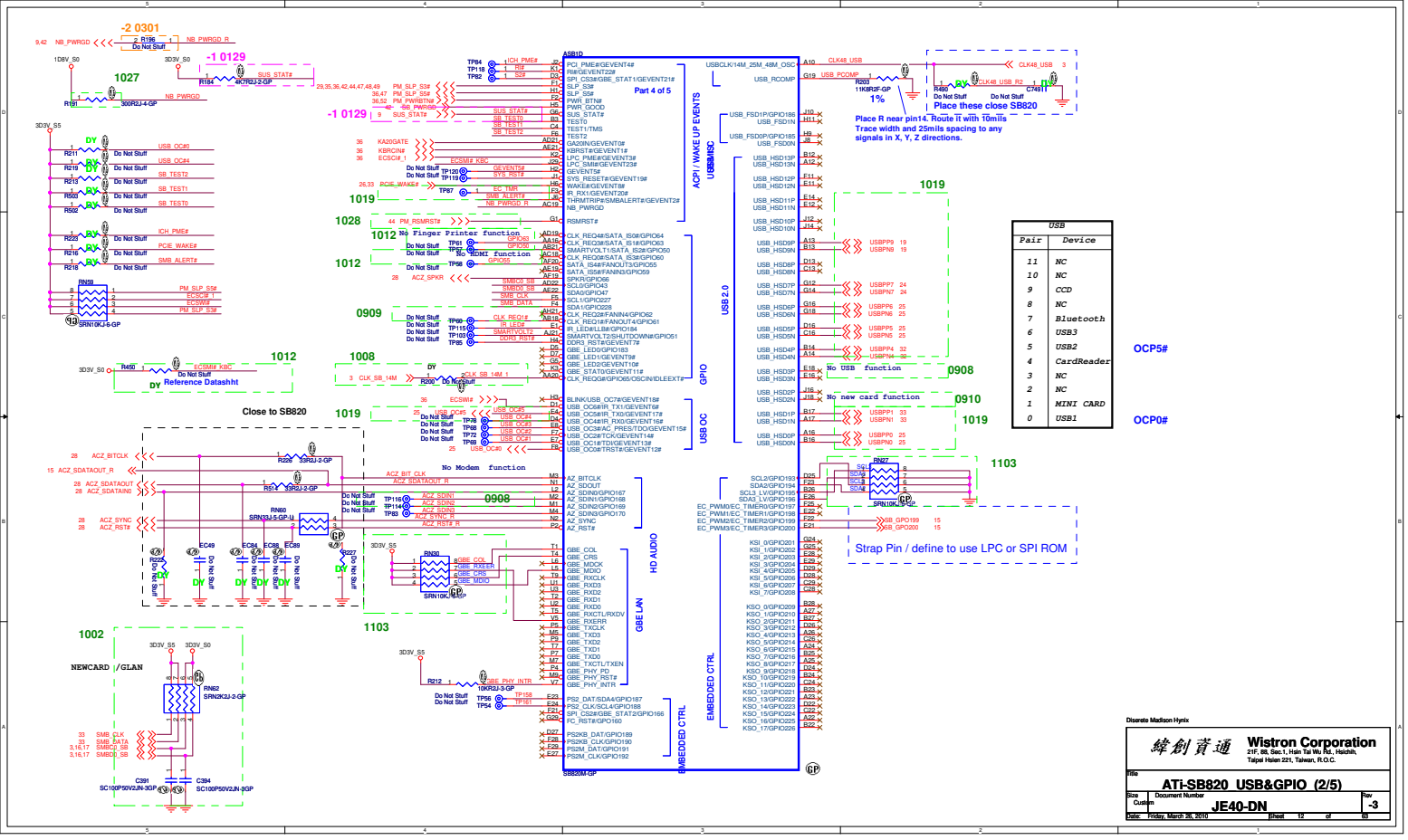
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	ATi-SB820_PCIE&PCI (1/5)	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 11 of 63	



USB	
Pair	Device
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	NC
2	NC
1	MINI CARD
0	USB1

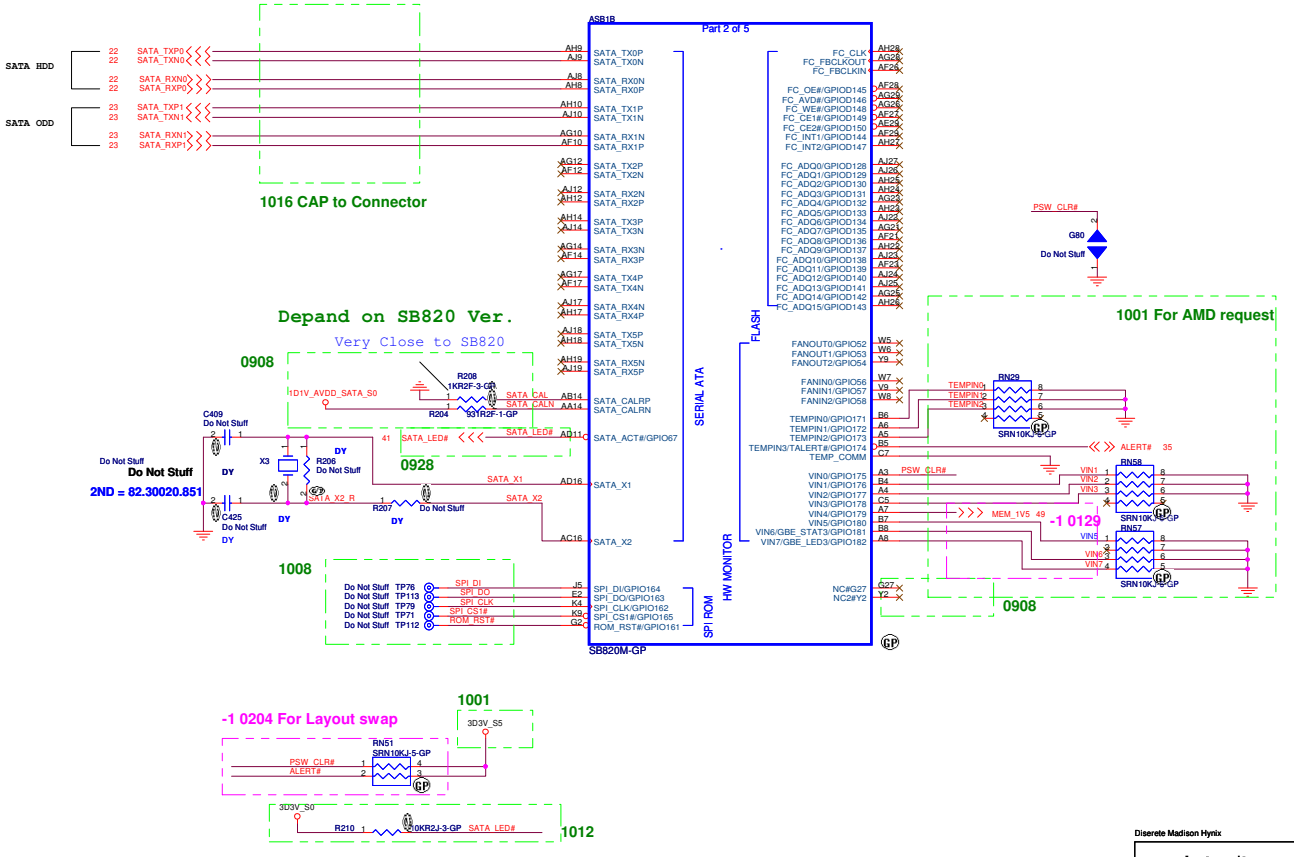
Discrete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB820 USB&GPIO (2/5)

Size	Document Number	Rev
Custom	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 12 of 53



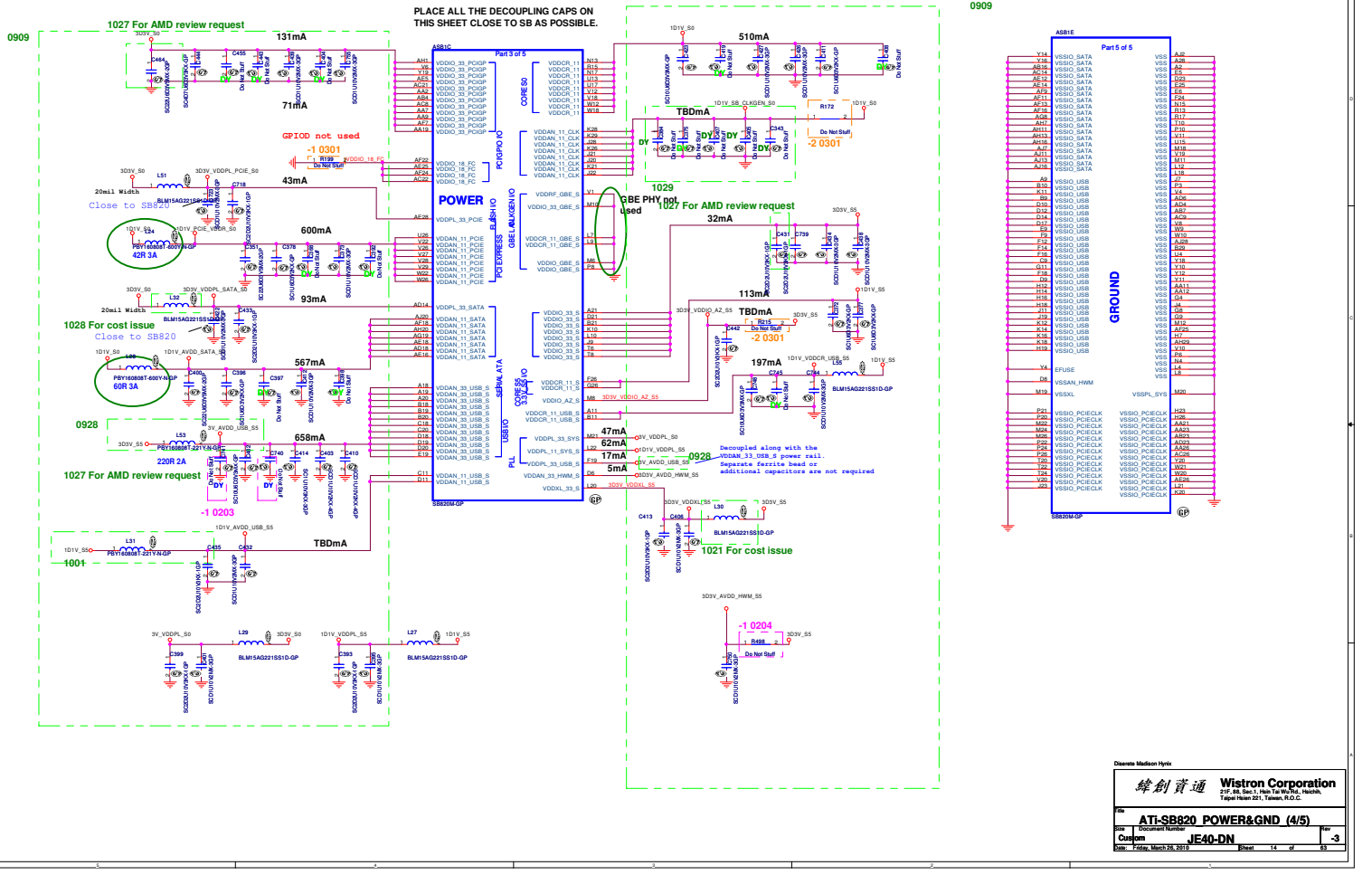
Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB820 SATA-IDE (3/5)**

Size	Document Number	Rev
A3	JE40-DN	-3

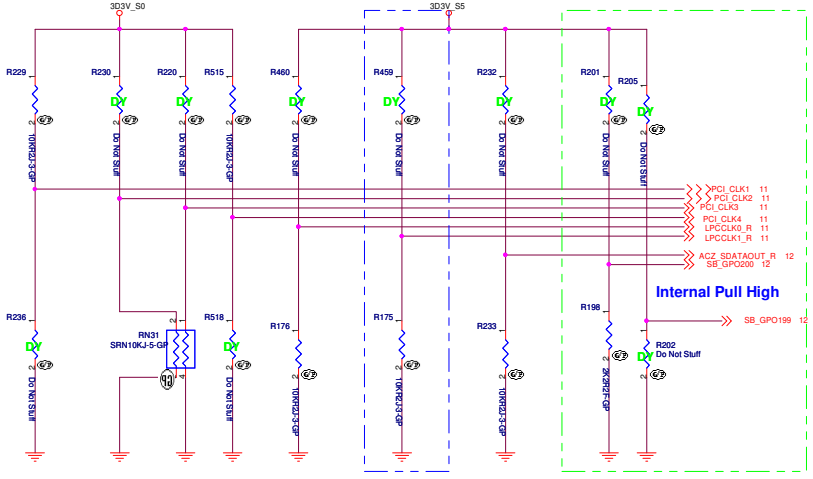
Date: Friday, March 26, 2010 Sheet 13 of 63


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
0909
1027 For AMD review request
131mA
71mA
GPIOD not used
-1 0301
Do Not Stuff
20mil Width
Close to SB820
43mA
42R 3A
600mA
93mA
1028 For cost issue
Close to SB820
60R 3A
567mA
0928
658mA
220R 2A
1027 For AMD review request
-1 0203
TBDmA
1001
ASB1C
Part 3 of 5
POWER
CORE SD
PCI/GPIO IO
PCI EXPRESS
GBE LAN/GEN IO
FLASH IO
SERIAL ATA
CORE 3.3V IO
USB IO
PLL
SB820M-GP
GBE PHY not used
1029
510mA
TBDmA
-2 0301
1027 For AMD review request
32mA
113mA
TBDmA
197mA
47mA
62mA
17mA
5mA
Decoupled along with the VDDAN_33_USB_S power rail. Separate ferrite bead or additional capacitors are not required
1021 For cost issue
-1 0204
ASB1E
Part 5 of 5
GROUND
SB820M-GP
Discrete Madison Hynix
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB820_POWER&GND (4/5)
Custom
JE40-DN
-3
Date: Friday, March 26, 2010
Sheet 14 of 83

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS

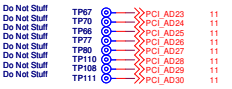
1115



1002

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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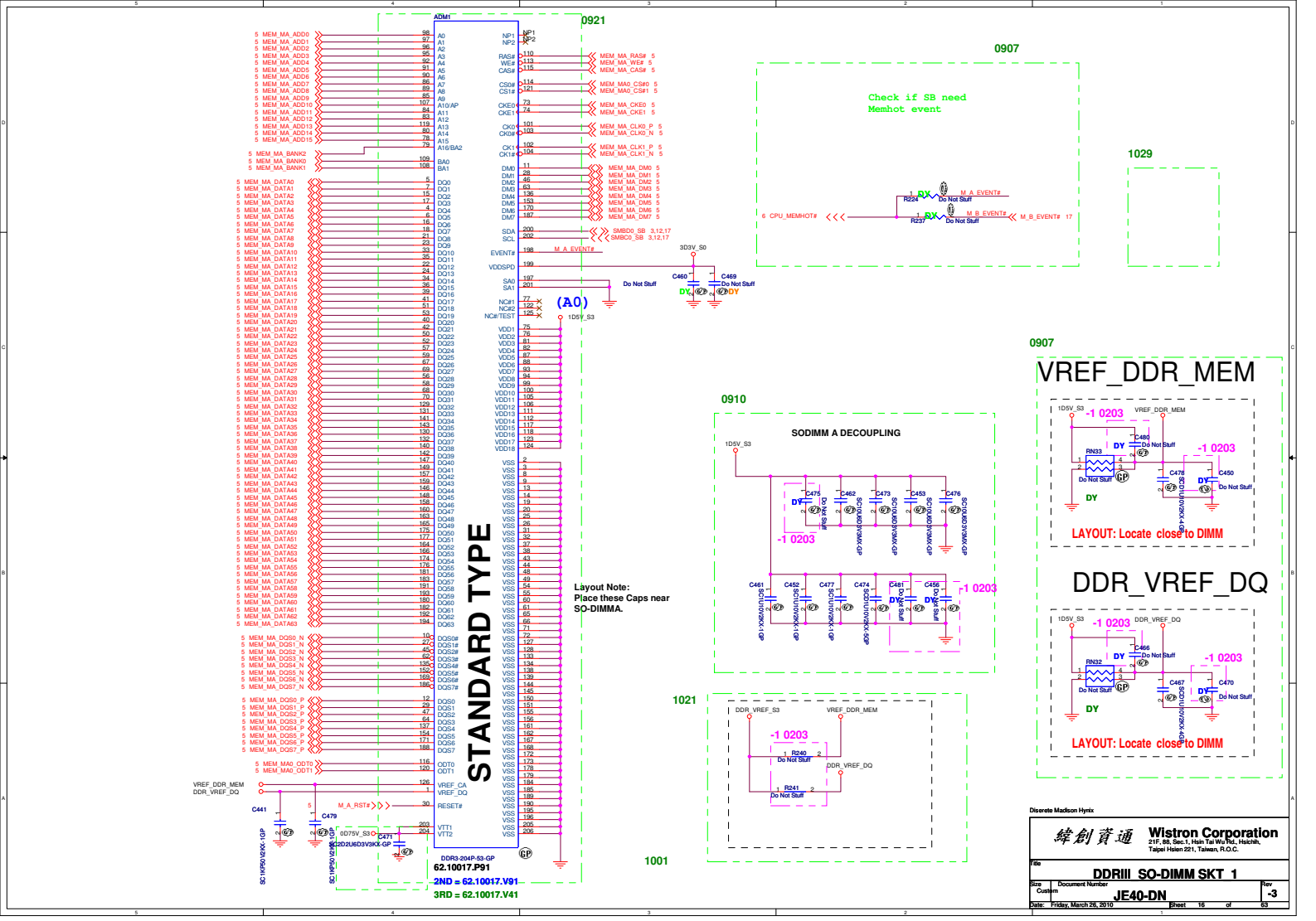
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB820 STRAPPING (5/5)

Size: A3 | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 15 of 63


0921
ADM1
STANDARD TYPE
DDR3-204P-53-GP
62.10017.P91
2ND = 62.10017.V91
3RD = 62.10017.V41
Layout Note:
Place these Caps near
SO-DIMMA.
0907
Check if SB need
Memhot event
1029
0907
VREF_DDR_MEM
-1 0203
LAYOUT: Locate close to DIMM
DDR_VREF_DQ
0910
SODIMM A DECOUPLING
1021
1001
Diserete Madison Hynix
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII SO-DIMM SKT 1
JE40-DN
-3
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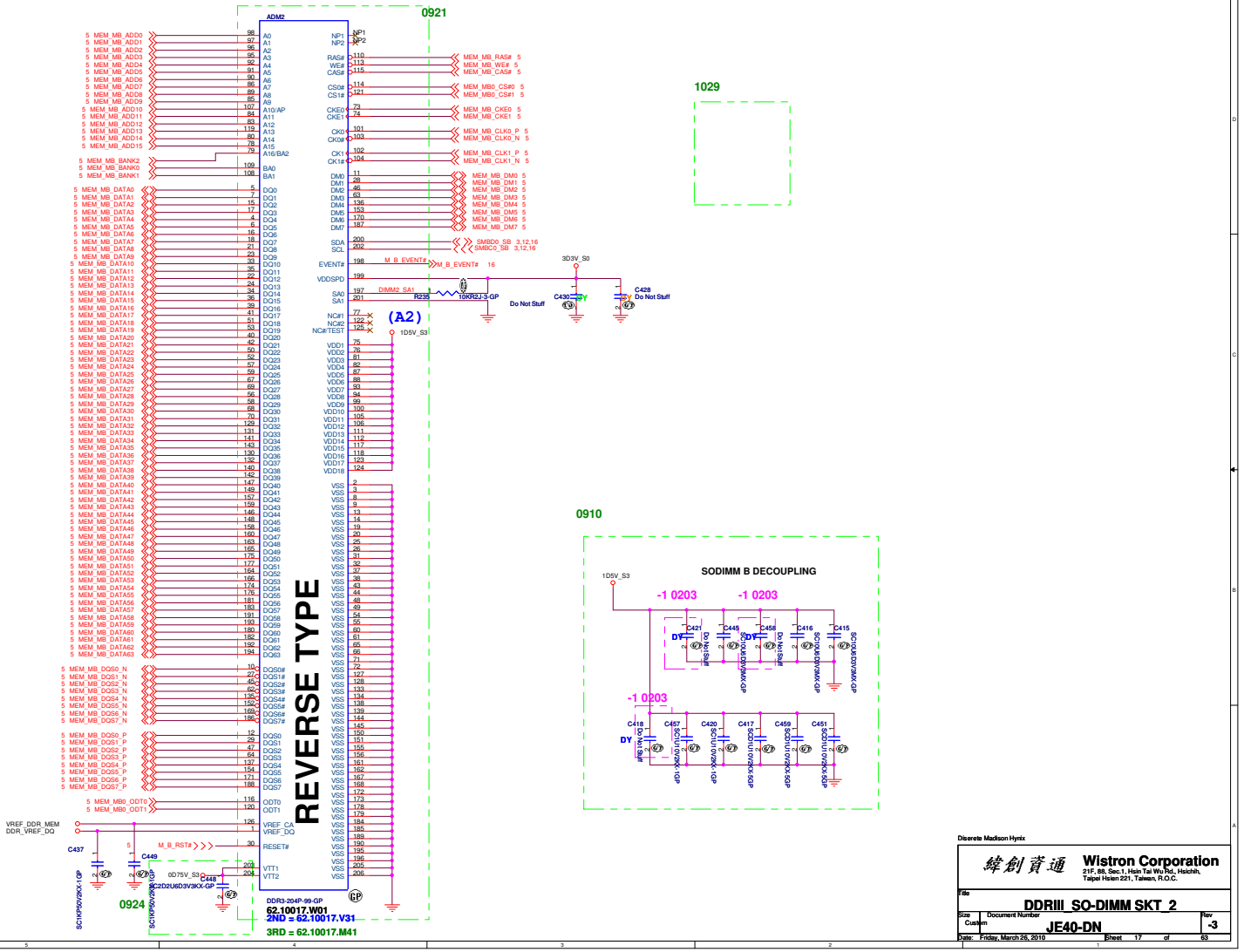
16
63



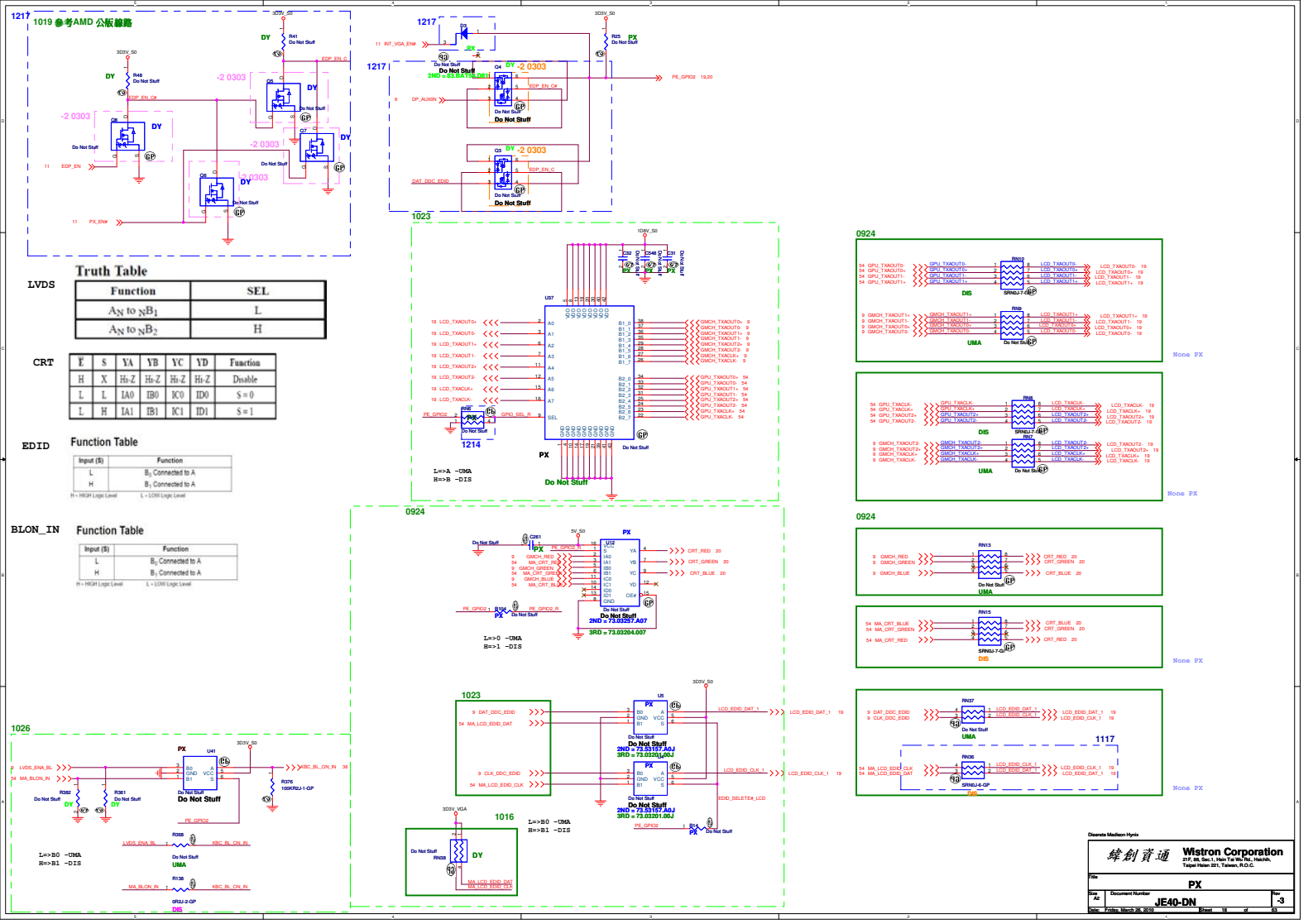
Discrete Madison Hynix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDRIII_SO-DIMM SKT_2**

Size	Document Number	Rev
Custom	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 17 of 63



LVDS

Truth Table

Function	SEL
A_N to $_NB_1$	L
A_N to $_NB_2$	H

CRT

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input ($)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

BLON_IN

Function Table

Input ($)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

Discrete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PX
Size: A0	Document Number: JE40-DN
Rev: -3
Date: Friday, March 26, 2010	Sheet 18 of 83

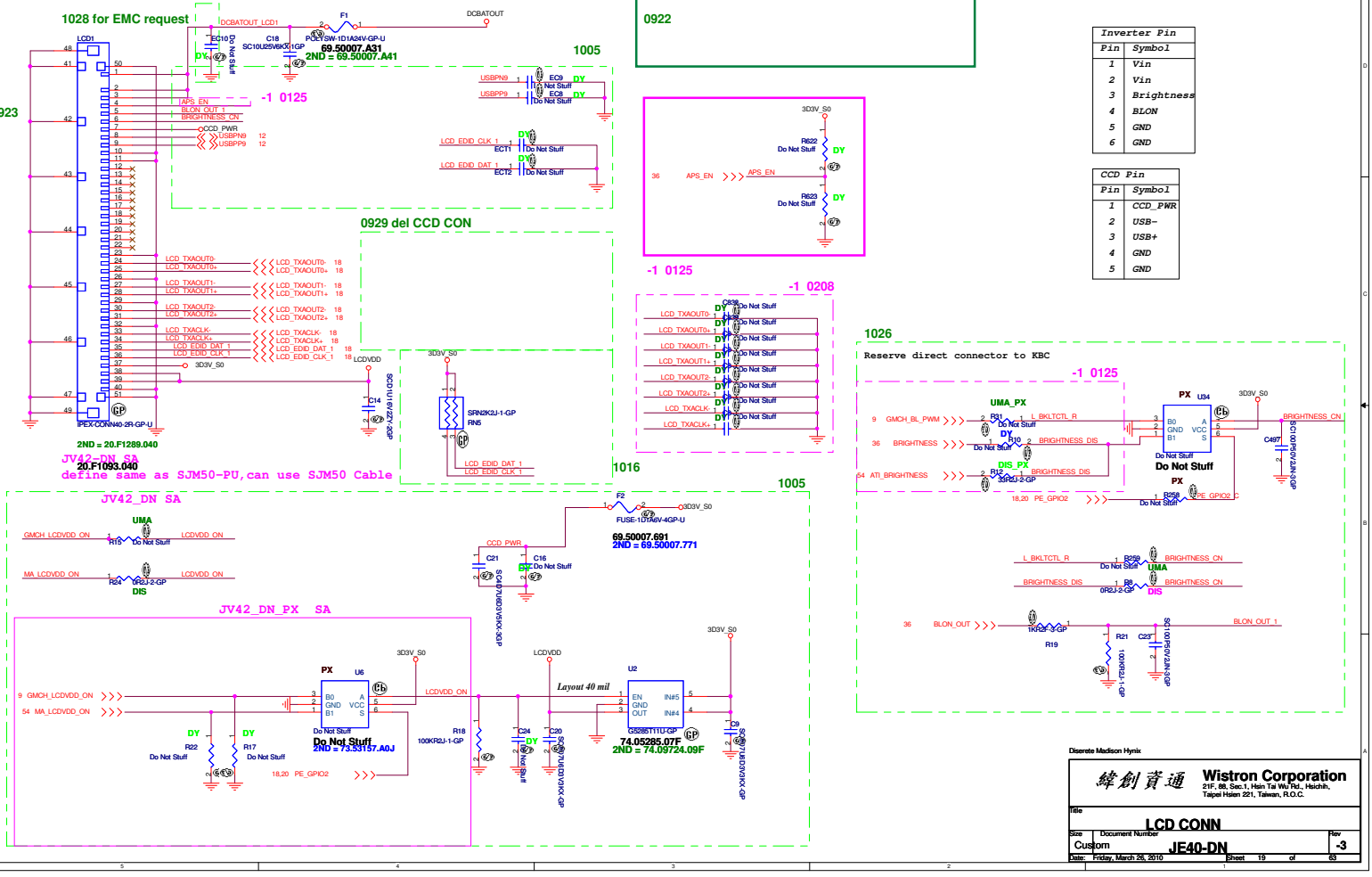
LCD/INVERTER/CCD CONN

Change PX

0922

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



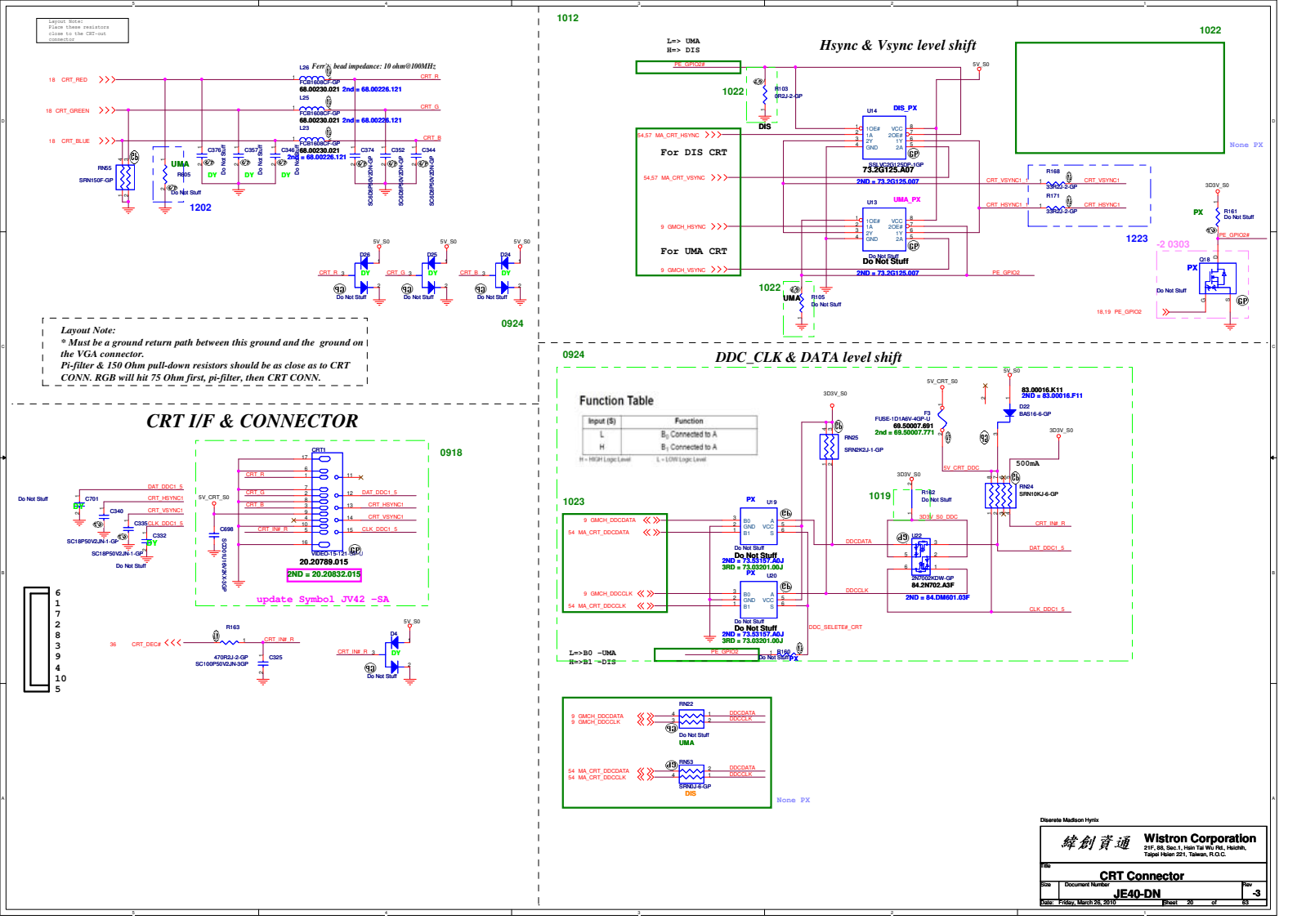
Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size	Document Number	Rev
Custom	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 19 of 63


Layout Note:
Place these resistors close to the CRT-out connector
L26 Ferrite bead impedance: 10 ohm@100MHz
68.00230.021 2nd = 68.00226.121
L25
68.00230.021 2nd = 68.00226.121
L23
68.00230.021 2nd = 68.00226.121
18 CRT_RED
18 CRT_GREEN
18 CRT_BLUE
CRT_R
CRT_G
CRT_B
RN55
SRN150F-GP
UMA
R605
Do Not Stuff
1202
C370
C358
C346
C374
C352
C344
DY
Do Not Stuff
5V_S0
D28
D25
D24
CRT_R_3
CRT_G_3
CRT_B_3
0924
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.
1012
L=> UMA
H=> DIS
Hsync & Vsync level shift
1022
PE_GPIO28
R103
0R2J-2-GP
DIS
U14
DIS_PX
73.2G125.A07
2ND = 73.2G125.007
54,57 MA_CRT_HSYNC
54,57 MA_CRT_VSYNC
9 GMCH_HSYNC
9 GMCH_VSYNC
For DIS CRT
For UMA CRT
U13
UMA_PX
Do Not Stuff
2ND = 73.2G125.007
R105
Do Not Stuff
CRT_VSYNC1
CRT_HSYNC1
R168
R171
33R2J-2-GP
PE_GPIO2
None PX
1223
-2 0303
R161
Do Not Stuff
Q18
18,19 PE_GPIO2
0924
DDC_CLK & DATA level shift
Function Table
Input (S) | Function
L | B0 Connected to A
H | B1 Connected to A
H = HIGH Logic Level
L = LOW Logic Level
3D3V_S0
5V_CRT_S0
5V_S0
RN25
SRN2K2J-1-GP
F3
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
D22
BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
500mA
RN24
SRN10KJ-6-GP
5V_CRT_DDC
1023
1019
R182
Do Not Stuff
3D3V_S0_DDC
9 GMCH_DDCDATA
54 MA_CRT_DDCDATA
9 GMCH_DDCCLK
54 MA_CRT_DDCCLK
U19
U20
U22
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
DDCDATA
DDCCLK
CRT_INIF_R
DAT_DDC1_5
CLK_DDC1_5
DDC_SELETE#_CRT
Do Not Stuff
2ND = 73.83157.A0J
3RD = 73.03201.00J
R160
L=>B0 -UMA
H=>B1 -DIS
RN22
RN53
SRN0J-8-GP
DIS
None PX
CRT I/F & CONNECTOR
0918
CRT1
CRT_R
CRT_G
CRT_B
5V_CRT_S0
DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
CRT_INIF_R
C698
VIDEO-15-121-GP
20.20789.015
2ND = 20.20832.015
update Symbol JV42 -SA
Do Not Stuff
C701
C340
C335
C332
SC18P50V2JN-1-GP
R163
470R2J-2-GP
SC100P50V2JN-3GP
C325
CRT_DEC#
36
P4
CRT_INIF_R_3
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT Connector
Size
Document Number
JE40-DN
Rev
-3
Date: Friday, March 26, 2010
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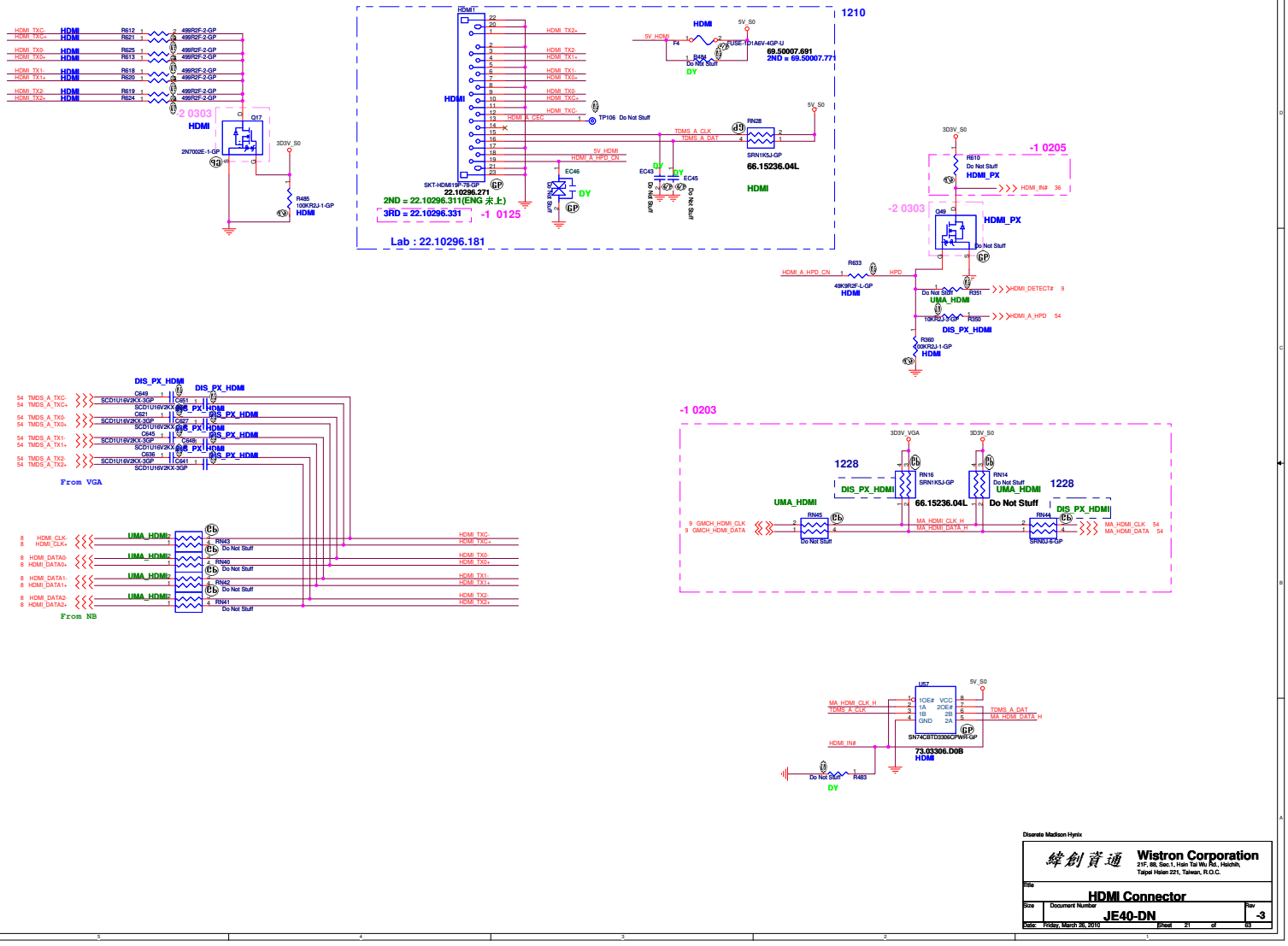
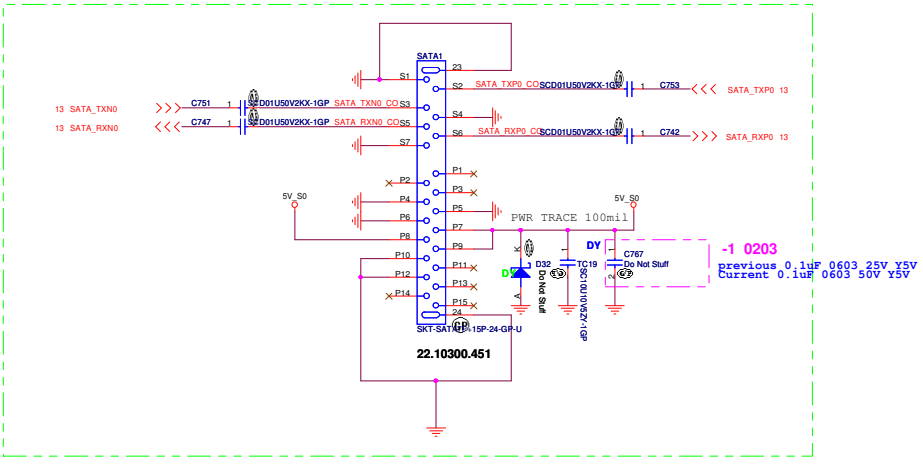


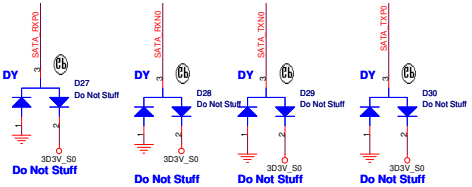
Disorete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDMI Connector**	
Size	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 21 of 63	

SATA Connector

0923





Diserete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD

Size	Document Number	Rev
	JE40-DN	-3

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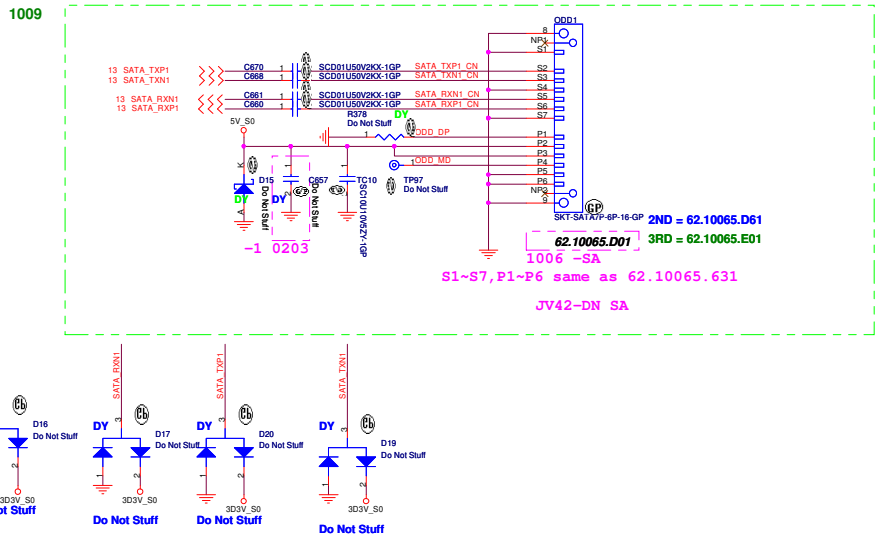
ODD Connector

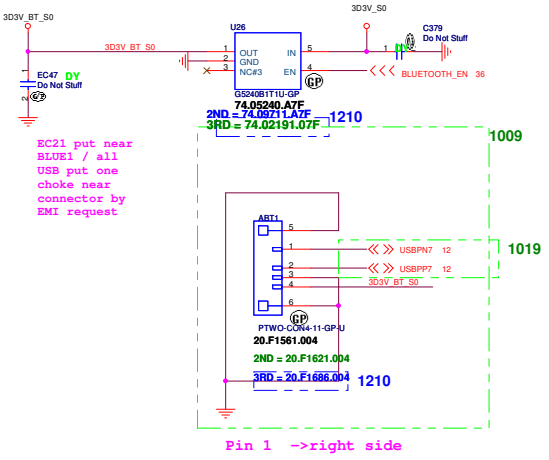


Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ODD**	
Size	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 23 of 63	

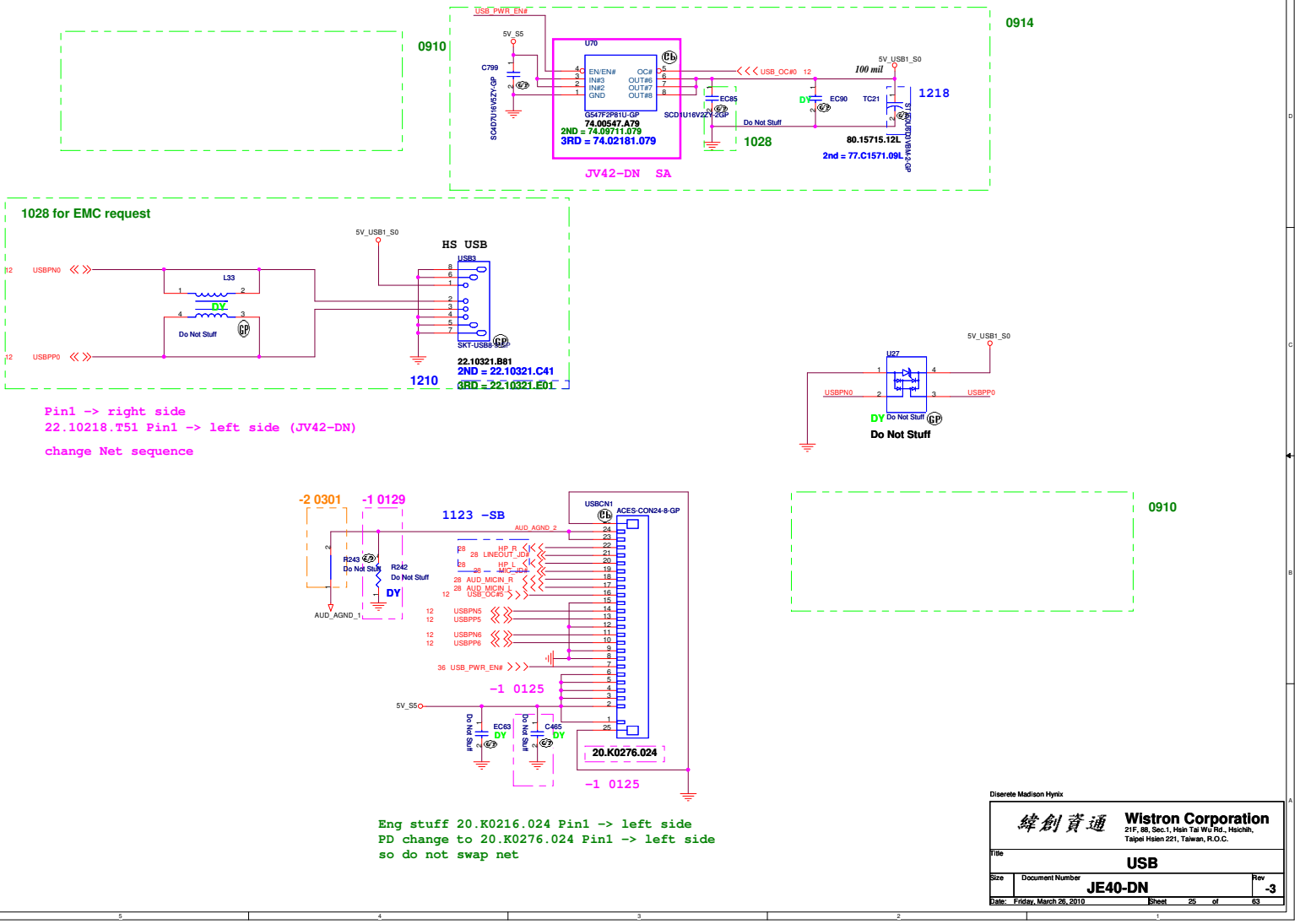
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



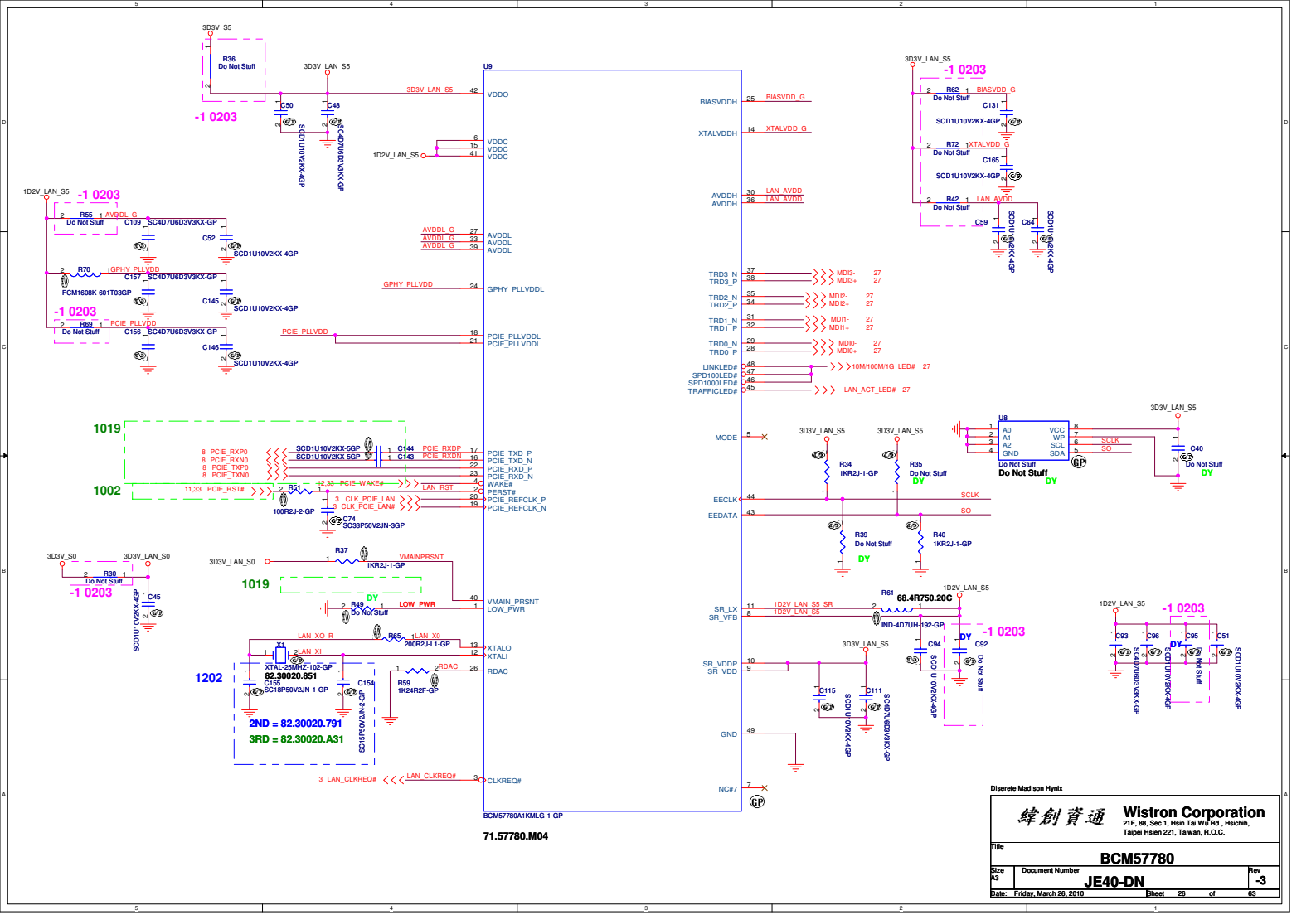
Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**BLUETOOTH**	
Size	Document Number **JE40-DN**	Rev **-3**
Date: Friday, March 26, 2010	Sheet 24 of 63	



Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB**	
Size	Document Number **JE40-DN**	Rev **-3**
Date: Friday, March 26, 2010	Sheet 25 of 63	


U9
BCM57780A1KMLG-1-GP
71.57780.M04
R36 Do Not Stuff
-1 0203
3D3V_S5
3D3V_LAN_S5
1D2V_LAN_S5
3D3V_S0
3D3V_LAN_S0
VDDO
VDDC
AVDDL
GPHY_PLVDDL
PCIE_PLLVDDL
BIASVDDH
XTALVDDH
AVDDH
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
MODE
EECLK
EEDATA
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
NC#7
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
VMAIN_PRSNT
LOW_PWR
XTALO
XTALI
RDAC
CLKREQ#
1019
1002
1202
DY
2ND = 82.30020.791
3RD = 82.30020.A31
Diserete Madison Hynix
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size A3
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1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

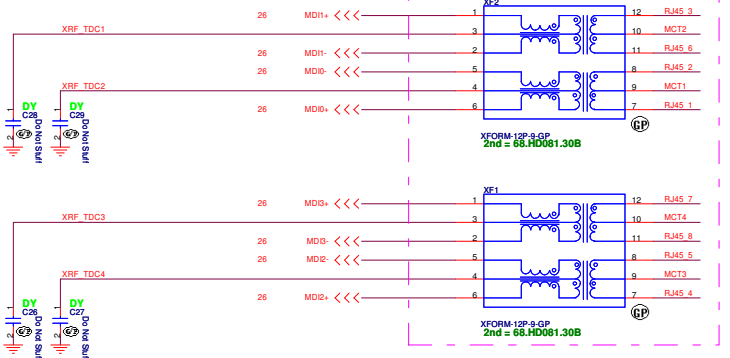
LAN Connector

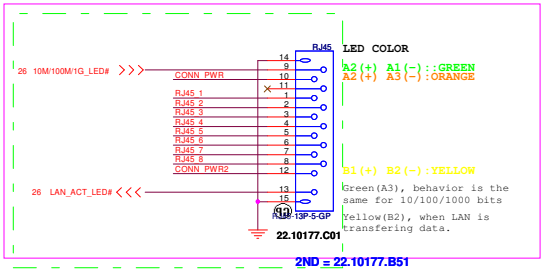
LAN Connector

0923

-1 0127 For EMI request

GIGA Lan Transformer



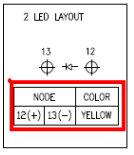


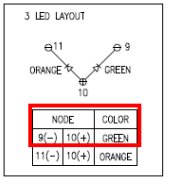
2ND = 22.10177.B51

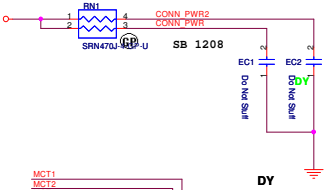
3RD = 22.10177.C21(lab 未上)

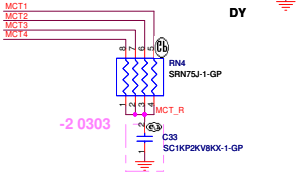
4TH = 22.10177.H31

5TH = 22.10177.B81

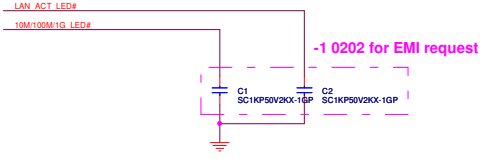








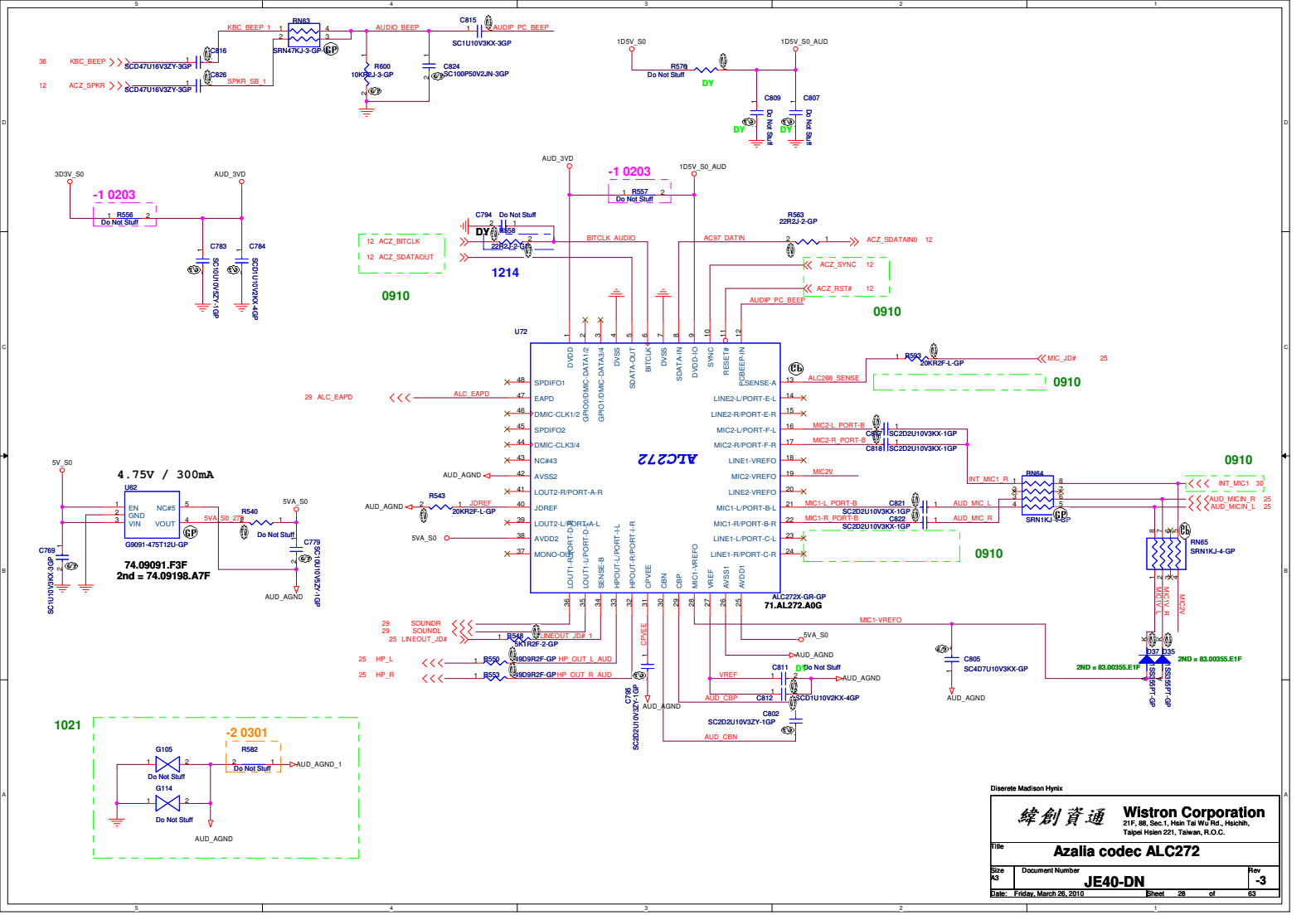
-2 0303



-1 0202 for EMI request

Diserete Madison Hynix

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN CONN		
Size: A3	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 27 of 63	

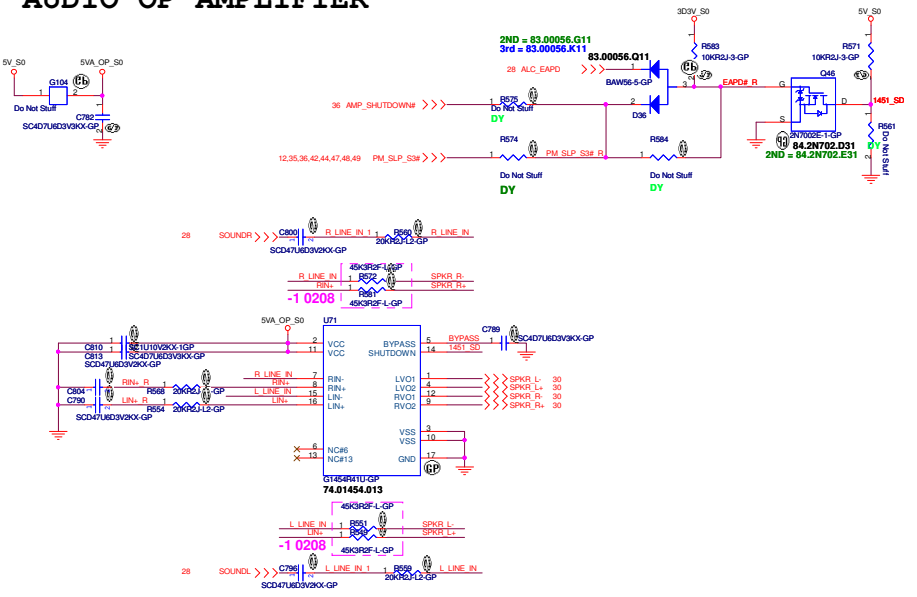


Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Azalia codec ALC272	
Size: A3	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 28 of 63	

AUDIO OP AMPLIFIER




```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W
```

Diserete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

Size	Document Number	Rev
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Internal Speaker

0914

0910

29 SPKR_L-
29 SPKR_L+
29 SPKR_R-
29 SPKR_R+

SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+

EC15 EC14 EC13 EC12

AZ2025-01H-GP-U

83.02025.0AF

-1 0125 for EMI request

SPKR1

SPKR_L+
SPKR_L-
SPKR_R+
SPKR_R-

PTWO-CON4-11-GP-U
20.F1561.004
2ND = 20.F1621.004
3RD = 20.F1686.004
1210

Plin 1- > right side

JV42-DN SA

0910

LINE OUT

0911

1016

Internal Mic

28 INT_MIC1

L59
MLVS0603K20-GP

AAMIC1

PTWO-CON2-6-GP
20.F1561.002
2ND = 20.F1621.002
3RD = 20.F1686.002
1210

-1 0209 For MIC issue

JV42-DN PX
Pin 1- >right side
20.F1240.002 Pin1->left side

same as JV70-CP

Diserete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO JACK		
Size	Document Number	Rev
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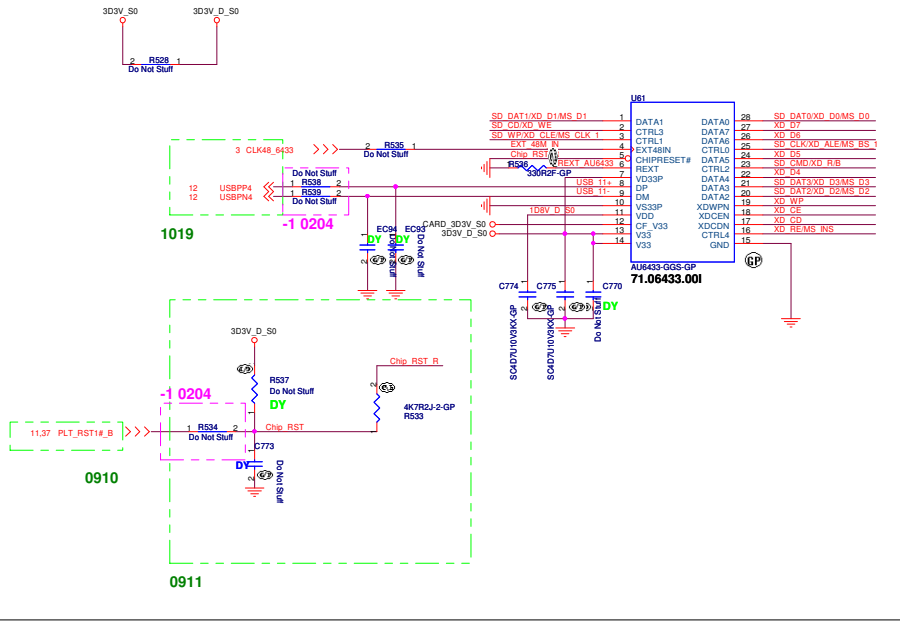
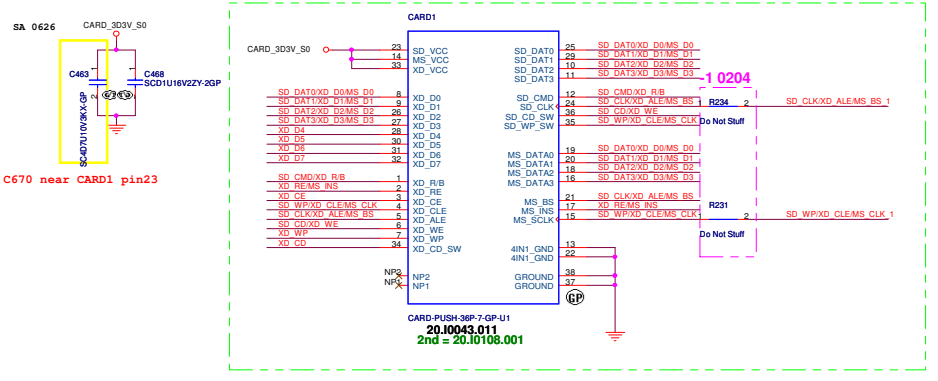
No Modem Function

Diserete Madison Hynix

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 31 of 63	

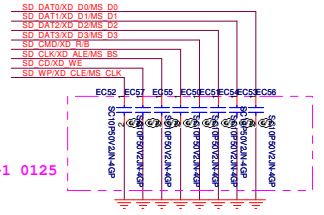


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



0914

EMI capacitor

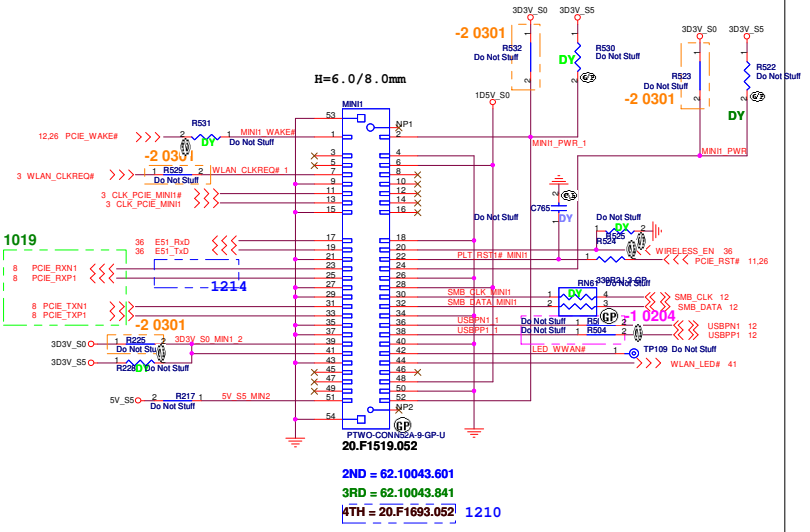


Diserete Madison Hynix

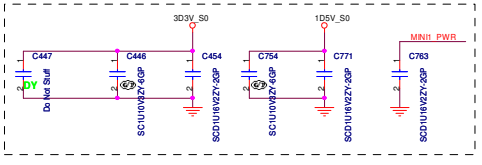
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CARDREADER		
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 32 of 63	

Mini Card Connector(WLAN)

0923



Place near MINI1



No Mini Card Function (Robson2 and 3G)

Diserete Madison Hynix

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
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No NEWCARD Function

Diserete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NEW CARD

Size	Document Number	Rev
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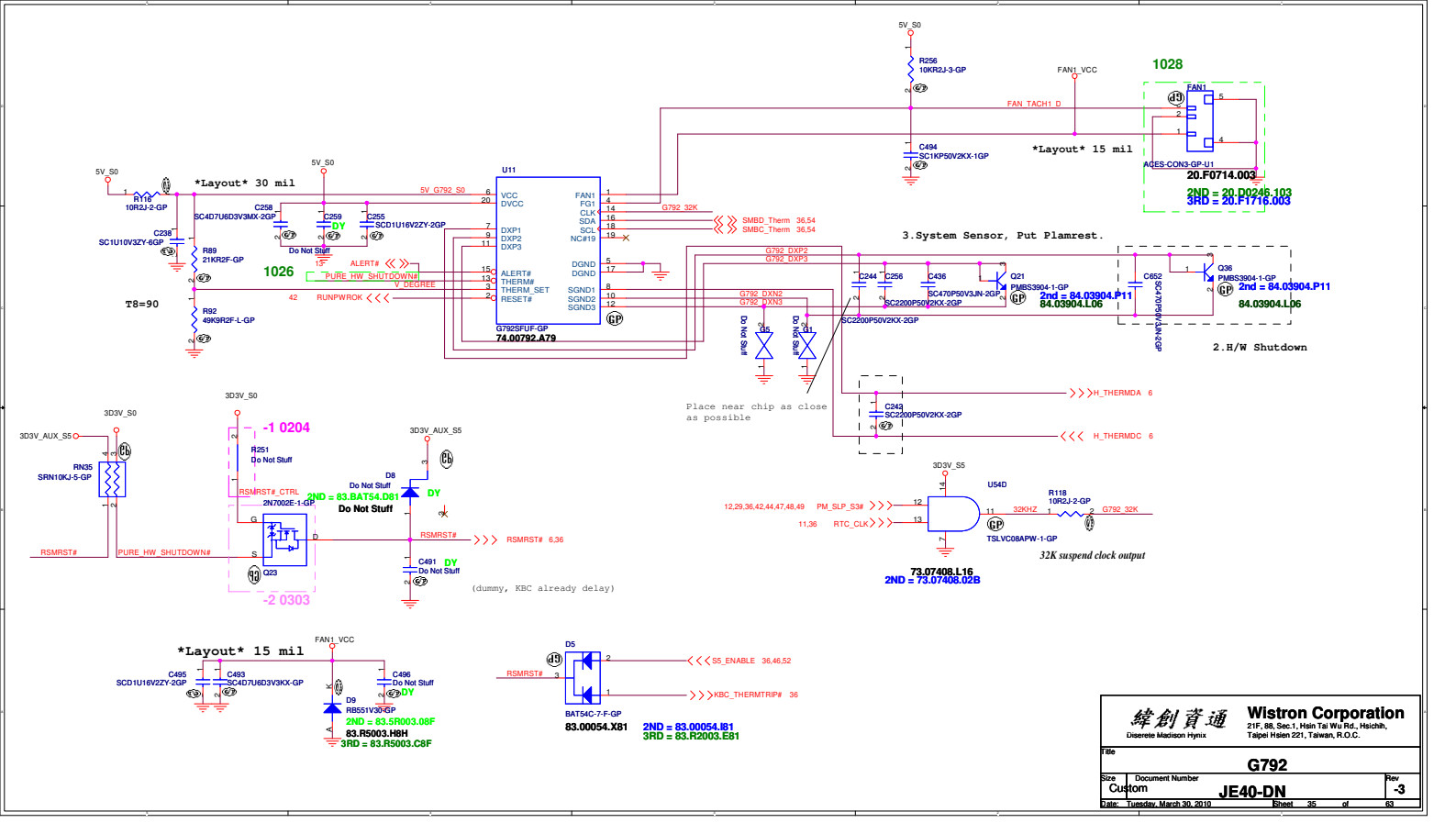
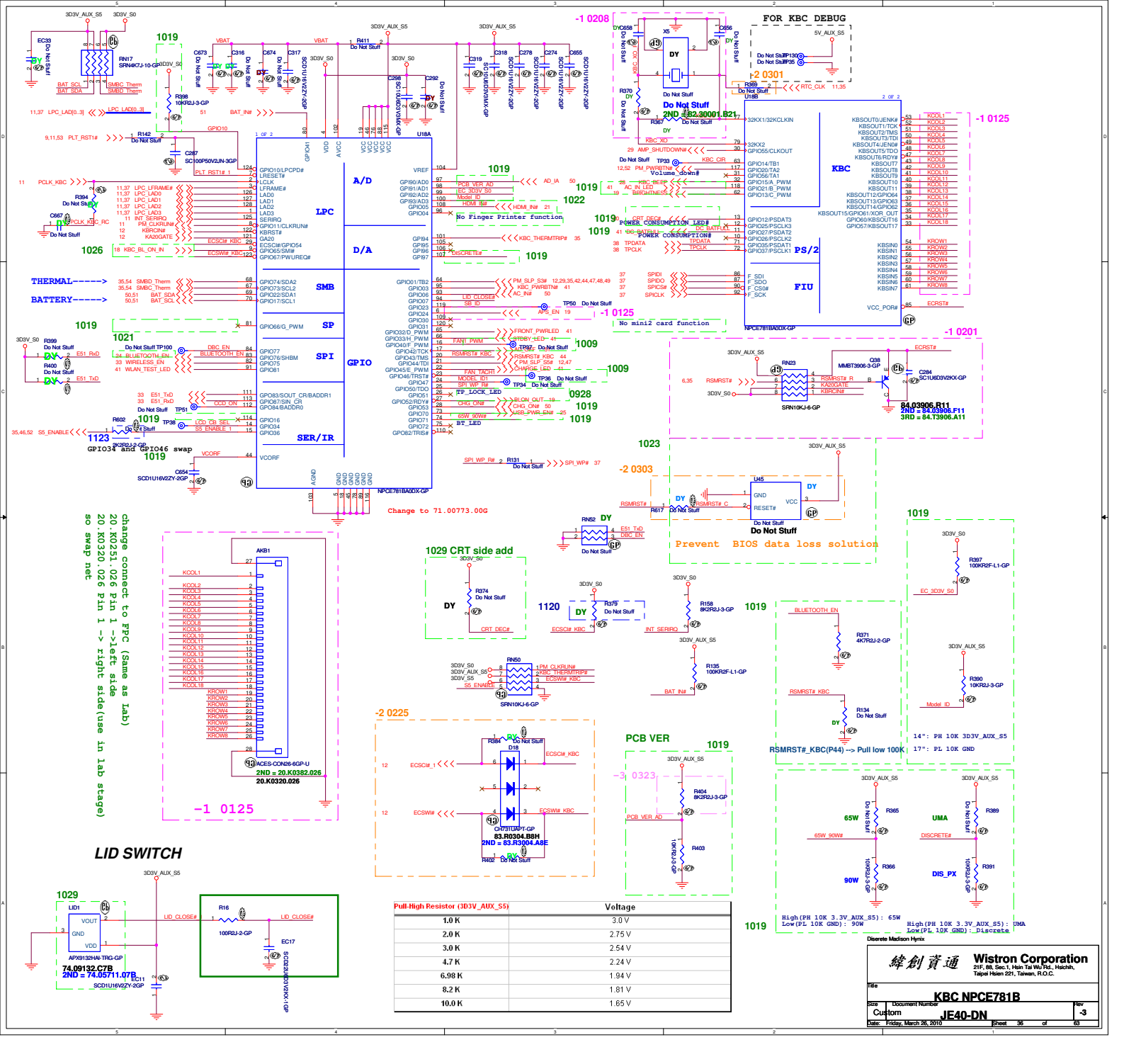


緯創資通 Wistron Corporation Diserete Madison Hynix	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: G792		
Size: Custom	Document Number: JE40-DN	Rev: -3
Date: Tuesday, March 30, 2010	Sheet 35 of 63	



Pull-High Resistor (3D3V_AUX_S5)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V

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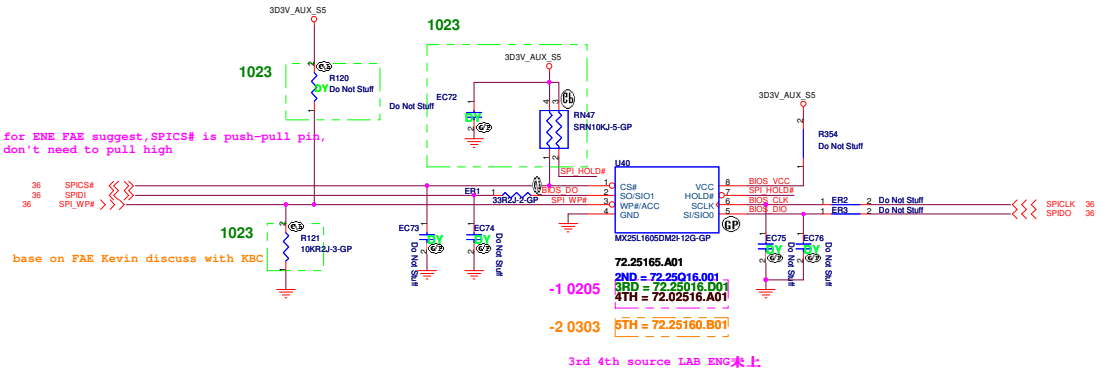
Title: KBC NPCE781B

Size: Custom | Document Number: JE40-DN | Rev: -3

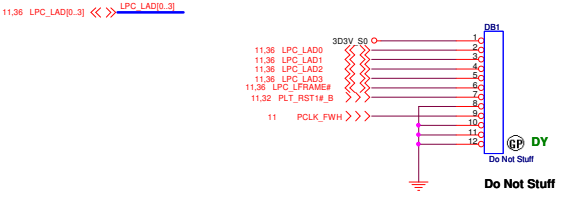
Date: Friday, March 26, 2010 | Sheet 36 of 63



3rd 4th source LAB ENG未上

16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



Diserete Madison Hynix

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Title: **BIOS**

Size	Document Number	Rev
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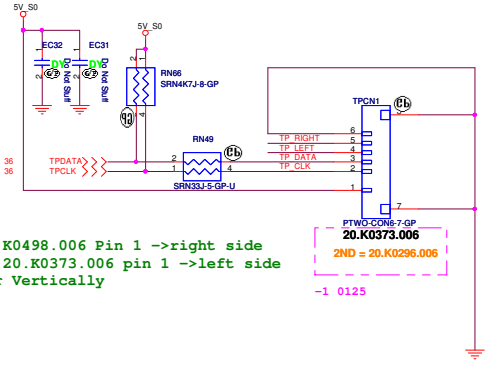
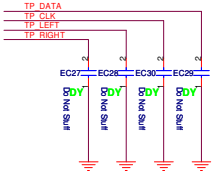
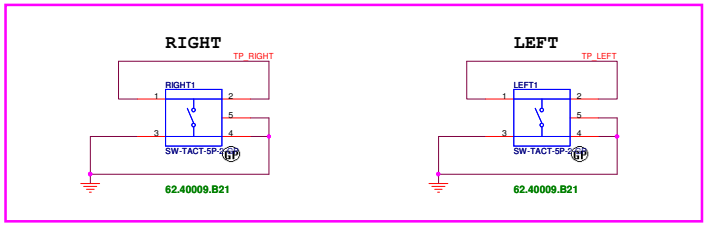


Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically



-1 0205



No Finger printer Function

Diserete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD

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NONE BOARD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: NONE BOARD

Size	Document Number	Rev
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緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SWITCH

Size	Document Number	Rev
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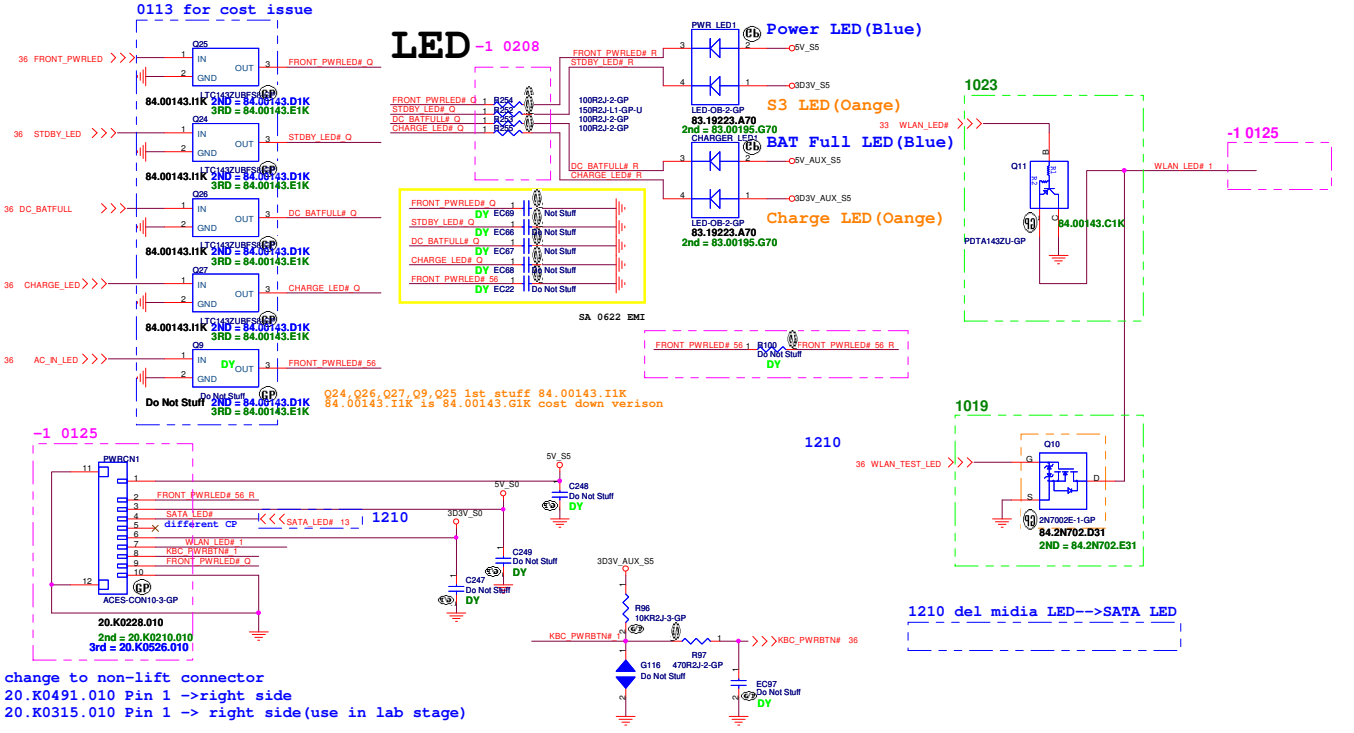

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	SATA_LED#	HDD
Pin 5	NA	
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

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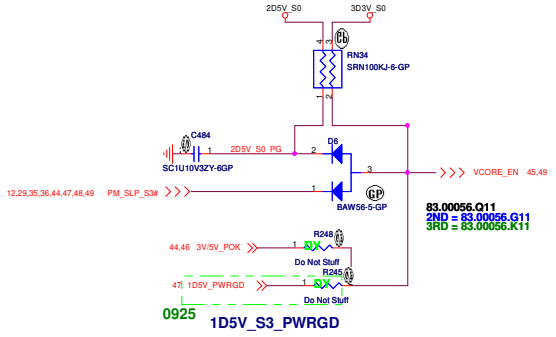
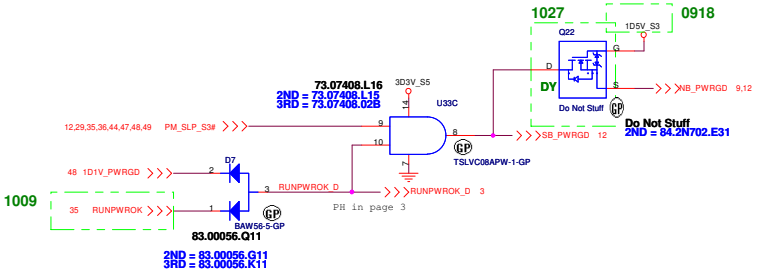
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	LED		
Size A3	Document Number JE40-DN		Rev -3
Date: Friday, March 26, 2010	Sheet 41 of 63		



P/H @ 1D8V_S3 PAGE



Diserete Madison Hynix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER ON LOGIC**

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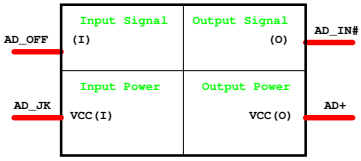
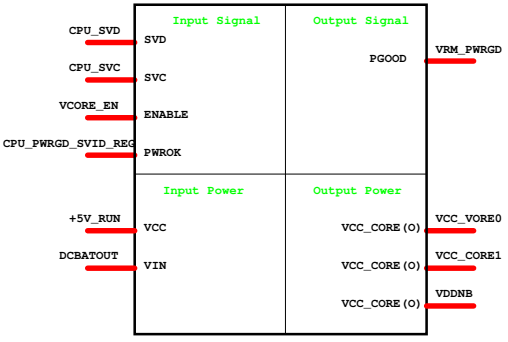
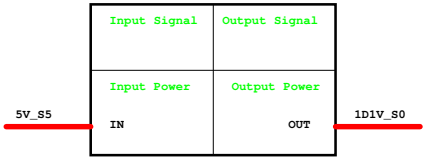
Adapter



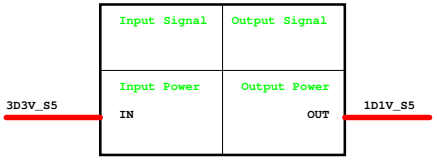
CPU_CORE
ISL6265HRTZ



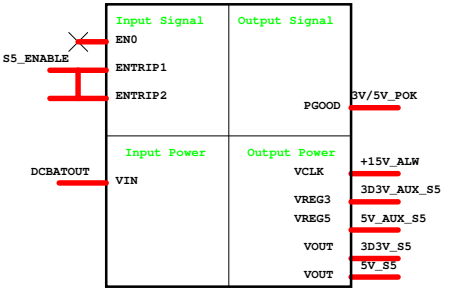
1D1V LDO RT8209E



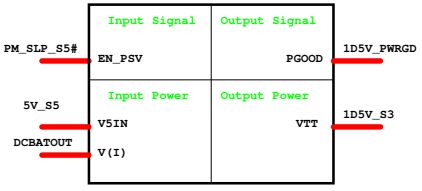
1D1V LDO RT9025



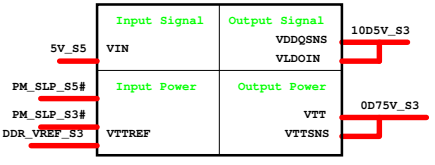
DCDC 5V/3D3V(RT8223)



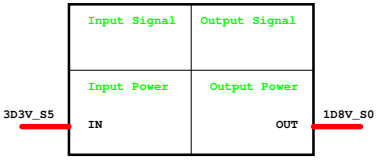
DCDC 1D5V(RT8209E)



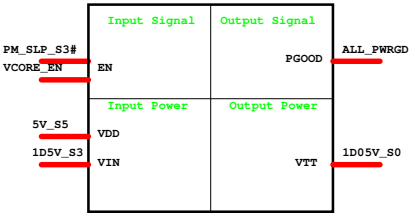
0D75V LDO RT9026



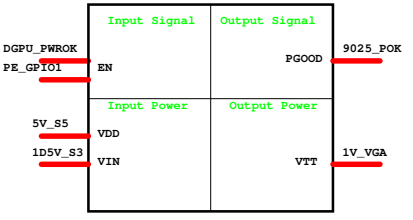
1D8V LDO RT8015A



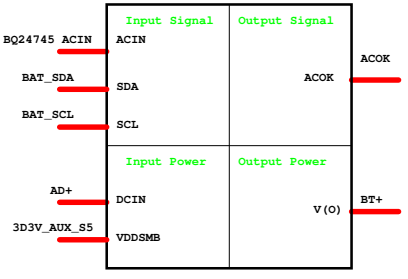
DCDC 1D05V_S0(RT9025)



DCDC 1V_VGA(RT9025)



CHARGER BQ24745



Diserete Madison Hynix

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Power Block Diagram		
Size: A3	Document Number: JE40-DN	Rev: -3
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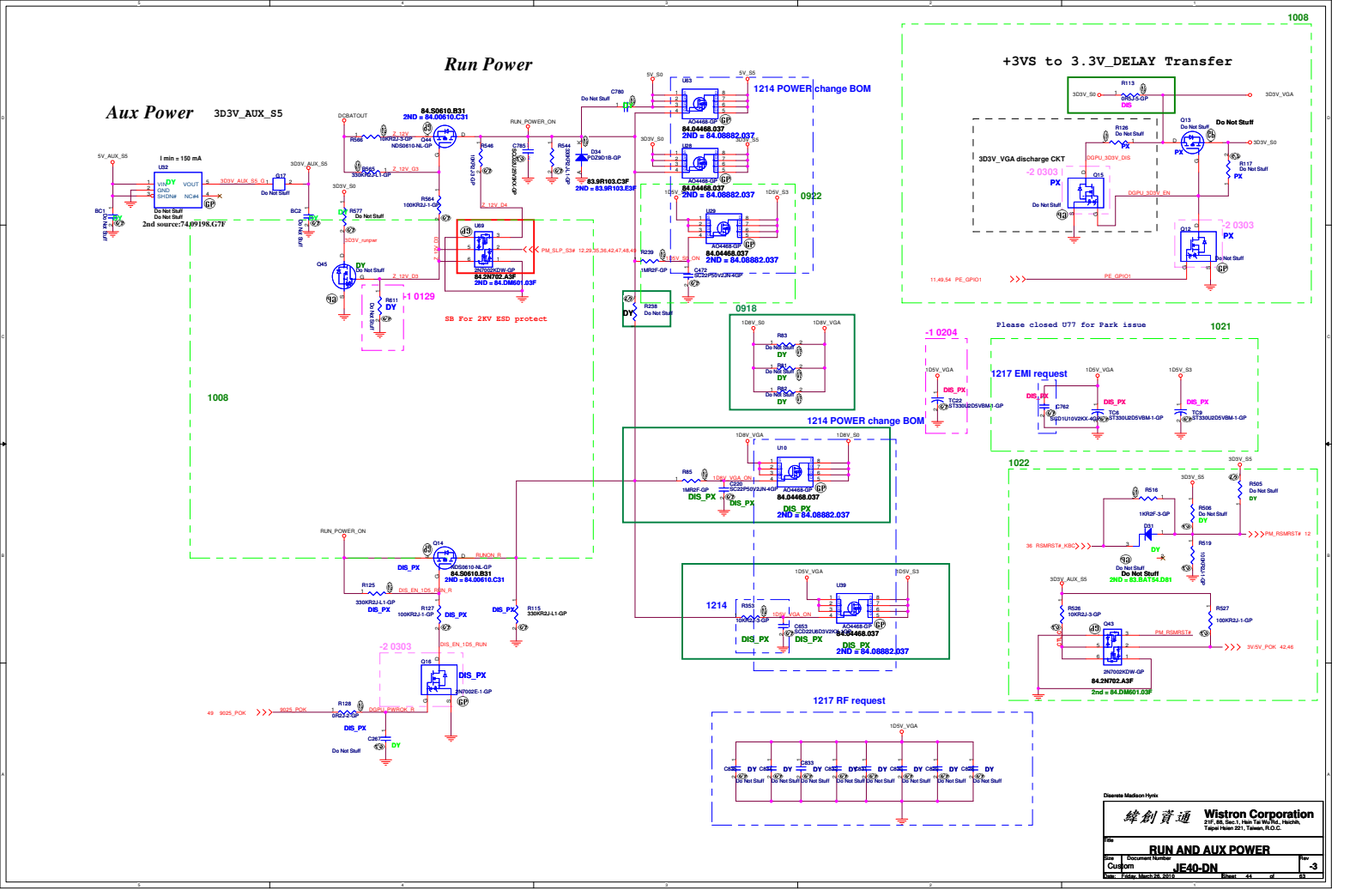
Run Power
Aux Power
3D3V_AUX_S5
+3VS to 3.3V_DELAY Transfer
1214 POWER change BOM
0922
0918
1008
1021
1214 POWER change BOM
1214 EMI request
1217 RF request
Please closed U77 for Park issue
SB For 2KV ESD protect
3D3V_VGA discharge CKT
Wistron Corporation
RUN AND AUX POWER
JE40-DN

1214 POWER change BOM
VCC_CORE_S0
Iomax=18A
OCP_min:24A
20091001 Wayne
2ND = 77.C3371.051
Parts close to PWM IC
R402 close to L37
-1 0202 for EMI request
1214 POWER change BOM
20091001 WAYNE
1022 change 74.06265.C73-->74.06265.B73
74.06265.B73
change to 74.06265.A73
20091001
1001
Close to CPU socket
Parallel
R379 close to L38
2ND = 77.C3371.051
1214 POWER change BOM
20091001 WAYNE
Diserete Madison Hynix
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore(ISL6265HR)
Size
Custom
Document Number
JE40-DN
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-3
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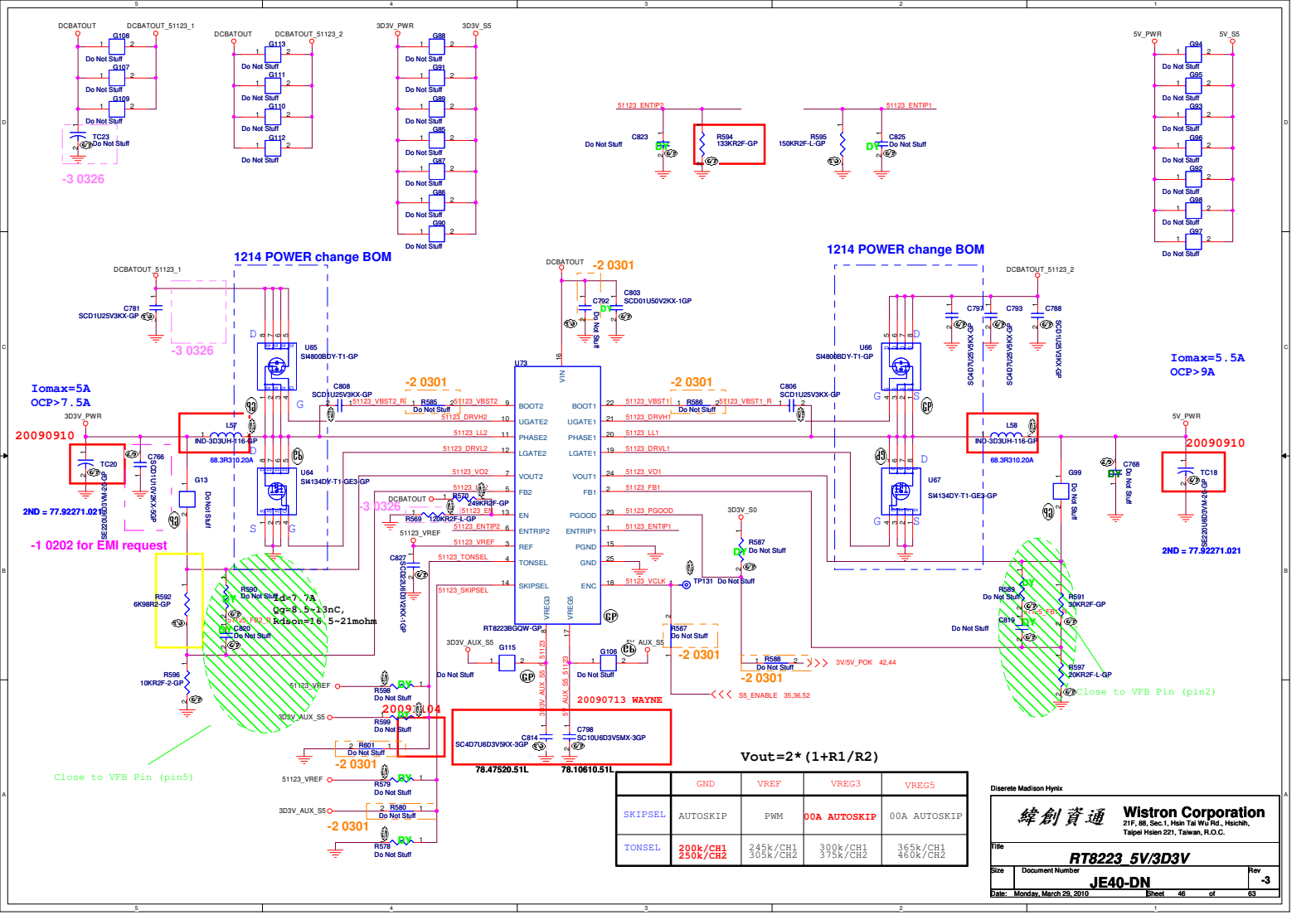
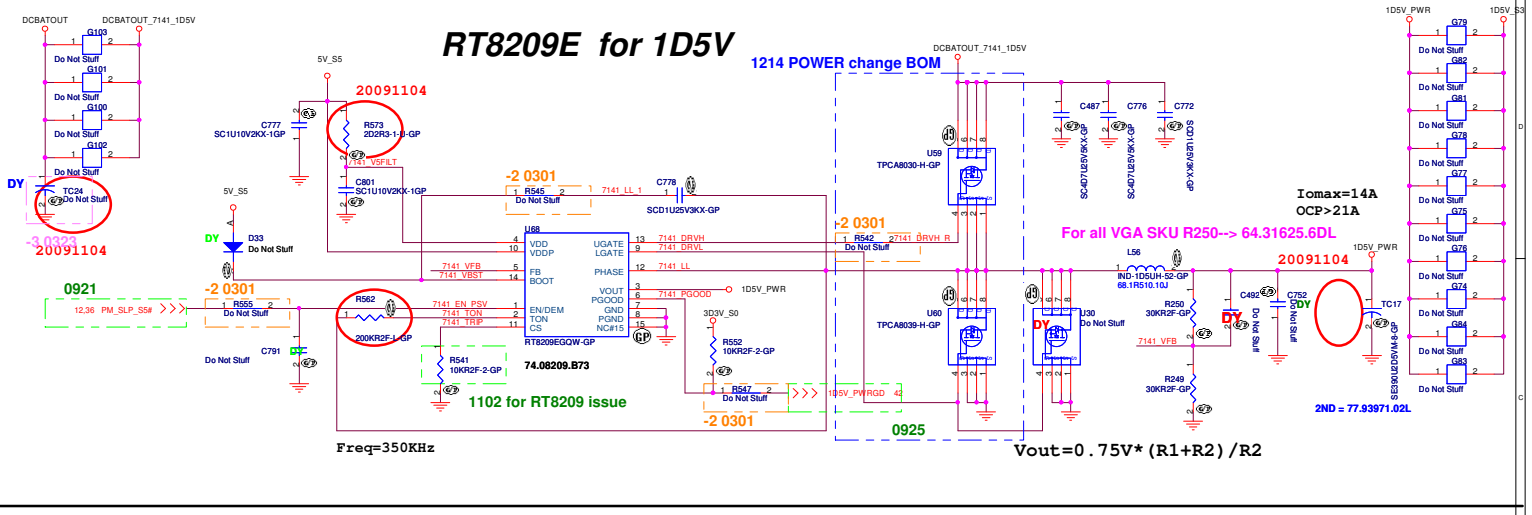
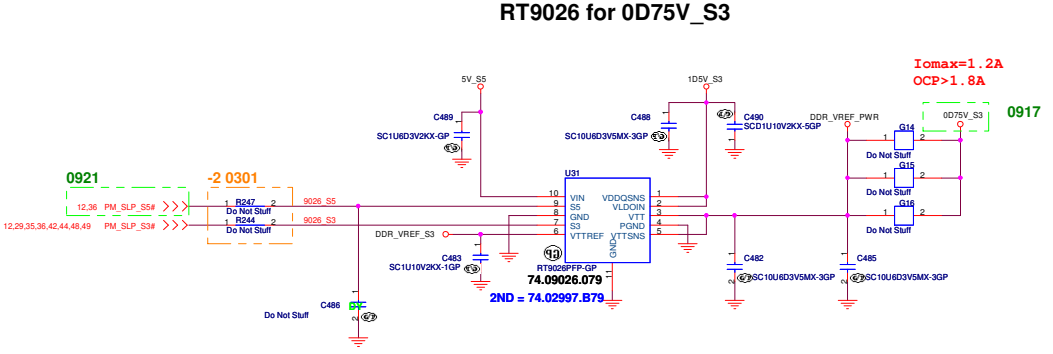


	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2





Diserete Madison Hynix

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Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209E_1D5V	
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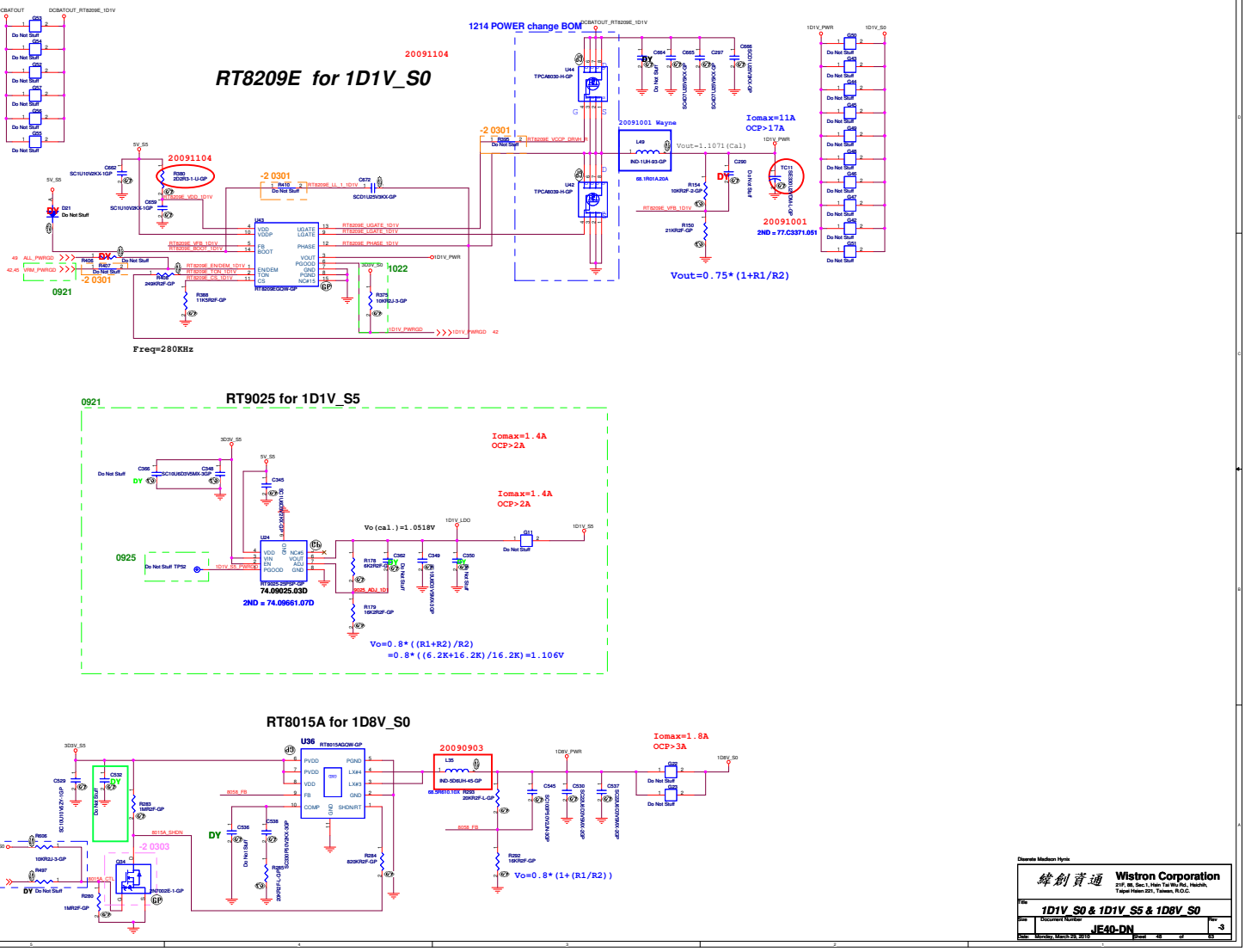
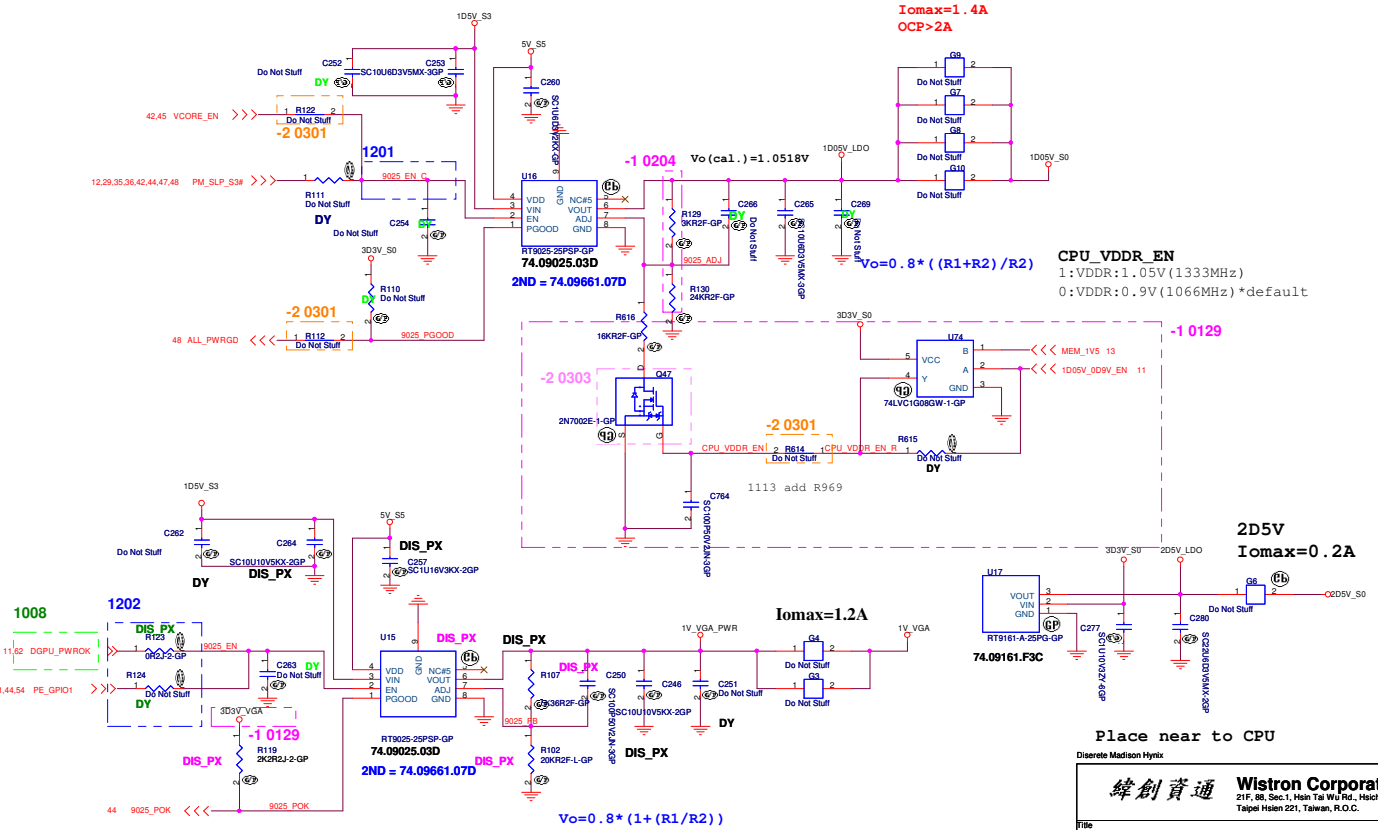
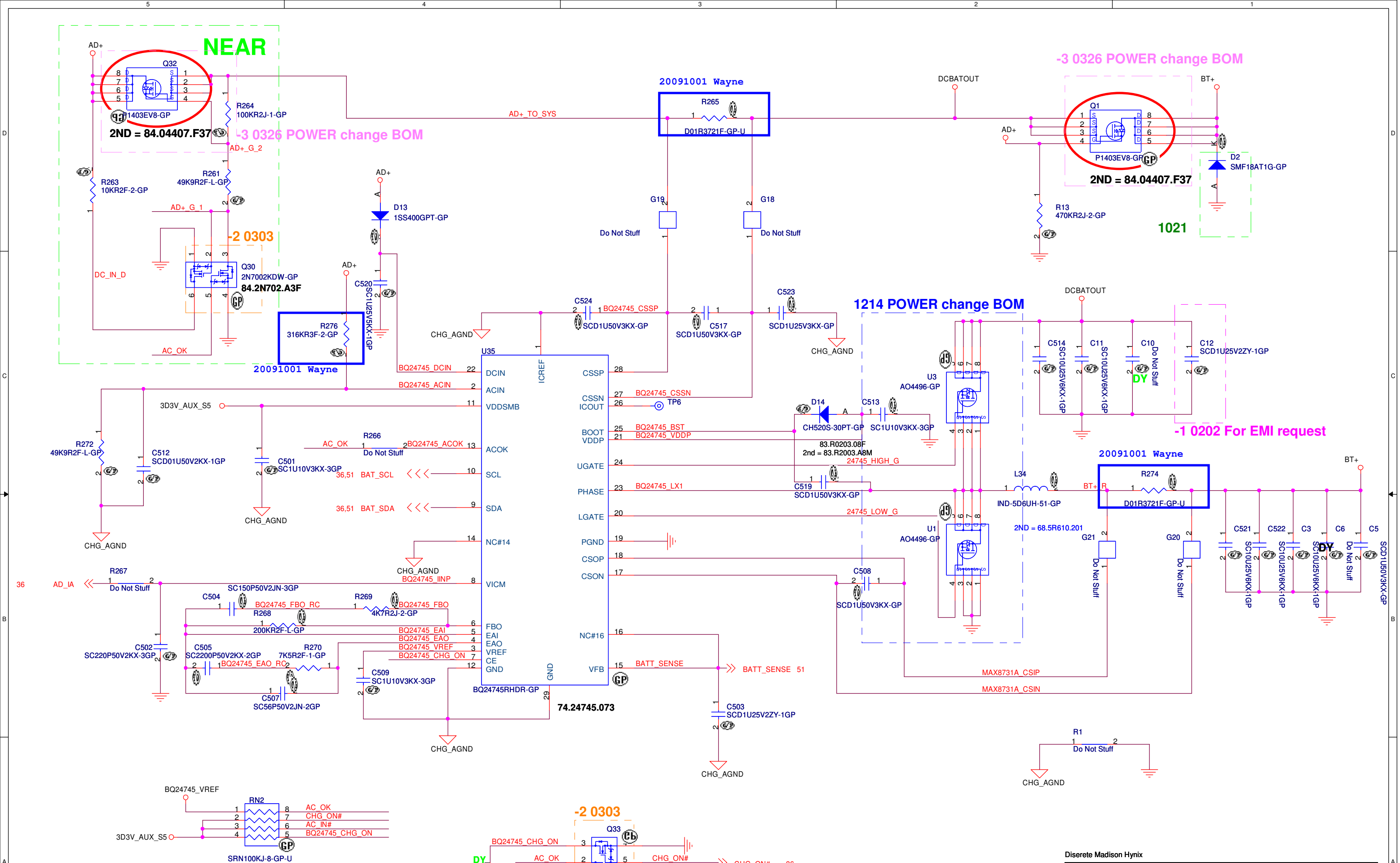
0917


RT8209E for 1D1V_S0
20091104
1214 POWER change BOM
Freq=280KHz
Vout=0.75*(1+R1/R2)
Iomax=11A
OCP>17A
20091001
2ND = 77.C3371.051
RT9025 for 1D1V_S5
Iomax=1.4A
OCP>2A
Vo(cal.)=1.0518V
Vo=0.8*((R1+R2)/R2)
=0.8*((6.2K+16.2K)/16.2K)=1.106V
RT8015A for 1D8V_S0
Iomax=1.8A
OCP>3A
20090903
Vo=0.8*(1+(R1/R2))
Wistron Corporation
1D1V_S0 & 1D1V_S5 & 1D8V_S0
JE40-DN

RT9025 for 1D05V_S0



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: LDO 1D05V/2D5V/1V			
Size: A3	Document Number: JE40-DN		Rev: -3
Date: Friday, March 26, 2010	Sheet 49 of 63		



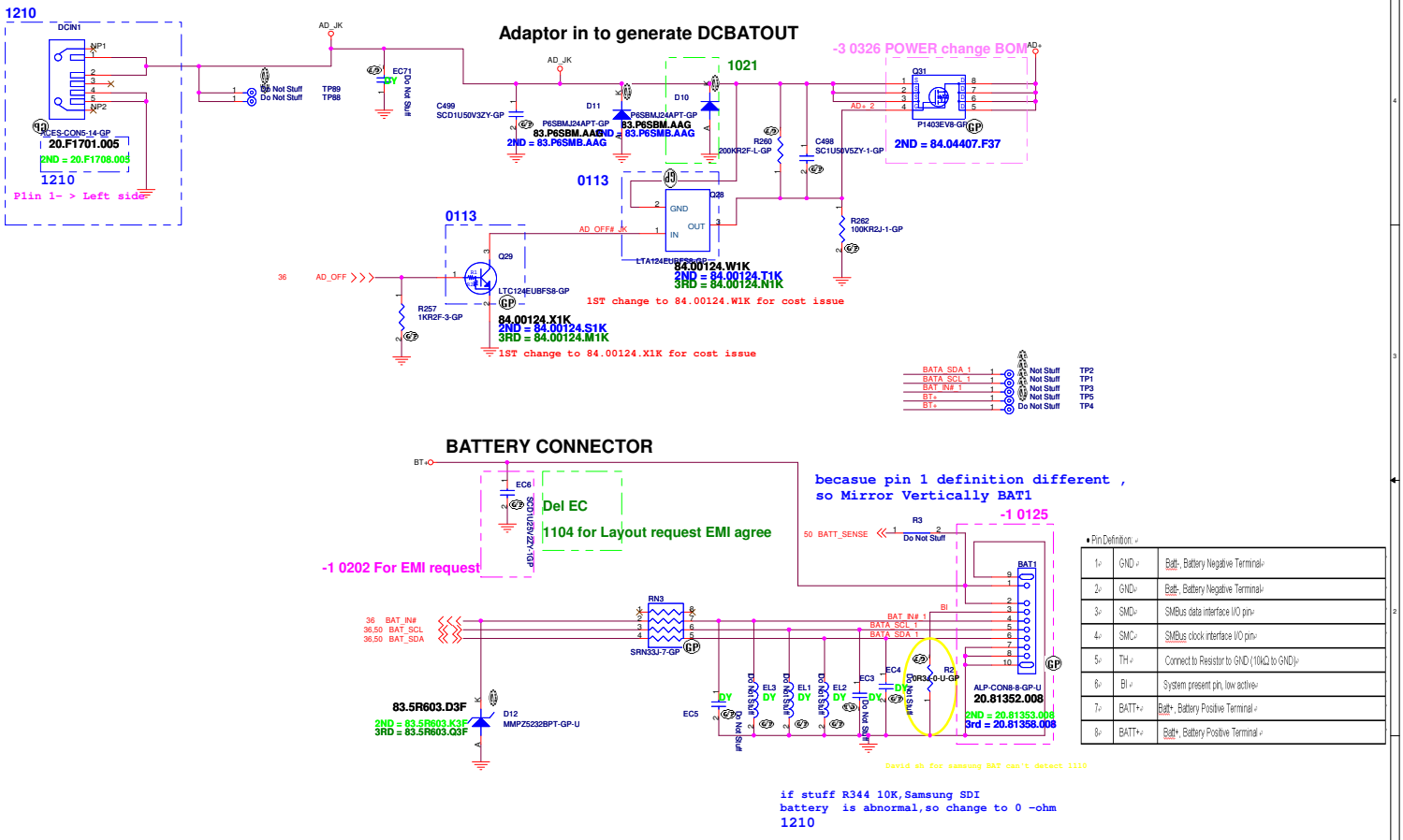
Diserete Madison Hynix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24745 Charger**

Size: A3 | Document Number: JE40-DN | Rev: -3

Date: Tuesday, March 30, 2010 | Sheet 50 of 63



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

Diserete Madison Hynix

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Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

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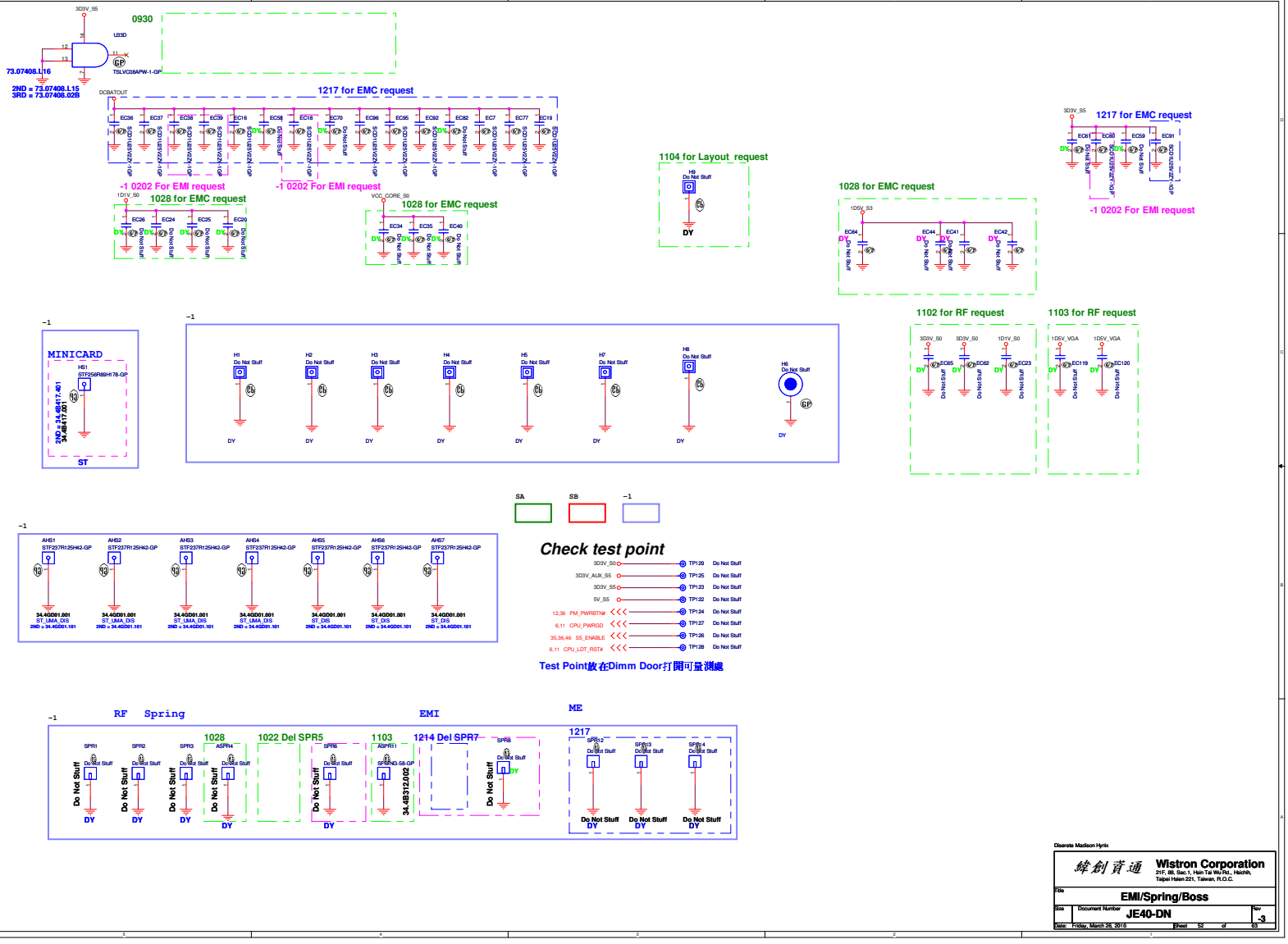
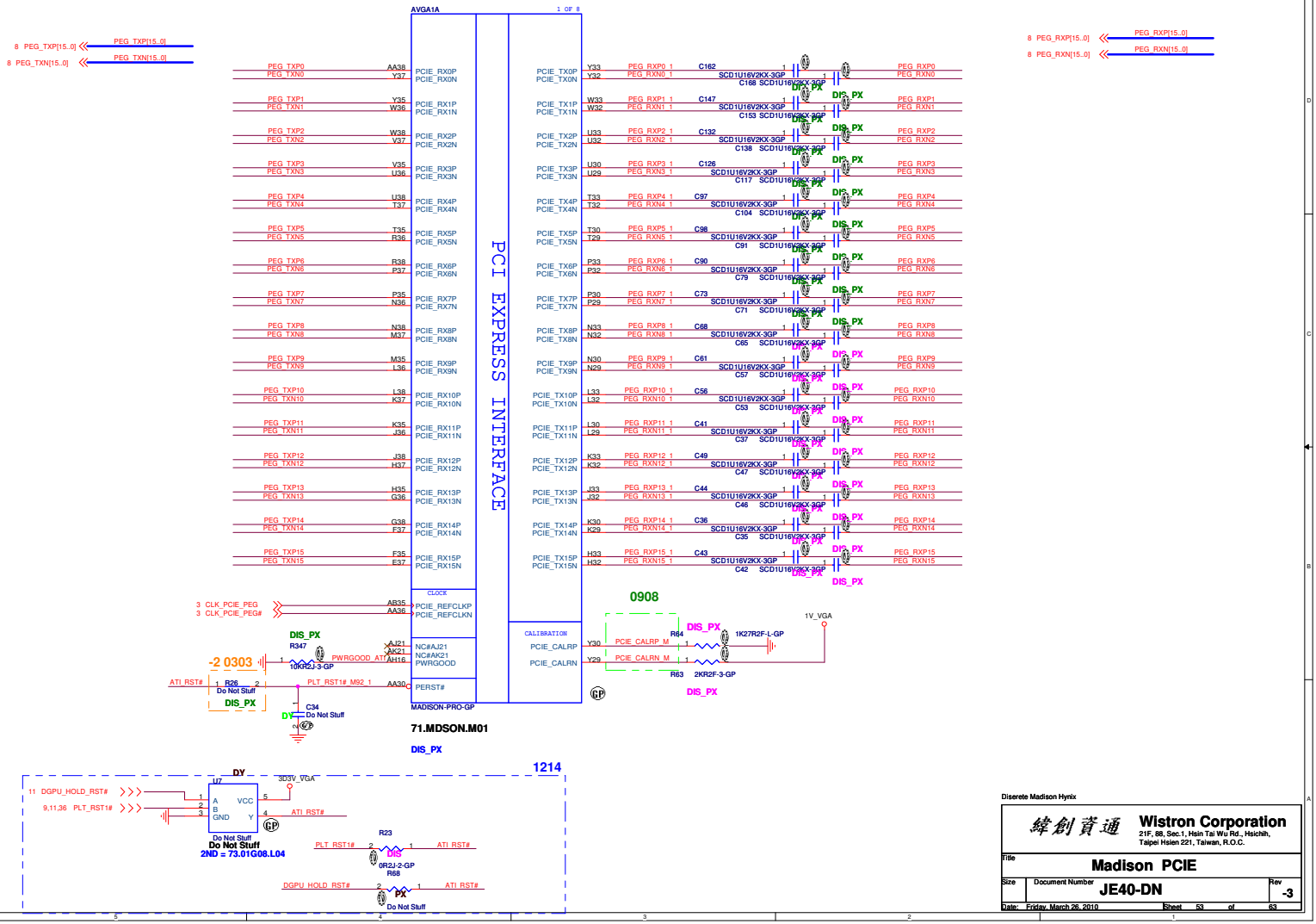


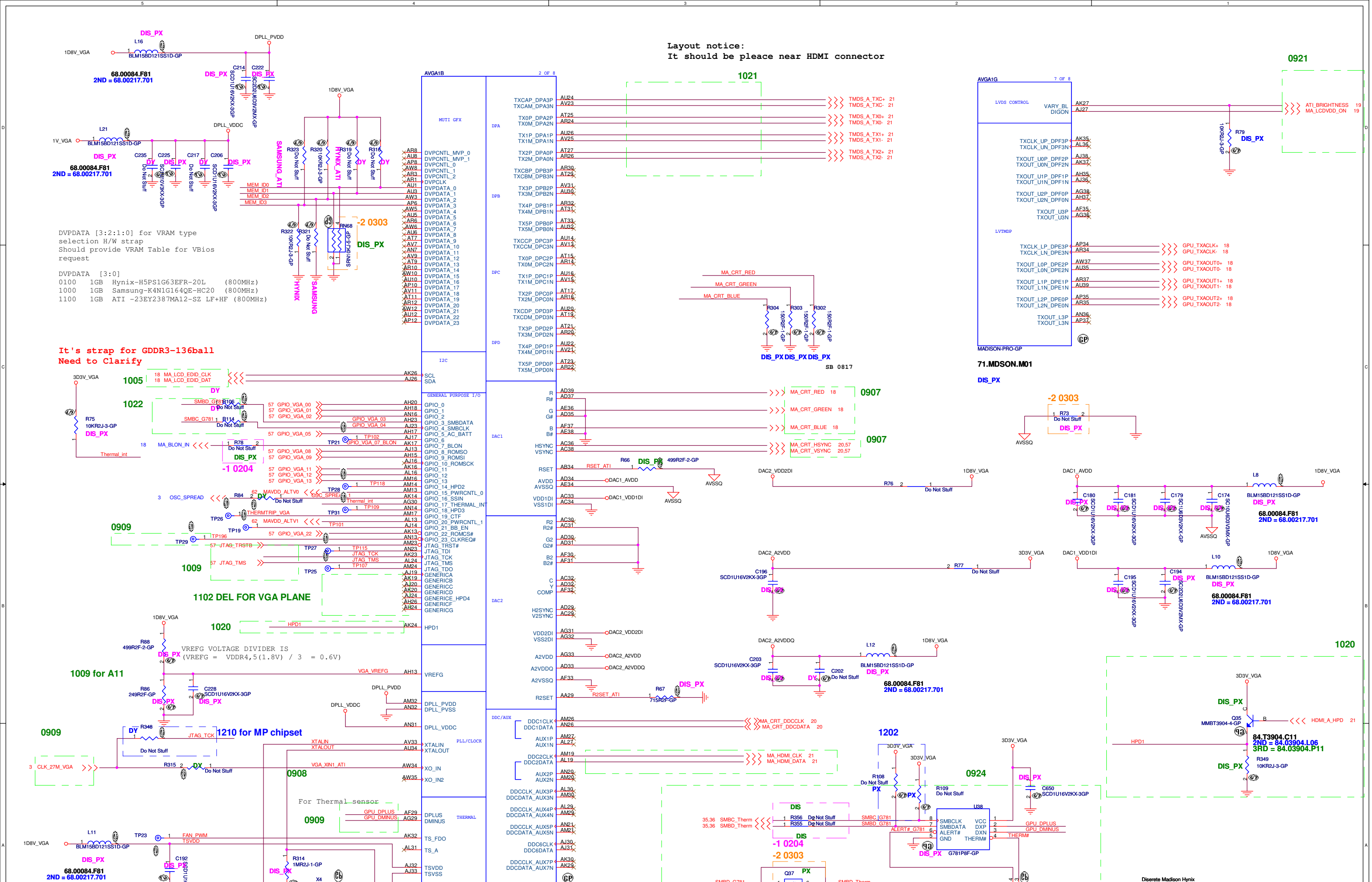
Discrete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	EMI/Spring/Boss	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 52 of 63	



Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Madison PCIE	
Size	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 53 of 63	



Discrete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison IO

Size | Document Number: JE40-DN | Rev: -3

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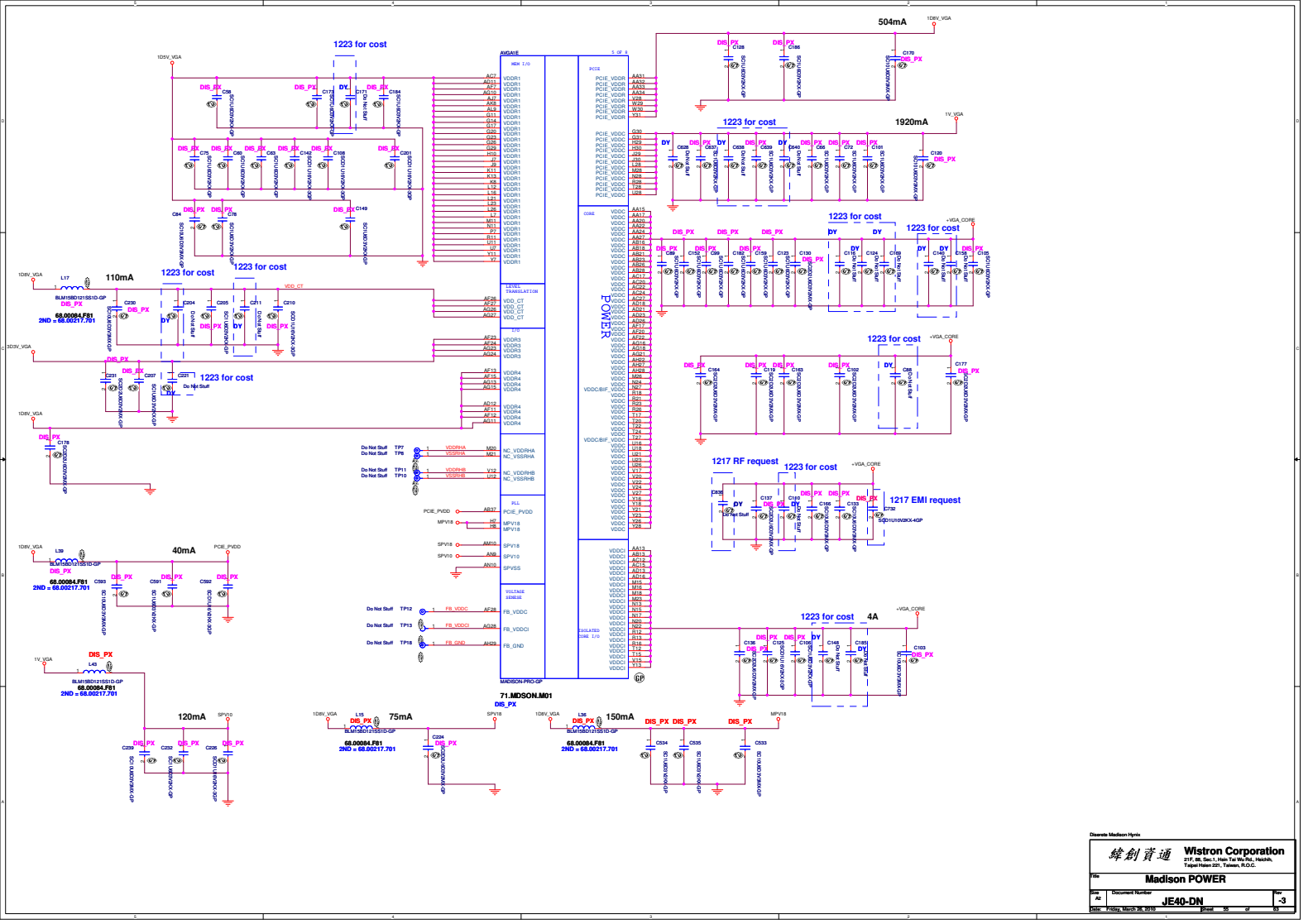
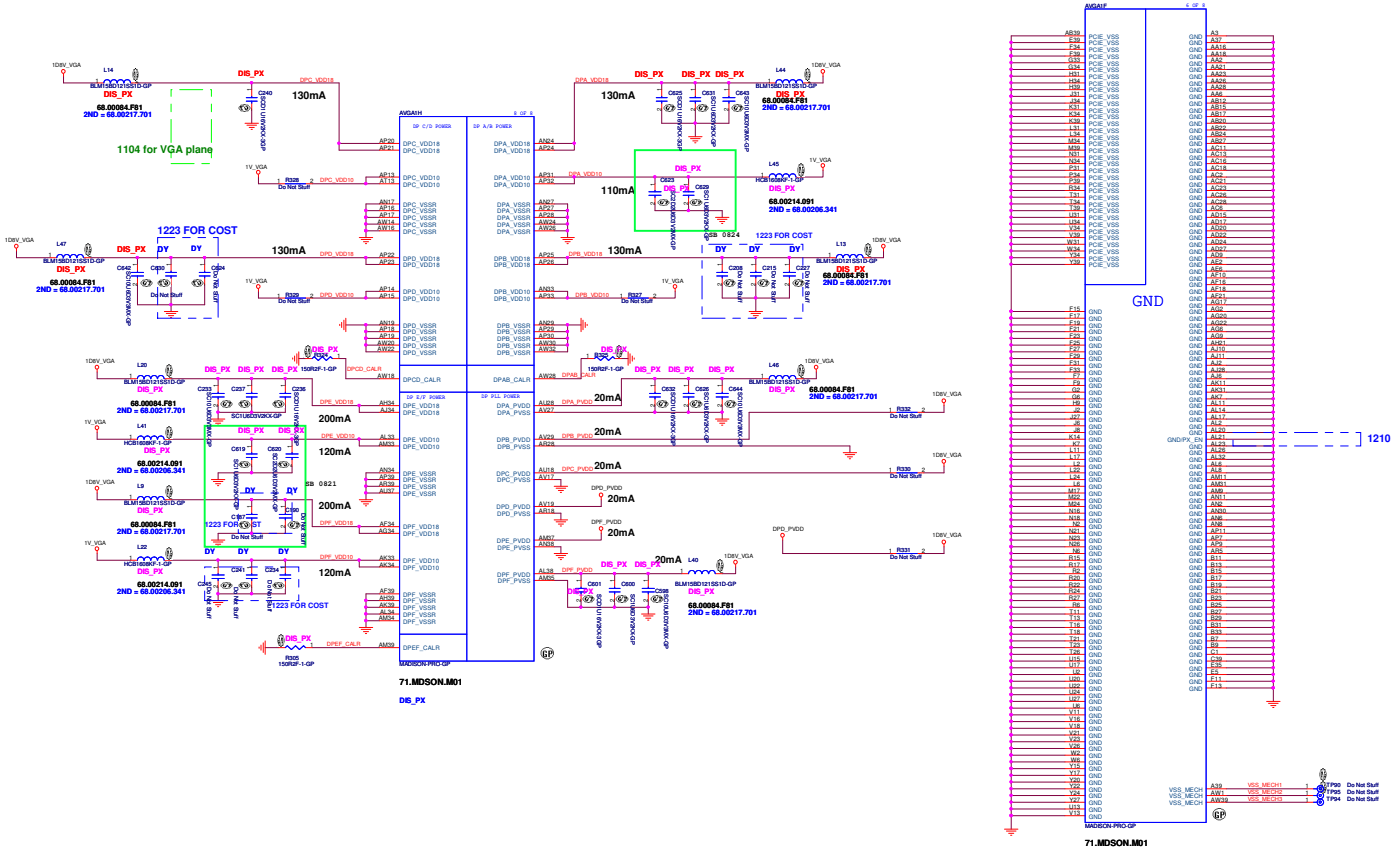


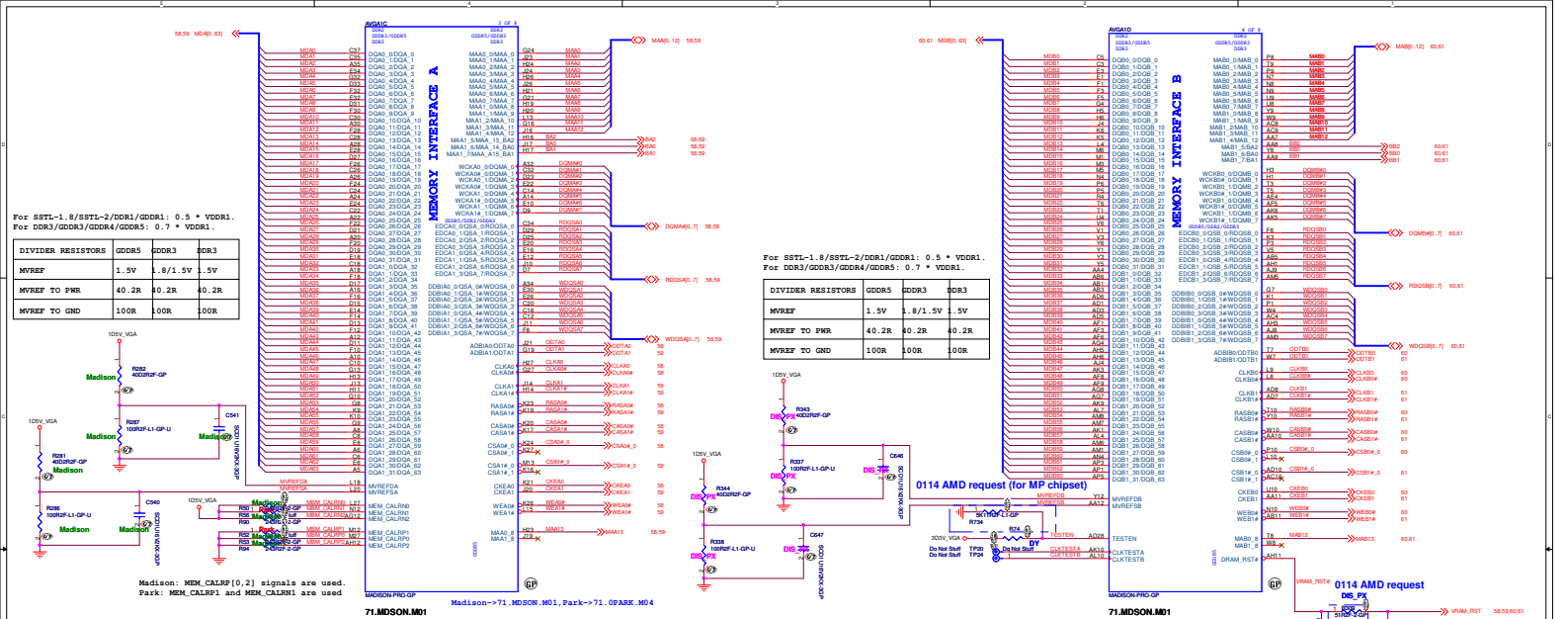
Discrete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title:	Madison POWER	
Size: A0	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 55 of 63	



Discrete Madison Hynix

緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size: A2	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 56 of 63	



STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	x
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	x
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	51R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

1103
1026
1210 for MP chipset
1210 for MP chipset

Discrete Madison Hynix

Wistron Corporation
2nF, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

Size	Document Number	Rev
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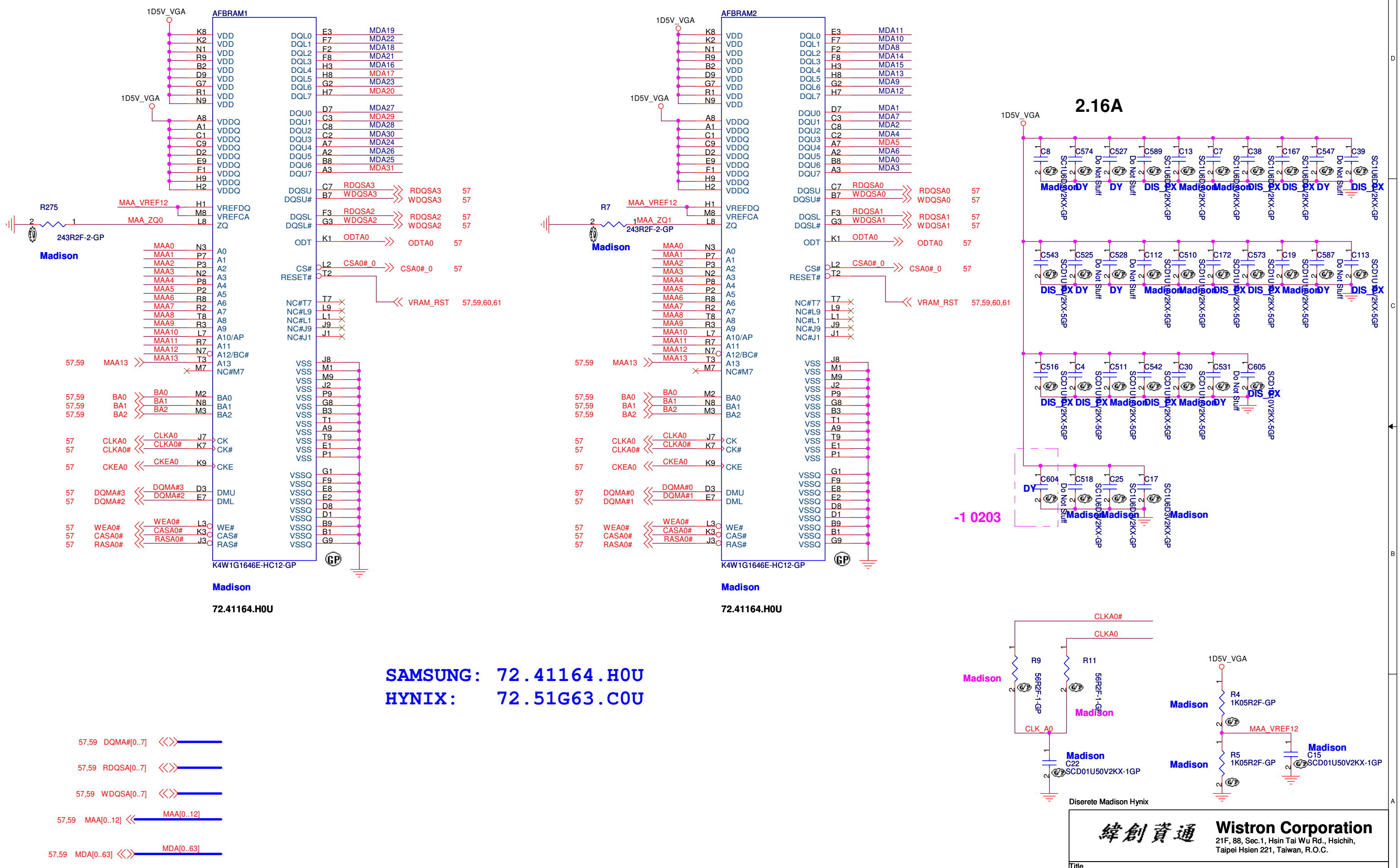
DDR3

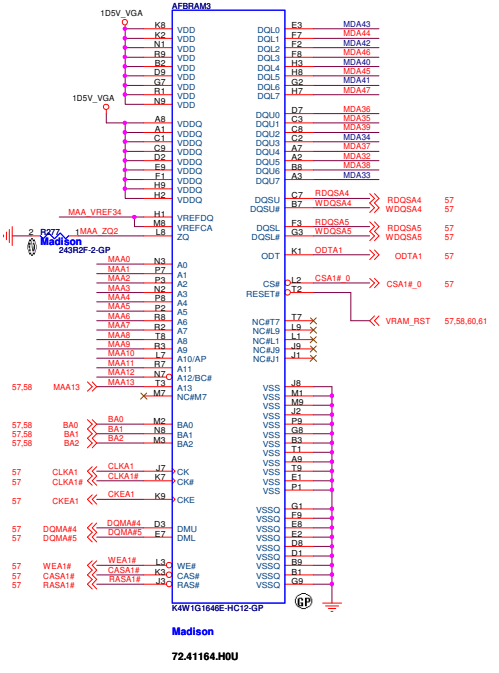


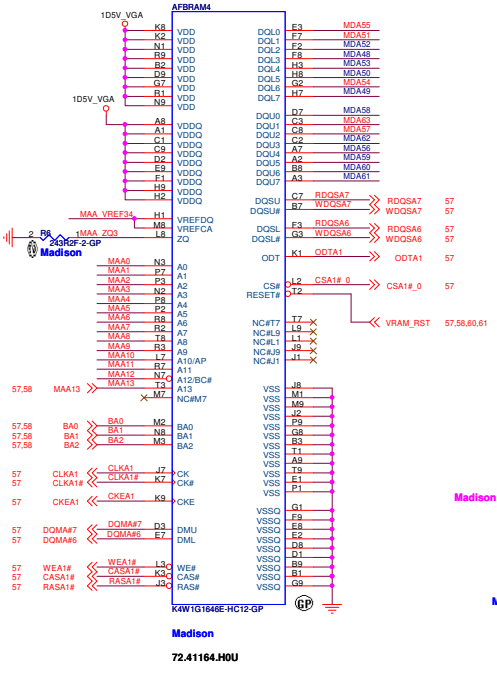
SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

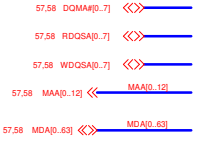
Title	VRAM(1/4)	
Size: A3	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 58 of 63	

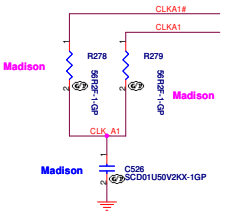
DDR3

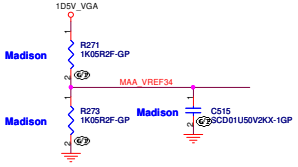




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U







Diserete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(2/4)**

Size	Document Number	Rev
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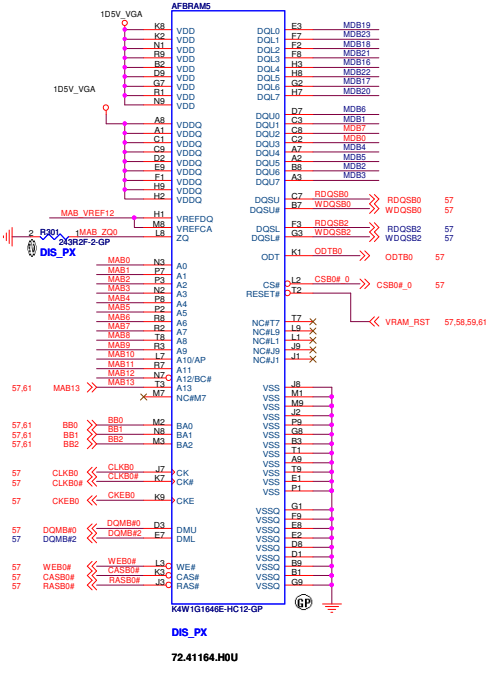
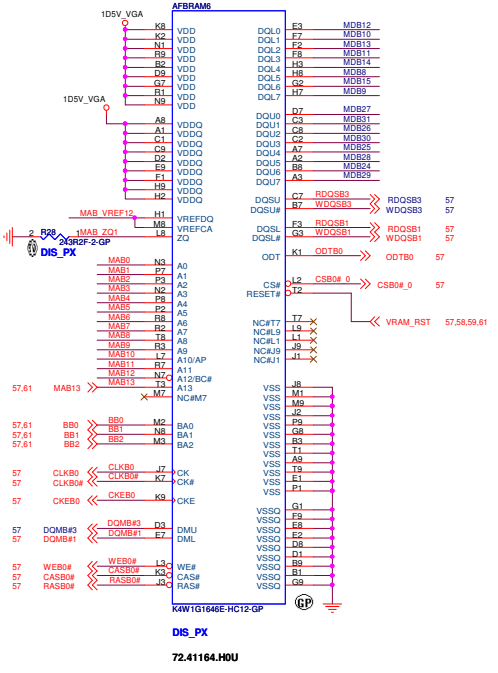
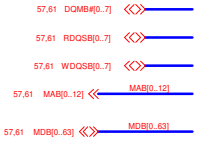
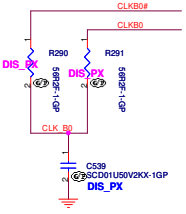
DDR3

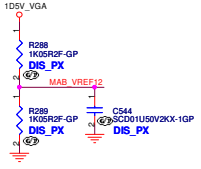




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U







Diserete Madison Hynix

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(3/4)		
Size: A3	Document Number: JE40-DN	Rev: -3
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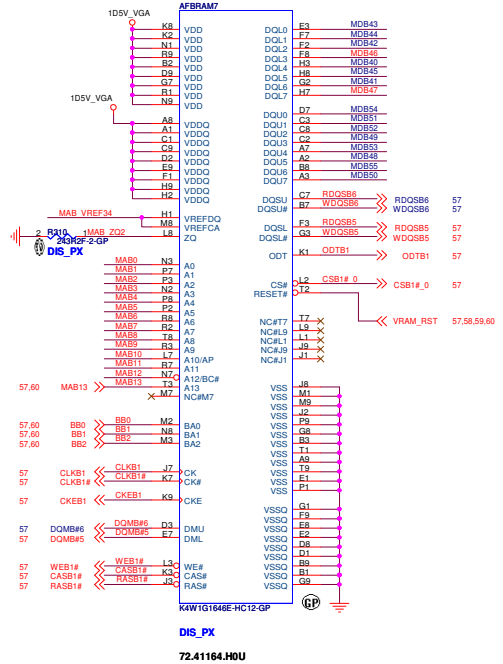
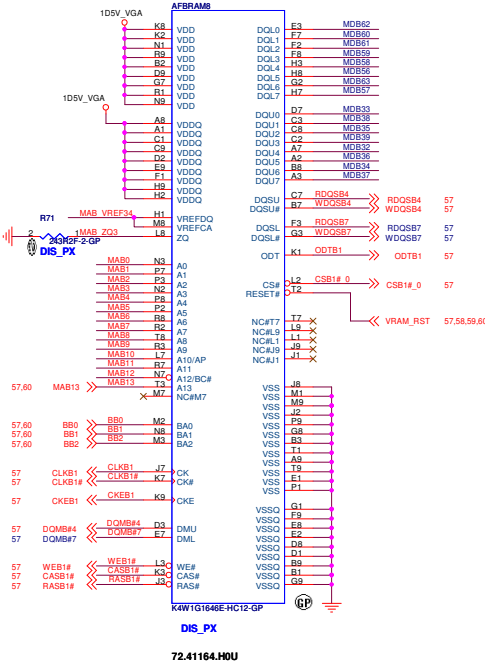
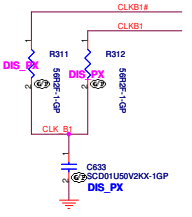
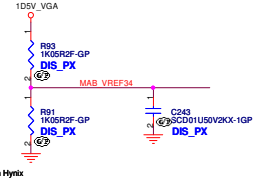
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(4/4)***	
Size A3	Document Number **JE40-DN**	Rev -3
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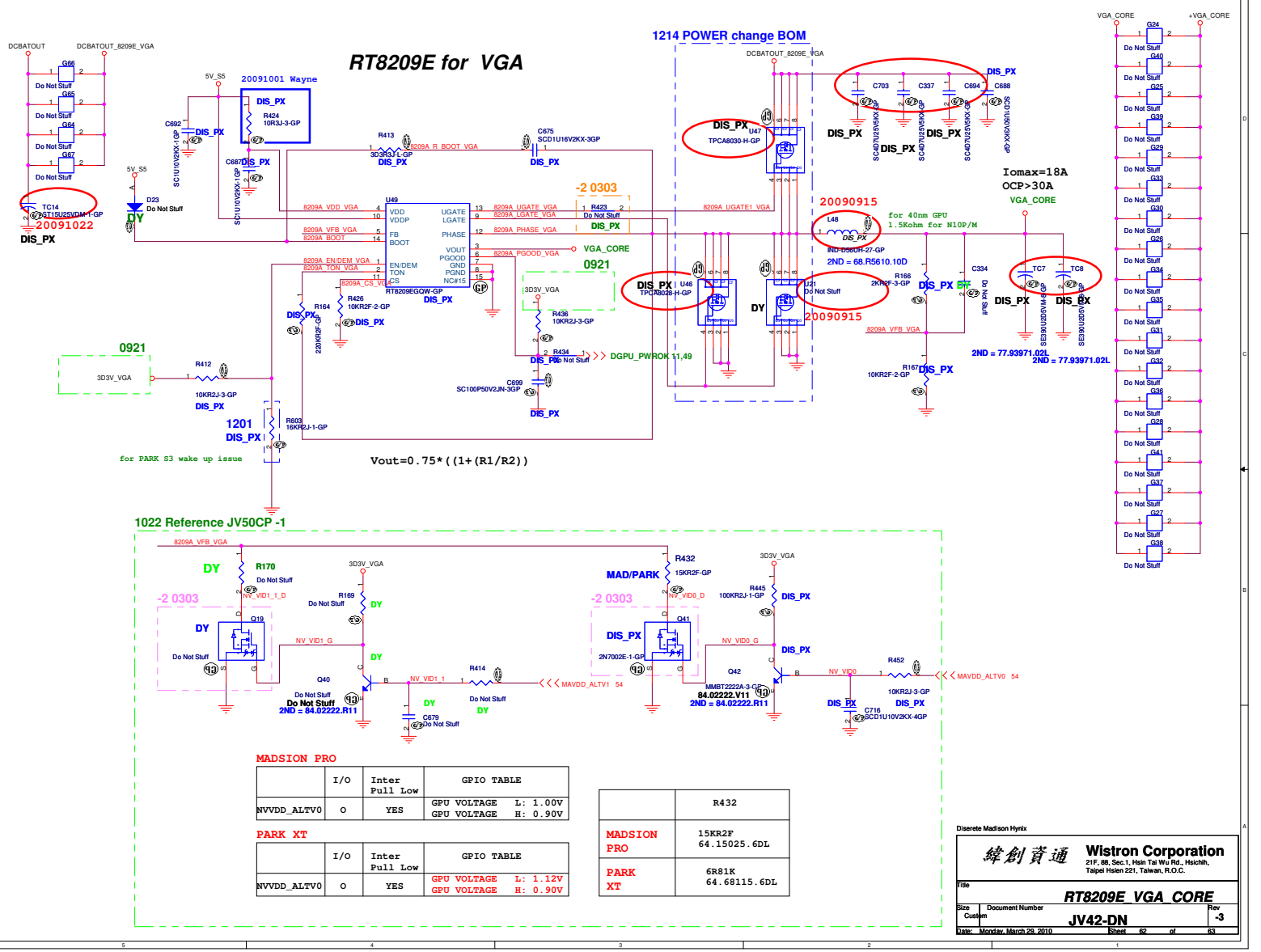
RT8209E for VGA
1214 POWER change BOM
20091001 Wayne
20091022
20090915
0921
0921
-2 0303
-2 0303
1201
DIS_PX
DY
Do Not Stuff
VGA_CORE
+VGA_CORE
Iomax=18A
OCP>30A
for 40nm GPU
1.5Kohm for N10P/M
2ND = 68.R5610.10D
2ND = 77.93971.02L
for PARK S3 wake up issue
Vout=0.75*((1+(R1/R2))
DGPU_PWROK 11,49
1022 Reference JV50CP -1
MADSION PRO
PARK XT
Wistron Corporation
RT8209E_VGA_CORE
JV42-DN

NB

RS780-->RS880M

71.RS780.M02-->71.RS880.M02

SB

SB820M-1-GP

71.SB820.00U-->71.SB820.M03

SATA_CALRP

A11: 80歐姆 1% resistor to GND

A12: TBD歐姆 1% resistor to GND

SATA_CALRN

A11:A11: 931歐姆1% resistor to VDDAN_11_SATA

A12: TBD歐姆 1% resistor to VDDAN_11_SATA.

BOM

1st -> All SKU

R250

Madison-->R250 64.32425.6DL R402H16 32K4R2F

Park -->R250 64.32425.6DL R402H16 32K4R2F

PX -->R250 64.32425.6DL R402H16 32K4R2F

VGA

Madison--> PN:71.MDSON.M01

Park--> PN:71.0PARK.M04

VRAM

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

ATI--> VRAM FBRAM1~8 PN: VR.1GB0T.002

CRT

UMA-->L1-->2R 0603

C62-->47U/6.3V

DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)

C62-->DY

PX--> 133 歐姆 (R58 63.10334.1DL R402H16 133R2F-GP)

R605(MAD/PARK/PX)

Madison-->R605 64.15005.6DL R402H16150R2F-L-GP

Park -->R605 64.15005.6DL R402H16150R2F-L-GP

PX -->R605 64.15005.6DL R402H16150R2F-L-GP

HDMI

UMA -->R612 R613 R618 R619 R620 R621 R624 R625 64.71505.6DL R402H16715R2F-2-GP

R432(MAD/PARK)

Madison-->15KR2F 64.15025.6DL

Park-->R432 64.68115.6DL R402H16 6.81KR2F

Diserete Madison Hynix

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NOTE

Size: A3 | Document Number: JV42-DN | Rev: -3

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