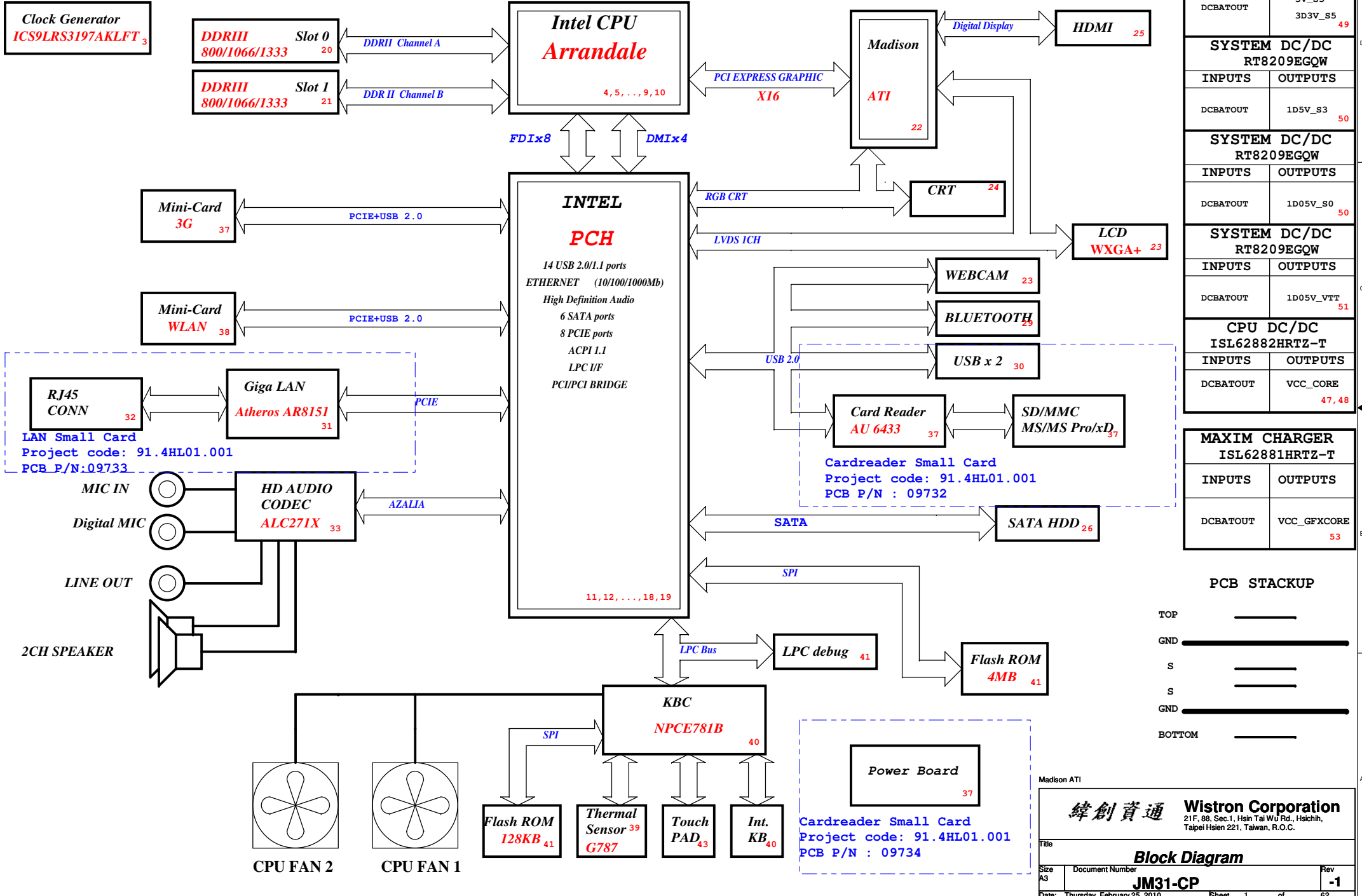


# JM31-CP Block Diagram

Project code: 91.4HL01.001

PCB P/N : 48.4HL01.031

REVISION : 09921-3



Madison ATI

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size A3 Document Number **JM31-CP** Rev **-1**

Date: Thursday, February 25, 2010 Sheet 1 of 62

# PCH Strapping

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)</b> = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

# Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	<b>Clarksfield (only for early samples pre-ES1) -</b> Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

## USB Table

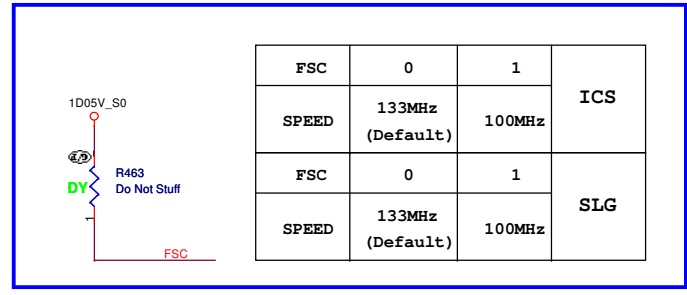
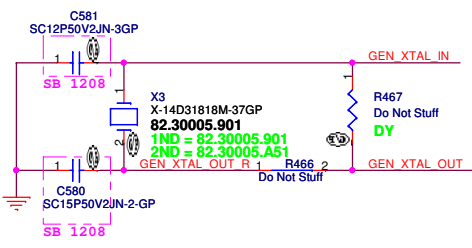
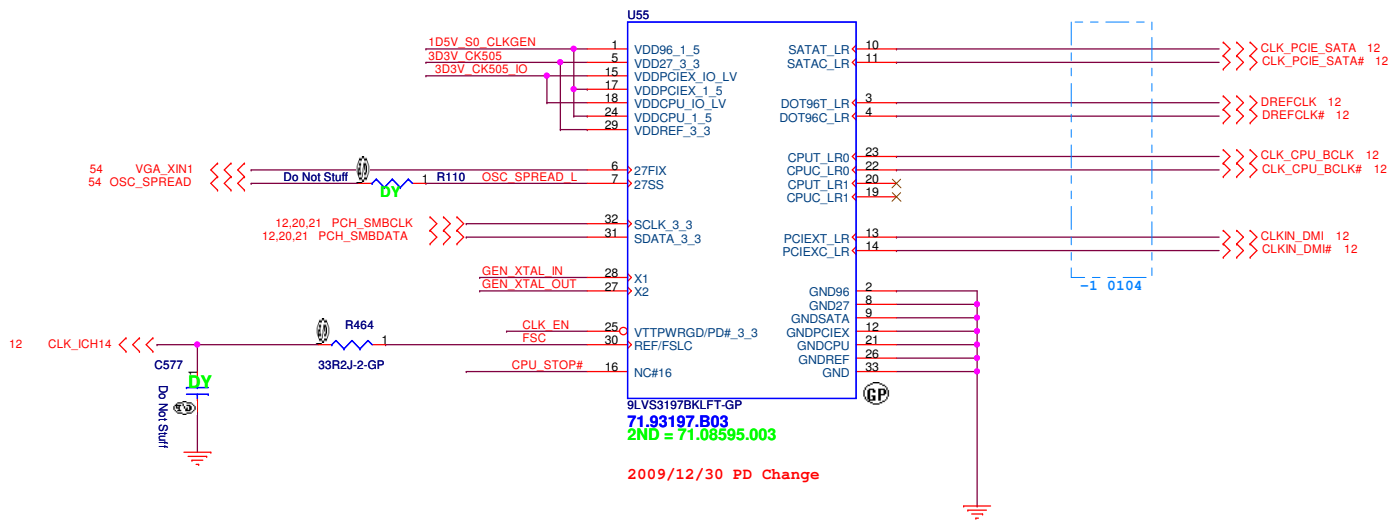
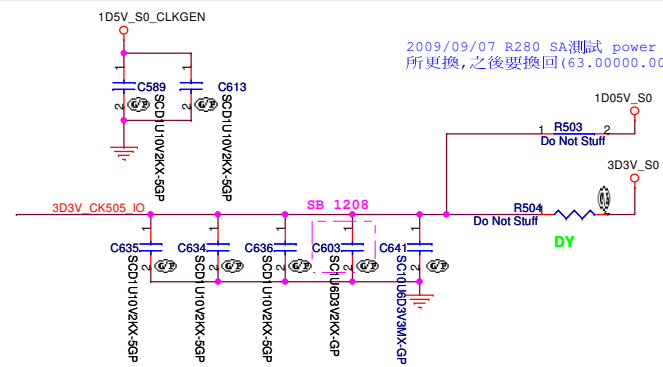
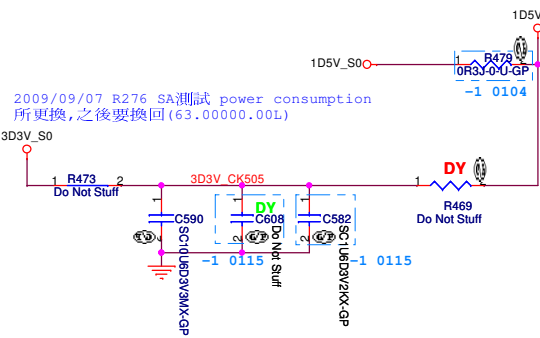
Pair	Device
0	USB1
1	USB2
2	USB4
3	MINICARD2
4	WECAM
5	Blue Tooth
6	MINIC1
7	Cardreader
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC

## PCIE Routing

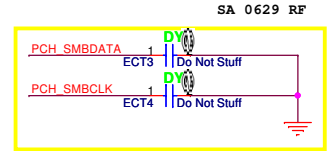
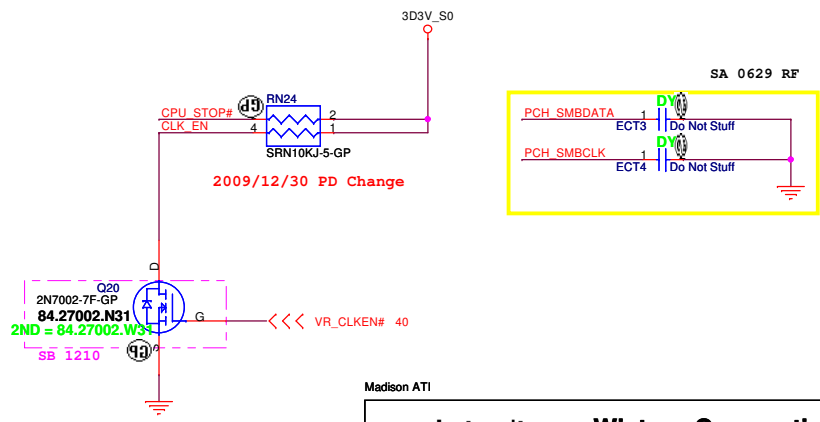
LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

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<b>Table of Content</b>			
Title			
Size A3	Document Number	Rev	
	<b>JM31-CP</b>	<b>SA</b>	
Date: Thursday, February 25, 2010	Sheet 2	of	62



FSC	0	1	ICS
SPEED	133MHz (Default)	100MHz	
FSC	0	1	SLG
SPEED	133MHz (Default)	100MHz	



SA 0929

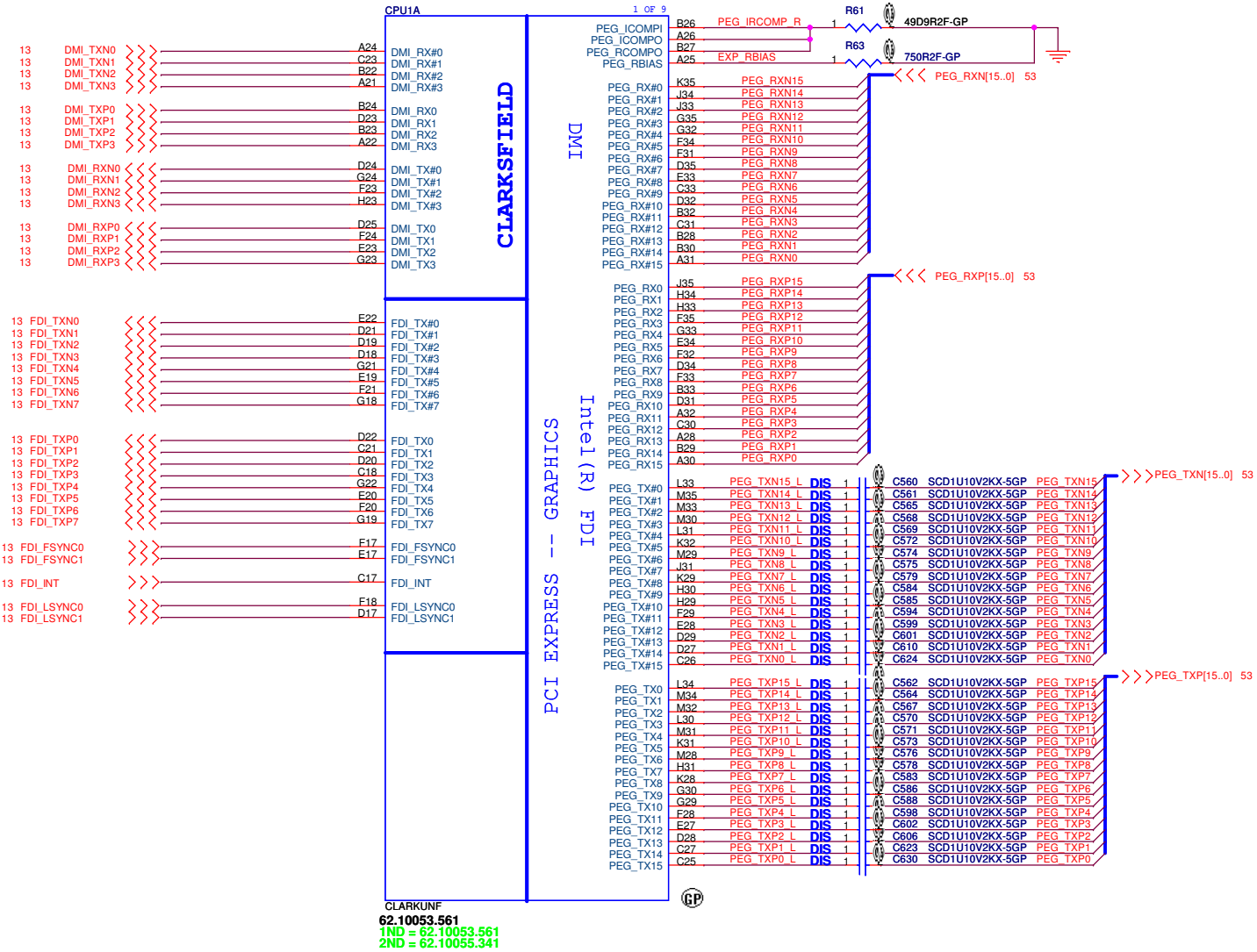
Madison ATI

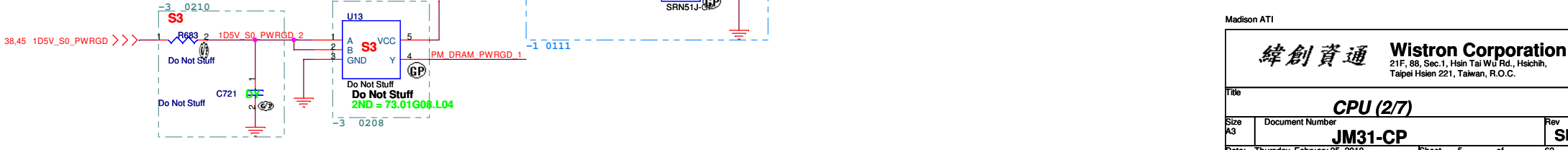
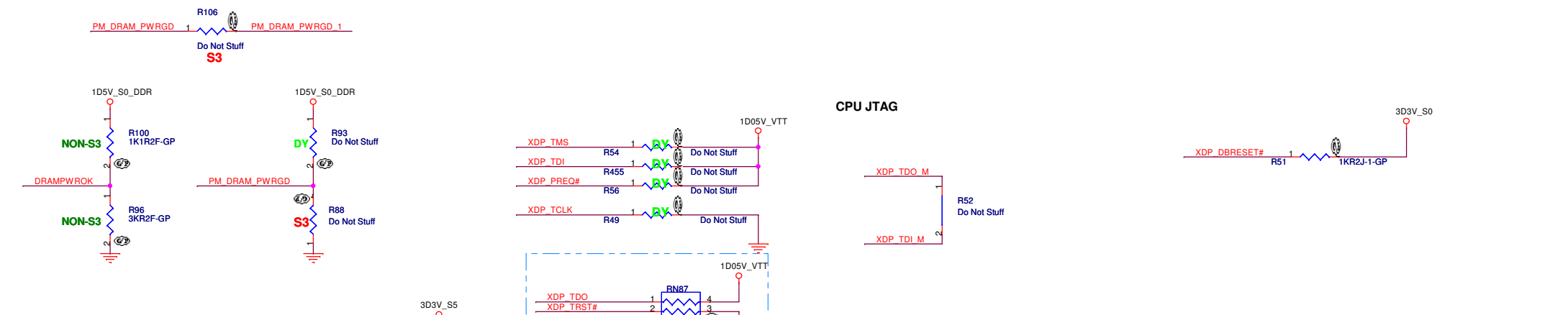
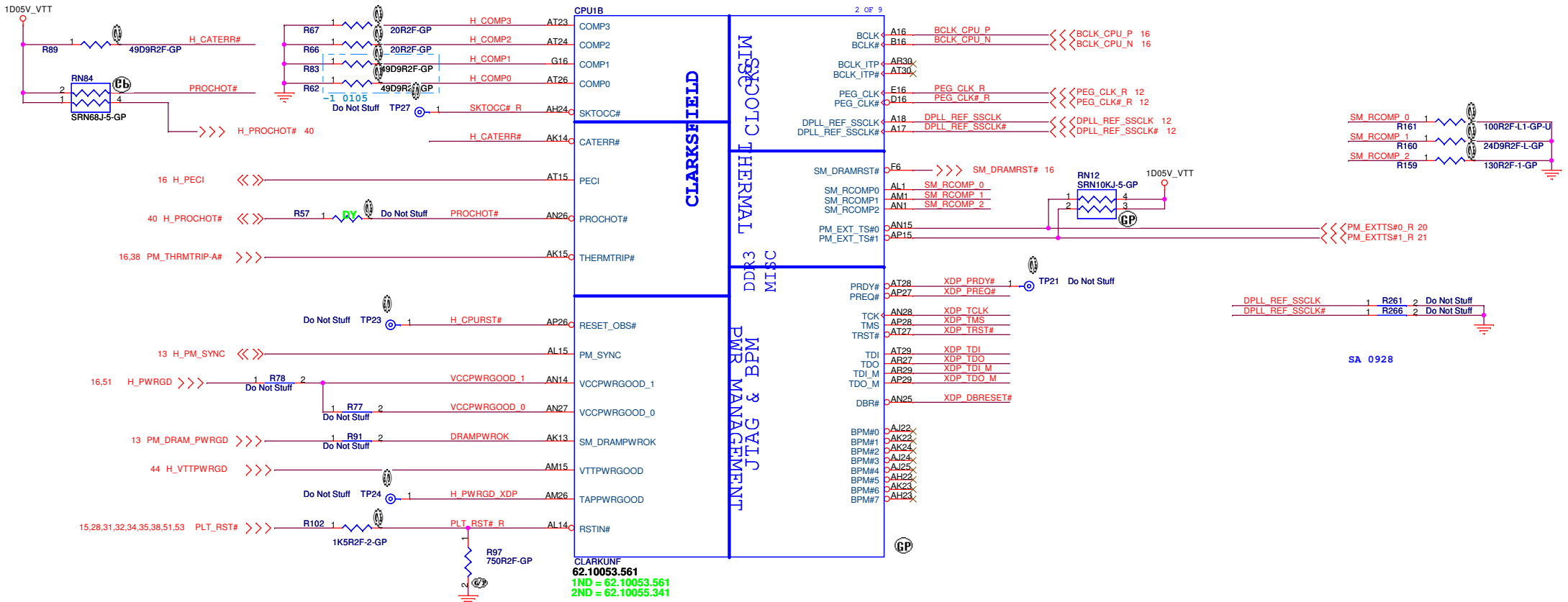
**緯創資通 Wistron Corporation**  
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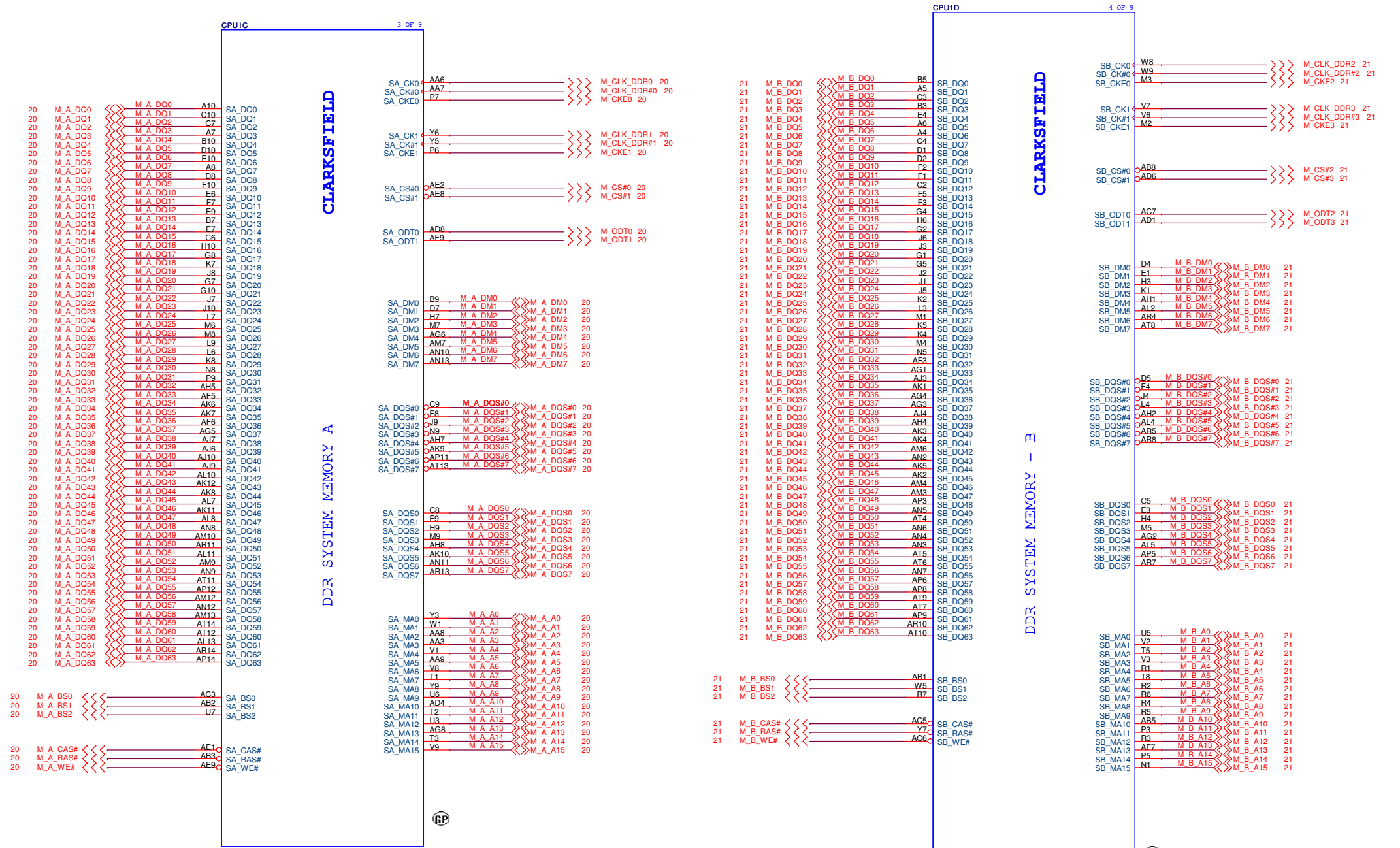
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Size A3 Document Number: **JM31-CP** Rev: **-1**

Date: Thursday, February 25, 2010 Sheet 3 of 62







CLARKUNF  
**62.10053.561**  
 1ND = 62.10053.561  
 2ND = 62.10055.341

CLARKUNF  
**62.10053.561**  
 1ND = 62.10053.561  
 2ND = 62.10055.341

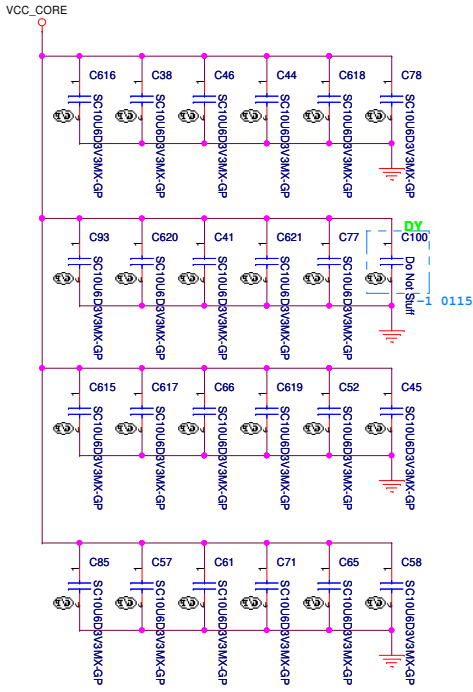
Madison AT1

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (3/7)**

Size A3 | Document Number: **JM31-CP** | Rev: **SA**

Date: Thursday, February 25, 2010 | Sheet 6 of 62



**PROCESSOR CORE POWER**

VCC\_CORE  
**48A**

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
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- R28 VCC
- R27 VCC
- P35 VCC
- P34 VCC
- P33 VCC
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- P28 VCC
- P27 VCC
- P26 VCC

**CLARKSFIELD**

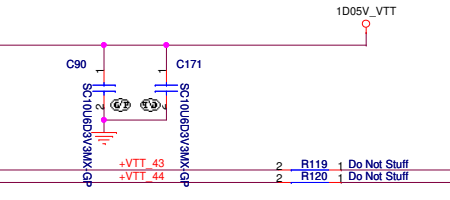
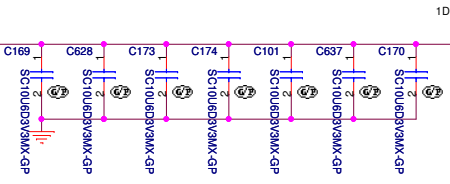
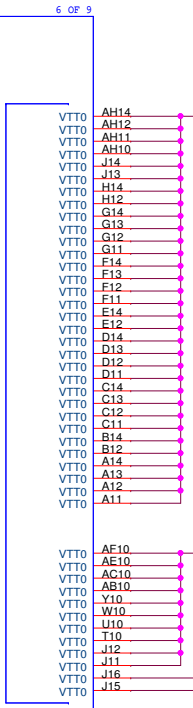
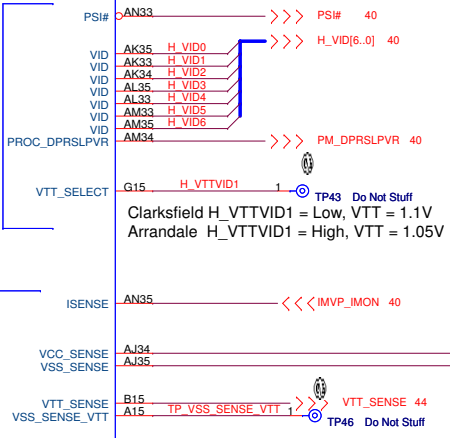
1.1V RAIL POWER

CPU CORE SUPPLY

**POWER**

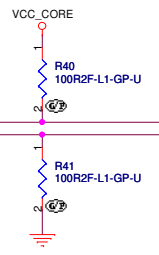
SPIN VIDS

SENSE LINES



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V



CLARKUNF  
62.10053.561  
1ND = 62.10053.561  
2ND = 62.10055.341

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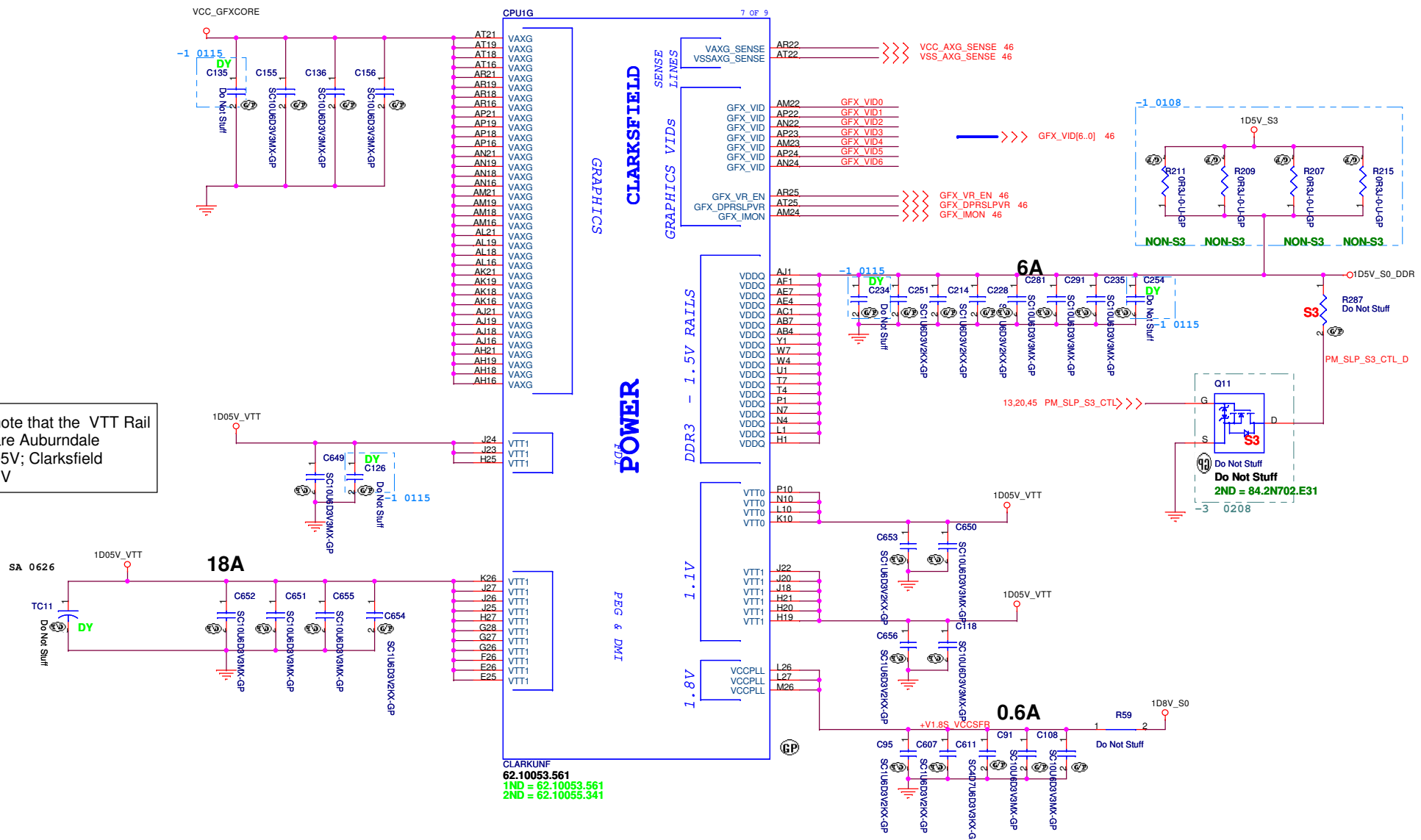
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Title: **CPU (4/7)**

Size: Document Number  
Custort: **JM31-CP**

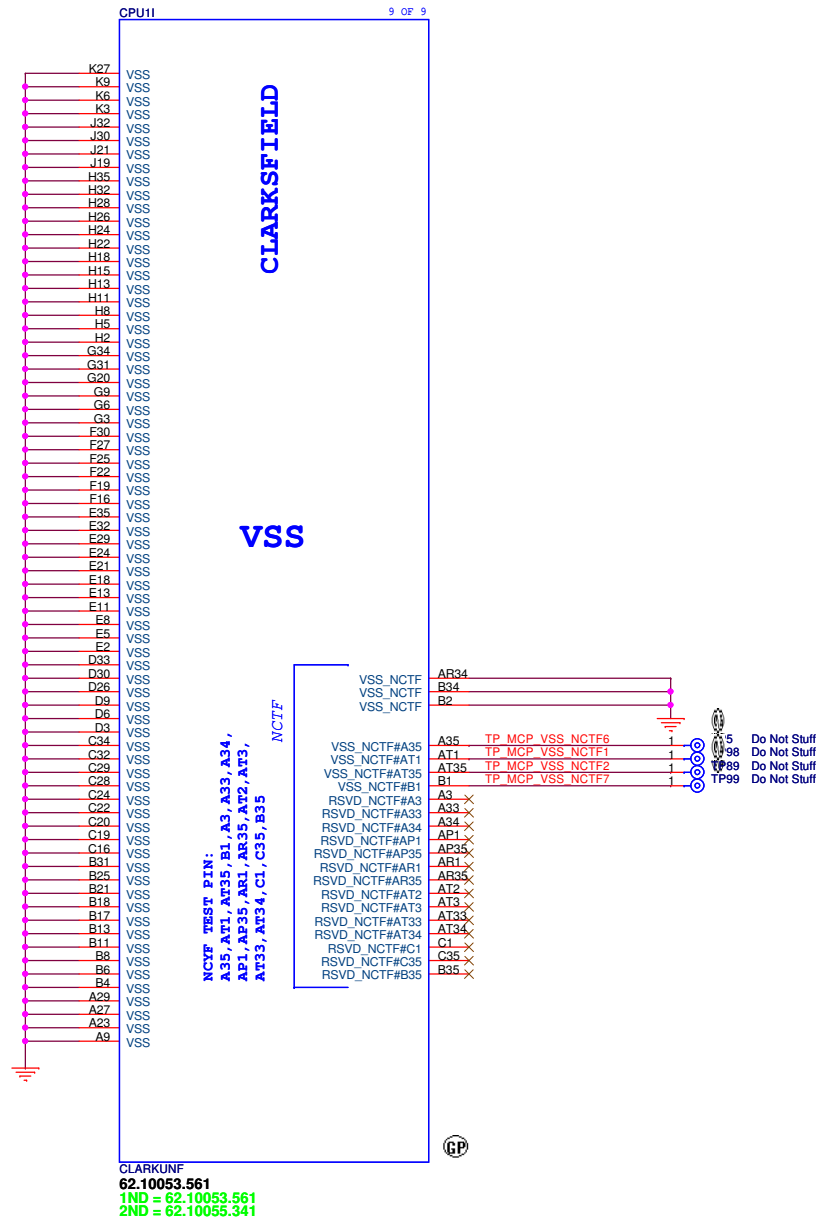
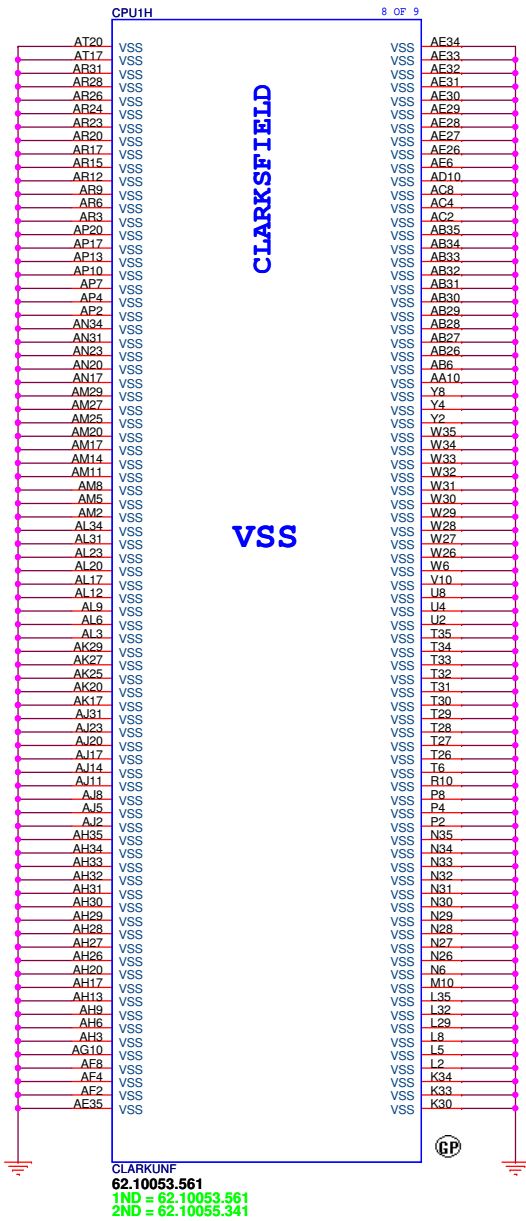
Date: Thursday, February 25, 2010 Sheet 7 of 62

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

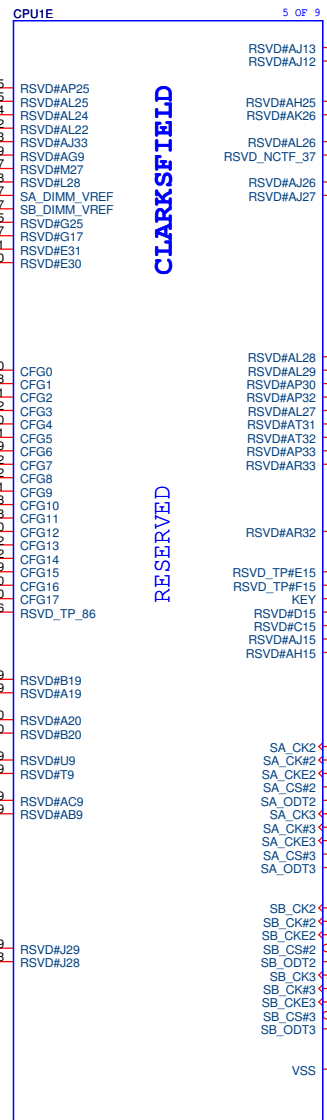
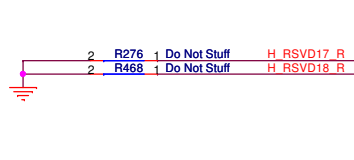
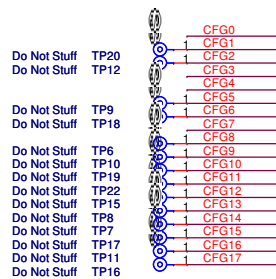
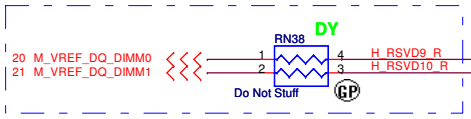


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1ND = 62.10053.561  
2ND = 62.10055.341





### SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor

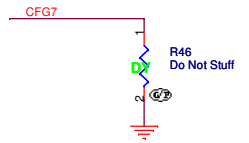
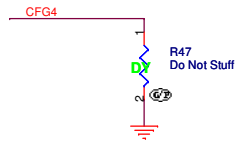
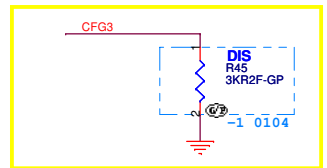
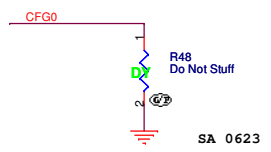


CLARKSFIELD

RESERVED

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

CLARKUNF  
62.10053.561  
1ND = 62.10053.561  
2ND = 62.10055.341



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.  Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

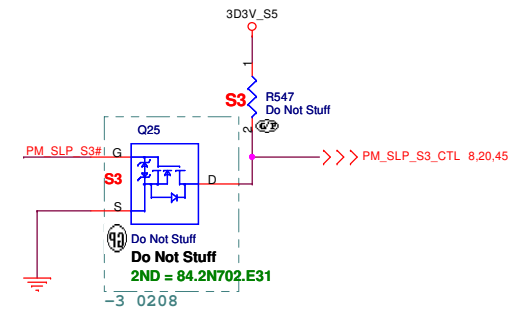
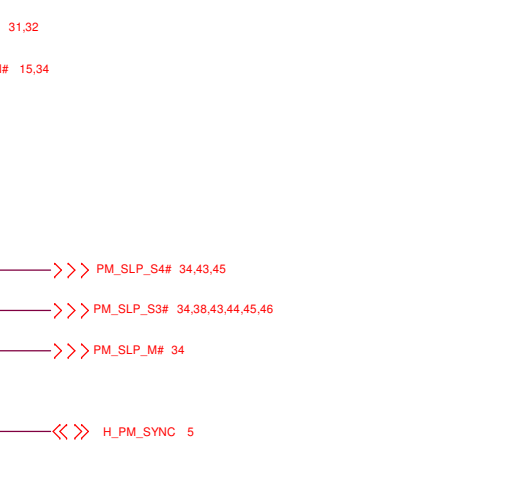
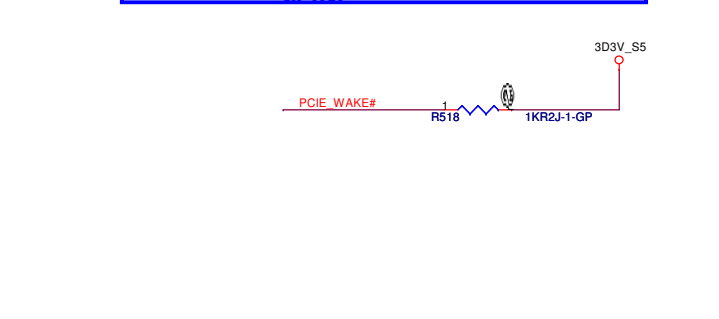
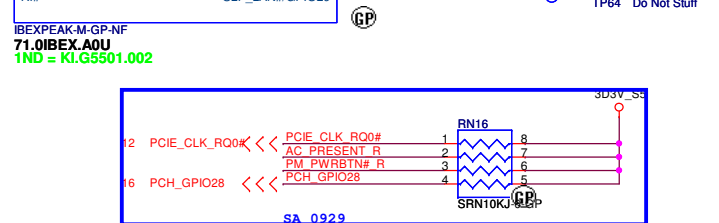
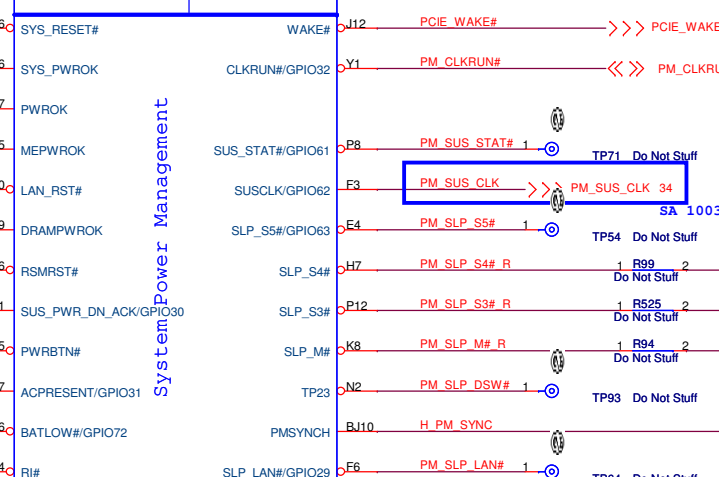
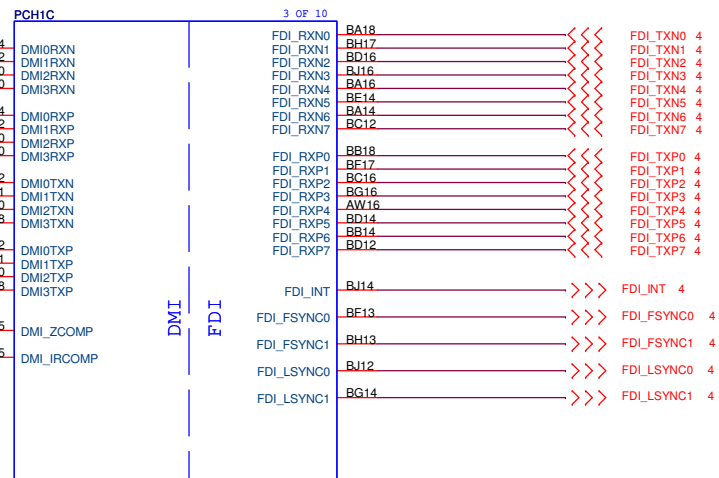
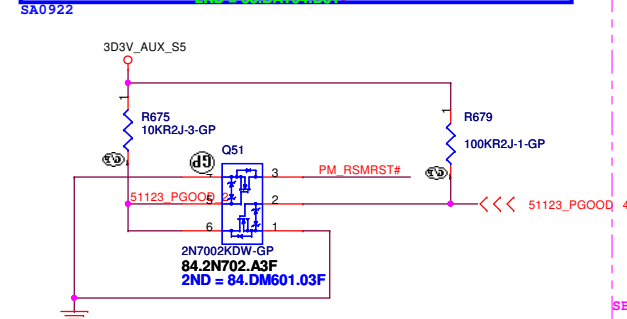
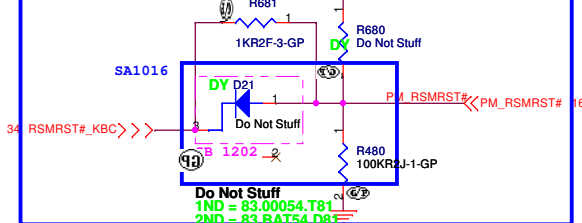
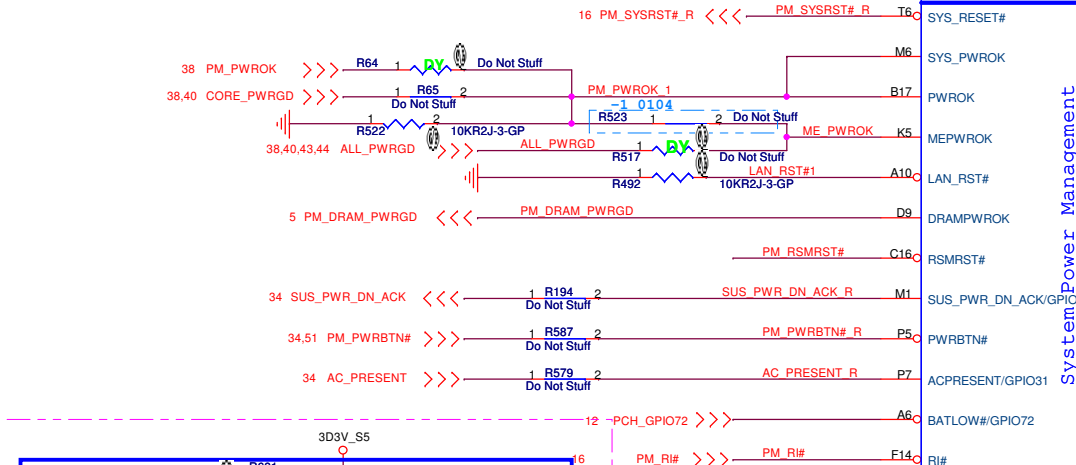
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<b>CPU (7/7)</b>	
Title	Rev
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12 SUS\_PWR\_DN\_ACK\_R >>> \_SUS\_PWR\_DN\_ACK\_R



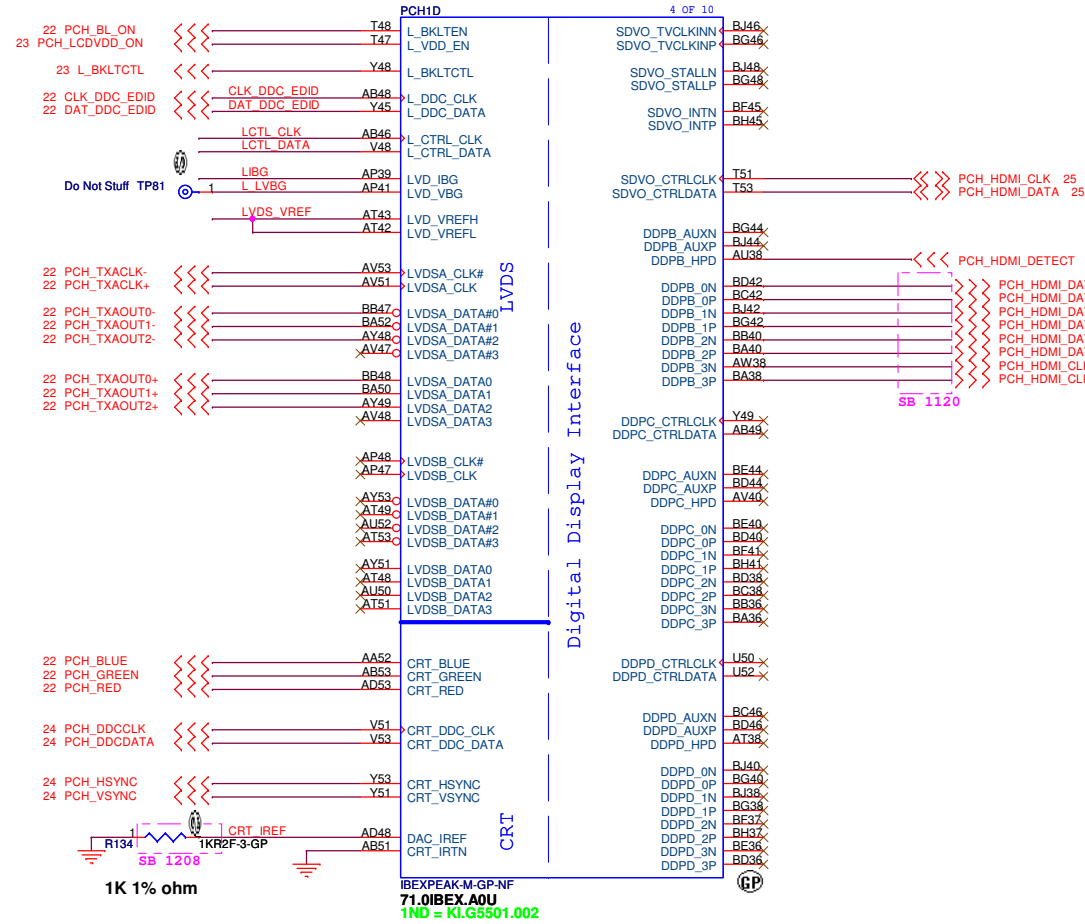
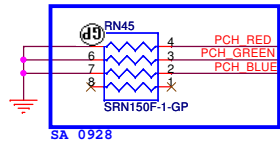
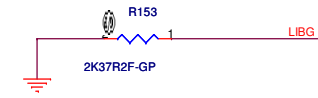
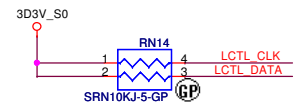
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Title: **PCH (3/9)**

Size A3 Document Number **JM31-CP** Rev -3

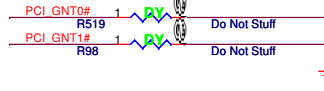
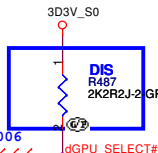
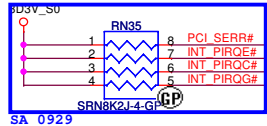
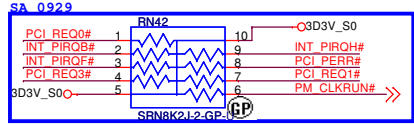
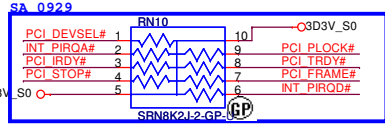
Date: Thursday, February 25, 2010 Sheet 13 of 62



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Title	
<b>PCH (4/9)</b>	
Size	Document Number
A3	<b>JM31-CP</b>
Date: Thursday, February 25, 2010	Rev <b>SB</b>
Sheet 14	of 62

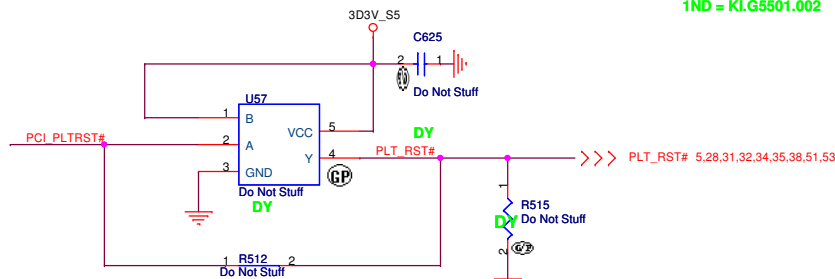
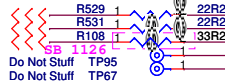
These pins are left as NC,  
because the function is disable.



**BOOT BIOS Strap**

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC (Default)
1	0	Reserved
0	1	PCI
1	1	SPI

- 35 PCLK\_FWH
- 12 CLK\_PCI\_FB
- 34 CLK\_PCI\_KBC



- H40 AD0
- N34 AD1
- C44 AD2
- A38 AD3
- C36 AD4
- J34 AD5
- A40 AD6
- D45 AD7
- E36 AD8
- H48 AD9
- E40 AD10
- C40 AD11
- M48 AD12
- M45 AD13
- F53 AD14
- M40 AD15
- M43 AD16
- J36 AD17
- K48 AD18
- F40 AD19
- C42 AD20
- K46 AD21
- M51 AD22
- J52 AD23
- K51 AD24
- L34 AD25
- F42 AD26
- J40 AD27
- G46 AD28
- F44 AD29
- M47 AD30
- H36 AD31
- J50 C/BE0#
- G42 C/BE1#
- H47 C/BE2#
- G34 C/BE3#
- G38 PIRQA#
- H51 PIRQB#
- B37 PIRQC#
- A44 PIRQD#
- F51 REQ0#
- A46 REQ1#/GPIO50
- E45 REQ2#/GPIO52
- M53 REQ3#/GPIO54
- F48 GNT0#
- K46 GNT1#/GPIO51
- F36 GNT2#/GPIO53
- H53 GNT3#/GPIO55
- B41 PIRQE#/GPIO2
- K53 PIRQF#/GPIO3
- A36 PIRQG#/GPIO4
- A48 PIRQH#/GPIO5
- K6 PCIRST#
- E44 SERR#
- E50 PERR#
- A42 PCI\_IRDY#
- H44 PAR
- F46 PCI\_DEVSEL#
- C46 PCI\_FRAME#
- D49 PLOCK#
- D41 PCI\_STOP#
- C48 PCI\_TRDY#
- M7 ICH\_PME#
- D5 PCI\_PLTRST#
- N52 CLKOUT\_PCIO
- P53 CLKOUT\_PC11
- P46 CLKOUT\_PC12
- P51 CLKOUT\_PC13
- P48 CLKOUT\_PC14

- NV\_CE#0 AY9
- NV\_CE#1 BD1
- NV\_CE#2 AP15
- NV\_CE#3 BDE
- NV\_DQS0 AV9
- NV\_DQS1 BGE
- NV\_DQ0/NV\_IO0 AP7
- NV\_DQ1/NV\_IO1 AP6
- NV\_DQ2/NV\_IO2 AT6
- NV\_DQ3/NV\_IO3 AT9
- NV\_DQ4/NV\_IO4 AV6
- NV\_DQ5/NV\_IO5 BB3
- NV\_DQ6/NV\_IO6 BA4
- NV\_DQ7/NV\_IO7 BA4
- NV\_DQ8/NV\_IO8 BE4
- NV\_DQ9/NV\_IO9 BB6
- NV\_DQ10/NV\_IO10 BB7
- NV\_DQ11/NV\_IO11 BC8
- NV\_DQ12/NV\_IO12 BJ8
- NV\_DQ13/NV\_IO13 BJ6
- NV\_DQ14/NV\_IO14 BG6
- NV\_DQ15/NV\_IO15 BG6
- NV\_ALE BD3
- NV\_GLE AY6
- NV\_RCOMP AU2
- NV\_RB# AV7
- NV\_WR#0\_RE# AY8
- NV\_WR#1\_RE# AY5
- NV\_WE#\_CK0 AV11
- NV\_WE#\_CK1 BE5
- USBPN# H18
- USBP0# J18
- USBP1# A18
- USBP2# C18
- USBP3# M20
- USBP4# F20
- USBP5# L20
- USBP6# F20
- USBP7# L20
- USBP8# G20
- USBP9# A20
- USBP10# C20
- USBP11# M22
- USBP12# N22
- USBP13# B21
- USBP14# D21
- USBP15# H22
- USBP16# J22
- USBP17# F22
- USBP18# A22
- USBP19# C22
- USBP20# G24
- USBP21# H24
- USBP22# L24
- USBP23# M24
- USBP24# A24
- USBP25# C24
- USBRBIAS# B25
- USBRBIAS D25
- OC0#/GPIO59 N16
- OC1#/GPIO40 J16
- OC2#/GPIO41 C16
- OC3#/GPIO42 E16
- OC4#/GPIO43 E14
- OC5#/GPIO3 G16
- OC6#/GPIO10 E12
- OC7#/GPIO14 T15
- USB\_OC#3 J16
- USB\_OC#0 28
- USB\_OC#1 28
- USB\_OC#2 28
- USB\_OC#3 28
- USB\_OC#0 28
- USB\_OC#1 28
- USB\_OC#2 28
- USB\_OC#3 28

IBEXPEAK-M-GP-NF  
71.0IBEX.A0U  
1ND = KLG5501.002

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

These pins are left as NC,  
because the function is disable.

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:  
Disabled when Low.  
Enable when High.

**USB**

Pair	Device
0	EXT USB1
1	USB1 (on board)
2	EXT USB2
3	MINICARD1
4	WECAM
5	SIM Card
6	NC
7	NC
8	NC
9	NC
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

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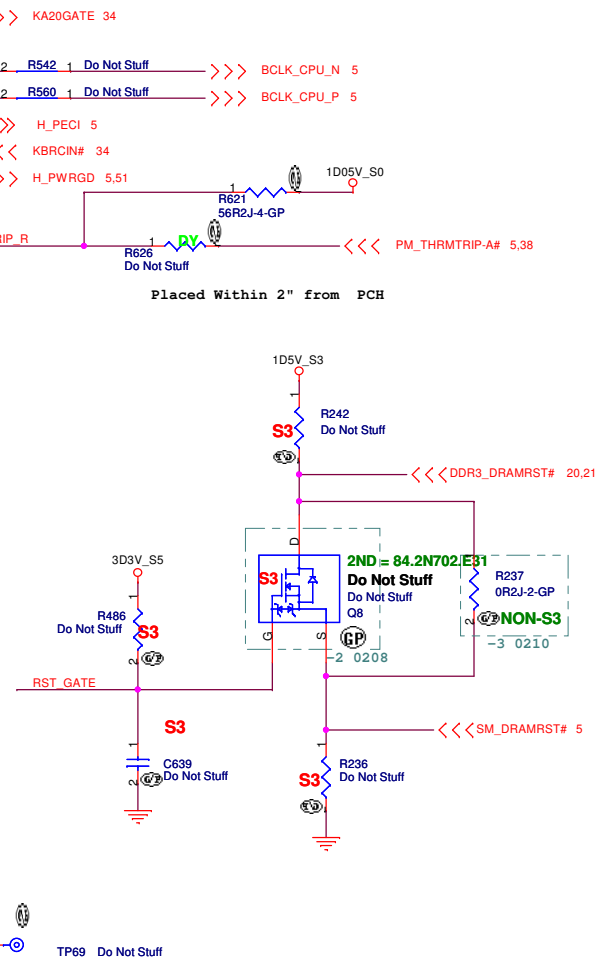
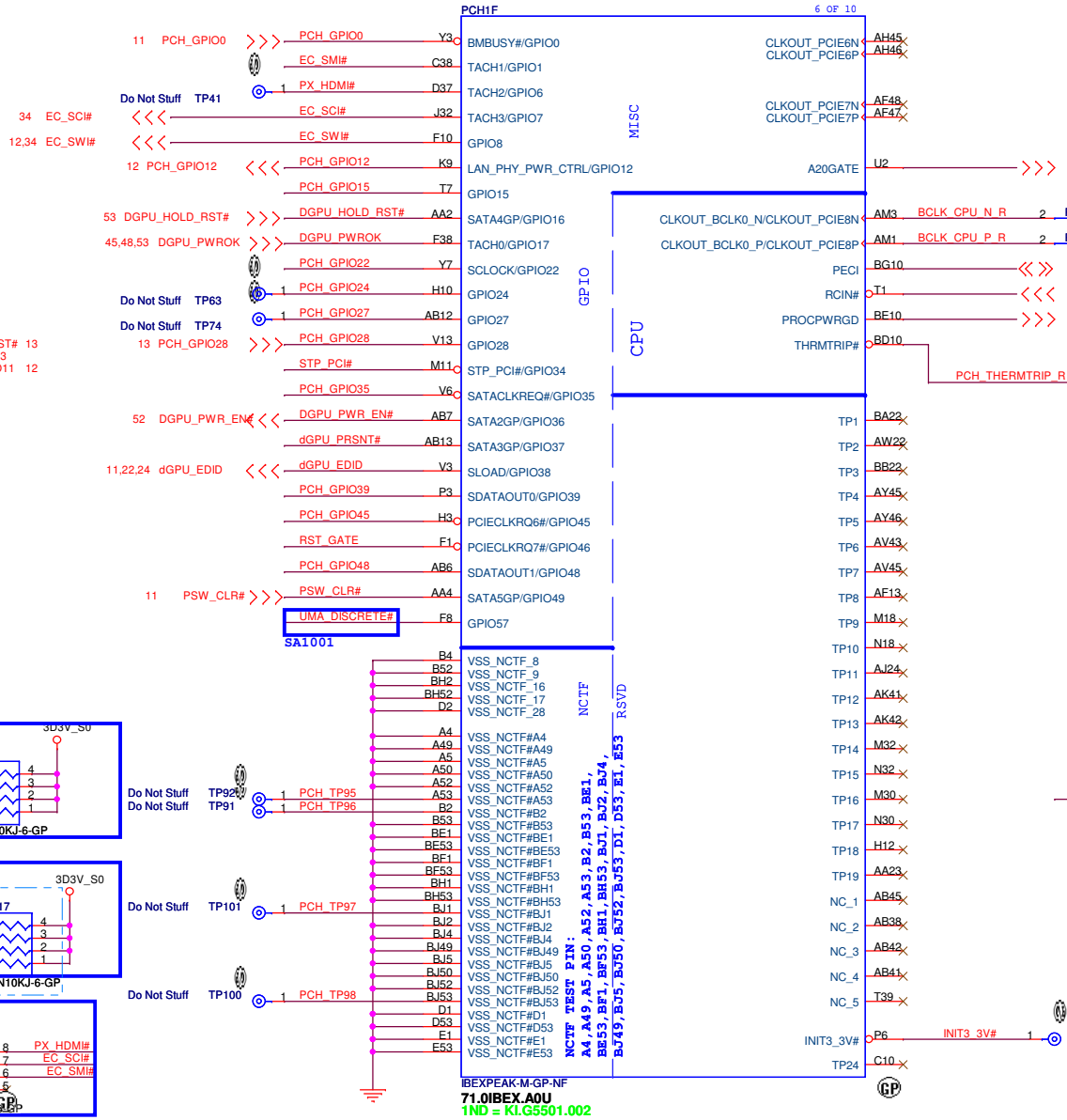
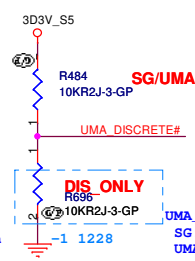
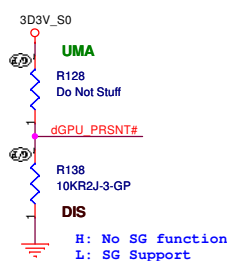
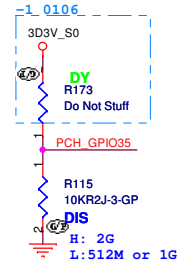
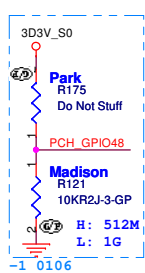
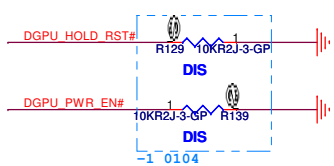
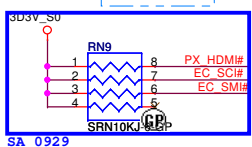
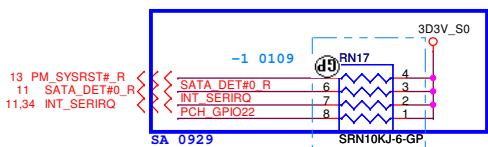
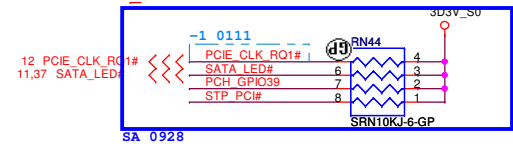
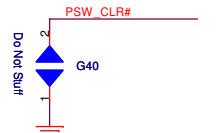
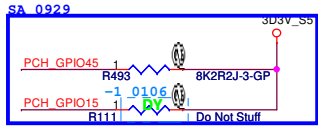
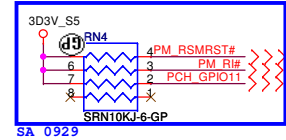
Title: **PCH (5/9)**

Size A3	Document Number <b>JM31-CP</b>	Rev <b>SB</b>
Date: Thursday, February 25, 2010	Sheet 15 of 62	

GPIO8 has a weak[20K] internal pull down.  
No need to have external pull down/up.  
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.  
No need to have external pull up/down.  
GPIO 15 pin is set to low at reset.  
Low : ME Crypto TLS with no confidentiality  
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.



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Title: **PCH (6/9)**

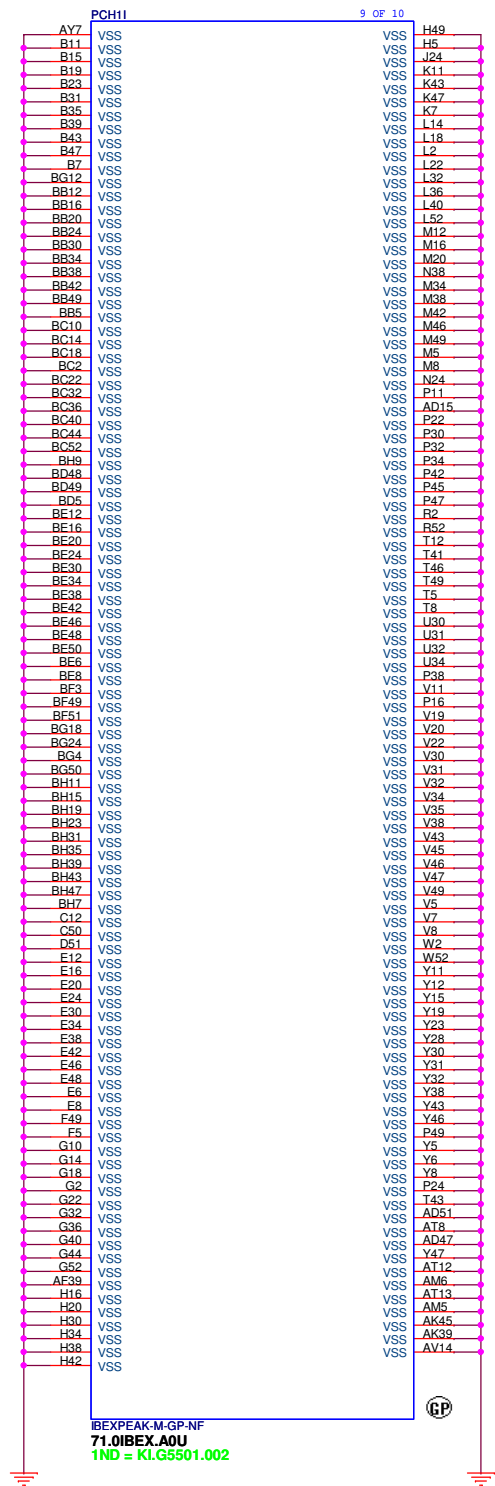
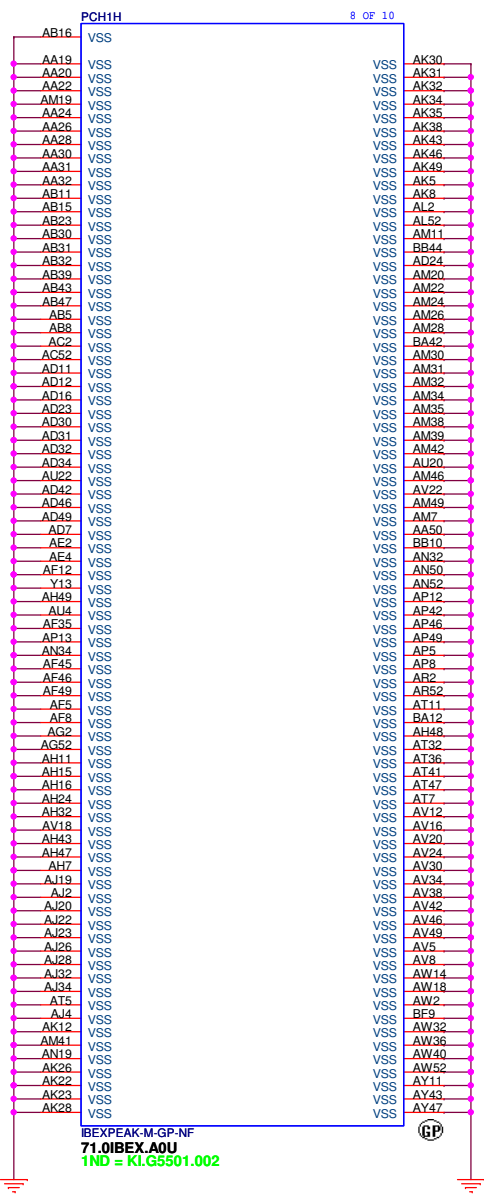
Size A3 Document Number: **JM31-CP** Rev: **-1**

Date: Thursday, February 25, 2010 Sheet 16 of 62









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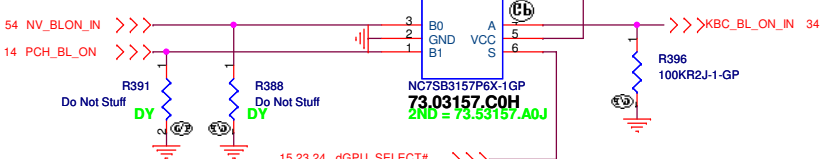
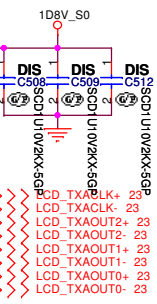
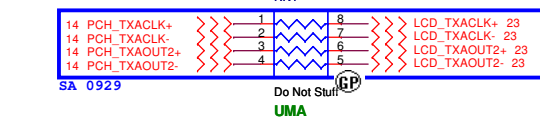
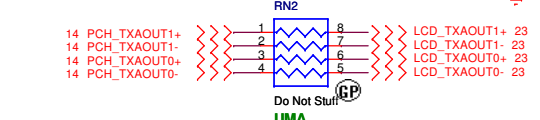
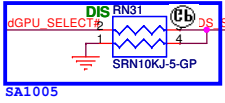
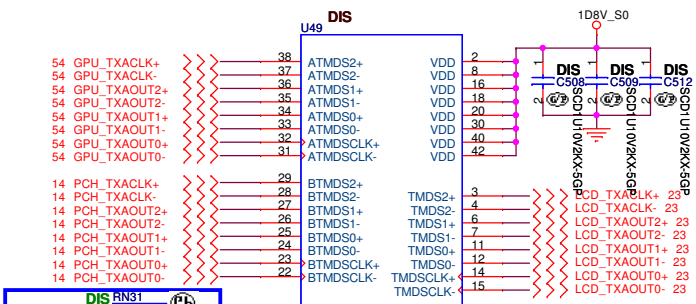
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH ( 9/9 )**

Size A3	Document Number <b>JM31-CP</b>	Rev <b>SA</b>
Date: Thursday, February 25, 2010	Sheet 19	of 62







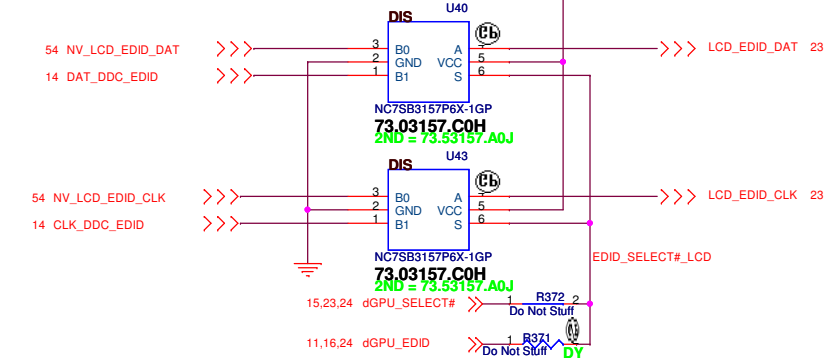
### FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

### Function Table

Input (S)	Function
L	B <sub>0</sub> Connected to A
H	B <sub>1</sub> Connected to A

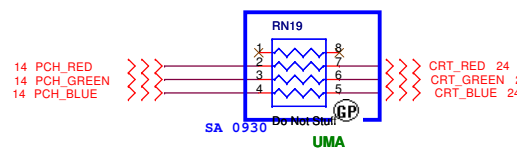
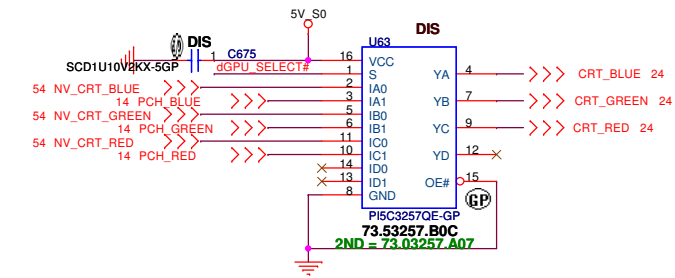
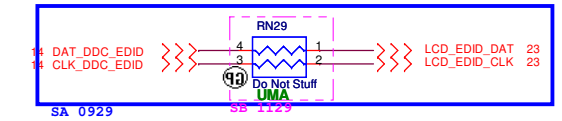
H = HIGH Logic Level      L = LOW Logic Level



### Function Table

Input (S)	Function
L	B <sub>0</sub> Connected to A
H	B <sub>1</sub> Connected to A

H = HIGH Logic Level      L = LOW Logic Level



$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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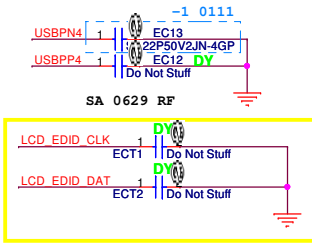
**緯創資通 Wistron Corporation**  
21F, 86, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX SWITCH**

Size A3 Document Number: **JM31-CP** Rev: **SB**

Date: Thursday, February 25, 2010 Sheet 22 of 62

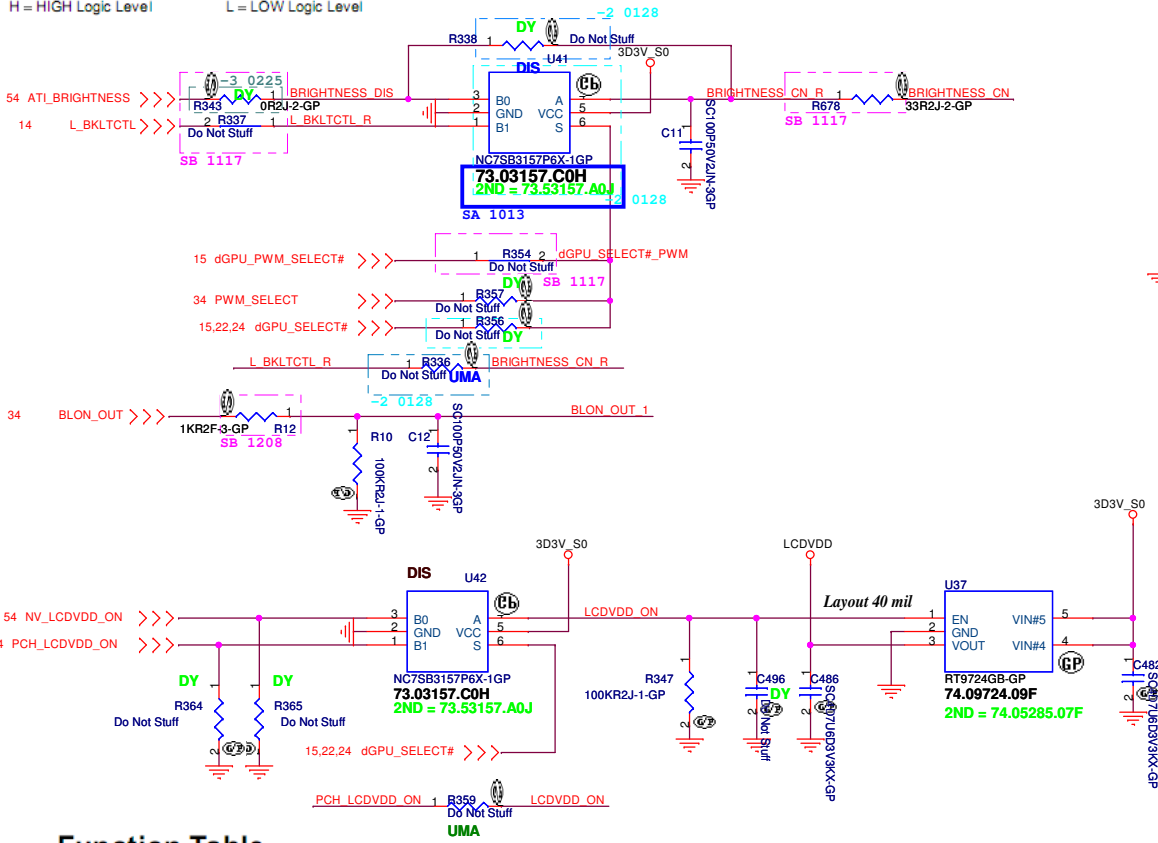
# LCD/INVERTER/CCD CONN



## Function Table

Input (S)	Function
L	B <sub>0</sub> Connected to A
H	B <sub>1</sub> Connected to A

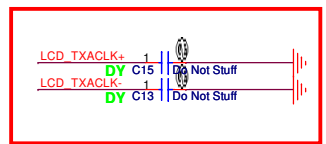
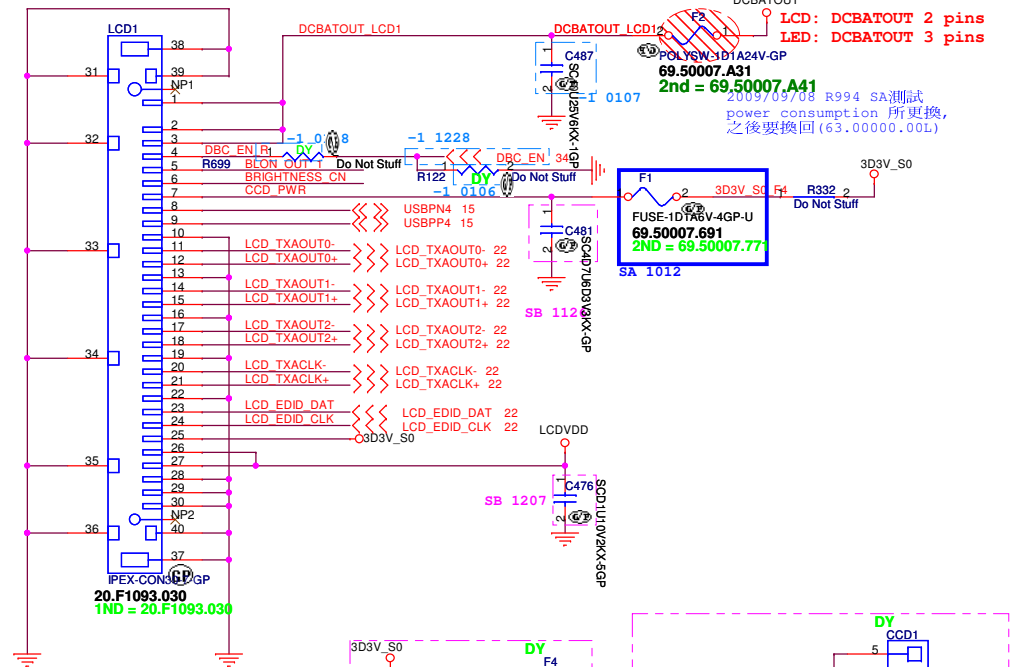
H = HIGH Logic Level L = LOW Logic Level



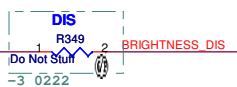
## Function Table

Input (S)	Function
L	B <sub>0</sub> Connected to A
H	B <sub>1</sub> Connected to A

H = HIGH Logic Level L = LOW Logic Level



modify by RF



Reserve direct connector to KBC

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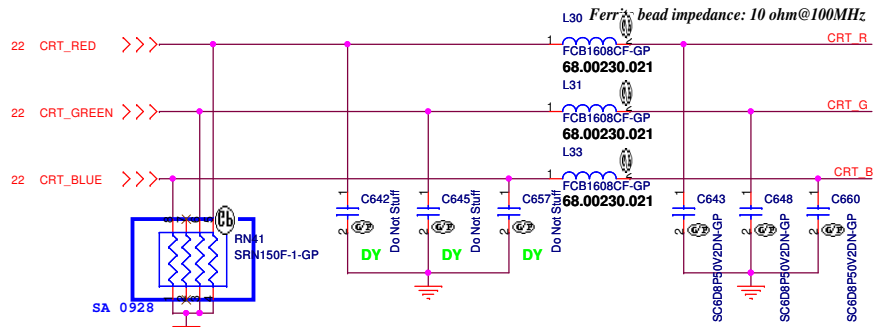
**緯創資通 Wistron Corporation**  
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File **LCD CONN**

Size A3	Document Number <b>JM31-CP</b>	Rev -1
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Date: Thursday, February 25, 2010 Sheet 23 of 62

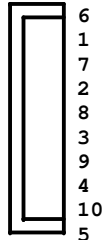
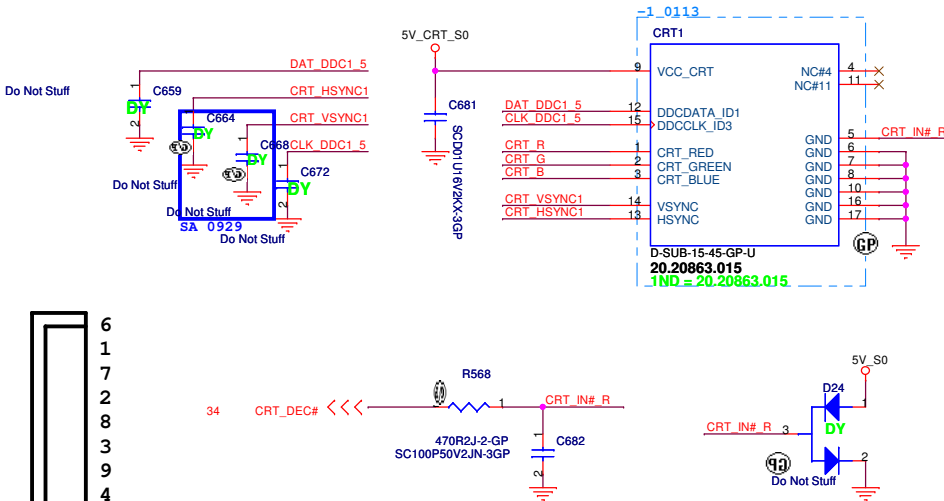
Layout Notes:  
Place these resistors  
close to the CRT-out  
connector



**Layout Note:**

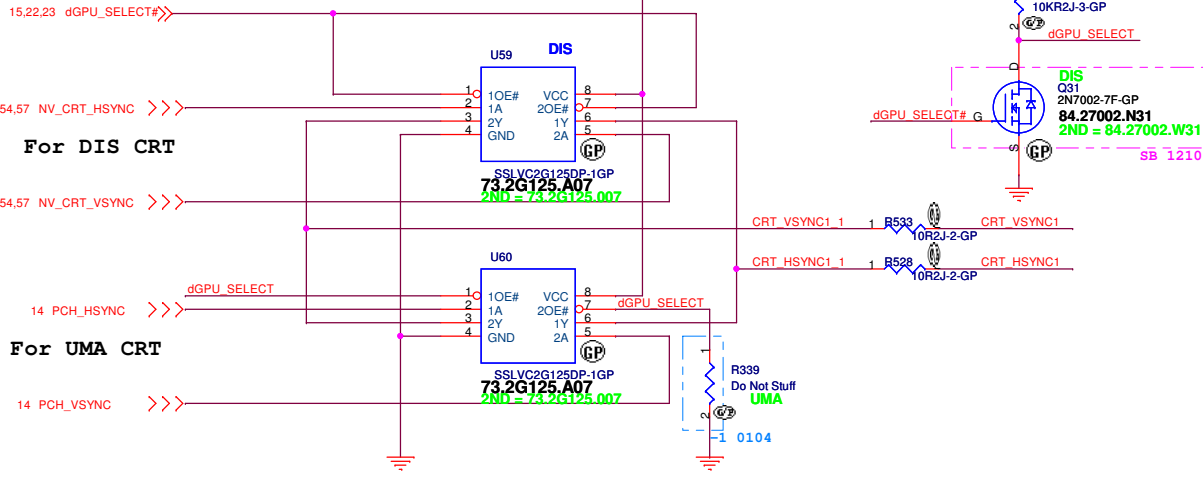
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## CRT I/F & CONNECTOR

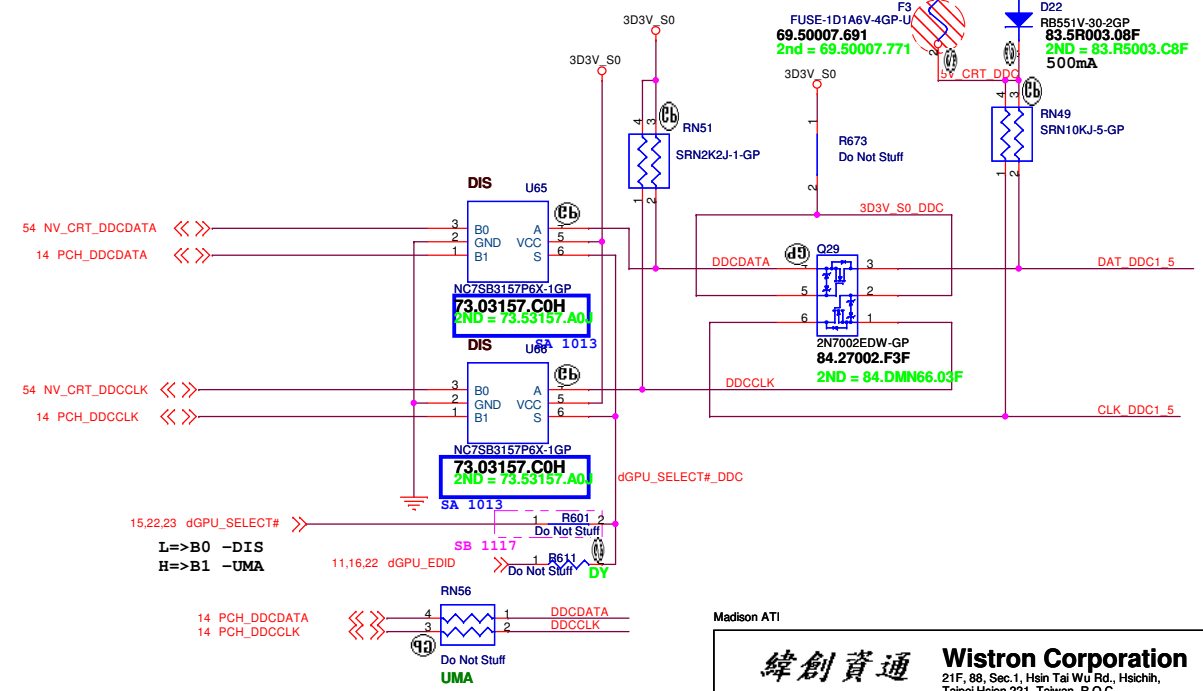


L=>B0 -DIS  
H=>B1 -UMA

## Hsync & Vsync level shift



## DDC\_CLK & DATA level shift



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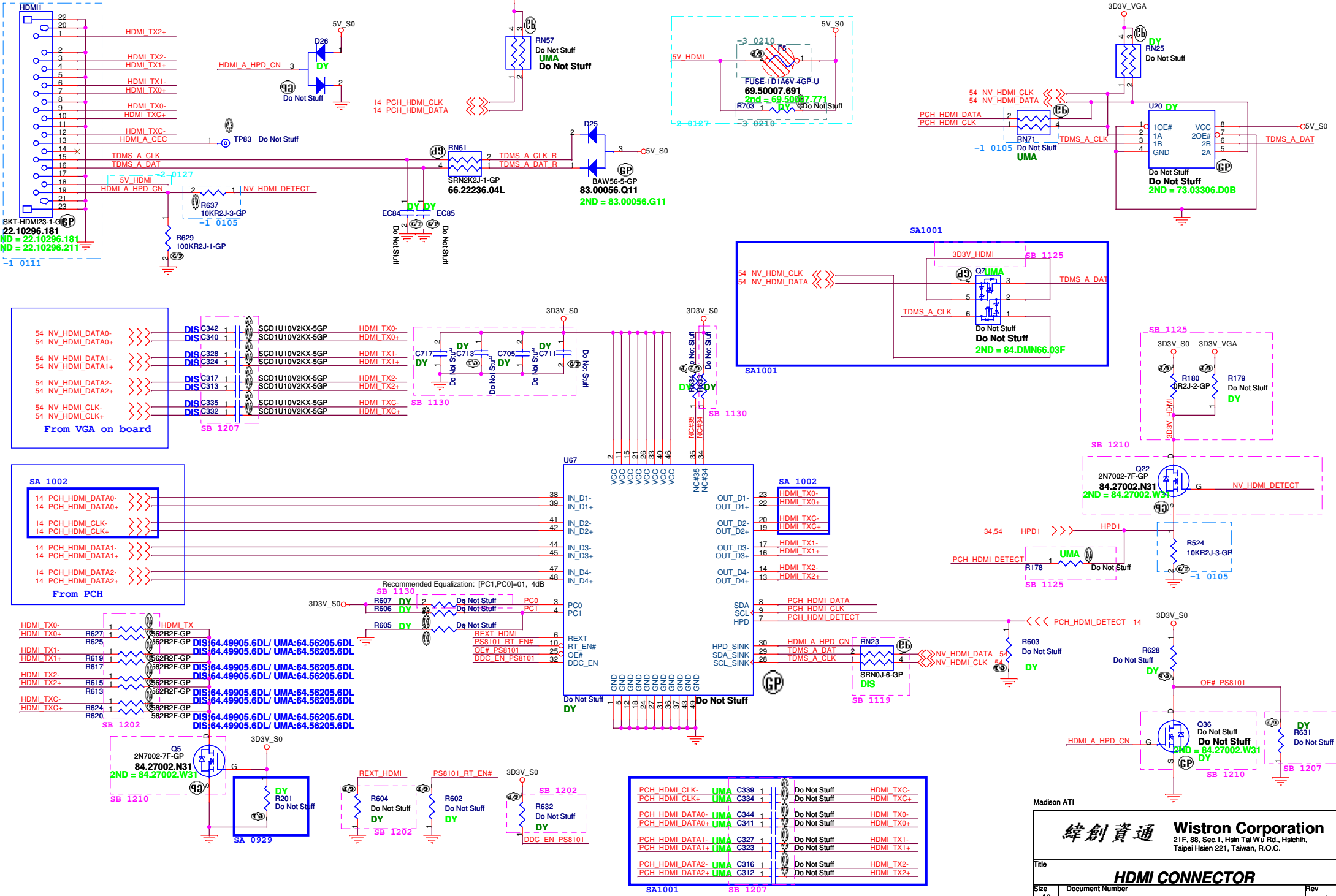
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

Size A3 Document Number: **JM31-CP** Rev: **SB**

Date: Thursday, February 25, 2010 Sheet 24 of 62





SKT-HDMI23-1-GP  
22.10296.181  
1ND = 22.10296.181  
2ND = 22.10296.211  
-1 0111

From VGA on board

54 NV_HDMI_DATA0-	DIS C342	1	SCD1U10V2KX-5GP	HDMI TX0-
54 NV_HDMI_DATA0+	DIS C340	1	SCD1U10V2KX-5GP	HDMI TX0+
54 NV_HDMI_DATA1-	DIS C328	1	SCD1U10V2KX-5GP	HDMI TX1-
54 NV_HDMI_DATA1+	DIS C324	1	SCD1U10V2KX-5GP	HDMI TX1+
54 NV_HDMI_DATA2-	DIS C317	1	SCD1U10V2KX-5GP	HDMI TX2-
54 NV_HDMI_DATA2+	DIS C313	1	SCD1U10V2KX-5GP	HDMI TX2+
54 NV_HDMI_CLK-	DIS C335	1	SCD1U10V2KX-5GP	HDMI TXC-
54 NV_HDMI_CLK+	DIS C332	1	SCD1U10V2KX-5GP	HDMI TXC+

From PCH

14 PCH_HDMI_DATA0-	DIS C342	1	SCD1U10V2KX-5GP	HDMI TX0-
14 PCH_HDMI_DATA0+	DIS C340	1	SCD1U10V2KX-5GP	HDMI TX0+
14 PCH_HDMI_CLK-	DIS C328	1	SCD1U10V2KX-5GP	HDMI TX1-
14 PCH_HDMI_CLK+	DIS C324	1	SCD1U10V2KX-5GP	HDMI TX1+
14 PCH_HDMI_DATA1-	DIS C317	1	SCD1U10V2KX-5GP	HDMI TX2-
14 PCH_HDMI_DATA1+	DIS C313	1	SCD1U10V2KX-5GP	HDMI TX2+
14 PCH_HDMI_DATA2-	DIS C335	1	SCD1U10V2KX-5GP	HDMI TXC-
14 PCH_HDMI_DATA2+	DIS C332	1	SCD1U10V2KX-5GP	HDMI TXC+

PCH HDMI CLK-	LIMA C339	1	Do Not Stuff	HDMI TXC-
PCH HDMI CLK+	LIMA C334	1	Do Not Stuff	HDMI TXC+
PCH HDMI_DATA0-	LIMA C344	1	Do Not Stuff	HDMI TX0-
PCH HDMI_DATA0+	LIMA C341	1	Do Not Stuff	HDMI TX0+
PCH HDMI_DATA1-	LIMA C327	1	Do Not Stuff	HDMI TX1-
PCH HDMI_DATA1+	LIMA C323	1	Do Not Stuff	HDMI TX1+
PCH HDMI_DATA2-	LIMA C316	1	Do Not Stuff	HDMI TX2-
PCH HDMI_DATA2+	LIMA C312	1	Do Not Stuff	HDMI TX2+

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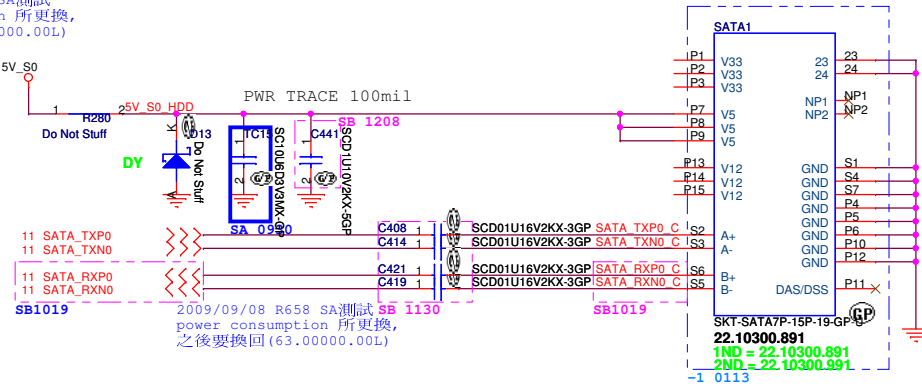
Title: **HDMI CONNECTOR**

Size A3 Document Number **JM31-CP** Rev -1

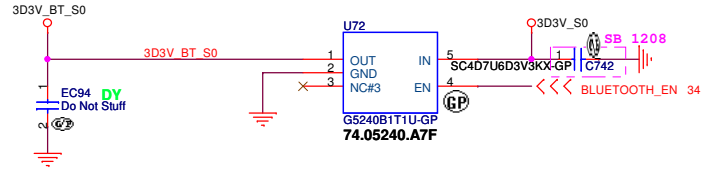
Date: Thursday, February 25, 2010 Sheet 25 of 62

# SATA Connector

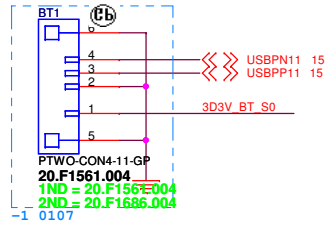
2009/09/08 R658 SA測試  
power consumption 所更換,  
之後要換回(63.00000.00L)



# BLUETOOTH MODULE



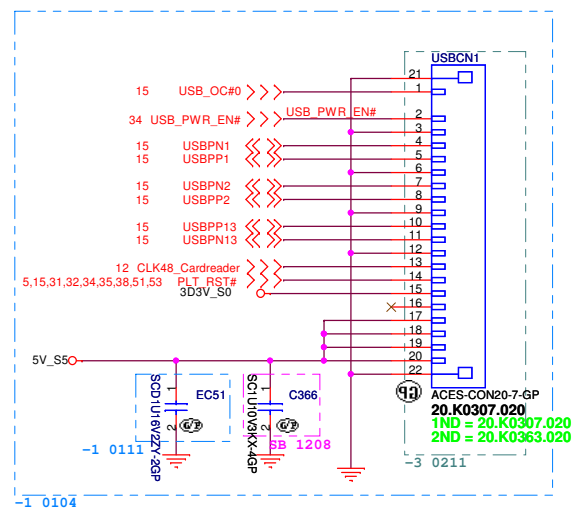
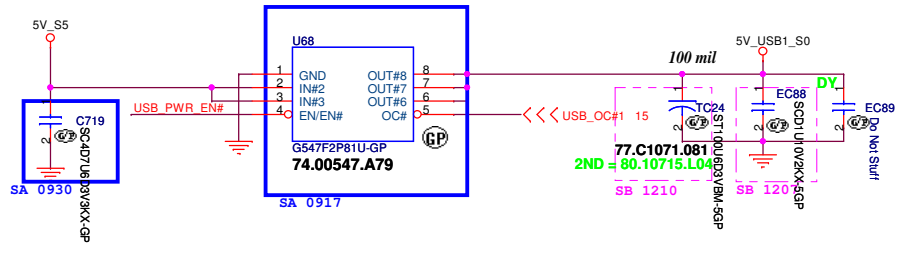
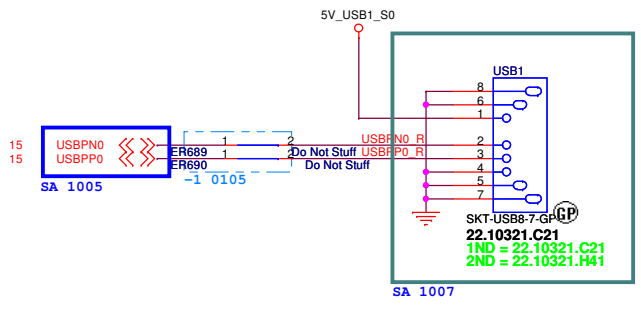
EC20 put near  
BLUE1 / all  
USB put one  
choke near  
connector by  
EMI request



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**緯創資通** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>BLUETOOTH</b>		
Size A3	Document Number <b>JM31-CP</b>	Rev -1
Date: Thursday, February 25, 2010	Sheet 27	of 62

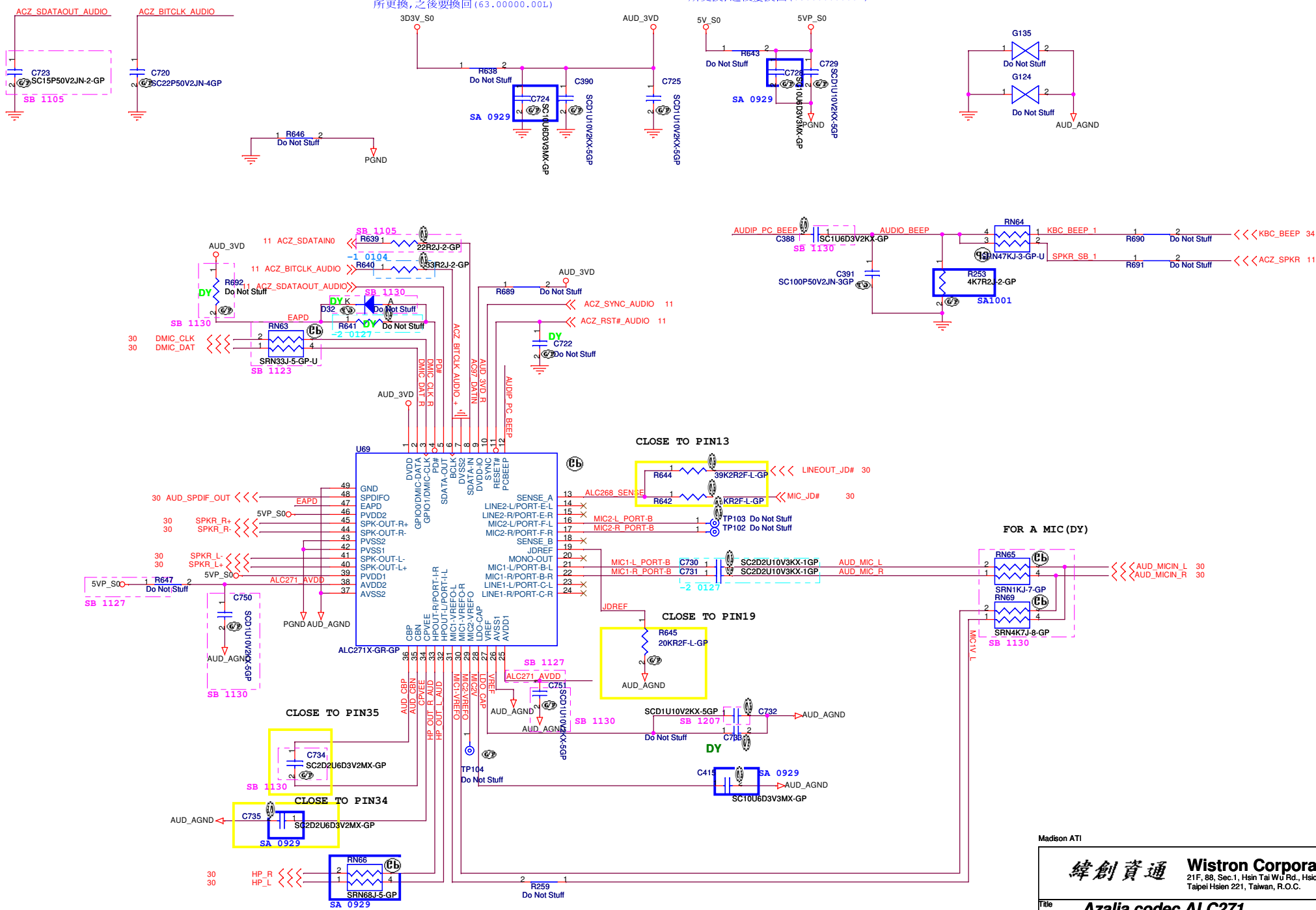


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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB CONN			
Size	Document Number	Rev	
A3	JM31-CP	-3	
Date: Thursday, February 25, 2010		Sheet	28 of 62

2009/09/14 R296 SA測試 power consumption  
所更換,之後要換回(63.00000.00L)

2009/09/16 R296 SA測試 power consumption  
所更換,之後要換回(63.00000.00L)



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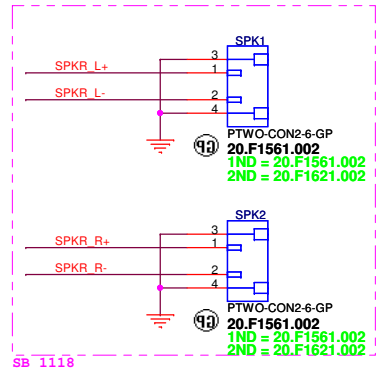
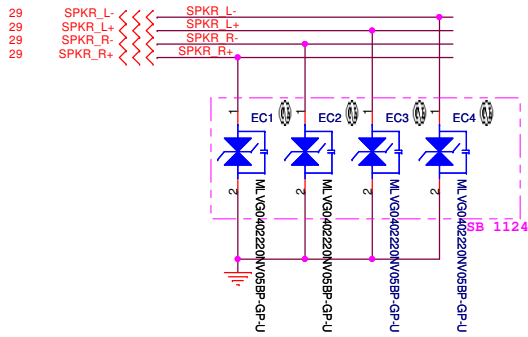
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Asalia codec ALC271**

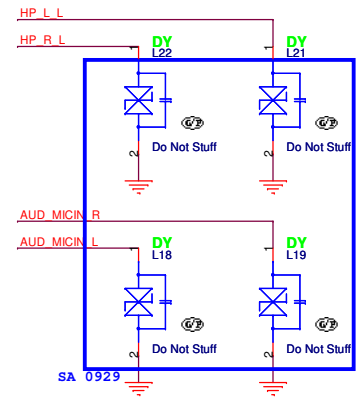
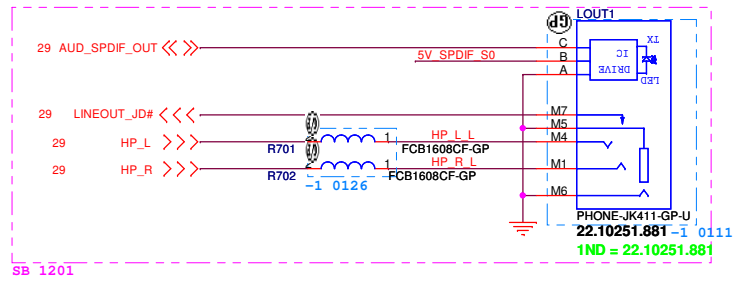
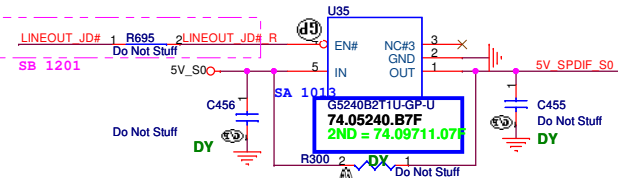
Size	Document Number	Rev
A3	<b>JM31-CP</b>	SB

Date: Thursday, February 25, 2010 Sheet 29 of 62

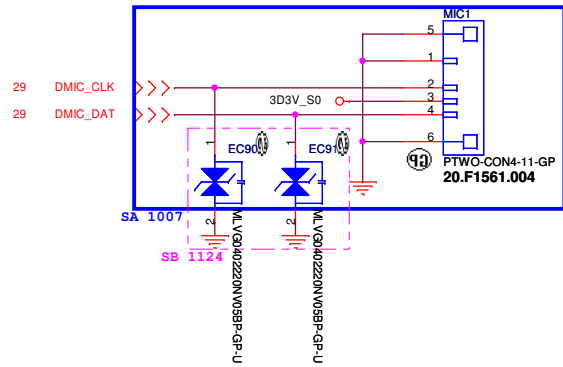
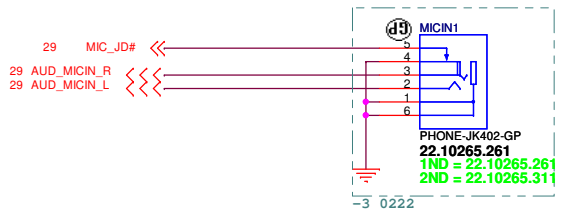
# Internal Speaker

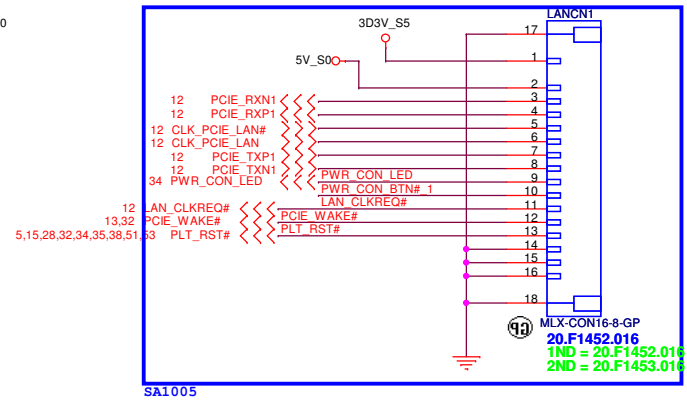
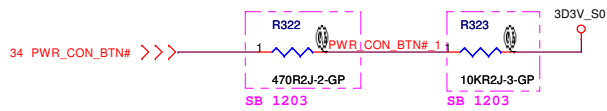


# LINE OUT



# MIC IN





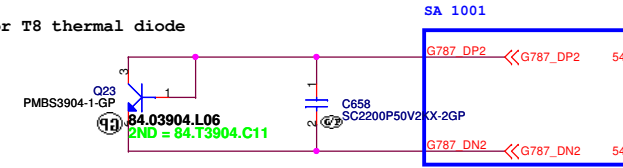
Madison AT1

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<b>LAN CONN</b>		
Size A3	Document Number <b>JM31-CP</b>	Rev <b>SB</b>
Date: Thursday, February 25, 2010		Sheet 31 of 62



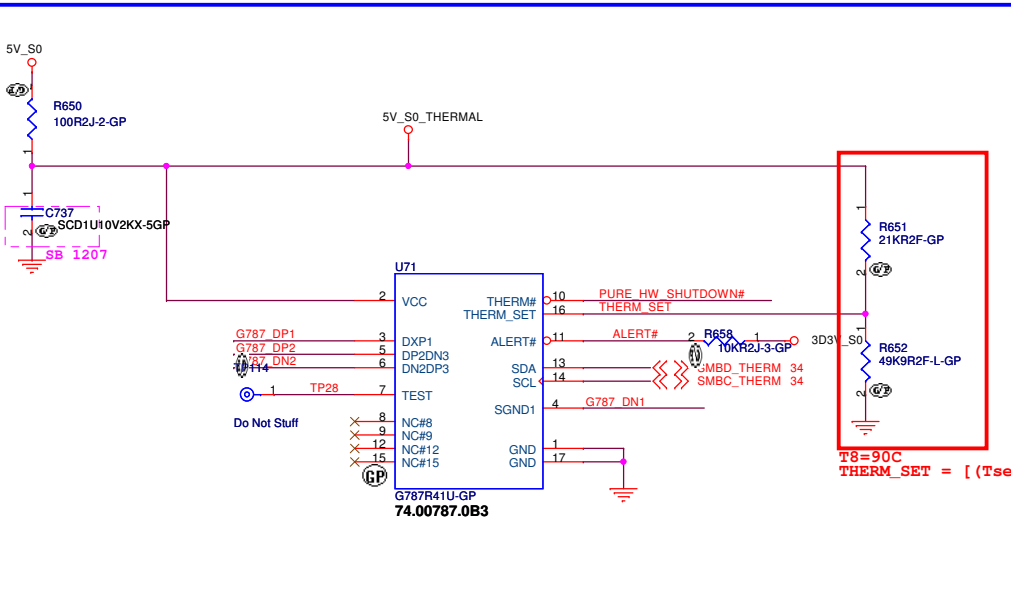
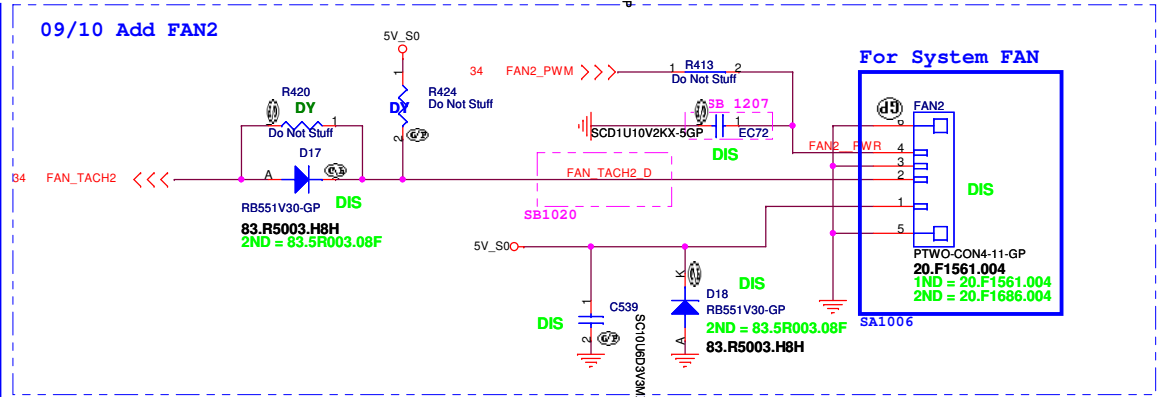
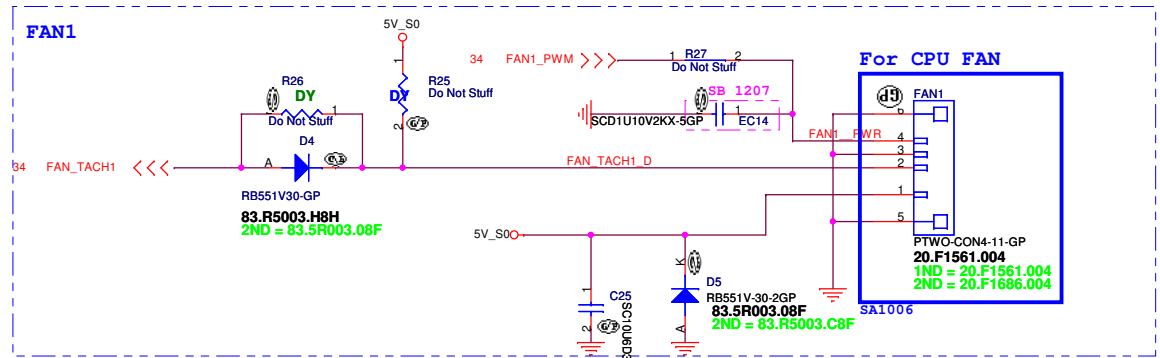
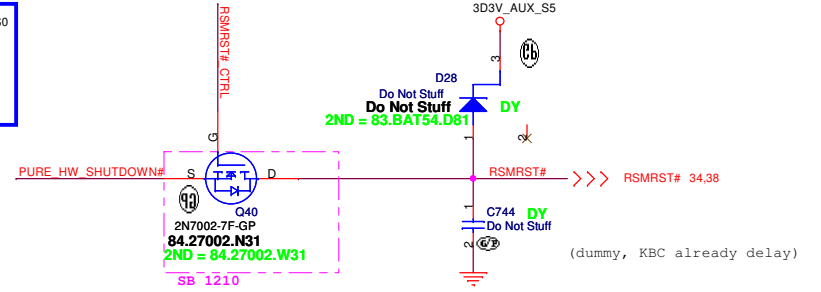
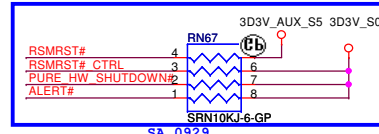
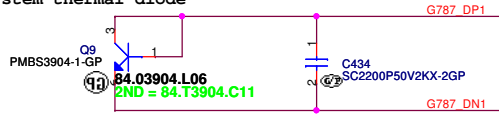


for T8 thermal diode



C82 & C561 CLOSE TO G787

for system thermal diode

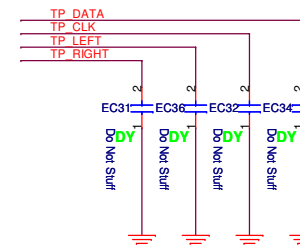
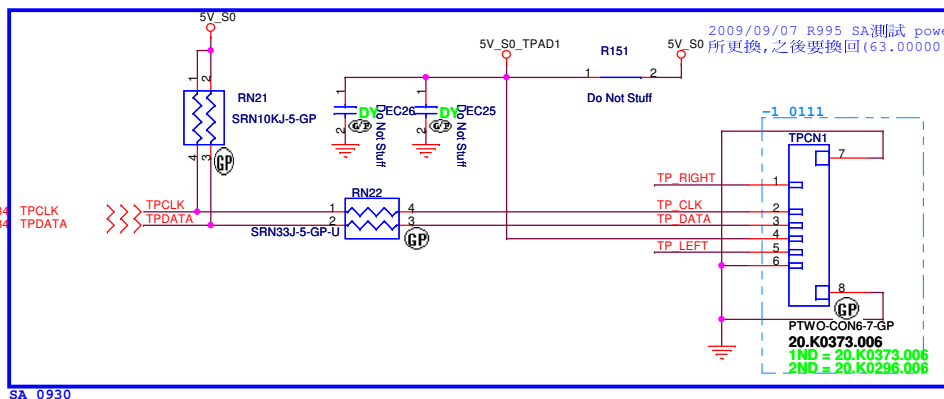
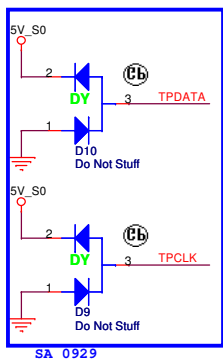


T8=90C  
 $THERM\_SET = [(T_{sec}-72) \times 0.02 + 0.34] \times VCC$

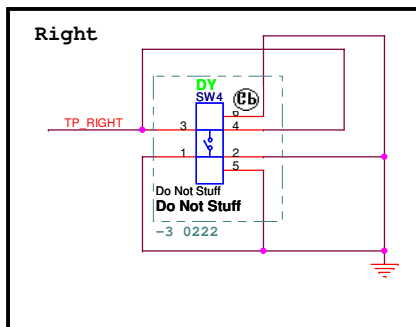
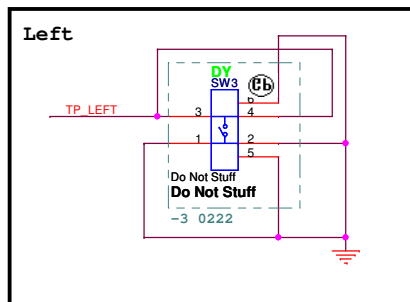
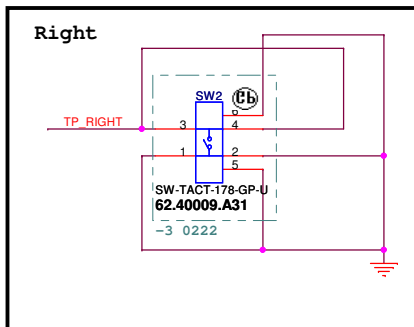
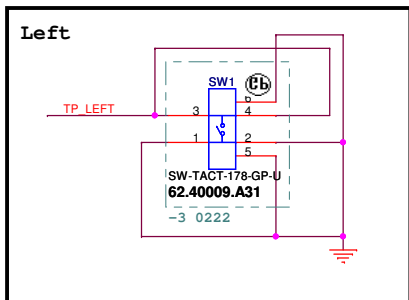




# TOUCH PAD

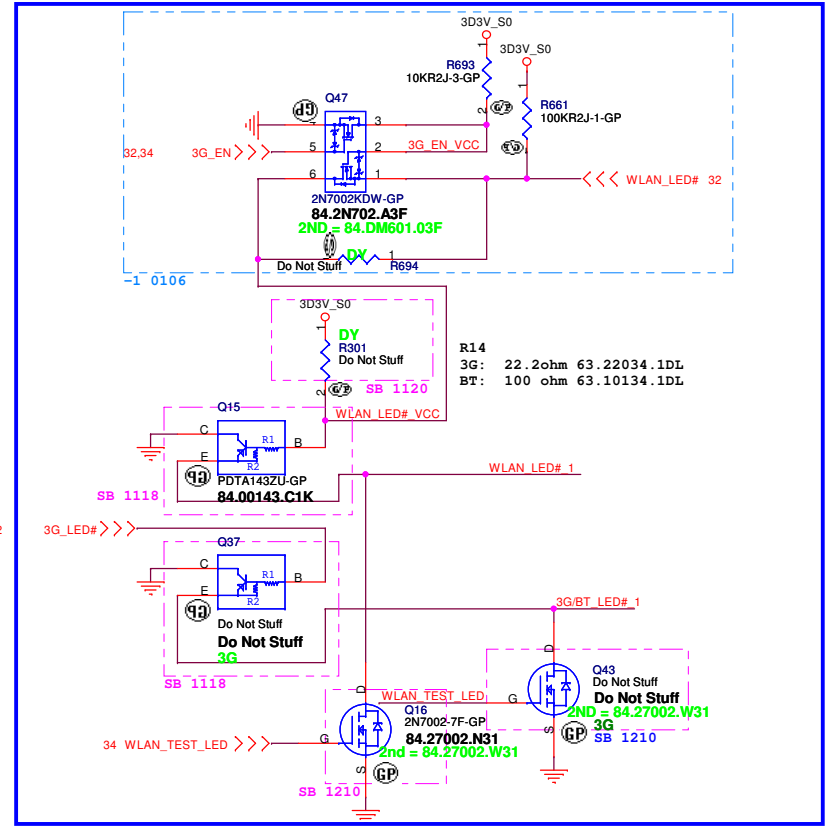
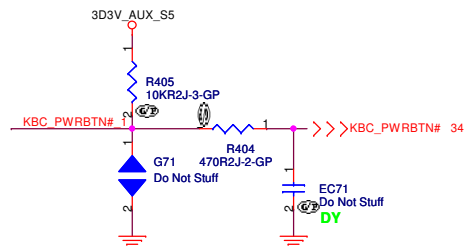
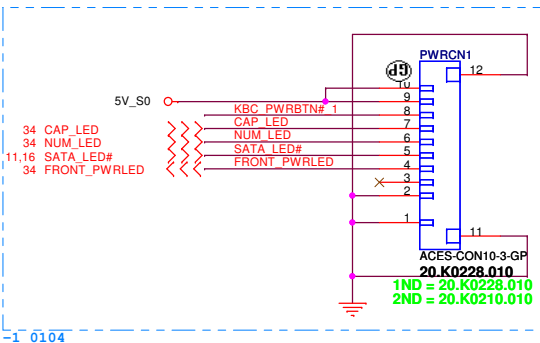
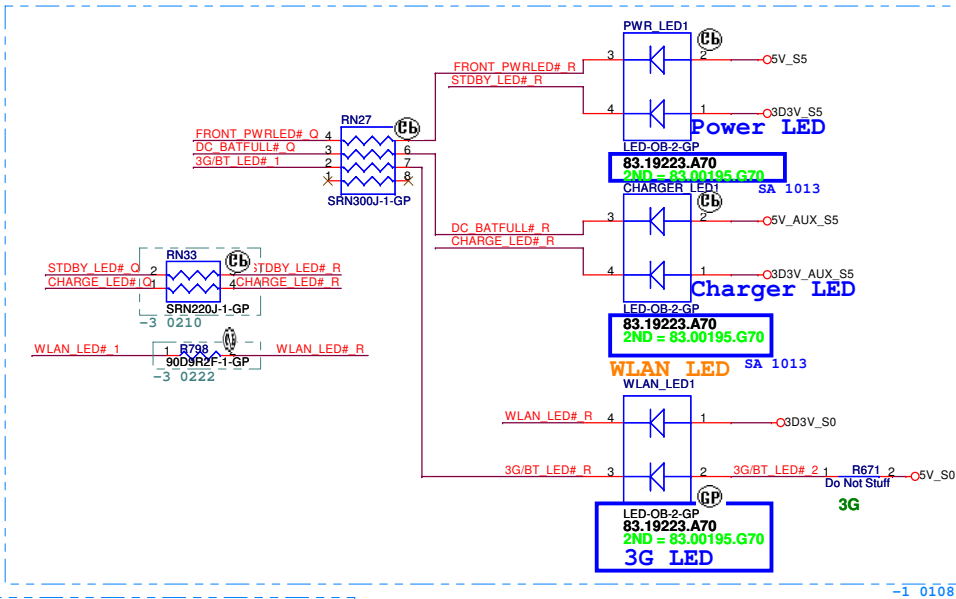
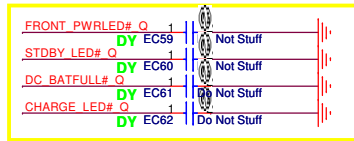
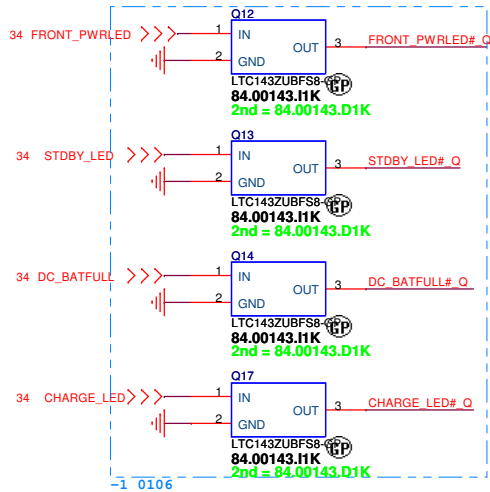


1 12  
T/P



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Title <b>Touch PAD</b>	
Size A3	Document Number <b>JM31-CP</b>
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Rev <b>-1</b>	



SA1006

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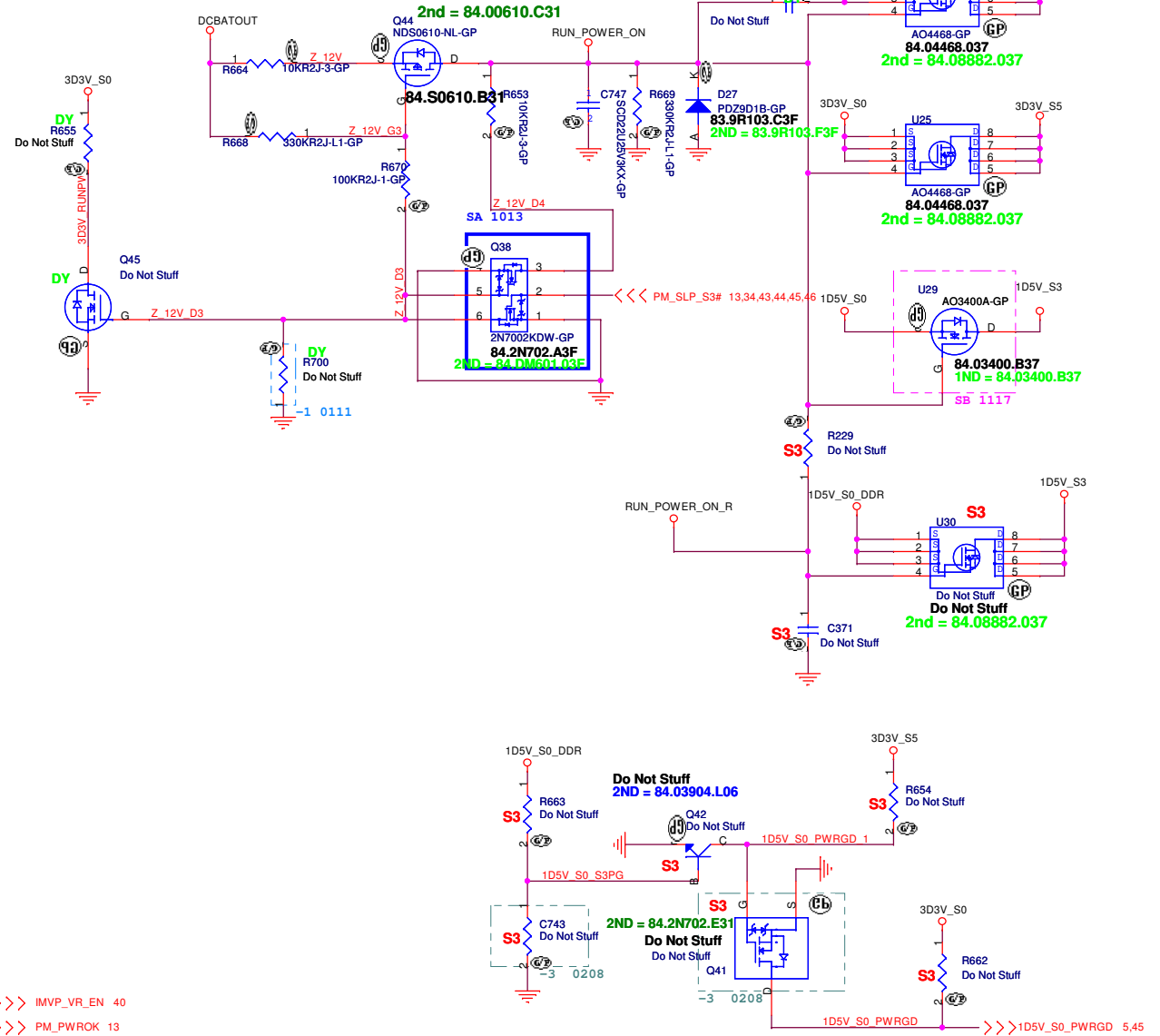
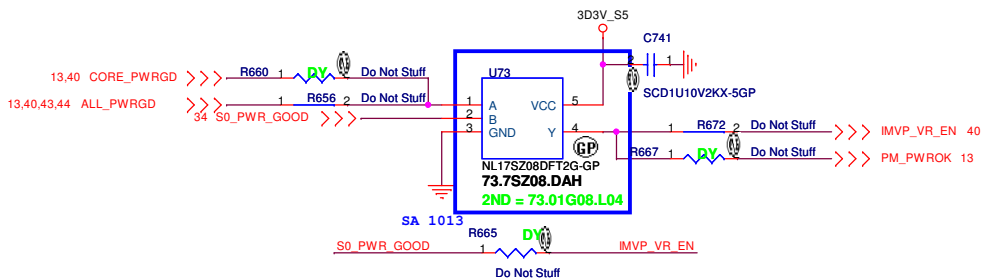
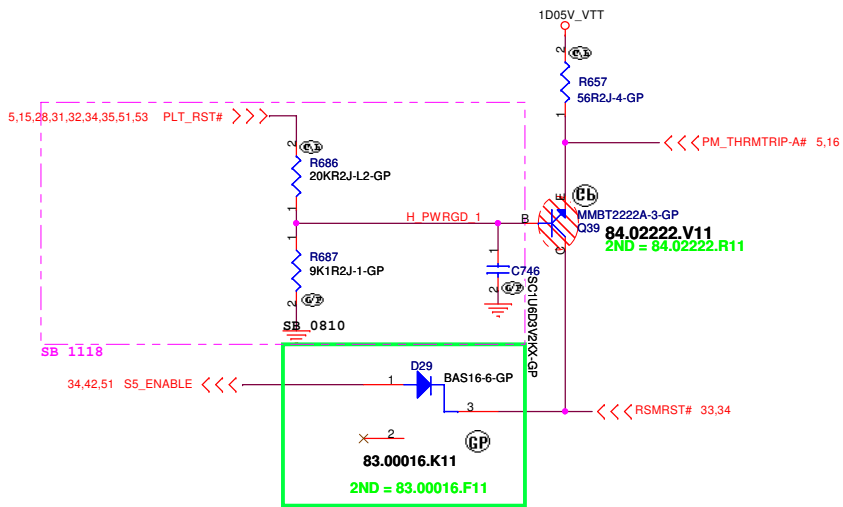
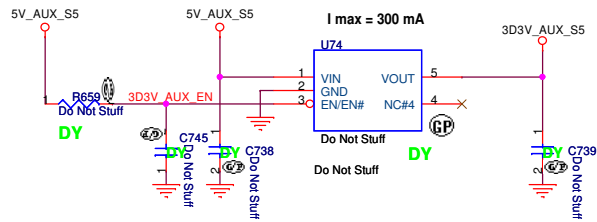
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			POWER CONN		
Size	Document Number		Rev		
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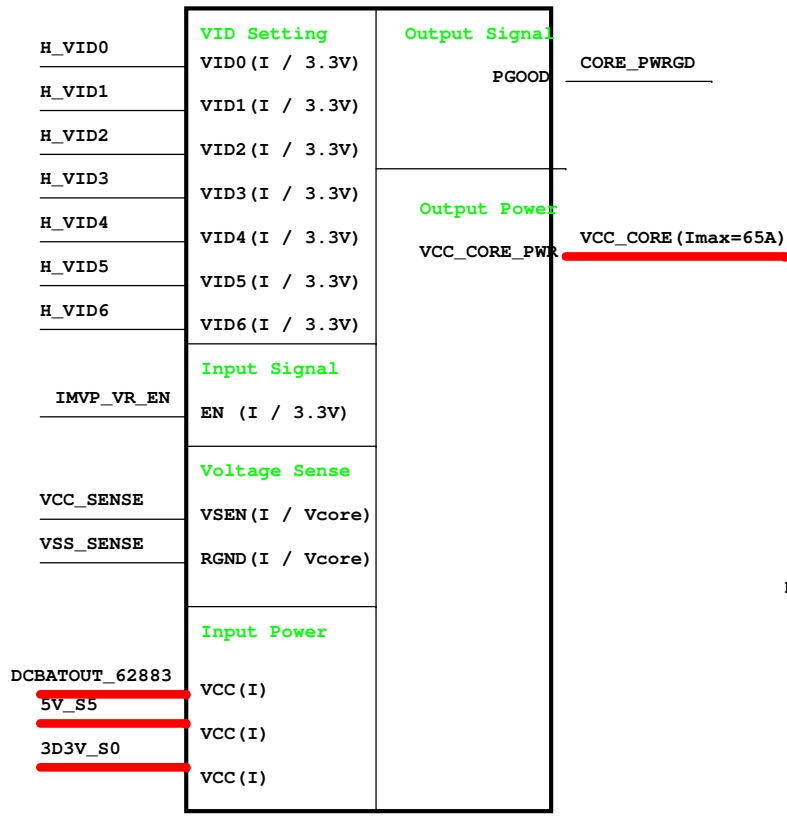
# Run Power

## Aux Power

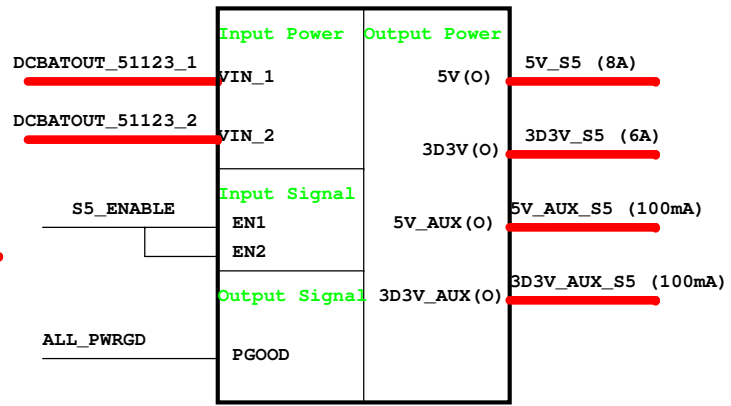
3D3V\_AUX\_S5



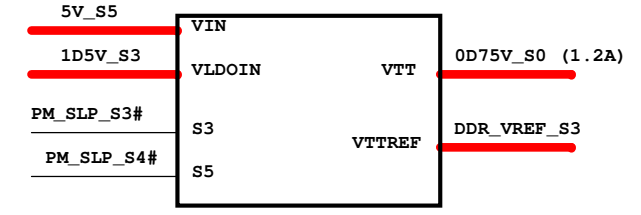
**ISL62883 VCC\_CORE**



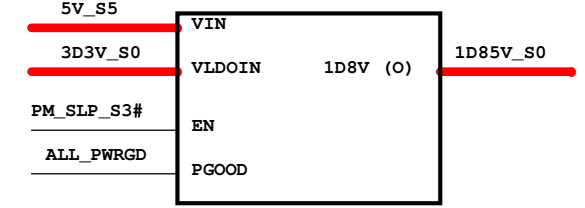
**TPS51123 5V/3D3V**



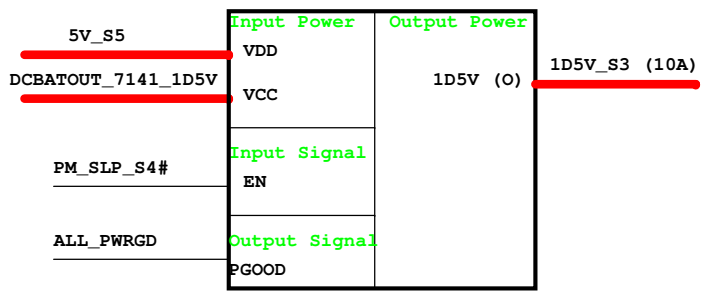
**RT9026 0D75V\_S0**



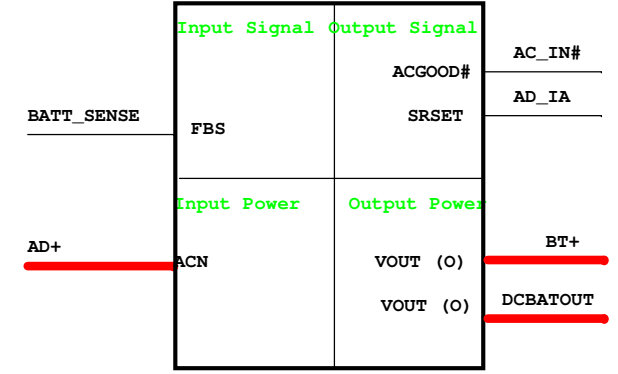
**RT9025 1D8V**



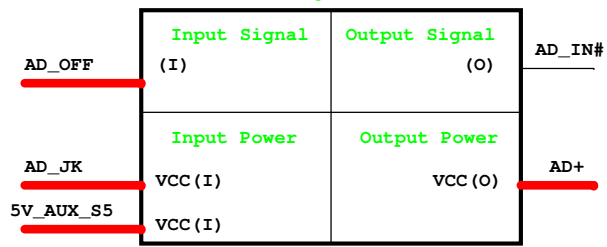
**RT9025 1D5V**



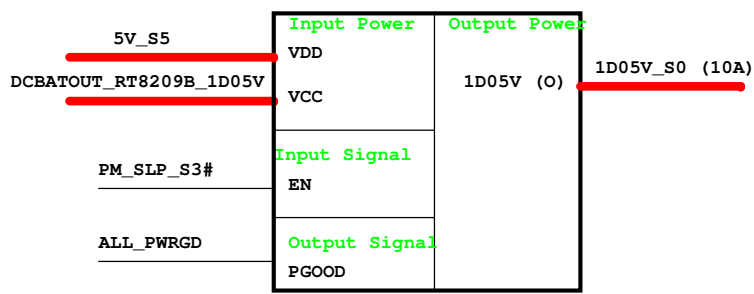
**Charger BQ24745**



**Adapter**

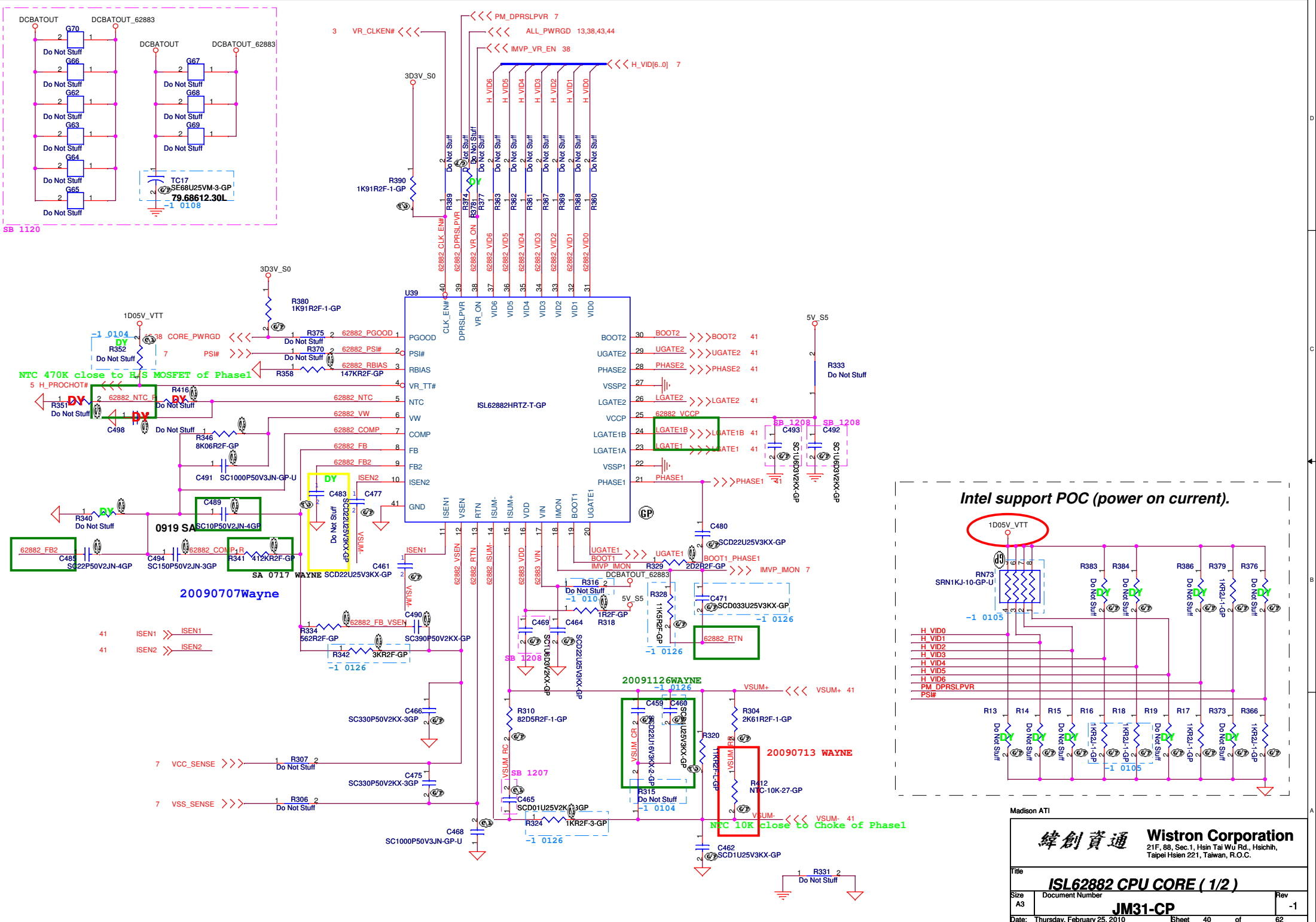


**RT8209B 1D05V**

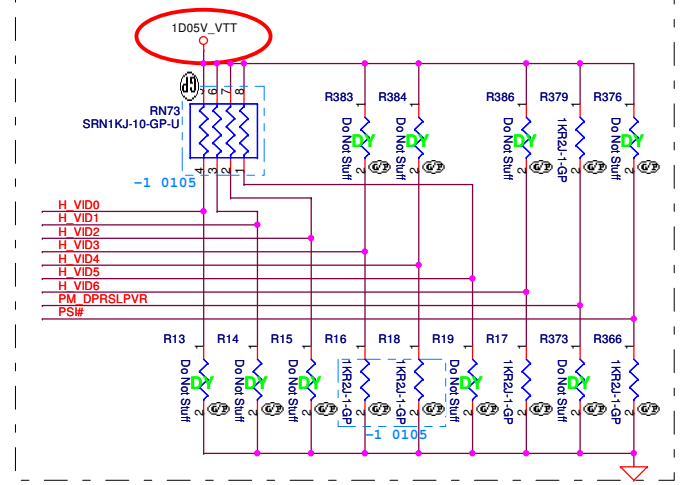


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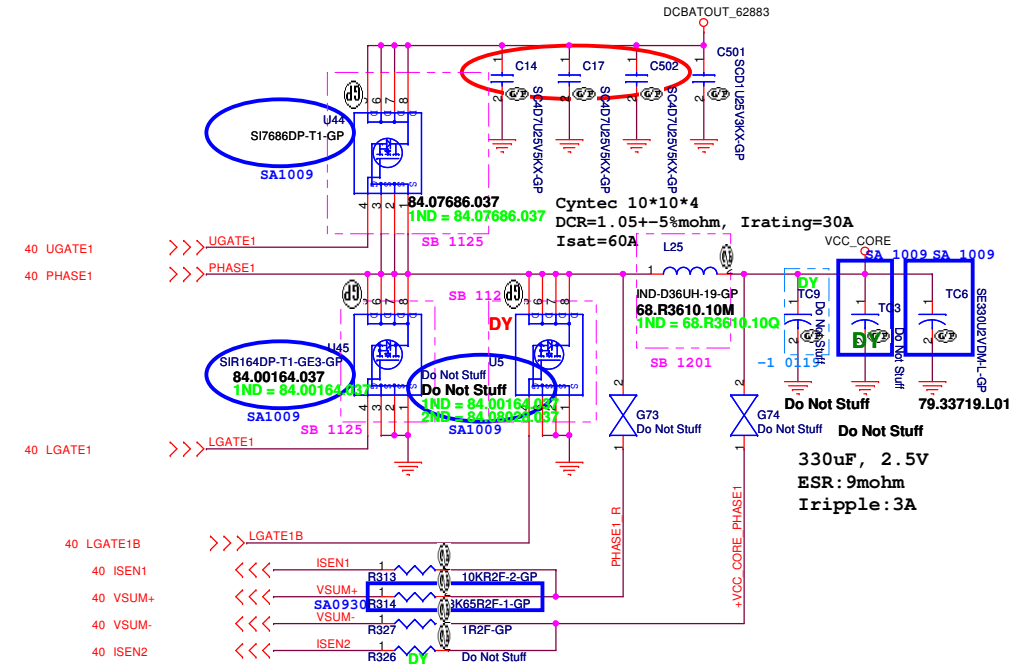
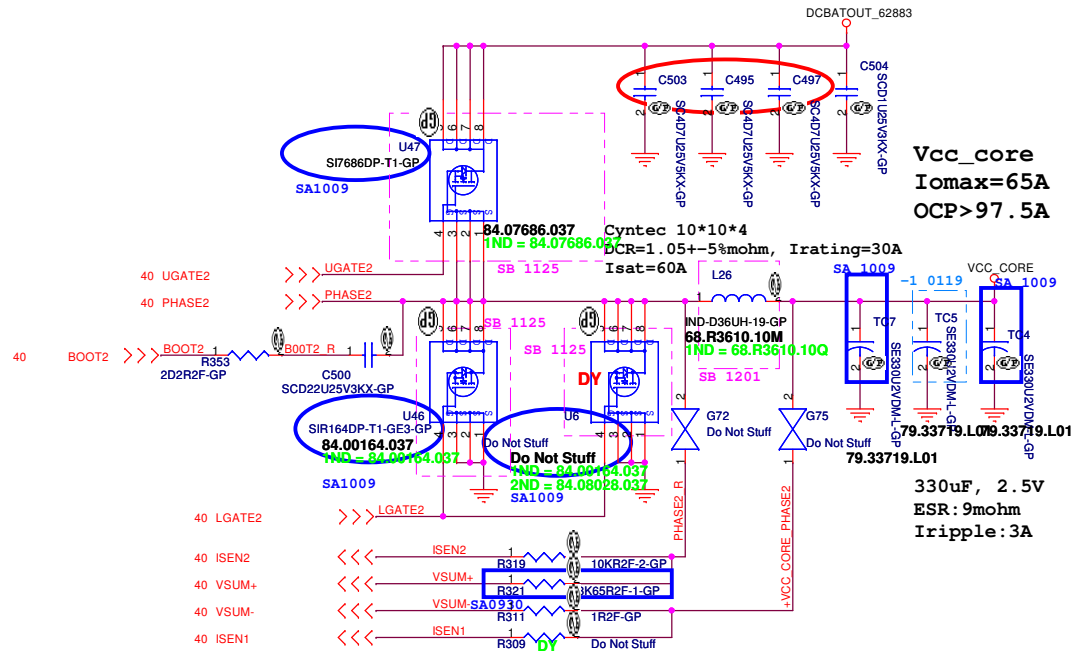
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>Power Block Diagram</b>			
Size	Document Number	Rev	SA
<b>JM31-CP</b>			
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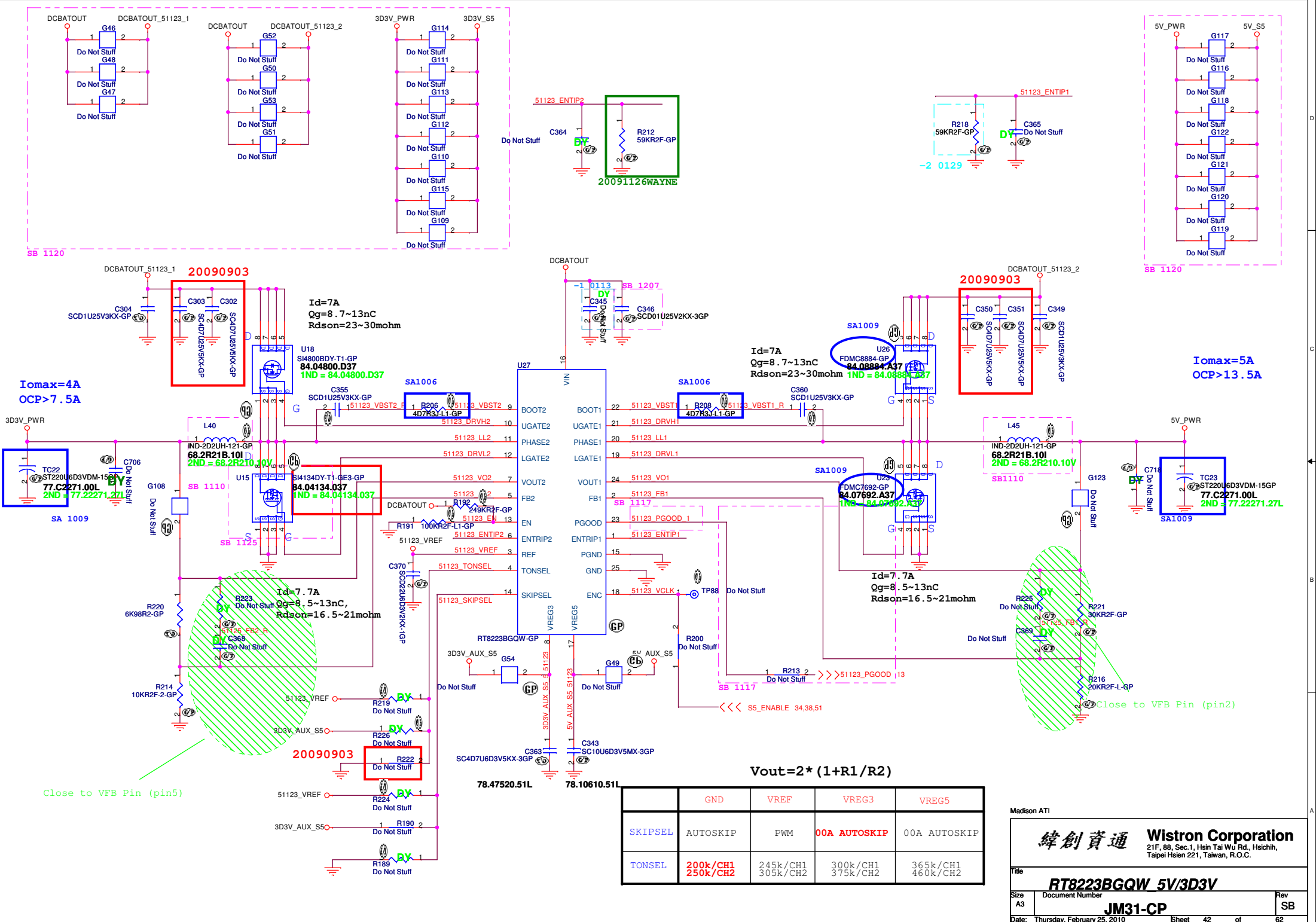


**Intel support POC (power on current).**









SB 1120

SB 1120

I<sub>omax</sub>=4A  
OCP>7.5A

I<sub>omax</sub>=5A  
OCP>13.5A

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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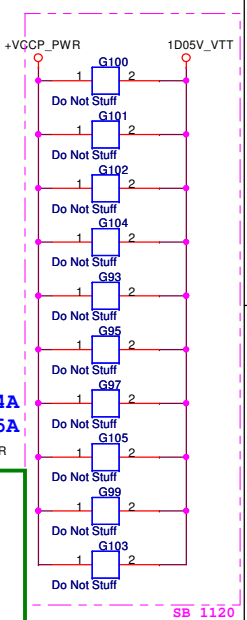
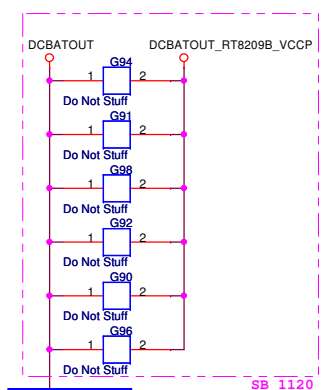
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223BGQW 5V/3D3V**

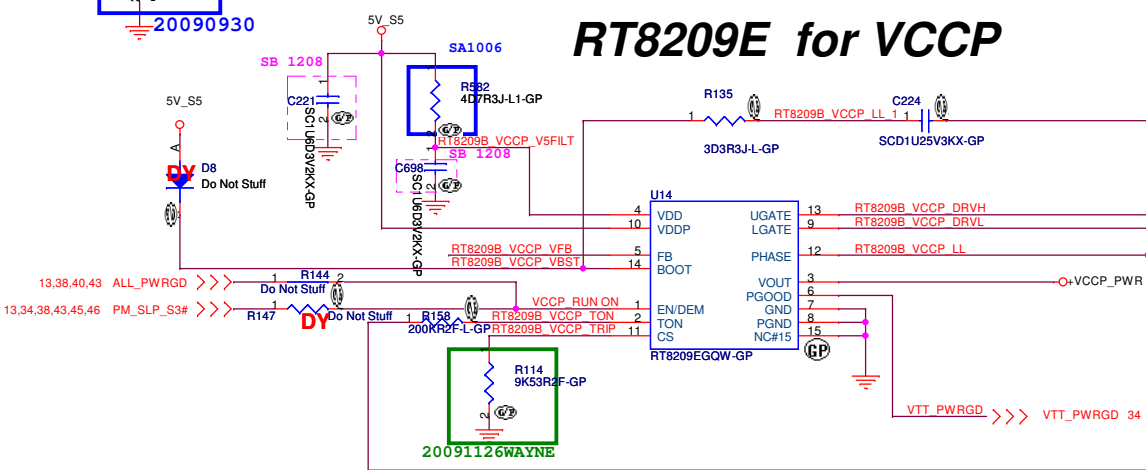
Size A3 Document Number **JM31-CP** Rev SB

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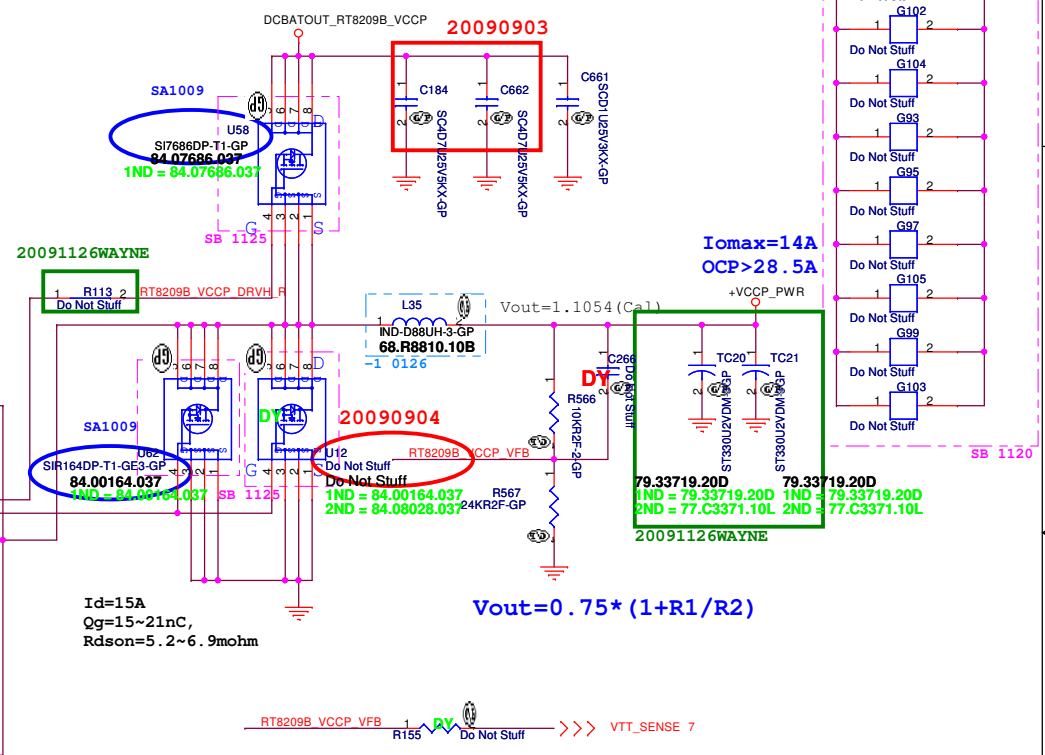




# RT8209E for VCCP



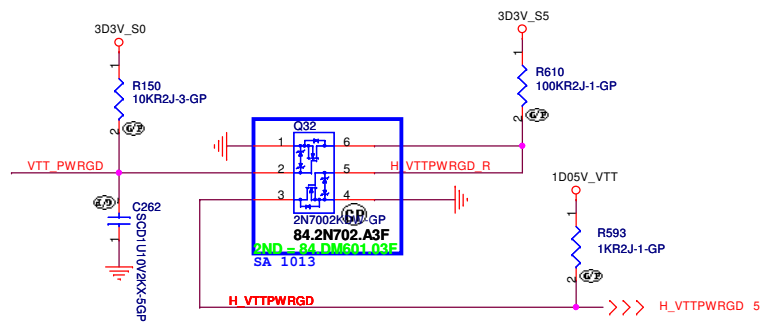
Freq=360KHz



Id=15A  
Qg=15~21nC,  
Rdson=5.2~6.9mohm

$$V_{out} = 0.75 * (1 + R1/R2)$$

I<sub>omax</sub>=14A  
OCP>28.5A



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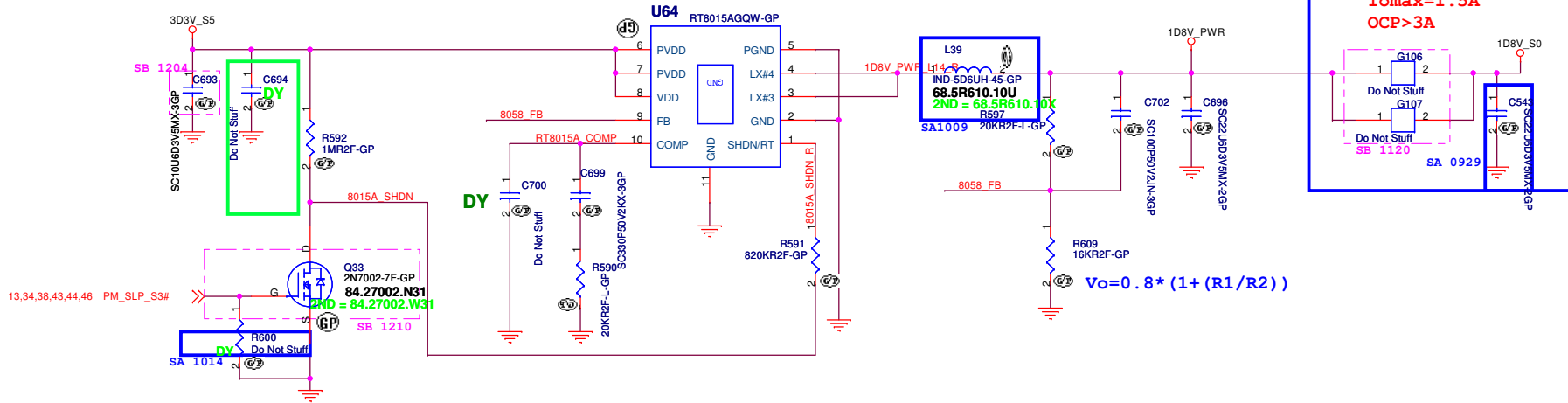
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8209E +VCCP**

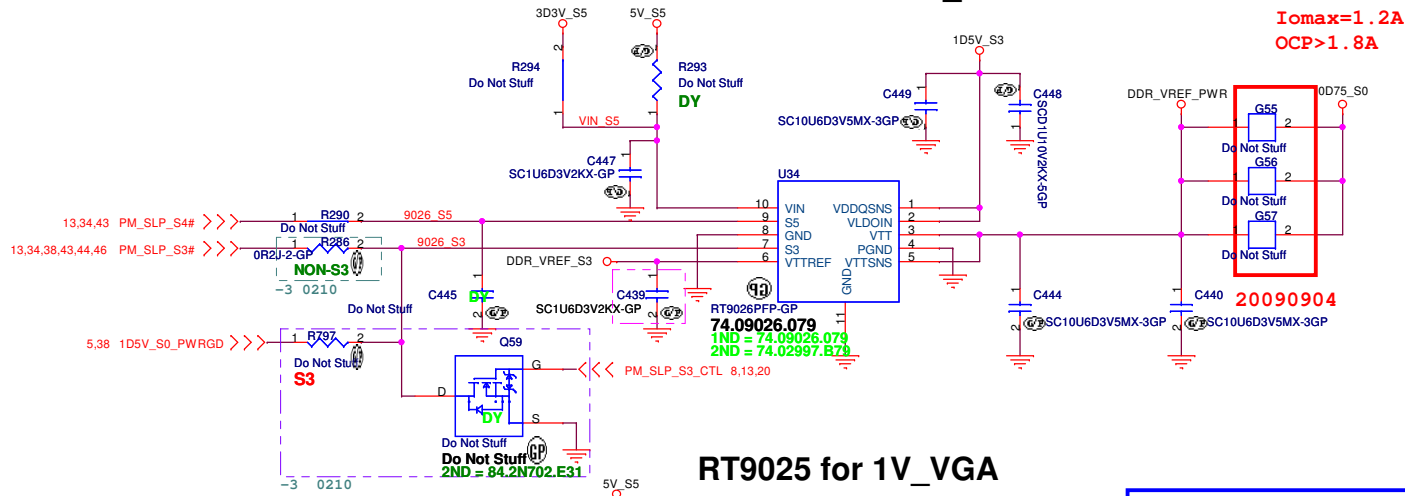
Size A3 Document Number **JM31-CP** Rev **SB**

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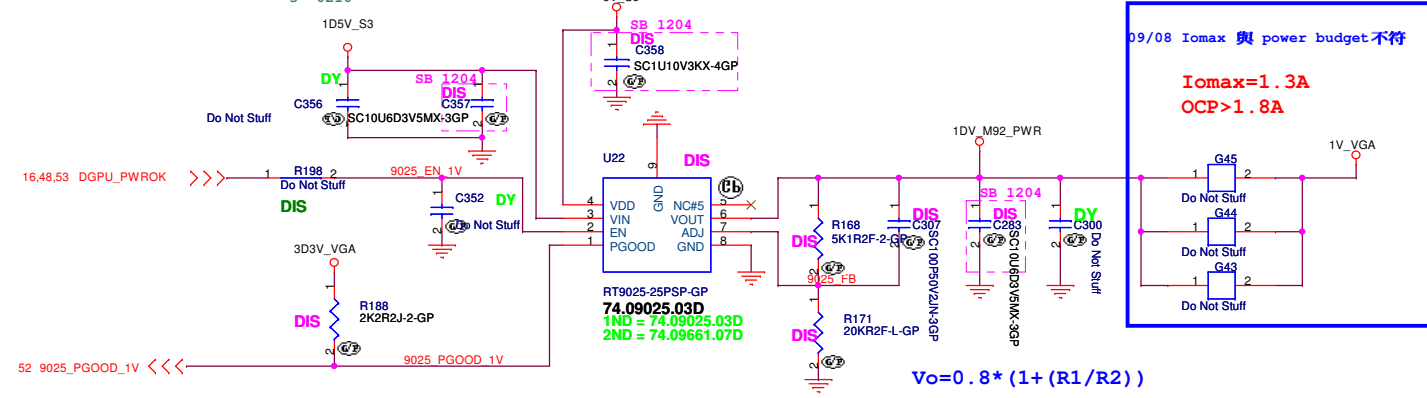
### RT8015A for 1D8V\_S0

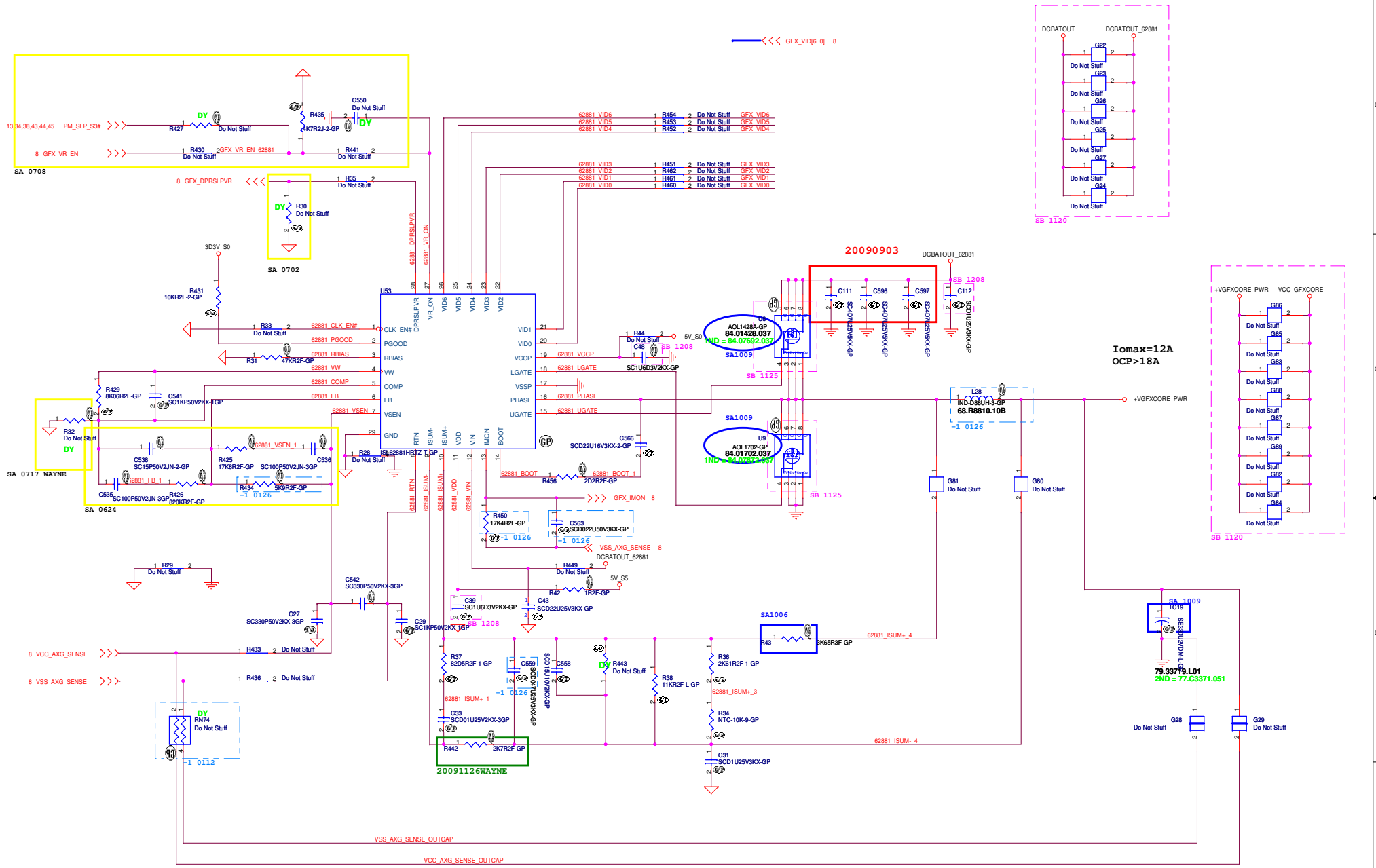


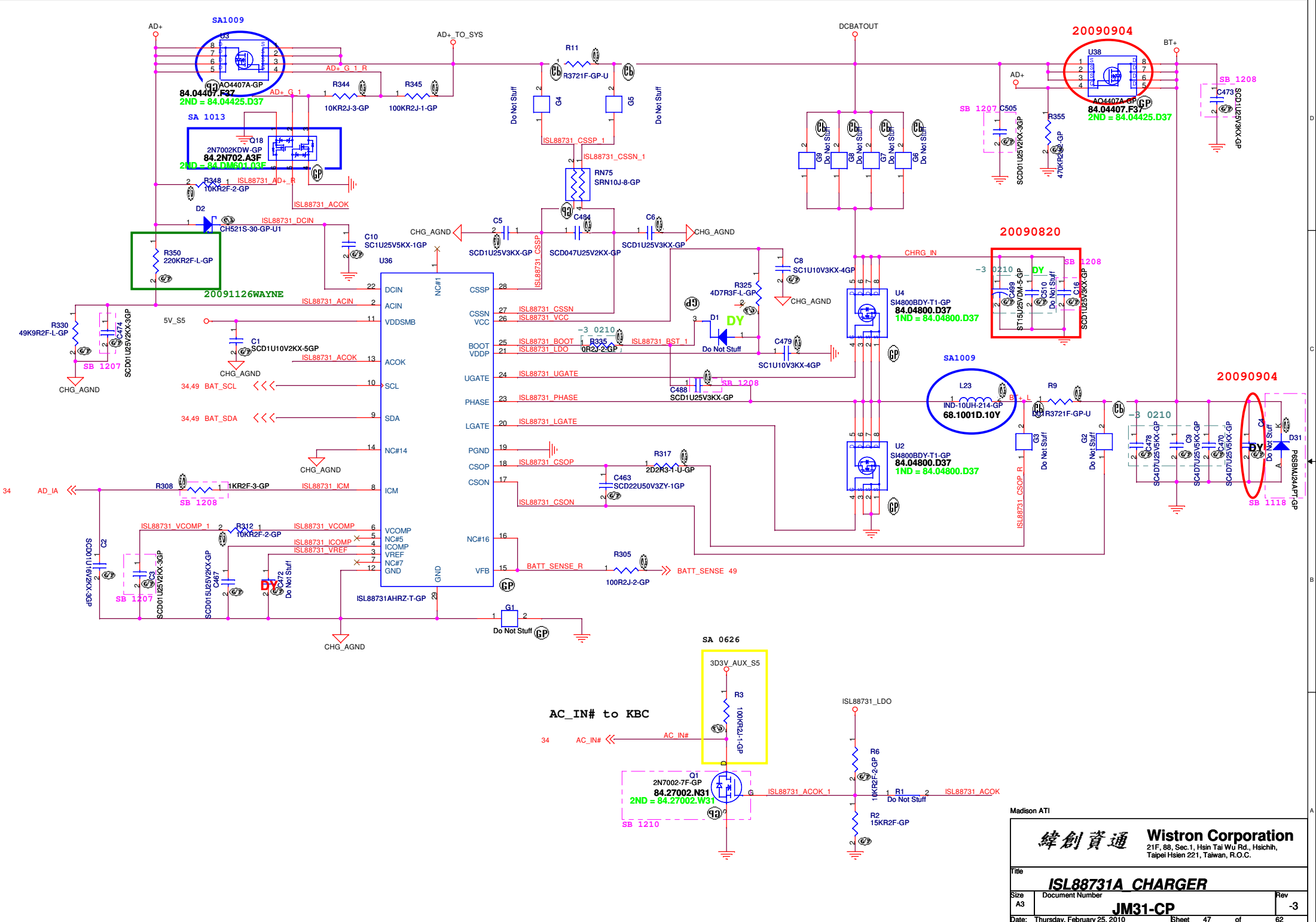
### 09/08 add 3D3V\_S5, R837, R836 RT9026 for 0D75V\_S3



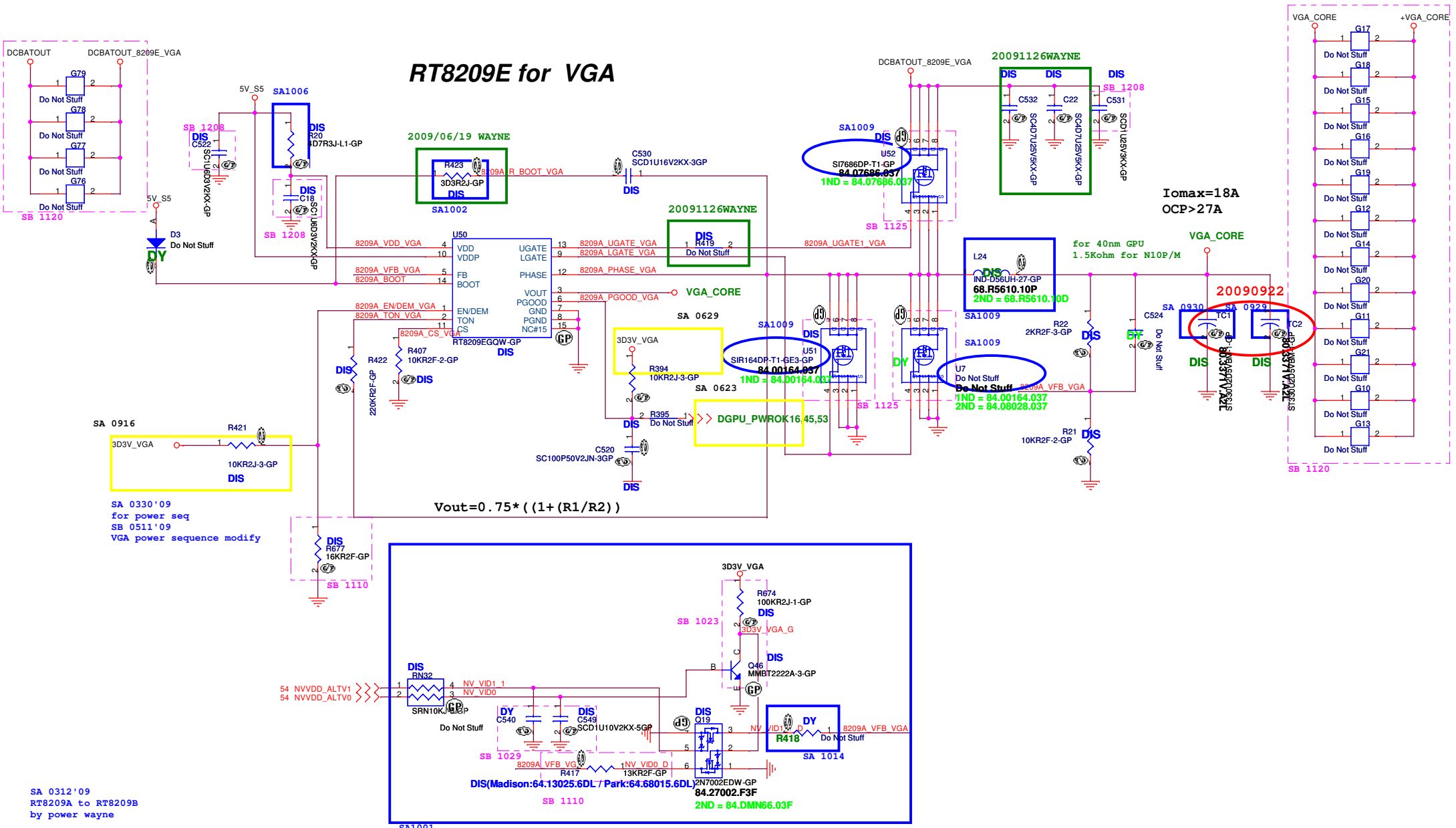
### RT9025 for 1V\_VGA







# RT8209E for VGA



I<sub>omax</sub>=18A  
OCP>27A

$$V_{out} = 0.75 * ((1 + (R1/R2)))$$

SA 0312'09  
RT8209A to RT8209B  
by power wayne

PARK ( 6.8K)	
GPIO15/VID0	VGA_CORE
0	0.90V
1	1.12V

MADISON (13K)	
GPIO15/VID0	VGA_CORE
0	0.90V
1	1.02V

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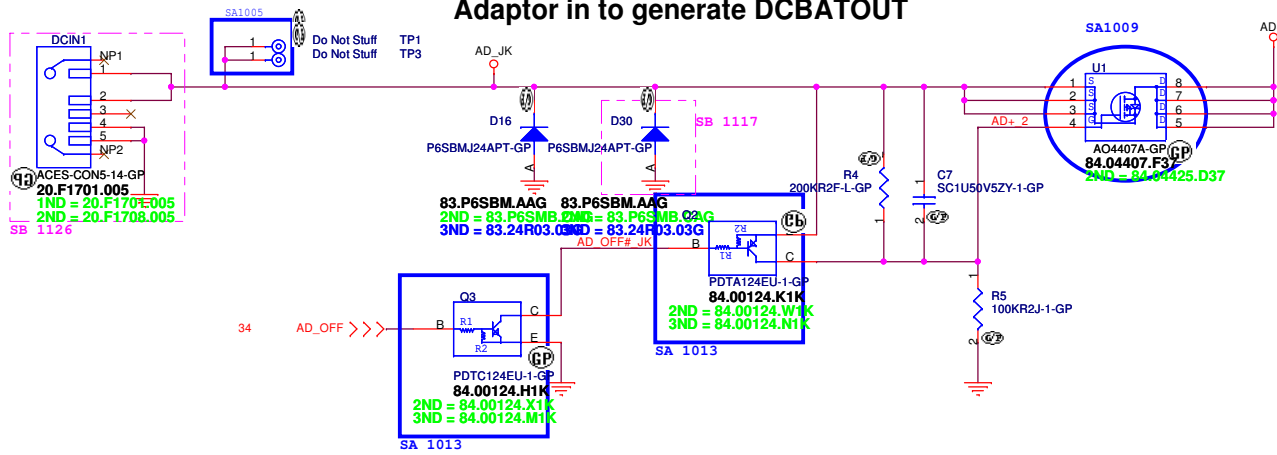
Title: **RT8209E VGA CORE**

Size A3 Document Number **JM31-CP** Rev SB

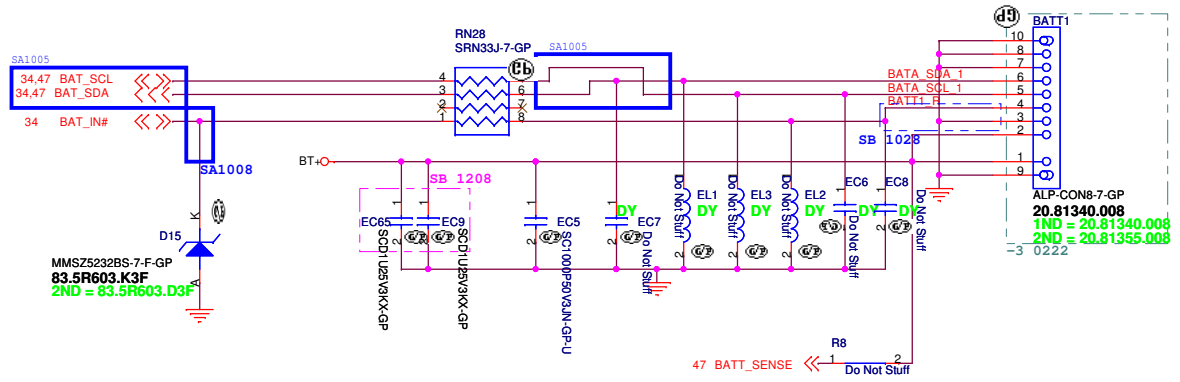
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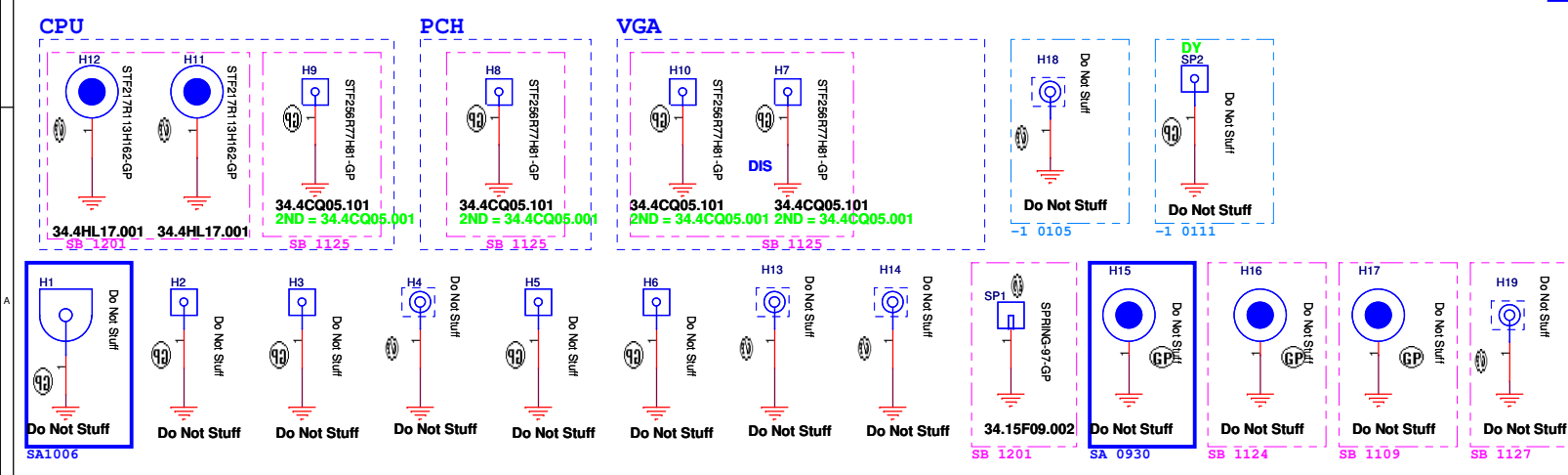
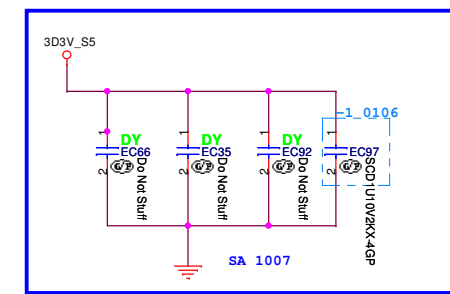
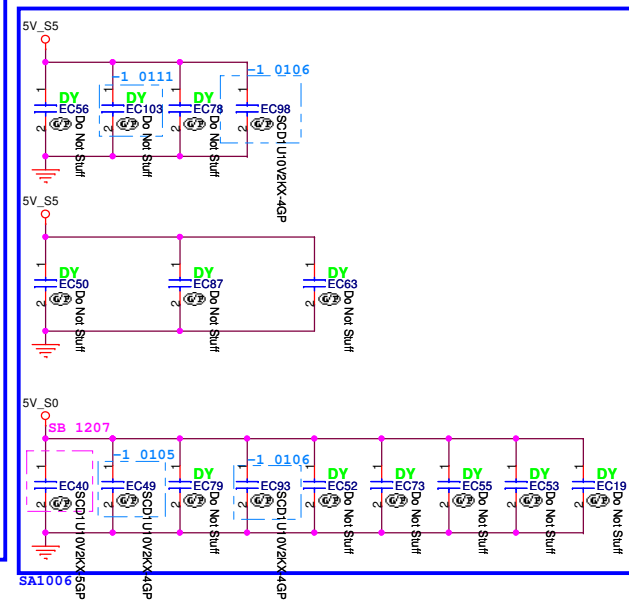
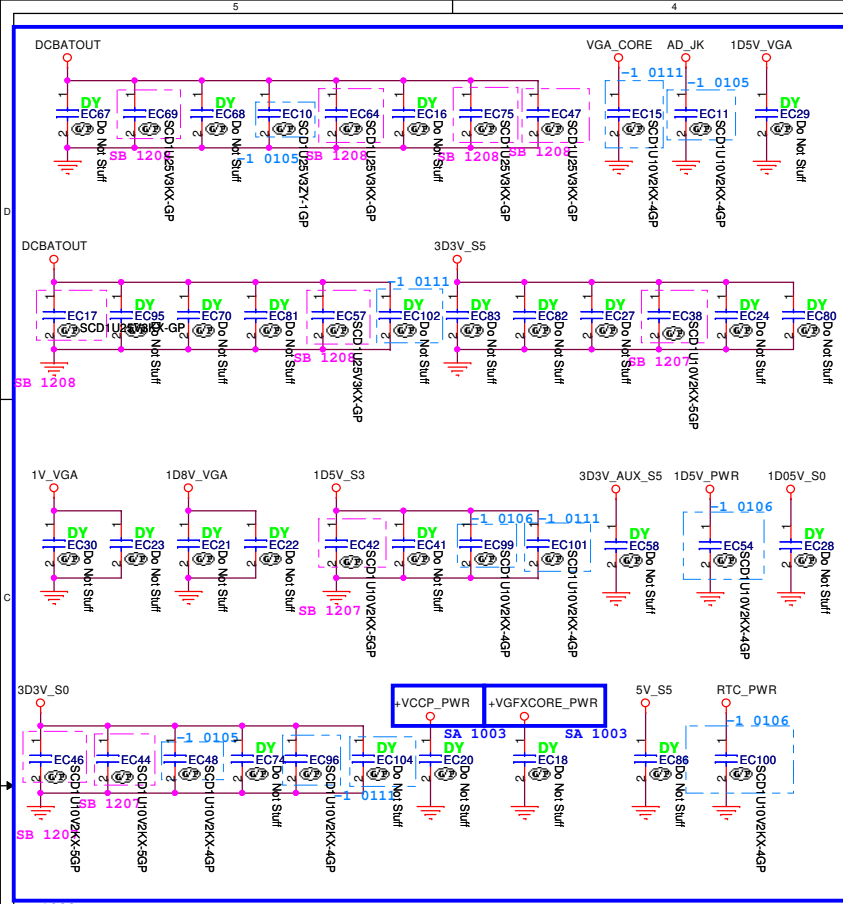


# Adaptor in to generate DCBATOUT



# BATTERY CONNECTOR





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Title

**EMI/Spring/Boss**

Size A3 Document Number

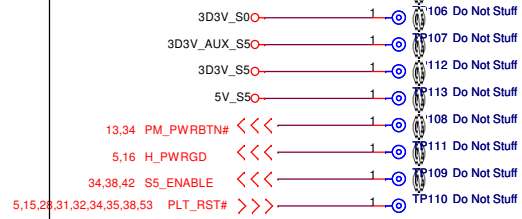
**JM31-CP**

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## Check test point



Test Point 放在 Dimm Door 打開可量測處

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 Taipei Hsien 221, Taiwan, R.O.C.

Title

**AFTE TP**

Size  
A3

Document Number

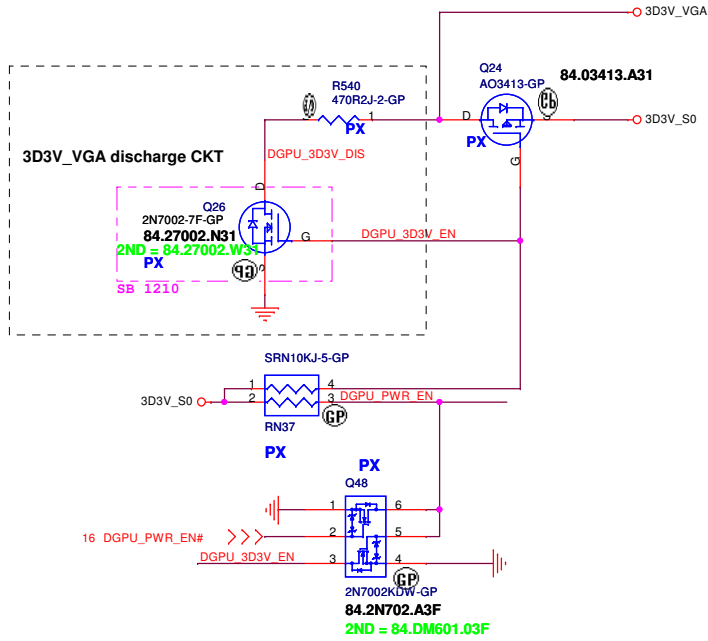
**JM31-CP**

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SA

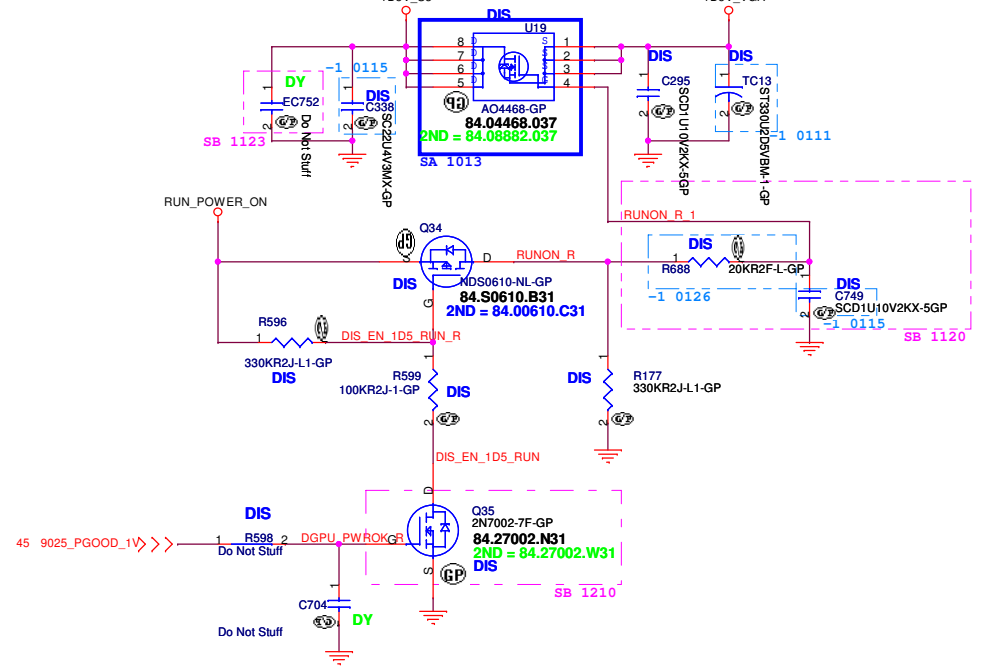
Date: Thursday, February 25, 2010

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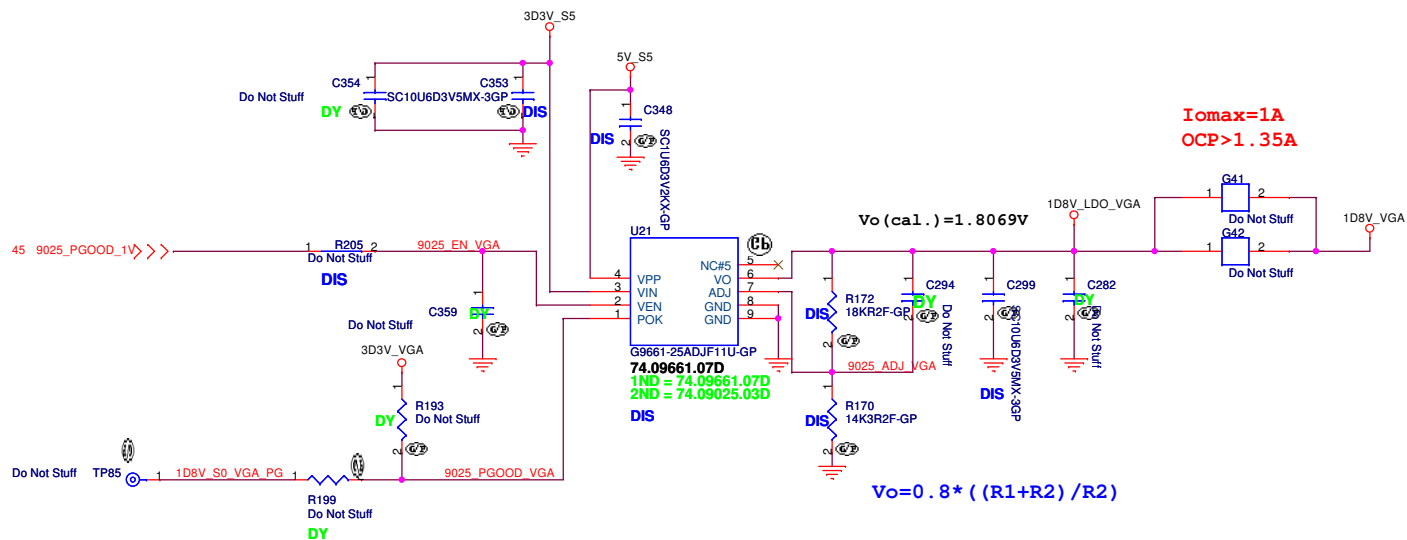
### +3VS to 3.3V\_DELAY Transfer



A04468, SO-8  
 $I_d=11.6A$ ,  $Q_g=9-12nC$   
 $R_{dson}=17.4-22m\ ohm$



### G9661 for 1D8V\_VGA



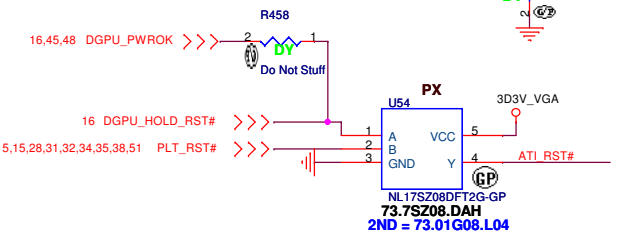
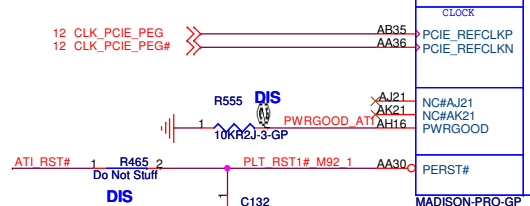
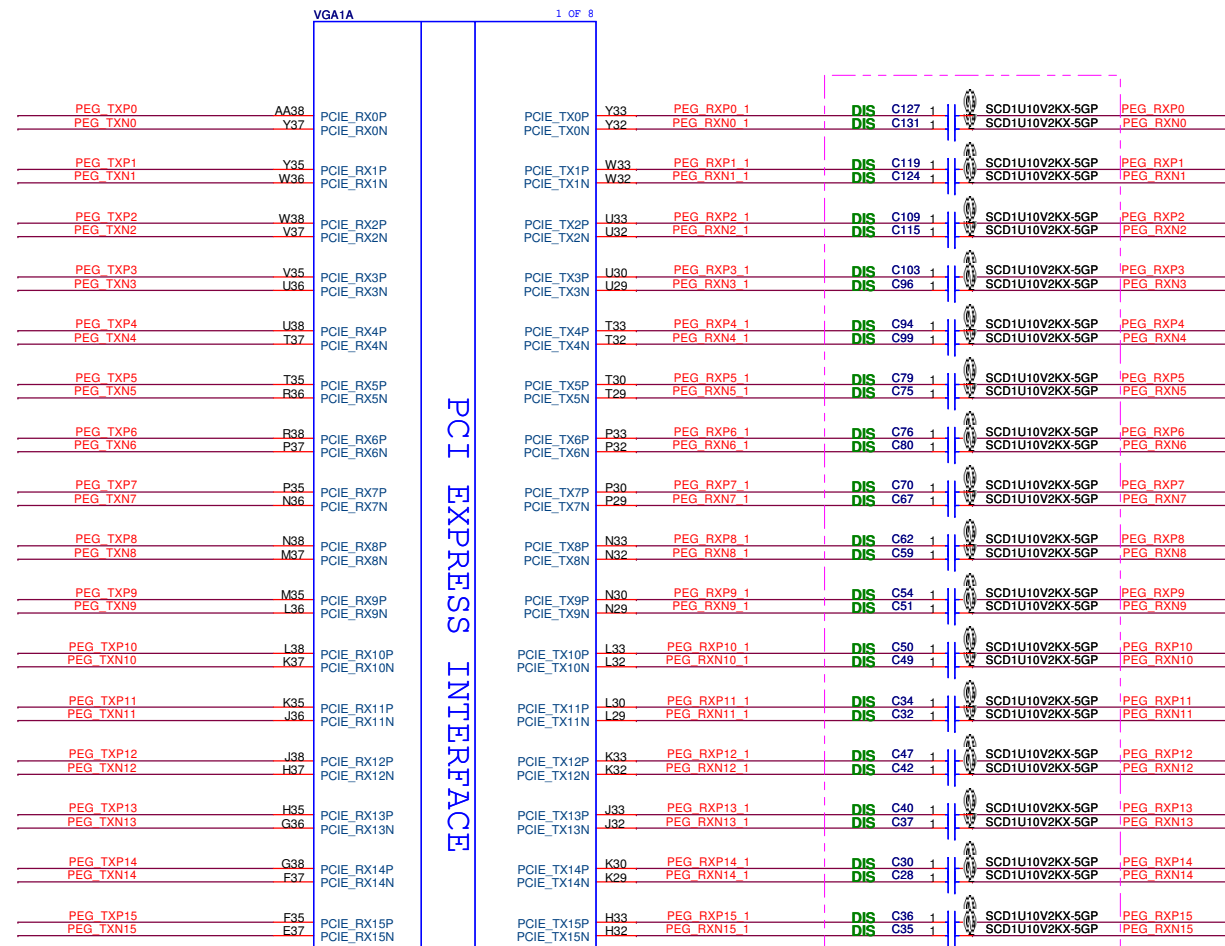
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		
ATI POWER		
Size	Document Number	Rev
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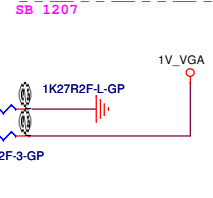
4 PEG\_TXP[15..0] << PEG\_TXP[15..0]  
 4 PEG\_TXN[15..0] << PEG\_TXN[15..0]

4 PEG\_RXP[15..0] << PEG\_RXP[15..0]  
 4 PEG\_RXN[15..0] << PEG\_RXN[15..0]



PCI EXPRESS INTERFACE

CLOCK  
 PCIE\_REFCLKP  
 PCIE\_REFCLKN  
 CALIBRATION  
 PCIE\_CALRP  
 PCIE\_CALRN  
 PERST#  
 MADISON-PRO-GP  
**71.MDSON.M01**  
 2ND = 71.0PARK.M04  
 DIS



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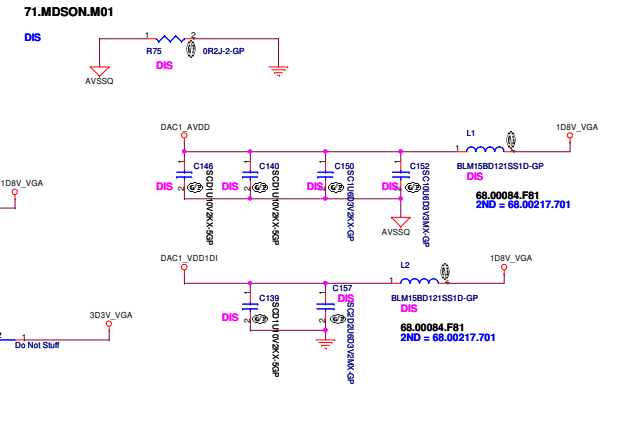
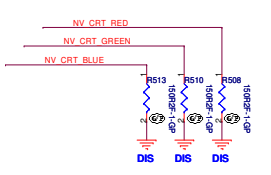
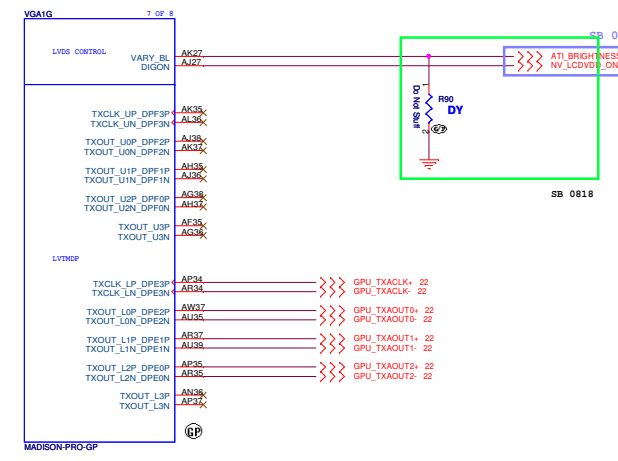
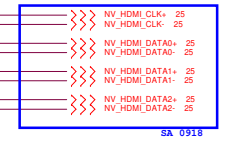
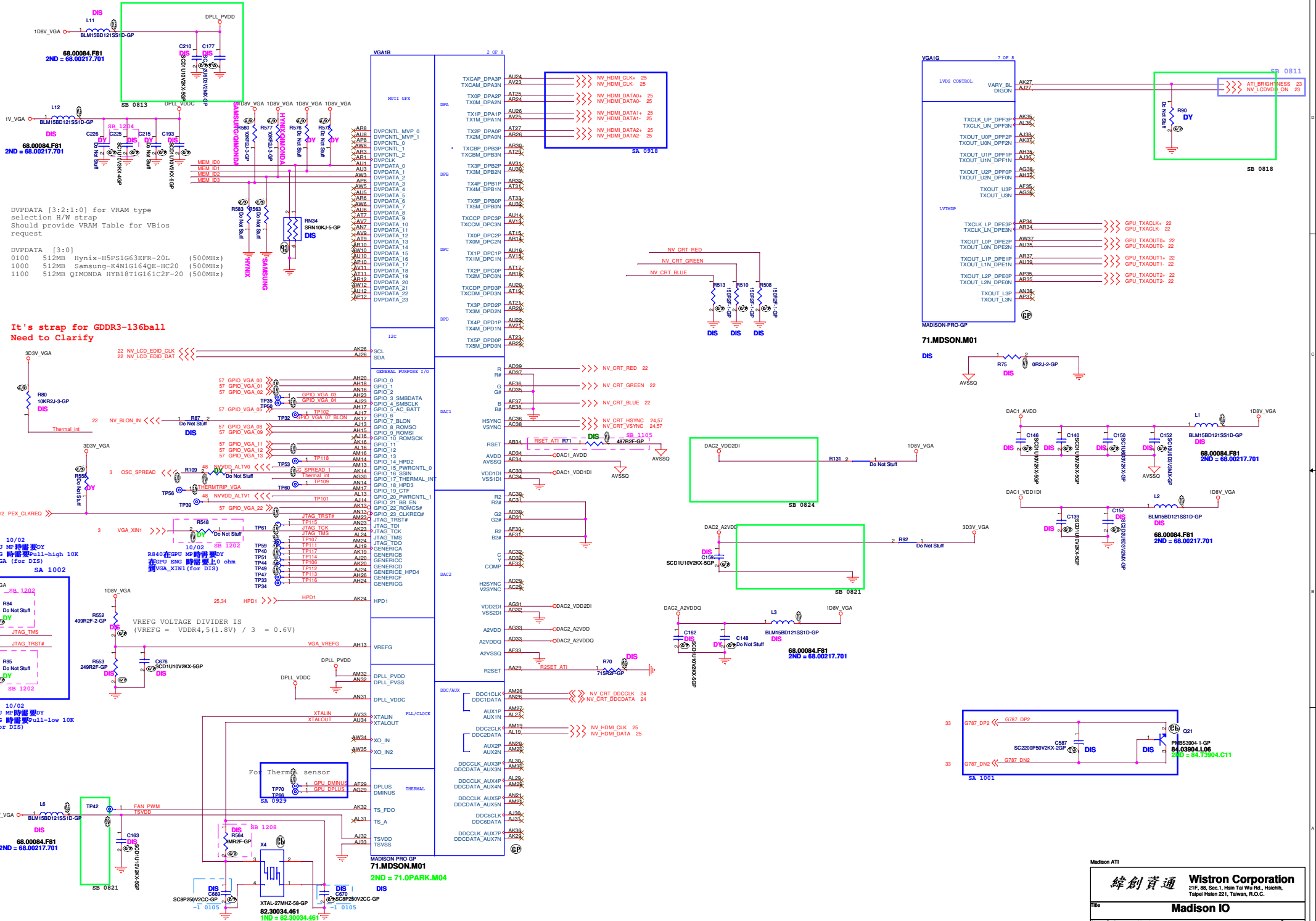
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**Madison PCIE**

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It's strap for GDDR3-136ball  
Need to Clarify

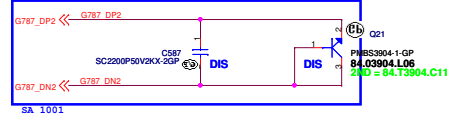
DVPPDATA [3:2:1:0] for VRAM type selection H/W strap  
Should provide VRAM Table for VBios request  
DVPPDATA [3:0]  
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)  
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)  
1100 512MB QIMONDA HYB18T1G16C2F-20 (500MHz)

10/02  
R841在GPU 埠時需要拉up  
在GPU ENG 時需要pull-high 10K 到3D3V\_VGA (for DIS)  
SA 1002

10/02  
R734在GPU 埠時需要拉up  
在GPU ENG 時需要pull-low 10K 到GND (for DIS)

10/02  
R734在GPU 埠時需要拉up  
在GPU ENG 時需要pull-low 10K 到GND (for DIS)

For Thermal sensor  
TP70 1 GPU DMINUS  
TP66 1 GPU DPLUS  
SA 0923



Madison A11

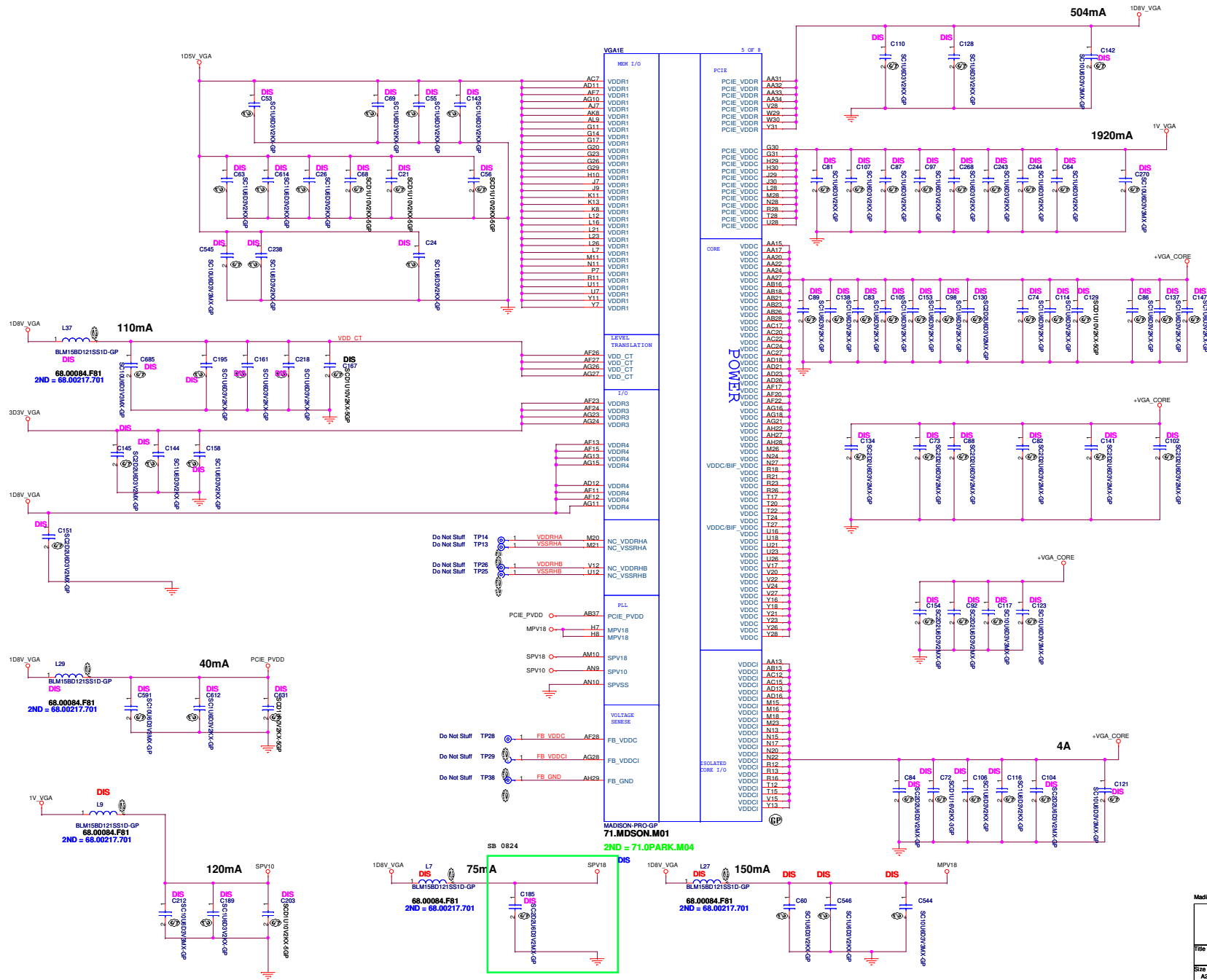
緯創資通 Wistron Corporation

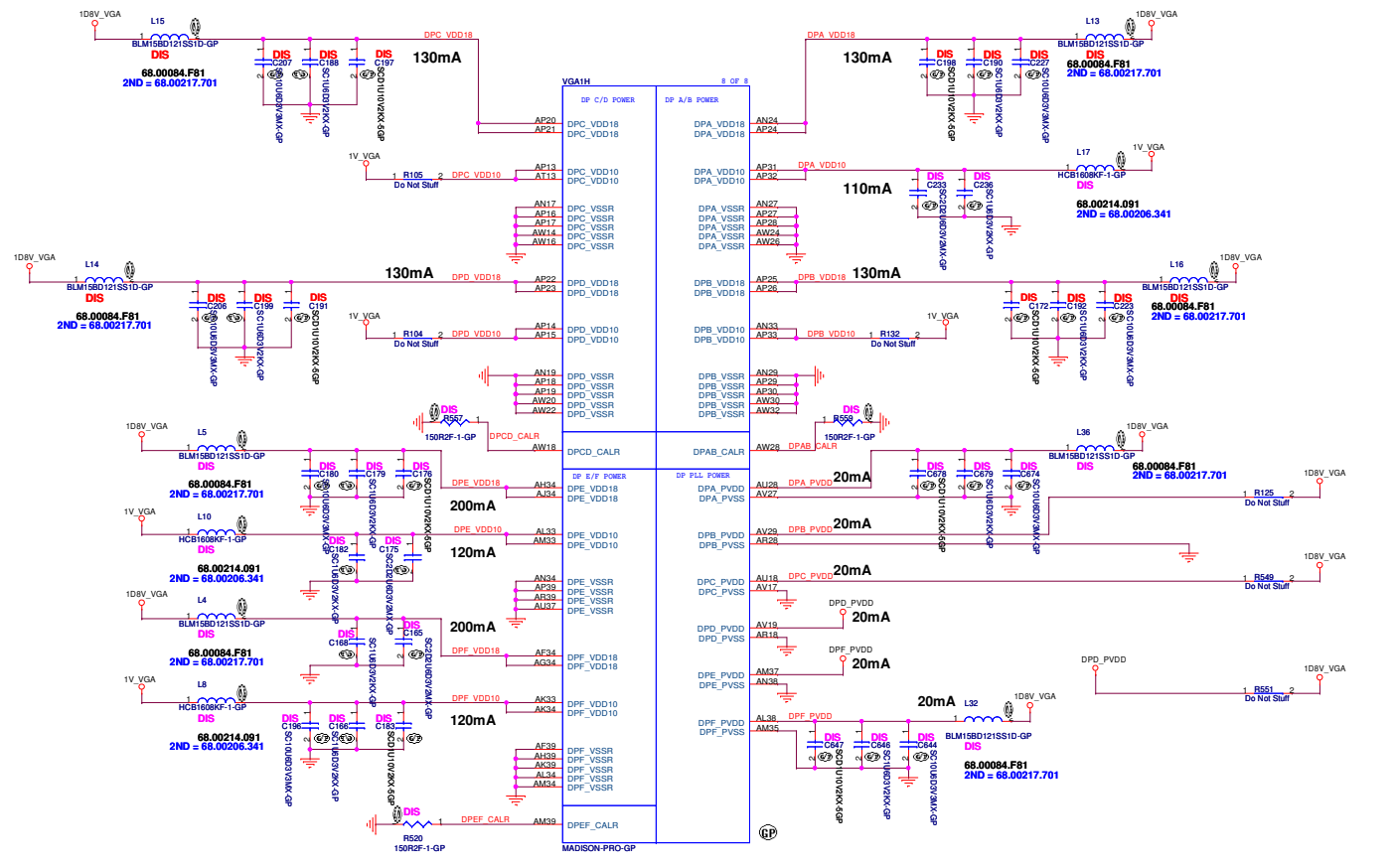
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Rev 1.1

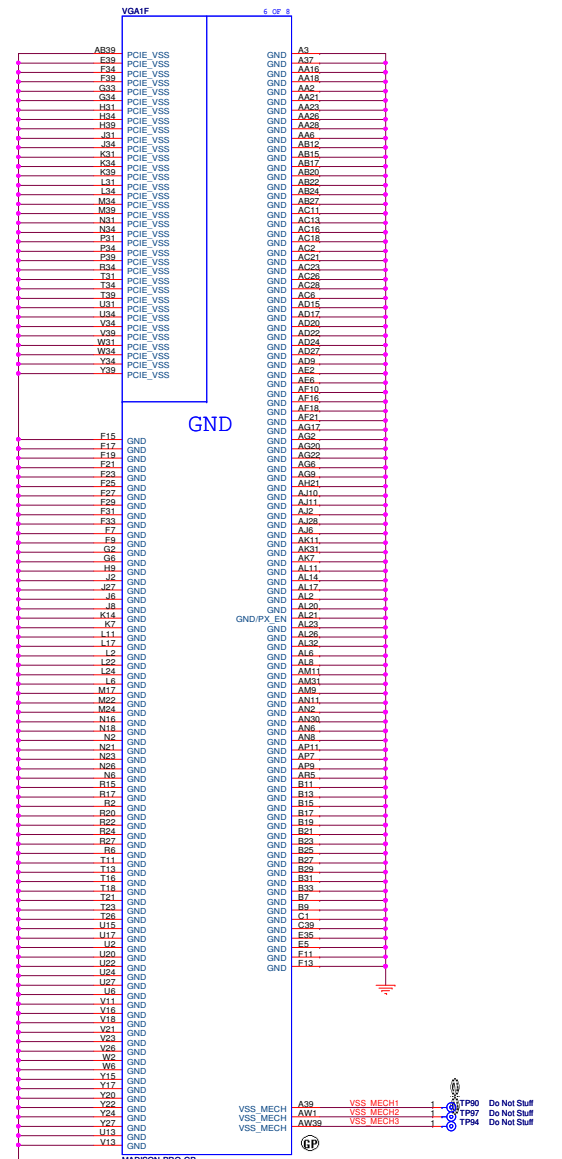
Document Number **JM31-CP**

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71.MDSON.M01  
2ND = 71.0PARK.M04  
DIS

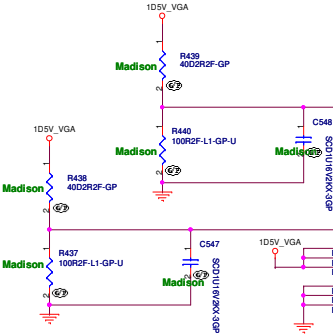


71.MDSON.M01  
2ND = 71.0PARK.M04  
DIS



For SST1-1.8/SST1-2/DDR1/GDDR1: 0.5 \* VDDR1.  
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 \* VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Madison: MEM\_CALRP[0,2] signals are used.  
Park: MEM\_CALRP1 and MEM\_CALRN1 are used.

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe Full Tx Output Swing Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 0: No audio function 01: Audio for DisplayPort and HDMI ( if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	X X

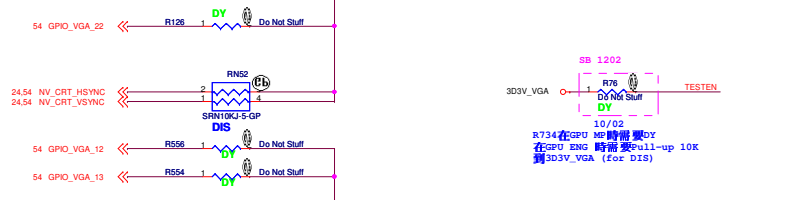
### AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR FULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST	M25P05A
256MB	x001	ST	M25P10A
64MB	x010	ST	M25P20
32MB	x	ST	M25P40
512MB	x	ST	M25P80
1GB	x	Chinglis (formerly PMC)	Pm25LV512A
2GB	x	Chinglis (formerly PMC)	Pm25LV010A
4GB	x	Chinglis (formerly PMC)	Pm25LV010A



Designator	For M97-M2	For Manhattan
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF



Madison AT1

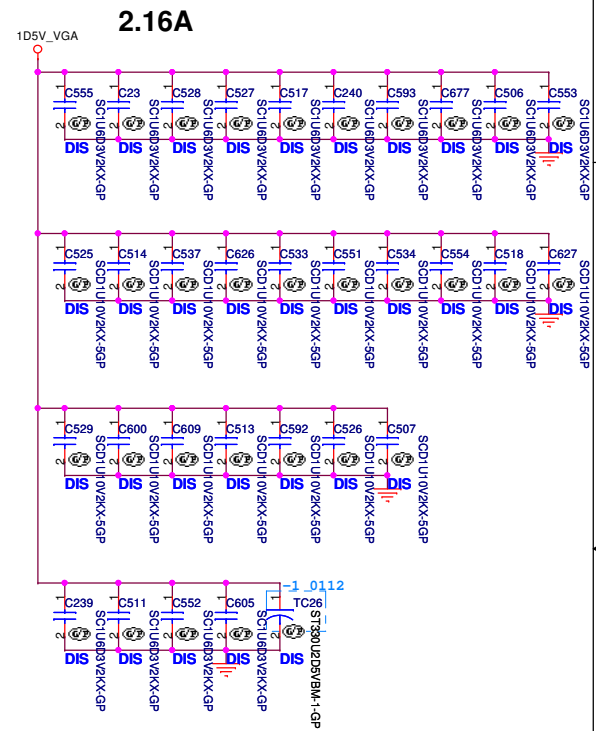
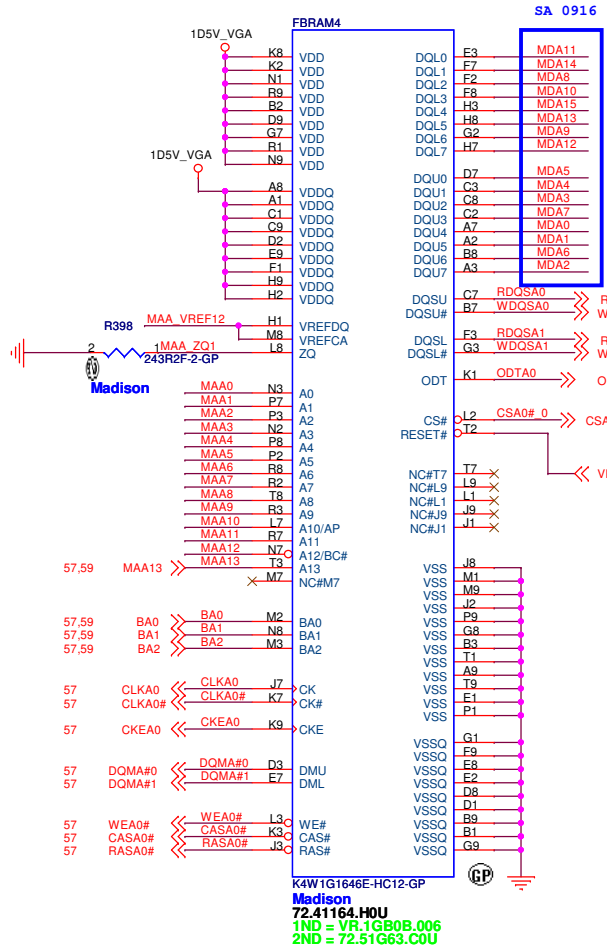
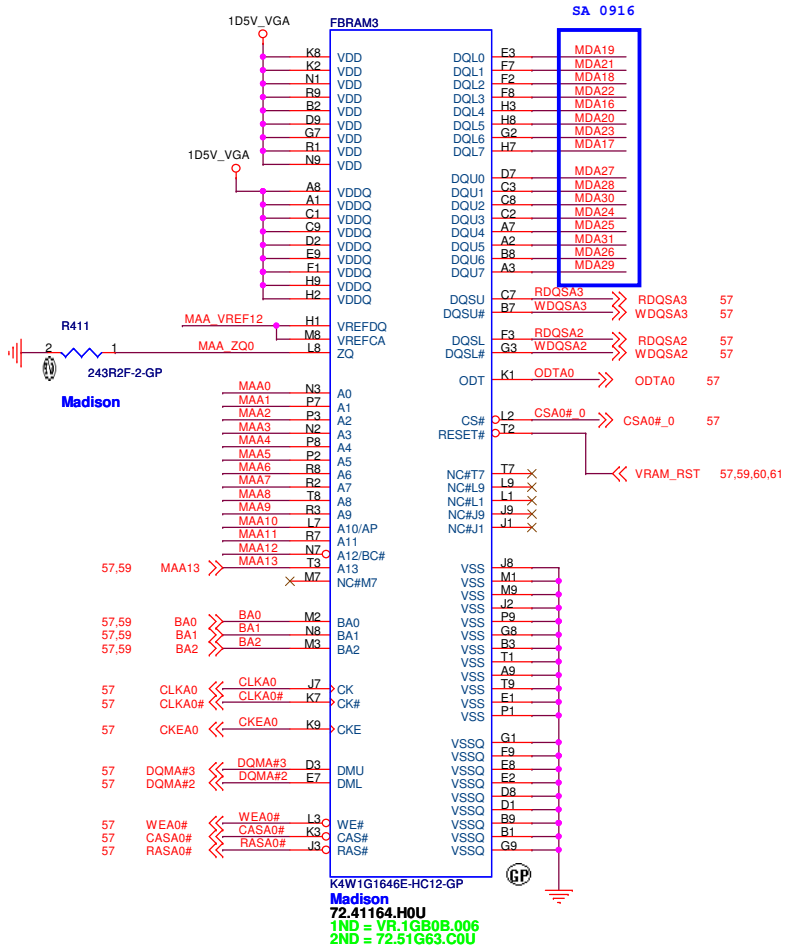
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File: **Madison Memory / Straps**

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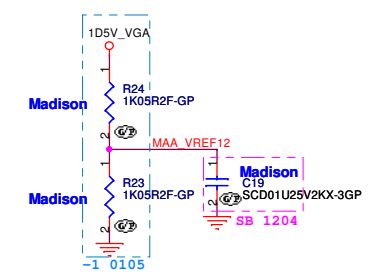
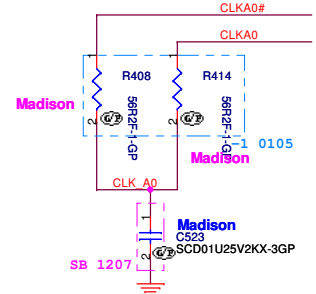
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# DDR3



**SAMSUNG: 72.41164.H0U (VR.1GB0B.006)**  
**HYNIX: 72.51G63.C0U (VR.1GB0G.004)**

- 57,59 DQMA#[0..7] <<>
- 57,59 RDQSA#[0..7] <<>
- 57,59 WDOQA#[0..7] <<>
- 57,59 MAA[0..12] <<
- 57,59 MDA[0..63] <<>



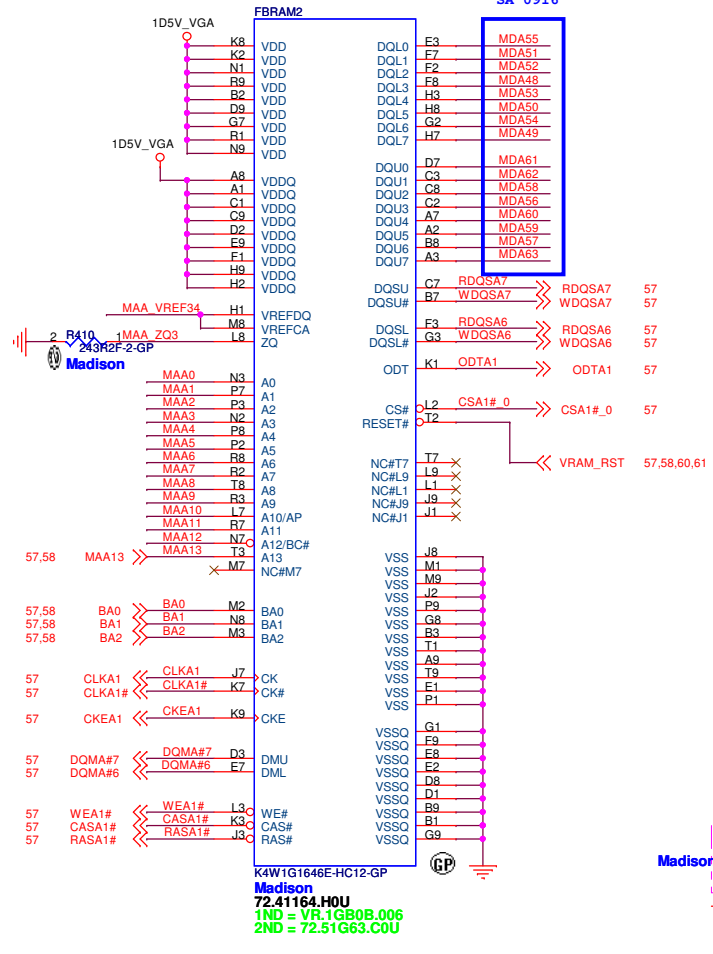
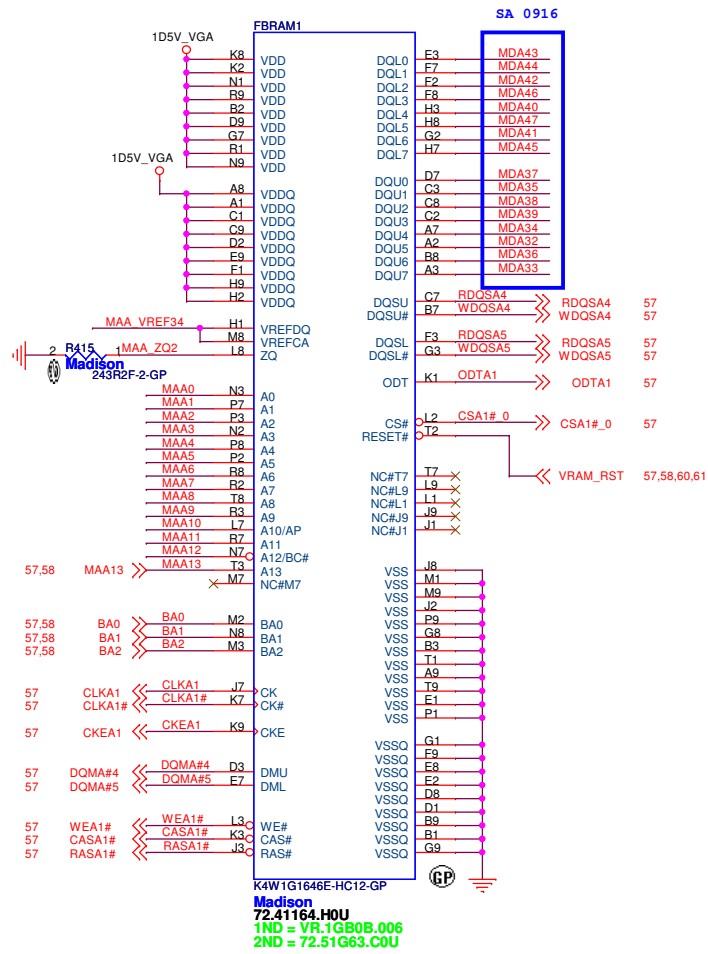
Madison ATI

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Title: **VRAM(1/4)**

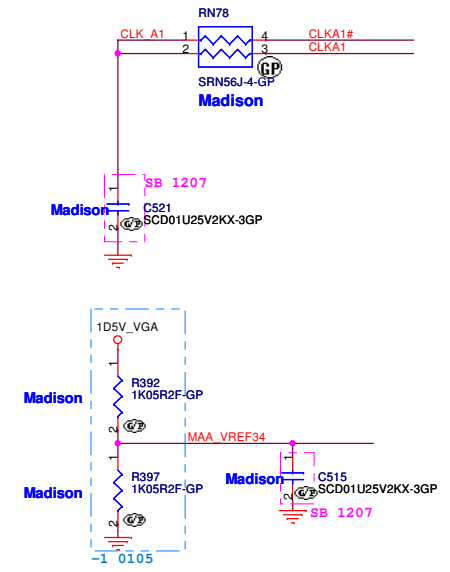
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# DDR3



**SAMSUNG: 72.41164.H0U (VR.1GB0B.006)**  
**HYNIX: 72.51G63.C0U (VR.1GB0G.004)**

- 57.58 DQMA#[0..7] <<>
- 57.58 RDQSA#[0..7] <<>
- 57.58 WDOQA#[0..7] <<>
- 57.58 MAA[0..12] << MAA[0..12]
- 57.58 MDA[0..63] <<> MDA[0..63]



**Madison ATI**

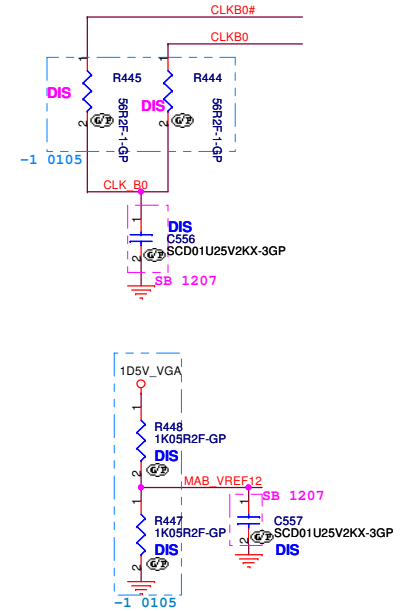
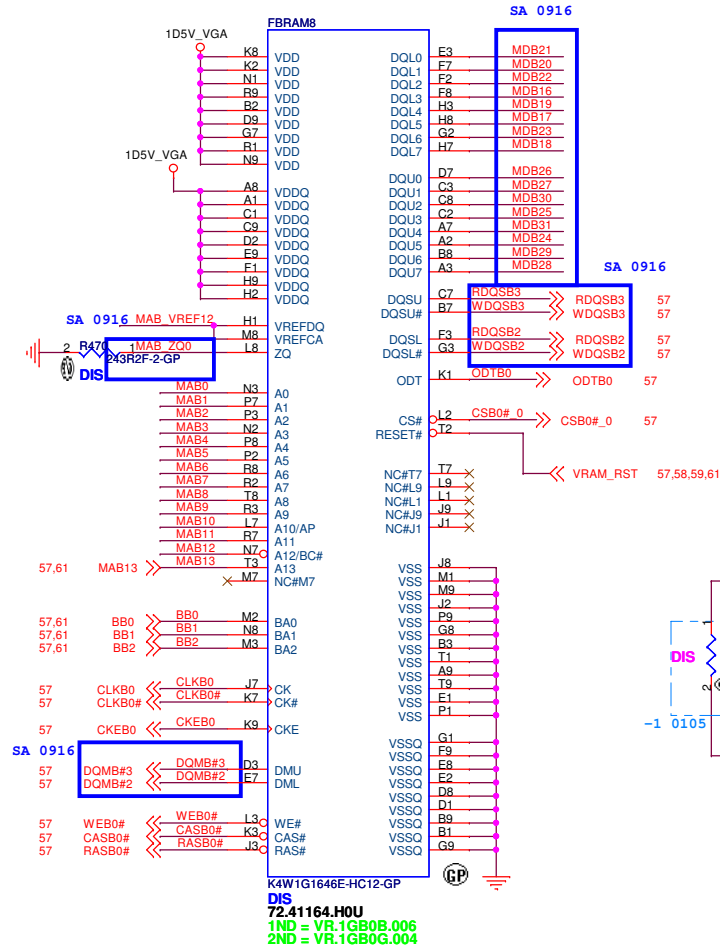
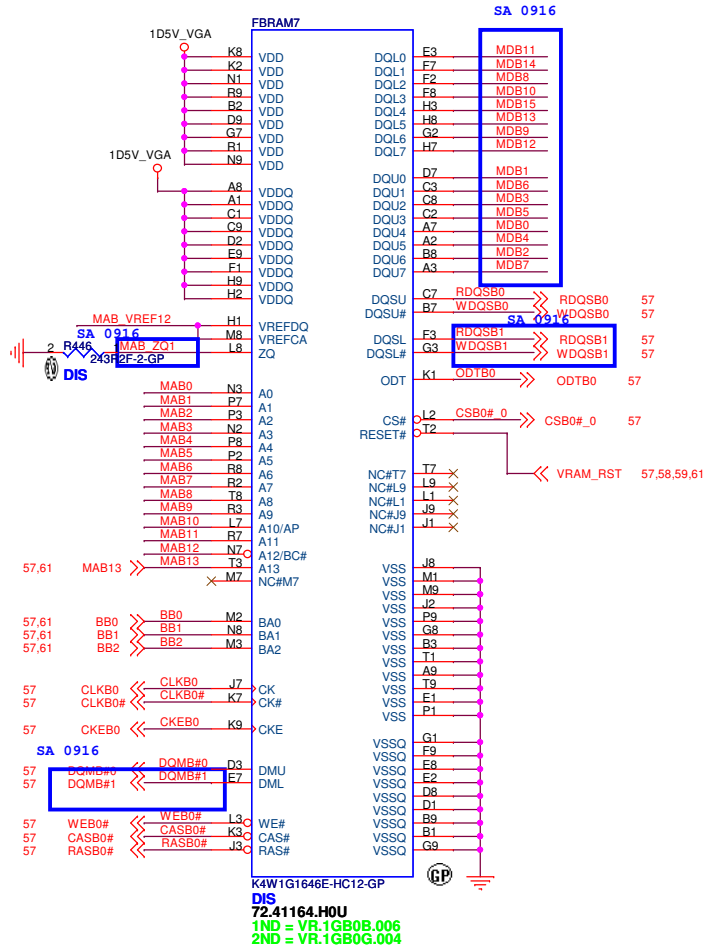
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Title: **VRAM(2/4)**

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# DDR3



**SAMSUNG: 72.41164.H0U (VR.1GB0B.006)**  
**HYNIX: 72.51G63.C0U (VR.1GB0G.004)**

- 57.61 DQMB[0..7] <<>
- 57.61 RDQSB[0..7] <<>
- 57.61 WDQSB[0..7] <<>
- 57.61 MAB[0..12] <<>
- 57.61 MDB[0..63] <<>

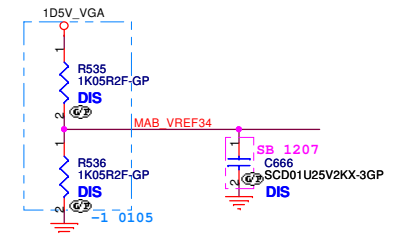
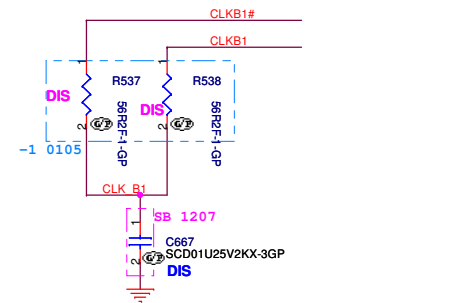
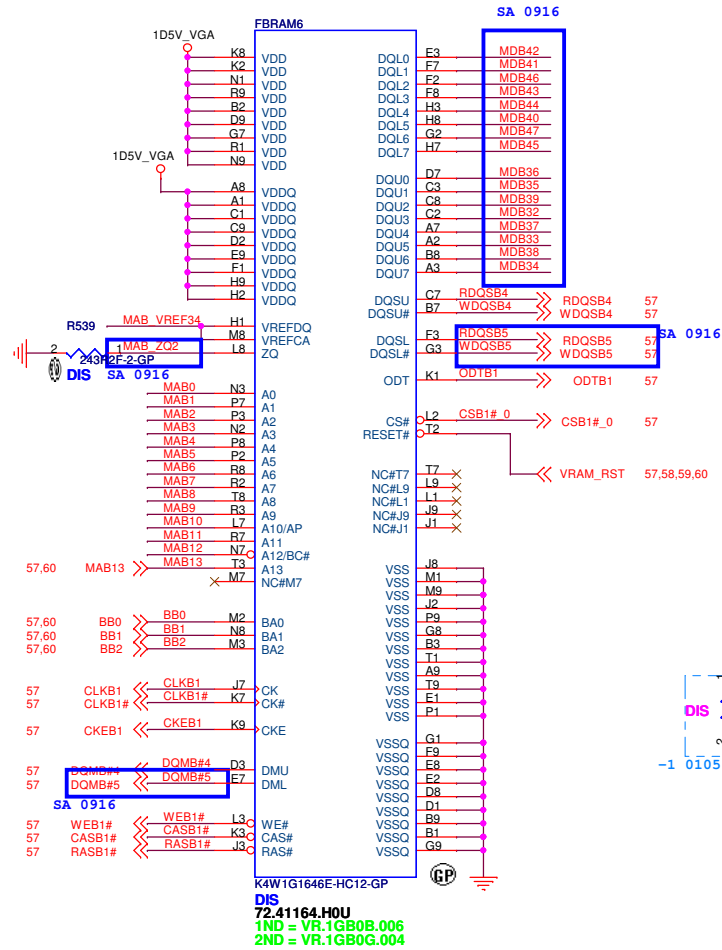
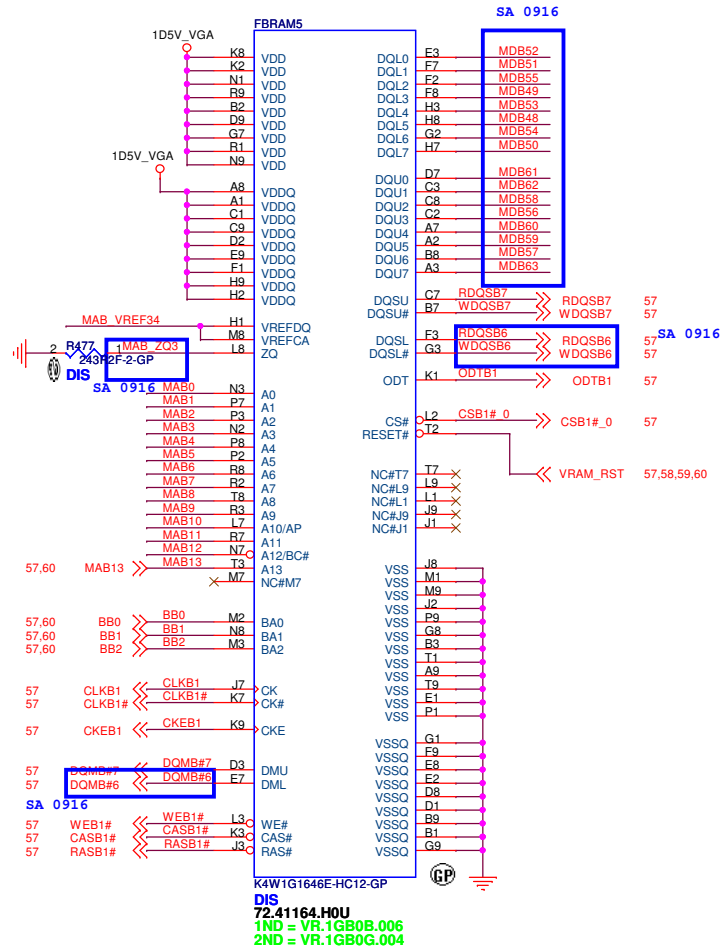
Madison ATI

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Title: **VRAM(3/4)**

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# DDR3

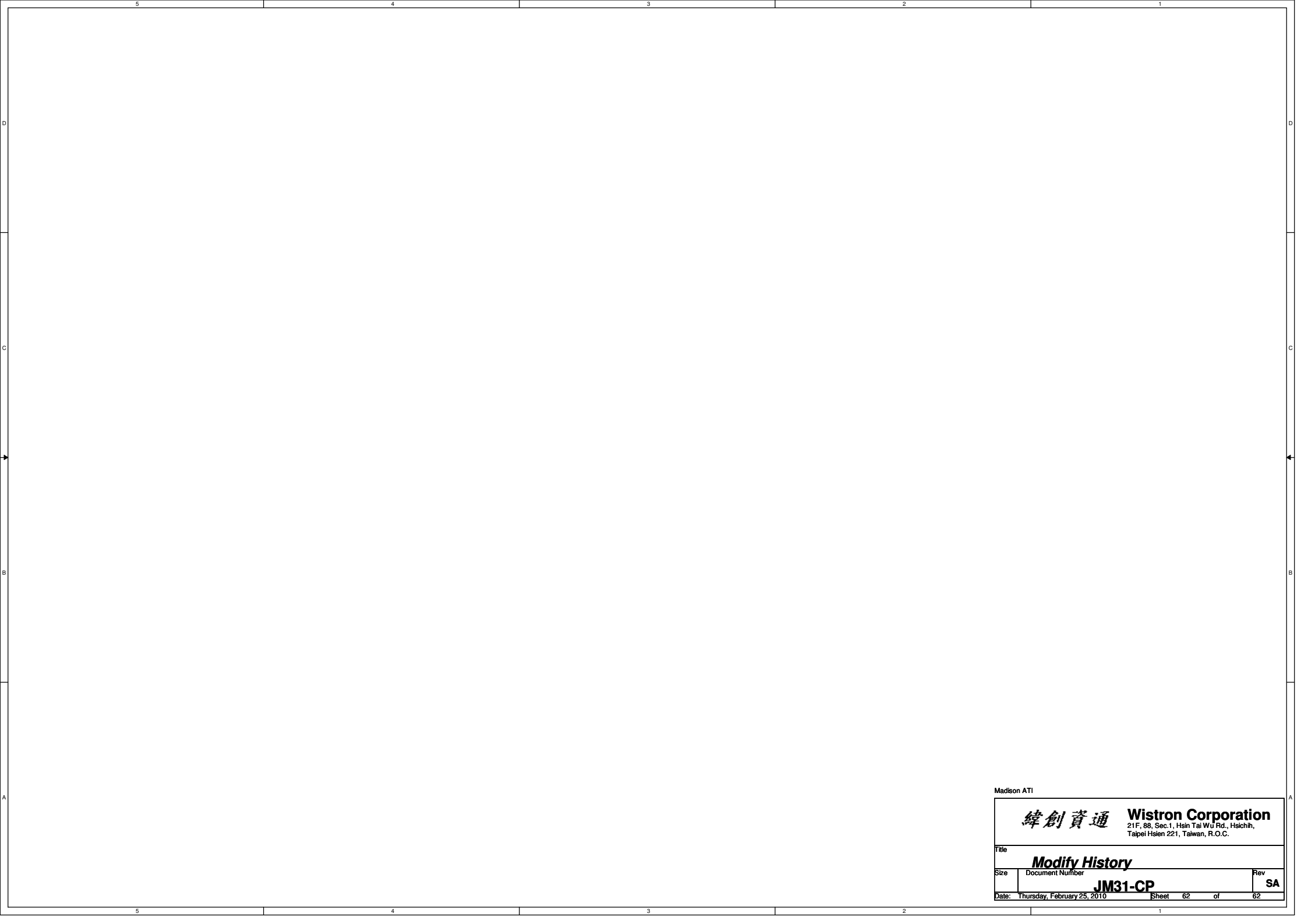


- 57.60 DQMB#[0..7] <<>
- 57.60 RDQSB#[0..7] <<>
- 57.60 WDQSB#[0..7] <<>
- 57.60 MAB#[0..12] <<
- 57.60 MDB#[0..63] <<>

**SAMSUNG: 72.41164.H0U (VR.1GB0B.006)**  
**HYNIX: 72.51G63.C0U (VR.1GB0G.004)**

Madison ATI

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<b>VRAM(4/4)</b>			
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Title		
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