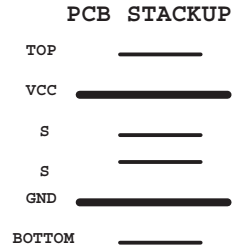
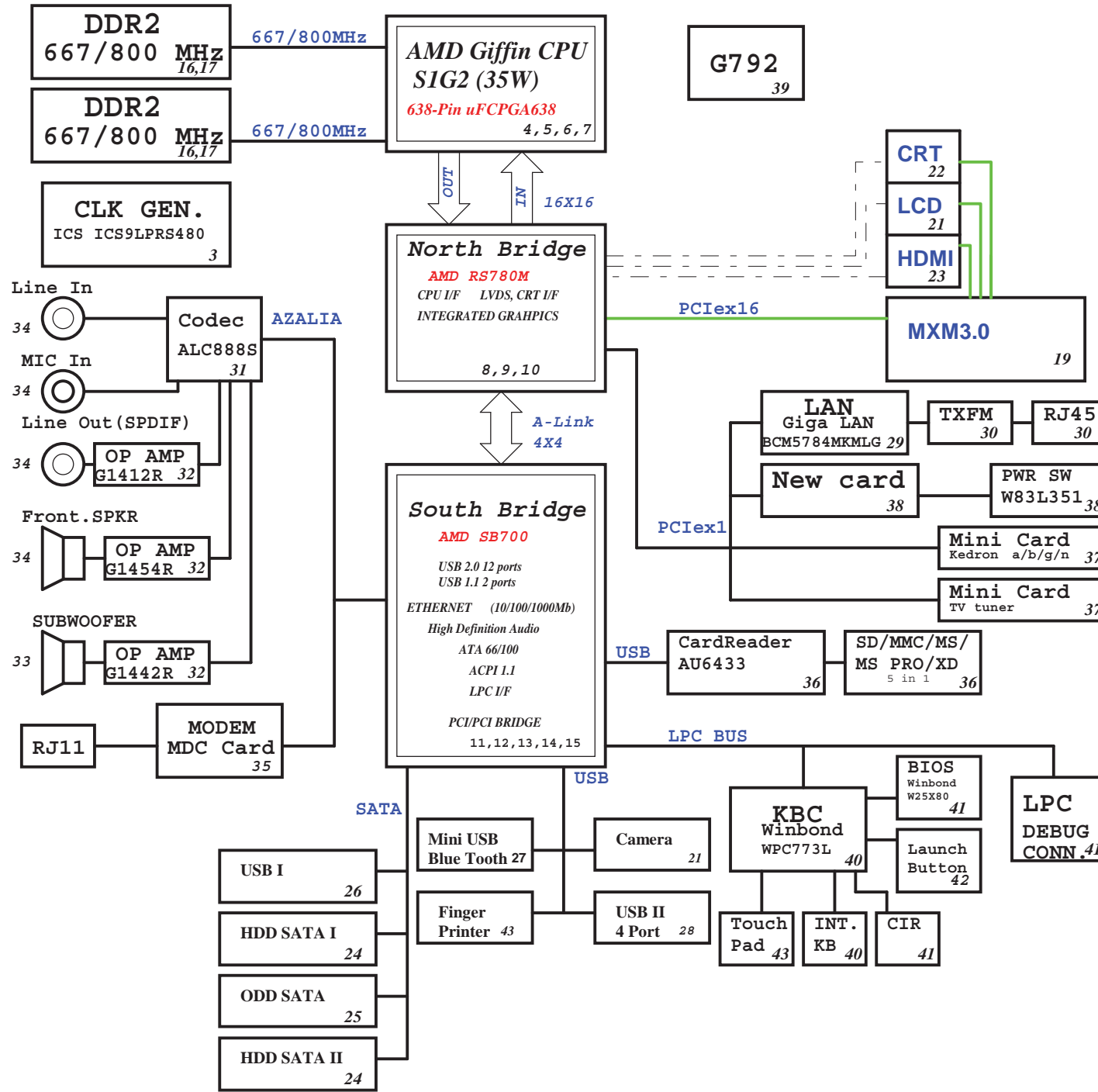
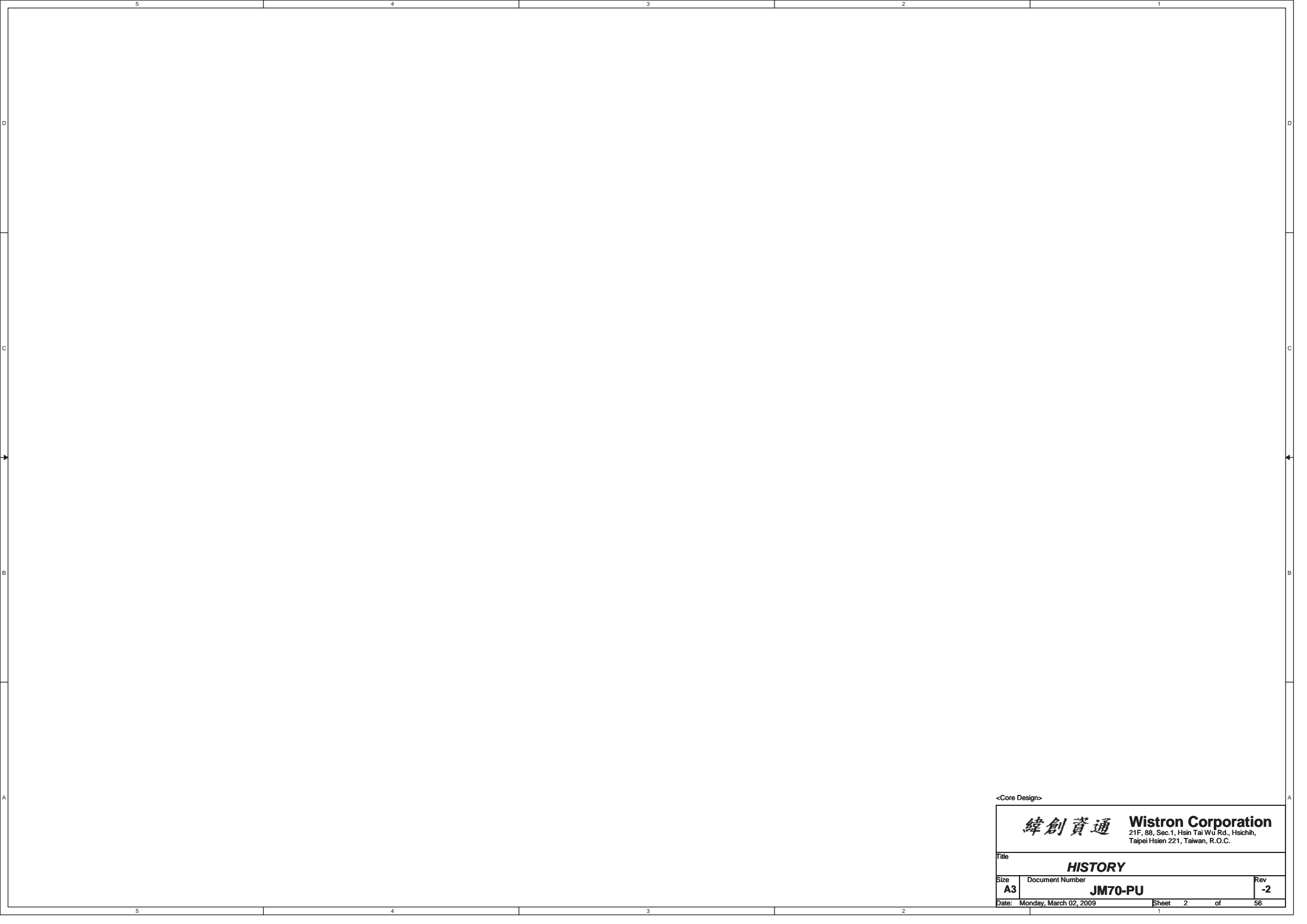


JM70-PU (AS 17") Block Diagram

Project code: 91.4CE01.001
 PCB P/N : 48.4CE01.0SC
 REVISION : 08255-SC



| SYSTEM DC/DC TPS51125 49 | |
|--------------------------|-----------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_S5 (7A) |
| | 3D3V_S5 (7A) |
| SYSTEM DC/DC TPS51124 50 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D1V_S0 (8A) |
| | 1D2V_S0 (5A) |
| SYSTEM DC/DC TPS51117 52 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D8V_S3 (10A) |
| RT9026PFP 51 | |
| 1D8V_S3 | DDR_VREF_S3 |
| | 0D9V_S3 (1A) |
| RT9166 51 | |
| 3D3V_S0 | 2D5V_S0 (300mA) |
| G957 51 | |
| 3D3V_S0 | 1D5V_S0 (1A) |
| G9161 (UMA) 51 | |
| 3D3V_S5 | 1D2V_S5 (400mA) |
| G9131 (DIS) 51 | |
| 3D3V_S5 | 1D2V_S5 (300mA) |
| CHARGER MAX8731A 53 | |
| INPUTS | OUTPUTS |
| DCBATOUT | CHG_PWR |
| | 1.8V 6.0A |
| | UP+5V |
| | 5V 100mA |
| CPU DC/DC ISL6265HR 48 | |
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE_S0_0 |
| | 0~1.55V 18A |
| | VCC_CORE_S0_1 |
| | 0~1.55V 18A |
| | VDDNB |
| | 0~1.55V 18A |



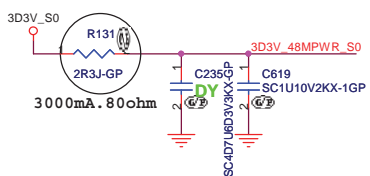
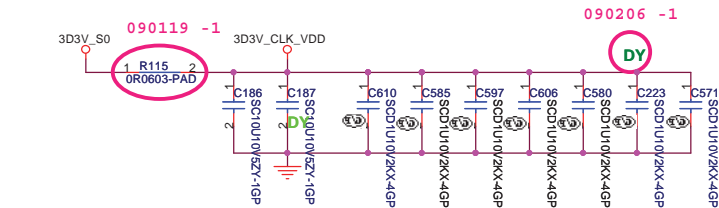
<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title **HISTORY**

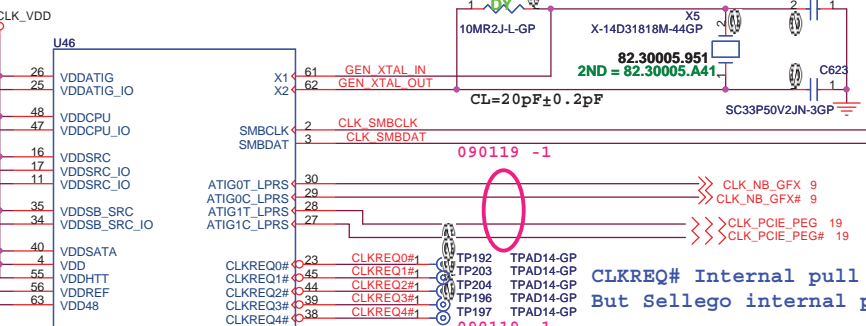
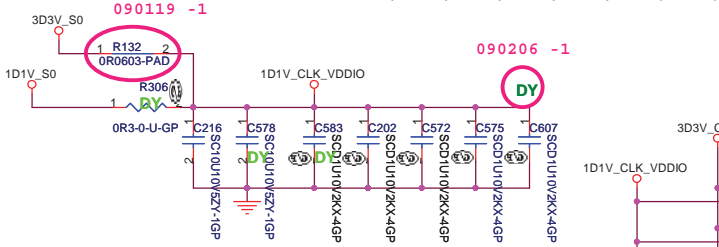
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|-----------|-----------------|-----------|
| Size | Document Number | Rev |
| A3 | JM70-PU | -2 |

Date: Monday, March 02, 2009 Sheet 2 of 56



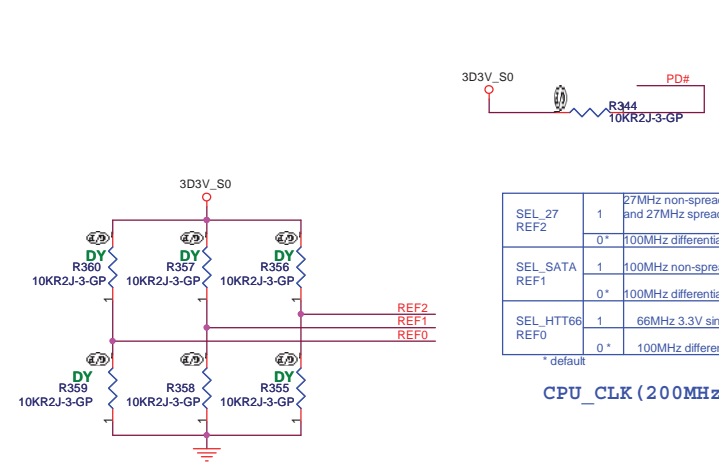
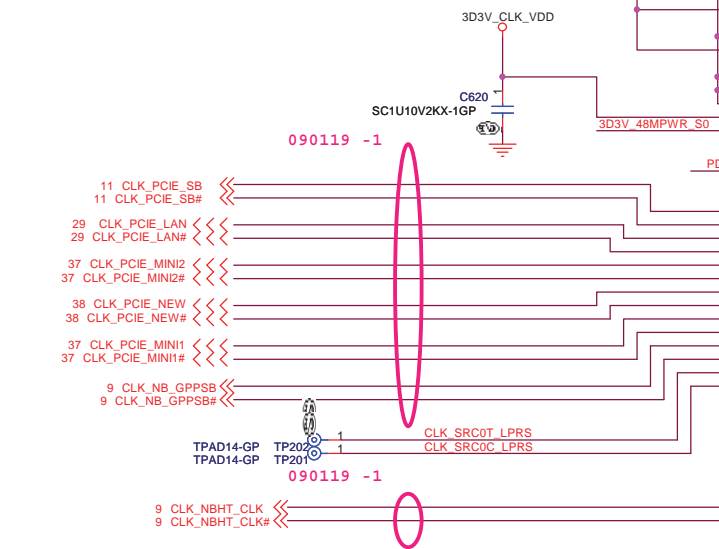
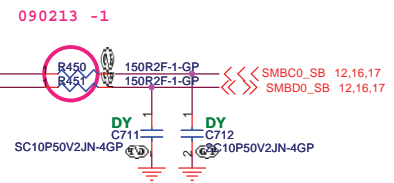
Due to PLL issue on current clock chip, the SBLink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



CLKREQ# Internal pull high But Sellego internal pull low

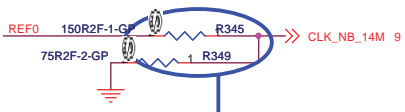
090210 as Larry's suggestion



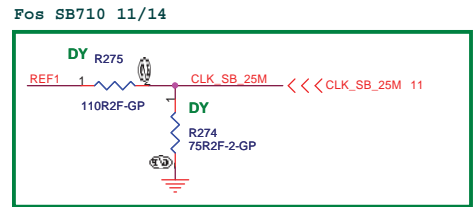
| | | |
|----------------|----|--|
| SEL_27 REF2 | 1 | 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6 |
| | 0* | 100MHz differential spreading SRC clock |
| SEL_SATA REF1 | 1 | 100MHz non-spreading differential SATA clock |
| | 0* | 100MHz differential spreading SRC clock |
| SEL_HTT66 REF0 | 1 | 66MHz 3.3V single ended HTT clock |
| | 0* | 100MHz differential HTT clock |

* default

CPU_CLK (200MHz)



OSC 14M NB
RS780M 1.1V 158R/90.9R



NB CLOCK INPUT TABLE

| NB CLOCKS | RS740 | RX780 | RS780 |
|--------------|--------------------|---------------|------------------------|
| HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF |
| HT_REFCLKN | NC | 100M DIFF | 100M DIFF |
| REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V) |
| REFCLK_N | NC | NC | vref |
| GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)* |
| GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT |
| GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF |

* RS780 can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

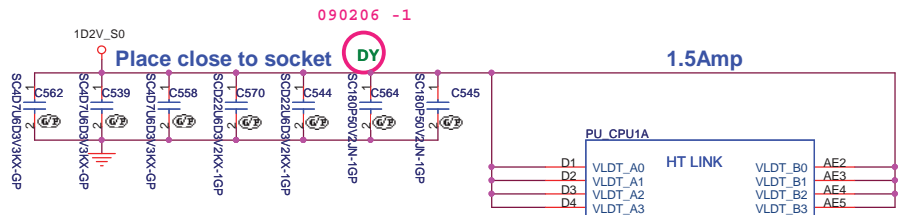
<Core Design>

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Title: **CLKGEN_ICS9LPRS480**

Size: **A3** Document Number: **JM70-PU** Rev: **-2**

Date: **Friday, March 06, 2009** Sheet **3** of **56**



| State | Specification | Notes | ZM200100M2303 |
|----------|-----------------|-------|---------------|
| S0.C0.Px | Tcase Max | 3 | TBD |
| | NB COF | 1 | 400 MHz |
| | VID_VDDNB Min | 2 | 0.950 V |
| | VID_VDDNB Max | 2 | 0.950 V |
| | Startup P-state | | S0.C0.P7 |
| S0.C0.P0 | CPU COF | 1 | 2000 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P1 | CPU COF | 1 | 1800 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P2 | CPU COF | 1 | 1500 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P3 | CPU COF | 1 | 1300 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P4 | CPU COF | 1 | 1000 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P5 | CPU COF | 1 | 800 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P6 | CPU COF | 1 | 500 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P7 | CPU COF | 1 | 300 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |

- | | | | | | | |
|---------------------|----|--------------|---------------|-----|-------------------|---|
| 8 HT_NB_CPU_CAD_H0 | E3 | L0_CADIN_H0 | L0_CADOUT_H0 | AD1 | HT_CPU_NB_CAD_H0 | 8 |
| 8 HT_NB_CPU_CAD_L0 | E2 | L0_CADIN_L0 | L0_CADOUT_L0 | AC1 | HT_CPU_NB_CAD_L0 | 8 |
| 8 HT_NB_CPU_CAD_H1 | E1 | L0_CADIN_H1 | L0_CADOUT_H1 | AC2 | HT_CPU_NB_CAD_H1 | 8 |
| 8 HT_NB_CPU_CAD_L1 | F1 | L0_CADIN_L1 | L0_CADOUT_L1 | AC3 | HT_CPU_NB_CAD_L1 | 8 |
| 8 HT_NB_CPU_CAD_H2 | G3 | L0_CADIN_H2 | L0_CADOUT_H2 | AB1 | HT_CPU_NB_CAD_H2 | 8 |
| 8 HT_NB_CPU_CAD_L2 | G2 | L0_CADIN_L2 | L0_CADOUT_L2 | AA1 | HT_CPU_NB_CAD_L2 | 8 |
| 8 HT_NB_CPU_CAD_H3 | G1 | L0_CADIN_H3 | L0_CADOUT_H3 | AA2 | HT_CPU_NB_CAD_H3 | 8 |
| 8 HT_NB_CPU_CAD_L3 | H1 | L0_CADIN_L3 | L0_CADOUT_L3 | AA3 | HT_CPU_NB_CAD_L3 | 8 |
| 8 HT_NB_CPU_CAD_H4 | J1 | L0_CADIN_H4 | L0_CADOUT_H4 | W2 | HT_CPU_NB_CAD_H4 | 8 |
| 8 HT_NB_CPU_CAD_L4 | K1 | L0_CADIN_L4 | L0_CADOUT_L4 | W3 | HT_CPU_NB_CAD_L4 | 8 |
| 8 HT_NB_CPU_CAD_H5 | L3 | L0_CADIN_H5 | L0_CADOUT_H5 | V1 | HT_CPU_NB_CAD_H5 | 8 |
| 8 HT_NB_CPU_CAD_L5 | L2 | L0_CADIN_L5 | L0_CADOUT_L5 | U1 | HT_CPU_NB_CAD_L5 | 8 |
| 8 HT_NB_CPU_CAD_H6 | L1 | L0_CADIN_H6 | L0_CADOUT_H6 | U2 | HT_CPU_NB_CAD_H6 | 8 |
| 8 HT_NB_CPU_CAD_L6 | M1 | L0_CADIN_L6 | L0_CADOUT_L6 | U3 | HT_CPU_NB_CAD_L6 | 8 |
| 8 HT_NB_CPU_CAD_H7 | N3 | L0_CADIN_H7 | L0_CADOUT_H7 | T1 | HT_CPU_NB_CAD_H7 | 8 |
| 8 HT_NB_CPU_CAD_L7 | N2 | L0_CADIN_L7 | L0_CADOUT_L7 | R1 | HT_CPU_NB_CAD_L7 | 8 |
| 8 HT_NB_CPU_CAD_H8 | E5 | L0_CADIN_H8 | L0_CADOUT_H8 | AD4 | HT_CPU_NB_CAD_H8 | 8 |
| 8 HT_NB_CPU_CAD_L8 | E6 | L0_CADIN_L8 | L0_CADOUT_L8 | AD3 | HT_CPU_NB_CAD_L8 | 8 |
| 8 HT_NB_CPU_CAD_H9 | F3 | L0_CADIN_H9 | L0_CADOUT_H9 | AD5 | HT_CPU_NB_CAD_H9 | 8 |
| 8 HT_NB_CPU_CAD_L9 | F4 | L0_CADIN_L9 | L0_CADOUT_L9 | AB4 | HT_CPU_NB_CAD_L9 | 8 |
| 8 HT_NB_CPU_CAD_H10 | G5 | L0_CADIN_H10 | L0_CADOUT_H10 | AB3 | HT_CPU_NB_CAD_H10 | 8 |
| 8 HT_NB_CPU_CAD_L10 | H5 | L0_CADIN_L10 | L0_CADOUT_L10 | AB5 | HT_CPU_NB_CAD_L10 | 8 |
| 8 HT_NB_CPU_CAD_H11 | H3 | L0_CADIN_H11 | L0_CADOUT_H11 | AA5 | HT_CPU_NB_CAD_H11 | 8 |
| 8 HT_NB_CPU_CAD_L11 | H4 | L0_CADIN_L11 | L0_CADOUT_L11 | W5 | HT_CPU_NB_CAD_L11 | 8 |
| 8 HT_NB_CPU_CAD_H12 | K3 | L0_CADIN_H12 | L0_CADOUT_H12 | V5 | HT_CPU_NB_CAD_H12 | 8 |
| 8 HT_NB_CPU_CAD_L12 | K4 | L0_CADIN_L12 | L0_CADOUT_L12 | V4 | HT_CPU_NB_CAD_L12 | 8 |
| 8 HT_NB_CPU_CAD_H13 | L5 | L0_CADIN_H13 | L0_CADOUT_H13 | V3 | HT_CPU_NB_CAD_H13 | 8 |
| 8 HT_NB_CPU_CAD_L13 | M3 | L0_CADIN_L13 | L0_CADOUT_L13 | V6 | HT_CPU_NB_CAD_L13 | 8 |
| 8 HT_NB_CPU_CAD_H14 | M5 | L0_CADIN_H14 | L0_CADOUT_H14 | U5 | HT_CPU_NB_CAD_H14 | 8 |
| 8 HT_NB_CPU_CAD_L14 | M4 | L0_CADIN_L14 | L0_CADOUT_L14 | T4 | HT_CPU_NB_CAD_L14 | 8 |
| 8 HT_NB_CPU_CAD_H15 | N5 | L0_CADIN_H15 | L0_CADOUT_H15 | T3 | HT_CPU_NB_CAD_H15 | 8 |
| 8 HT_NB_CPU_CAD_L15 | P5 | L0_CADIN_L15 | L0_CADOUT_L15 | T2 | HT_CPU_NB_CAD_L15 | 8 |
| 8 HT_NB_CPU_CLK_H0 | J3 | L0_CLKIN_H0 | L0_CLKOUT_H0 | Y1 | HT_CPU_NB_CLK_H0 | 8 |
| 8 HT_NB_CPU_CLK_L0 | J2 | L0_CLKIN_L0 | L0_CLKOUT_L0 | W1 | HT_CPU_NB_CLK_L0 | 8 |
| 8 HT_NB_CPU_CLK_H1 | J5 | L0_CLKIN_H1 | L0_CLKOUT_H1 | Y4 | HT_CPU_NB_CLK_H1 | 8 |
| 8 HT_NB_CPU_CLK_L1 | K5 | L0_CLKIN_L1 | L0_CLKOUT_L1 | Y3 | HT_CPU_NB_CLK_L1 | 8 |
| 8 HT_NB_CPU_CTL_H0 | N1 | L0_CTLIN_H0 | L0_CTLOUT_H0 | R2 | HT_CPU_NB_CTL_H0 | 8 |
| 8 HT_NB_CPU_CTL_L0 | P1 | L0_CTLIN_L0 | L0_CTLOUT_L0 | R3 | HT_CPU_NB_CTL_L0 | 8 |
| 8 HT_NB_CPU_CTL_H1 | P3 | L0_CTLIN_H1 | L0_CTLOUT_H1 | T5 | HT_CPU_NB_CTL_H1 | 8 |
| 8 HT_NB_CPU_CTL_L1 | P4 | L0_CTLIN_L1 | L0_CTLOUT_L1 | R5 | HT_CPU_NB_CTL_L1 | 8 |

SKT-CPU638P-GP-U2

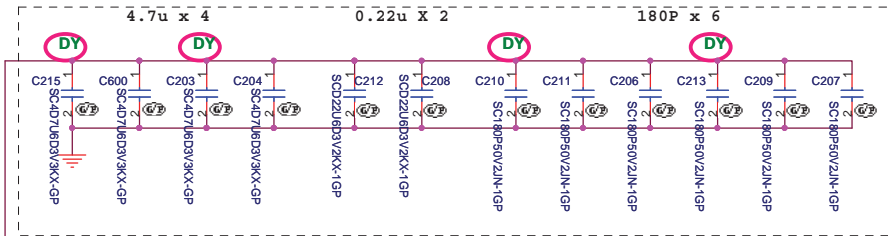
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090109 SC

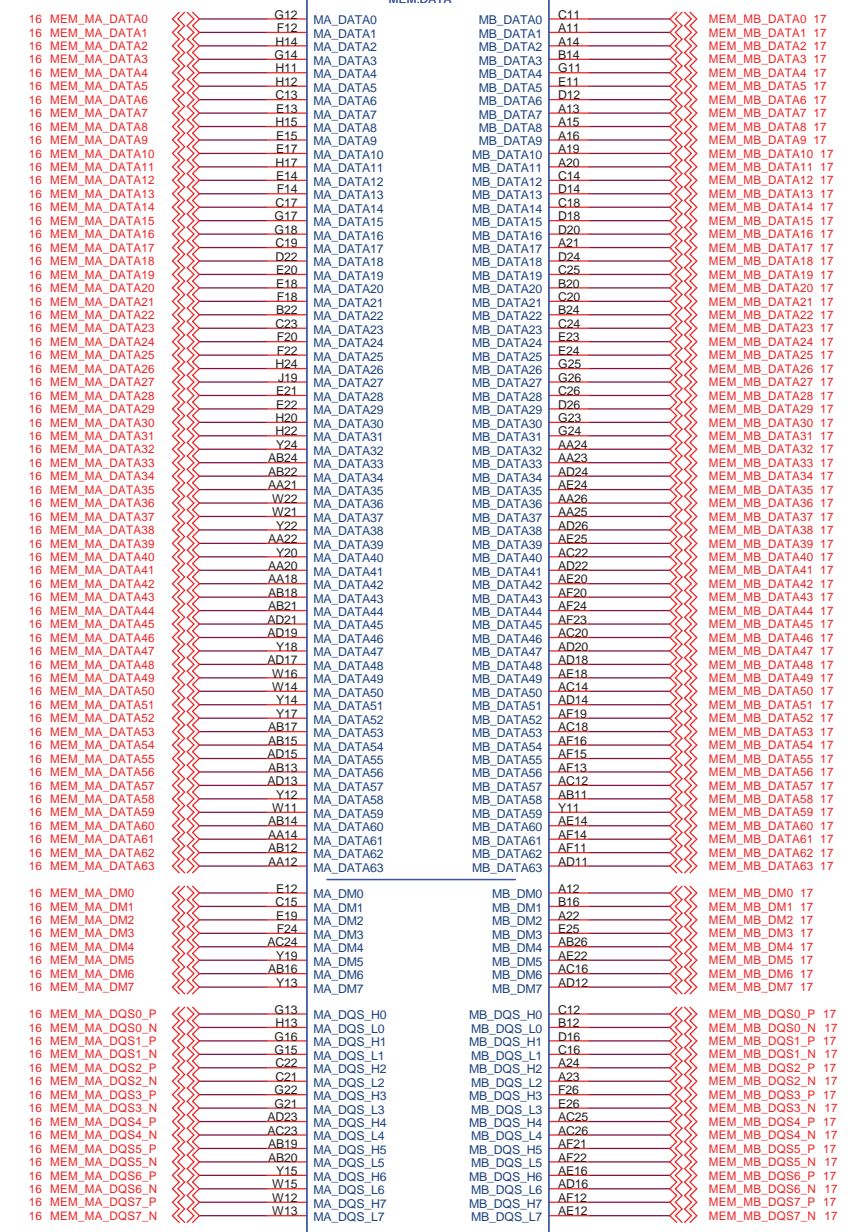
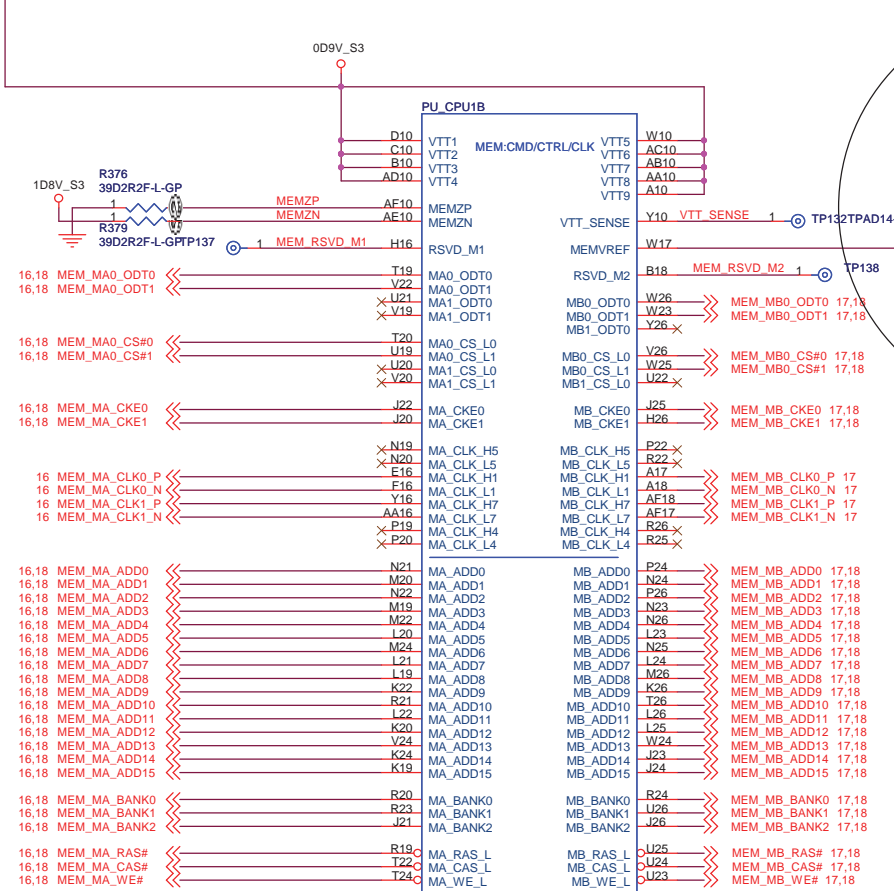
SKT-BGA638H176

090206 -1

Place near to CPU



CLOSE TO CPU



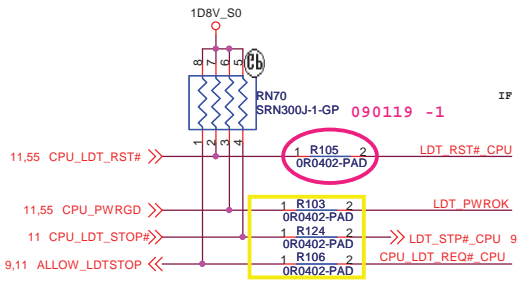
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62.10055.111
2ND = 62.10055.251

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Taipei Hsien 221, Taiwan, R.O.C.

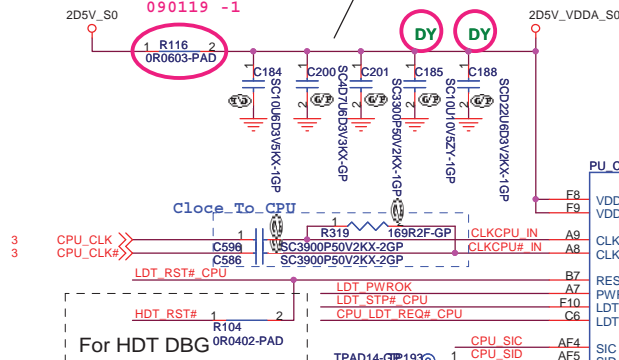
LYAOUT:ROUTE VDDA TRACE APPROX.
40 mils WIDE
(USE 2X25 mil TRACES TO EXIT BALL FIELD)
& 500 mils LONG.

The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN



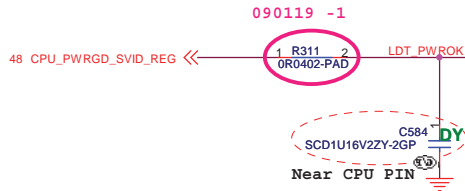
SB with 0402 PAD

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

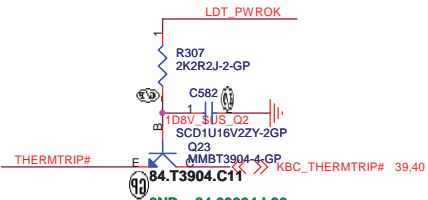
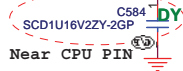


Close To CPU

For HDT DBG



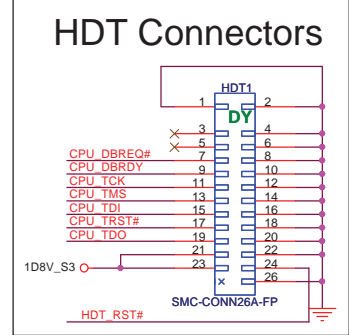
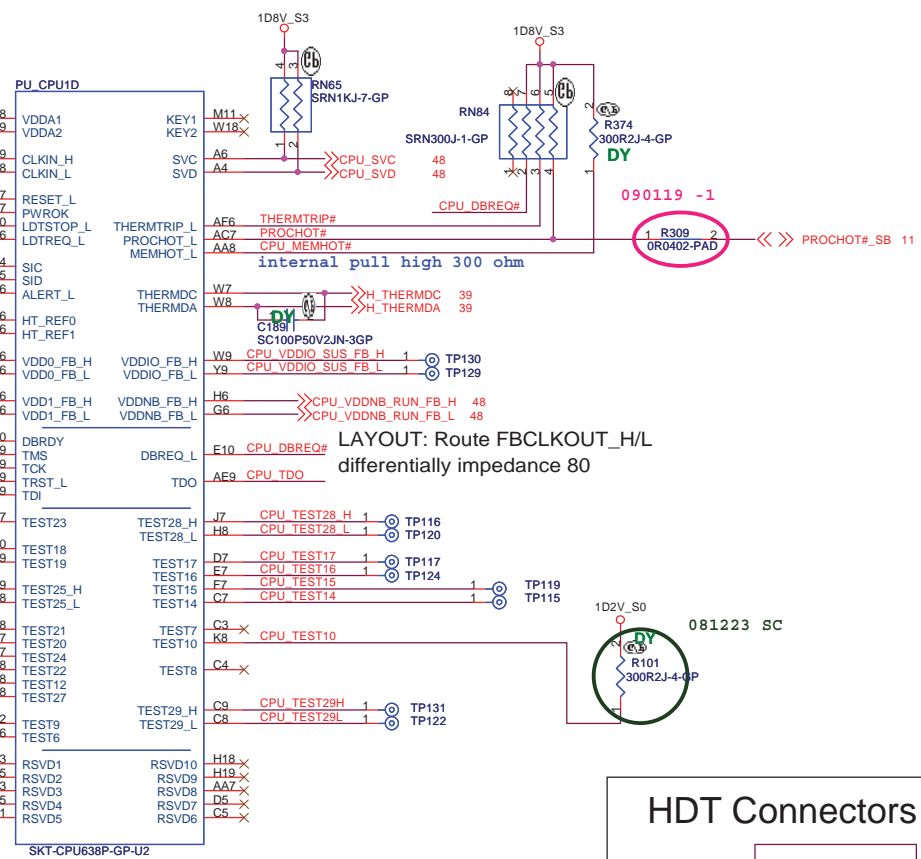
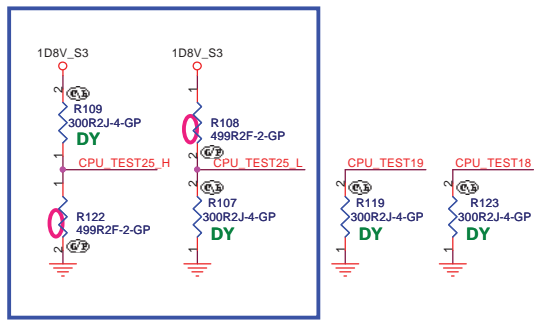
090119 -1



CPU exceeds to 125°C

081223 SC

090113 -1



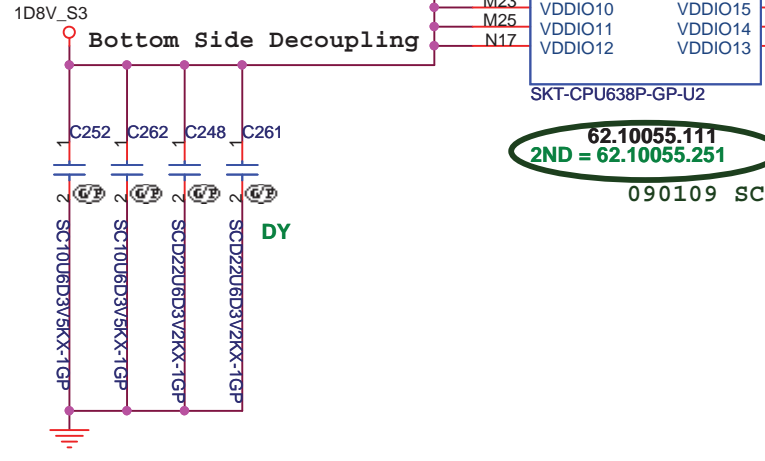
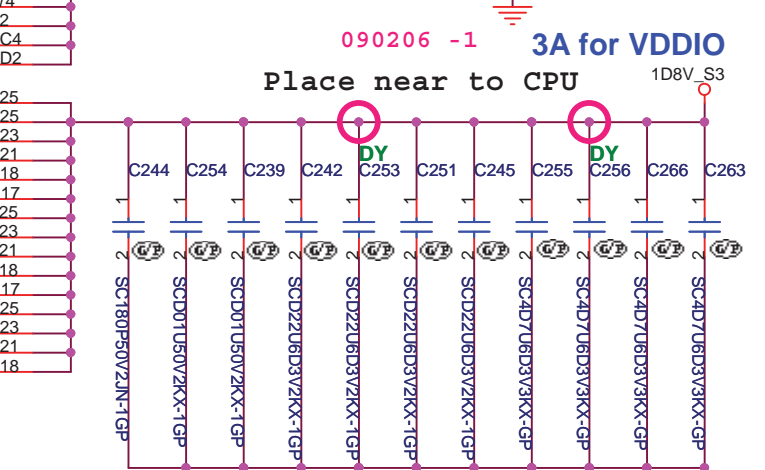
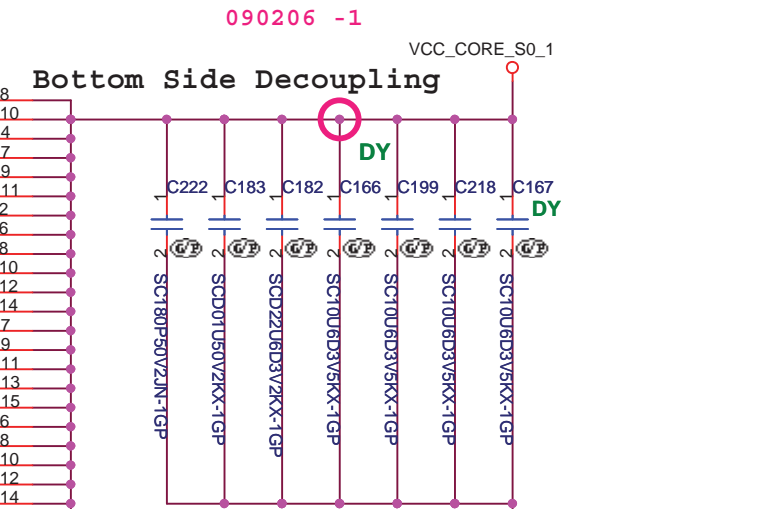
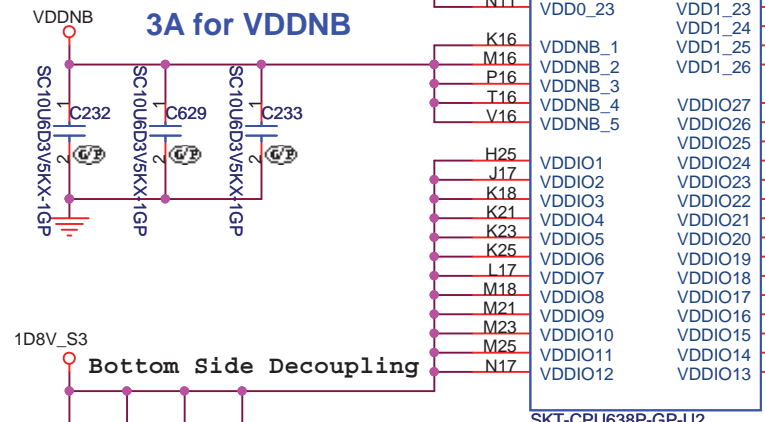
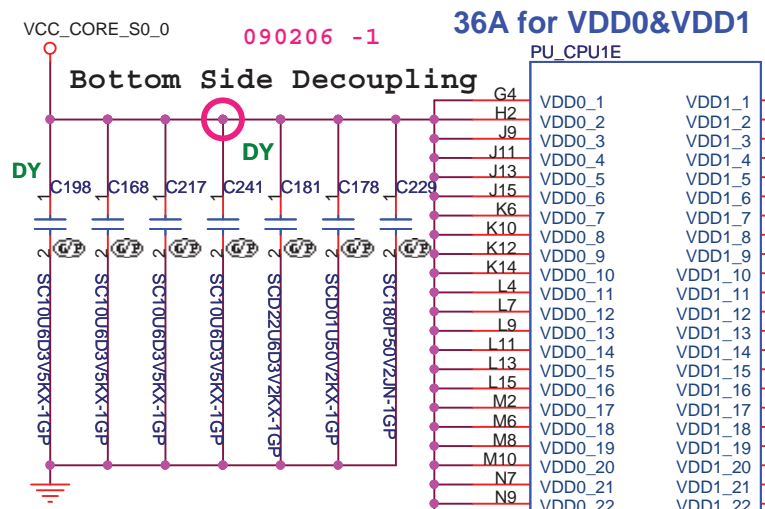
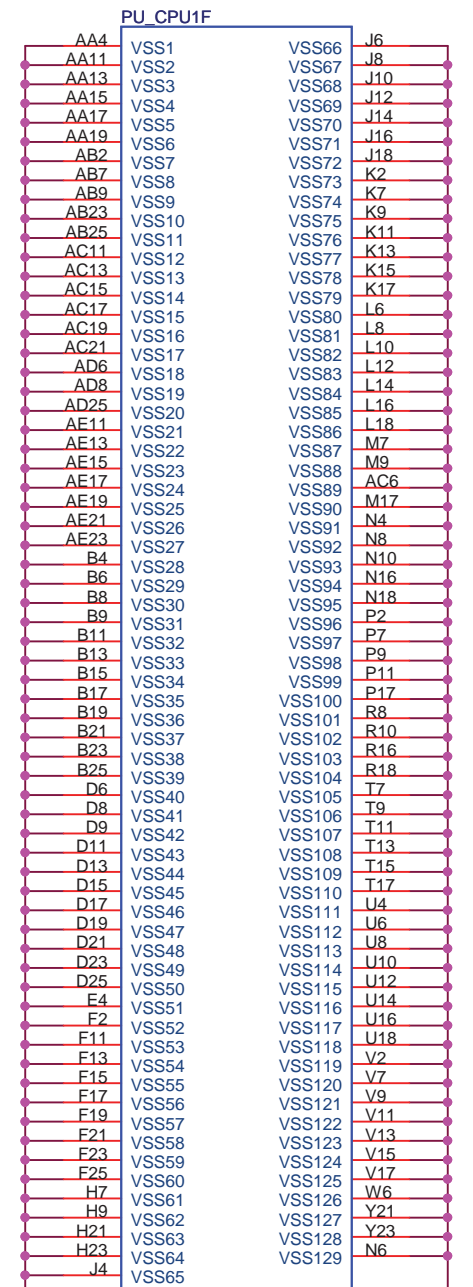
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Title CPU_Control&Debug (3/4)

Size A3 Document Number JM70-PU Rev -2


Date: Friday, March 06, 2009 Sheet 6 of 56

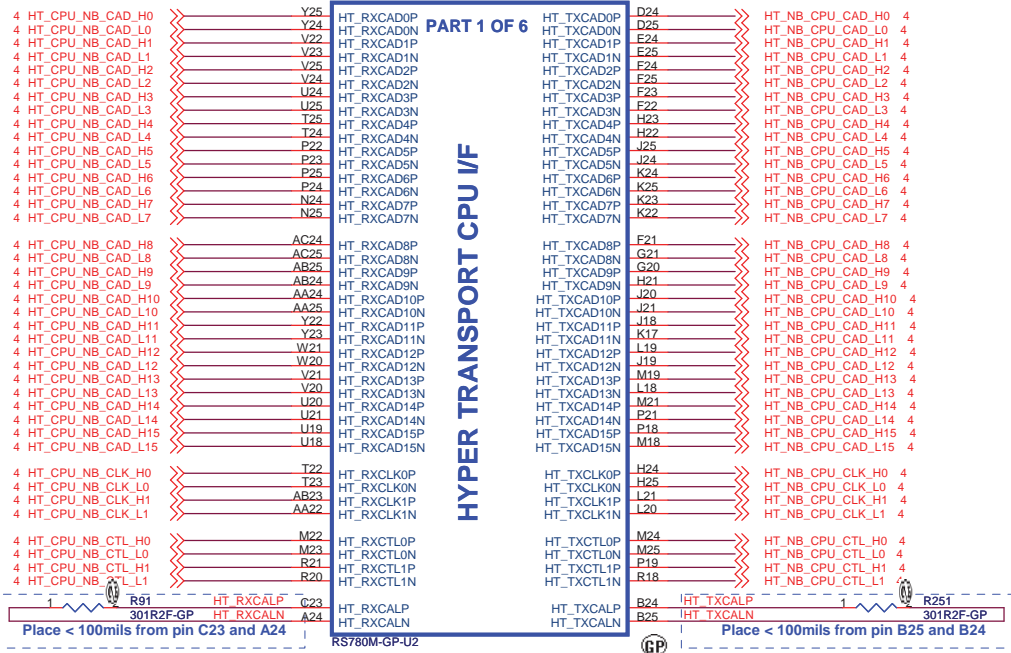


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090109 SC

62.10055.111
2ND = 62.10055.251
090109 SC

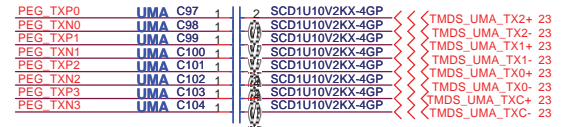
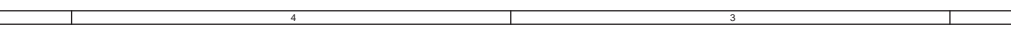
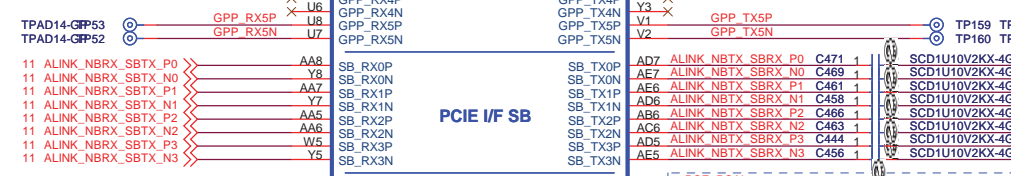
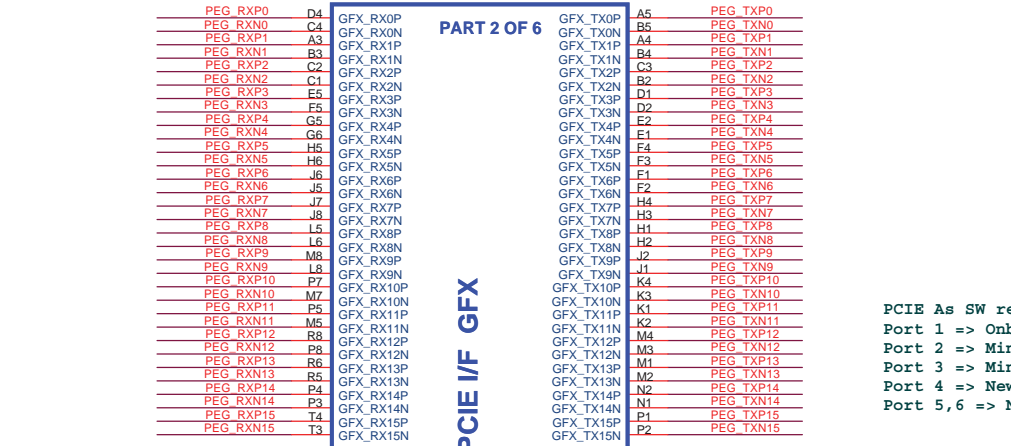
<Core Design>

| | | |
|---|------------------------|---------------|
|  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title | | |
| CPU_Power_(4/4) | | |
| Size | Document Number | Rev |
| A4 | JM70-PU | -2 |
| Date: | Monday, March 02, 2009 | Sheet 7 of 56 |



Place < 100mils from pin C23 and A24

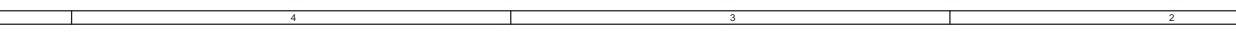
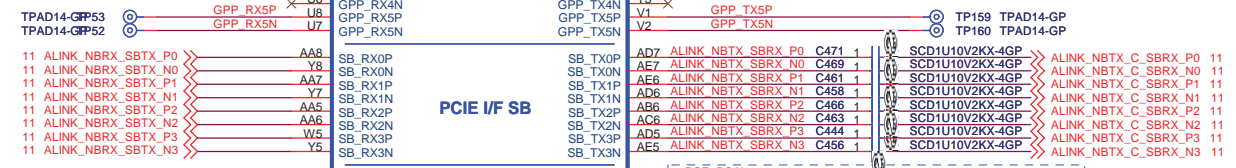
Place < 100mils from pin B25 and B24



RS780M Display Port Support (muxed on GFX)

| | |
|-----|------------------------------------|
| DP0 | GFX_TX0, TX1, TX2, TX3, AUX0, HPD0 |
| DP1 | GFX_TX4, TX5, TX6, TX7, AUX1, HPD1 |

PCIE As SW request 11/17
 Port 1 => Onboard LAN
 Port 2 => Mini Card WLAN
 Port 3 => Mini Card#2
 Port 4 => New Card
 Port 5, 6 => NC



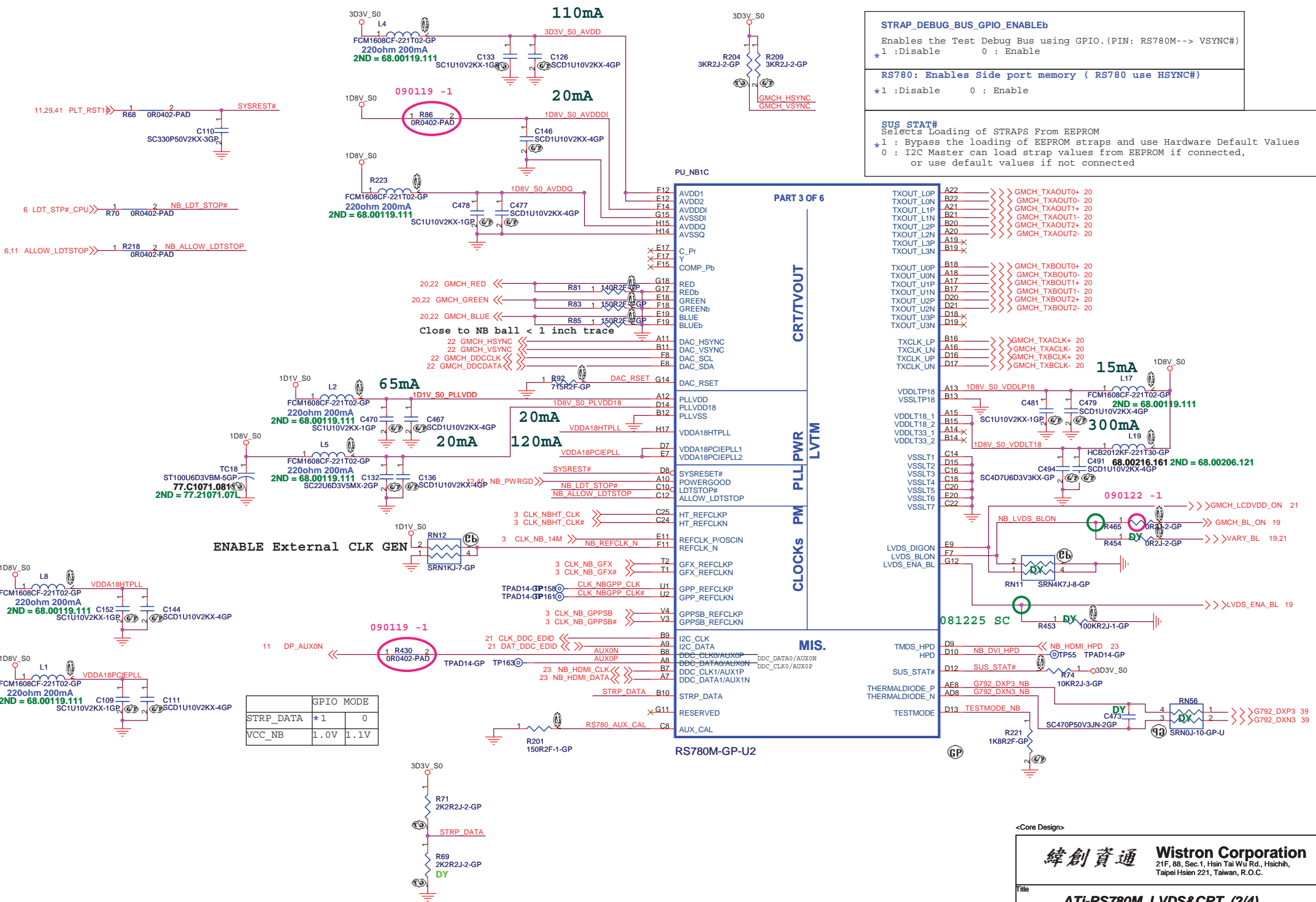
Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

ATI-RS780M_HT LINK&PCIE(1/3)

File: **JM70-PU**

Size: A3 Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet 8 of 56

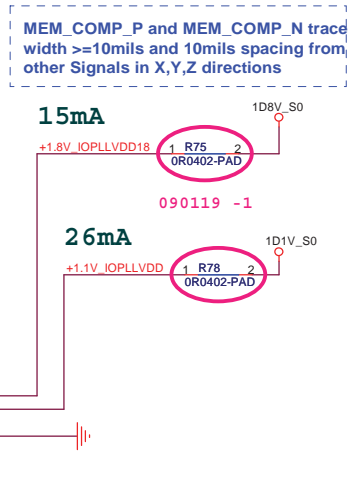
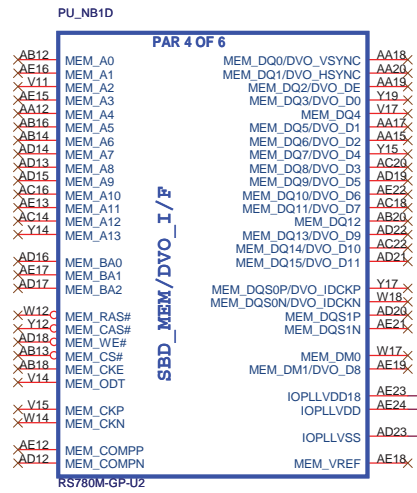
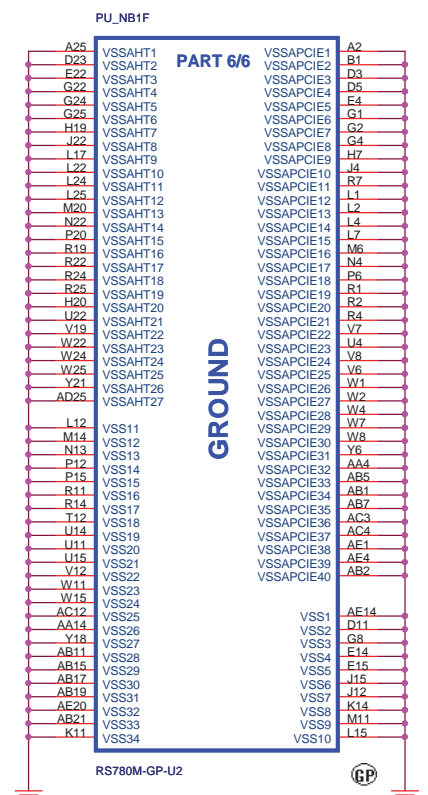
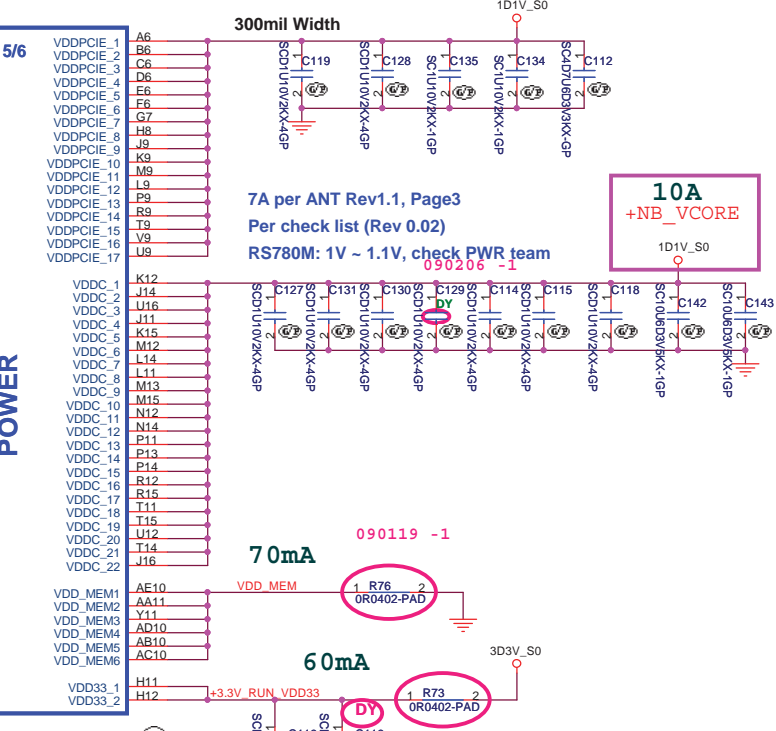
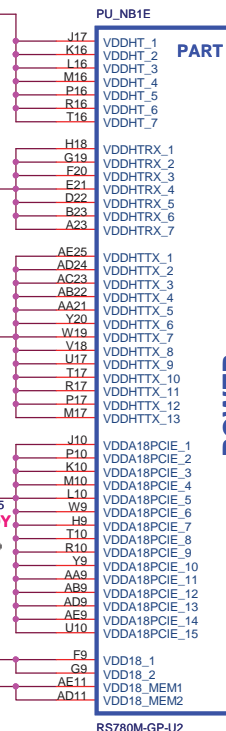
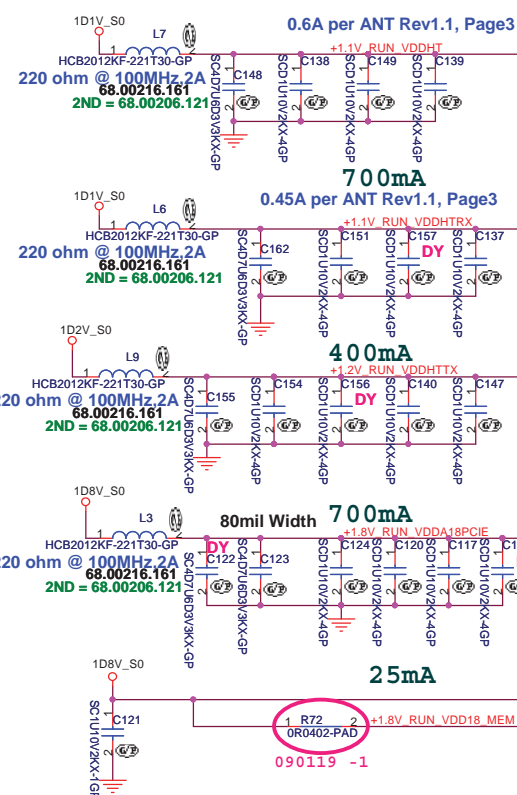


STRAP_DEBUG_BUS_GPIO_ENABLEB
 Enables the Test Debug Bus using GPIO. (PIN: RS780M--> VSYNC#)
 * 1 : Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
 * 1 : Disable 0 : Enable

SUS_STAT#
 Selects Loading of STRAPS from EEPROM
 * 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

| | GPIO MODE | |
|-----------|-----------|------|
| STRP_DATA | * 1 | 0 |
| VCC_NB | 1.0V | 1.1V |



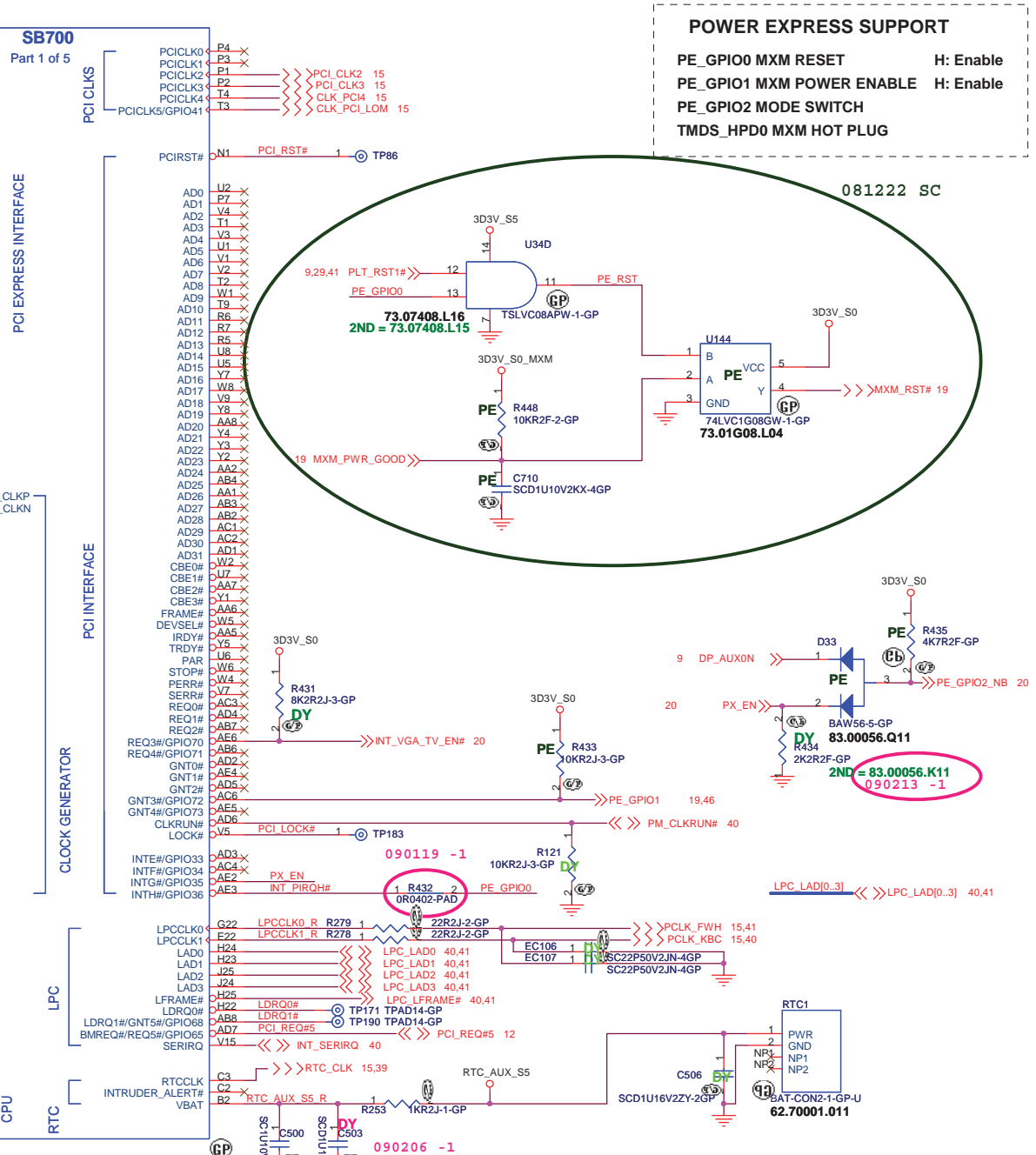
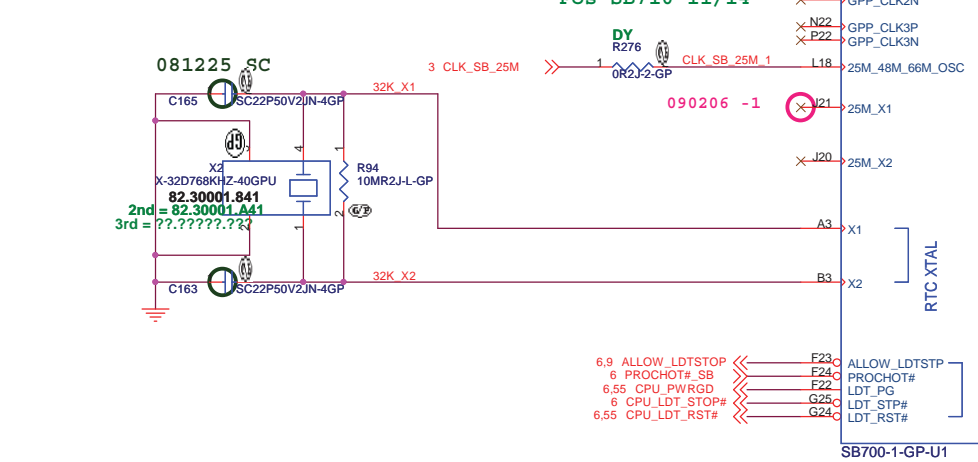
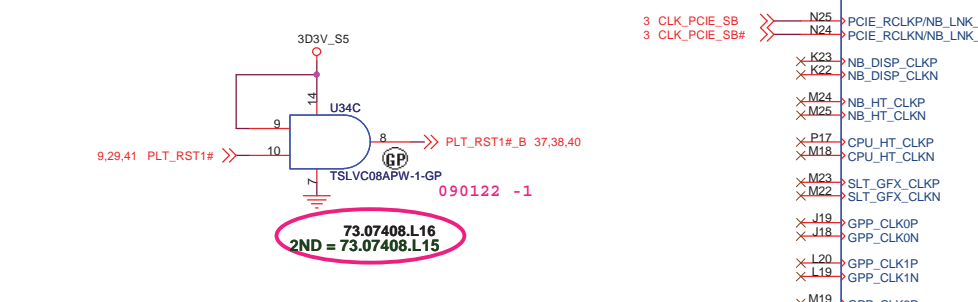
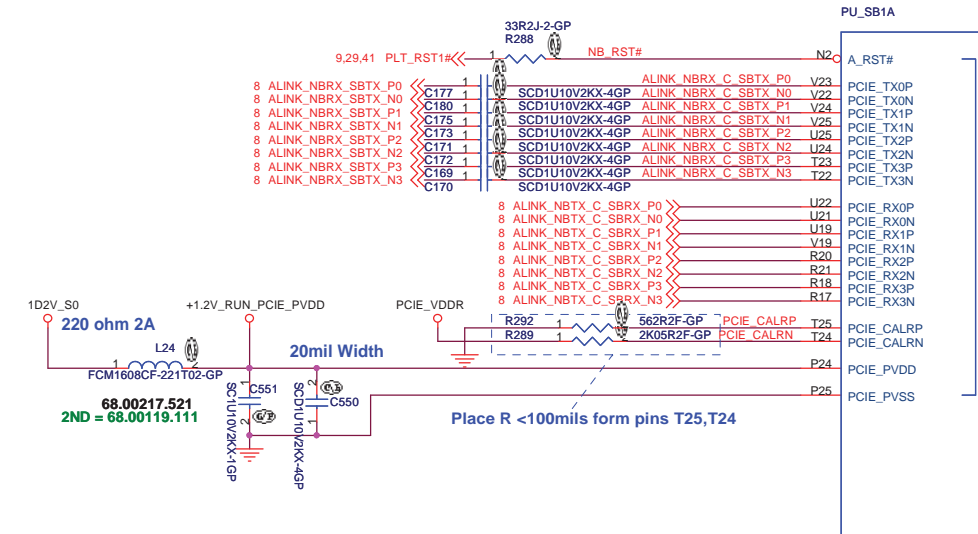
<Core Design>

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

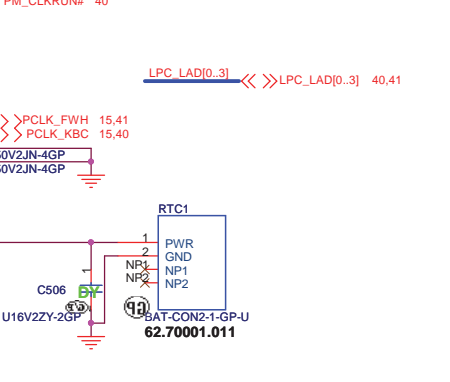
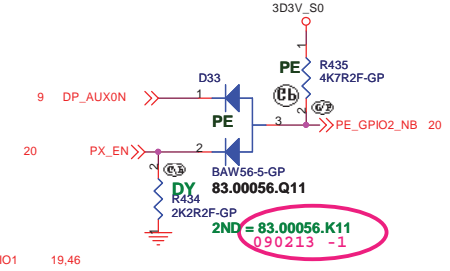
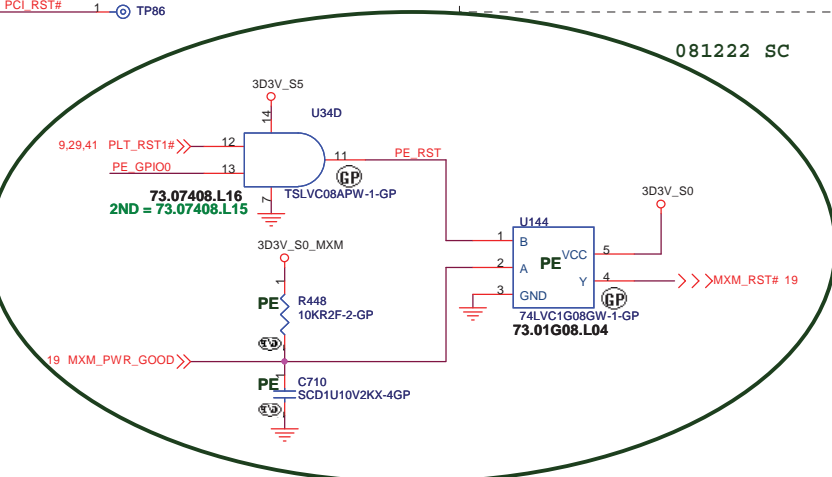
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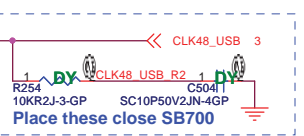
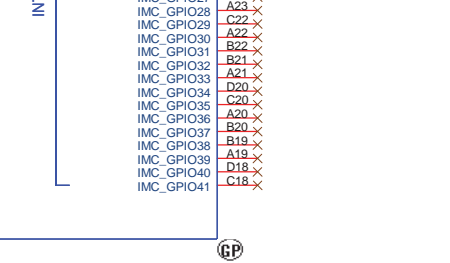
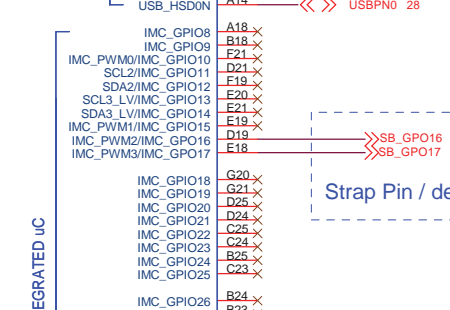
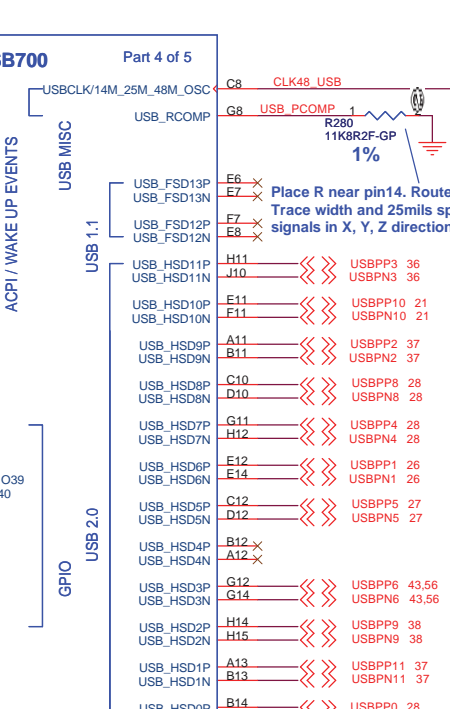
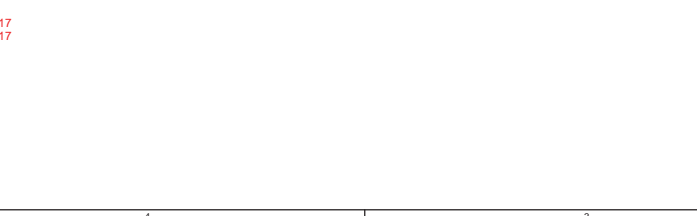
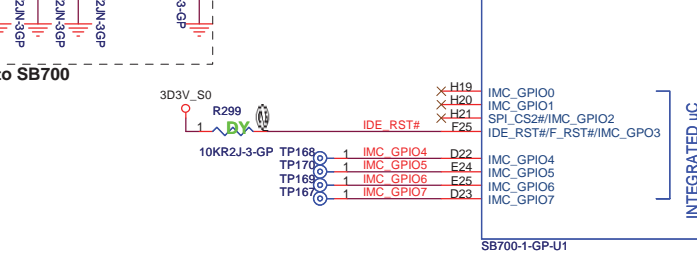
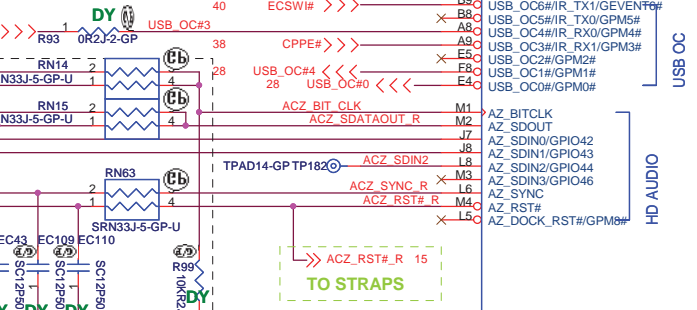
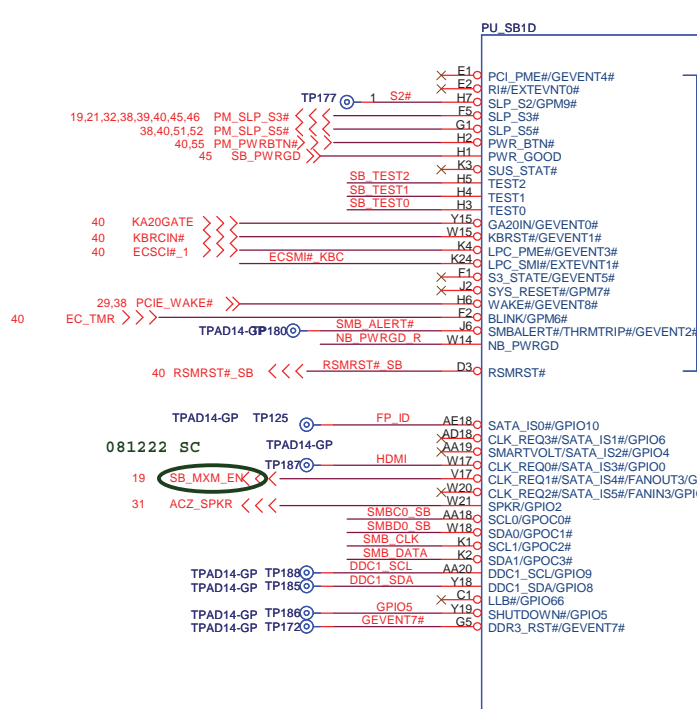
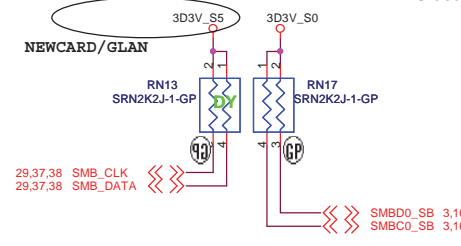
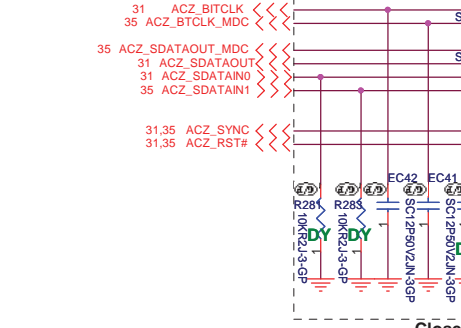
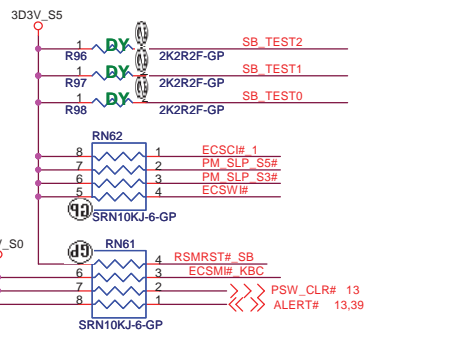
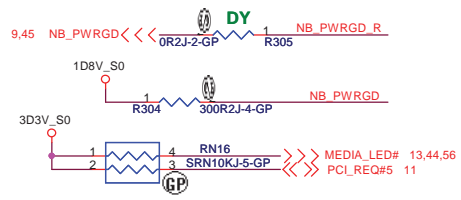
Size: A3 Document Number: **JM70-PU** Rev: -2

Date: Monday, March 02, 2009 Sheet 10 of 56



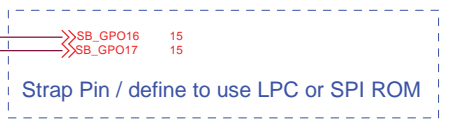
POWER EXPRESS SUPPORT
 PE_GPIO0 MXM RESET H: Enable
 PE_GPIO1 MXM POWER ENABLE H: Enable
 PE_GPIO2 MODE SWITCH
 TMD5_HPD0 MXM HOT PLUG





| USB | |
|------|-------------|
| Pair | Device |
| 11 | Card reader |
| 10 | WEBCAM |
| 9 | MINIC2 TV |
| 8 | USBCN1 |
| 7 | USBCN1 |
| 6 | ESATA |
| 5 | Bluetooth |
| 4 | NC |
| 3 | FingerPrint |
| 2 | NEW1 |
| 1 | MINIC1 |
| 0 | USB1 CN |

OC4#
OC0#



<Core Design>

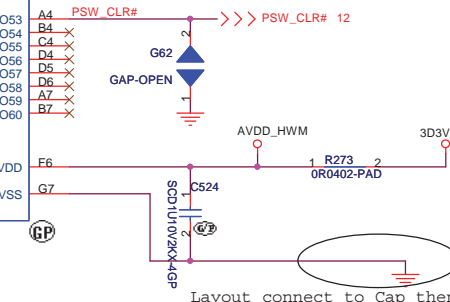
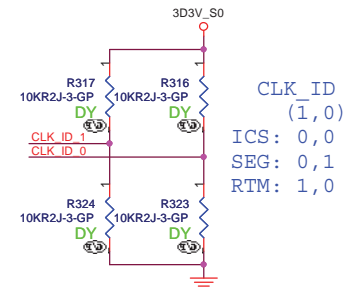
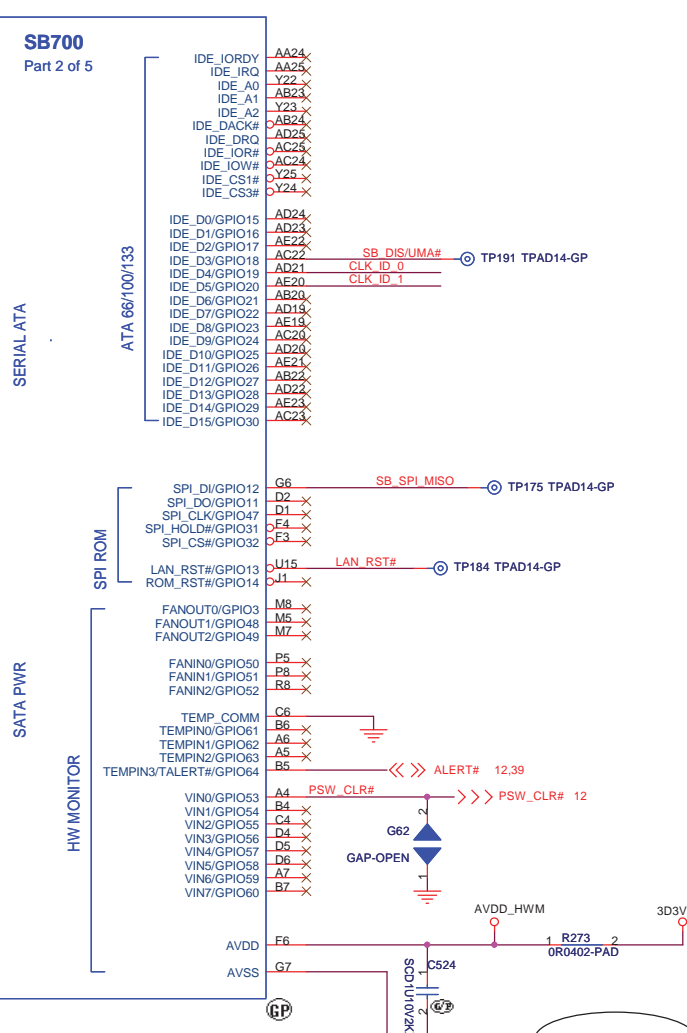
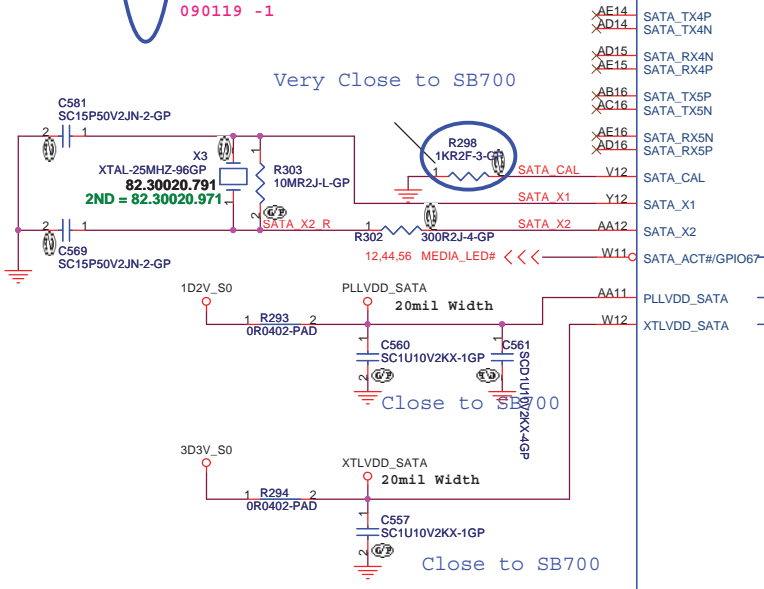
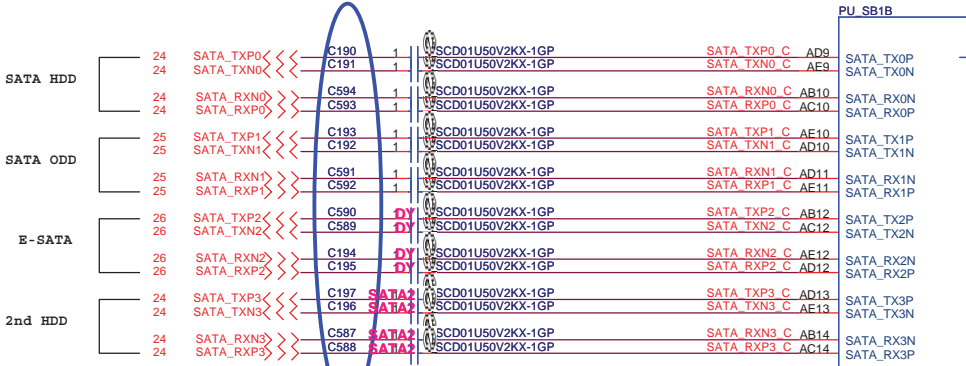
緯創資通 Wistron Corporation
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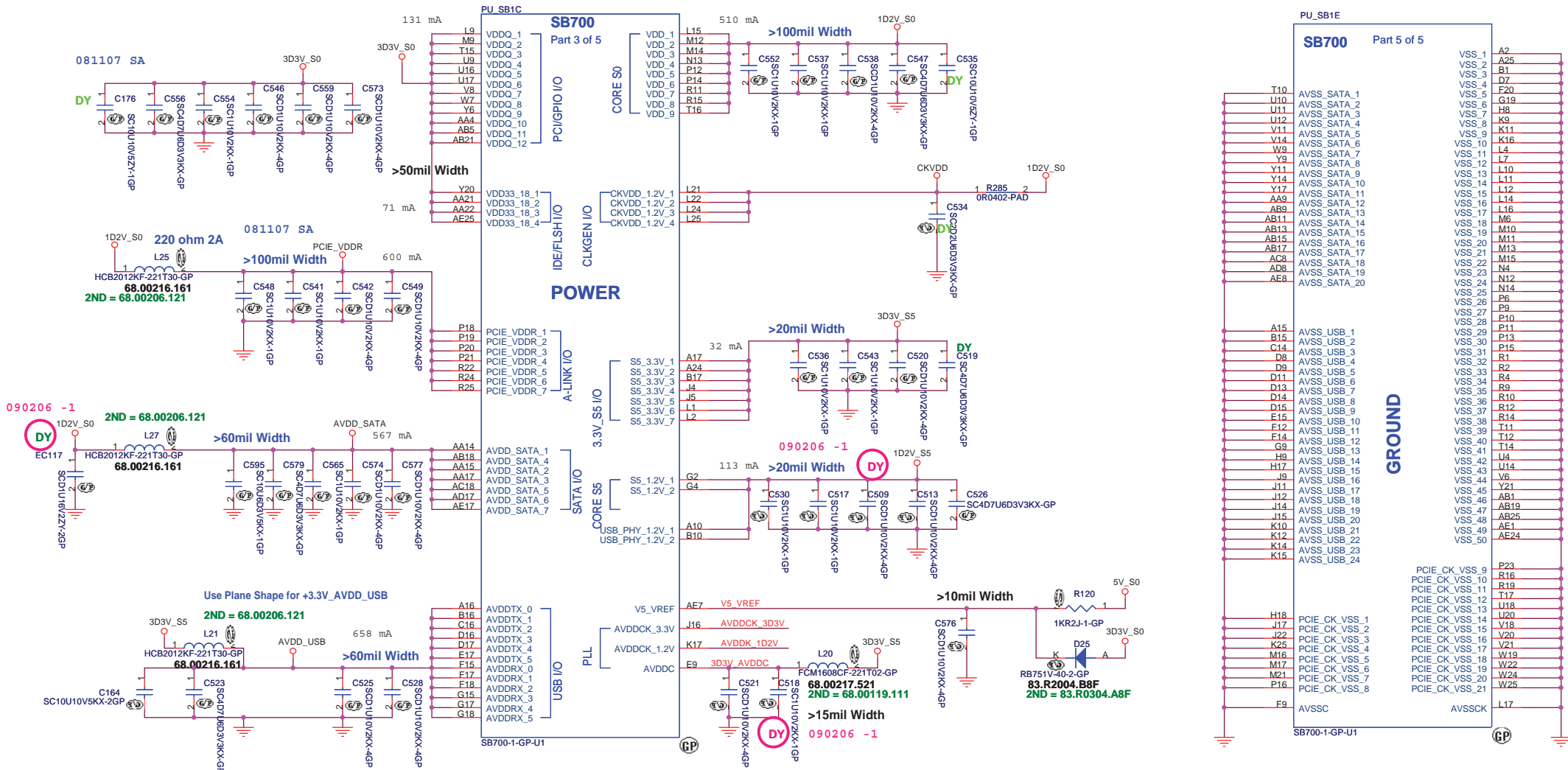
Title: **ATI-SB700_USB&GPIO_(2/5)**

Size: A3 Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet 12 of 56

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



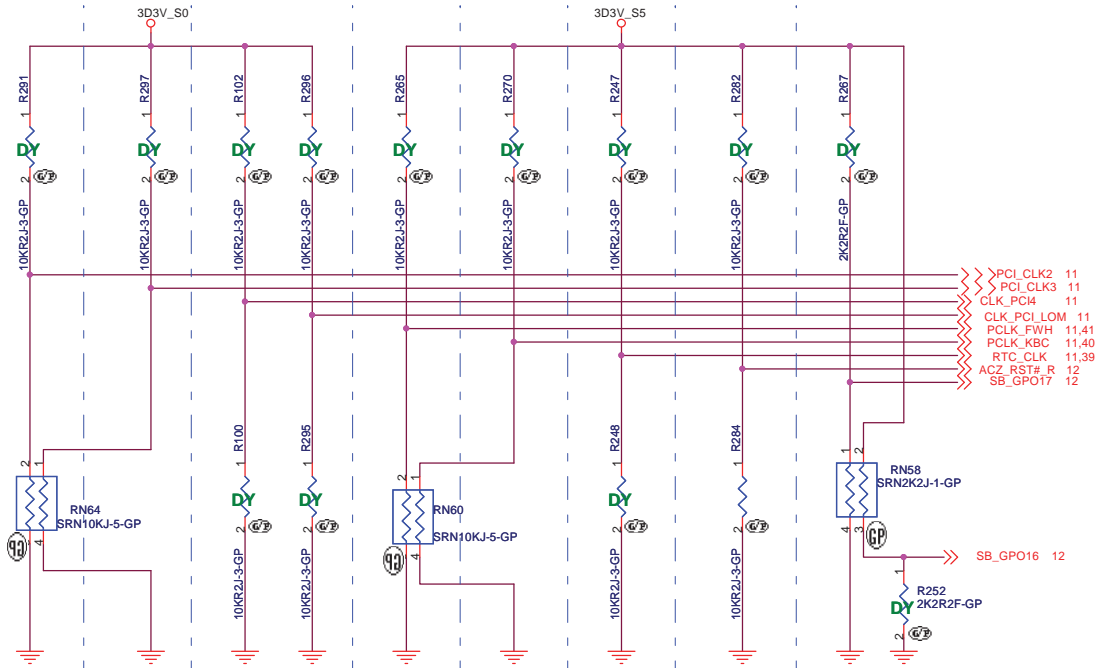


<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|--------------------------------------|------------------------|----------------|
| Title | | |
| ATI-SB700 POWER&GND (4/5) | | |
| Size | Document Number | Rev |
| A3 | JM70-PU | -2 |
| Date: | Monday, March 02, 2009 | Sheet 14 of 56 |

REQUIRED STRAPS REQUIRED SYSTEM STRAPS



DEBUG STRAPS

| | PCI_CLK2 | PCI_CLK3 | CLK_PCI_LOM CLK_PCI4 | PCLK_FWH | PCLK_KBC | RTCCLK | AZ_RST# | SB_GPO17, SB_GPO16 |
|------------------|---|--------------------------------|-------------------------|-------------------------|--|---|---------------------------------|--|
| PULL HIGH | WatchDog (NB_PWRGD) ENABLED | USE DEBUG STRAPS | RESERVED | IMC ENABLED | CLKGEN ENABLED (Use Internal) | INTERNAL RTC DEFAULT | ENABLE PCI ROM BOOT | ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT |
| PULL LOW | WatchDog (NB_PWRGD) DISABLED DEFAULT | IGNORE DEBUG STRAPS DEFAULT | | IMC DISABLED DEFAULT | CLKGEN DISABLED (Use External) DEFAULT | EXT. RTC (PD on X1, apply 32KHz to RTC_CLK) | DISABLE PCI ROM BOOT DEFAULT | L, H = LPC ROM L, L = FWH ROM |

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

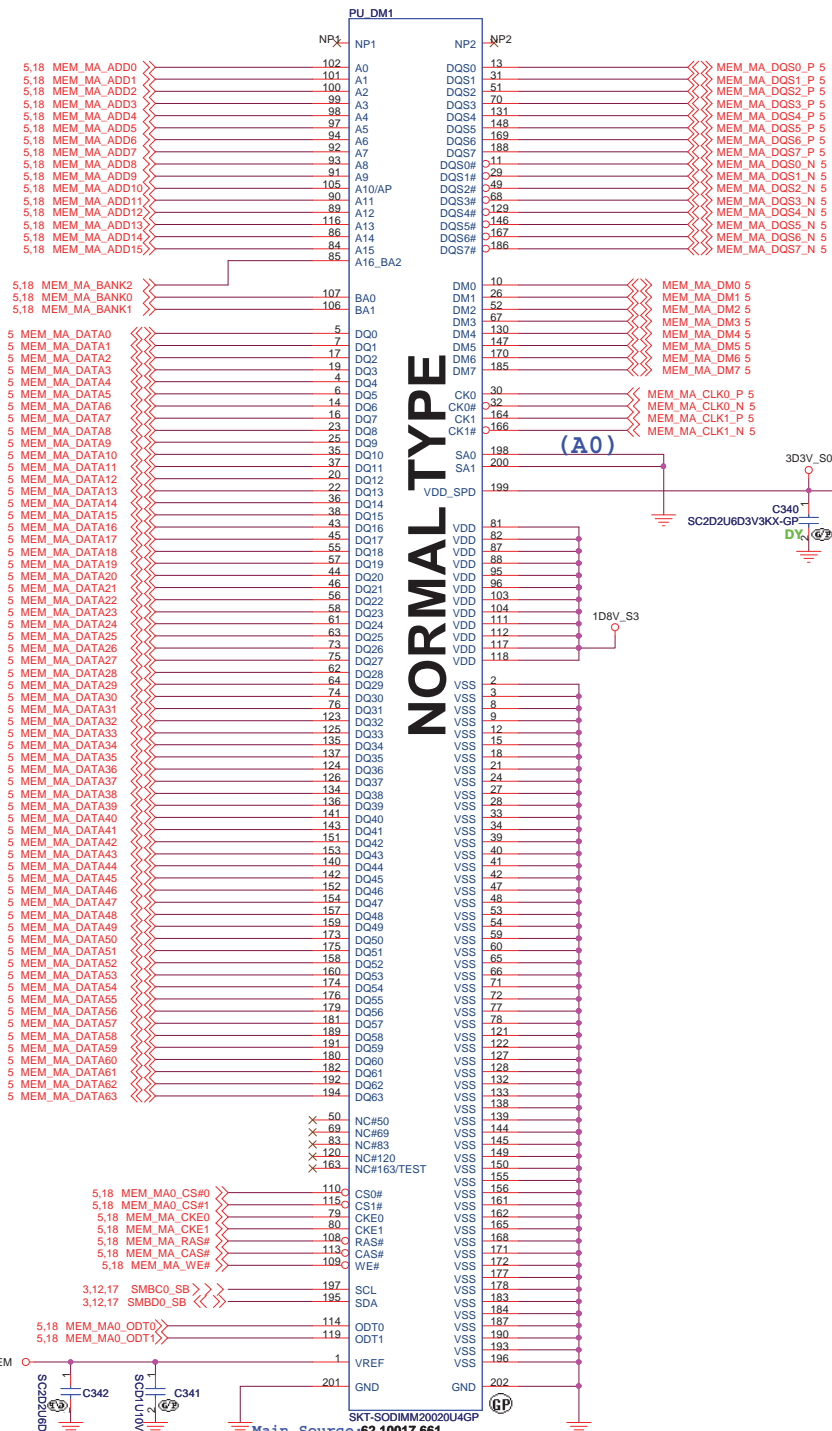
| | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 | PCI_AD30 PCI_AD29 |
|------------------|-----------------------------|--------------------------|----------------------------|--------------------------|--------------------------------------|-----------------------|----------------------|
| PULL HIGH | USE LONG RESET (DEFAULT) | USE PCI PLL (DEFAULT) | USE ACPI BCLK (DEFAULT) | USE IDE PLL (DEFAULT) | USE DEFAULT PCIE STRAPS (DEFAULT) | Reserved (DEFAULT) | Reserved |
| PULL LOW | USE SHORT RESET | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | Reserved | |

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Core Design>

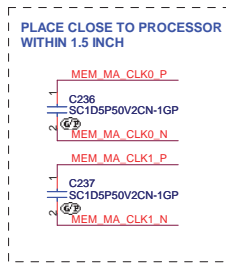
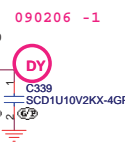
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|-----------------------------------|------------------|
| Title ATI-SB700 STRAPPING (5/5) | | |
| Size A3 | Document Number JM70-PU | Rev -2 |
| Date: Friday, March 06, 2009 | Sheet 15 of 56 | |

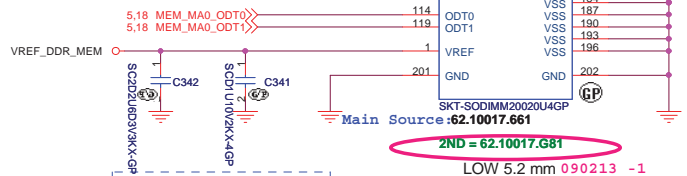
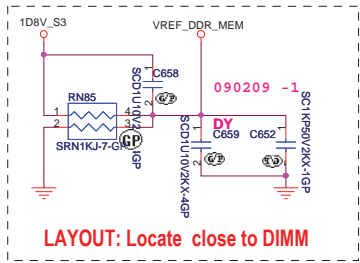


NORMAL TYPE

(A0)



DDR_VREF



<Core Design>

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Title: **DDR_SO-DIMM SKT_1**

Size: Custom Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet: 16 of 56

5,18 MEM_MB_ADD0 102 A0
 5,18 MEM_MB_ADD1 101 A1
 5,18 MEM_MB_ADD2 99 A2
 5,18 MEM_MB_ADD3 98 A3
 5,18 MEM_MB_ADD4 97 A4
 5,18 MEM_MB_ADD5 96 A5
 5,18 MEM_MB_ADD6 95 A6
 5,18 MEM_MB_ADD7 94 A7
 5,18 MEM_MB_ADD8 93 A8
 5,18 MEM_MB_ADD9 91 A9
 5,18 MEM_MB_ADD10 90 A10/AP
 5,18 MEM_MB_ADD11 89 A11
 5,18 MEM_MB_ADD12 88 A12
 5,18 MEM_MB_ADD13 86 A13
 5,18 MEM_MB_ADD14 84 A14
 5,18 MEM_MB_ADD15 85 A15
 5,18 MEM_MB_BANK2 107 A16/BA2
 5,18 MEM_MB_BANK0 106 BA0
 5,18 MEM_MB_BANK1 106 BA1

5 MEM_MB_DATA0 7 DO0
 5 MEM_MB_DATA1 17 DO1
 5 MEM_MB_DATA2 19 DO2
 5 MEM_MB_DATA3 4 DO3
 5 MEM_MB_DATA4 4 DO4
 5 MEM_MB_DATA5 6 DO5
 5 MEM_MB_DATA6 14 DO6
 5 MEM_MB_DATA7 16 DO7
 5 MEM_MB_DATA8 23 DO8
 5 MEM_MB_DATA9 25 DO9
 5 MEM_MB_DATA10 35 DO10
 5 MEM_MB_DATA11 37 DO11
 5 MEM_MB_DATA12 30 DO12
 5 MEM_MB_DATA13 22 DO13
 5 MEM_MB_DATA14 36 DO14
 5 MEM_MB_DATA15 38 DO15
 5 MEM_MB_DATA16 43 DO16
 5 MEM_MB_DATA17 45 DO17
 5 MEM_MB_DATA18 55 DO18
 5 MEM_MB_DATA19 44 DO19
 5 MEM_MB_DATA20 44 DO20
 5 MEM_MB_DATA21 46 DO21
 5 MEM_MB_DATA22 58 DO22
 5 MEM_MB_DATA23 61 DO23
 5 MEM_MB_DATA24 58 DO24
 5 MEM_MB_DATA25 63 DO25
 5 MEM_MB_DATA26 73 DO26
 5 MEM_MB_DATA27 62 DO27
 5 MEM_MB_DATA28 75 DO28
 5 MEM_MB_DATA29 64 DO29
 5 MEM_MB_DATA30 74 DO30
 5 MEM_MB_DATA31 76 DO31
 5 MEM_MB_DATA32 123 DO32
 5 MEM_MB_DATA33 125 DO33
 5 MEM_MB_DATA34 135 DO34
 5 MEM_MB_DATA35 137 DO35
 5 MEM_MB_DATA36 124 DO36
 5 MEM_MB_DATA37 126 DO37
 5 MEM_MB_DATA38 134 DO38
 5 MEM_MB_DATA39 136 DO39
 5 MEM_MB_DATA40 141 DO40
 5 MEM_MB_DATA41 143 DO41
 5 MEM_MB_DATA42 151 DO42
 5 MEM_MB_DATA43 153 DO43
 5 MEM_MB_DATA44 140 DO44
 5 MEM_MB_DATA45 142 DO45
 5 MEM_MB_DATA46 152 DO46
 5 MEM_MB_DATA47 154 DO47
 5 MEM_MB_DATA48 157 DO48
 5 MEM_MB_DATA49 159 DO49
 5 MEM_MB_DATA50 173 DO50
 5 MEM_MB_DATA51 175 DO51
 5 MEM_MB_DATA52 158 DO52
 5 MEM_MB_DATA53 160 DO53
 5 MEM_MB_DATA54 174 DO54
 5 MEM_MB_DATA55 176 DO55
 5 MEM_MB_DATA56 179 DO56
 5 MEM_MB_DATA57 181 DO57
 5 MEM_MB_DATA58 189 DO58
 5 MEM_MB_DATA59 191 DO59
 5 MEM_MB_DATA60 180 DO60
 5 MEM_MB_DATA61 182 DO61
 5 MEM_MB_DATA62 192 DO62
 5 MEM_MB_DATA63 194 DO63

5 MEM_MB_DQS0_N 11C DQS0#
 5 MEM_MB_DQS1_N 29C DQS1#
 5 MEM_MB_DQS2_N 49C DQS2#
 5 MEM_MB_DQS3_N 68C DQS3#
 5 MEM_MB_DQS4_N 129C DQS4#
 5 MEM_MB_DQS5_N 146C DQS5#
 5 MEM_MB_DQS6_N 167C DQS6#
 5 MEM_MB_DQS7_N 186C DQS7#

5 MEM_MB_DQS0_P 13 DQS0
 5 MEM_MB_DQS1_P 31 DQS1
 5 MEM_MB_DQS2_P 51 DQS2
 5 MEM_MB_DQS3_P 70 DQS3
 5 MEM_MB_DQS4_P 131 DQS4
 5 MEM_MB_DQS5_P 148 DQS5
 5 MEM_MB_DQS6_P 169 DQS6
 5 MEM_MB_DQS7_P 188 DQS7

5,18 MEM_MB_ODT0 114 OTD0
 5,18 MEM_MB_ODT1 119 OTD1

NORMAL TYPE

RAS# 108 A0
 WE# 109 A1
 CAS# 113 A2
 CS0# 110 A3
 CS1# 115 A4
 CKE0 79 A5
 CKE1 80 A6
 CK0 30 A7
 CK0# 32 A8
 CK1 164 A9
 CK1# 166 A10

DM0 10 MEM_MB_DM0_5
 DM1 26 MEM_MB_DM1_5
 DM2 52 MEM_MB_DM2_5
 DM3 67 MEM_MB_DM3_5
 DM4 130 MEM_MB_DM4_5
 DM5 147 MEM_MB_DM5_5
 DM6 170 MEM_MB_DM6_5
 DM7 185 MEM_MB_DM7_5

SDA 195 SMBD0_SB 3,12,16
 SCL 197 SMBD0_SB 3,12,16

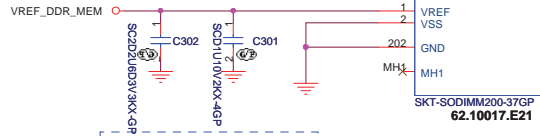
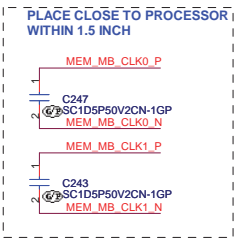
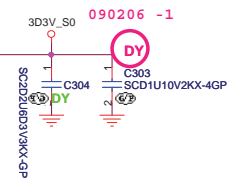
VDDSPD 199
 SA0 198
 SA1 200

NC#50 50 X
 NC#69 69 X
 NC#83 83 X
 NC#120 120 X
 NC#163 163 X

VDD 81
 VDD 82
 VDD 87
 VDD 88
 VDD 95
 VDD 96
 VDD 103
 VDD 104
 VDD 111
 VDD 112
 VDD 117
 VDD 118

VSS 3
 VSS 8
 VSS 9
 VSS 12
 VSS 15
 VSS 18
 VSS 21
 VSS 24
 VSS 27
 VSS 28
 VSS 33
 VSS 34
 VSS 38
 VSS 40
 VSS 41
 VSS 42
 VSS 47
 VSS 48
 VSS 53
 VSS 59
 VSS 60
 VSS 65
 VSS 66
 VSS 71
 VSS 72
 VSS 77
 VSS 78
 VSS 121
 VSS 122
 VSS 127
 VSS 128
 VSS 132
 VSS 133
 VSS 138
 VSS 139
 VSS 144
 VSS 145
 VSS 149
 VSS 150
 VSS 155
 VSS 156
 VSS 161
 VSS 162
 VSS 165
 VSS 168
 VSS 171
 VSS 172
 VSS 177
 VSS 178
 VSS 183
 VSS 184
 VSS 187
 VSS 190
 VSS 193
 VSS 196

GND 201
 MH2 202



Place C2.2uF and 0.1uF < 500mils from DDR connector
 HI 9.2mm
 ZND = 62.10017.071

<Core Design>

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Title: **DDR_SO-DIMM SKT_2**

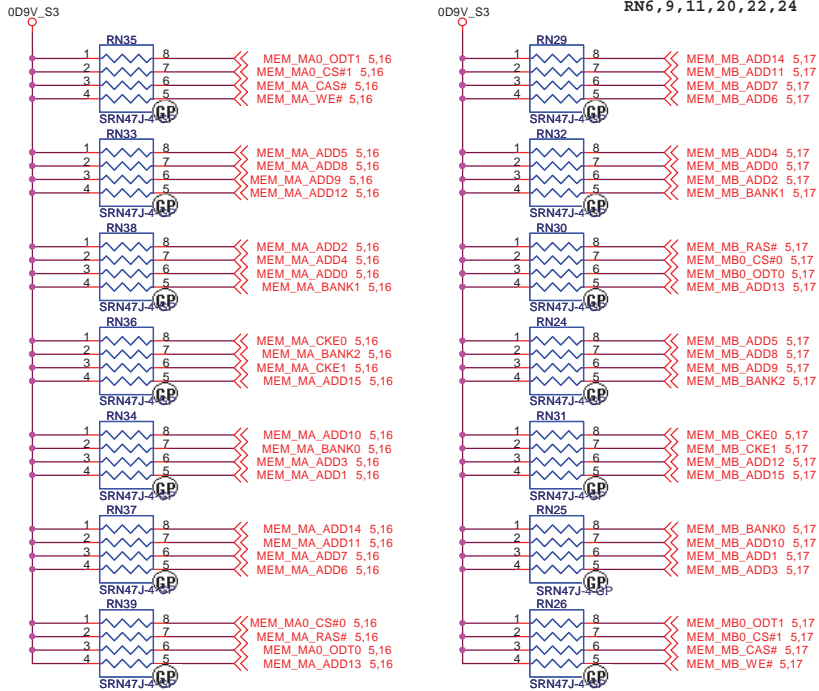
Size: Custom Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet 17 of 56

PARALLEL TERMINATION

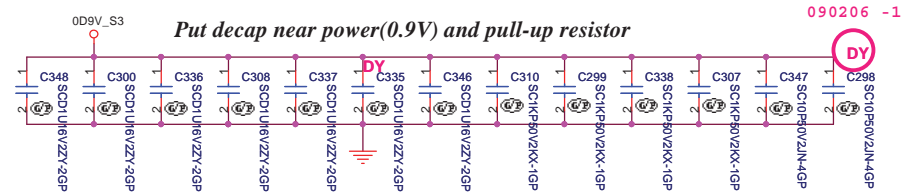
Put decap near power(0.9V) and pull-up resistor

Net swap 11/14
RN6, 9, 11, 20, 22, 24

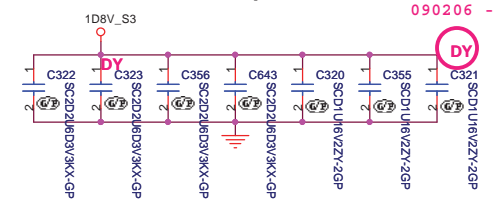


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

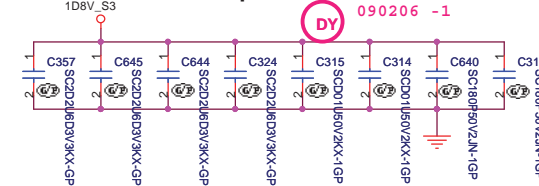


Place these Caps near DM1

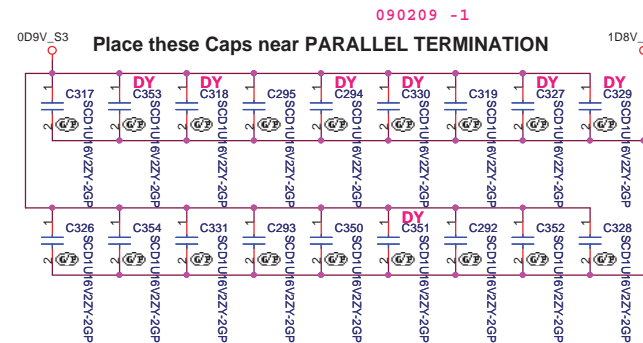


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3



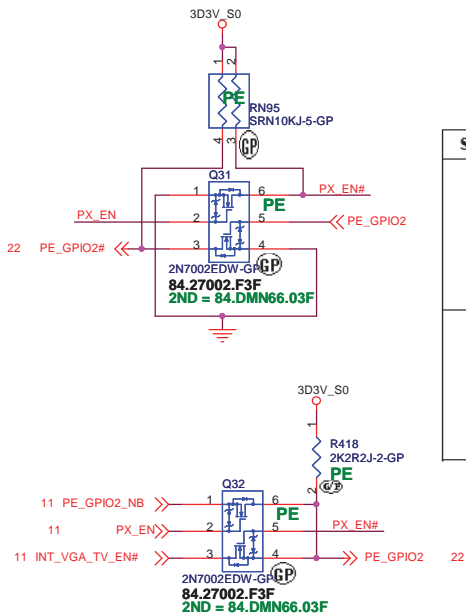
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Taipei Hsien 221, Taiwan, R.O.C.

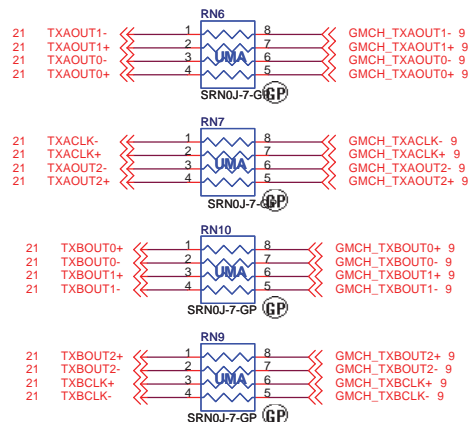
Title
DDR DAMPING & TERMINATION

Size A3 Document Number **JM70-PU** Rev -2

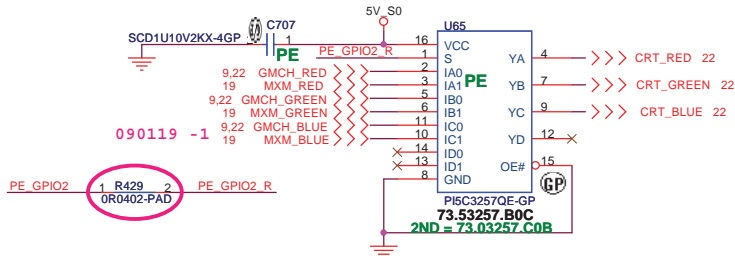
Date: Friday, March 06, 2009 Sheet 18 of 56



| FUNCTION TABLE | | |
|----------------|--|--|
| SEL | FUNCTION | OUTPUT |
| L | TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance | TMDSn+ TMDSn- TMDSCLK+ TMDSCLK- |
| H | TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance | TMDSn+ TMDSn- TMDSCLK+ TMDSCLK- |

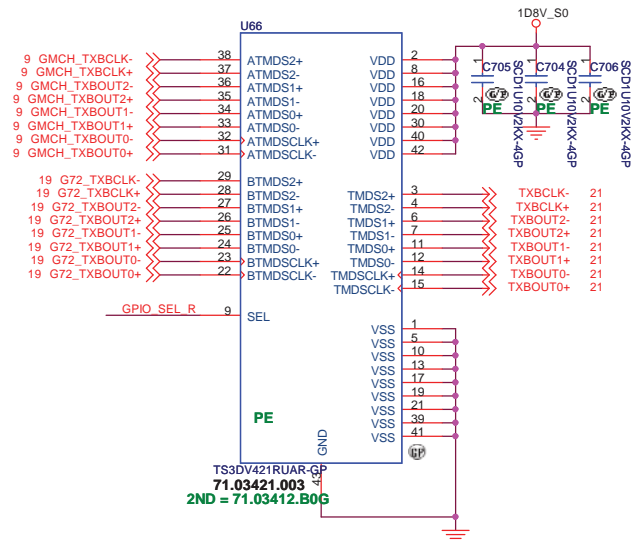
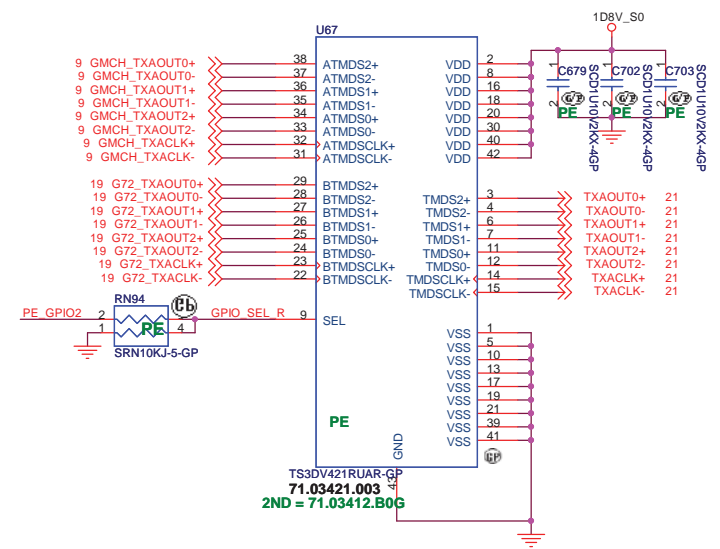


| \bar{E} | S | YA | YB | YC | YD | Function |
|-----------|---|------|------|------|------|----------|
| H | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Disable |
| L | L | IA0 | IB0 | IC0 | ID0 | S = 0 |
| L | H | IA1 | IB1 | IC1 | ID1 | S = 1 |



DISPLAY SUPPORT TABLE

| | PX_EN | PE_GPIO2_NB | INT_VGA_EN# | DISPLAY OUTPUT |
|--------------------|-------|-------------|-------------|----------------------------------|
| IGP only mode | 0 | X | 0 | IGP(LVDS,VGA,HDMI,DP) |
| MXM only mode | 0 | X | 1 | MXM(LVDS,VGA,HDMI,DP) |
| Power Express mode | 1 | 0/1 | X | *MXM(VGA,HDMI,DP); MXM/IGP(LVDS) |
| IGP + MXM | 0 | X | 0 | IGP(LVDS,VGA,HDMI) |



<Core Design>

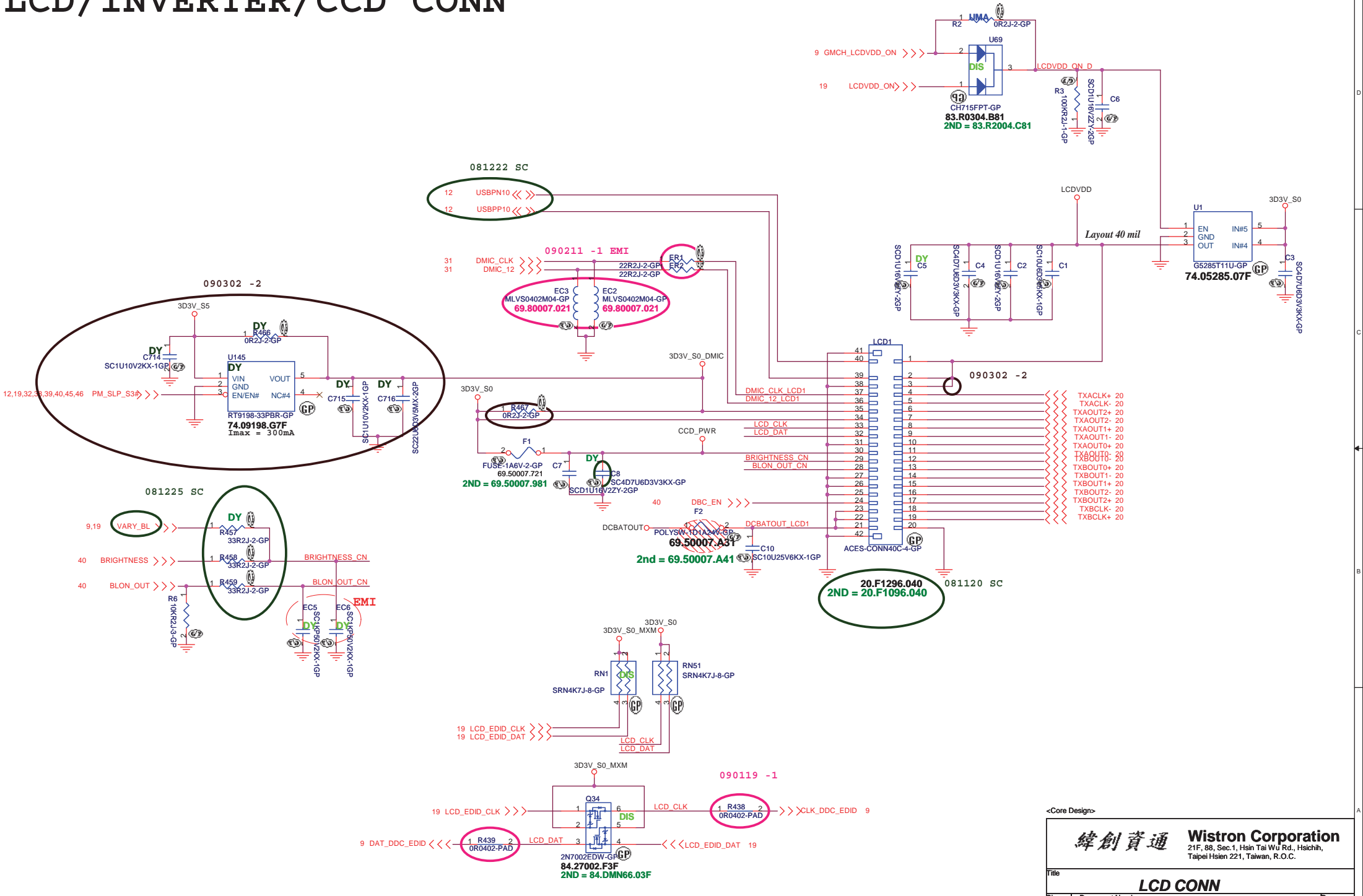
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Title: **SWITCH**

Size: Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet 20 of 56

LCD/INVERTER/CCD CONN

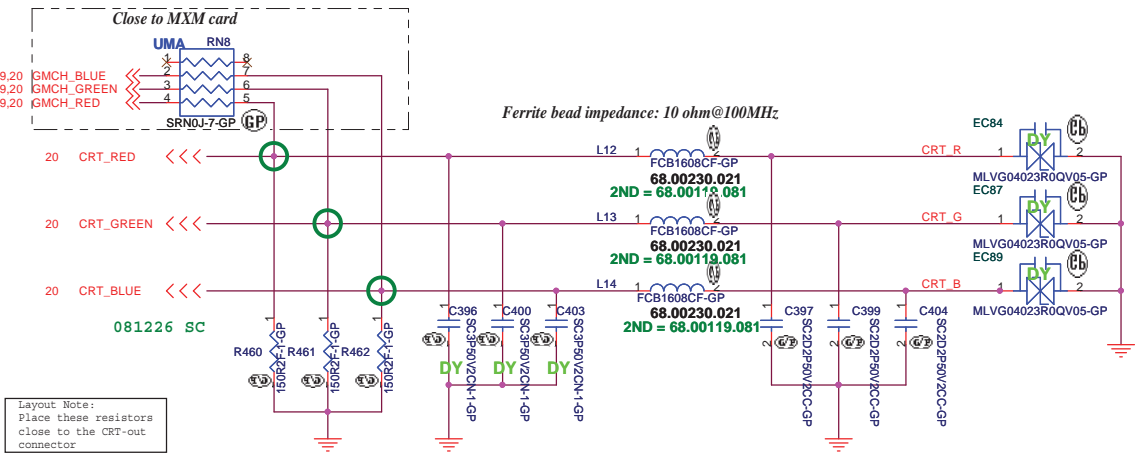


<Core Design>

緯創資通 Wistron Corporation
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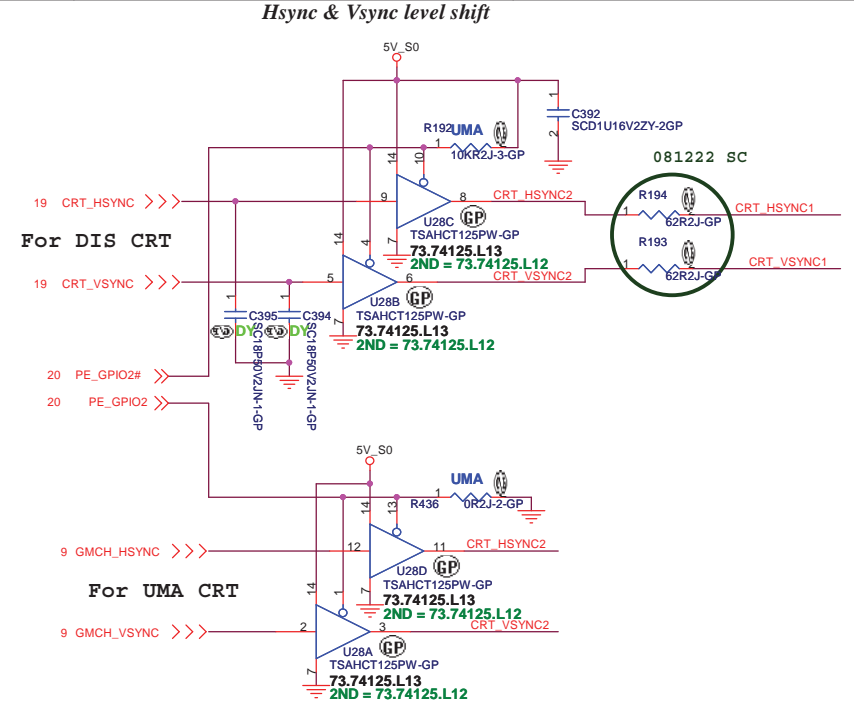
Title: **LCD CONN**

| | | |
|------------------------------|---------------------------------|---------|
| Size: A3 | Document Number: JM70-PU | Rev: -2 |
| Date: Friday, March 06, 2009 | Sheet: 21 of 56 | |

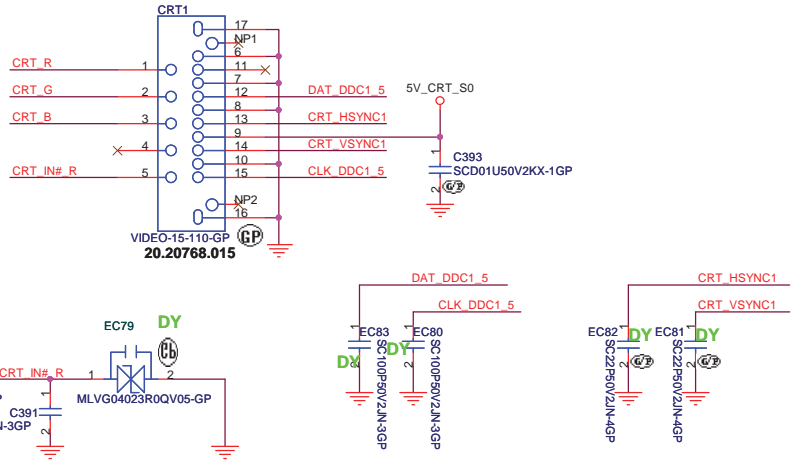
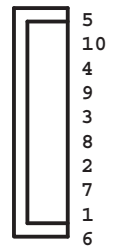


Layout Note:
Place these resistors close to the CRT-out connector

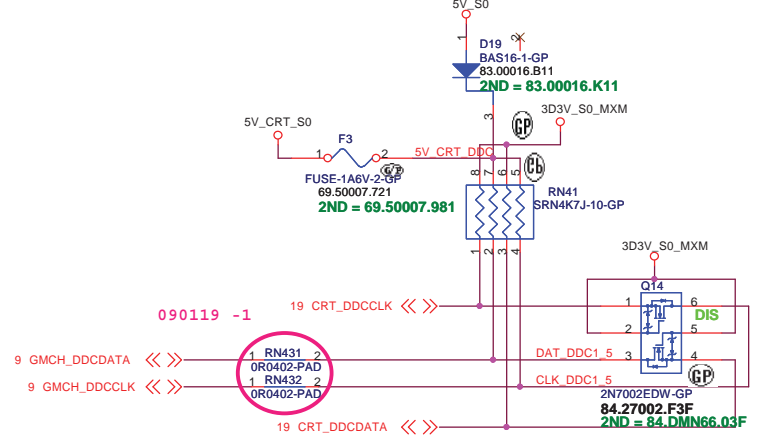
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

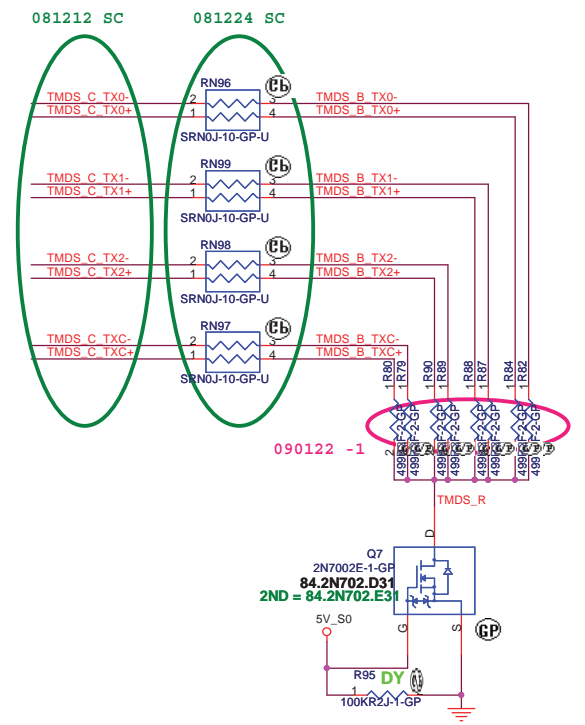
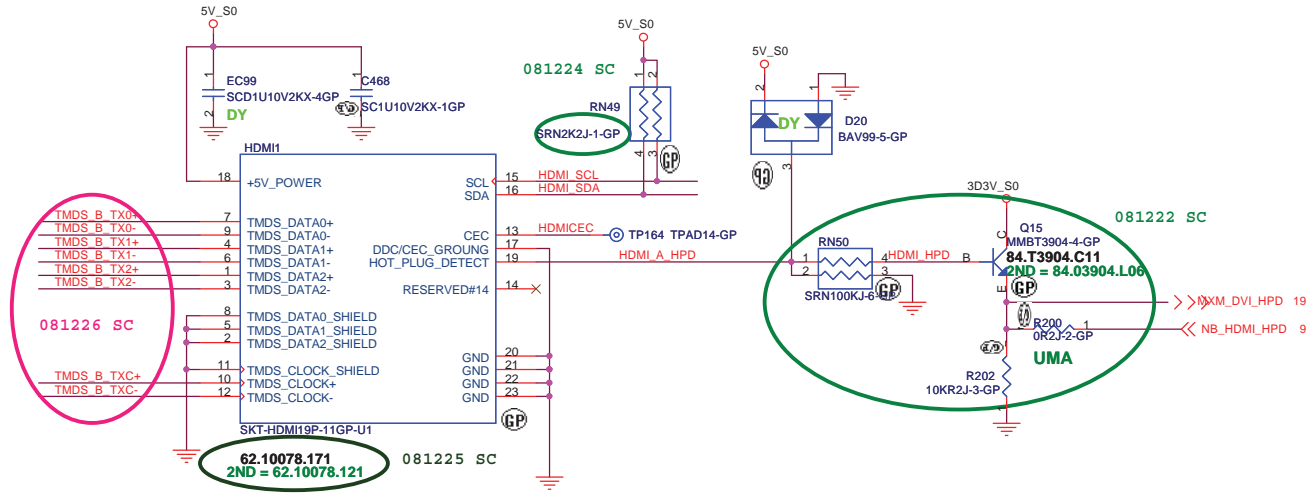


CRT I/F & CONNECTOR

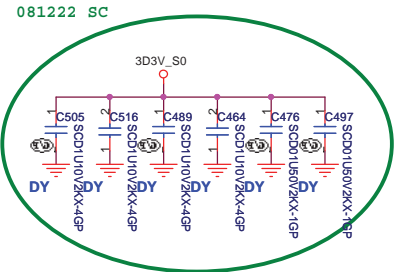
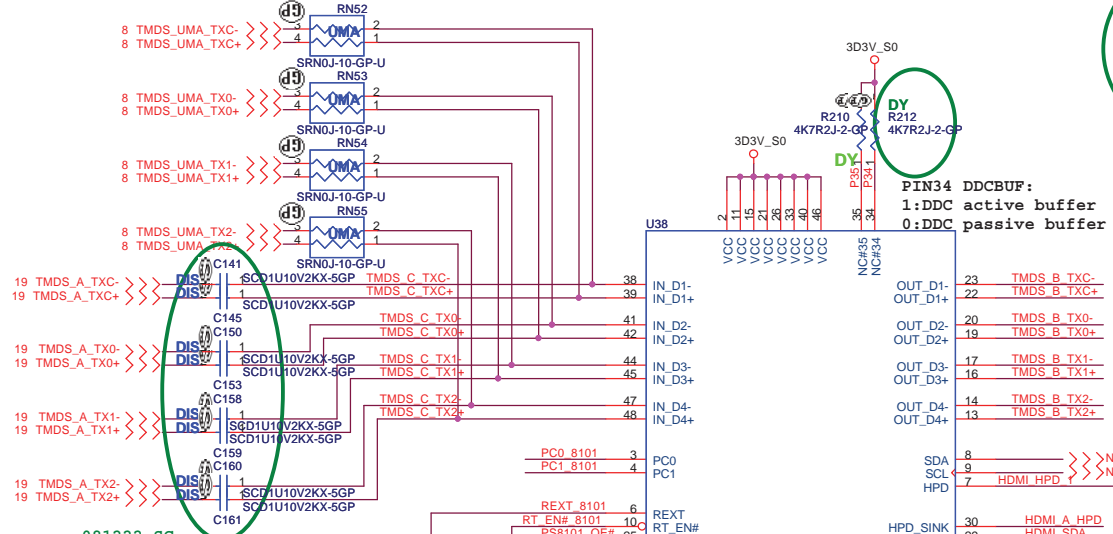


DDC_CLK & DATA level shift



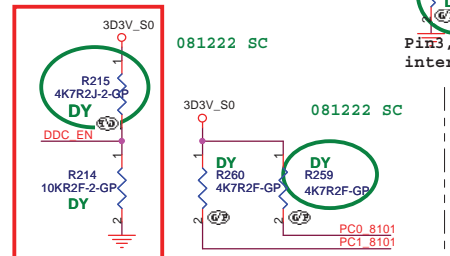
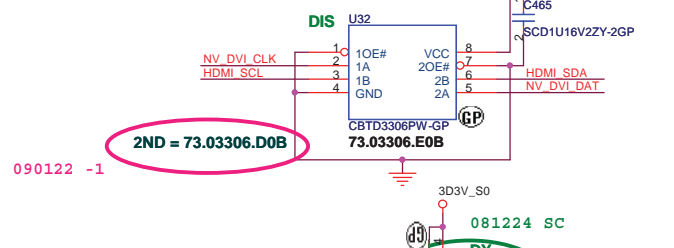


Place Near MXM3 Connector

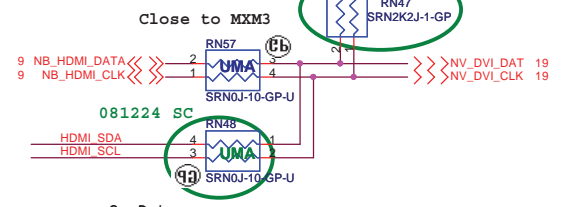
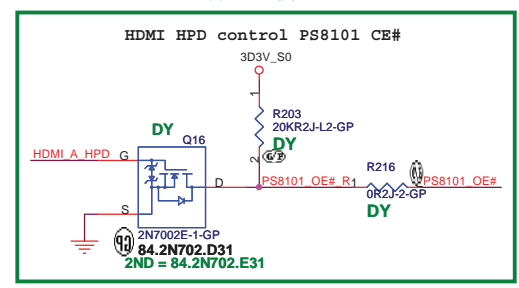
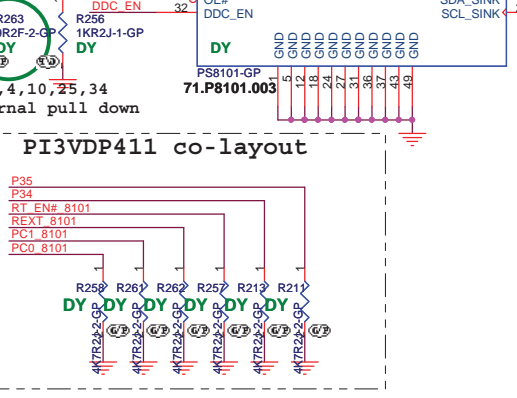


HDMI SM BUS LEVEL shifter

Close HDMI1



Recommended Equalization:
[PC1, PC0]=01, 4dB



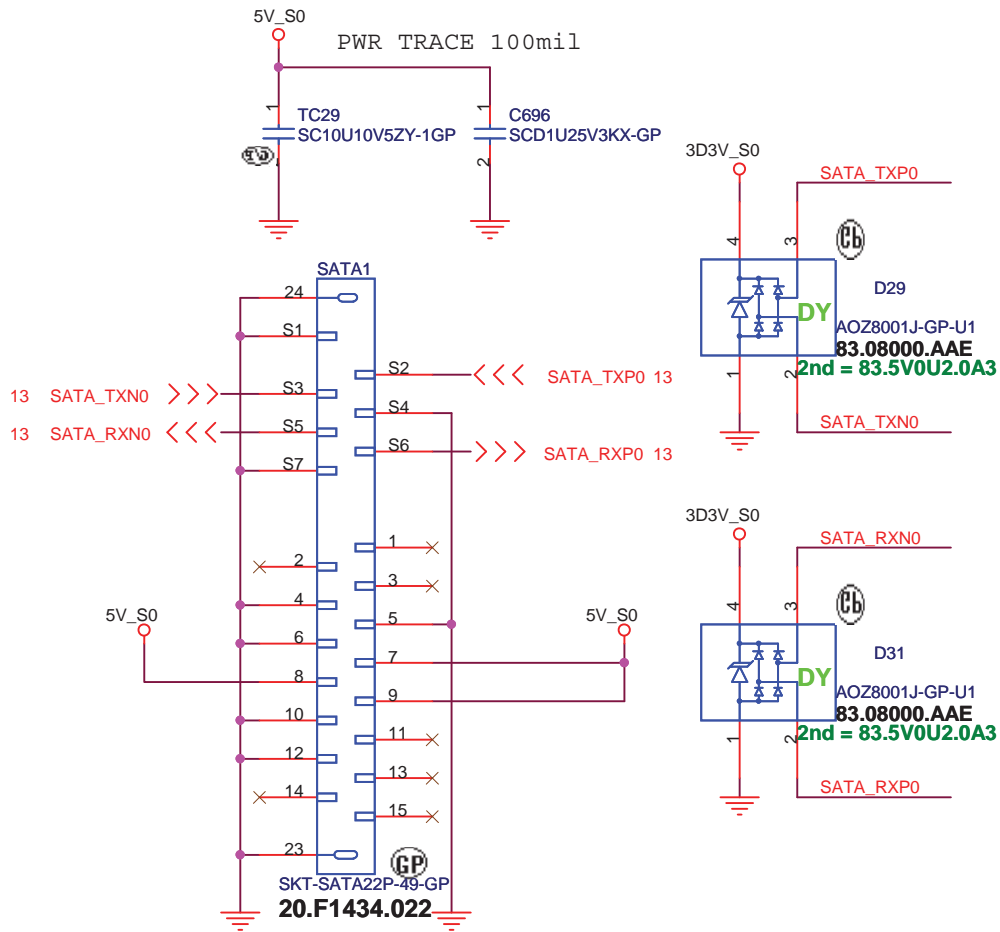
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HDMI CONNECTOR

Size A3 Document Number **JM70-PU** Rev -2

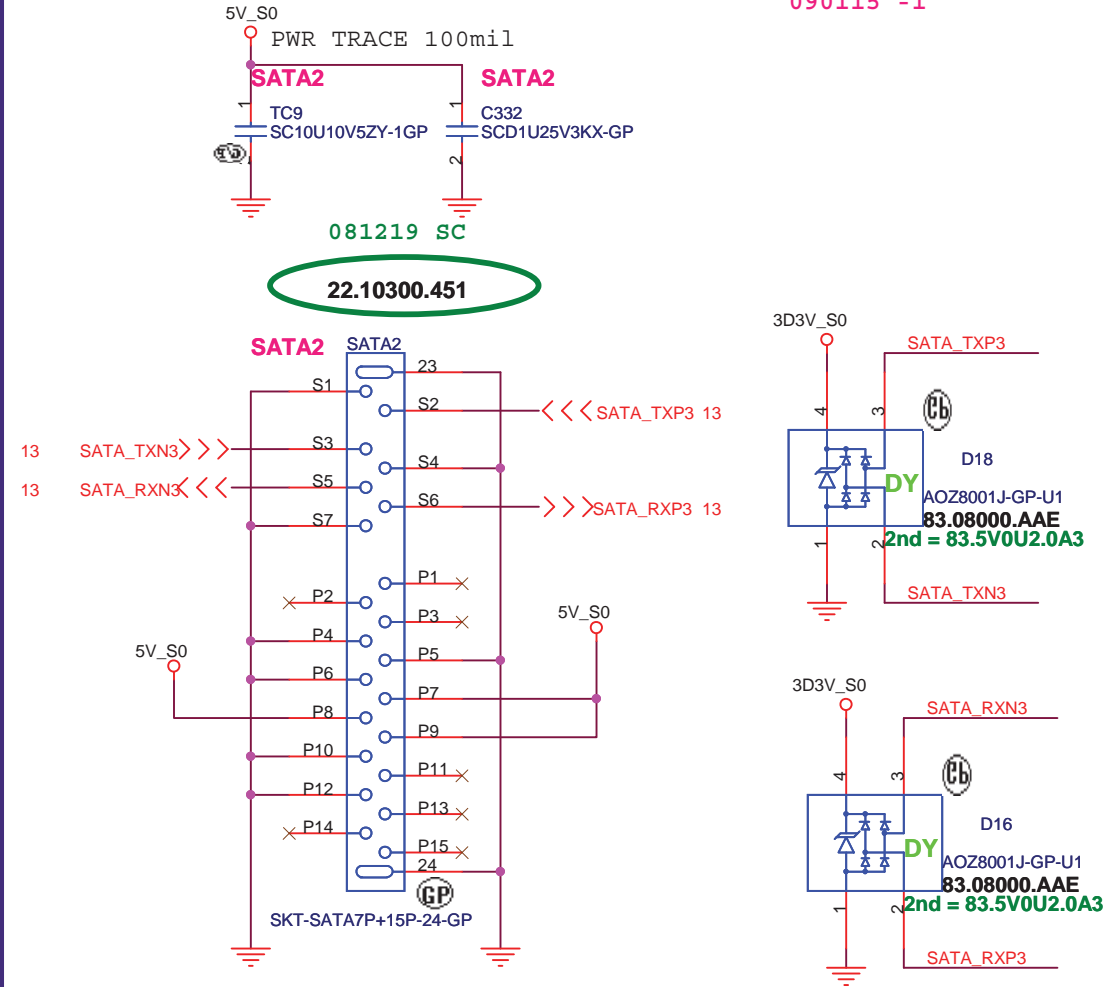
Date: Friday, March 06, 2009 Sheet 23 of 56

SATA HDD Connector




2ND SATA HDD Connector

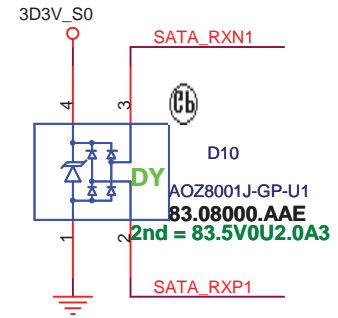
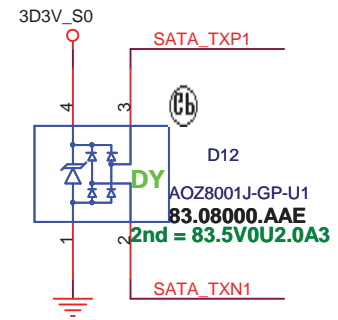
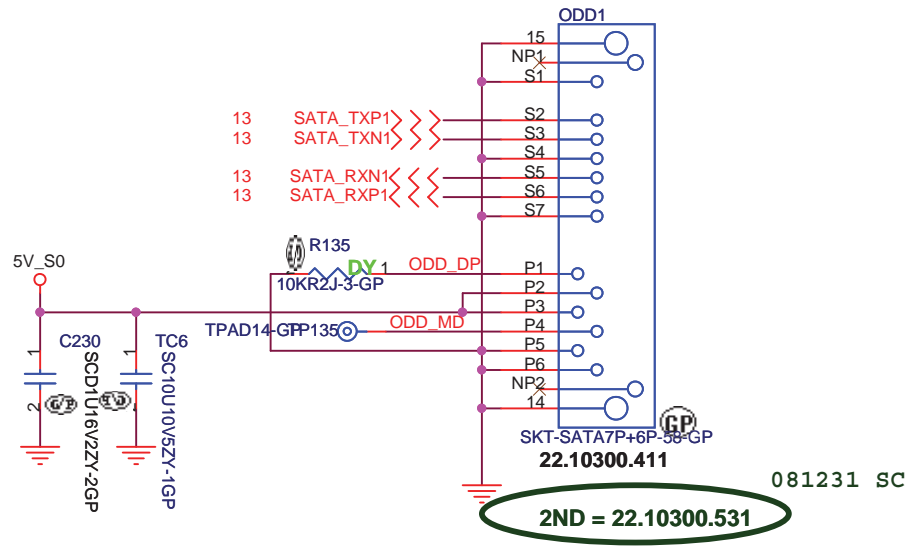
090115 -1



<Core Design>

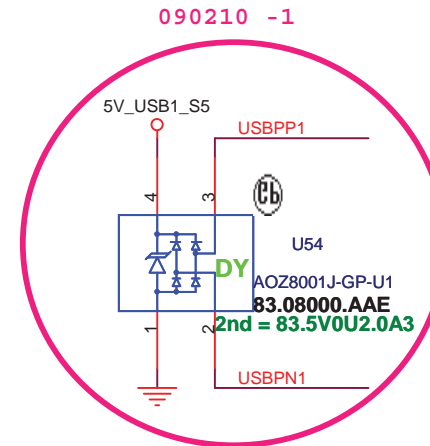
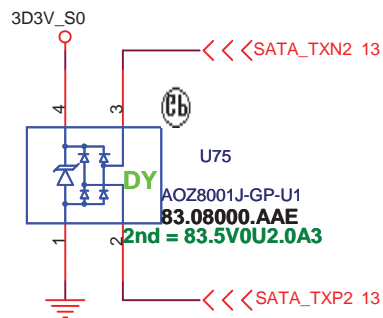
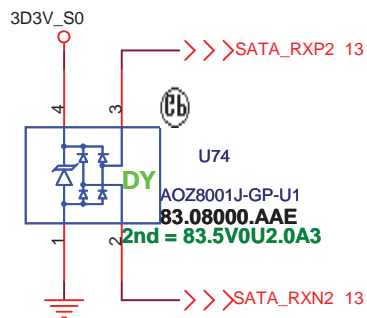
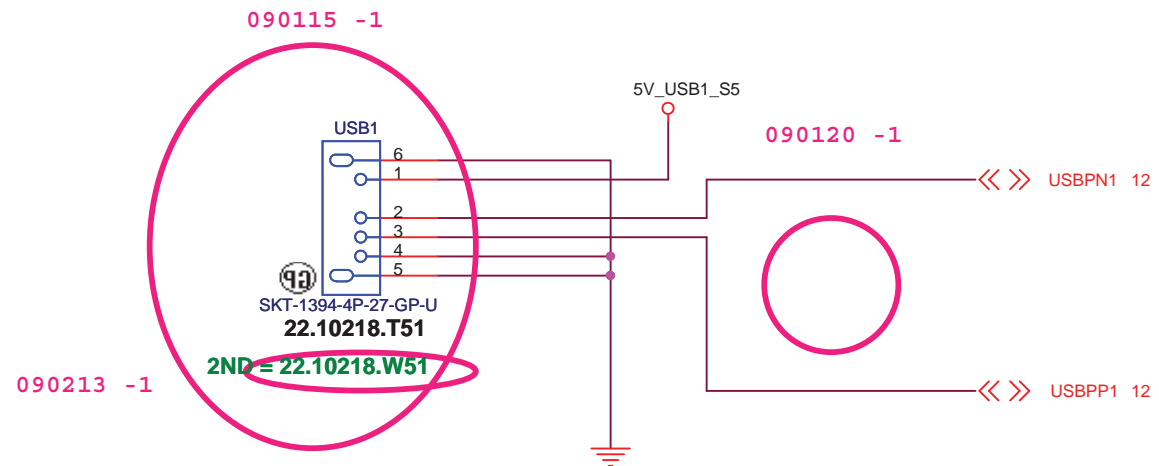
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|  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title | | |
| HDD | | |
| Size | Document Number | Rev |
| A4 | JM70-PU | -2 |
| Date: | Friday, March 06, 2009 | Sheet 24 of 56 |

ODD Connector



<Core Design>

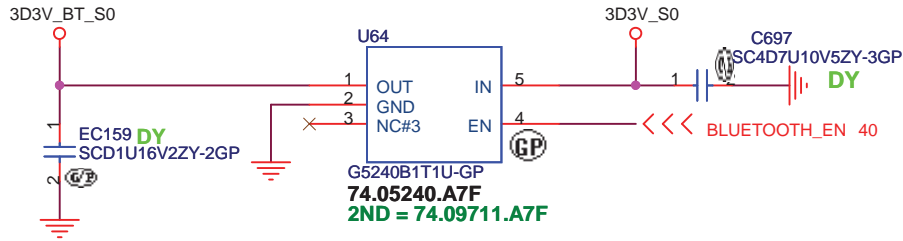
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| Title | |
| CDROM | |
| Size | Document Number |
| A4 | JM70-PU |
| Date: | Rev |
| Friday, March 06, 2009 | -2 |
| Sheet 25 of 56 | |



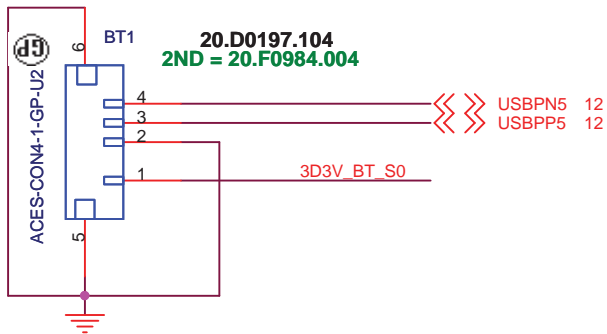
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| 緯創資通 | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | USB1 | |
| Size | Document Number | | Rev |
| A4 | JM70-PU | | -2 |
| Date: | Friday, March 06, 2009 | Sheet | 26 of 56 |


BLUETOOTH MODULE



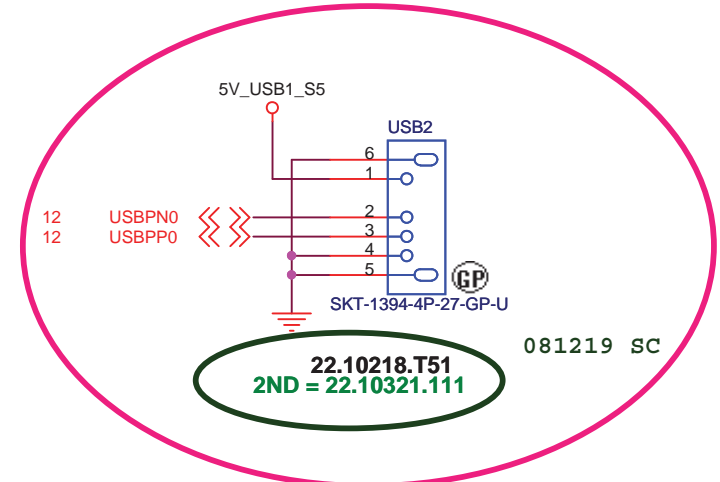
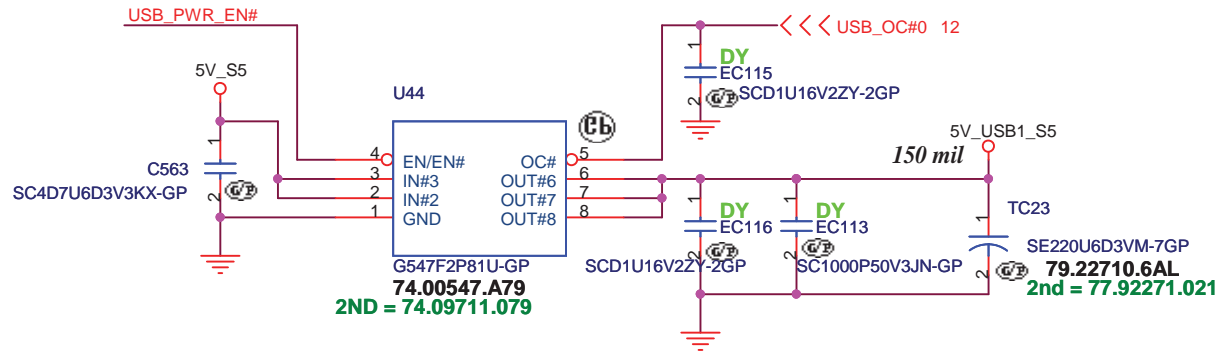
EC40 put near BLUE1 / all USB put one choke near connector by EMI request



<Core Design>

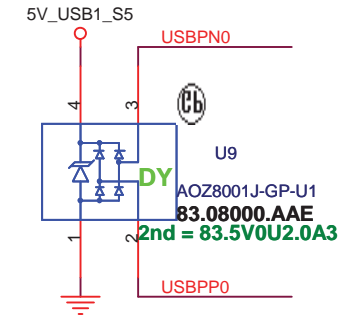
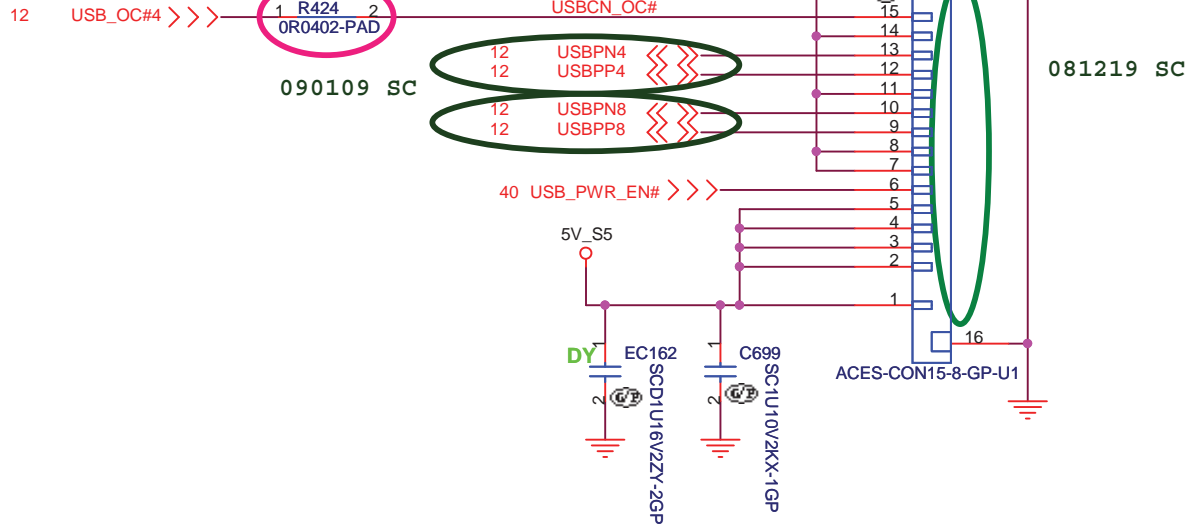
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| Title | |
| BLUETOOTH | |
| Size | Document Number |
| A4 | JM70-PU |
| Date: | Rev |
| Friday, March 06, 2009 | -2 |
| Sheet 27 of 56 | |

090115 -1



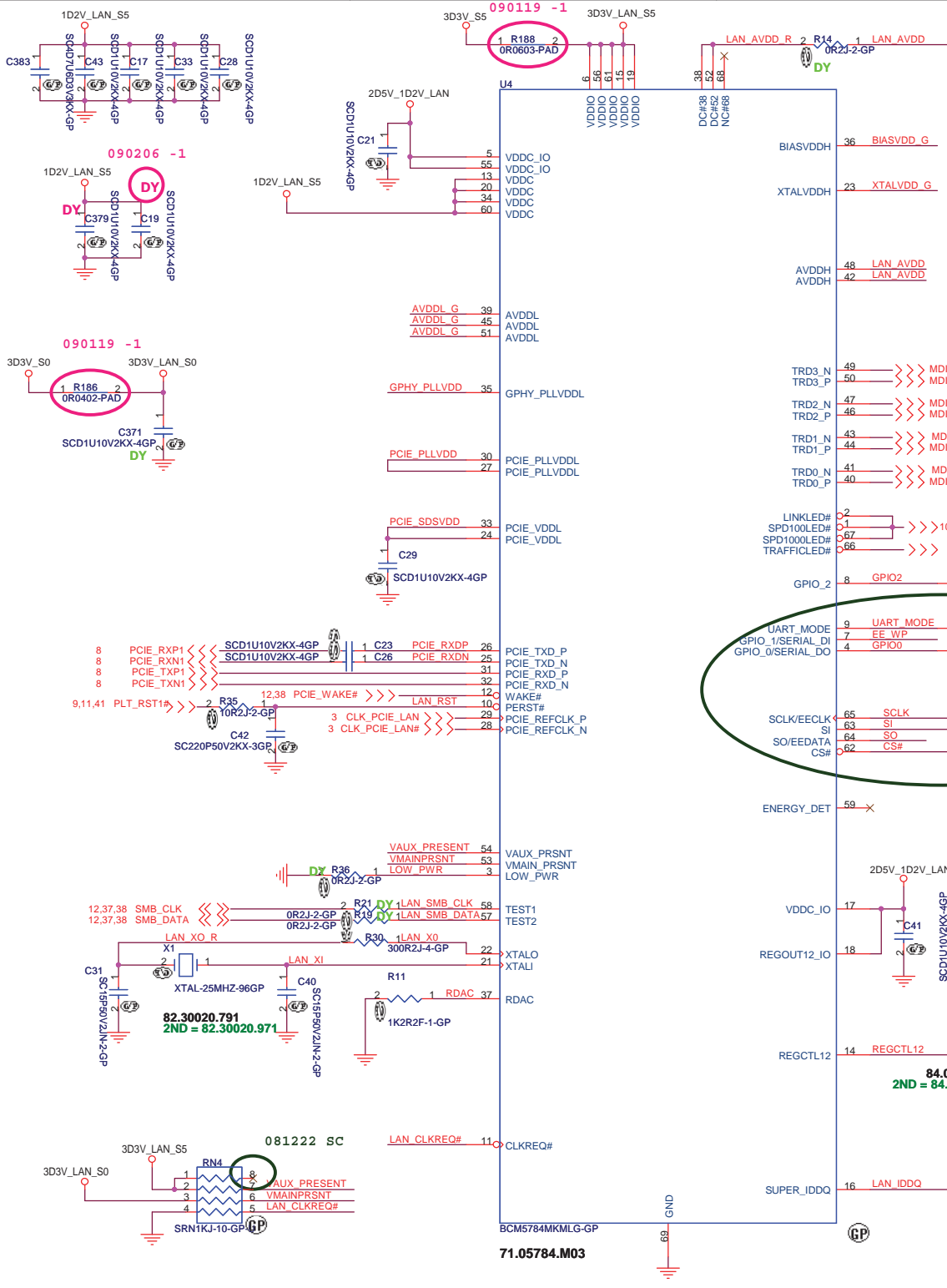
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2ND = 21.D0214.115

090119 -1



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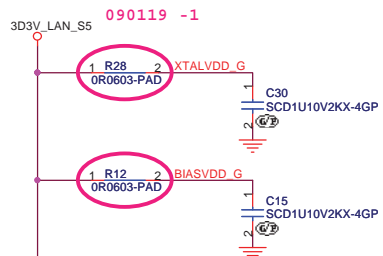
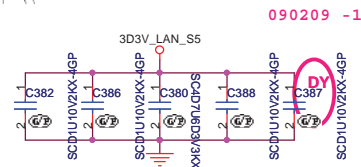
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| | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| USB2 | | | |
| Size | Document Number | | Rev |
| A4 | JM70-PU | | -2 |
| Date: | Friday, March 06, 2009 | Sheet | 28 of 56 |



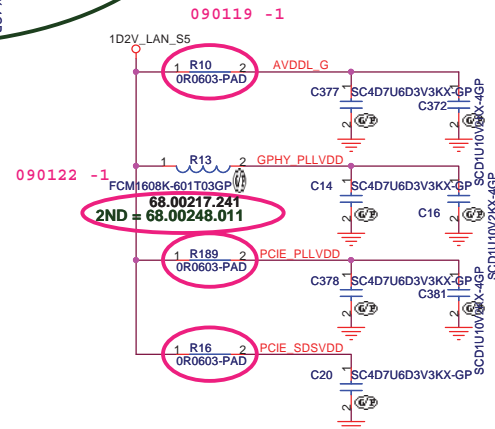
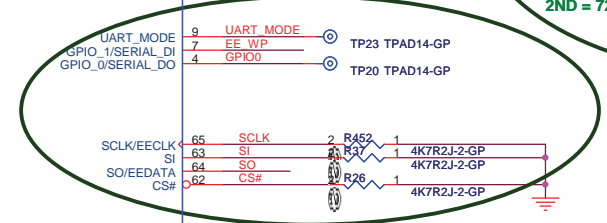
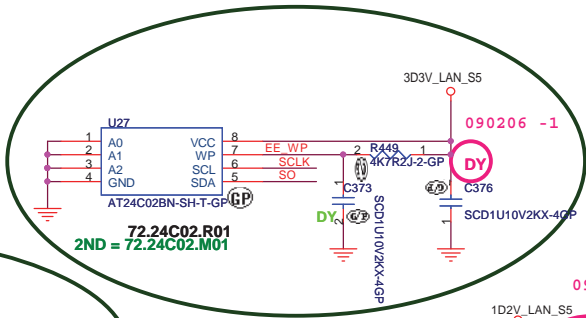
Note: SI, SO, CS, and SCLK have internal pull-ups.

Table 7: NVRAM Pin Strapping (EEPROM)

| NVRAM Type | SO | SI | CS | SCLK |
|--------------------------|----|----|----|------|
| EEPROM—24c64—376 KHz | 1 | 1 | 0 | 1 |
| EEPROM—24c512—376 KHz | 1 | 1 | 0 | 1 |
| Microchip 24LC02—376 KHz | 1 | 0 | 0 | 0 |
| Microchip 24LC04—376 KHz | 1 | 0 | 0 | 0 |
| Microchip 24LC08—376 KHz | 1 | 0 | 0 | 0 |



Place PLLVDD/AVDDL CKT as close to chip as possible



R349 change to Bead for Transmitter Distortion

<Core Design>

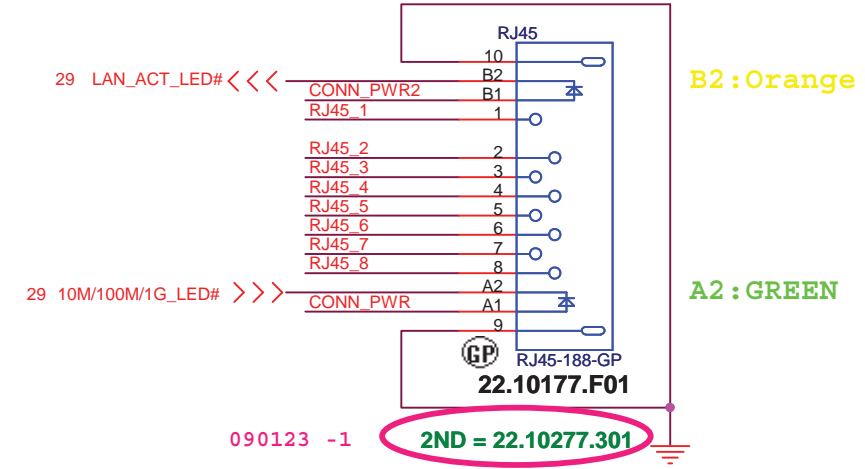
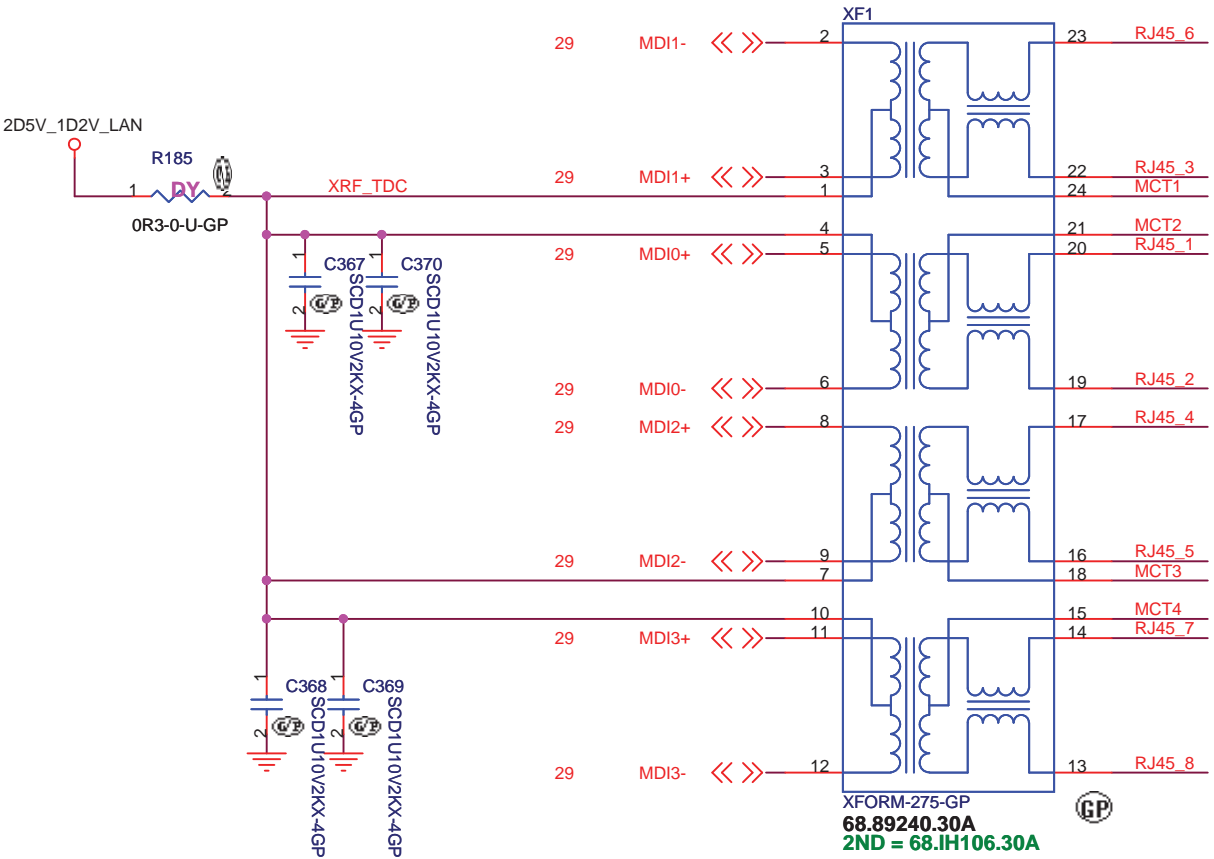
緯創資通 Wistron Corporation
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Title: **BCM5784MKMLG**

Size: **A3** Document Number: **JM70-PU** Rev: **-2**

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LAN Connector



LAN Link: Green(A2), behavior is the same for 10/100/1000 bits

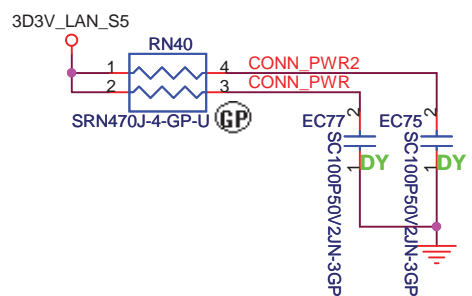
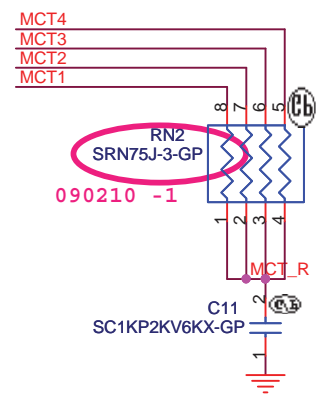
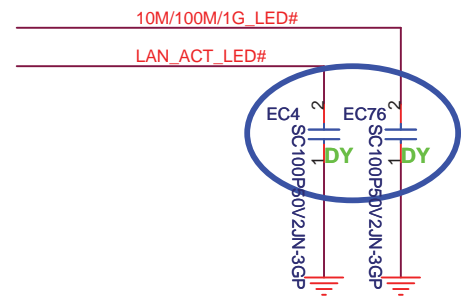
LAN Data: Yellow(B2), when LAN is transferring data.

XFORM-275-GP
68.89240.30A
2ND = 68.IH106.30A

Soucrer want to add 3rd source 11/10
68.05009.301 GST5009-R LF
Angela Chi 0955-314886

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

For EMI Near LAN1 CONN

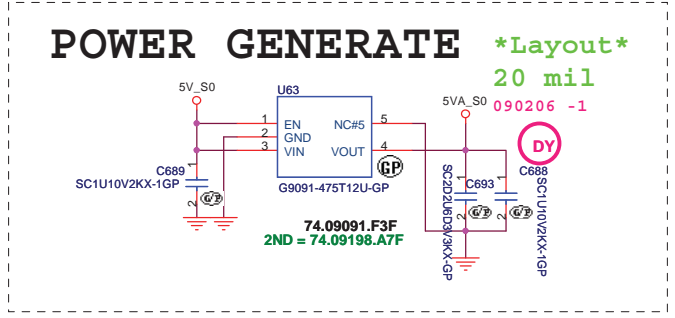
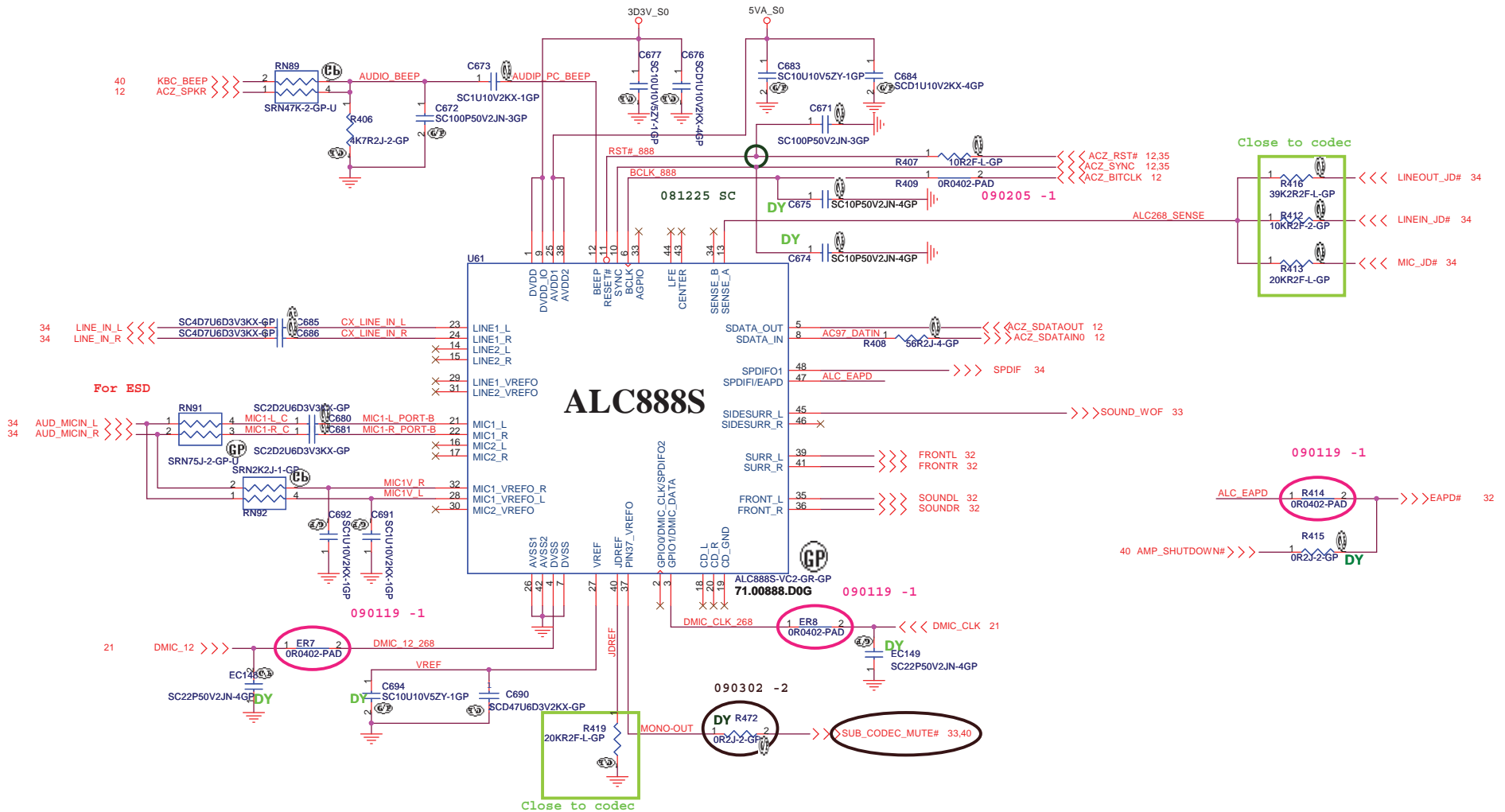


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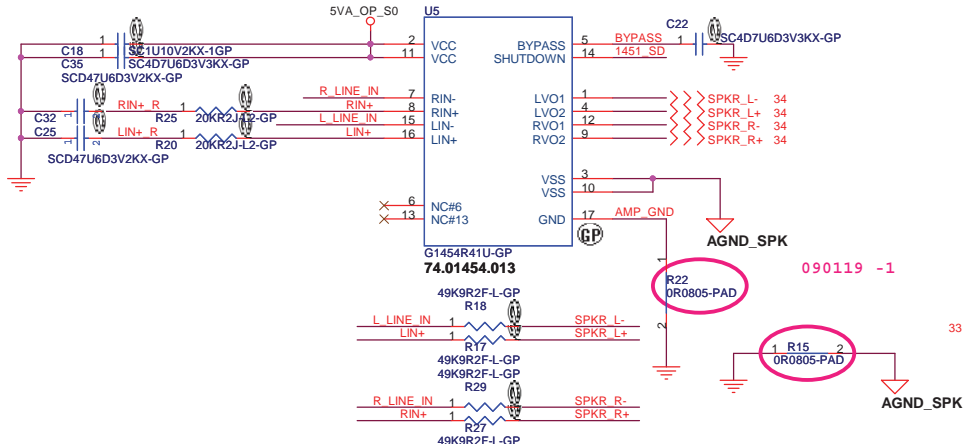
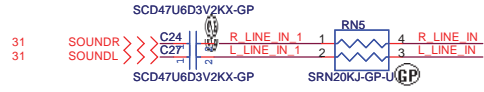
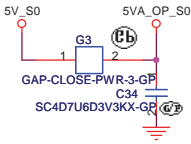
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Title: **LAN CONN**

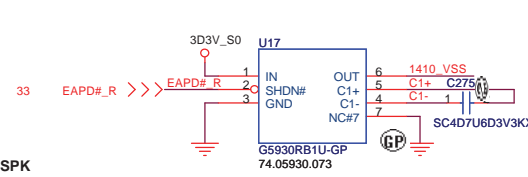
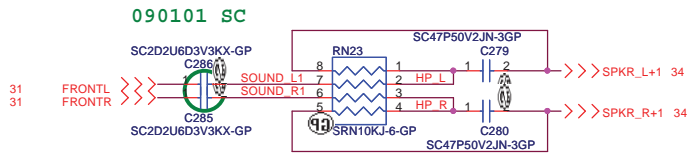
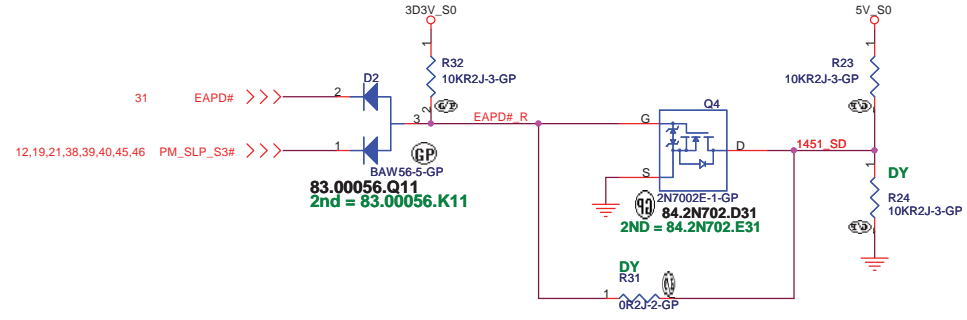
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| Size: A4 | Document Number: JM70-PU | Rev: -2 |
| Date: Friday, March 06, 2009 | | Sheet 30 of 56 |



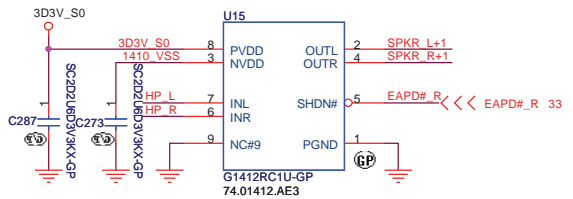
AUDIO OP AMPLIFIER



Gain= $R_f/R_i=49.9K/20K=2.495V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$
 If $V_{IN}=1.54V$ Gain=2.6V/V $R_L=4\Omega$ $V_O(peak) = 4V$
 $V(rms)=2.828V$
 Power= $2.828^2/4=1.999W$



Gain= $R_f/R_i=20K/18K=0.9V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$
 If $V_{IN}=1.54V$ Gain=0.9V/V $R_L=4\Omega$ $V_O(peak) = 4V$ $V(rms)=2.828V$
 Power= ?



<Core Design>

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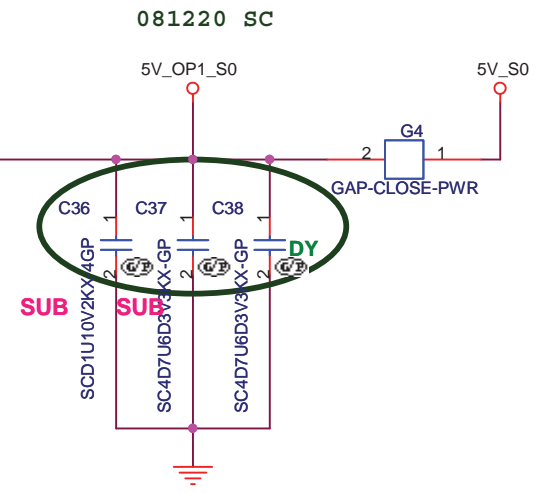
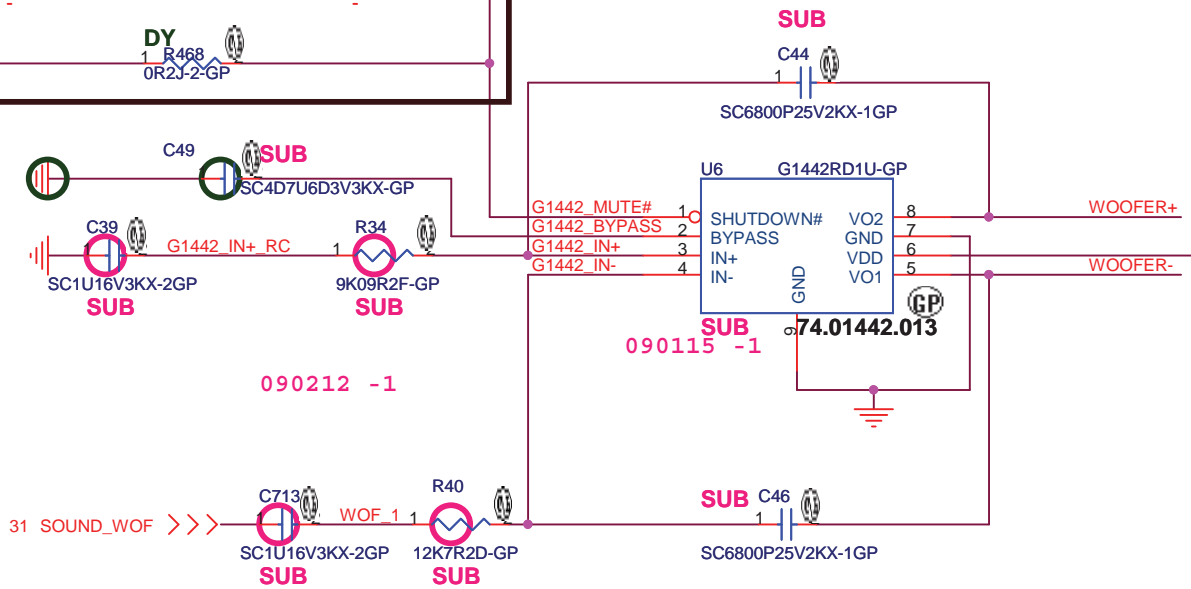
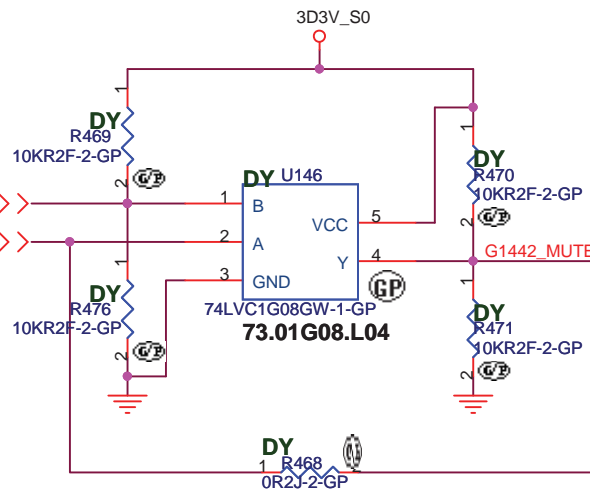
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Size: **A3** Document Number: **JM70-PU** Rev: **-2**

Date: **Friday, March 06, 2009** Sheet: **32** of **56**

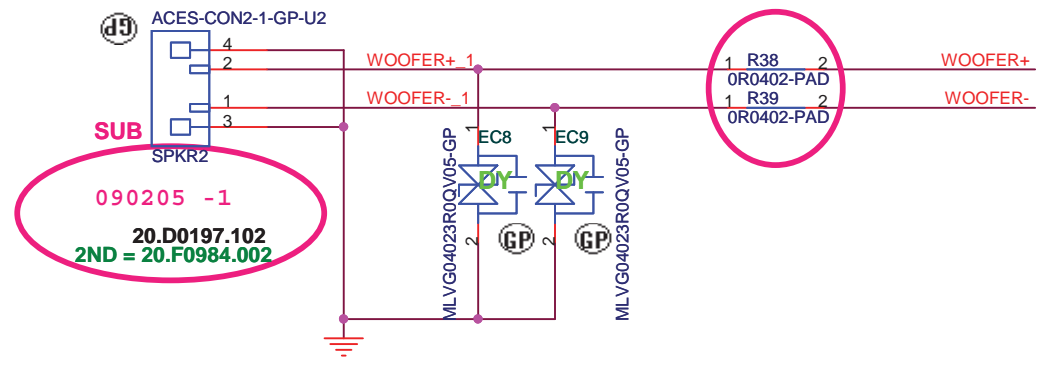
090305 -2

31, 30 SUB_CODEC_MUTE# >>>
32 EAPD#_R >>>



SUBWOOFER CONN.

090119 -1

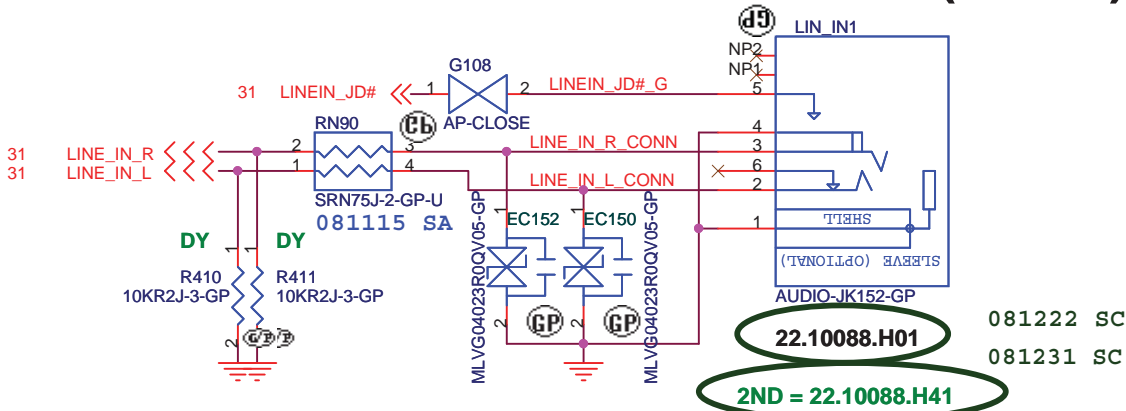


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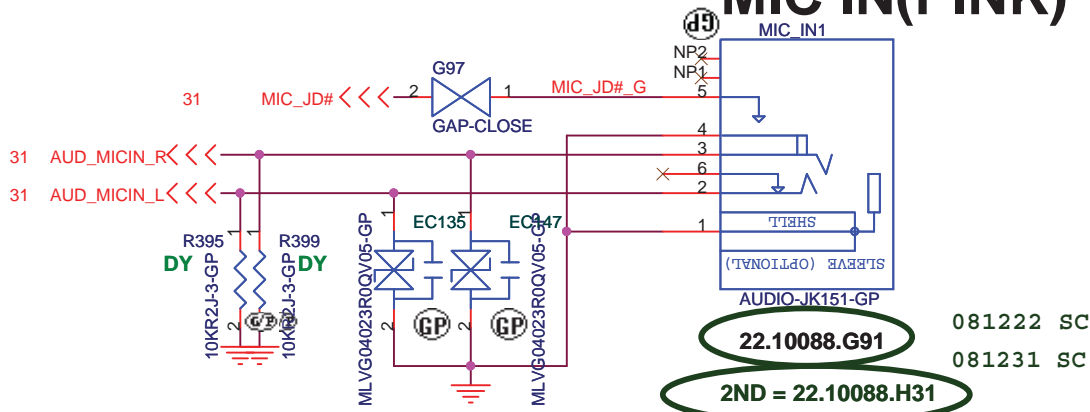
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Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|-----------------------------------|------------------|
| Title Audio AMP for Subwoofer | | |
| Size A4 | Document Number JM70-PU | Rev -2 |
| Date: Friday, March 06, 2009 | Sheet 33 | of 56 |

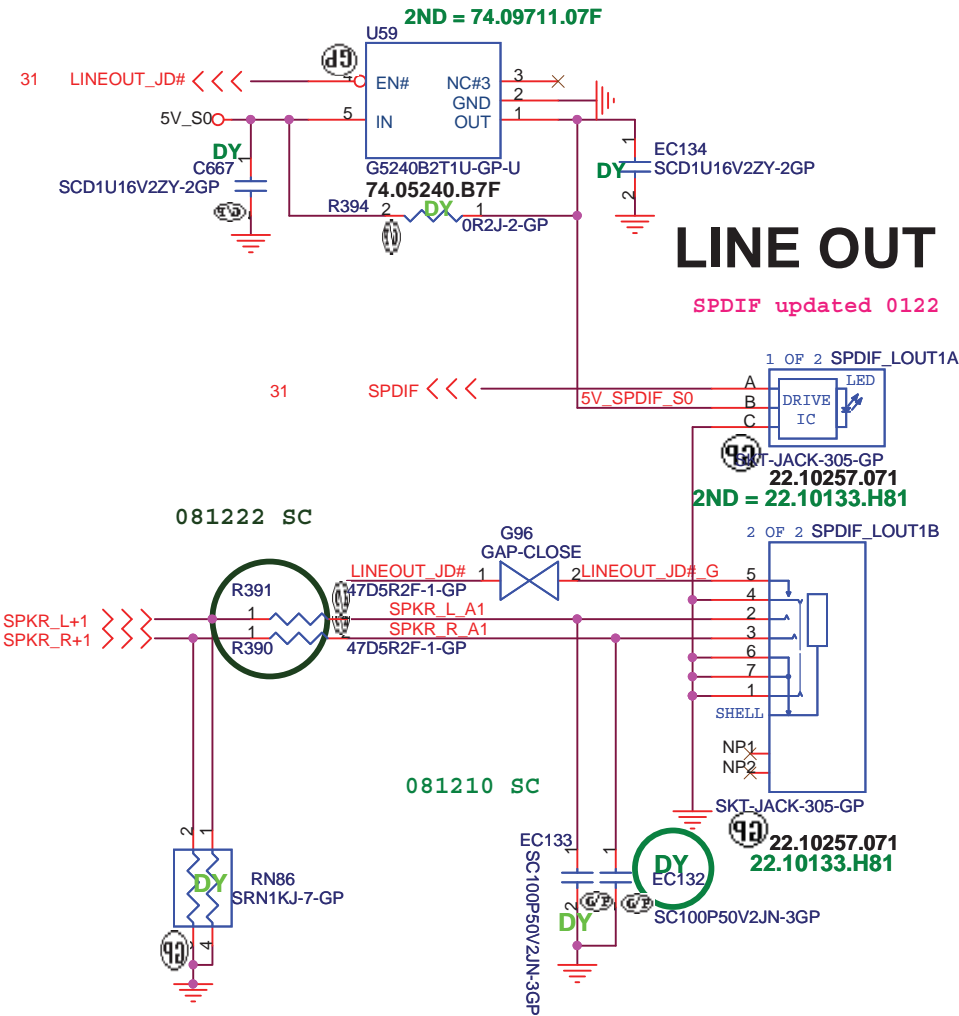
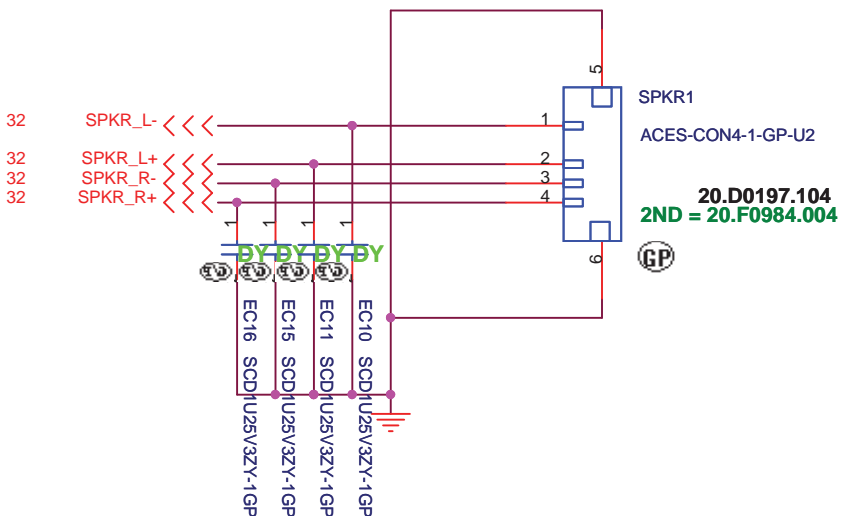
LINE IN(BLUE)



MIC IN(PINK)



REAR Speaker



LINE OUT

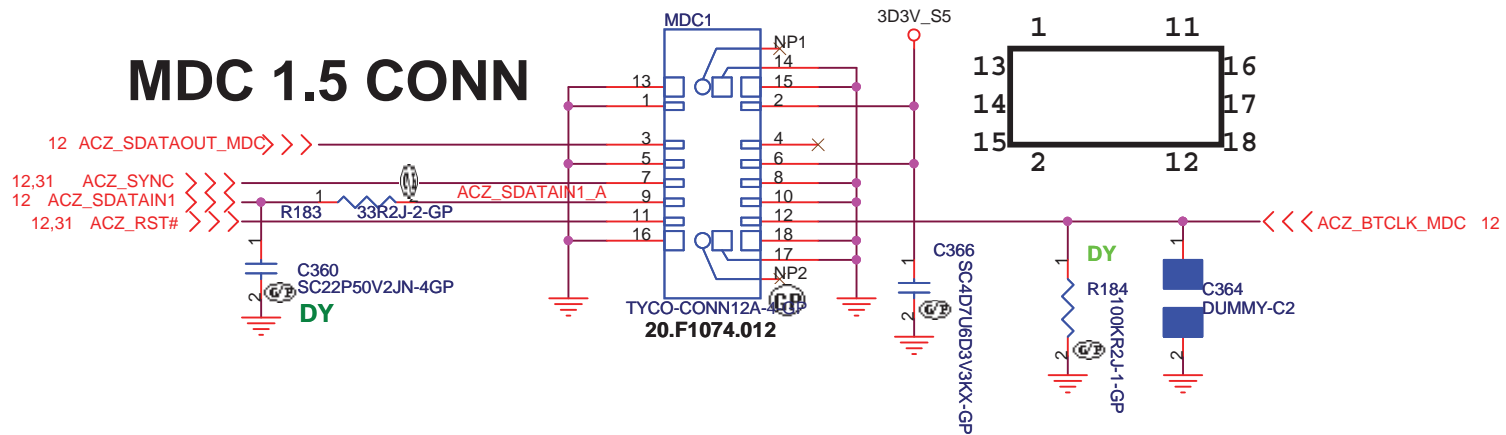
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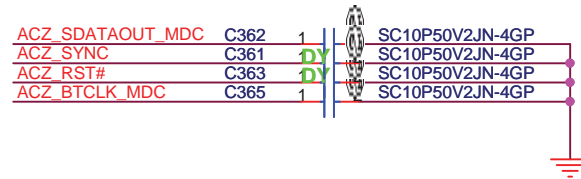
緯創資通 Wistron Corporation
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| Title AUDIO JACK | | |
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MDC 1.5 CONN



090211 -1 EMI
Stuff C362,C365 (10P)

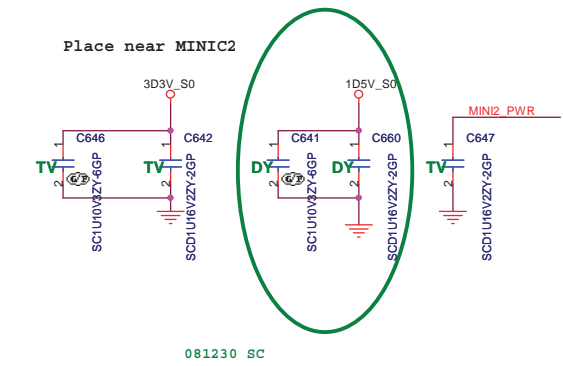
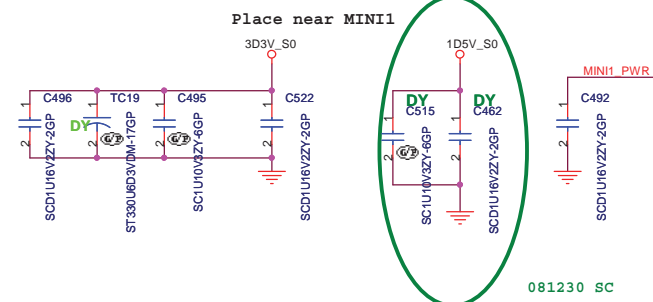
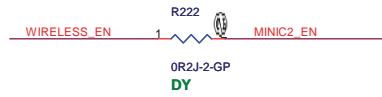
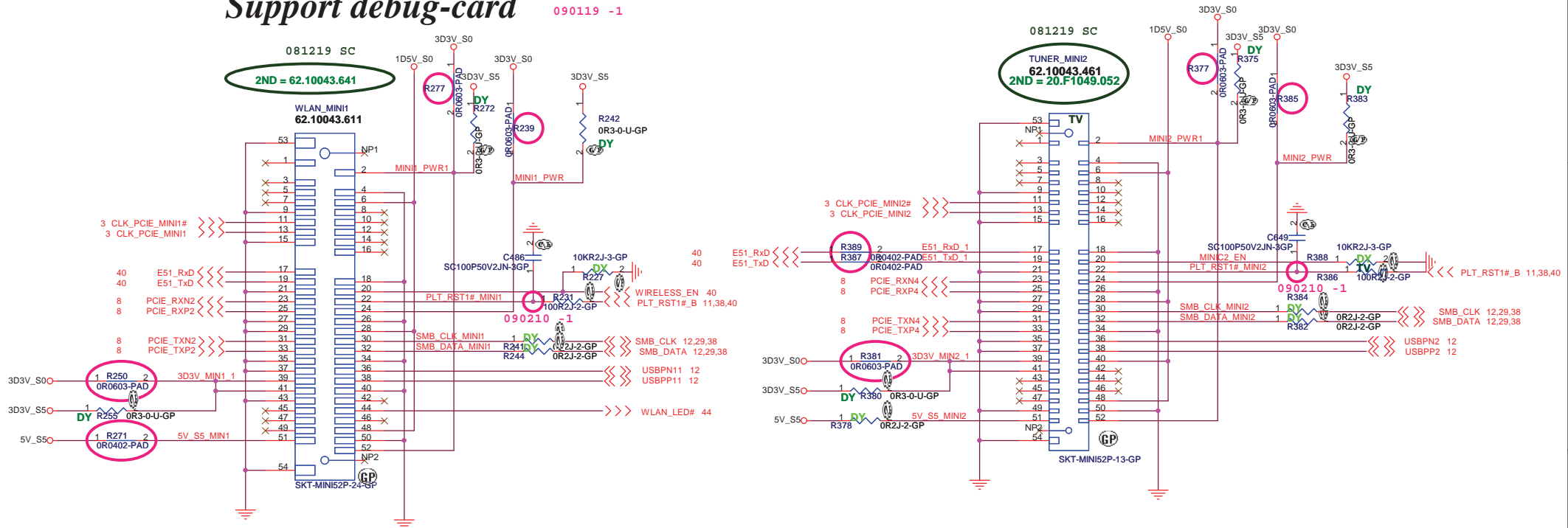


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|  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | |
| MDC | |
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Mini2 Card Connector(TV tuner)

Mini1 Card Connector(WLAN) Support debug-card 090119 -1



<Core Design>

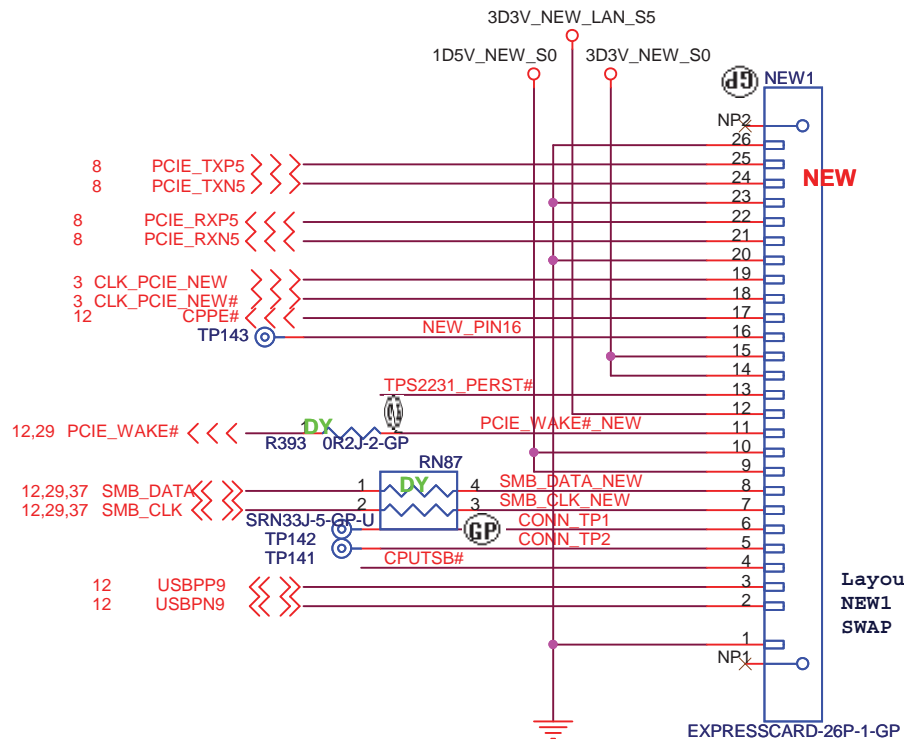
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Mini Card**

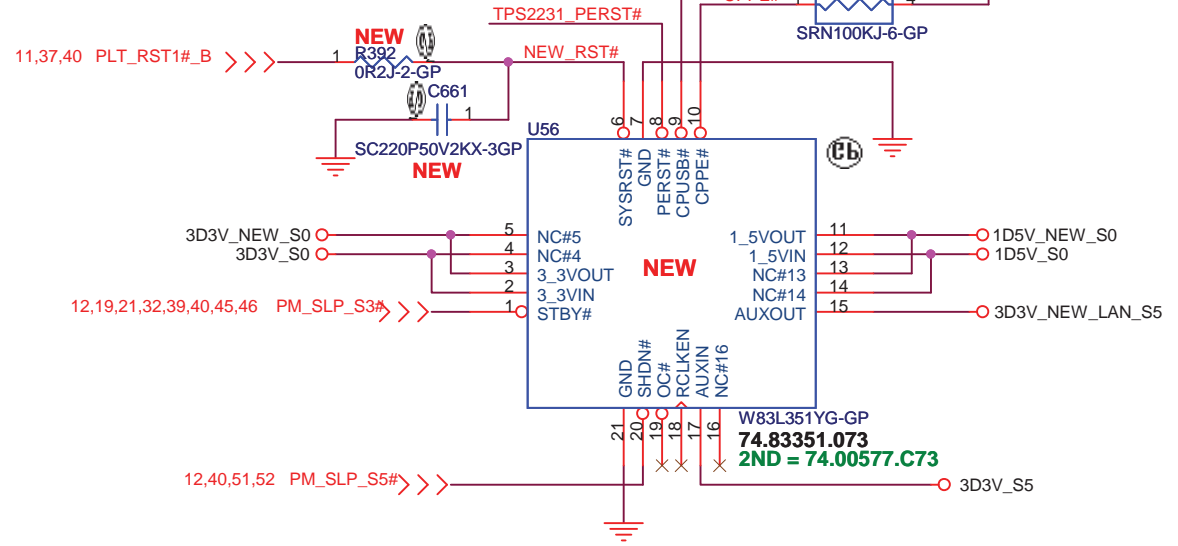
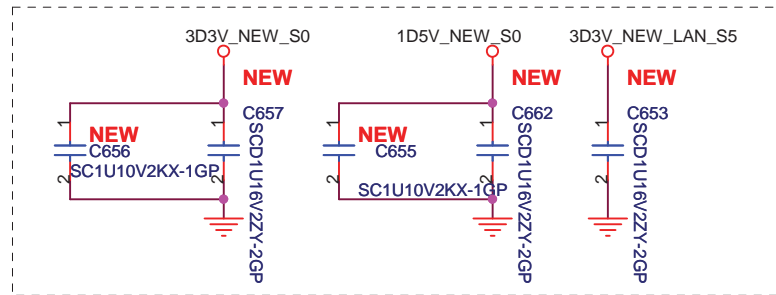
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NEWCARD Connector

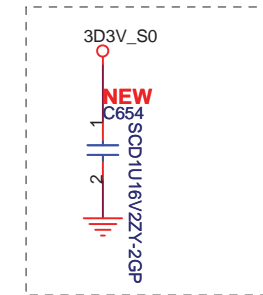
ENG stage without NEW card function 12/22



TOP VIEW



Place them Near to Chip



74.00577.C73
new card power switch
GMT cost down solution

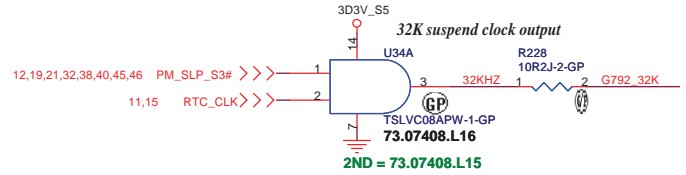
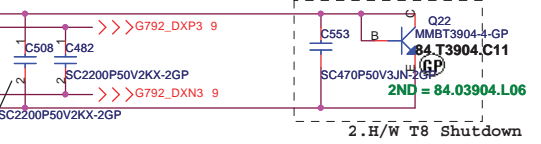
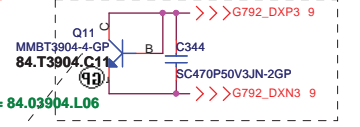
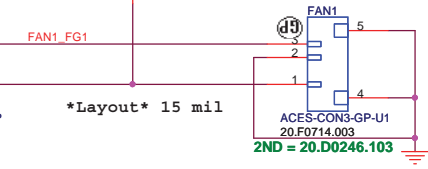
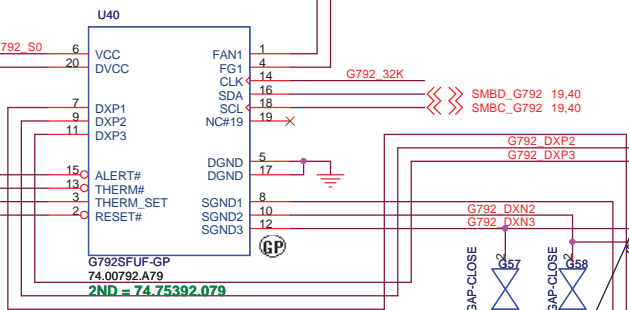
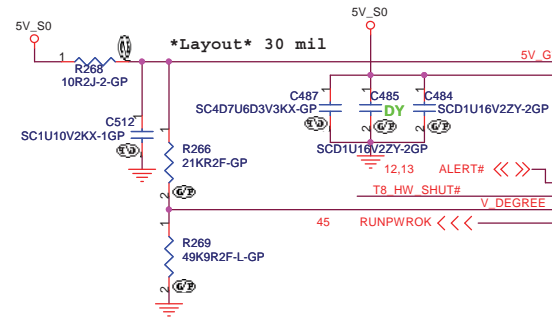
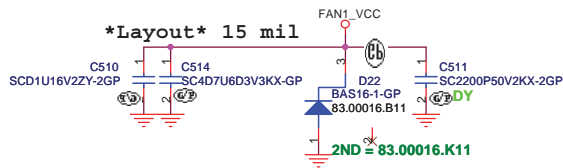
Layout Request 1226
NEW1 & NEW2
SWAP 1st & 2nd

62.10081.151 081219 SC
2ND = 62.10081.131

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| | | |
|--------------------------------|-----------------------------------|------------------|
| Title NEW CARD | | |
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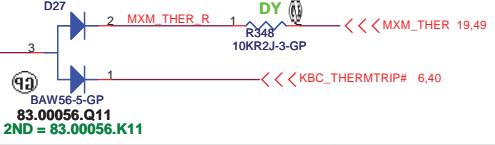
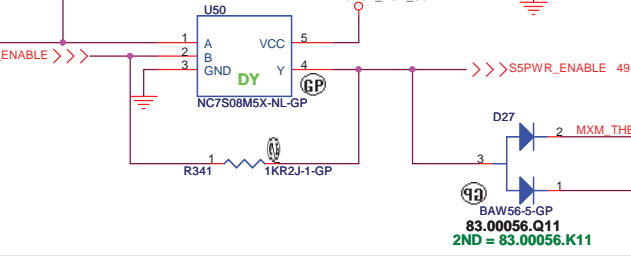
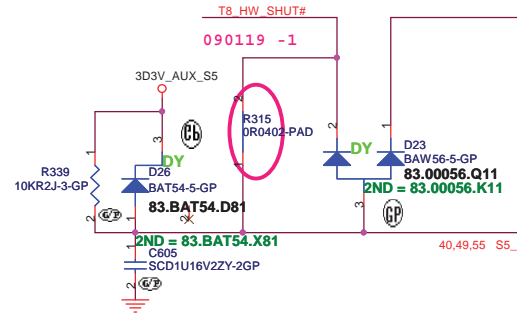
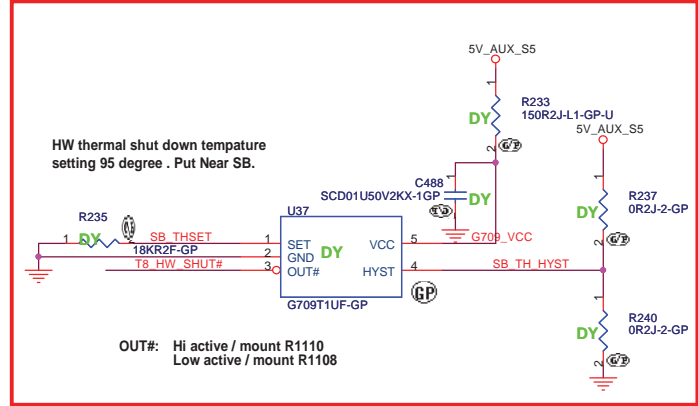
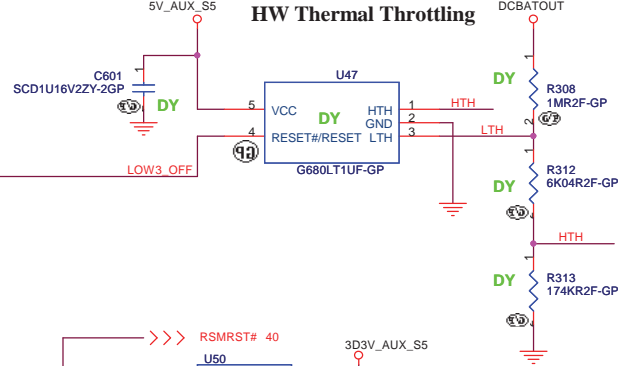


DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

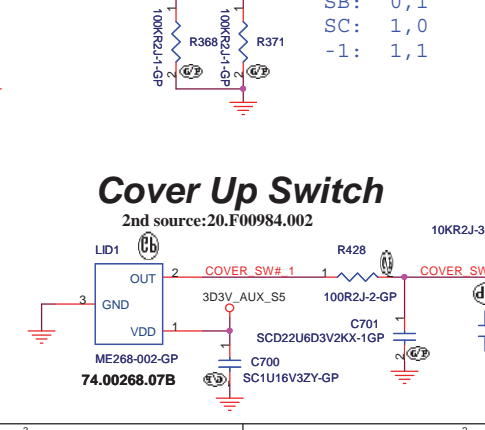
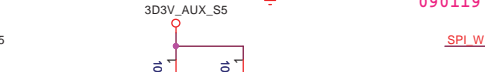
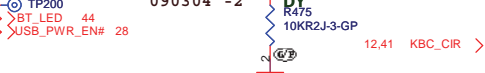
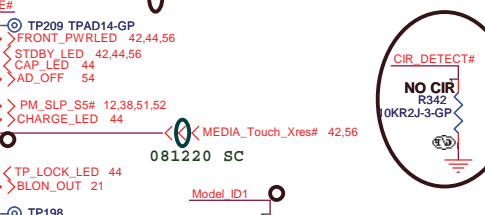
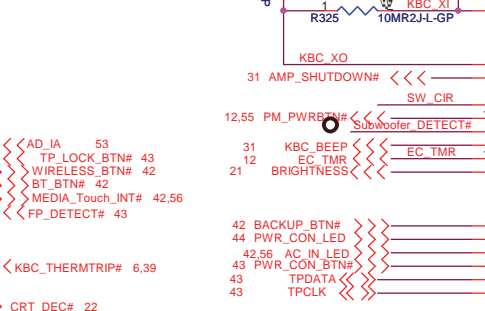
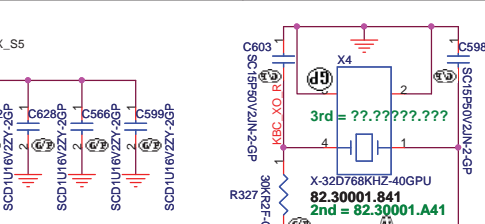
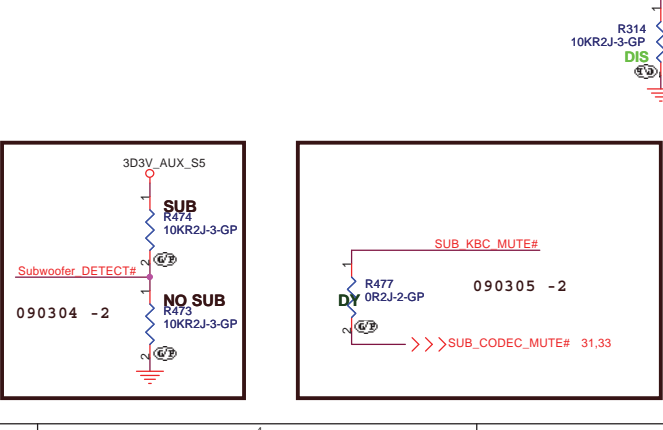
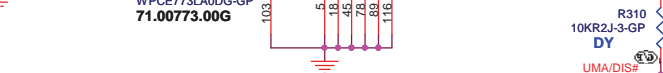
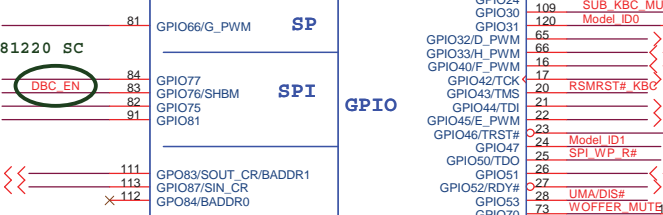
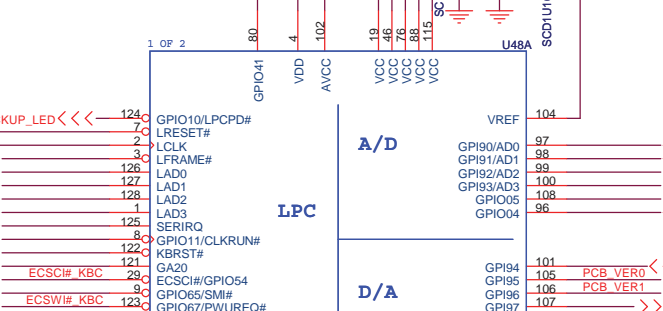
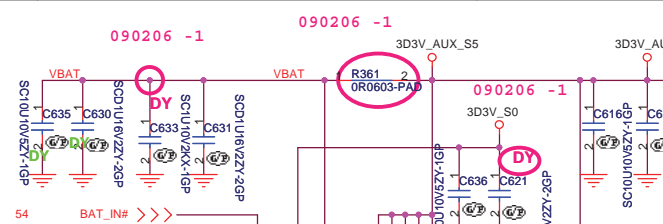
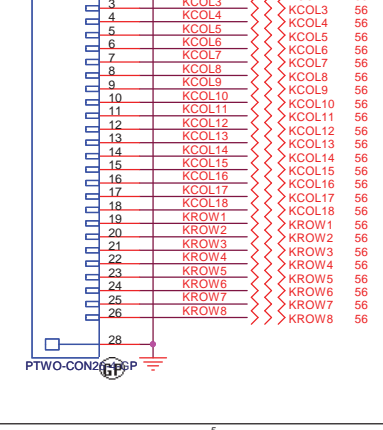
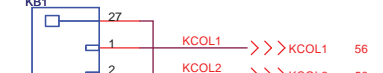
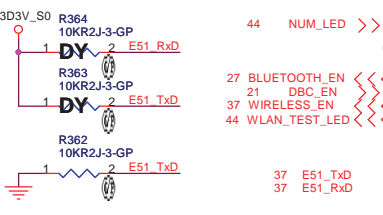
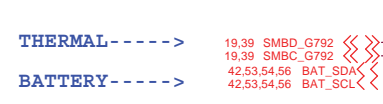
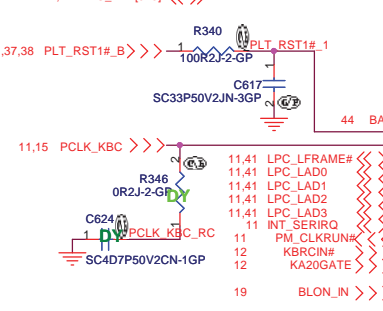
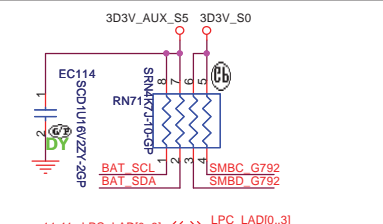
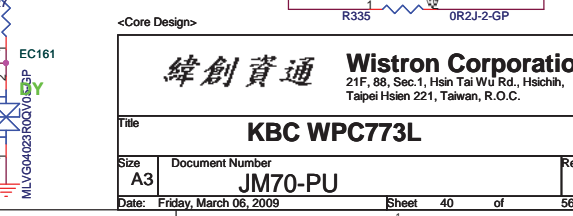
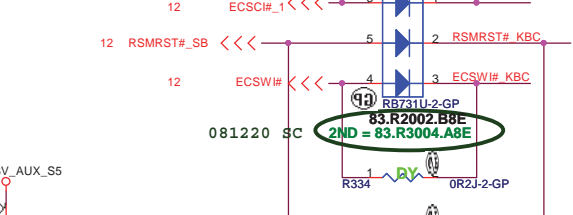
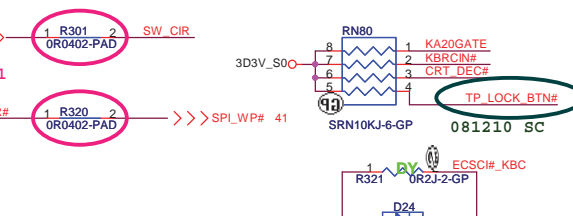
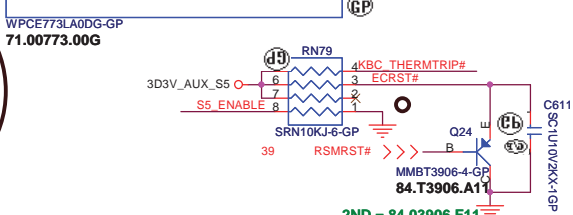
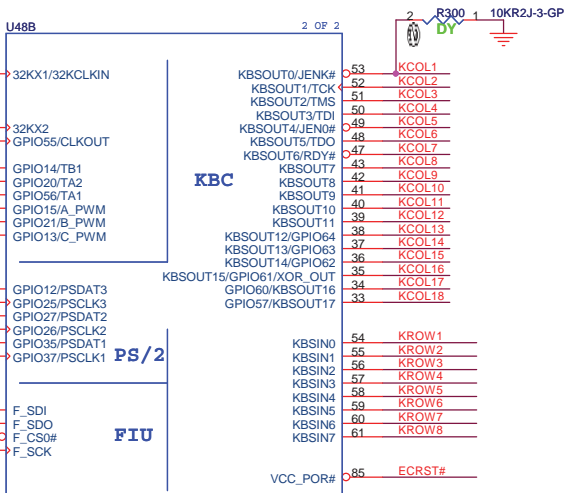
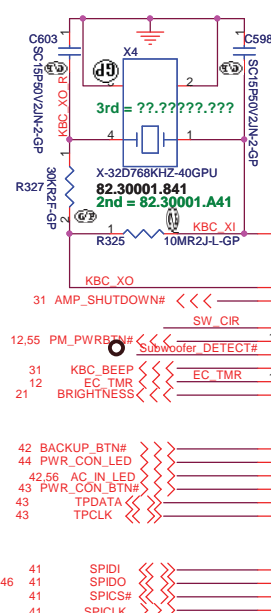
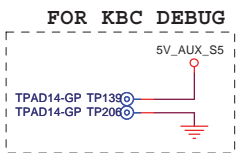
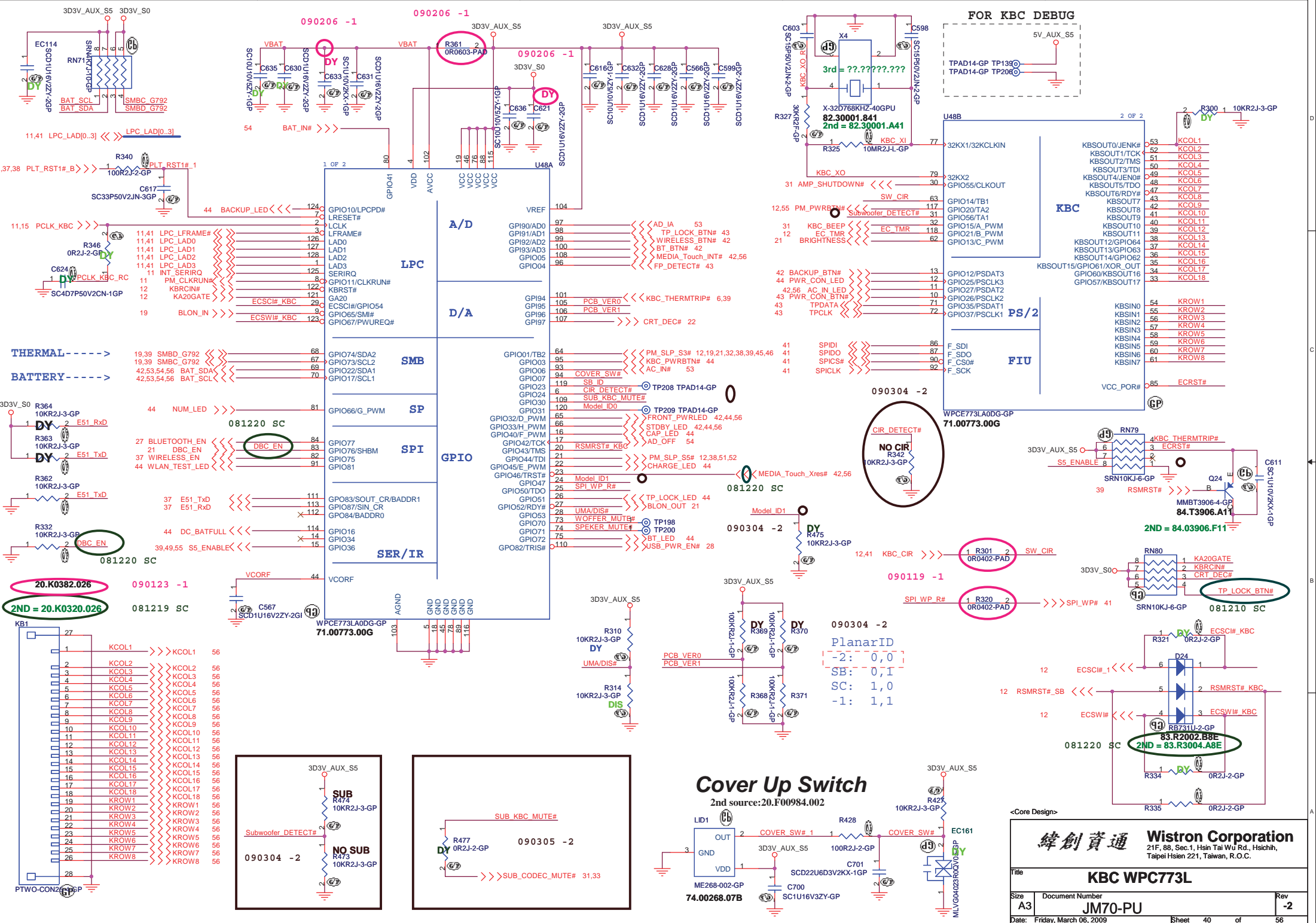
BL3#

HW Thermal Throttling



<Core Design>

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| G792 | | | |
| Title | | | |
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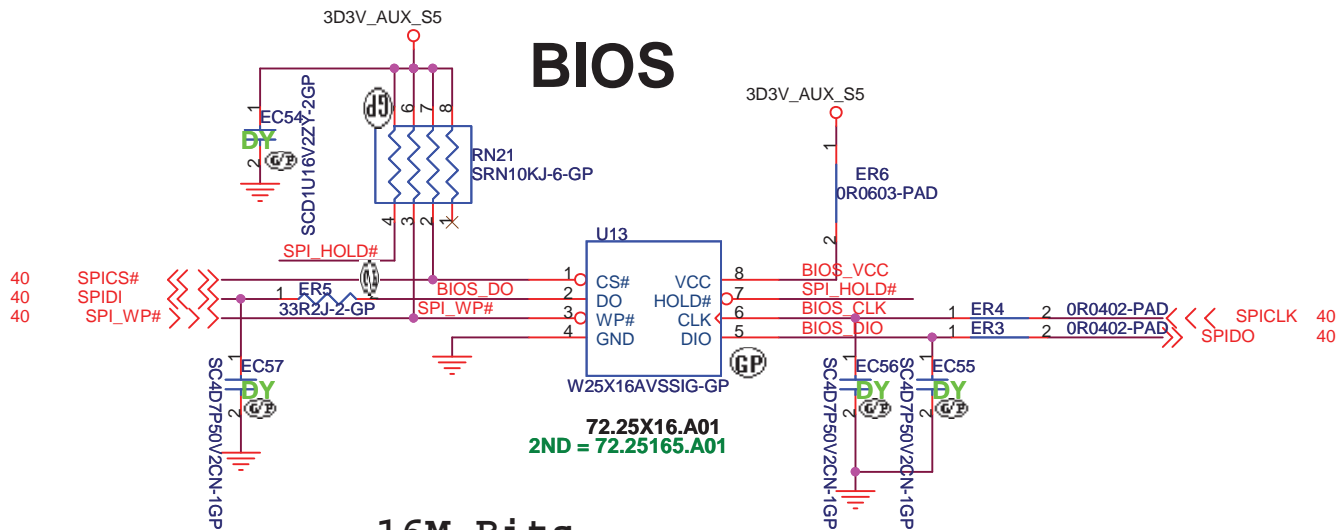


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KBC WPC773L

File: JM70-PU
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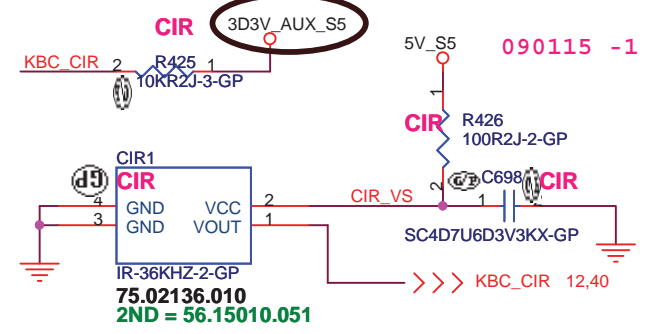
BIOS



16M Bits
SPI FLASH ROM

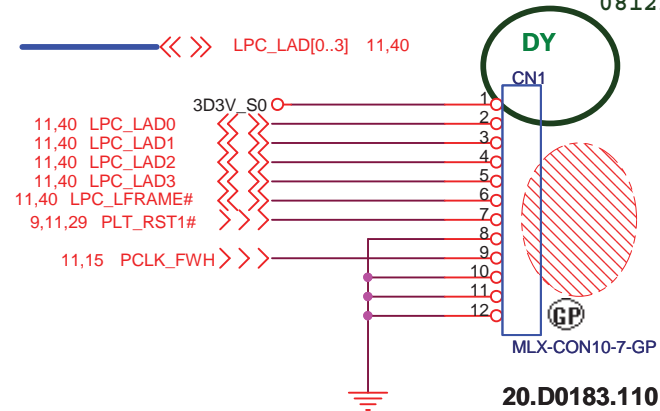
CIR Module

090304 -2




GOLDEN FINGER FOR DEBUG BOARD

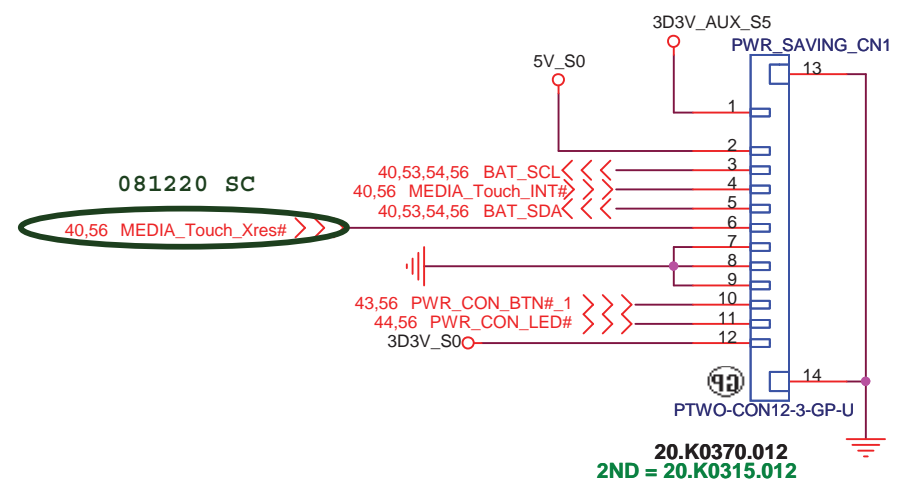
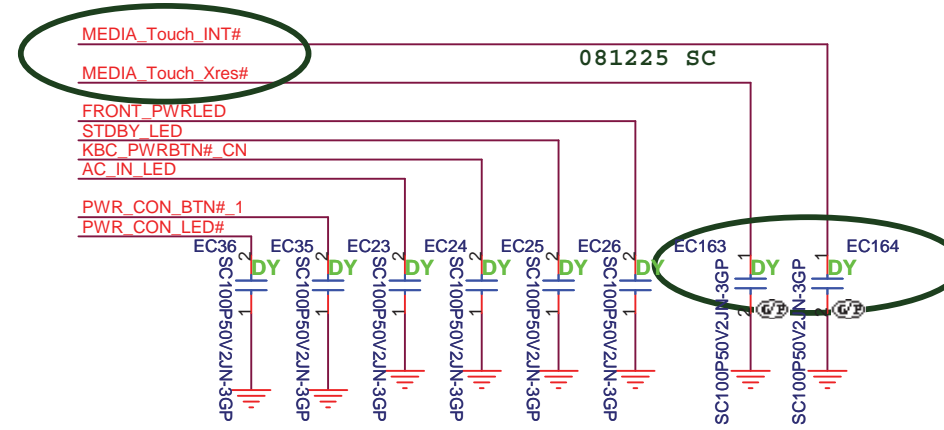
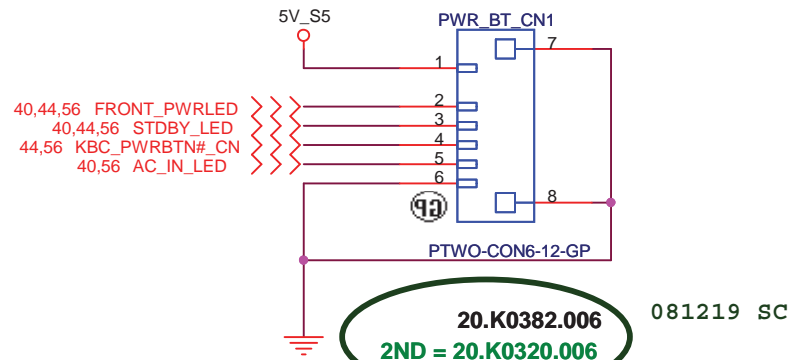
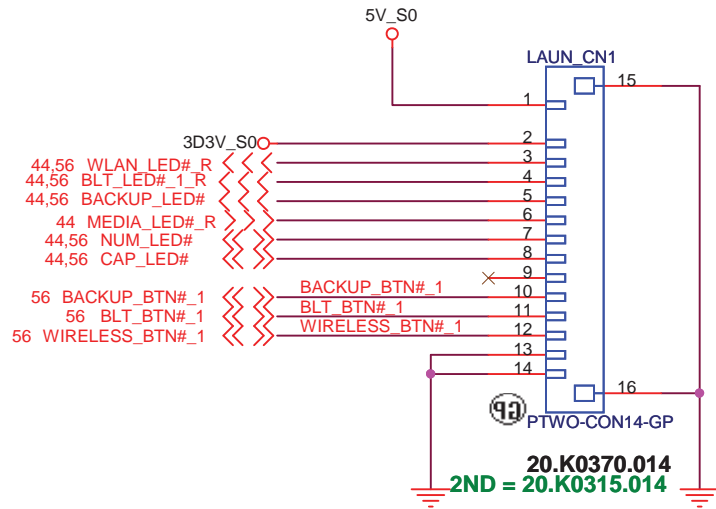
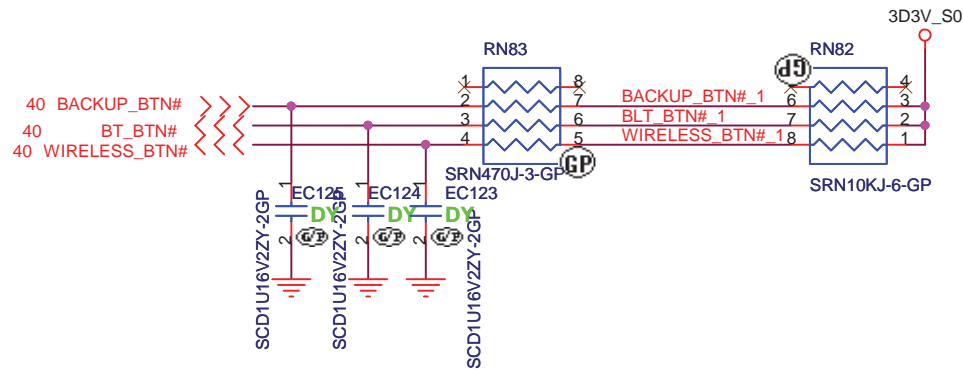
081225 SC




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| BIOS & CIR | | |
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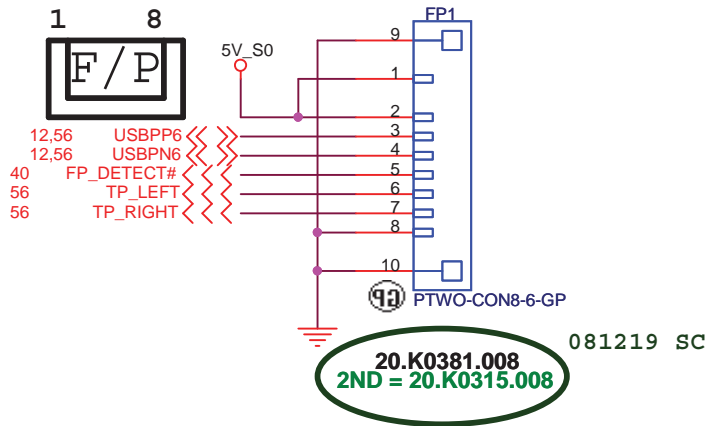
LAUNCH



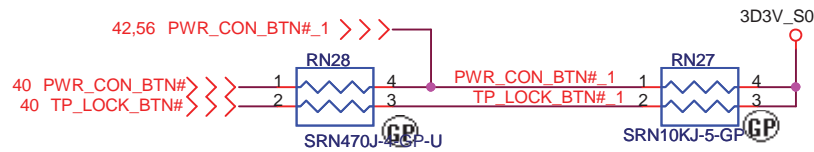
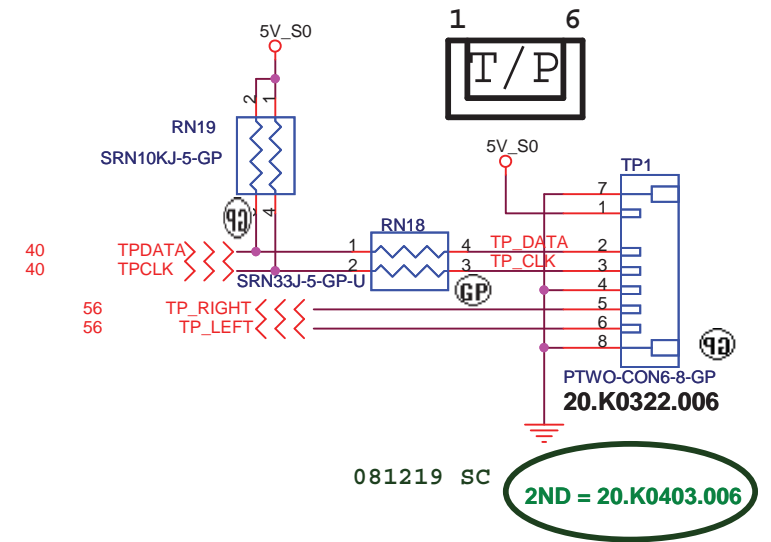
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| LAUNCH & LID | |
| Title LAUNCH & LID | Date: Friday, March 06, 2009 |
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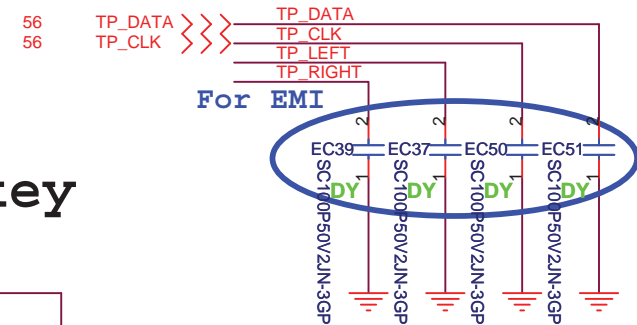
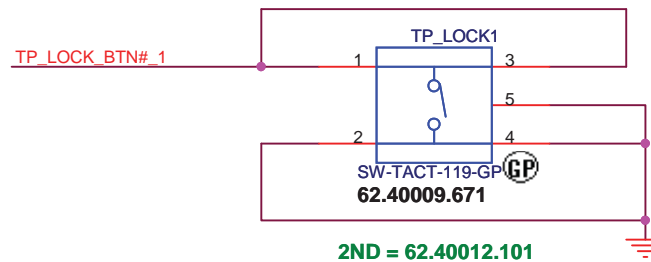
Finger printer



TOUCH PAD



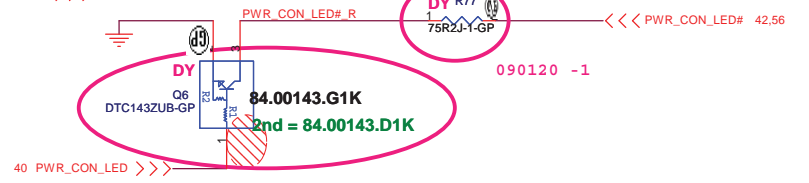
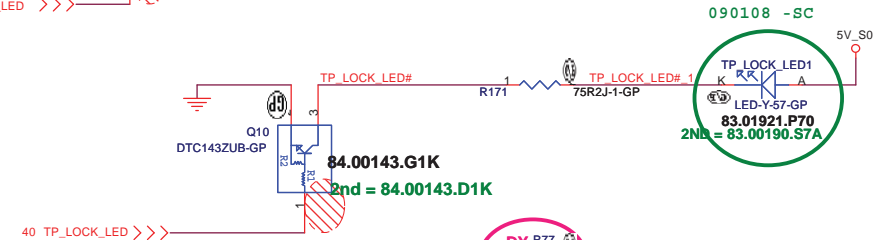
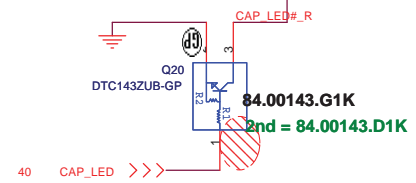
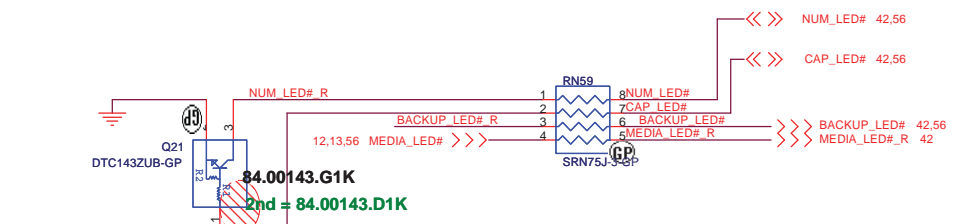
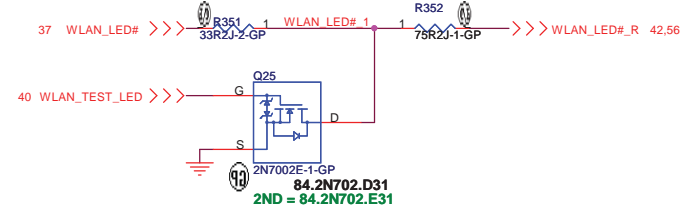
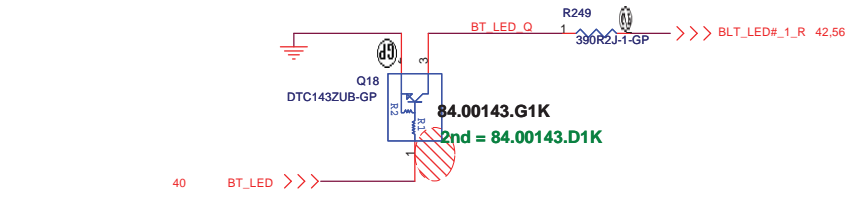
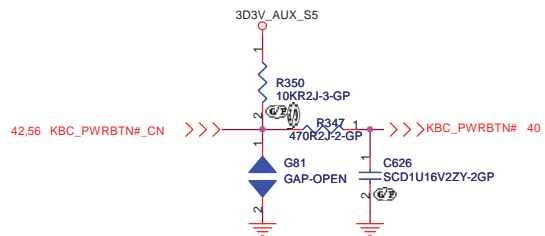
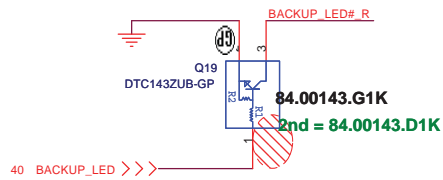
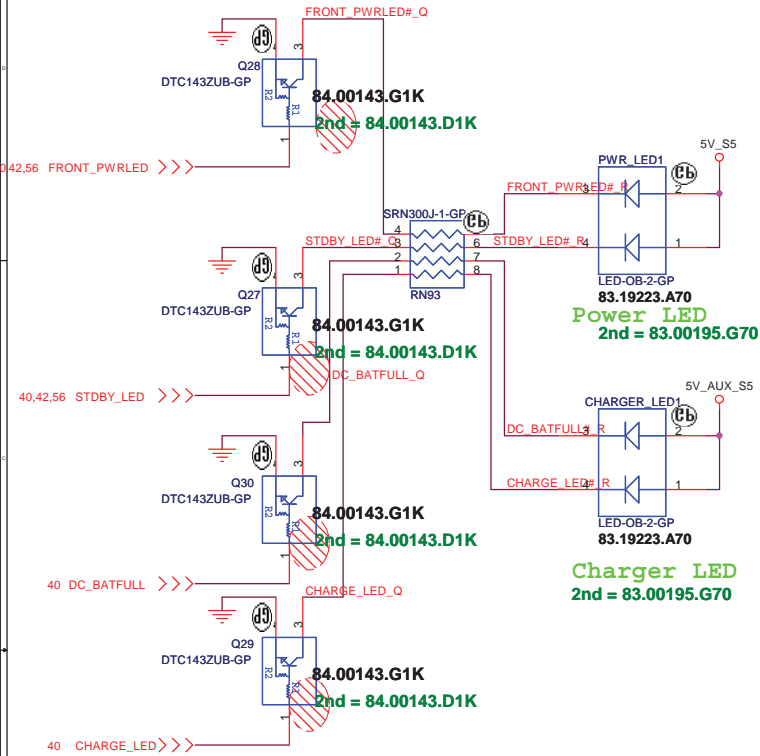
TP_LOCK key



<Core Design>

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| Title | | | |
| Finger Printer | | | |
| Size | Document Number | Rev | |
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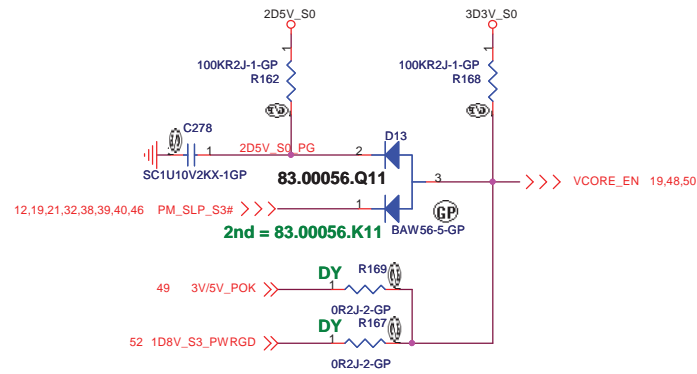
LED



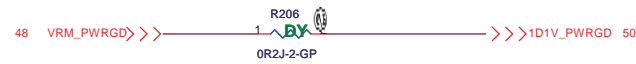
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Title: LED & LAUNCH

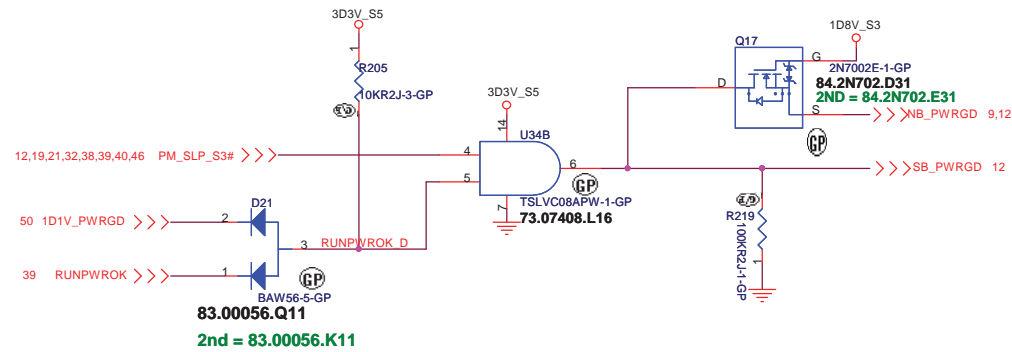
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P/H @ 1D8V_S3 PAGE

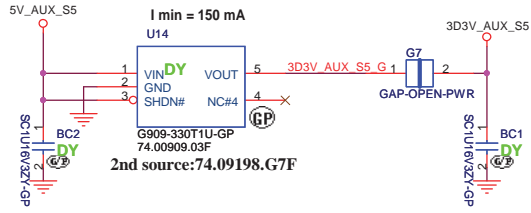


Reference schematic recommend

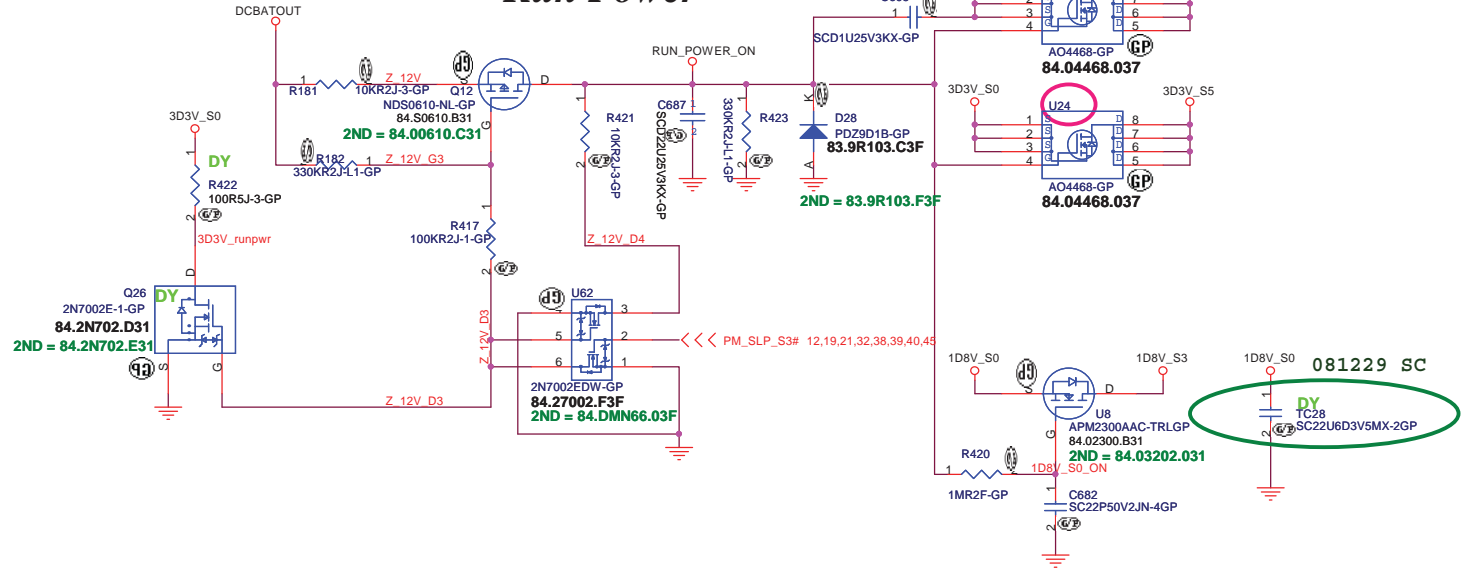


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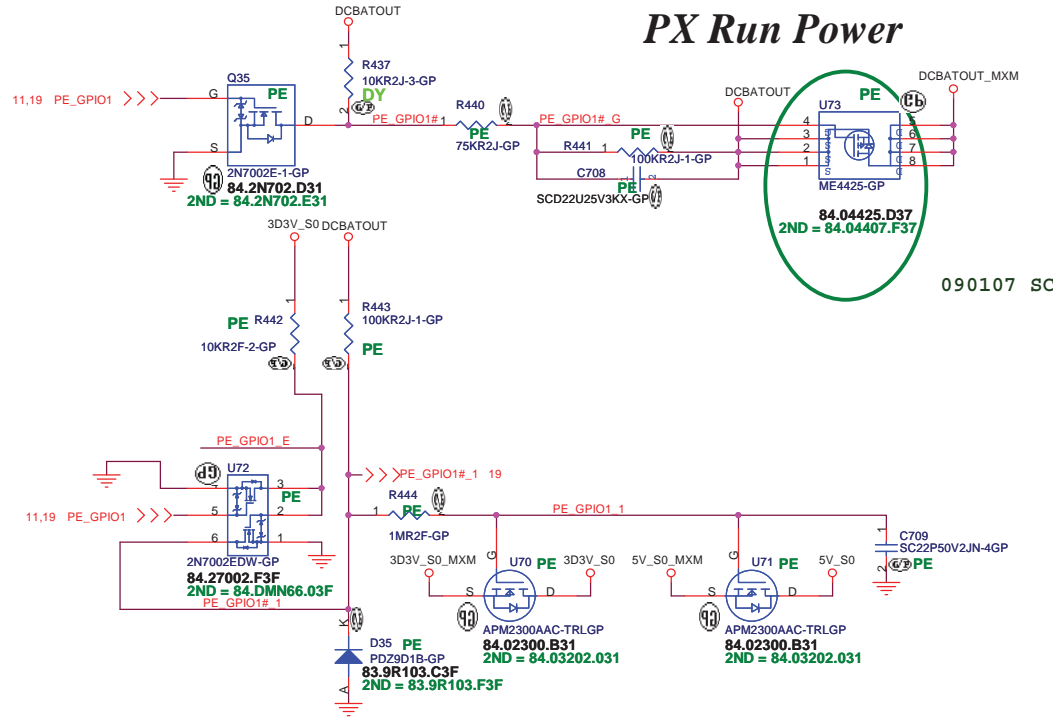
Aux Power 3D3V_AUX_S5



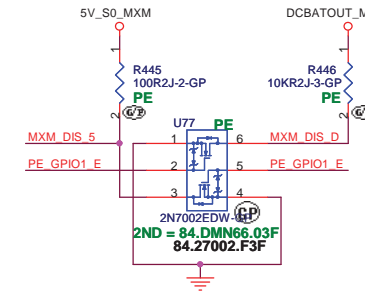
Run Power



PX Run Power

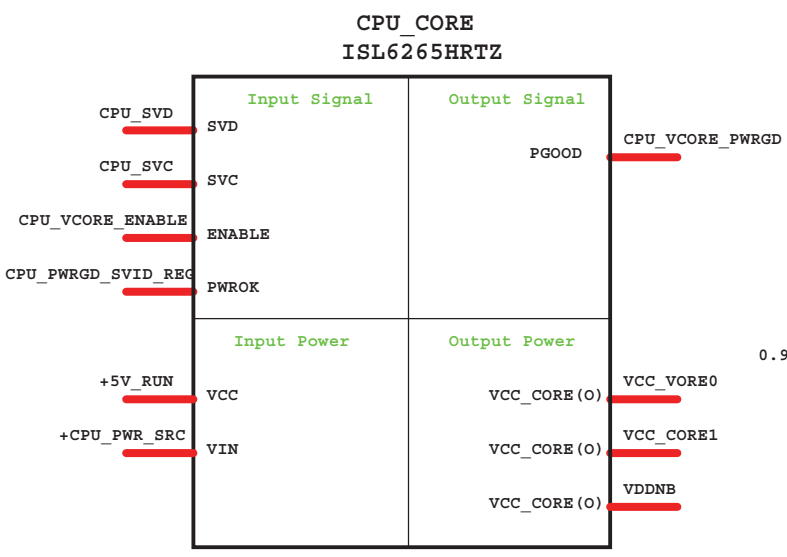
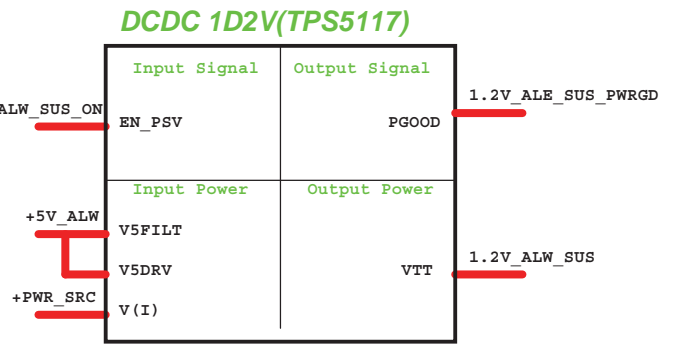
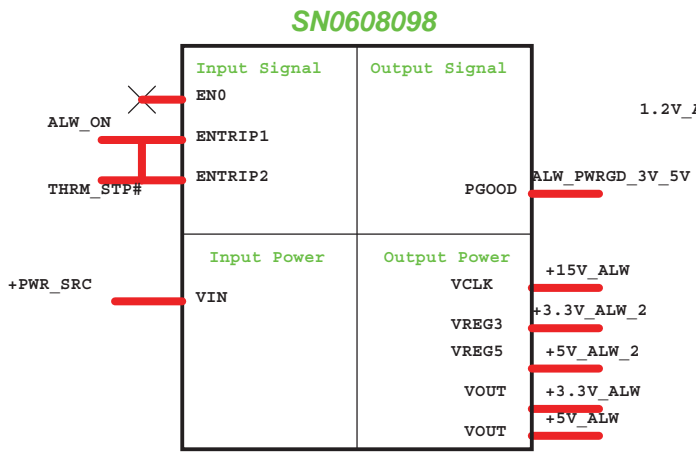
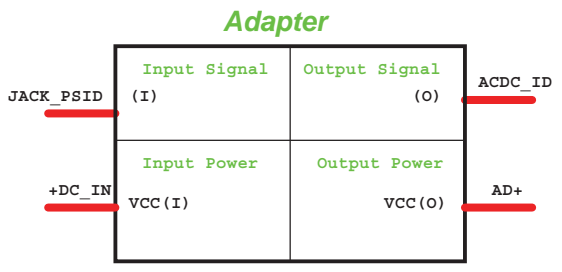


PX Run Power Discharge circuit

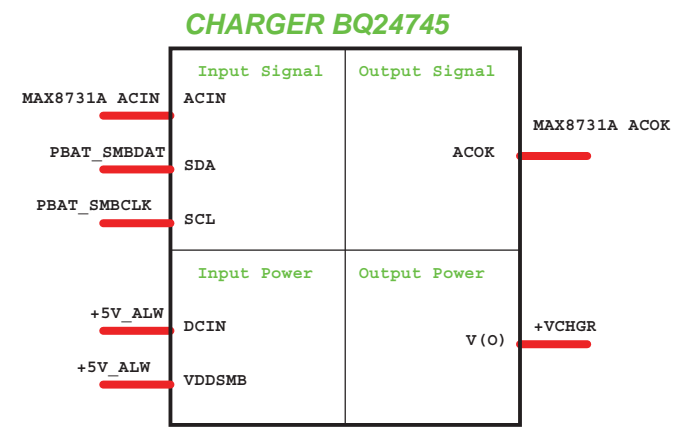
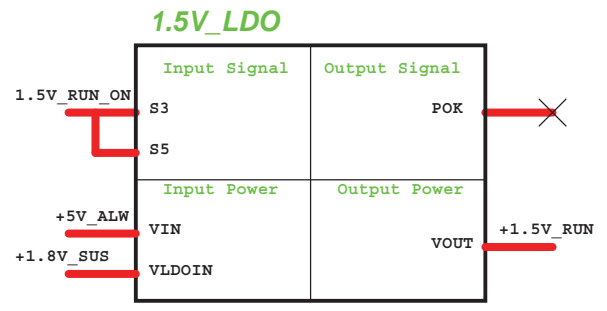
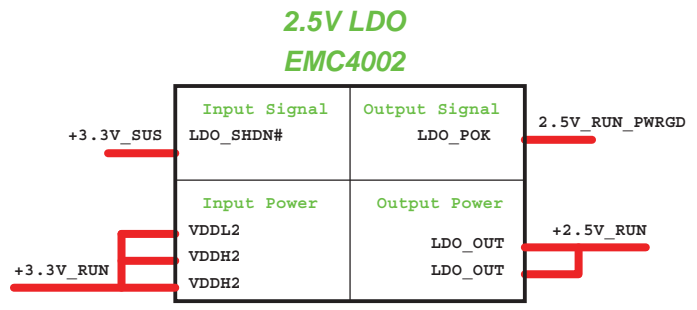
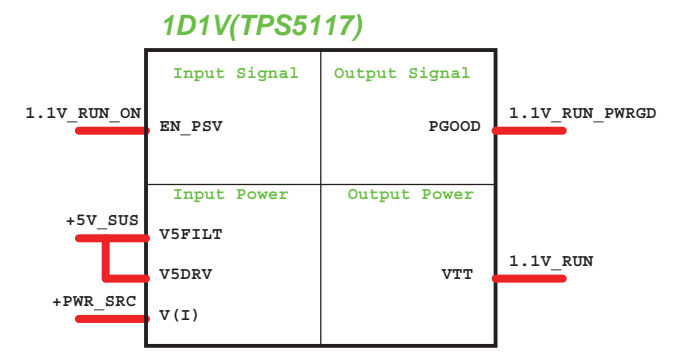
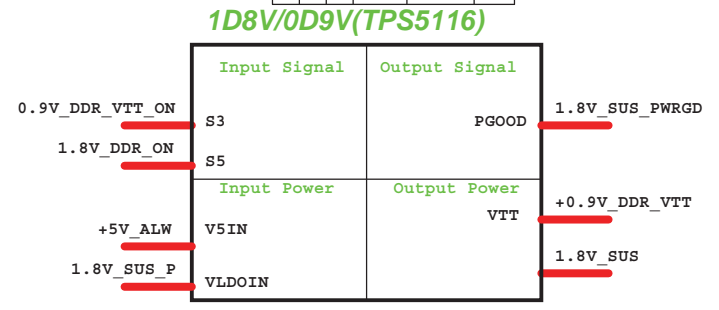


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|---|------------------------|----------------------------|----------|
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| RUN POWER and 3D3V_AUX_S5 | | | |
| Size | Document Number | Rev | |
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| | S3 | S5 | VDDQ | VTTREF | VTT |
|----|----|----|------|--------|-----|
| S0 | 1 | 1 | 1 | 1 | 1 |
| S3 | 1 | 1 | 1 | 1 | 1 |
| S4 | 0 | 0 | 0 | 0 | 0 |
| S5 | 0 | 0 | 0 | 0 | 0 |

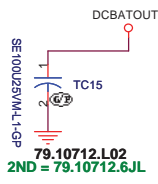


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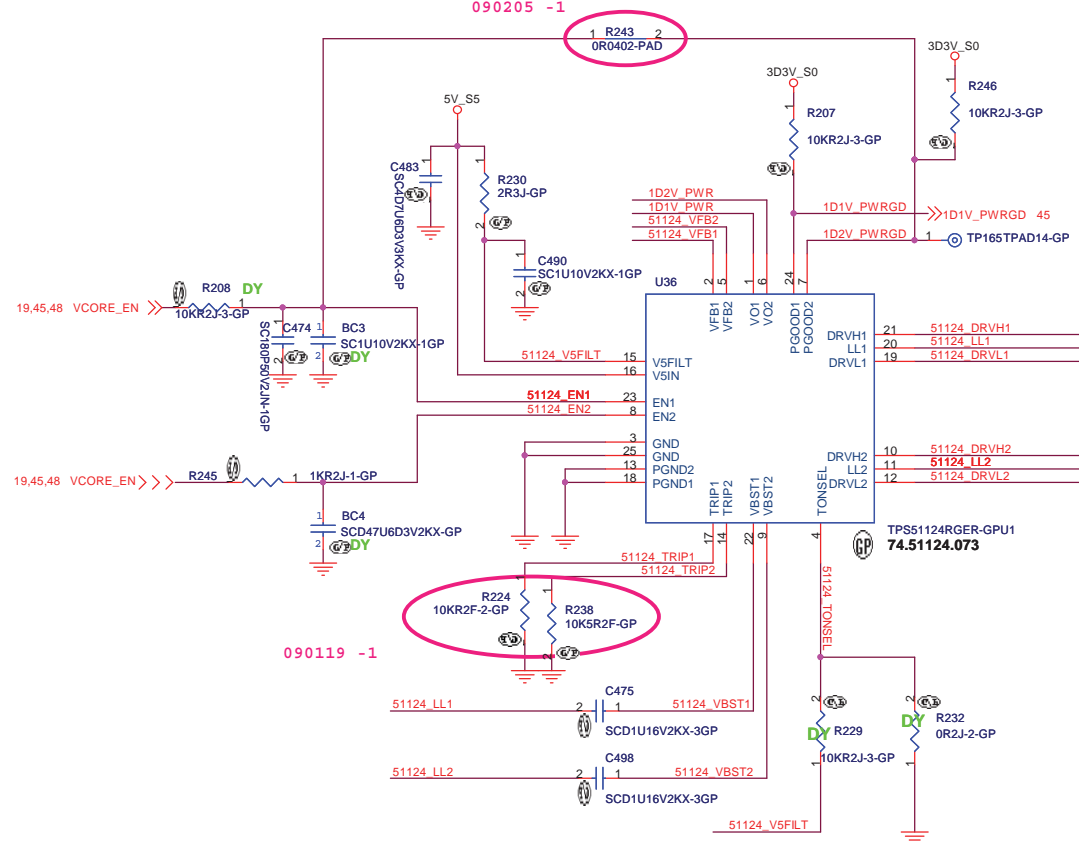
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Title: **Power Block Diagram**

| | | |
|------------------------------|---------------------------------|---------|
| Size: A3 | Document Number: JM70-PU | Rev: -2 |
| Date: Monday, March 02, 2009 | Sheet: 47 of 56 | |

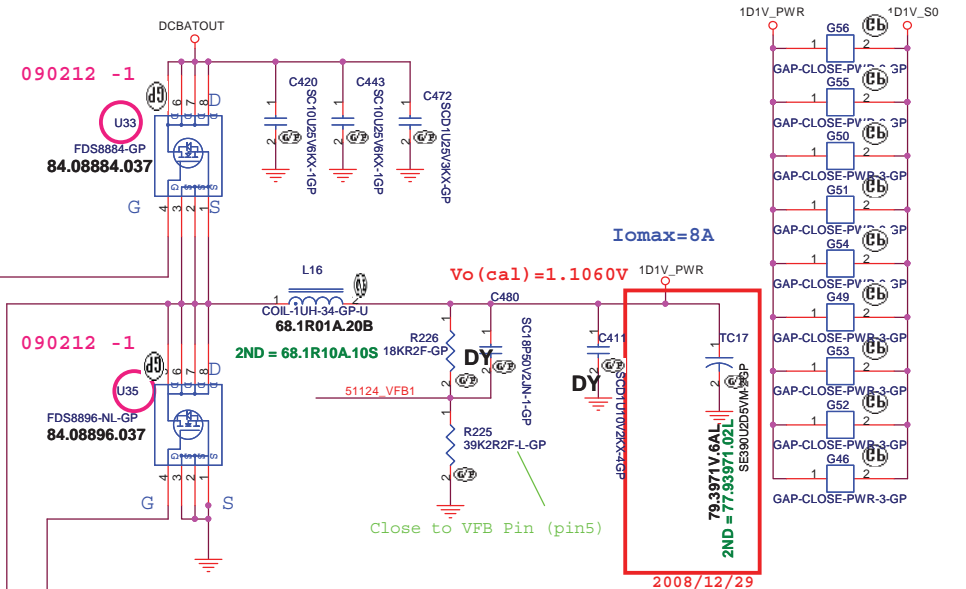


$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$
 $I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * E)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$

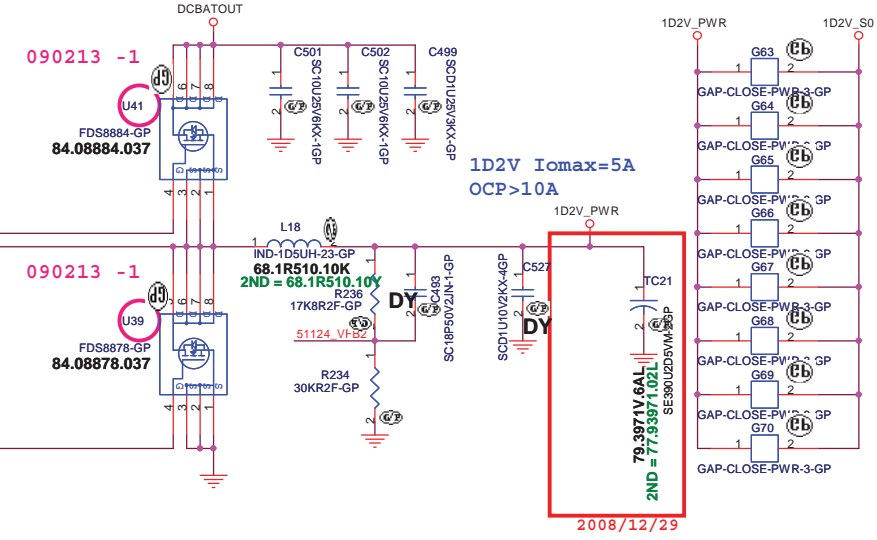


| | GND | OPEN | V5FILT |
|--------|----------------------|----------------------|----------------------|
| TONSEL | 240k/CH1 300k/CH2 | 300k/CH1 360k/CH2 | 360k/CH1 420k/CH2 |

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode



20080307_Modify by
Brian
ACOUSTIC NIOSE



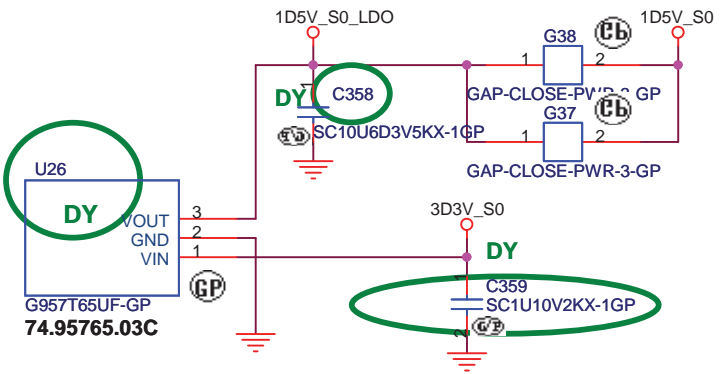
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 Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|-------|------------------------|-------|--------------------|
| Title | | | TPS51124 1D1V 1D2V |
| Size | Document Number | Rev | |
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| Date: | Friday, March 06, 2009 | Sheet | 50 of 56 |

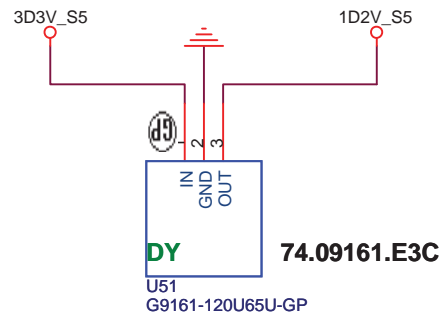
G957

1D5V_S0
Iomax=1A

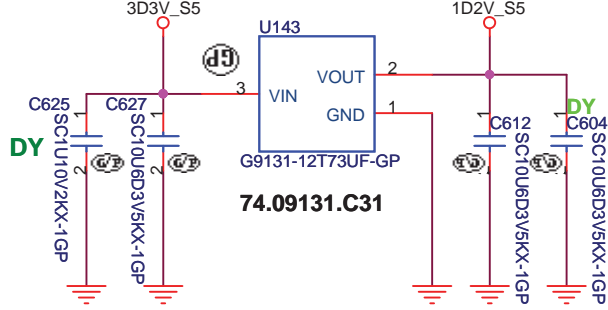


081230 SC

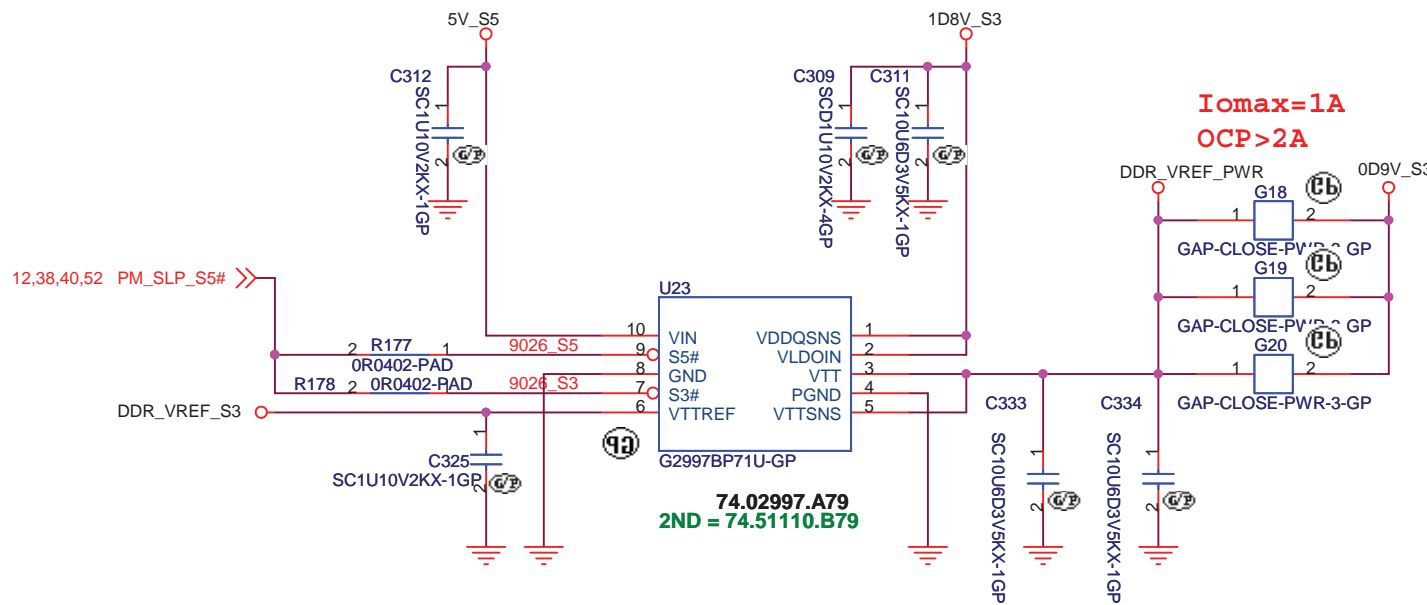
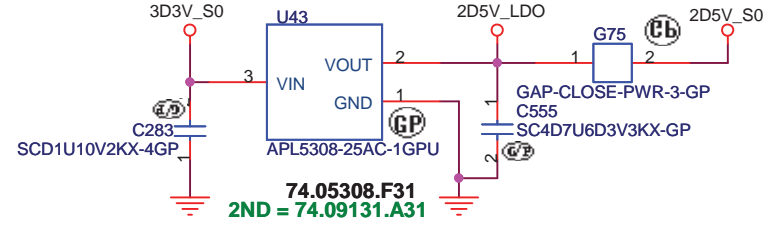
1D2V_S5
Iomax=400mA



Place near to SB700



2D5V_S0
Iomax=0.3A 2D5V/300mA

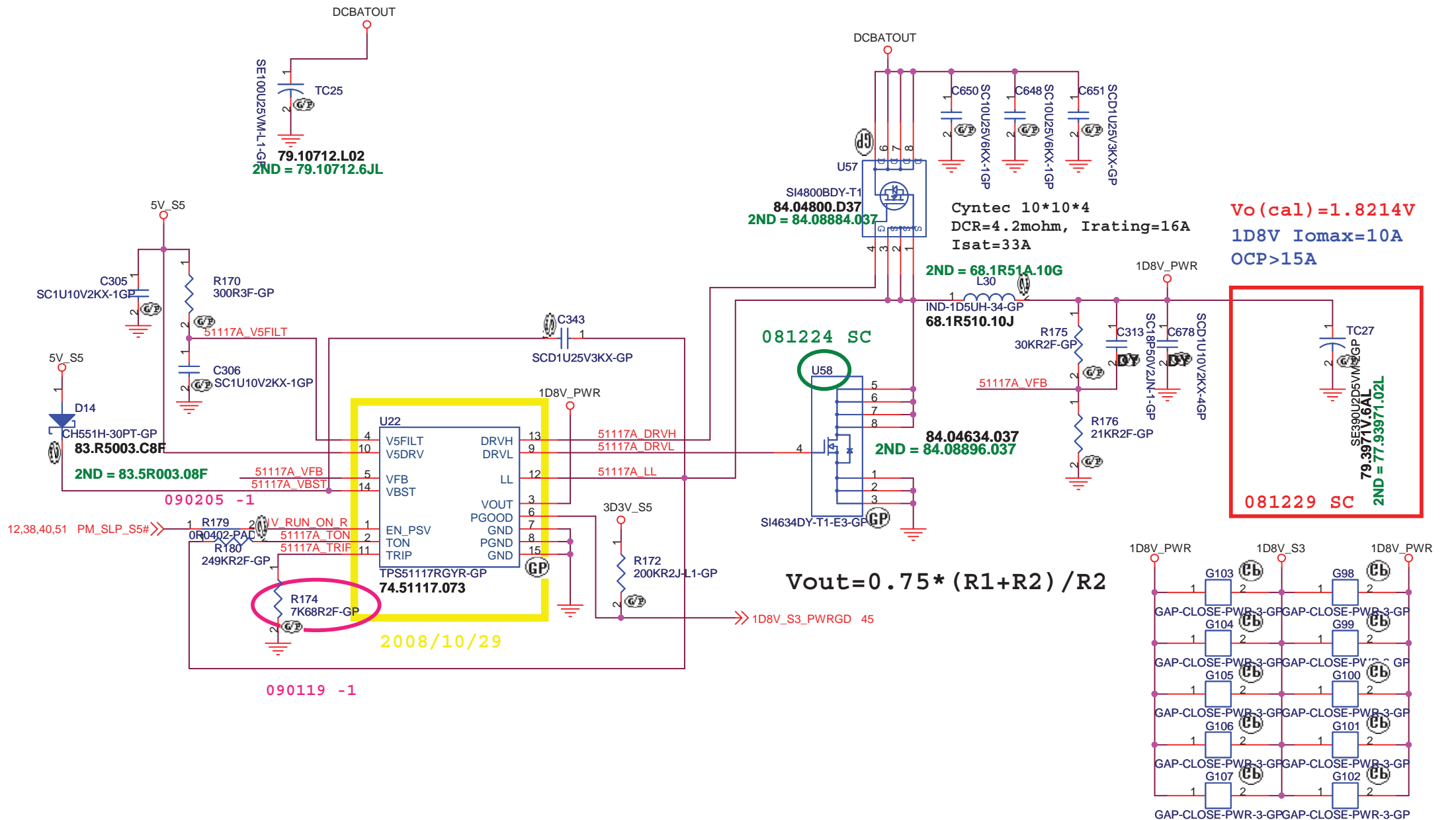


Iomax=1A
OCP>2A

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| | | |
|---|------------------------|----------------|
| Title | | |
| 0D9V&2D5V&1D25V&1D5V | | |
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SE100U25VM-L1-G
TC25
79.10712.L02
2ND = 79.10712.6JL

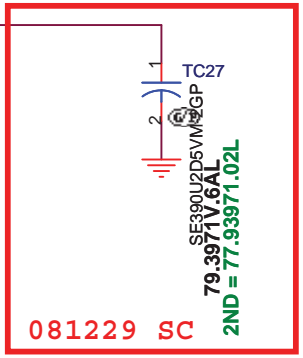
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037

Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A

Vo(cal)=1.8214V
1D8V Iomax=10A
OCP>15A

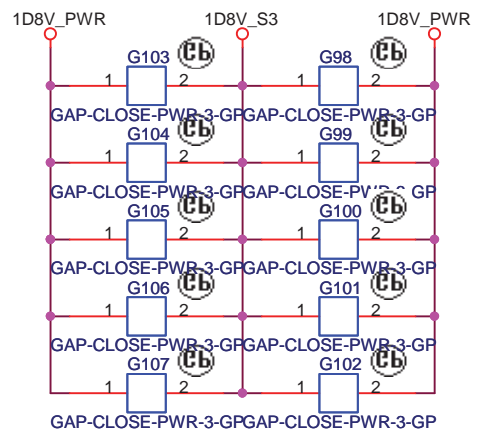
081224 SC
U58

2ND = 68.1R51A.10G
L30
IND-1D5UH-34-GP
68.1R510.10J



SE390U25VM-L1-G
TC27
79.3971V.6AL
2ND = 77.93971.02L
081229 SC

$$V_{out} = 0.75 * (R1 + R2) / R2$$



12,38,40,51 PM_SLP_S5#

090205 -1

TPS5117R GYR-GP
74.51117.073

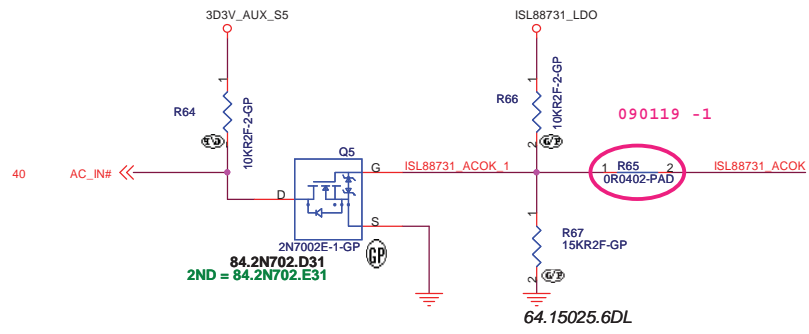
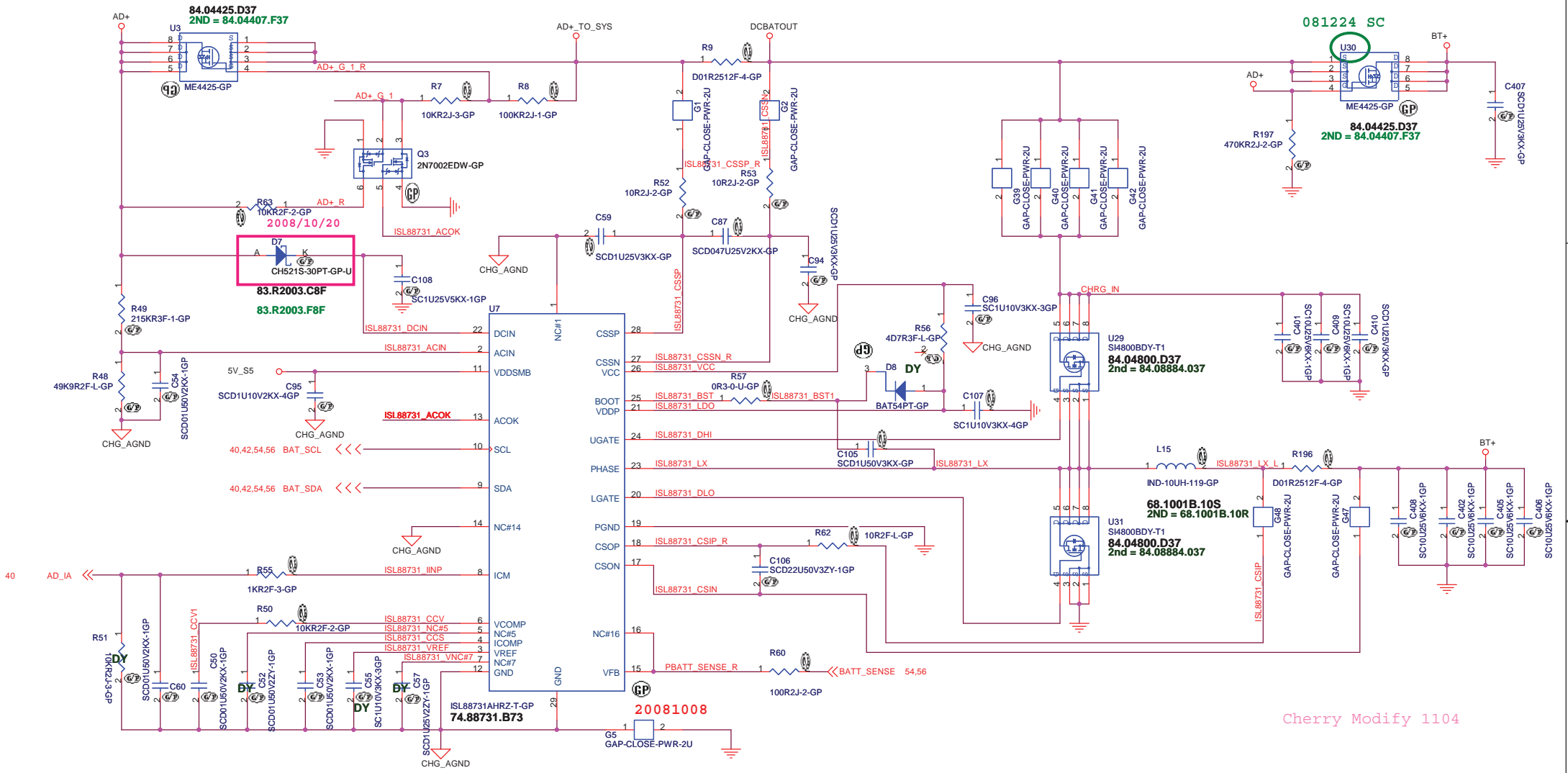
2008/10/29

090119 -1

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| | | |
|---------------|------------------------|----------------|
| Title | | |
| 1D8V(TPS5117) | | |
| Size | Document Number | Rev |
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Title: **ISL88731A Charger**

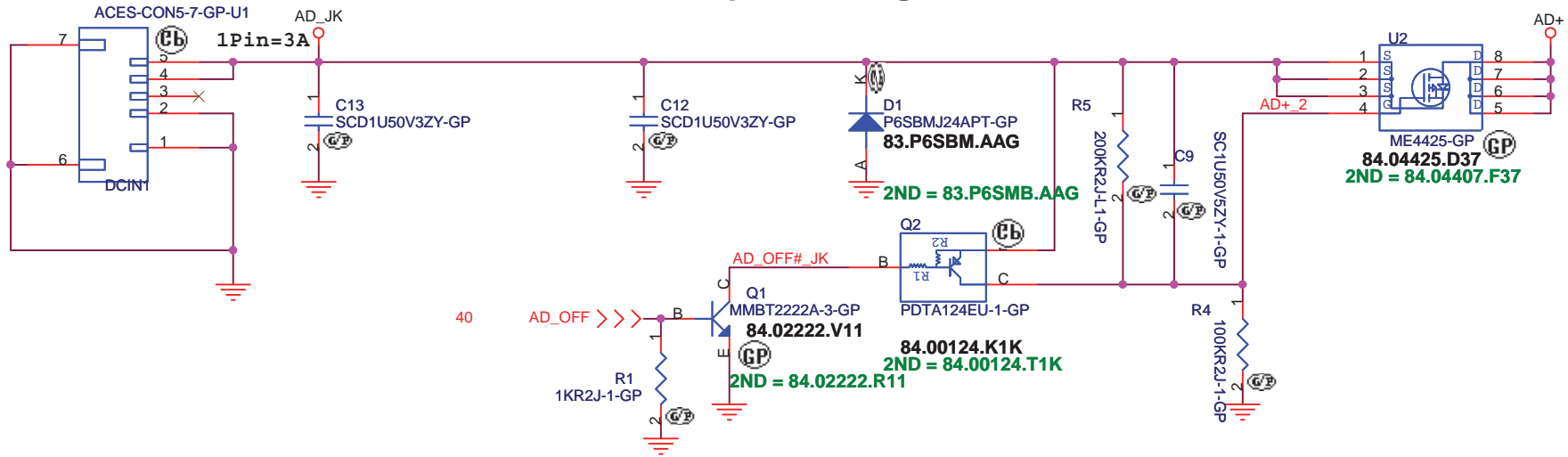
Size A3 Document Number: **JM70-PU** Rev: **-2**

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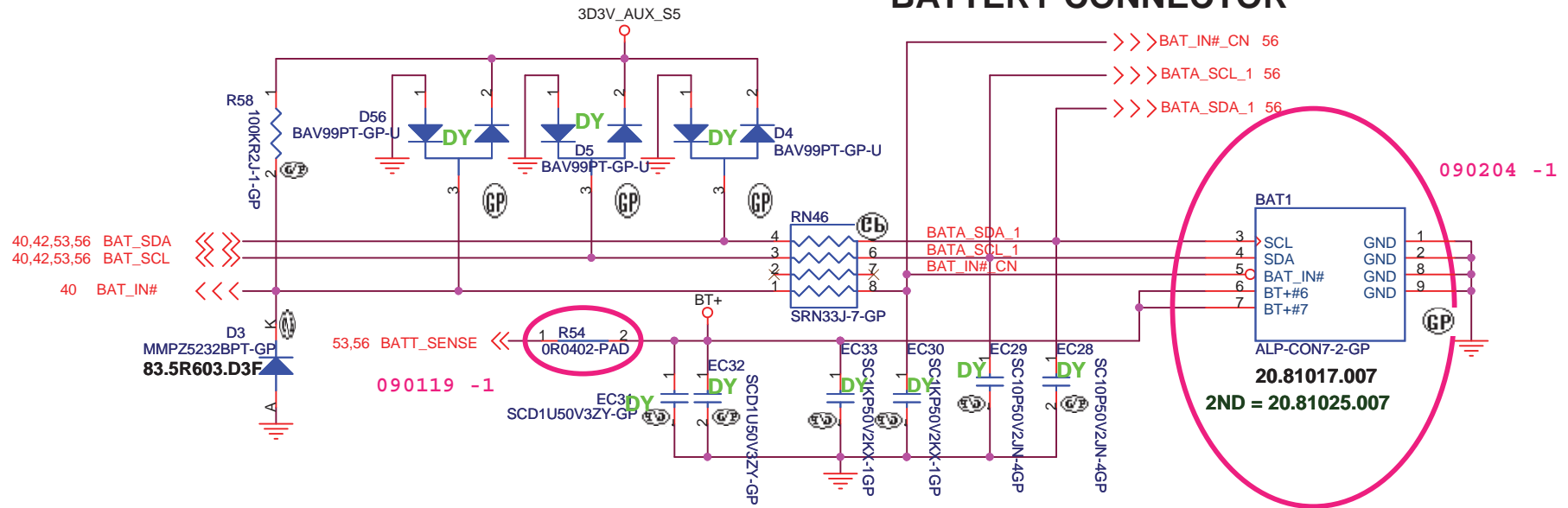
20.F1002.005

2ND = 20.F1170.005

Adaptor in to generate DCBATOUT



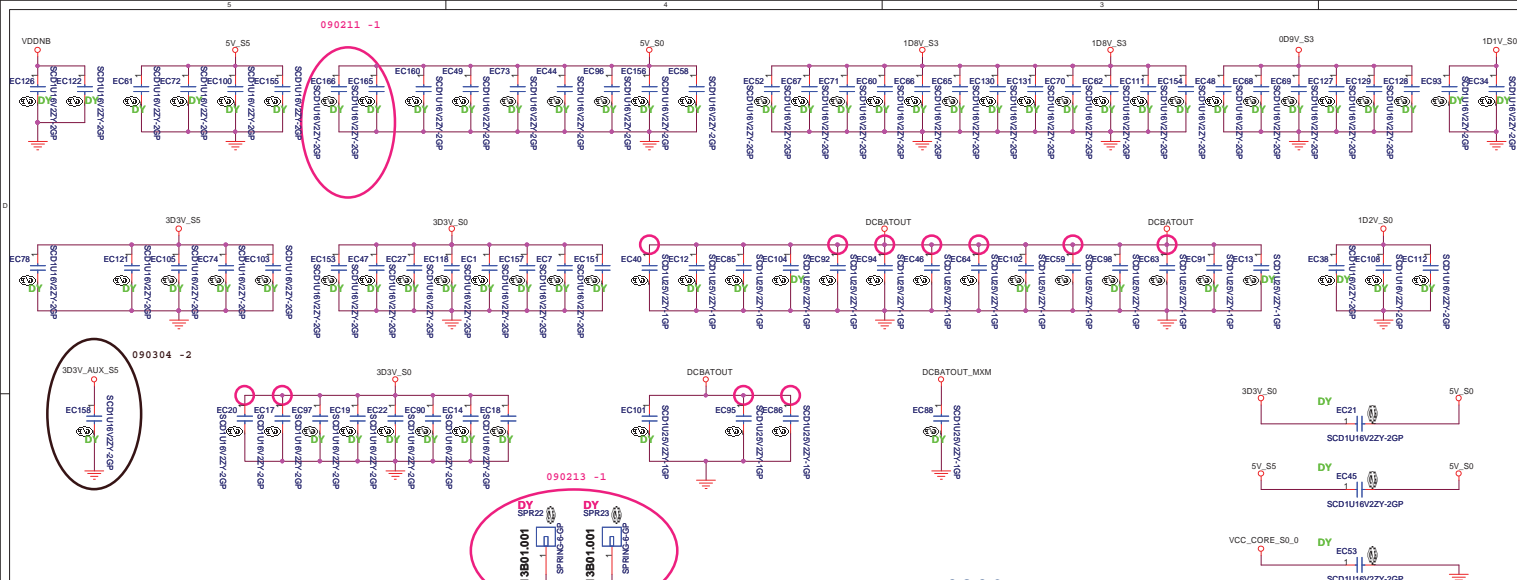
BATTERY CONNECTOR



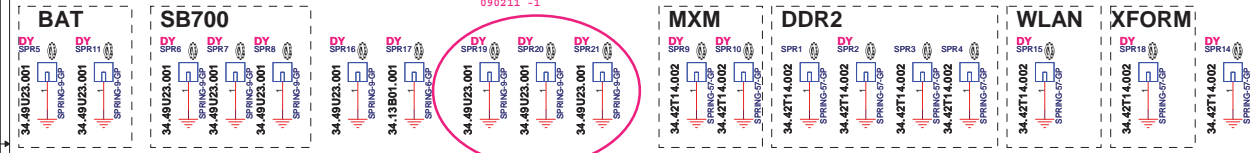
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| | | |
|---------------------|------------------------|----------------|
| Title | | |
| AD/BATT CONN | | |
| Size | Document Number | Rev |
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SPRING ON TOP ~ 0209
 34.49U23.001 + 34.13B01.001
 34.42T14.002

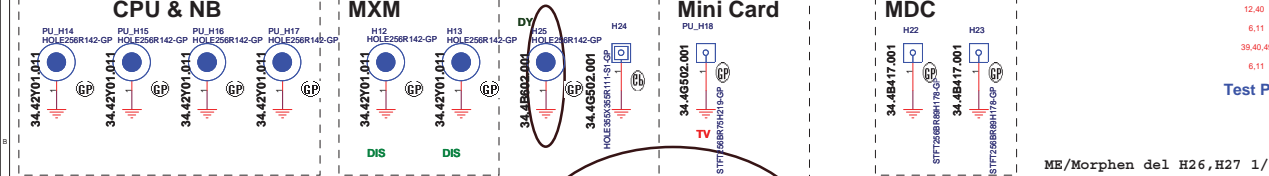


Check test point

- 3D3V_S0 ○ TP213 TPAD14-GP
- 3D3V_AUX_S5 ○ TP215 TPAD14-GP
- 3D3V_S5 ○ TP212 TPAD14-GP
- 5V_S5 ○ TP211 TPAD14-GP
- 12.40_PML_PWRSTN <<< TP176 TPAD14-GP
- 6.11_CPU_PWRGD <<< TP189 TPAD14-GP
- 39.40_49_SS_ENABLE <<< TP207 TPAD14-GP
- 6.11_CPU_LDT_RST <<< TP195 TPAD14-GP

Test Point放在Dimm Door打開可量測處

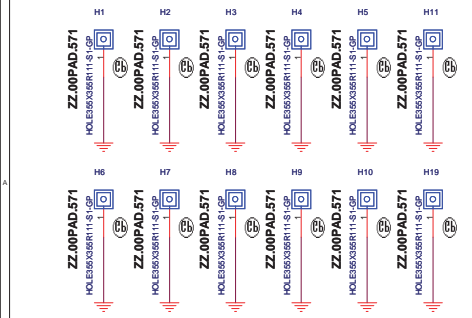
STAND OFF ON BOTTOM ~ 0210
 STAND OFF ON TOP ~ 0209

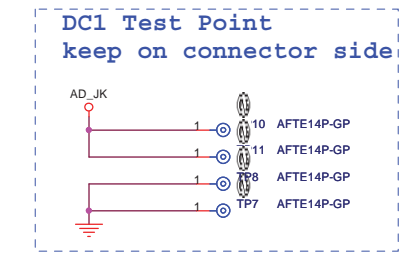
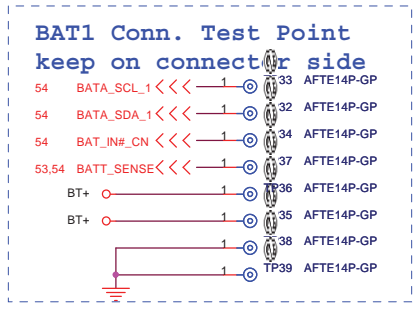
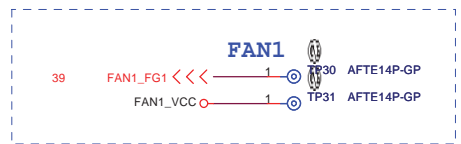
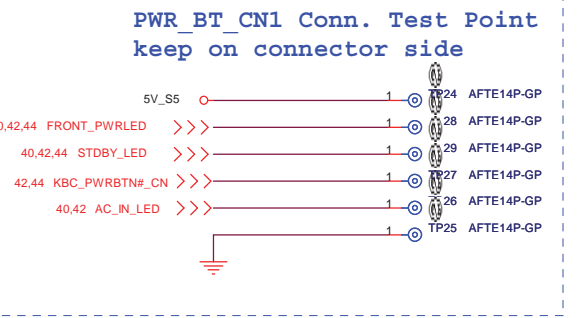
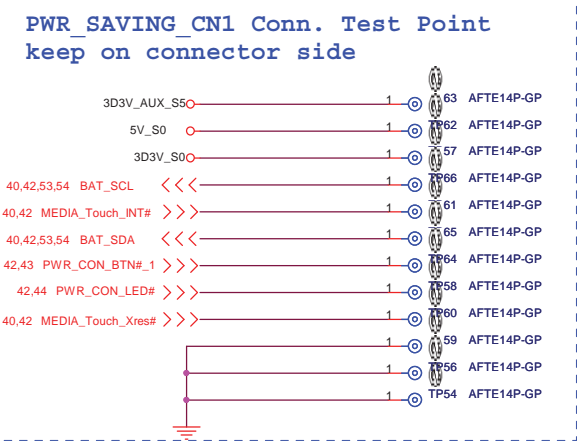
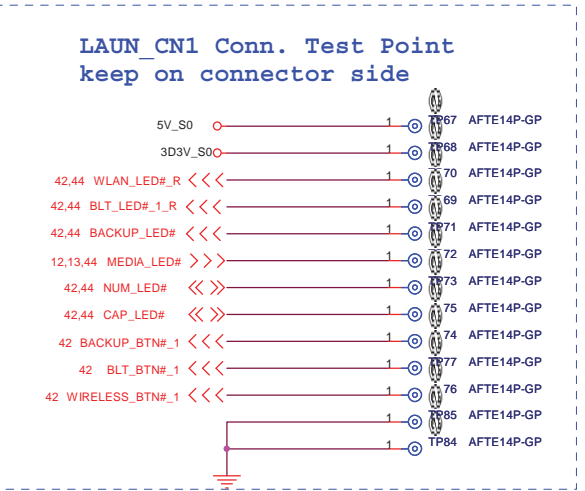
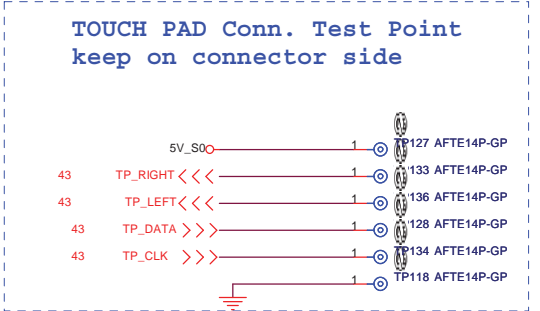
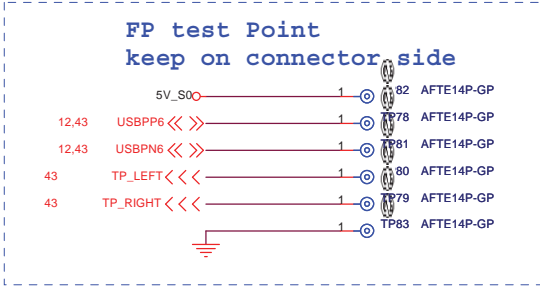
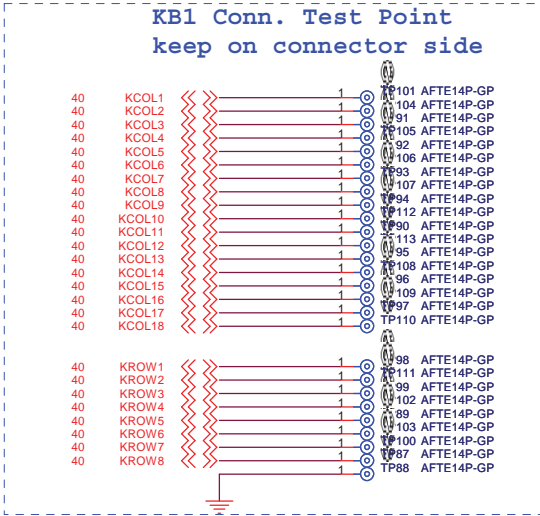


ME/Morphen del H26, H27 1/8

ME/Morphen del H25 2/10
 R recover H25 3/2
 R Add H28 3/5

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