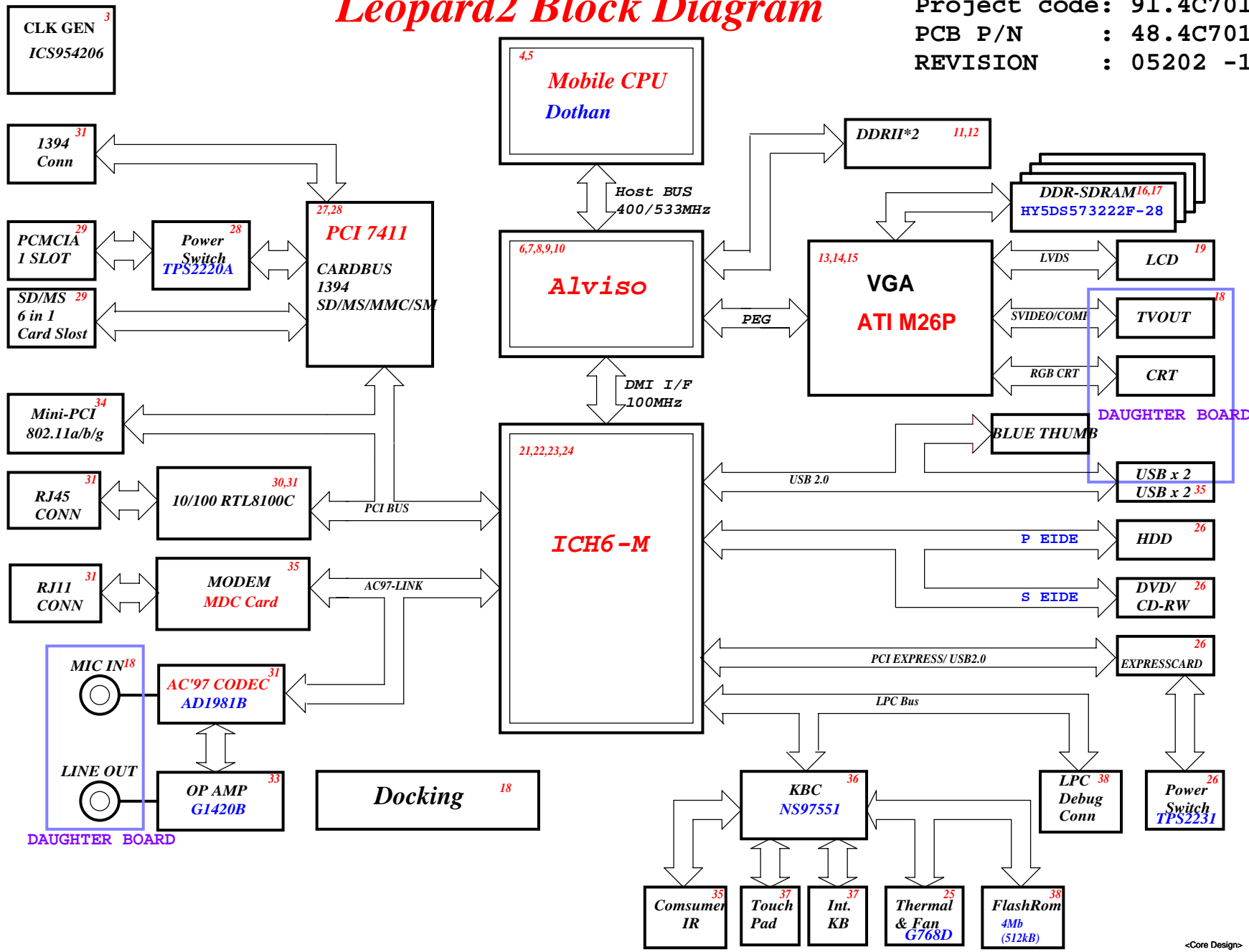


Leopard2 Block Diagram

Project code: 91.4C701.001
 PCB P/N : 48.4C701.011
 REVISION : 05202 -1



SYSTEM DC/DC	
42 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 5V_S3 3V_AUX

SYSTEM DC/DC	
45 MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_VGA_S0

MAXIM CHARGER	
40 MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC	
41 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844-1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet 1 of 47

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/PB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
 5V_S3= 5 Voltage suspend to RAM(S3 state)
 5V_S5= 5 Voltage soft off(S5 state)
 3D3V_S0= 3.3 Voltage power up on system work(S0 state)
 3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
 3D3V_S5= 3.3 Voltage soft off(S5 state)
 LVDDR_2D8V= 2.8 Voltage power up on system work(S0 state)
 1D8V_S3= 1.8 Voltage suspend to RAM(S3 state)
 2D5V_S0= 2.5 Voltage power up on system work(S0 state)

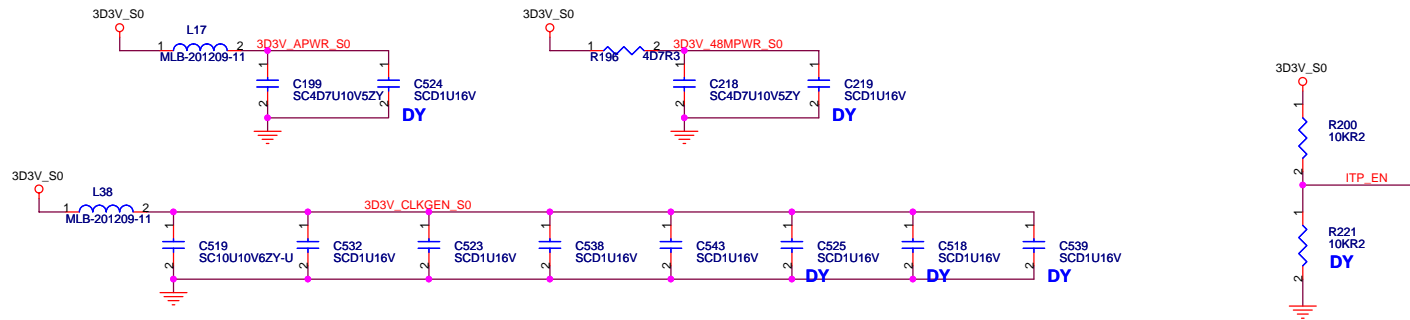
VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
 1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S5= 1.5 Voltage soft off(S5 state)
 DDR_VREF= 0.9 Voltage power up on system work(S0 state)
 1D2V_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
 VRAM_VDDQ= 1.8 Voltage power up on system work(S0 state) for VRAM
 1D05V_S0= 1.05 Voltage power up on system work(S0 state)
 CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
 VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# / GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1# / GNT1#
LAN	AD23	P_INTE#	REQ2# / GNT2#
Blue Thumb	AD24		

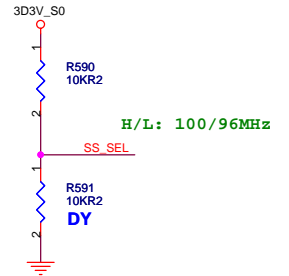
<Core Design>

緯創資通		Wistron Corporation	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>			
Title		ITP	
Size A3	Document Number	Leopard2	
Date: Wednesday, July 06, 2005	Sheet 2	of	47
			Rev -1

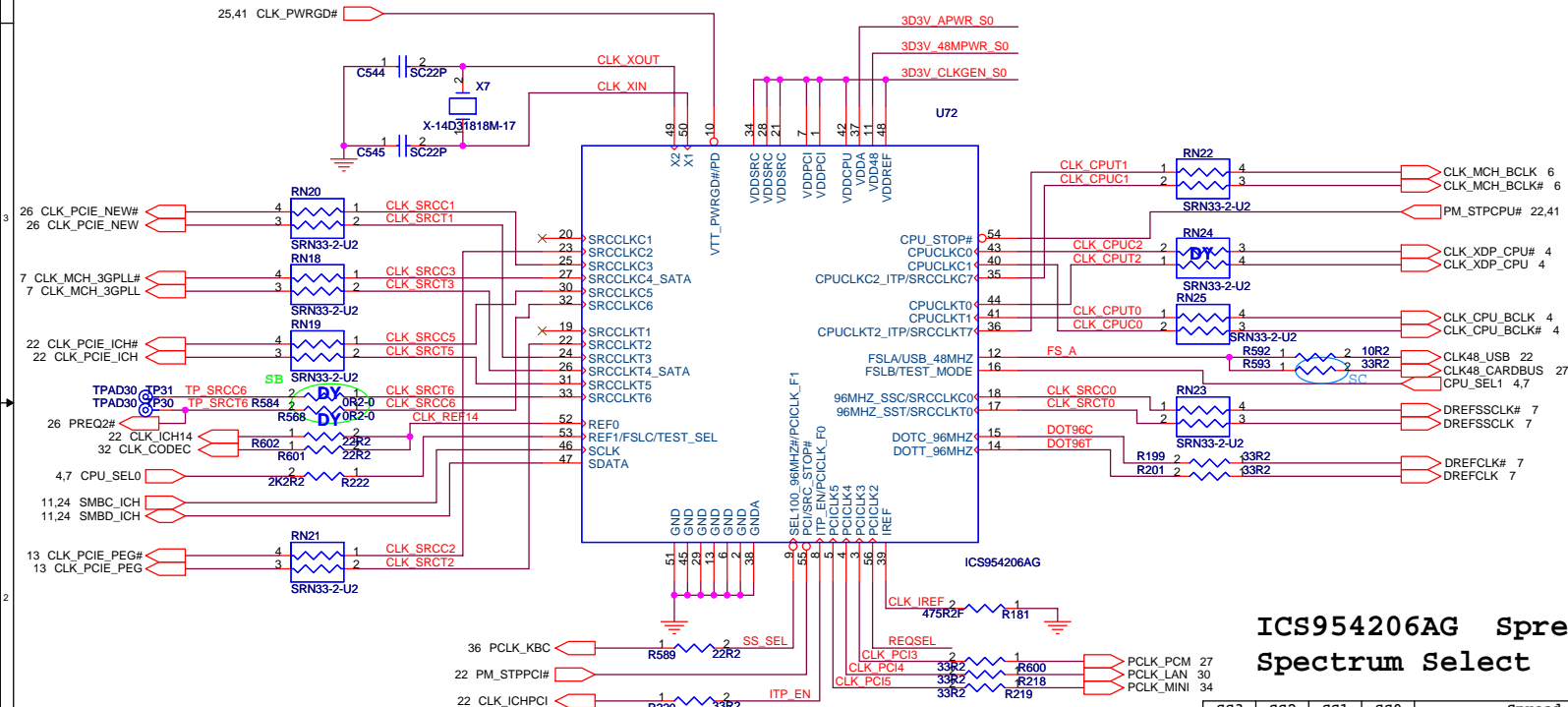


DummyR200(up side),Mounting R221(down side)
--SRC7 on

Mounting R200(up side),DummyR221(down side)
--CPU2_ITP on

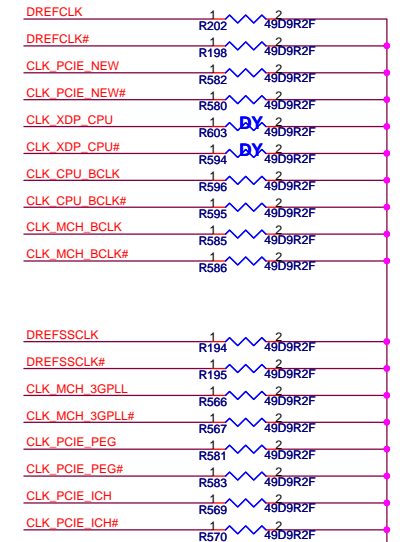


H/L: 100/96MHz

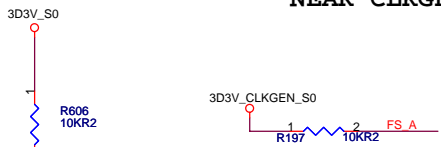


ICS954206AG Spread Spectrum Select

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+0.3
1	0	0	1	+0.4
1	0	1	0	+0.5
1	0	1	1	+0.6
1	1	0	0	+0.8
1	1	0	1	+1.0
1	1	1	0	+1.25
1	1	1	1	+1.5



NEAR CLKGEN



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

CLK_CPU_BCLK TP33
CLK_CPU_BCLK# TPAD30
TP32
TPAD30

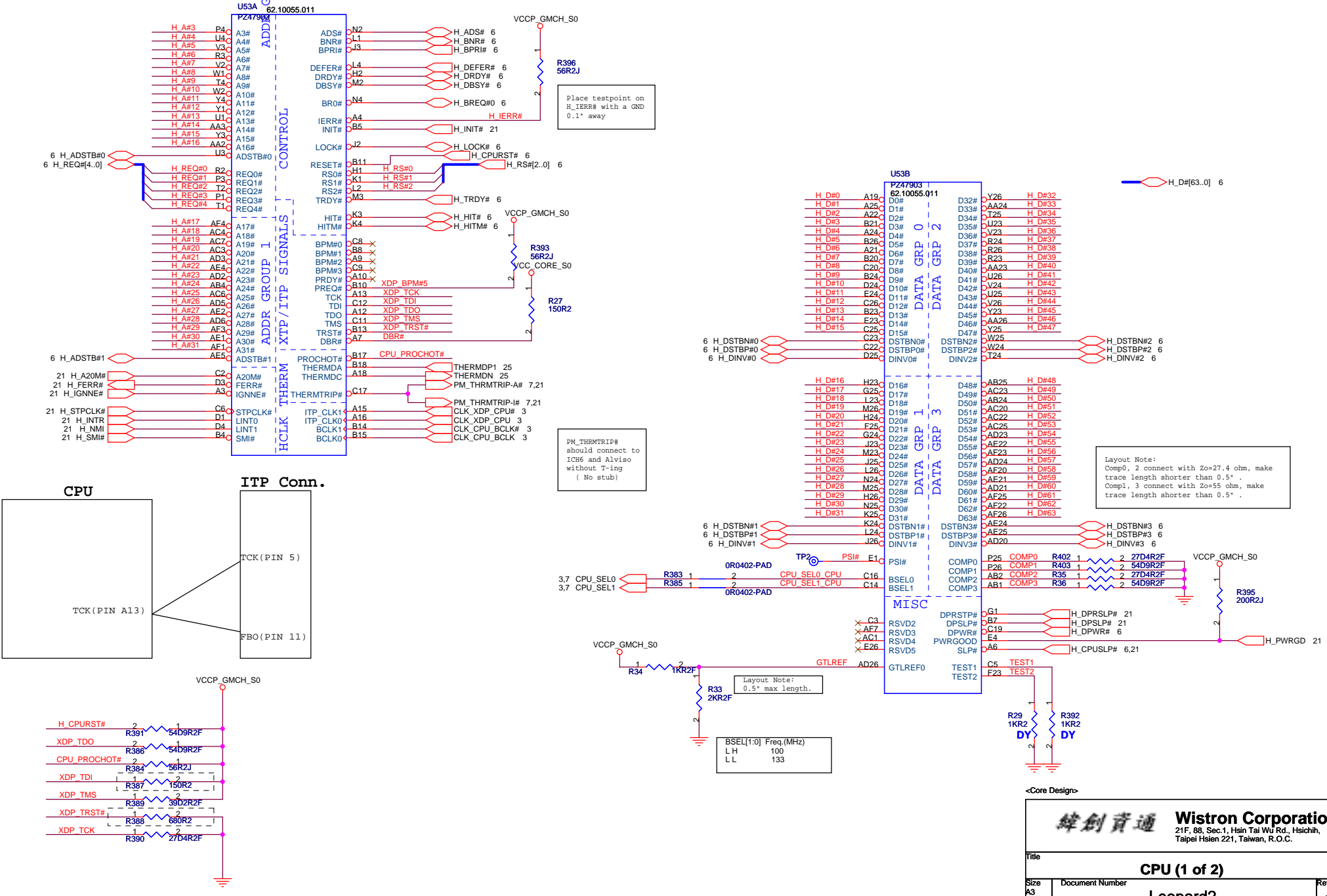
close to CPU

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator (ICS954206AG)**
Size A3 Document Number: **Leopard2** Rev -1
Date: Monday, July 11, 2005 Sheet 3 of 47

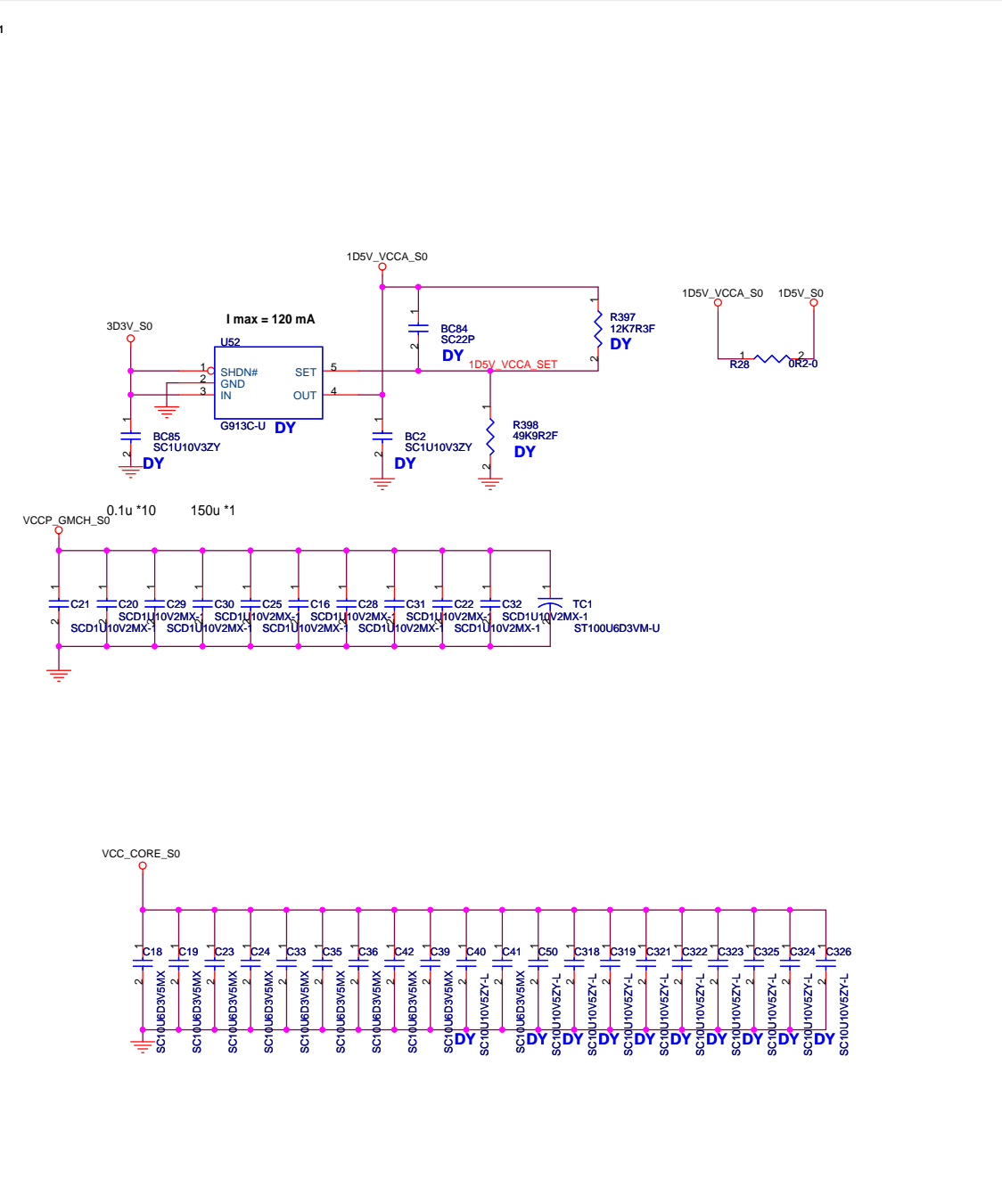
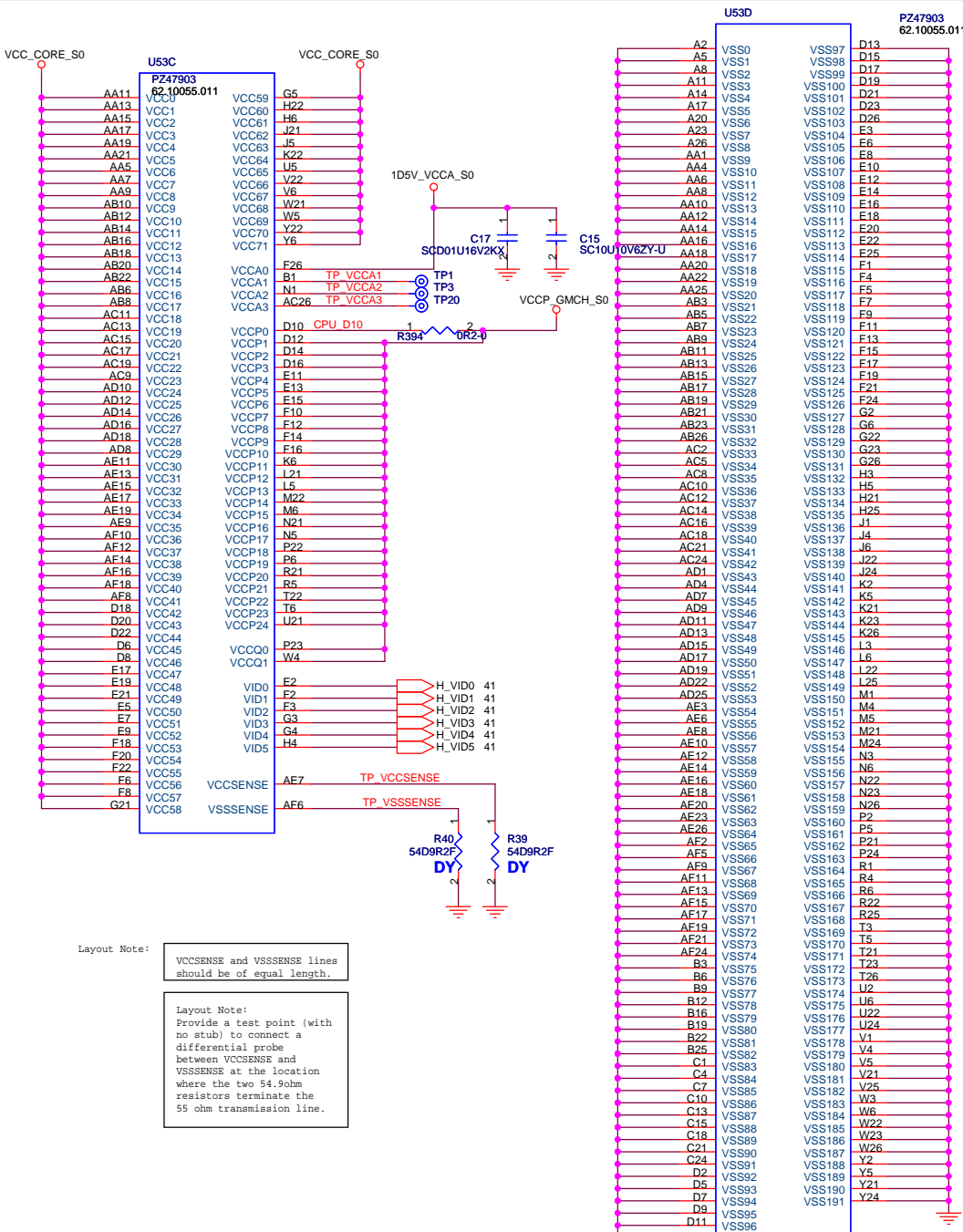
6 H_A#(31..3)



All place within 2" to CPU

<Core Design>

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU (1 of 2)		
Size A3	Document Number	Rev -1
Leopard2		
Date: Monday, July 11, 2005	Sheet 4 of 47	



Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

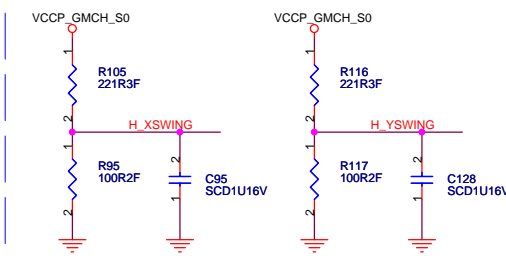
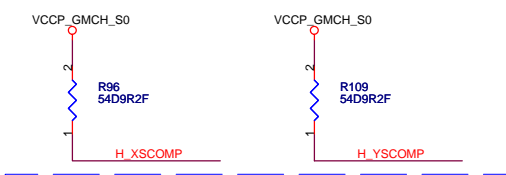
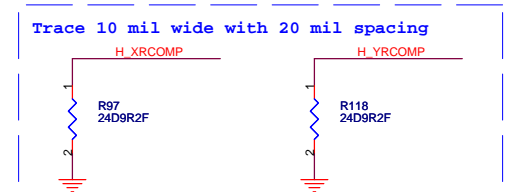
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (2 of 2)

Size A3 Document Number: Leopard2 Rev SC

Date: Sunday, July 03, 2005 Sheet 5 of 47



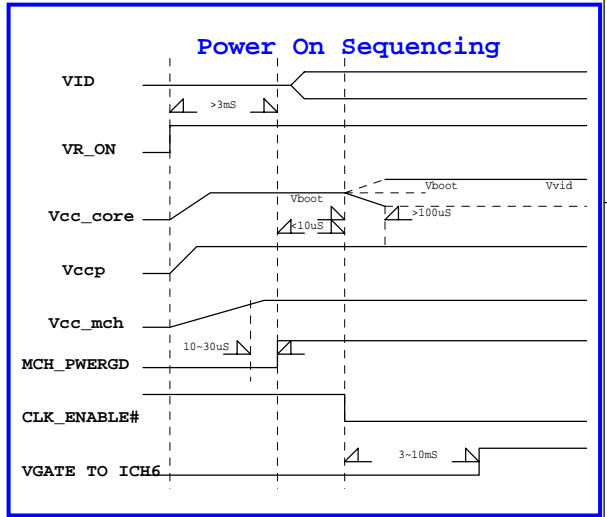
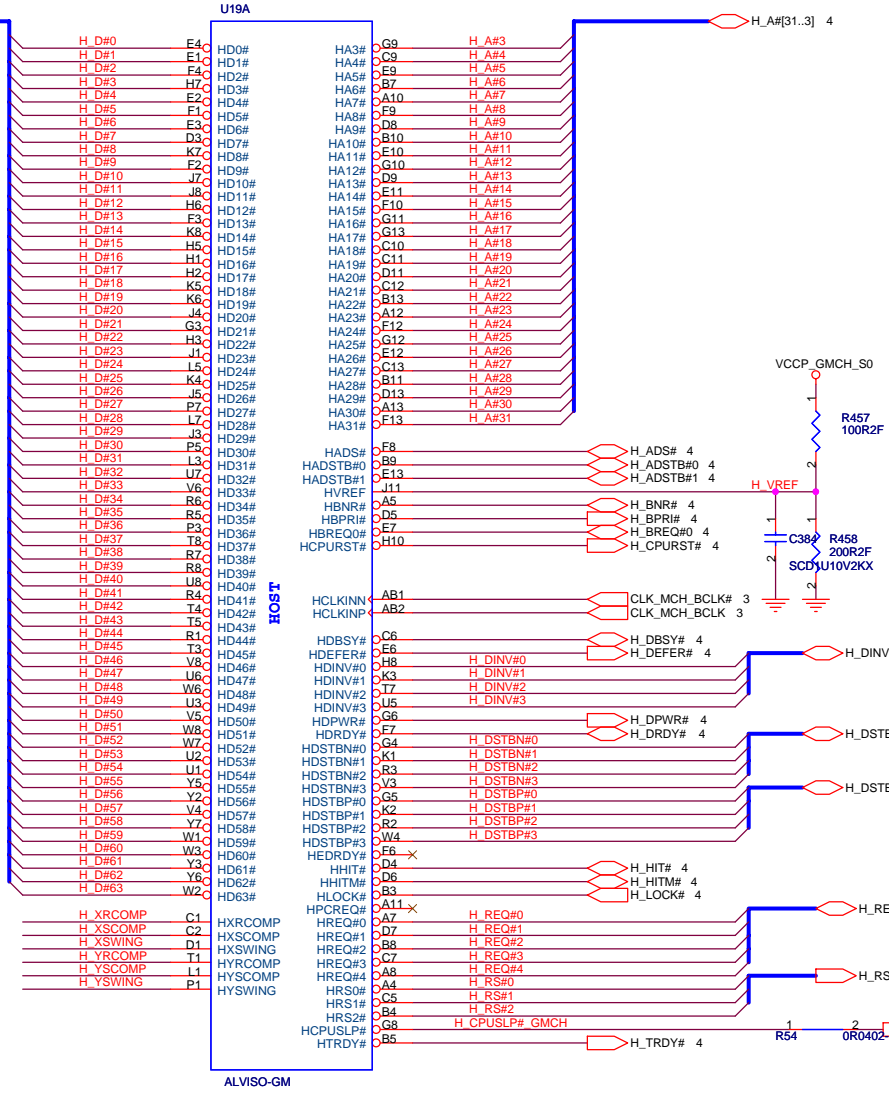
Trace 10 mil wide with 20 mil spacing

Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reserved	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reserved	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present(Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX In signal.



ALVISO-GM: 71.0GMCH.08U
ALVISO-PM: 71.0GMCH.0BU
ALVISO-GML: 71.0GMCH.0JU

<Core Design>

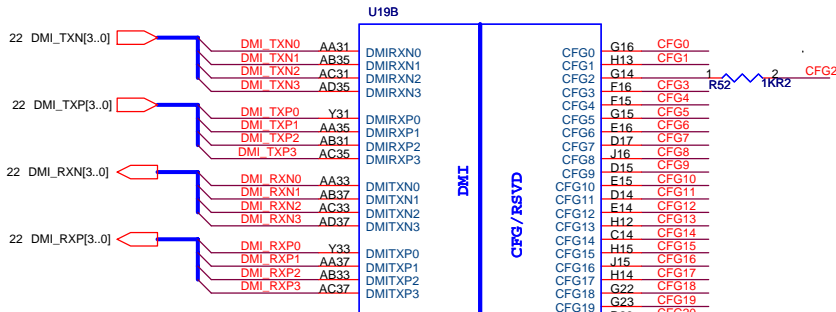
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (1 of 5)**

Size A3 Document Number **Leopard2** Rev **-1**

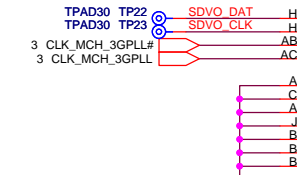
Date: Monday, July 11, 2005 Sheet 6 of 47

Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die



Note: CRT_RED, CRT_GREEN, CRT_BLUE, are ground referenced.

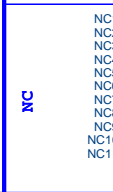
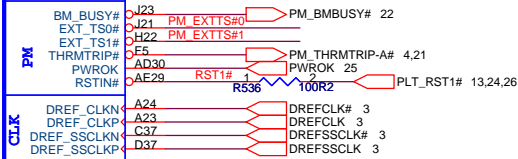
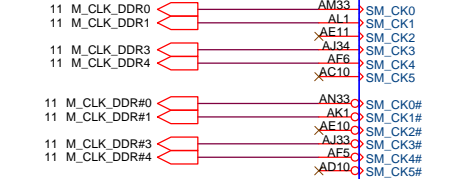
Intel suggest NC Due to votusly DVO



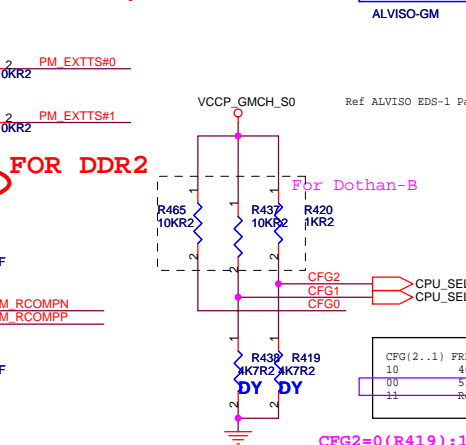
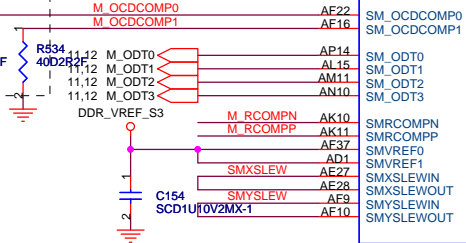
Intel design guide suggest Ref no.:14511 page 210

Place 150 Ohm termination resistors close to GMCH

Note: Intel design guide suggest(page 203) If the LVDS interface is not implemented, all signals associated with the interface can be left as no connects.

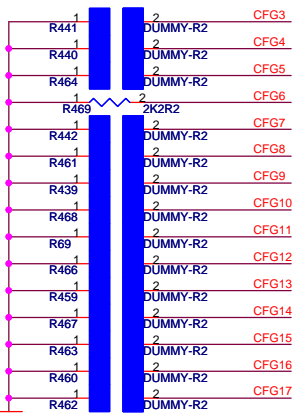


Layout Note: Route as short as possible



Ref ALVISO EDS-1 Page 115

When Low 2.2K Ohm

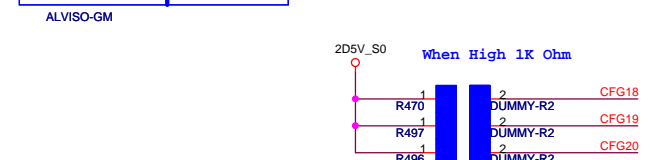
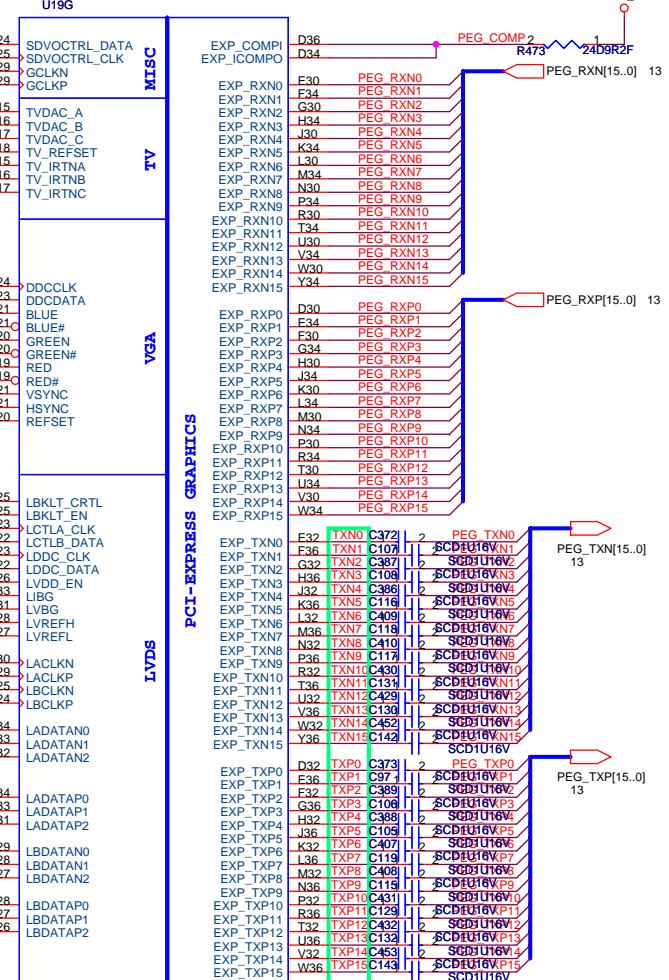


CFG(2..1) FREQ.(MHz) 10 400 00 533 Reserved

CFG2=0(R419):133MHZ CFG2=1(R420):100MHZ

FOR DDR2

For Dothan-B



When High 1K Ohm

Strapping

CFG[17:3] have internal pullup resistors. CFG[19:18] have internal pulldown resistors

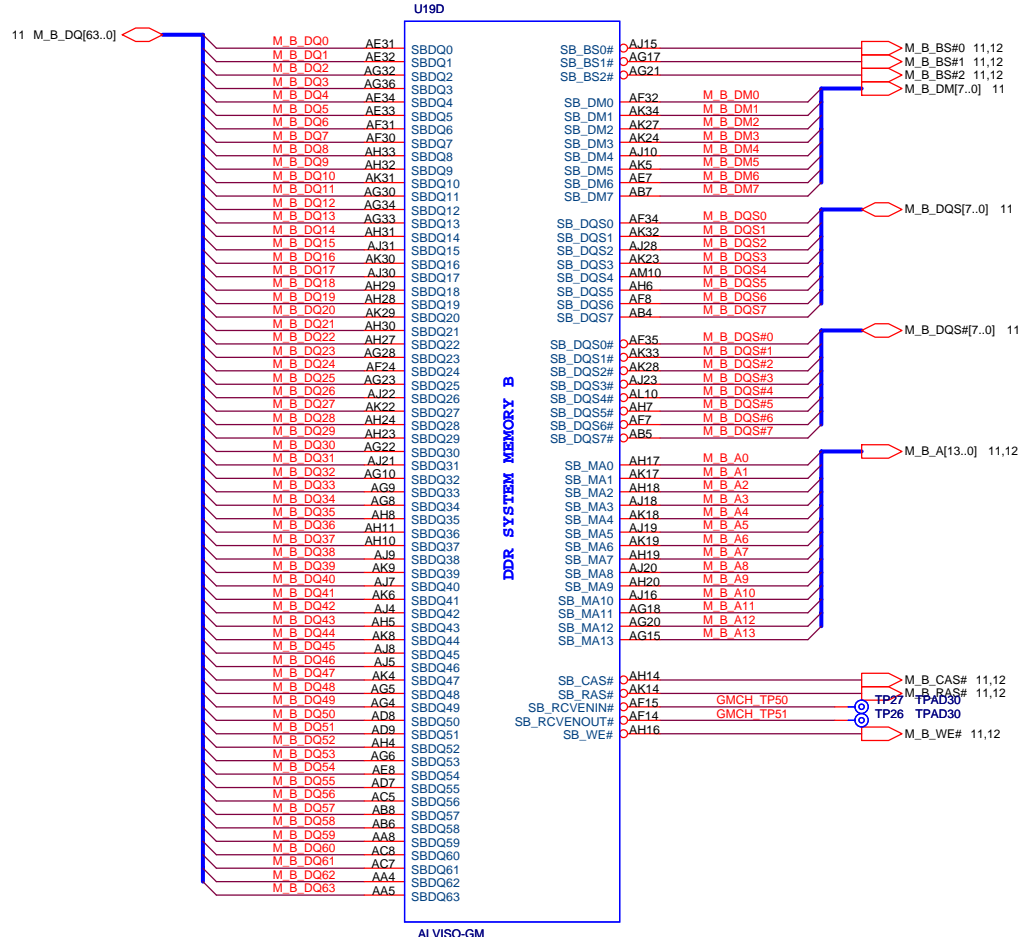
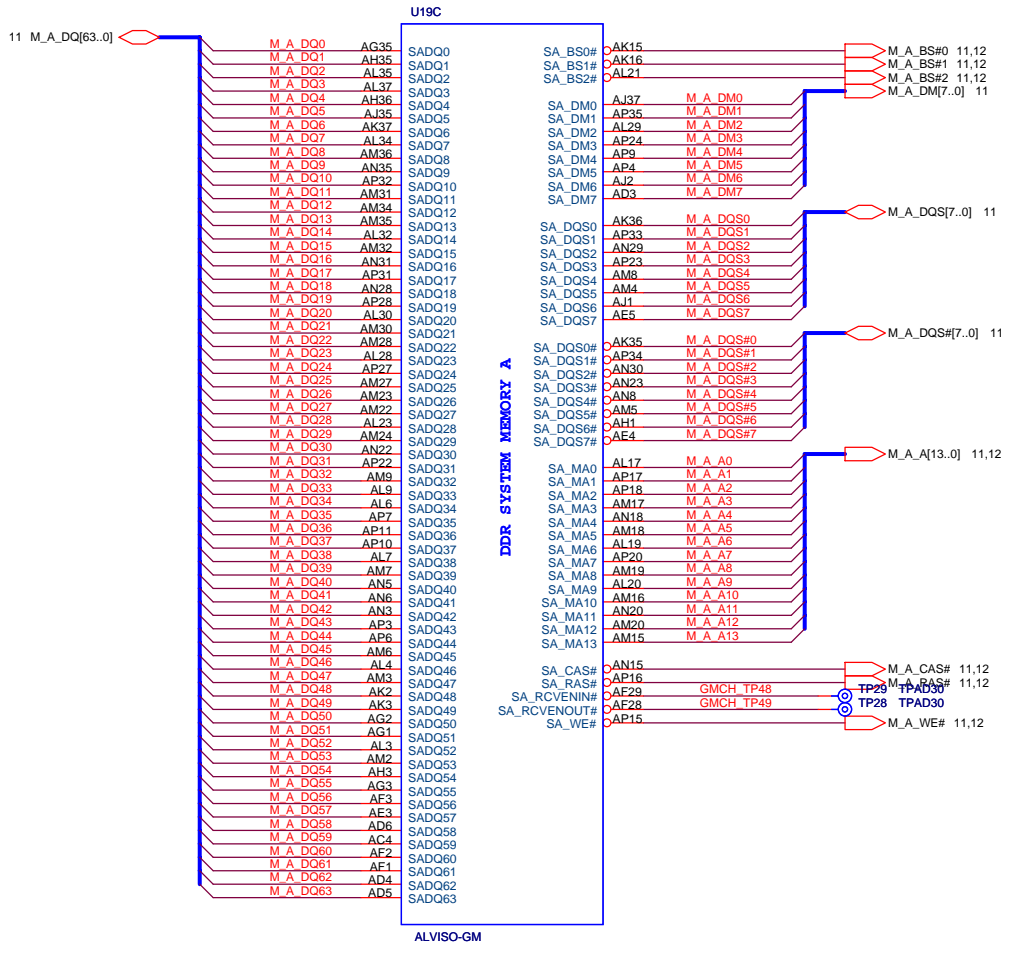
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (2 of 5)**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Thursday, July 07, 2005 Sheet: 7 of 47



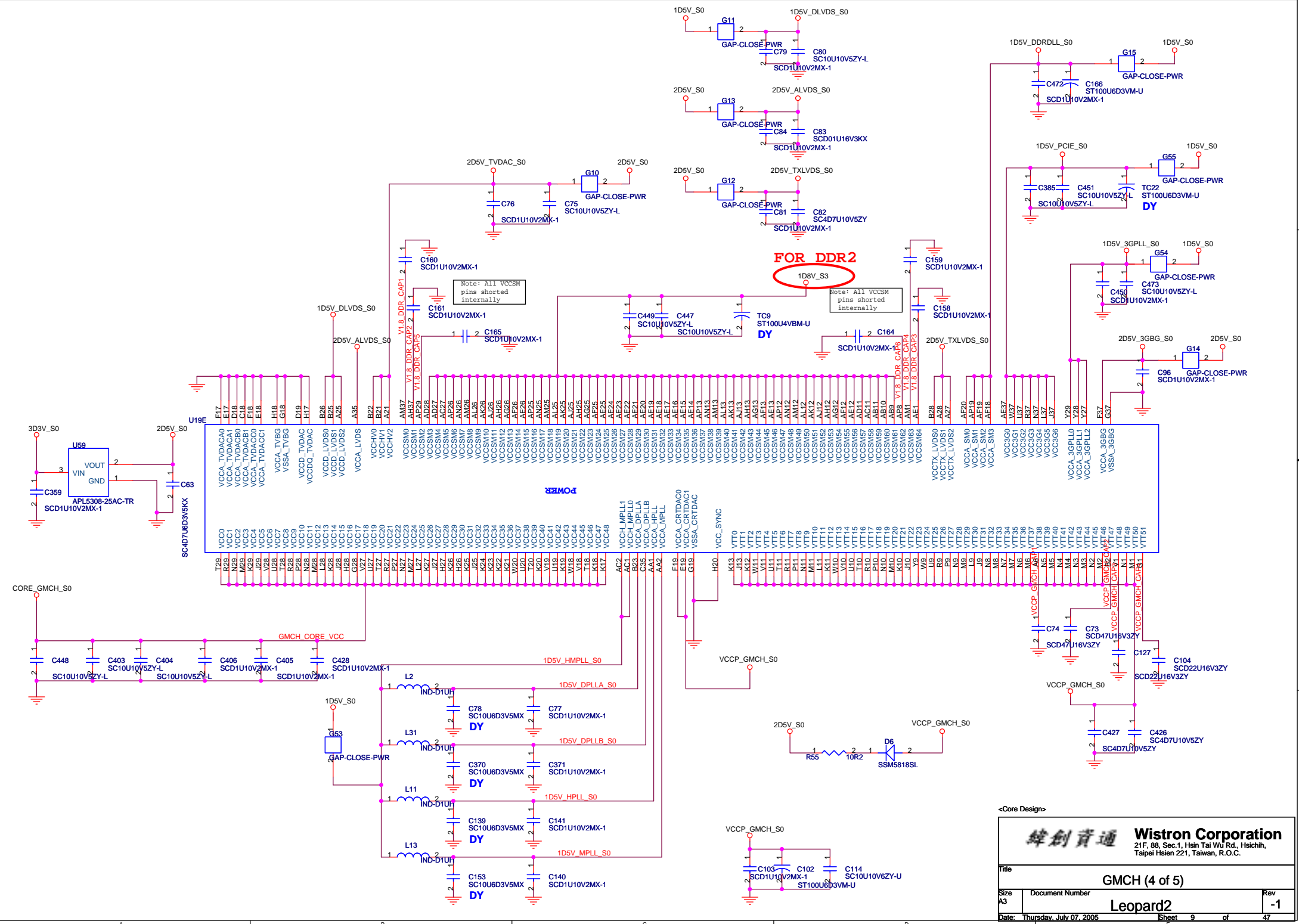
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (3 of 5)**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 8 of 47



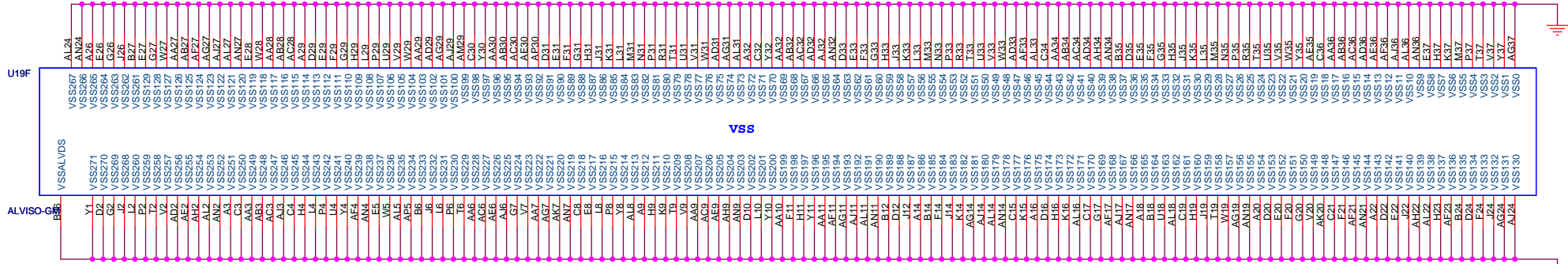
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (4 of 5)**

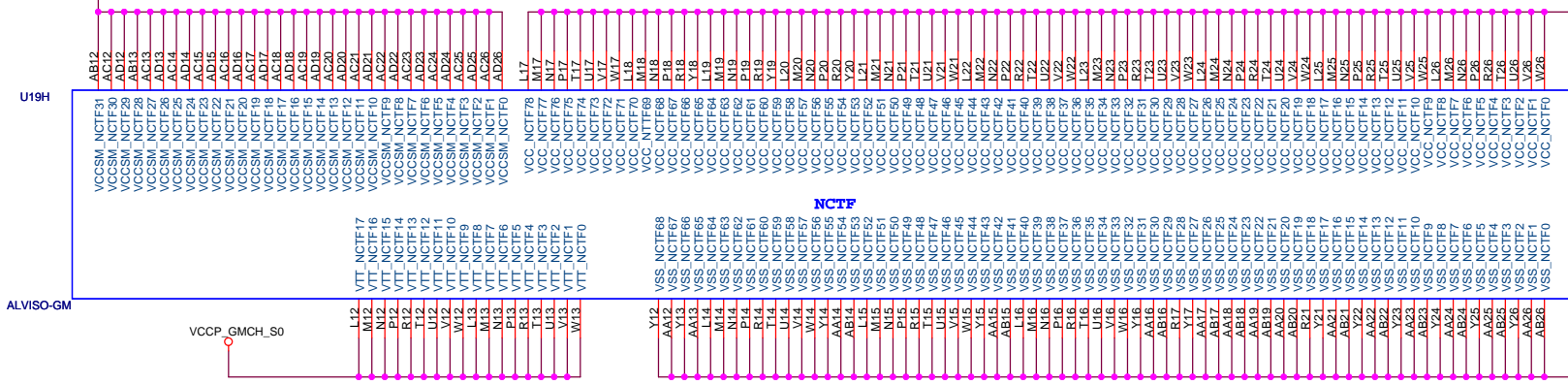
Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 9 of 47



1D8V_S3

FOR DDR2



CORE_GMCH_S0

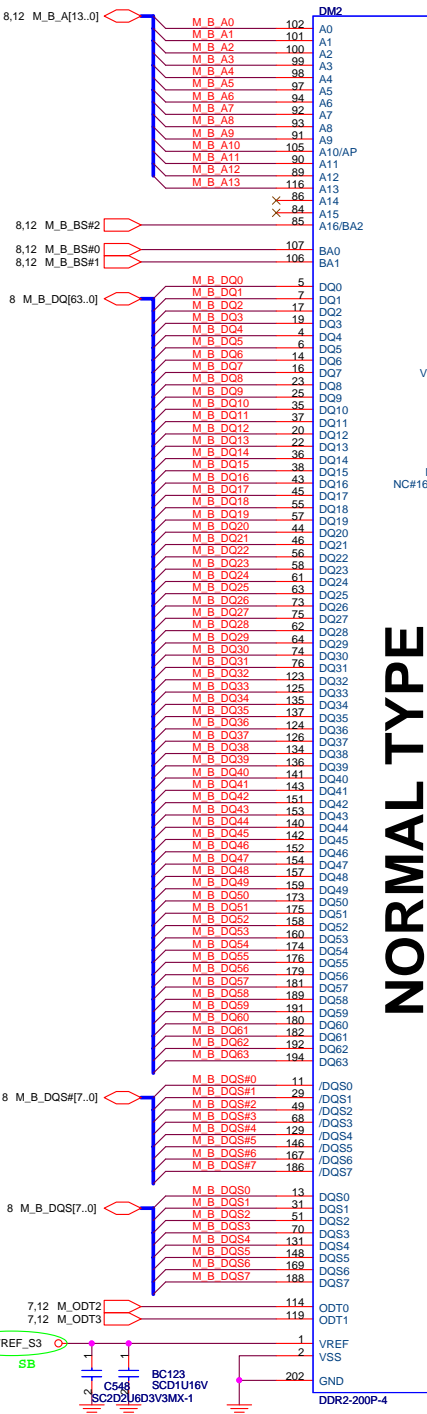
<Core Design>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (5 of 5)**

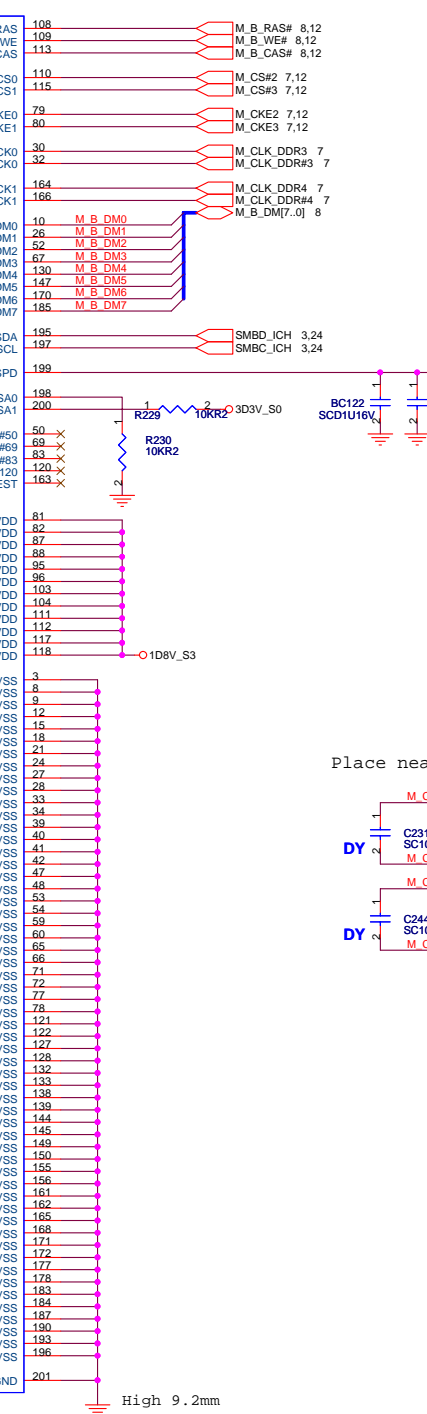
Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet 10 of 47

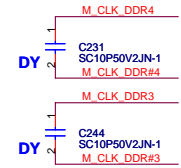


NORMAL TYPE

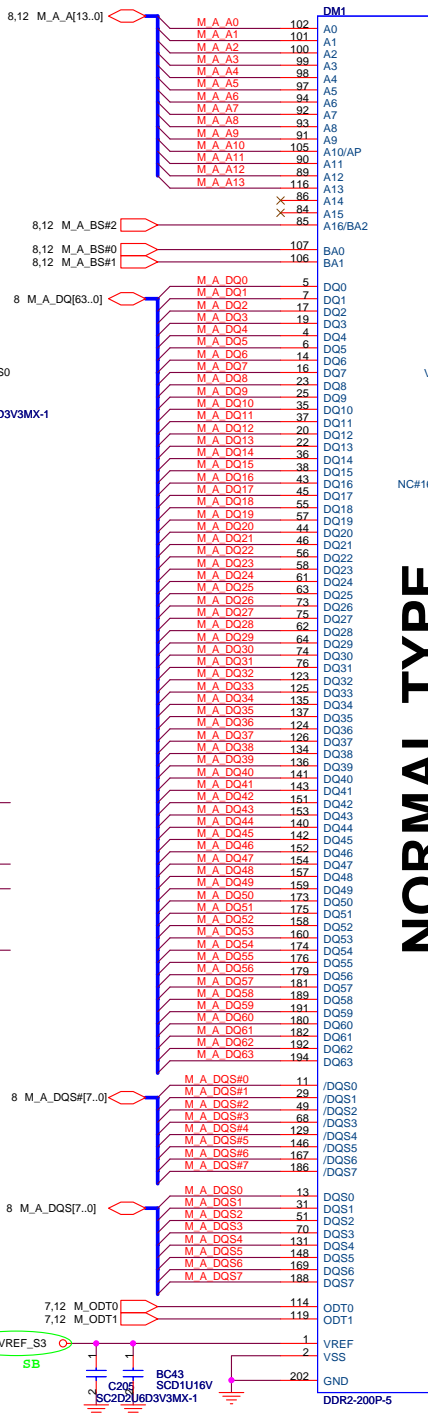
Hi 9.2 mm



Place near DM1

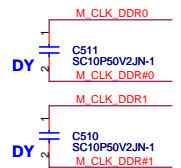


Low 5.2 mm



NORMAL TYPE

Place near DM2

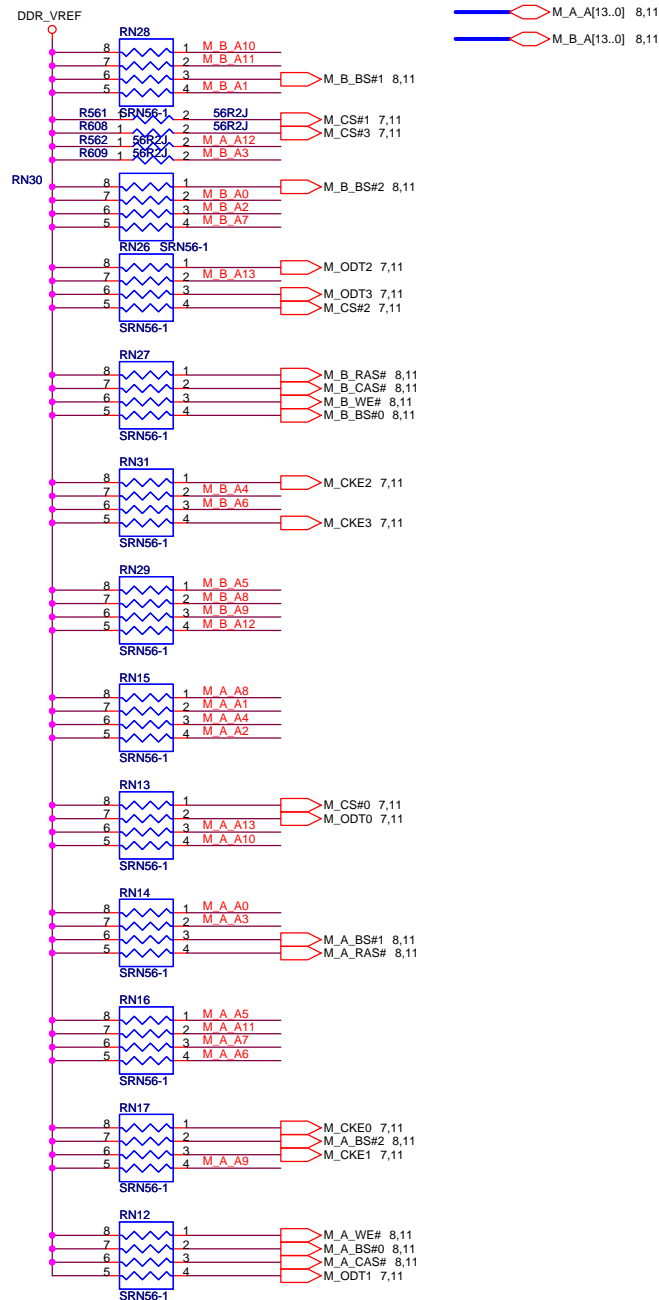


Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		DDR2 Socket	
Size	Document Number	Rev	
Custom		Leopard2	-1
Date:	Thursday, July 07, 2005	Sheet	11 of 47

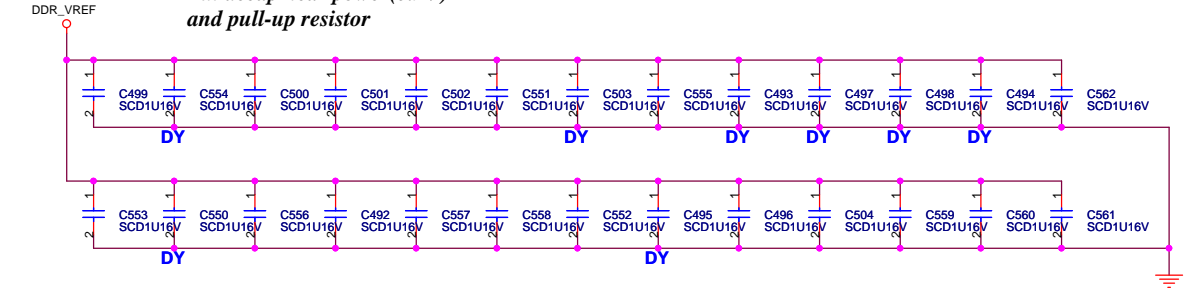
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

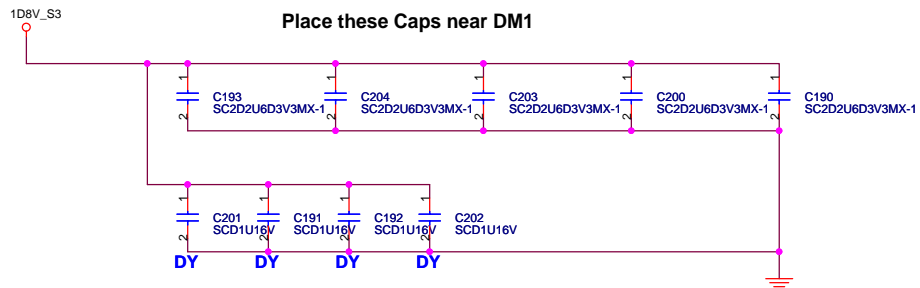


Decoupling Capacitor

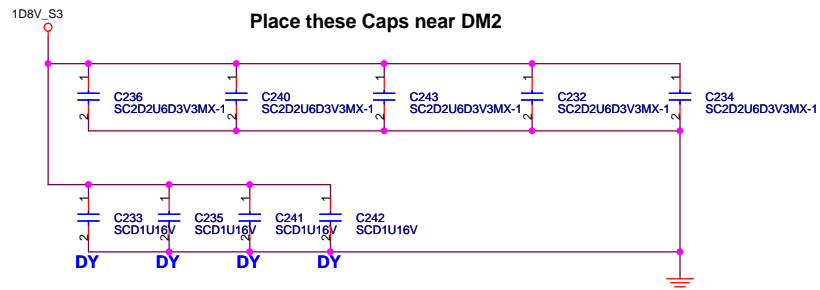
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



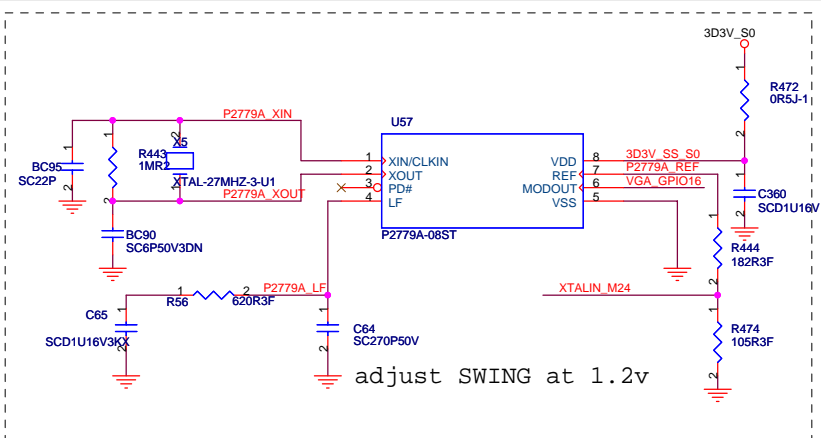
<Core Design>

緯創資通

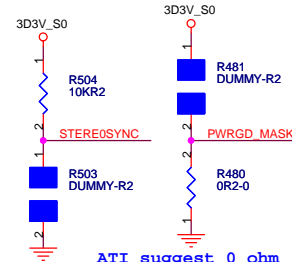
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

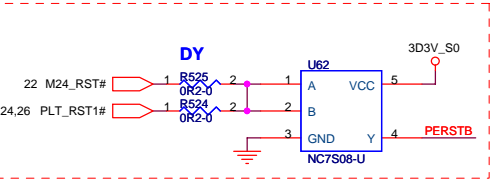
Title		
DDR2 Termination Resistor		
Size	Document Number	Rev
A3		-1
Date:	Thursday, July 07, 2005	Sheet 12 of 47



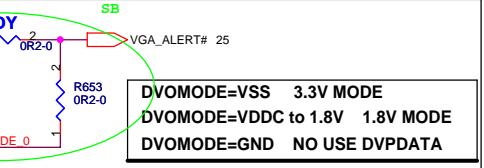
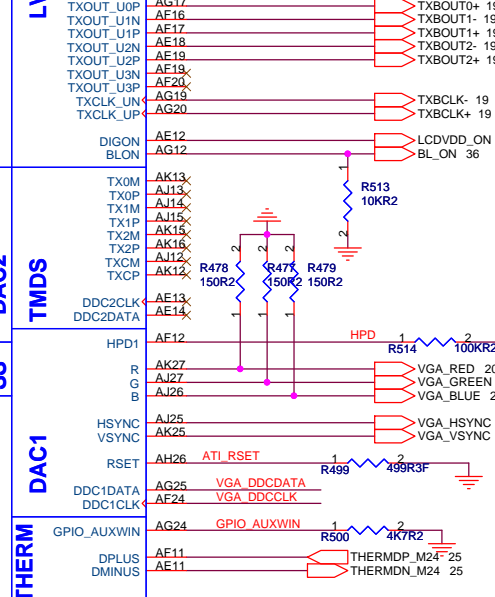
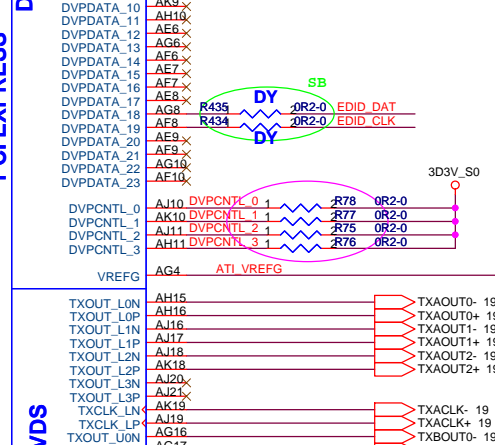
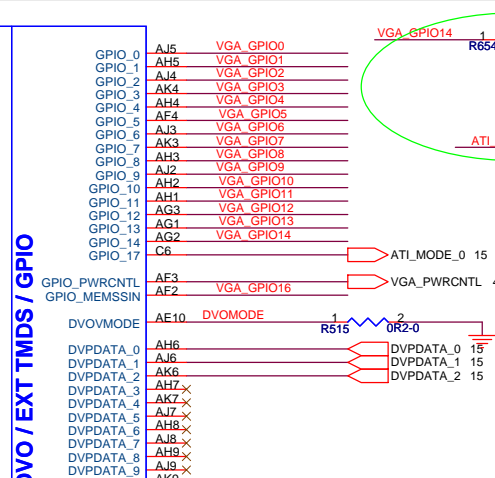
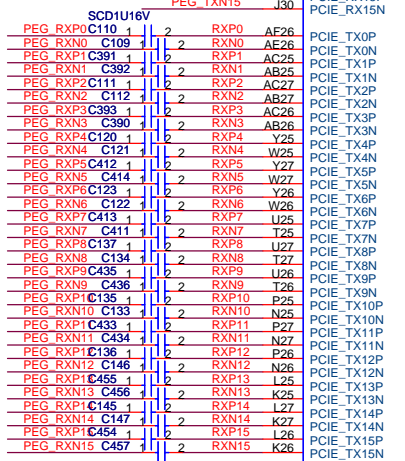
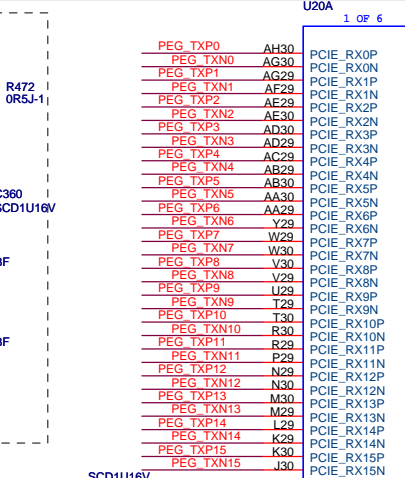
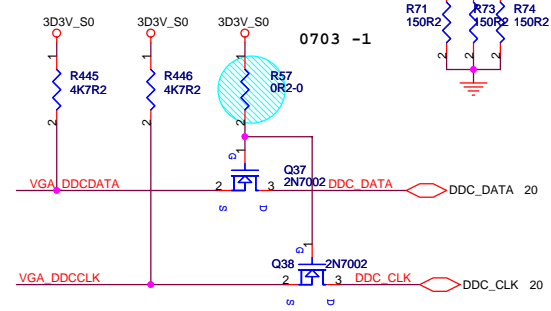
adjust SWING at 1.2v



ATI suggest 0 ohm



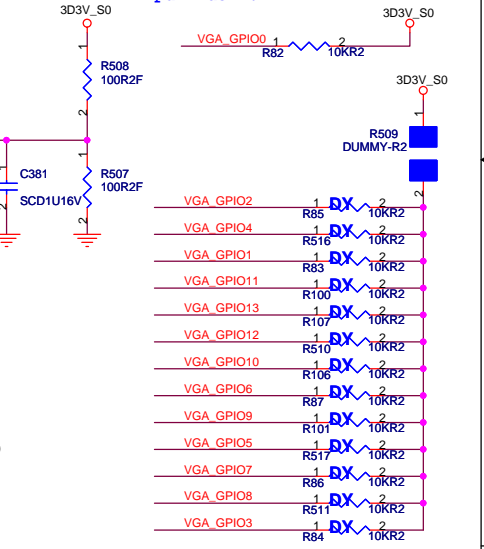
DDC_CLK & DATA level shift



DVOMODE=VSS 3.3V MODE
 DVOMODE=VDDC to 1.8V 1.8V MODE
 DVOMODE=GND NO USE DVPDATA

STRAPS	PIN	DEFAULT
CAL_BG_BACKUP	GPIO0	0
PLL_CAL_FORCE_EN	GPIO1	0
PCIE_MODE(1:0)	GPIO(3:2)	00
CAL_OFF	GPIO4	0
BYPASS_PLL	GPIO5	0
ICOMP	GPIO6	0
DEBUG_ACCESS	GPIO8	0
ROMIDCFG(3:0)	GPIO(9,13:11)	0000
MULTIFUNC(1:0)	LCDDATA(17:16)	00
VIP_DEVICE	LCDDATA(20)	0
DWNGR0	LCDDATA(21)	0 (internal pull-down)

ATI Ref. Datasheets (page 3-32)
 DOC.NO.:CHS-216M24-03
 GPIO[0..13] are internal pull-down.

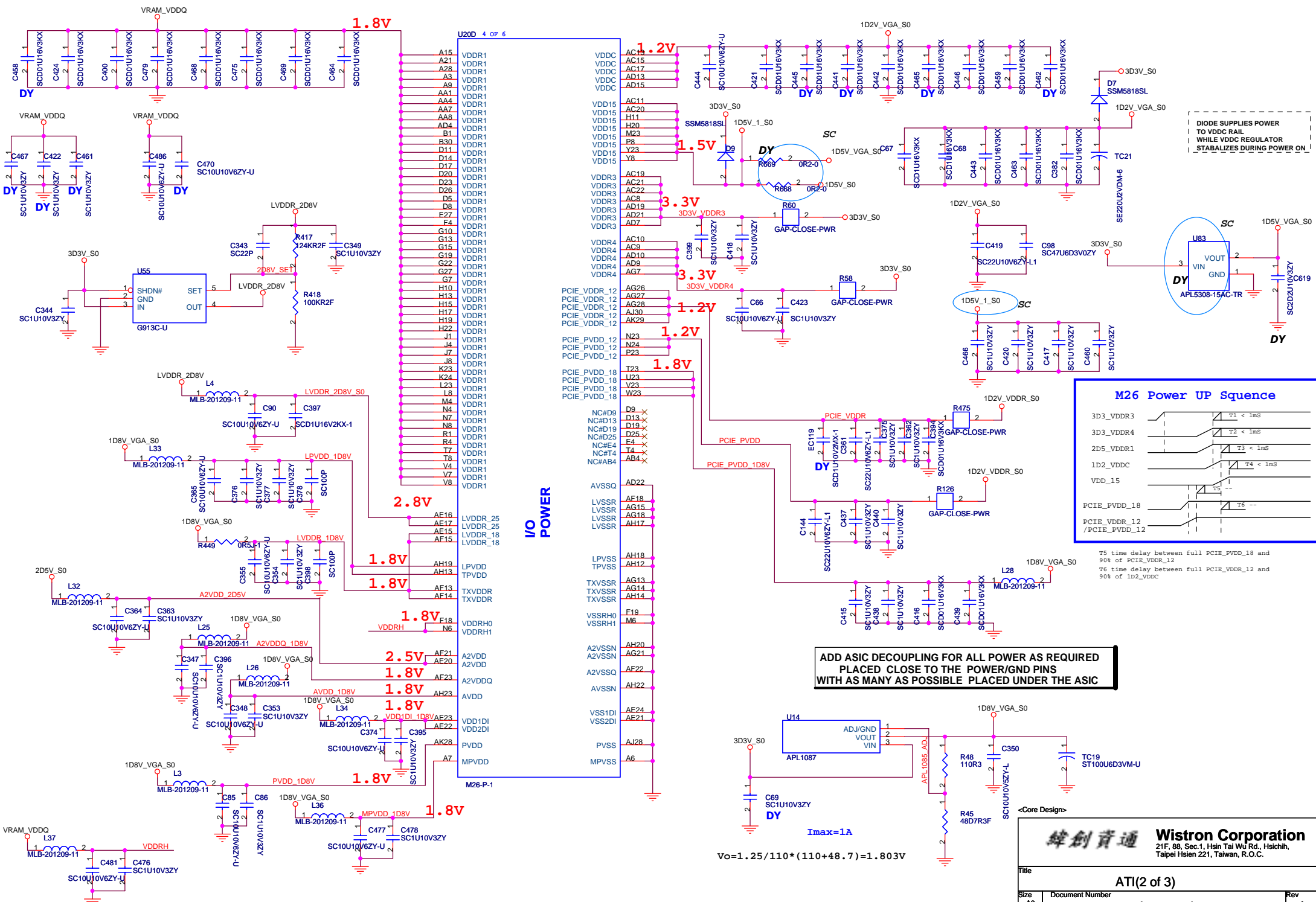


Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

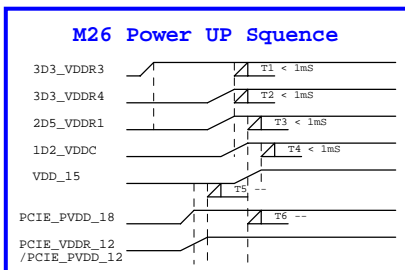
ATI(1 of 3)

Leopard2

Monday, July 11, 2005

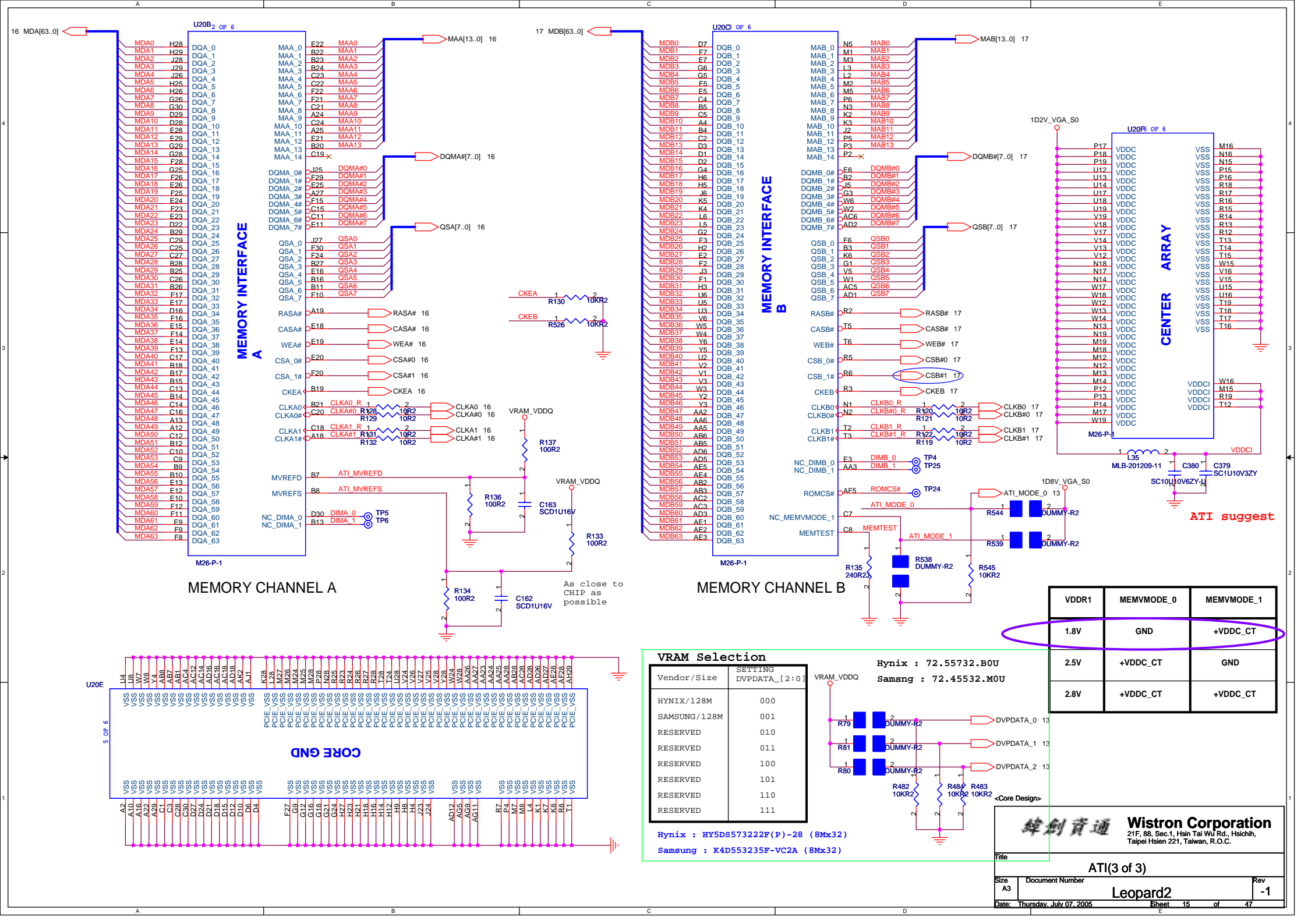


DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABILIZES DURING POWER ON



ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED PLACED CLOSE TO THE POWER/GND PINS WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.



U20B₂ OP 6

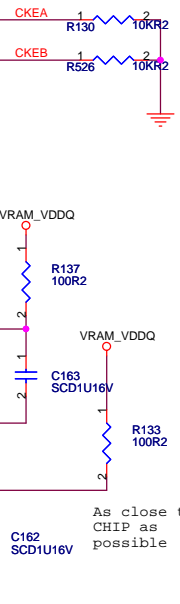
- MDA0 H28 DQA_0
- MDA1 H29 DQA_1
- MDA2 J28 DQA_2
- MDA3 J29 DQA_3
- MDA4 H25 DQA_4
- MDA5 H26 DQA_5
- MDA6 H26 DQA_6
- MDA7 G26 DQA_7
- MDA8 G30 DQA_8
- MDA9 D29 DQA_9
- MDA10 D28 DQA_10
- MDA11 E28 DQA_11
- MDA12 E29 DQA_12
- MDA13 G29 DQA_13
- MDA14 G28 DQA_14
- MDA15 F28 DQA_15
- MDA16 G25 DQA_16
- MDA17 F26 DQA_17
- MDA18 E26 DQA_18
- MDA19 E26 DQA_19
- MDA20 E24 DQA_20
- MDA21 F23 DQA_21
- MDA22 E23 DQA_22
- MDA23 D22 DQA_23
- MDA24 B22 DQA_24
- MDA25 C22 DQA_25
- MDA26 C25 DQA_26
- MDA27 C27 DQA_27
- MDA28 B28 DQA_28
- MDA29 B25 DQA_29
- MDA30 C26 DQA_30
- MDA31 B26 DQA_31
- MDA32 E17 DQA_32
- MDA33 E17 DQA_33
- MDA34 D16 DQA_34
- MDA35 F16 DQA_35
- MDA36 E15 DQA_36
- MDA37 F14 DQA_37
- MDA38 F14 DQA_38
- MDA39 F13 DQA_39
- MDA40 C17 DQA_40
- MDA41 B18 DQA_41
- MDA42 B17 DQA_42
- MDA43 B15 DQA_43
- MDA44 C13 DQA_44
- MDA45 C14 DQA_45
- MDA46 C14 DQA_46
- MDA47 C16 DQA_47
- MDA48 A16 DQA_48
- MDA49 A12 DQA_49
- MDA50 C12 DQA_50
- MDA51 B12 DQA_51
- MDA52 C10 DQA_52
- MDA53 C9 DQA_53
- MDA54 B9 DQA_54
- MDA55 B10 DQA_55
- MDA56 E13 DQA_56
- MDA57 F13 DQA_57
- MDA58 F12 DQA_58
- MDA59 F12 DQA_59
- MDA60 E11 DQA_60
- MDA61 F9 DQA_61
- MDA62 F9 DQA_62
- MDA63 F8 DQA_63

MEMORY INTERFACE A

M26-P-1

MEMORY CHANNEL A

- MAA_0 E22 MAA0
- MAA_1 B22 MAA1
- MAA_2 B23 MAA2
- MAA_3 B24 MAA3
- MAA_4 C22 MAA4
- MAA_5 F22 MAA5
- MAA_6 F21 MAA6
- MAA_7 C21 MAA7
- MAA_8 A24 MAA8
- MAA_9 C24 MAA9
- MAA_10 C24 MAA10
- MAA_11 A25 MAA11
- MAA_12 B20 MAA12
- MAA_13 C19 MAA13
- MAA_14 C19 X
- DQMA_0# J25 DQMA#0
- DQMA_1# E29 DQMA#1
- DQMA_2# C26 DQMA#2
- DQMA_3# E15 DQMA#3
- DQMA_4# C15 DQMA#4
- DQMA_5# C11 DQMA#5
- DQMA_6# E11 DQMA#6
- DQMA_7#
- QSA_0 J27 QSA0
- QSA_1 F30 QSA1
- QSA_2 F24 QSA2
- QSA_3 B27 QSA3
- QSA_4 F16 QSA4
- QSA_5 B16 QSA5
- QSA_6 B11 QSA6
- QSA_7 F10 QSA7
- RASA# A19 RASA# 16
- CASA# E18 CASA# 16
- WEA# E19 WEA# 16
- CSA_0# E20 CSA#0 16
- CSA_1# E20 CSA#1 16
- CKEA B19 CKEA 16
- CLKA0 R B21 CLKA0 R 16
- CLKA0# R C20 CLKA0# R 16
- CLKA1 R C18 CLKA1 R 16
- CLKA1# R A18 CLKA1# R 16
- MVREFD B7 ATI MVREFD
- MVREFS B8 ATI MVREFS
- NC_DIMA_0 D30 DIMA 0 TP5
- NC_DIMA_1 B13 DIMA 1 TP6



As close to CHIP as possible

C163 SCD1U16V
C162 SCD1U16V

R137 100R2
R136 100R2
R134 100R2

R130 10KR2
R526 10KR2

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

VRAM_VDDQ

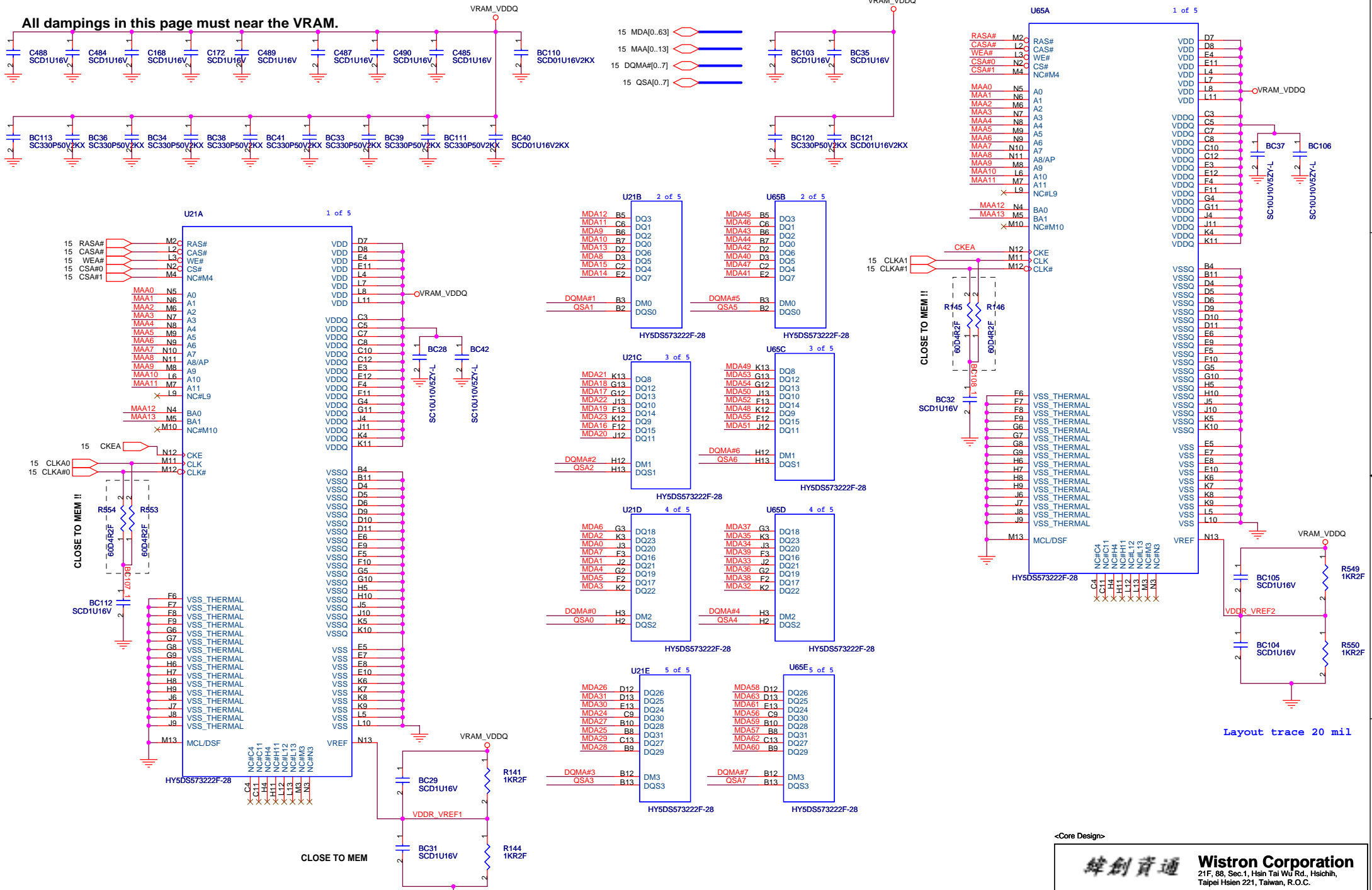
VRAM_VDDQ

VRAM_VDDQ

U20C OP 6

- MDB0 D7 DOB_0
- MDB1 F7 DOB_1
- MDB2 E7 DOB_2
- MDB3 G6 DOB_3
- MDB4 G5 DOB_4
- MDB5 G5 DOB_5
- MDB6 E5 DOB_6
- MDB7 C4 DOB_7
- MDB8 B5 DOB_8
- MDB9 C5 DOB_9
- MDB10 A4 DOB_10
- MDB11 B4 DOB_11
- MDB12 C2 DOB_12
- MDB13 D1 DOB_13
- MDB14 D1 DOB_14
- MDB15 D2 DOB_15
- MDB16 G4 DOB_16
- MDB17 H6 DOB_17
- MDB18 H6 DOB_18
- MDB19 J6 DOB_19
- MDB20 K5 DOB_20
- MDB21 K4 DOB_21
- MDB22 L6 DOB_22
- MDB23 L5 DOB_23
- MDB24 C2 DOB

All dampings in this page must near the VRAM.



Layout trace 20 mil

Layout trace 20 mil

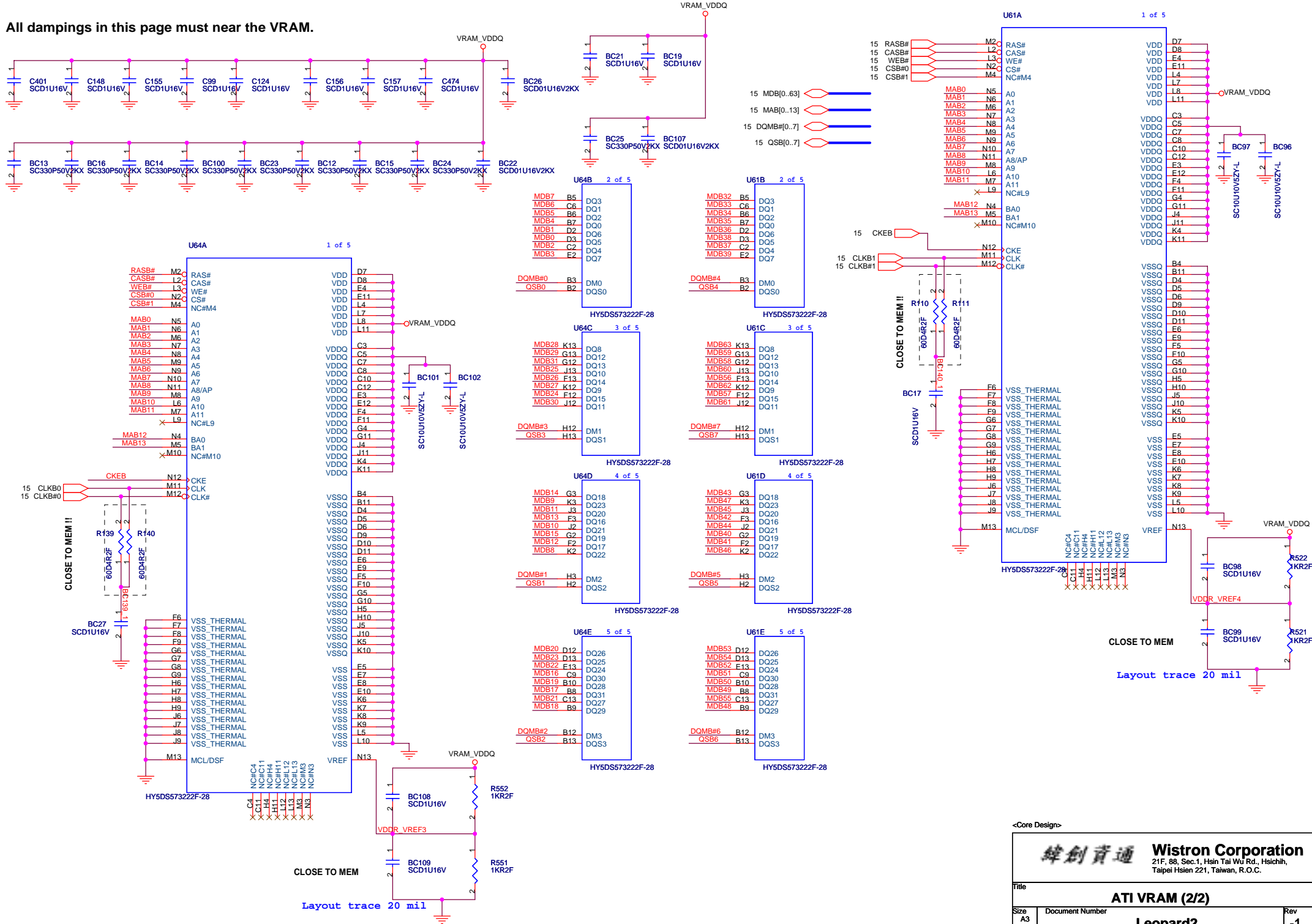
<Core Design>

緯創資通

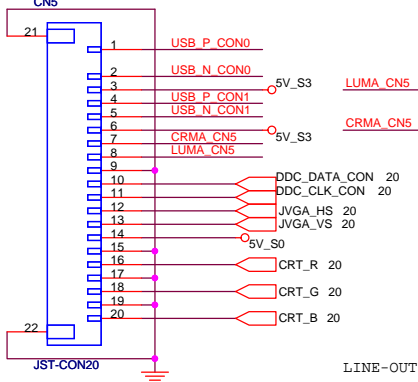
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		ATI VRAM (1/2)	
Size	A3	Document Number	Leopard2
Date:	Thursday, July 07, 2005	Sheet	16 of 47
Rev	-1		

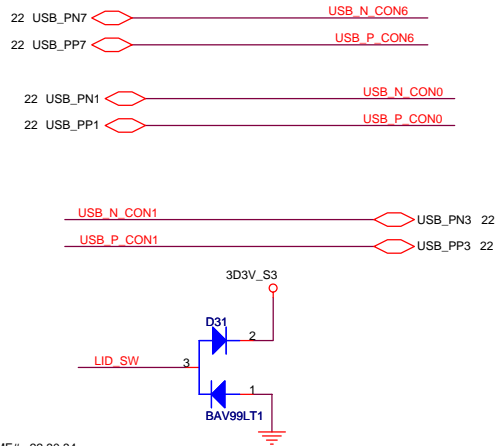
All dampings in this page must near the VRAM.



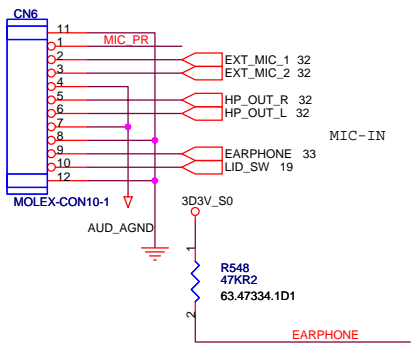
Digital Signal CONN



Close to Docking CN

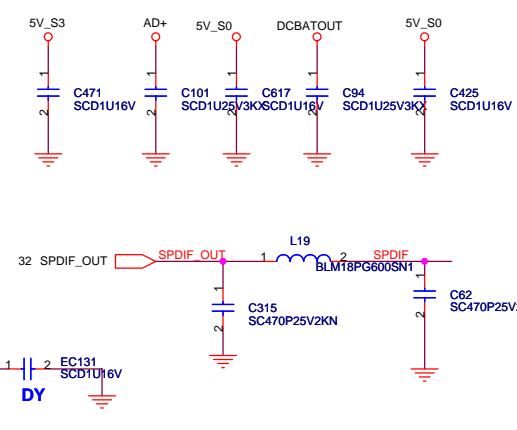
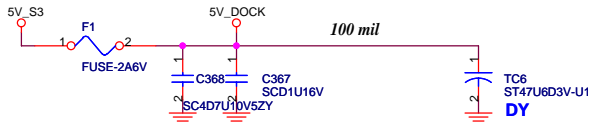
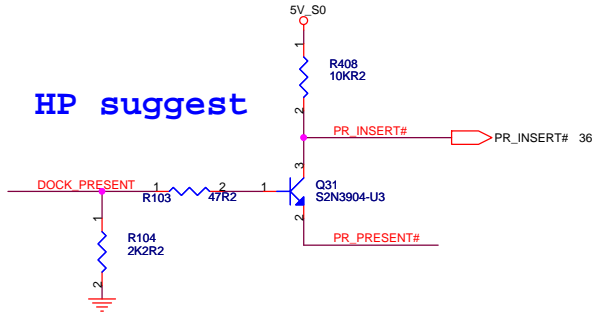


Analog Signal CONN



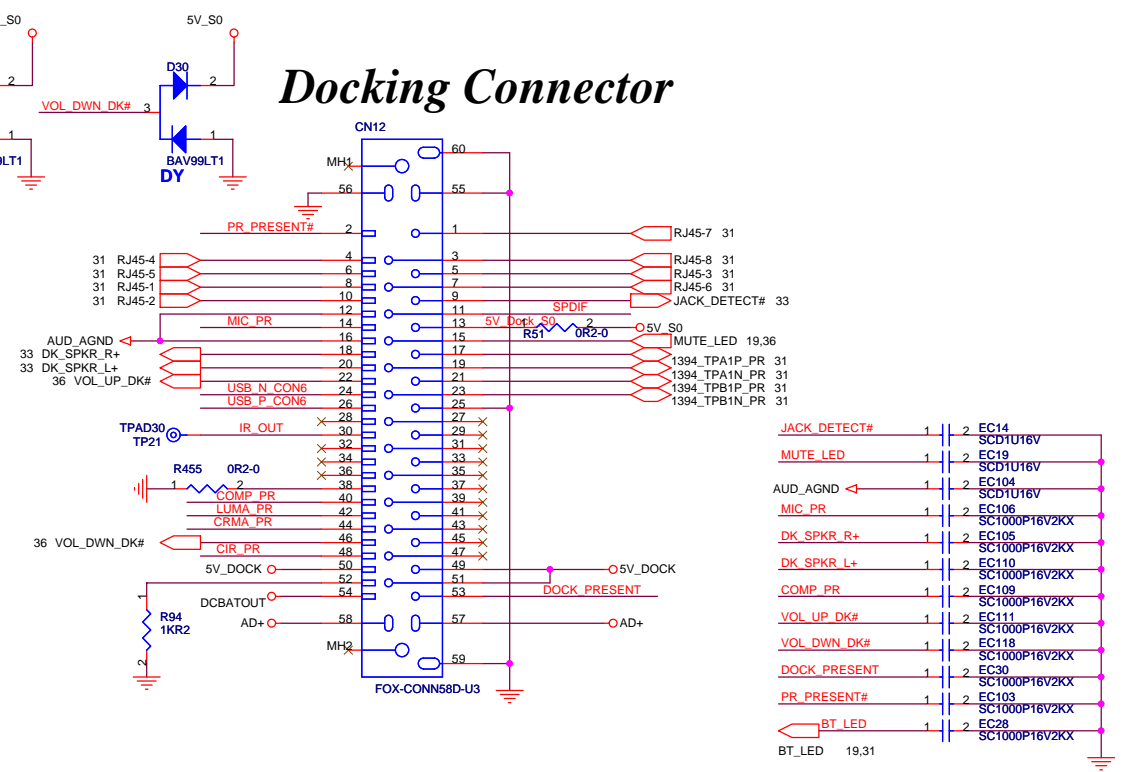
Please close to ICH6

HP suggest



CIR, CIR_PR, CIR_KBC are connect together. default setting 12/12

Docking Connector



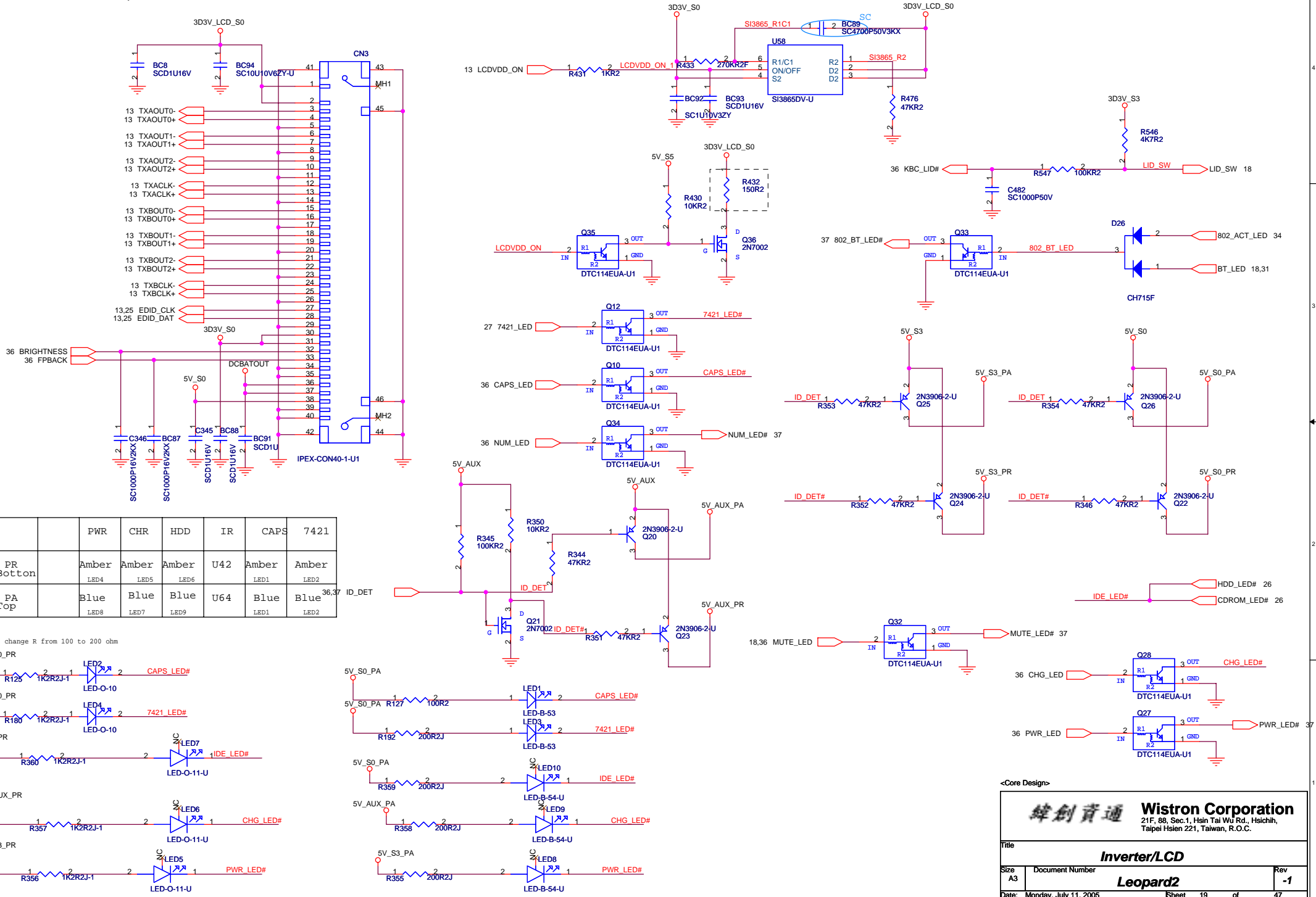
INPUT	FUNCTION
LOW	B0
HIGH	B1

Place near the GMCH

Place near the DOCK
 <Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

INVERTER / LCD



	PWR	CHR	HDD	IR	CAPS	7421
PR Botton	Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top	Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

<Core Design>

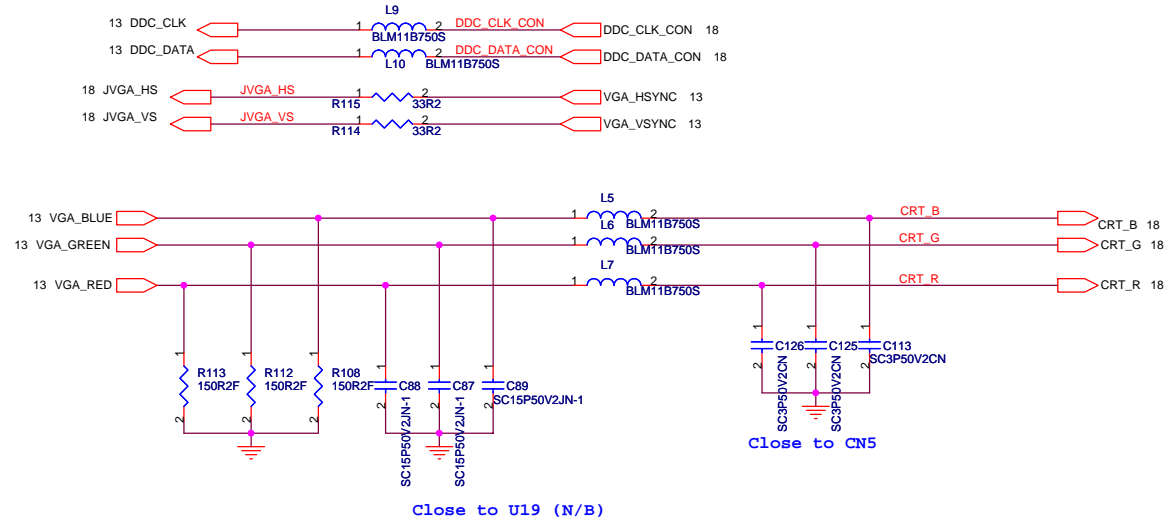
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Inverter/LCD**

Size: A3 Document Number: **Leopard2** Rev: **-1**

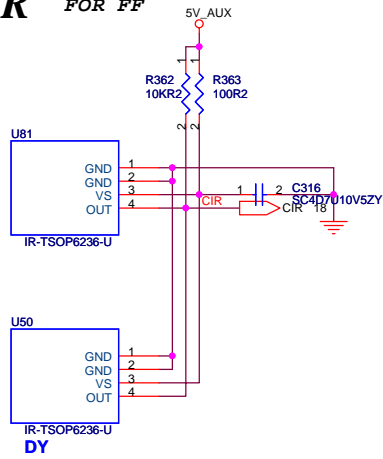
Date: Monday, July 11, 2005 Sheet: 19 of 47

CRT



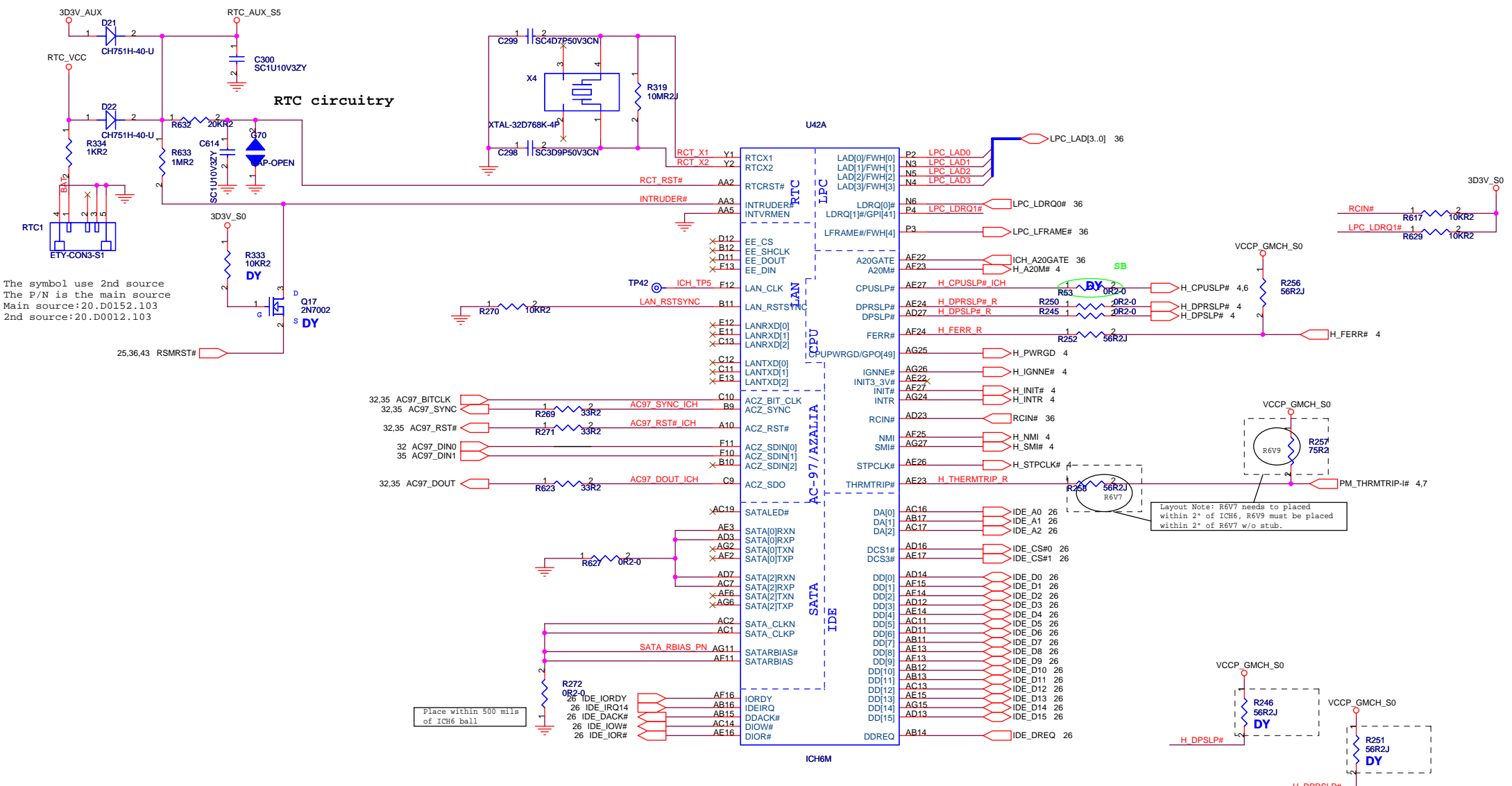
010804 Modified on Astro ID request

CIR FOR FF



<Core Design>

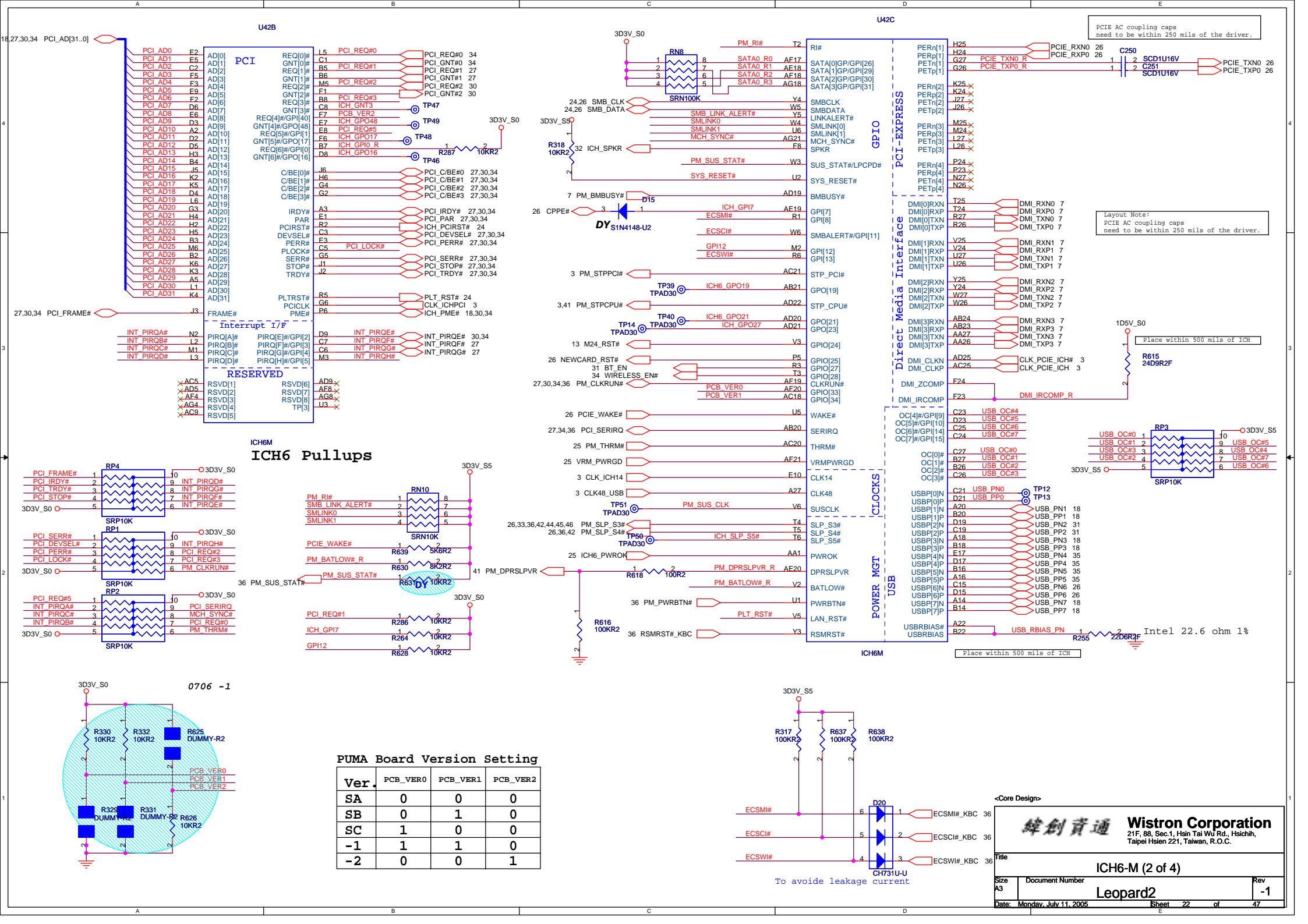
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT/ CIR	
Size A3	Document Number Leopard2
Date: Thursday, July 07, 2005	Rev -1
Sheet 20 of 47	



The symbol use 2nd source
 The P/N is the main source
 Main source: 20.D0152.103
 2nd source: 20.D0012.103

Place within 500 mils
 of ICH6 ball

Layout Note: R6V7 needs to be placed
 within 2" of ICH6, R6V9 must be placed
 within 2" of R6V7 w/o stub.



U42B

U42C

PCI AC coupling caps need to be within 250 mils of the driver.

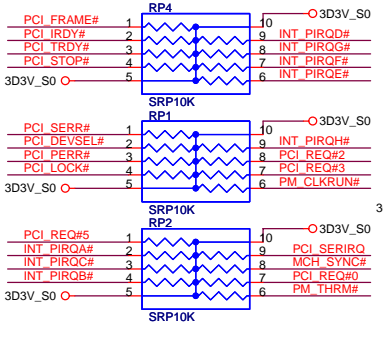
Layout Note: PCI AC coupling caps need to be within 250 mils of the driver.

Place within 500 mils of ICH

Place within 500 mils of ICH

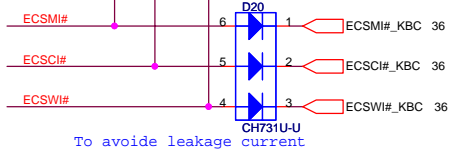
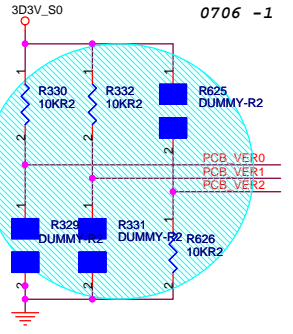
Place within 500 mils of ICH

ICH6M Pullups



PUMA Board Version Setting

Ver.	PCB_VER0	PCB_VER1	PCB_VER2
SA	0	0	0
SB	0	1	0
SC	1	0	0
-1	1	1	0
-2	0	0	1



Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH6-M (2 of 4)**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet: 22 of 47

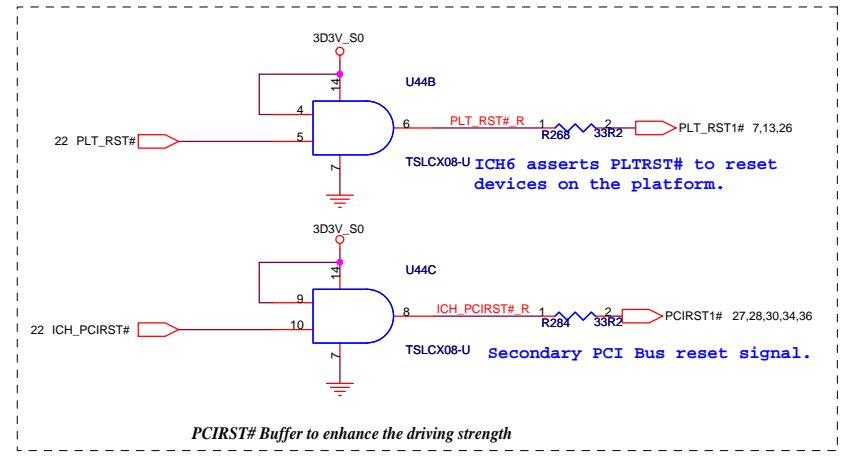
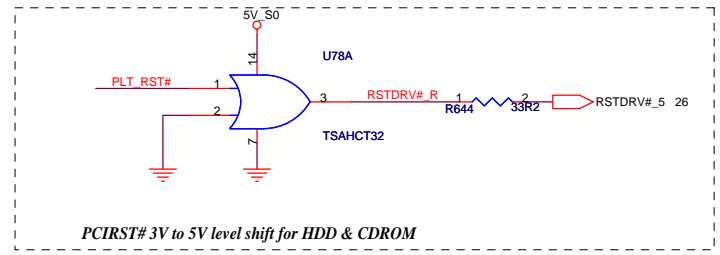
E27	VSS	VSS	F4
Y6	VSS	VSS	F22
Y27	VSS	VSS	F19
Y26	VSS	VSS	F17
Y23	VSS	VSS	F25
W7	VSS	VSS	E19
W25	VSS	VSS	E18
W24	VSS	VSS	E15
W23	VSS	VSS	E14
W1	VSS	VSS	D7
V4	VSS	VSS	D22
V27	VSS	VSS	D18
V26	VSS	VSS	D18
V23	VSS	VSS	D14
U25	VSS	VSS	D13
U24	VSS	VSS	D10
U23	VSS	VSS	D1
U15	VSS	VSS	C4
U13	VSS	VSS	C22
I7	VSS	VSS	C20
T27	VSS	VSS	C18
T26	VSS	VSS	C14
T23	VSS	VSS	B25
T16	VSS	VSS	B24
T15	VSS	VSS	B23
T14	VSS	VSS	B21
T13	VSS	VSS	B19
T12	VSS	VSS	B15
T1	VSS	VSS	B13
R4	VSS	VSS	AG7
R25	VSS	VSS	AG3
R24	VSS	VSS	AG22
R23	VSS	VSS	AG20
R17	VSS	VSS	AG17
R16	VSS	VSS	AG14
R15	VSS	VSS	AG12
R14	VSS	VSS	AG1
R13	VSS	VSS	AF7
R12	VSS	VSS	AF3
R11	VSS	VSS	AF26
P22	VSS	VSS	AF12
P16	VSS	VSS	AF10
P15	VSS	VSS	AF1
P14	VSS	VSS	AE7
P13	VSS	VSS	AE6
P12	VSS	VSS	AE25
N7	VSS	VSS	AE21
N17	VSS	VSS	AE2
N16	VSS	VSS	AE12
N15	VSS	VSS	AE11
N14	VSS	VSS	AE10
N13	VSS	VSS	AD6
N12	VSS	VSS	AD24
N11	VSS	VSS	AD2
N1	VSS	VSS	AD18
M4	VSS	VSS	AD15
M27	VSS	VSS	AD10
M26	VSS	VSS	AD1
M23	VSS	VSS	AC6
M16	VSS	VSS	AC3
M15	VSS	VSS	AC26
M14	VSS	VSS	AC24
M13	VSS	VSS	AC23
M12	VSS	VSS	AC22
L25	VSS	VSS	AC12
L24	VSS	VSS	AC10
L23	VSS	VSS	AB9
L15	VSS	VSS	AB7
L13	VSS	VSS	AB2
K7	VSS	VSS	AB19
K27	VSS	VSS	AB10
K26	VSS	VSS	AB1
K23	VSS	VSS	AA4
K1	VSS	VSS	AA16
J4	VSS	VSS	AA13
J25	VSS	VSS	AA11
J24	VSS	VSS	A9
J23	VSS	VSS	A7
H27	VSS	VSS	A4
H26	VSS	VSS	A26
H23	VSS	VSS	A23
G9	VSS	VSS	A21
G7	VSS	VSS	A19
G21	VSS	VSS	A15
G12	VSS	VSS	A12
G1	VSS	VSS	A1

VSS

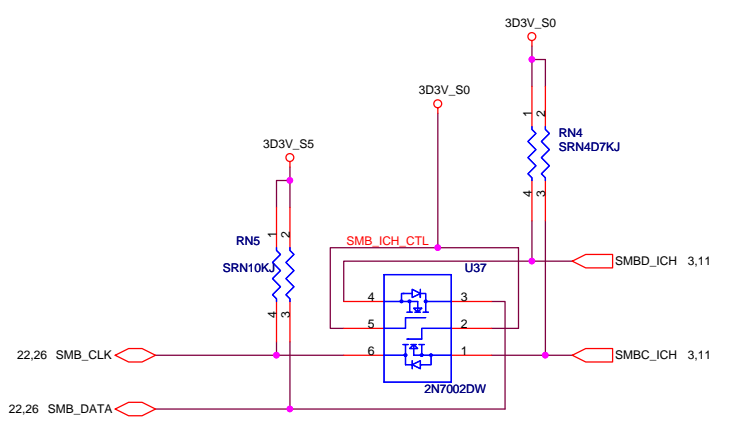
ICH6M

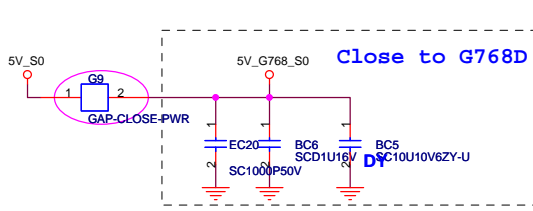
<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		ICH6-M (4 of 4)	
Size	Document Number	Rev	
A3		-1	
Leopard2			
Date: Thursday, July 07, 2005	Sheet 24	of 47	

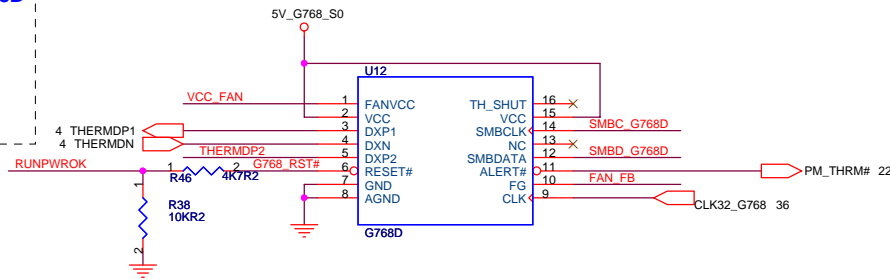


SMBUS (ICH6 ---> SODIMM, CLKGEN)

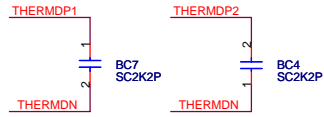
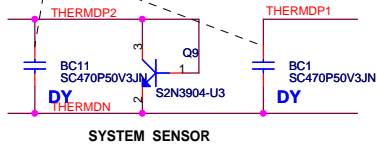




Reserve for G768B works at High Speed

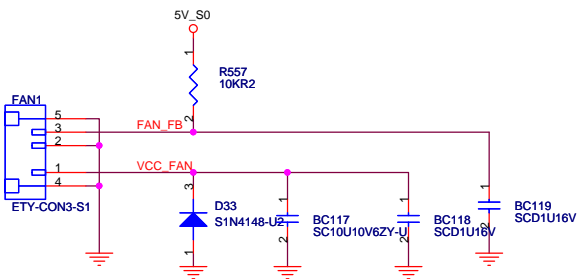


Put these two Caps near the thermal diode.

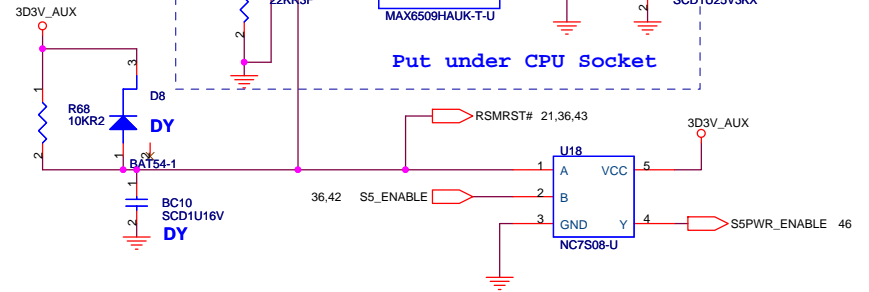
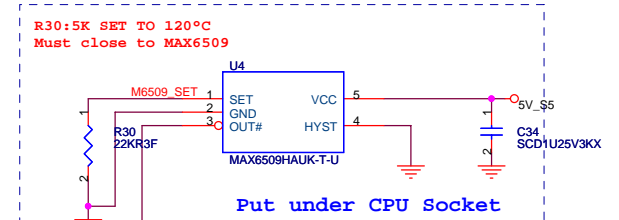
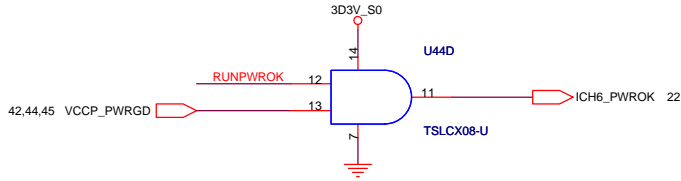
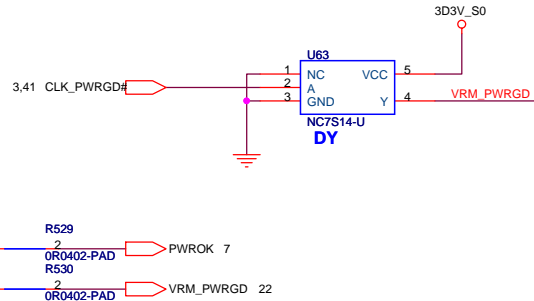


THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

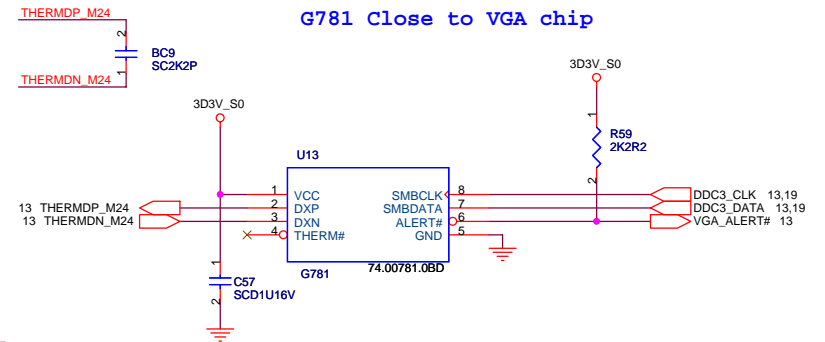
180 ms after VCC_G768 > 4.38v, p2, 7



The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103



G781 Close to VGA chip

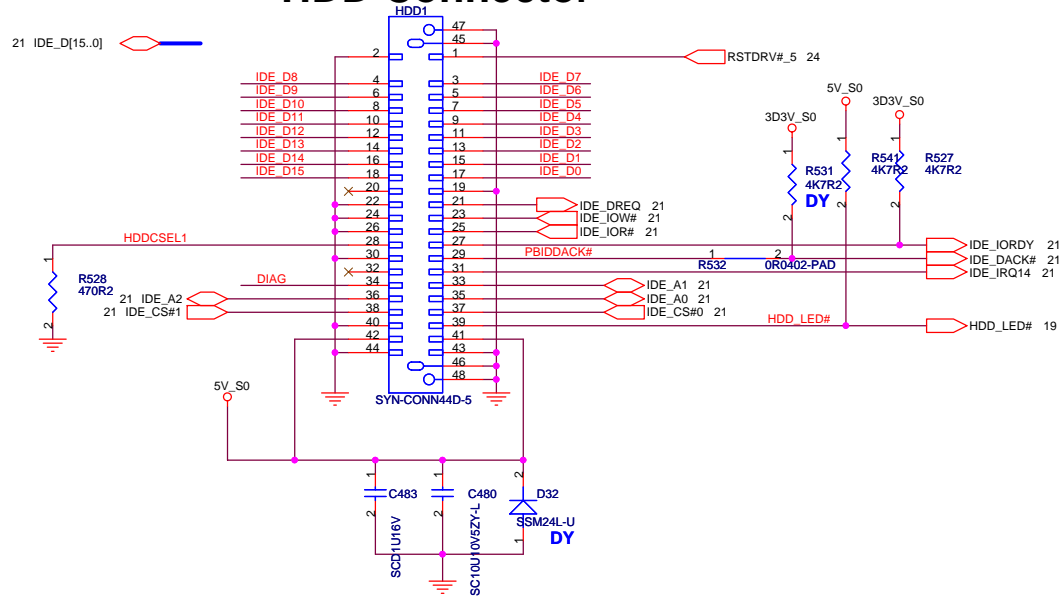


<Core Design>

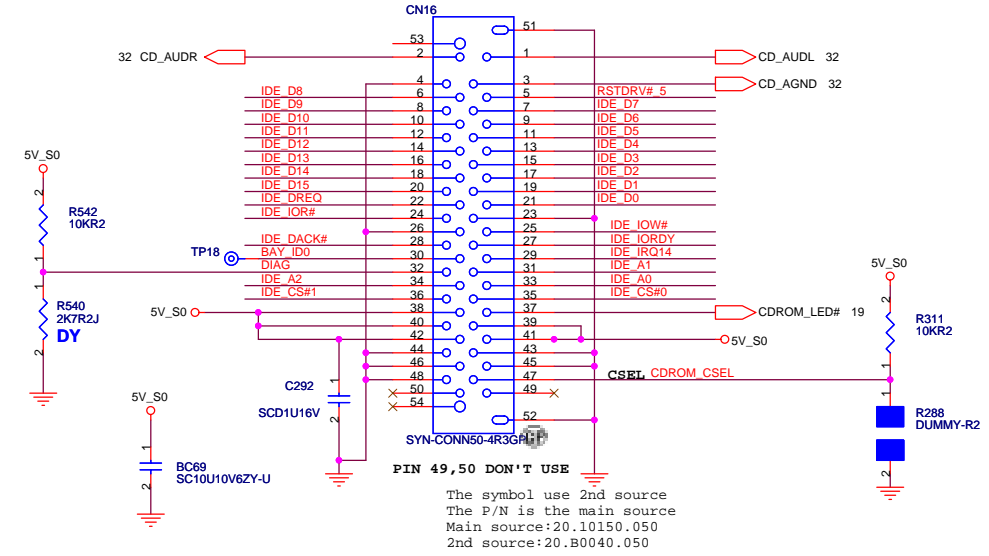
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			G768D		
Size	Document Number		Rev		
A3	Leopard2		-1		
Date:	Monday, July 11, 2005	Sheet	25	of	47

HDD Connector

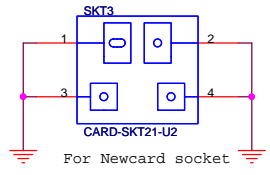
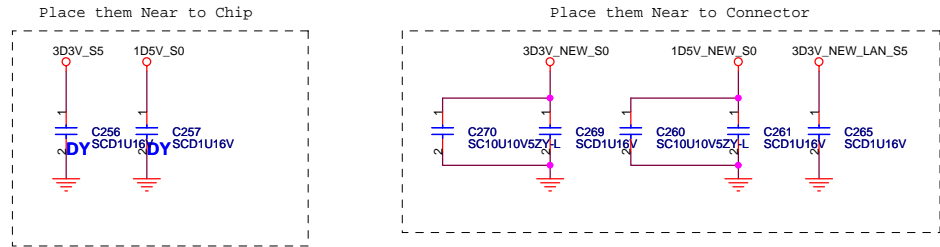


CDROM

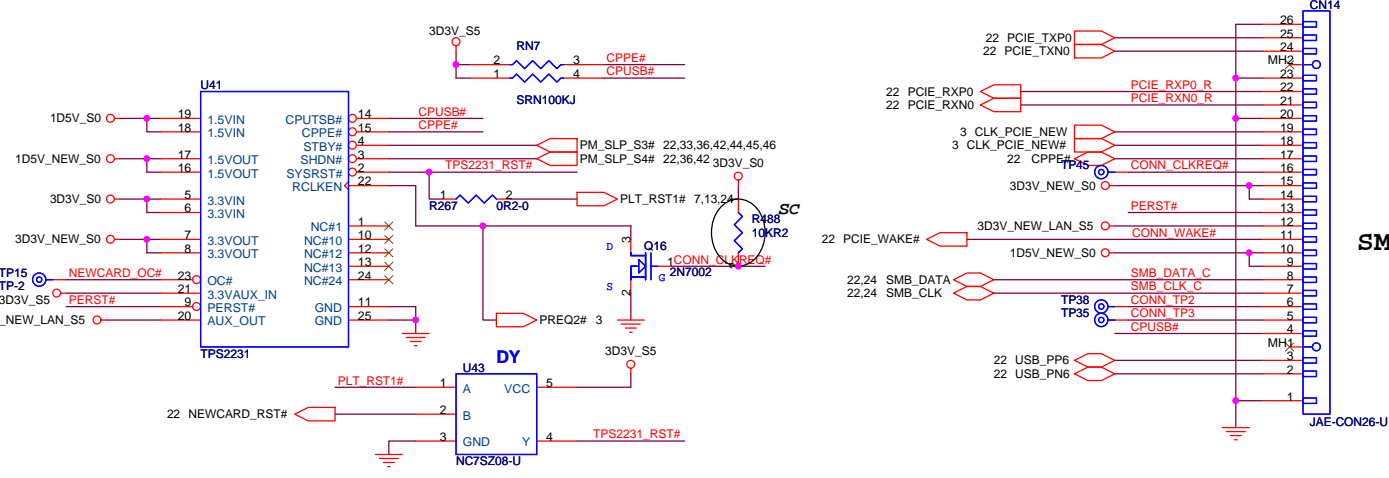


The symbol use 2nd source
 The P/N is the main source
 Main source:20.10150.050
 2nd source:20.B0040.050

NEWCARD Connector



SMBUS (ICH6 -- NEWCARD , LAN)

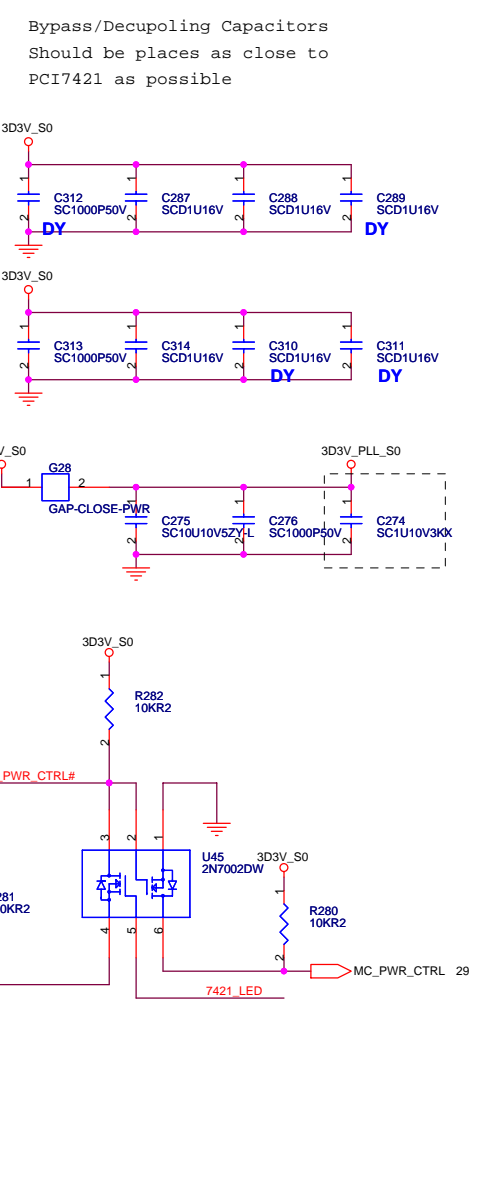
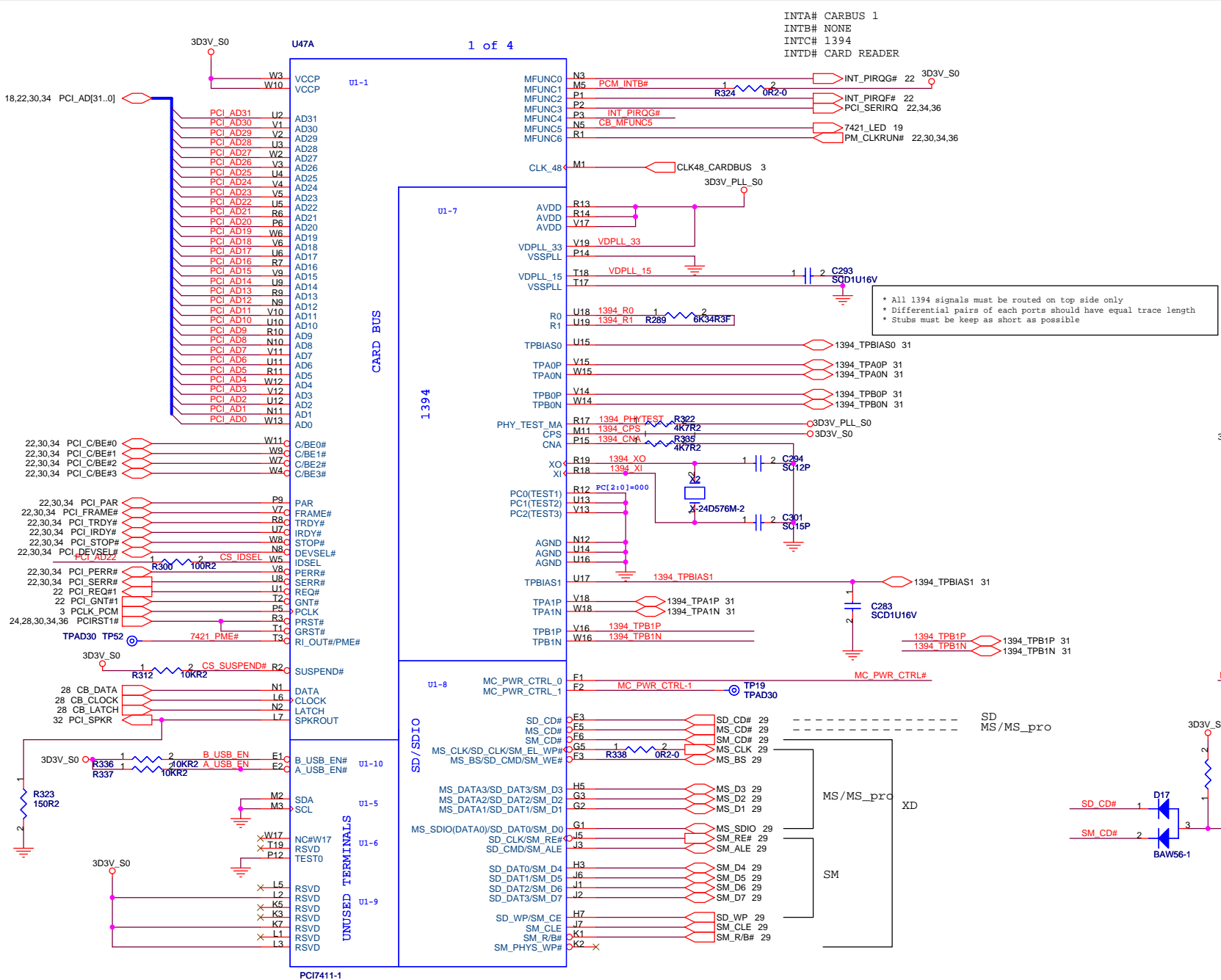


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD / CDROM/NEWCARD**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet: 26 of 47



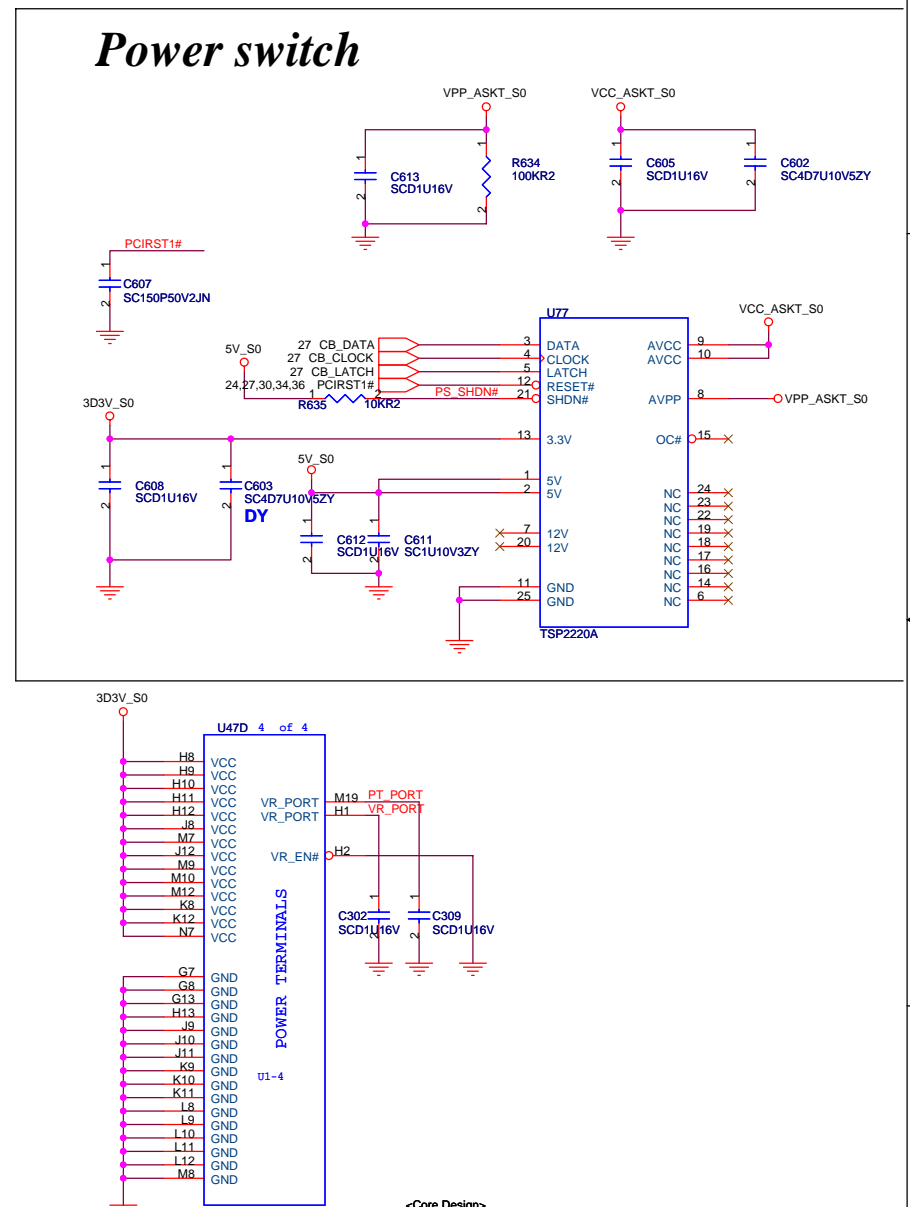
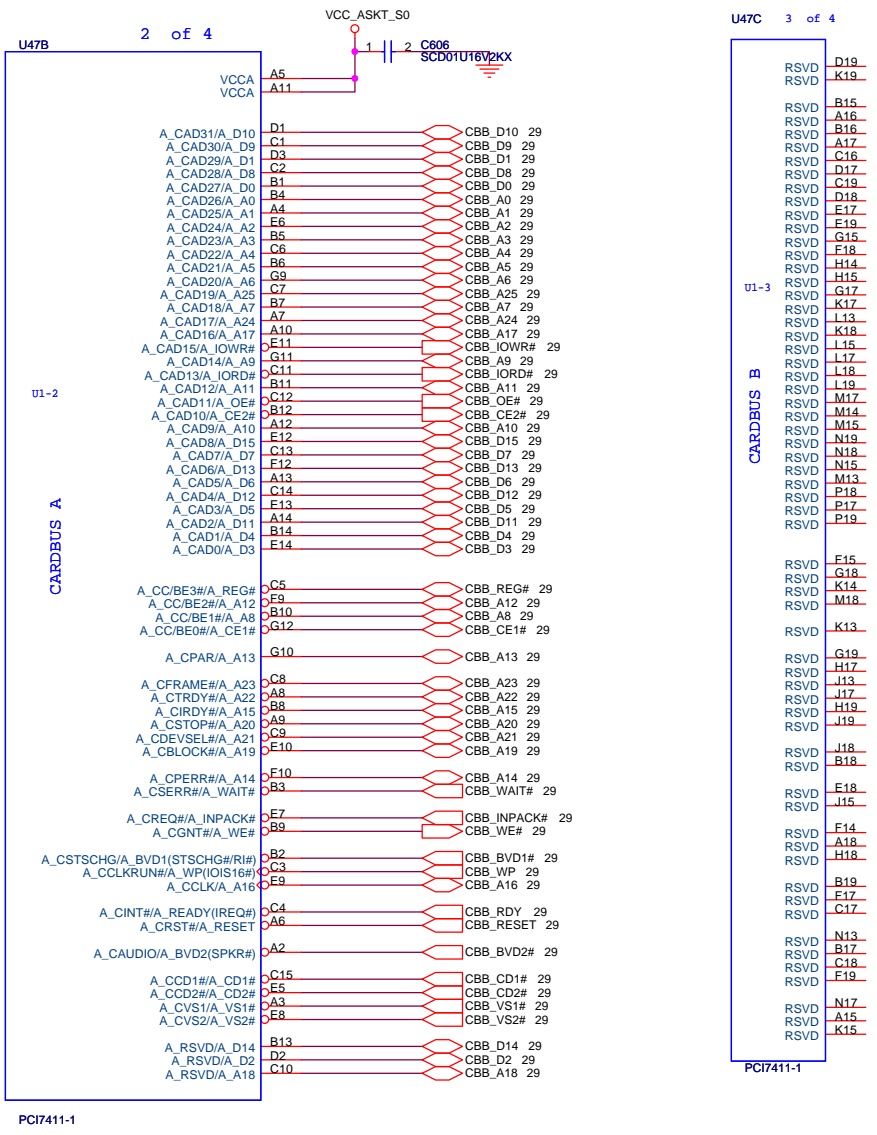
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI SNC1Q21 (1 of 2)**

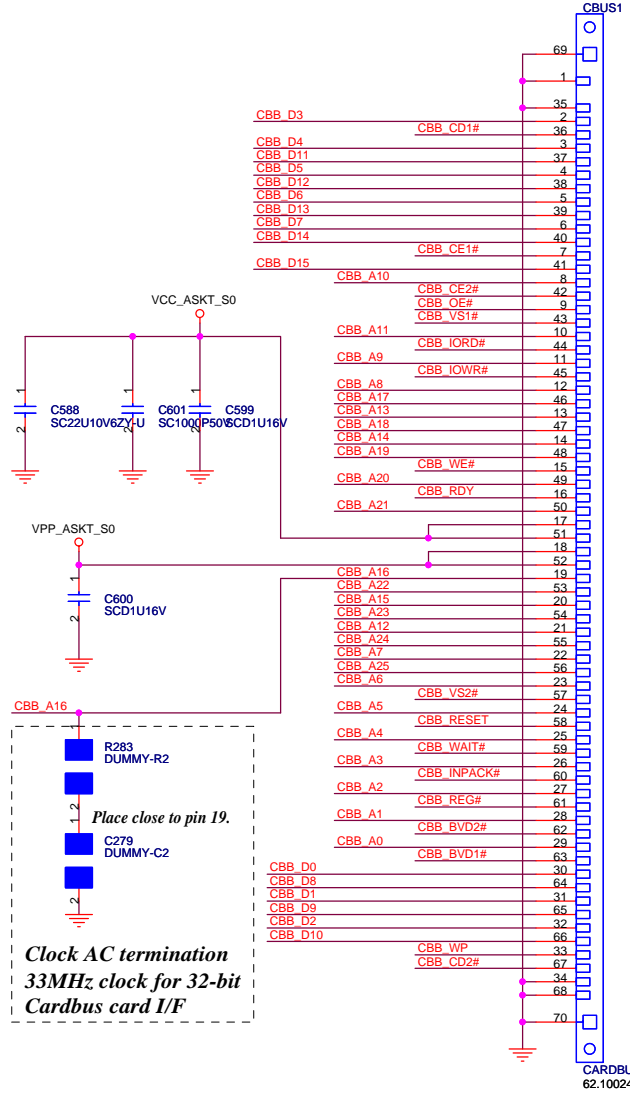
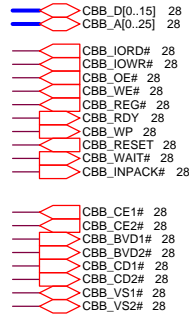
Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Monday, July 11, 2005 Sheet: 27 of 47

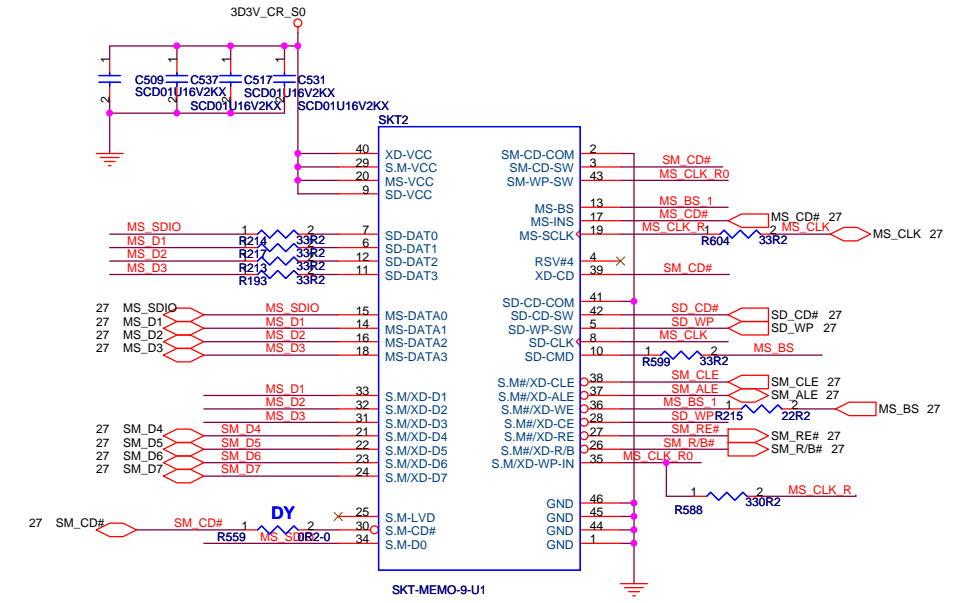


PCMCIA Socket

Cardbus I/F



6 in 1 Connector



Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

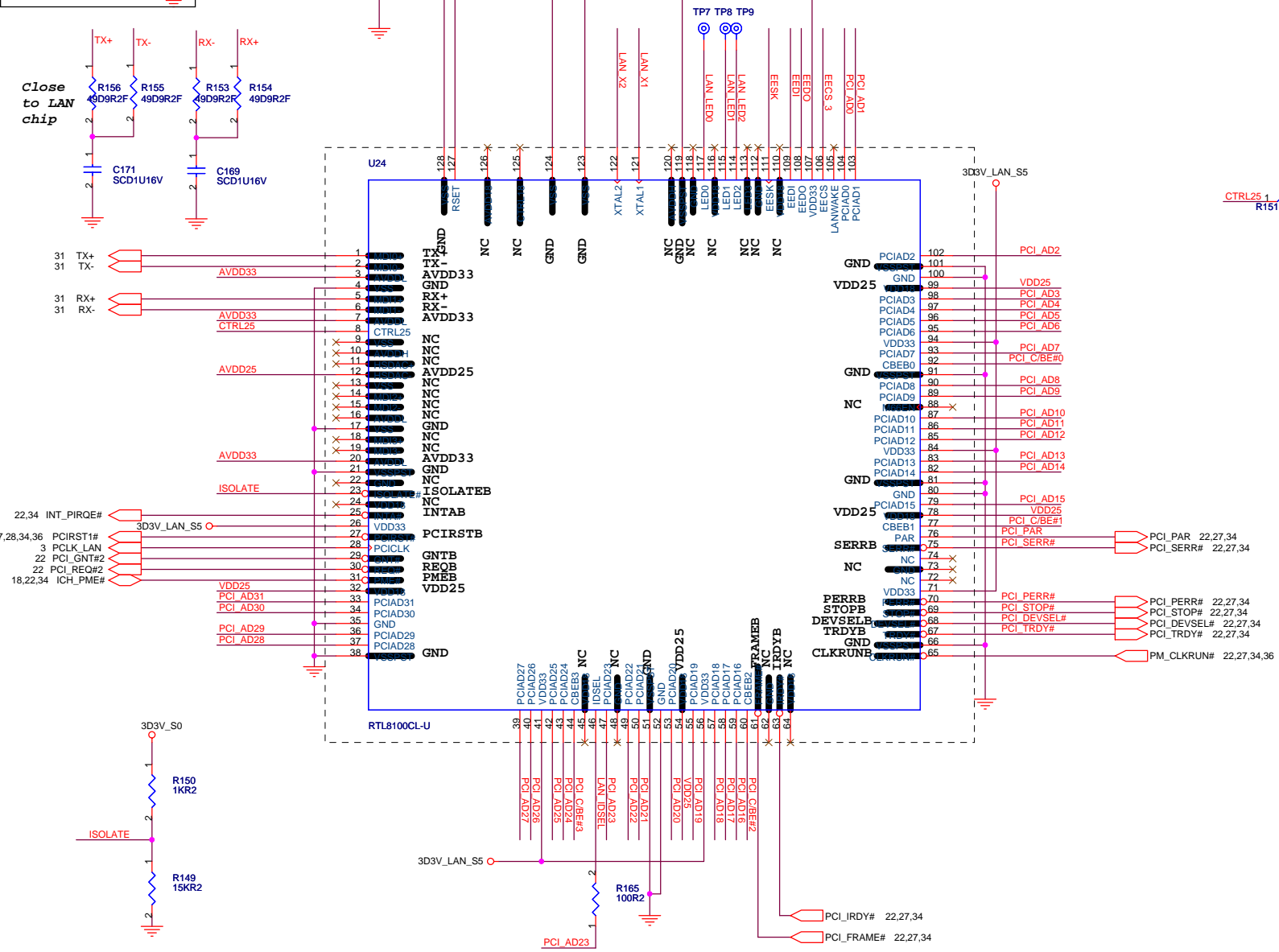
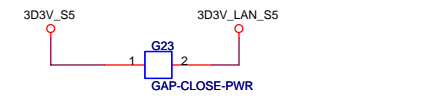
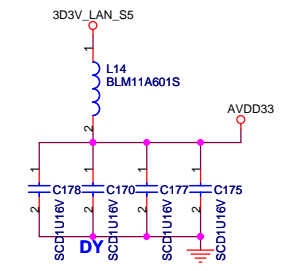
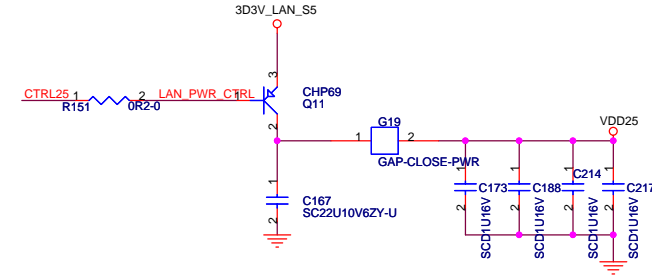
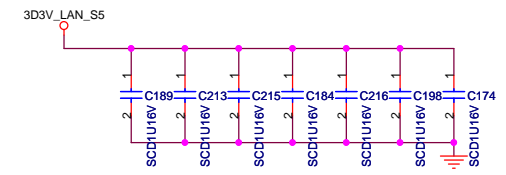
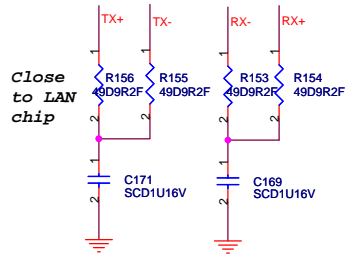
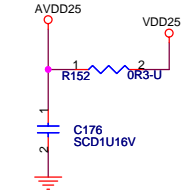
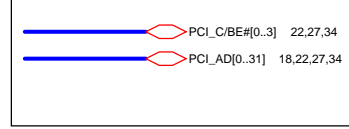
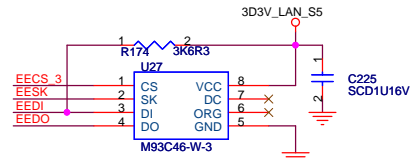
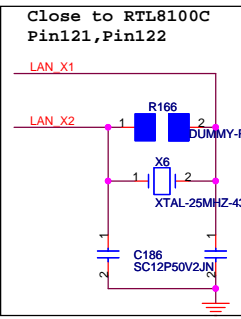
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCMCIA SLOT/ CARDBUS SKT**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 29 of 47



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN RTL8100C**

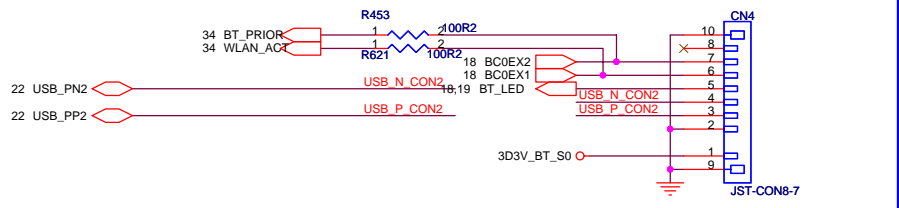
Size A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet 30 of 47

Blue thumb

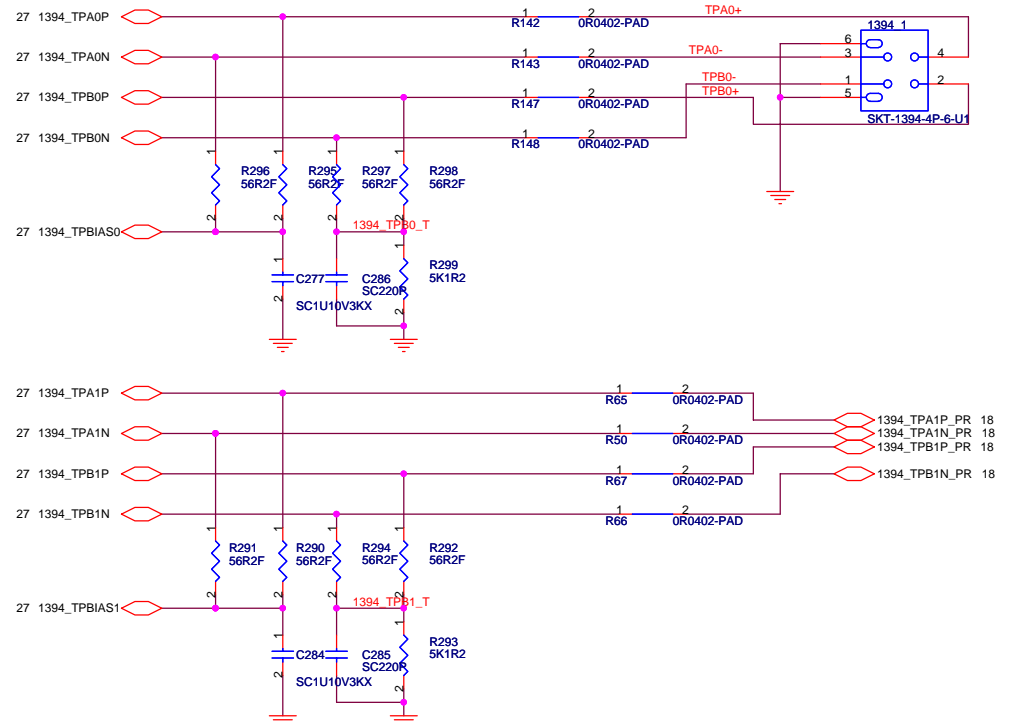
Place on bottom side

From NEW!
1004-1



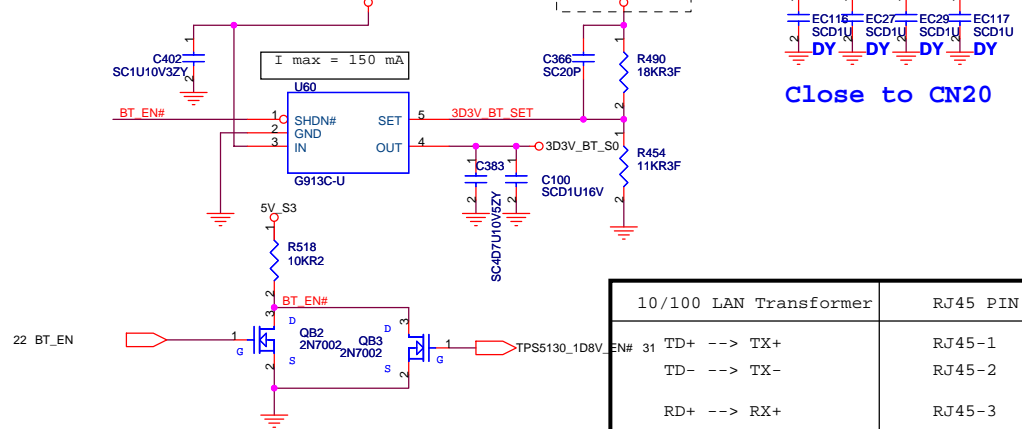
BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PMB# on main board.

1394 Connector



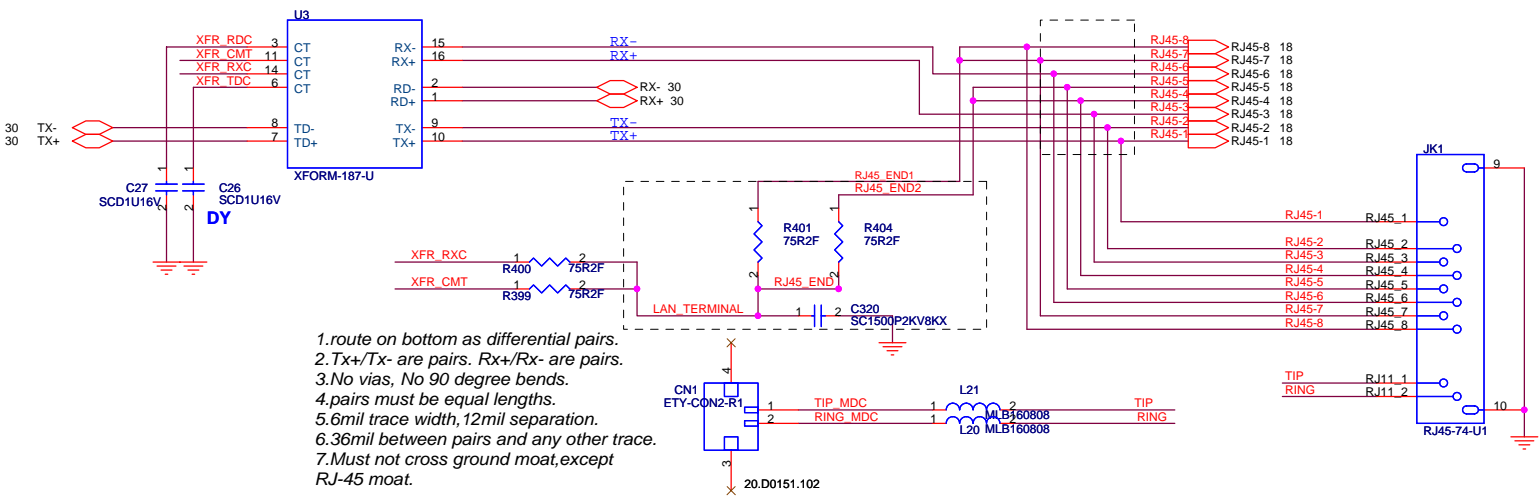
These components near to chip side.

POWER SWITCH



10/100 LAN Transformer	RJ45 PIN
TD+ ---> TX+	RJ45-1
TD- ---> TX-	RJ45-2
RD+ ---> RX+	RJ45-3
RD- ---> RX-	RJ45-6

10/100M Lan Transformer



- route on bottom as differential pairs.
- Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- No vias, No 90 degree bends.
- pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- Must not cross ground moat, except RJ-45 moat.

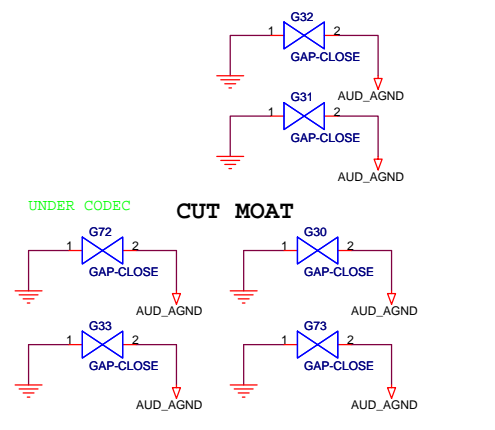
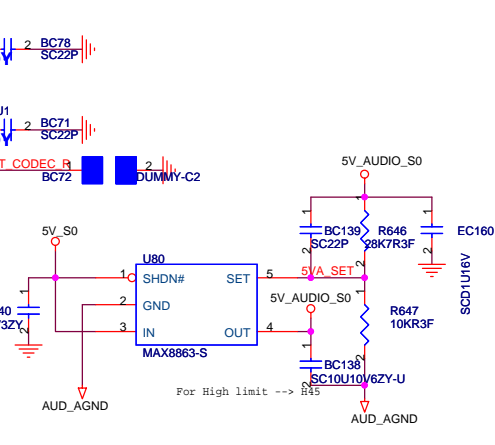
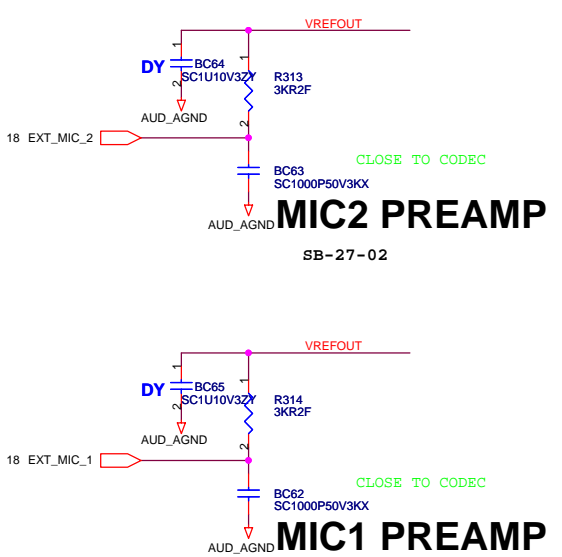
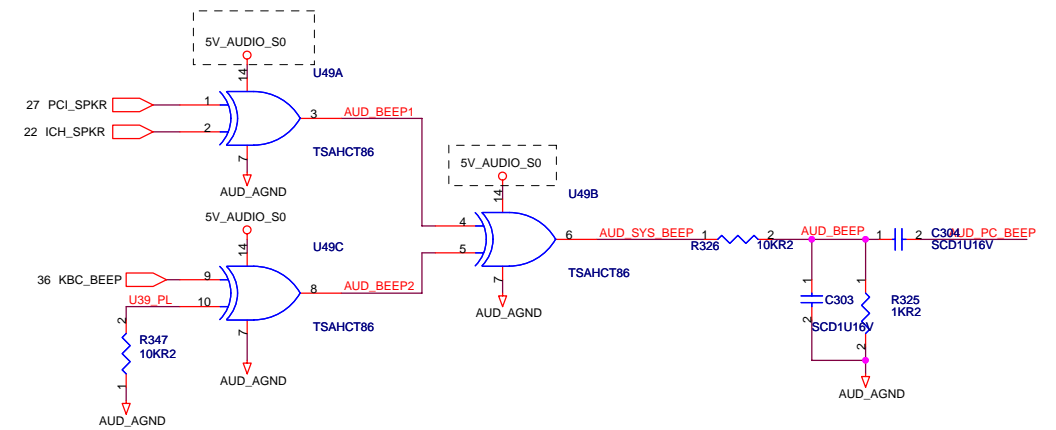
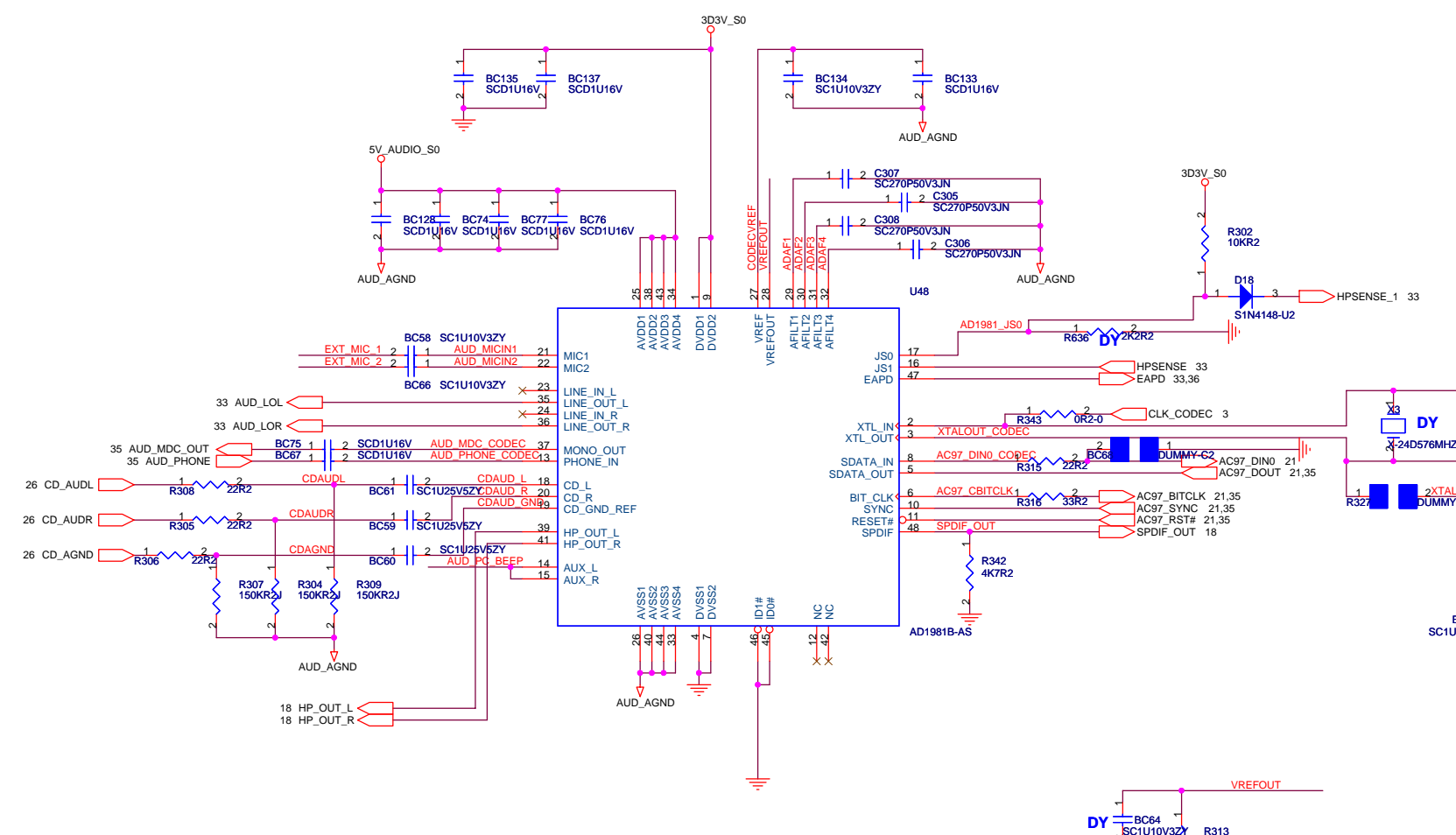
<Core Design>

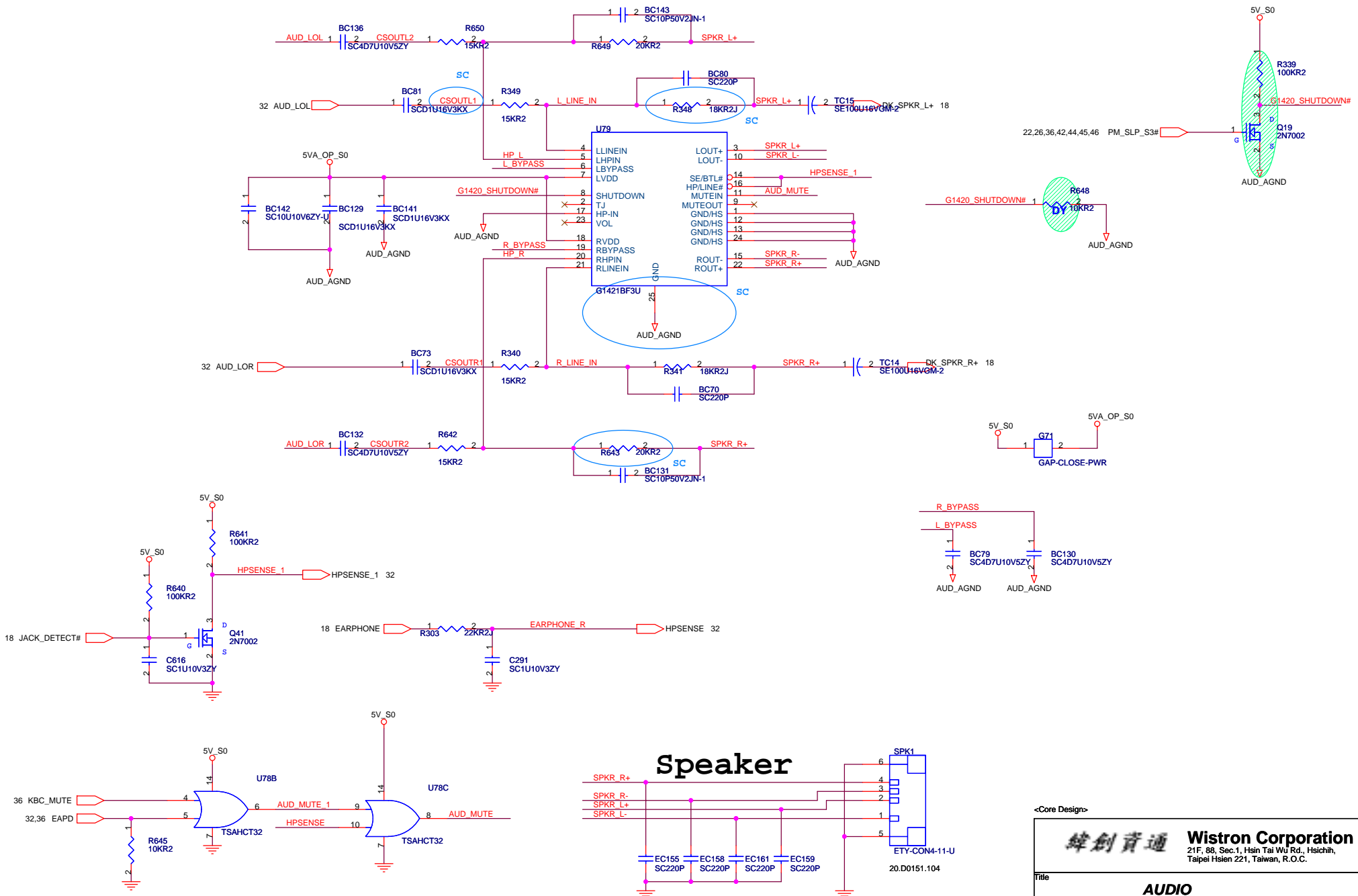
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN / 1394 Connector**

Size A3 Document Number **Leopard2** Rev **-1**

Date: Monday, July 11, 2005 Sheet 31 of 47





<Core Design>

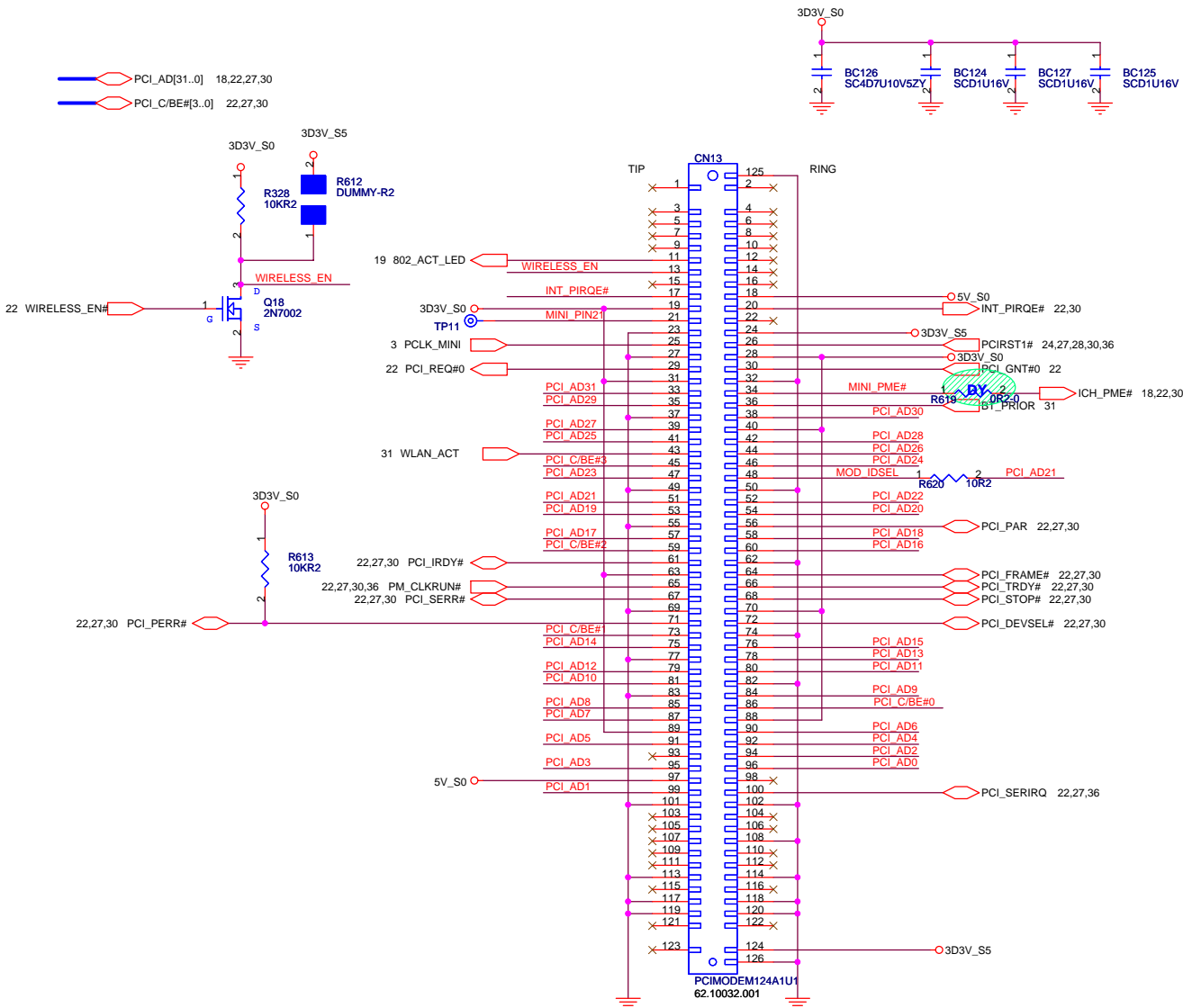
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO**

Size: A3 Document Number: **Leopard2** Rev: **-1**


Date: Thursday, July 07, 2005 Sheet: 33 of 47

MINI-PCI

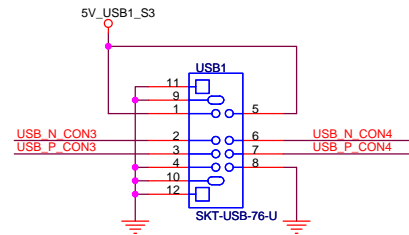
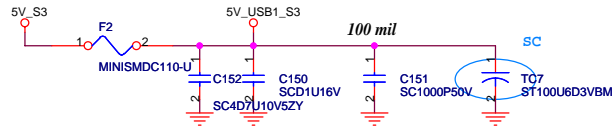


The symbol use 2nd source
 The P/N is the main source
 Main source:62.10032.001
 2nd source:62.10032.031

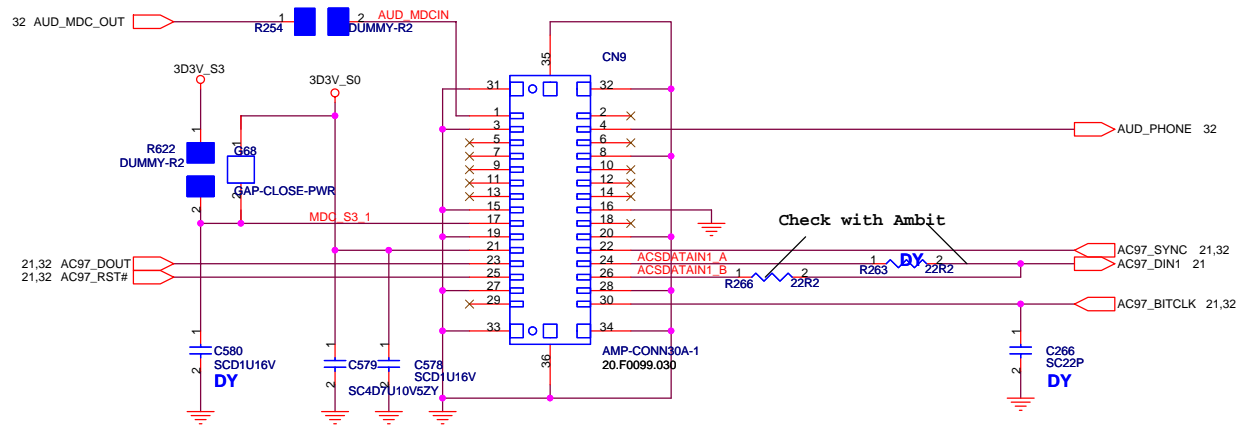
<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MINI-PCI	
Title	
Size A3	Document Number
Date: Thursday, July 07, 2005	Sheet 34 of 47
Rev -1	

USB POWER



MDC Connector

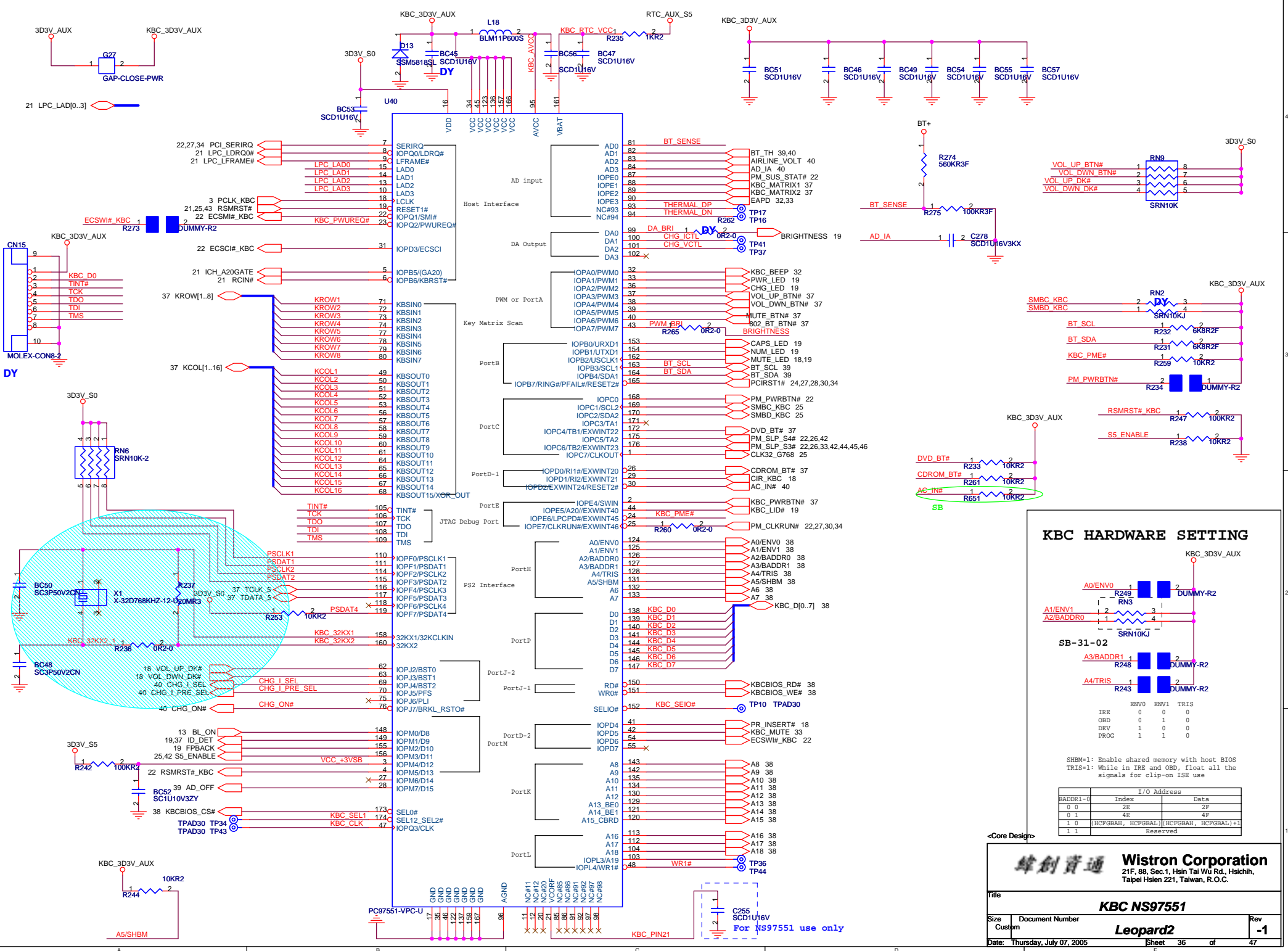


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB / MDC CONN.**

Size: A3	Document Number: Leopard2	Rev: -1
Date: Thursday, July 07, 2005	Sheet: 35	of 47



KBC HARDWARE SETTING

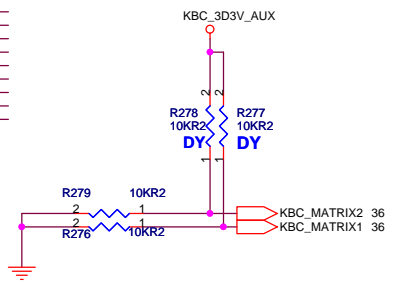
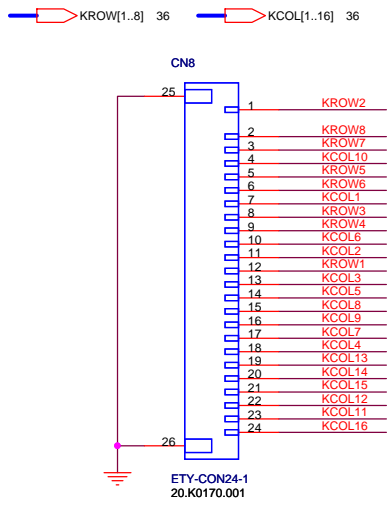
SB-31-02

IRE	ENVO	ENV1	TRIS
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	0

SHM=1: Enable shared memory with host BIOS
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

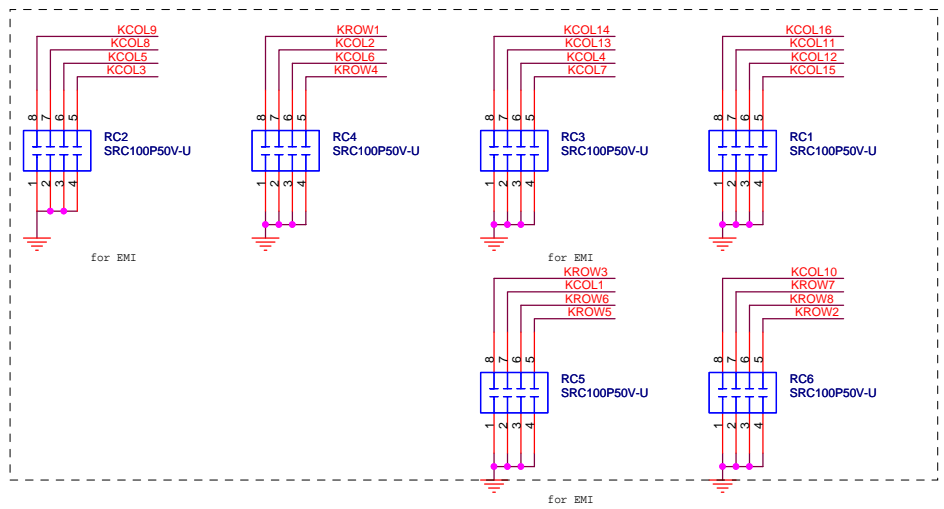
BADDR1-0	Index	I/O Address	Data
0	2E	2F	
0	4E	4F	
1	0	[HCFGBAH, HCFGBAL, HCFGBAH, HCFGBAL]+1	
1	1	Reserved	

INTERNAL KEYBOARD CONNECTOR

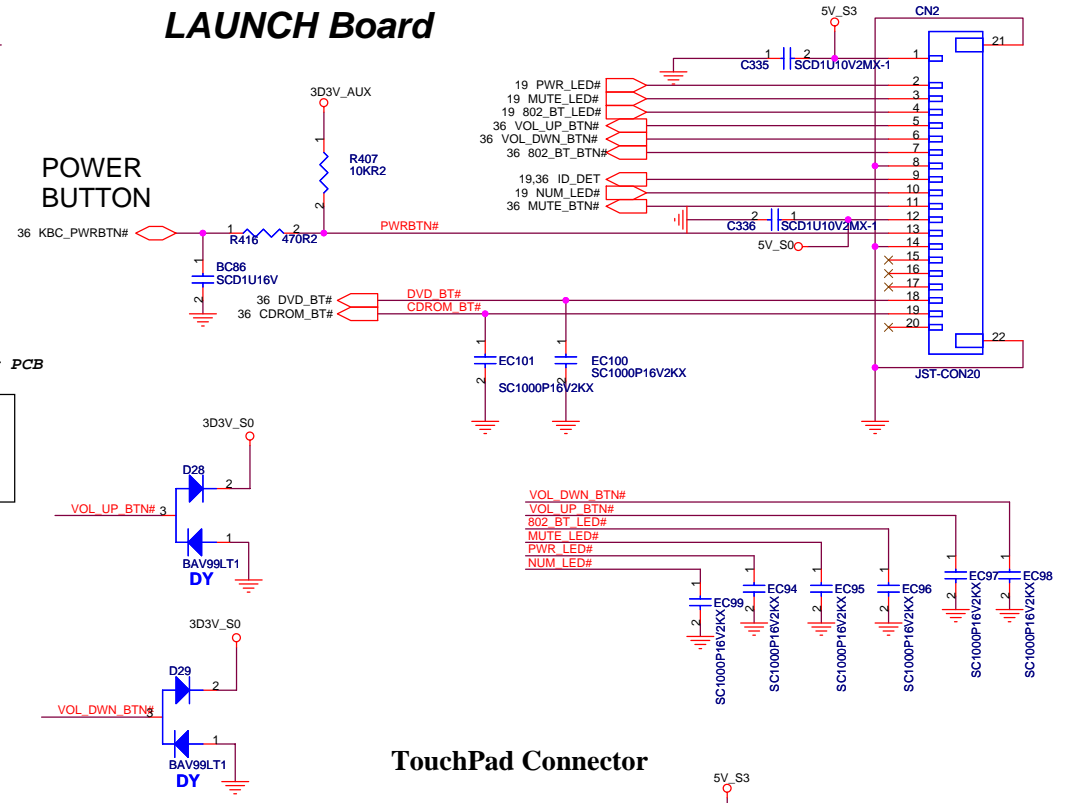


the matrix table for PCB

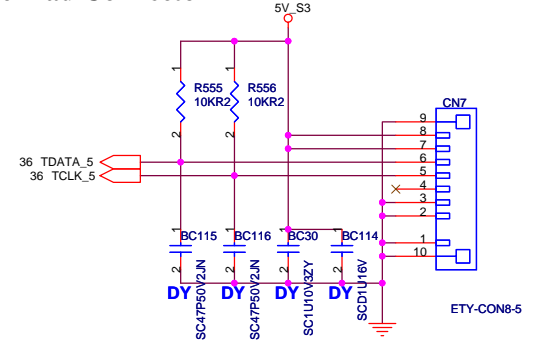
	PA	PR
Discrete	00	01
UMA	10	11



LAUNCH Board



TouchPad Connector



<Core Design>

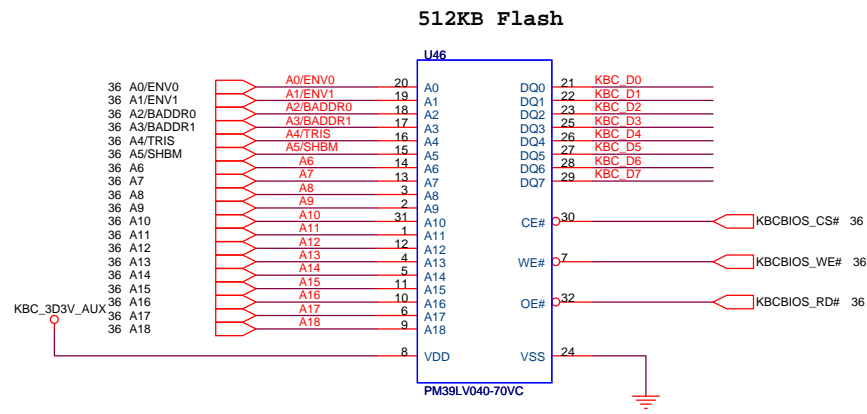
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KEYBOARD/TOUCH PAD/Launch key**

Size: A3, Document Number: **Leopard2**, Rev: **-1**

Date: Thursday, July 07, 2005, Sheet: 37 of 47

FLASH ROM



KBC_D[0..7] 36

<Core Design>

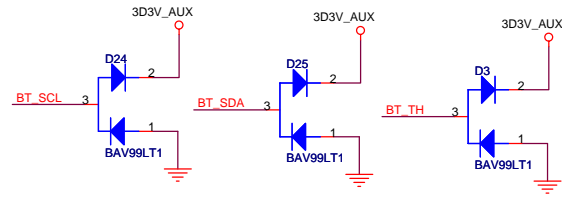
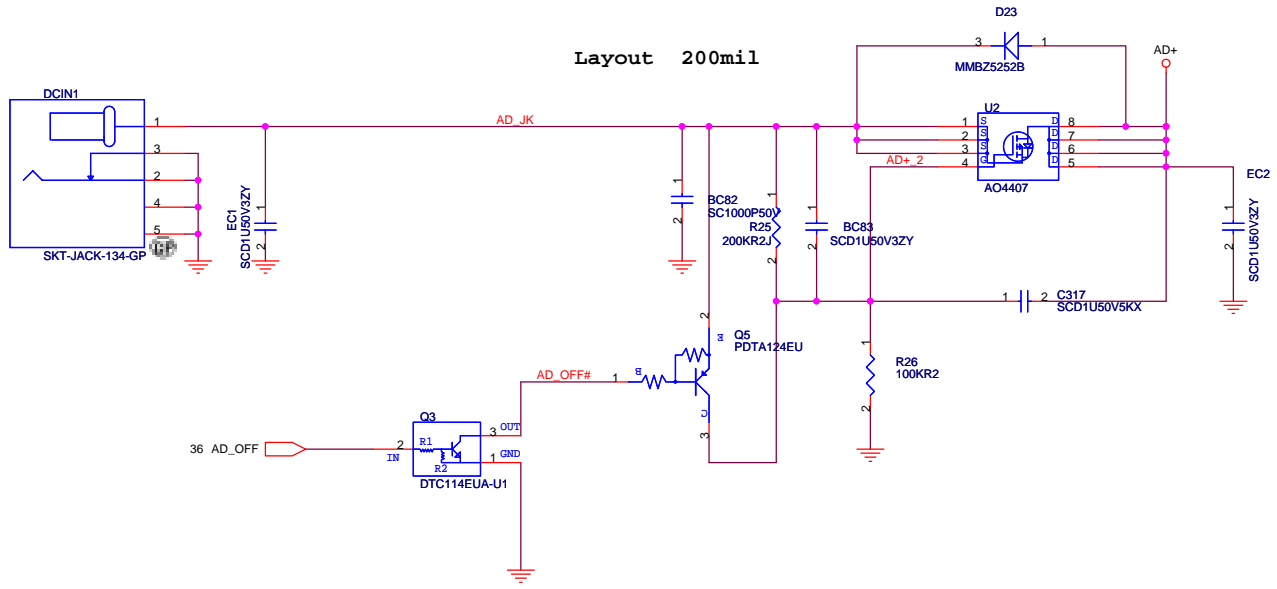
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS/GF**

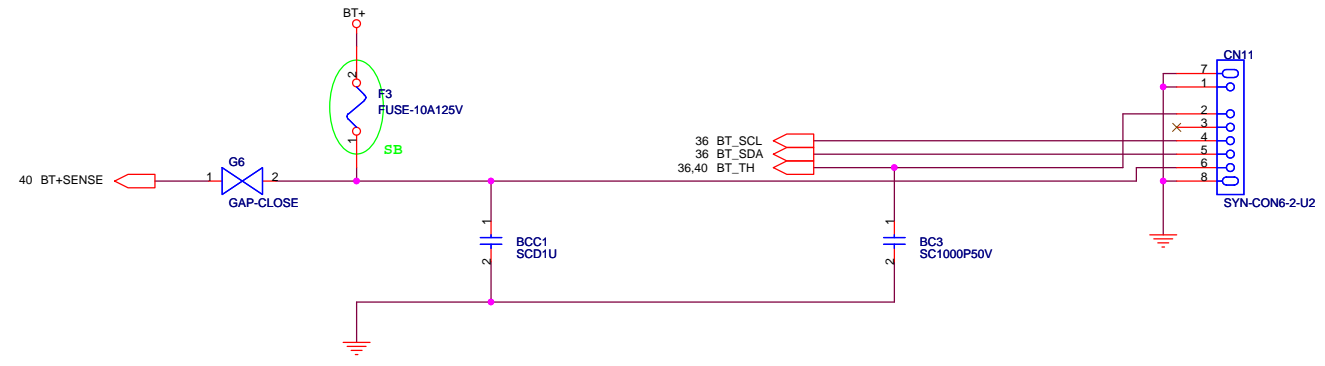
Size: A3	Document Number: Leopard2	Rev: -1
----------	----------------------------------	----------------

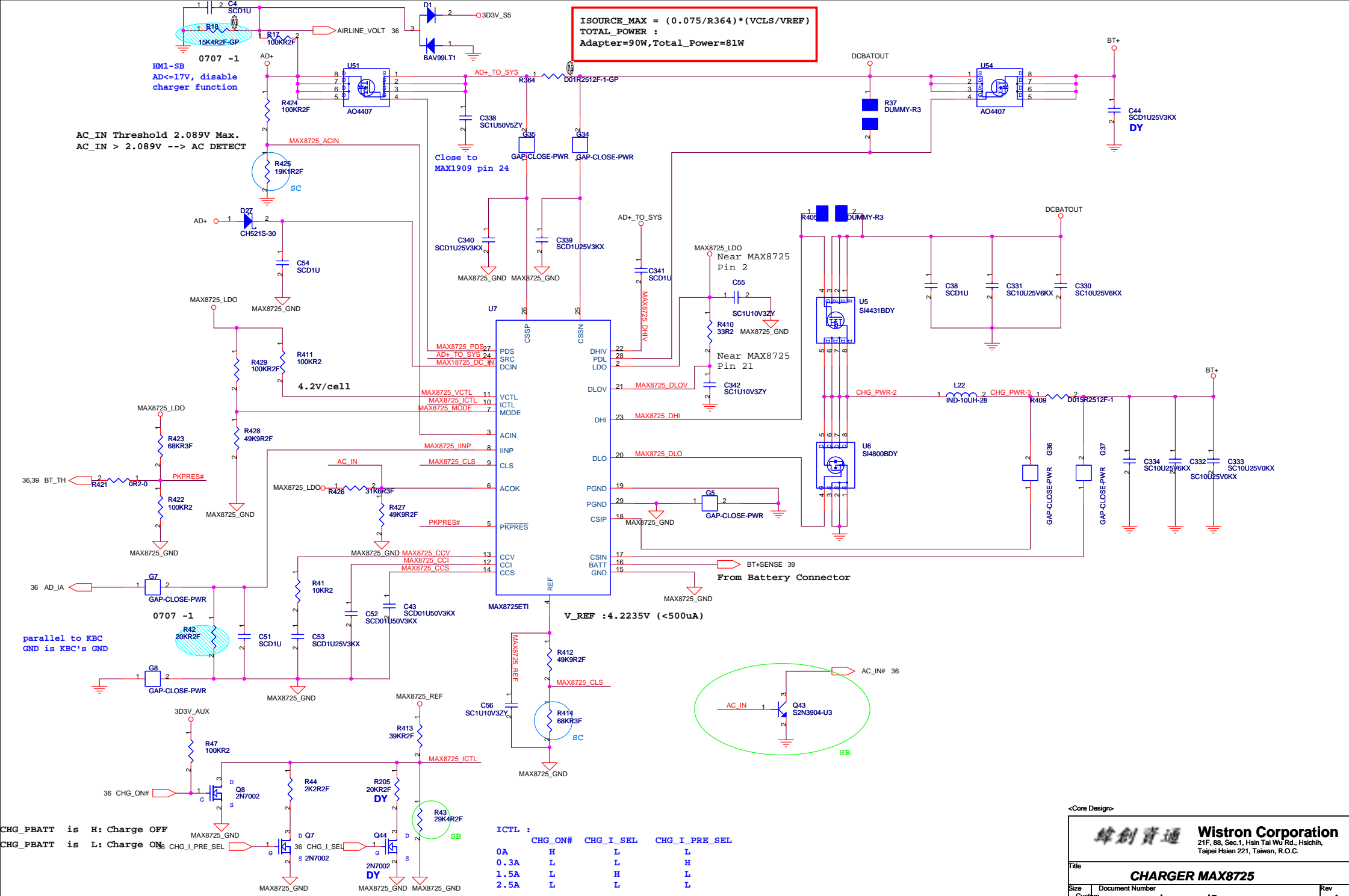
Date: Thursday, July 07, 2005 Sheet 38 of 47

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





AC_IN Threshold 2.089V Max.
 AC_IN > 2.089V --> AC DETECT

parallel to KBC
 GND is KBC's GND

CHG_PBATT is H: Charge OFF
 CHG_PBATT is L: Charge ON

If Charger is MAX1909, dummy them.

<Core Design>

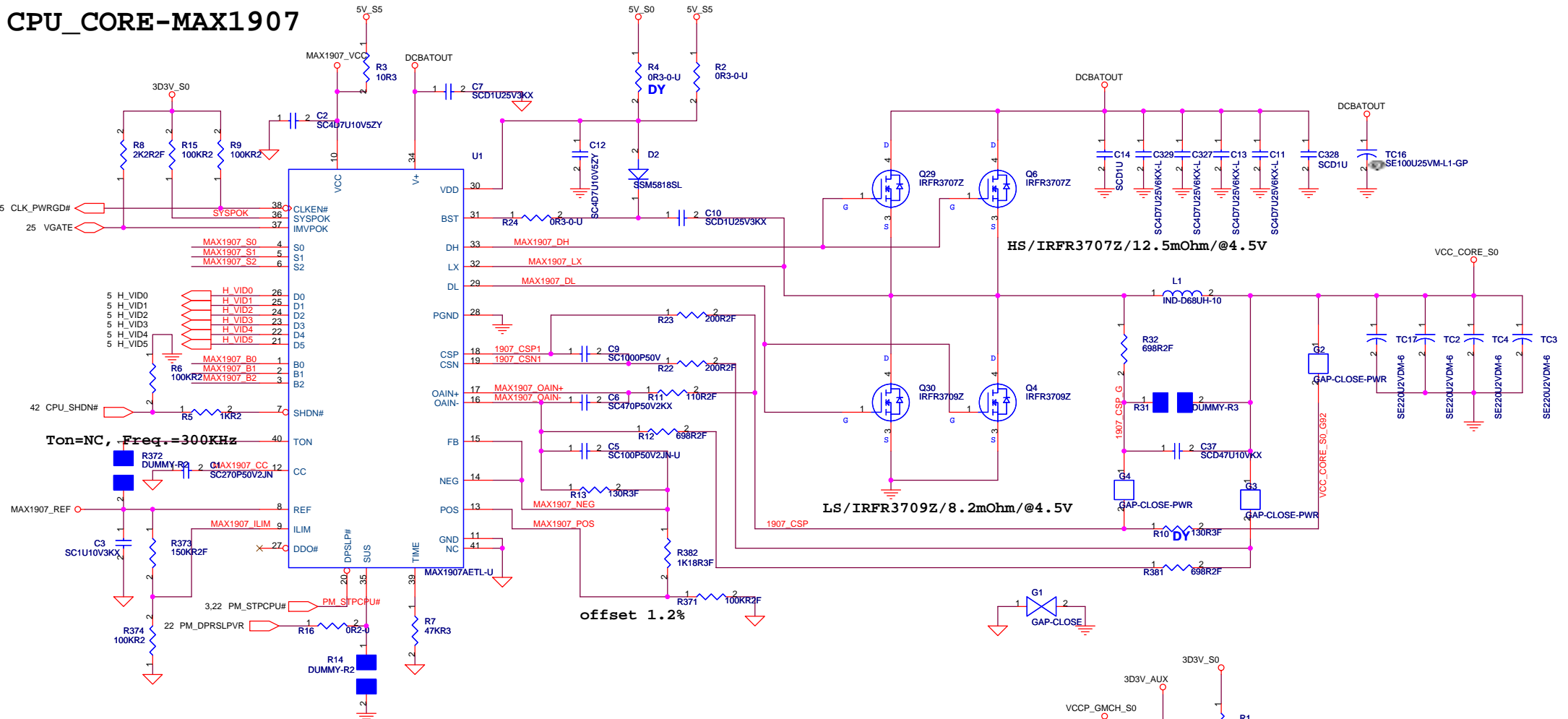
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8725**

Size: Document Number
 Custom: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet 40 of 47

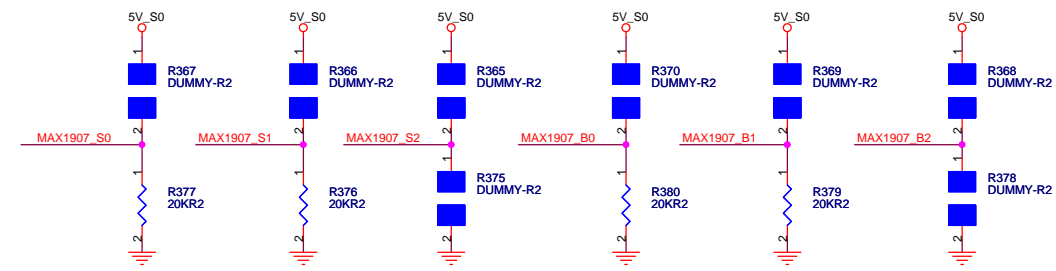
CPU_CORE-MAX1907



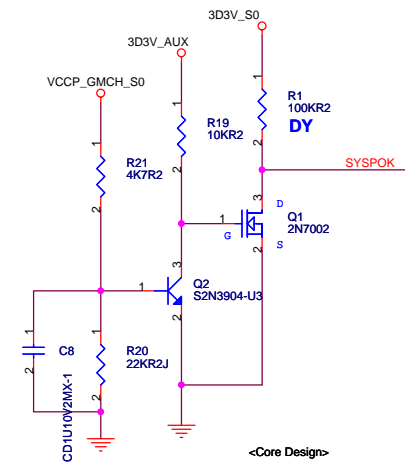
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	v
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



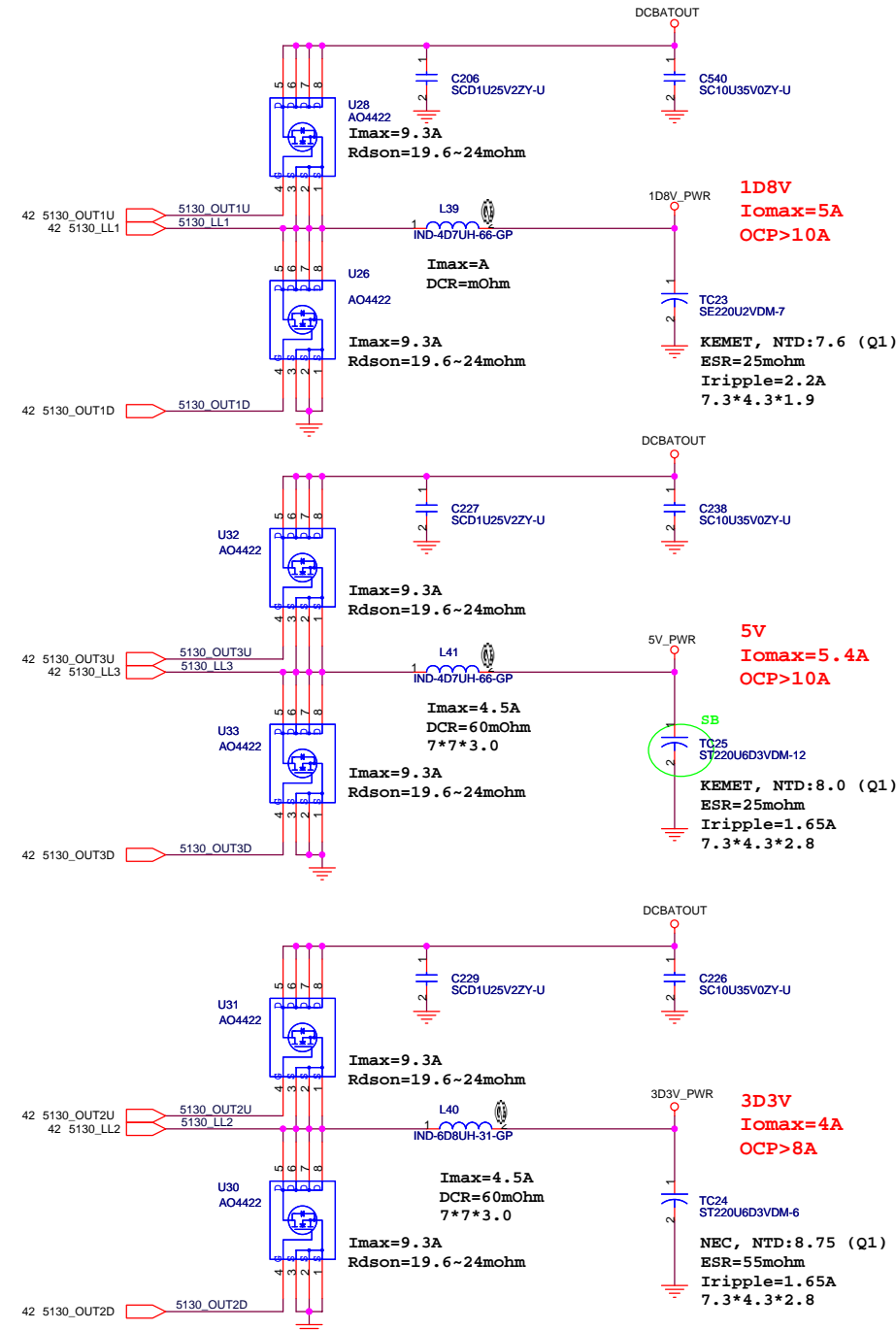
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

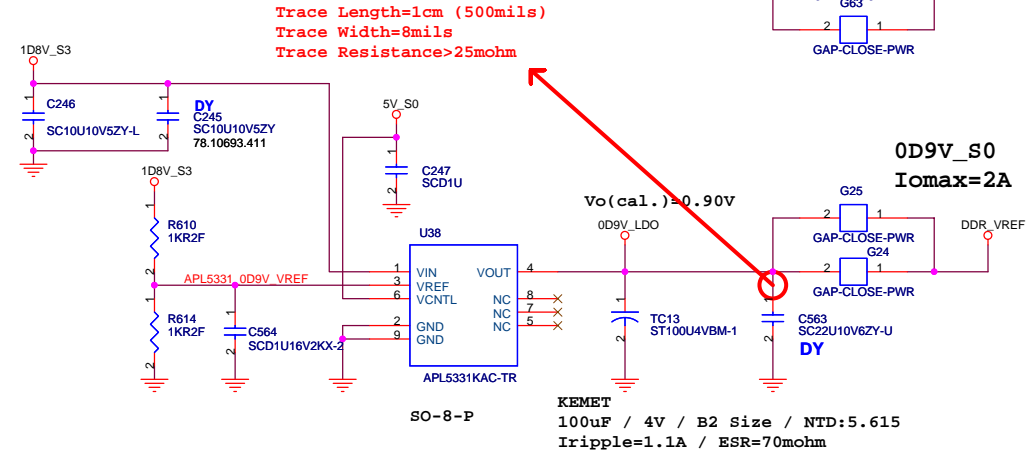
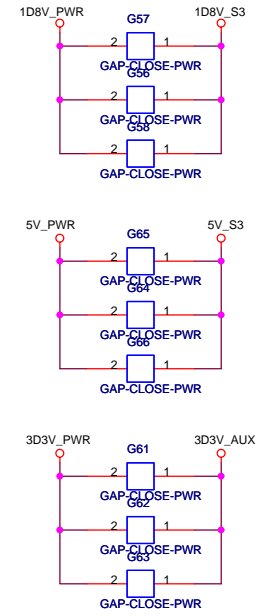
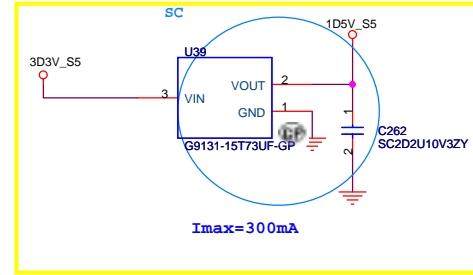
Title	IMVP IV-CPU POWER-MAX1907	
Size	Document Number	Rev
A3	Leopard2	-1
Date: Monday, July 11, 2005	Sheet 41	of 47

TI TPS5130 for 1D2V, 5V, 3D3V

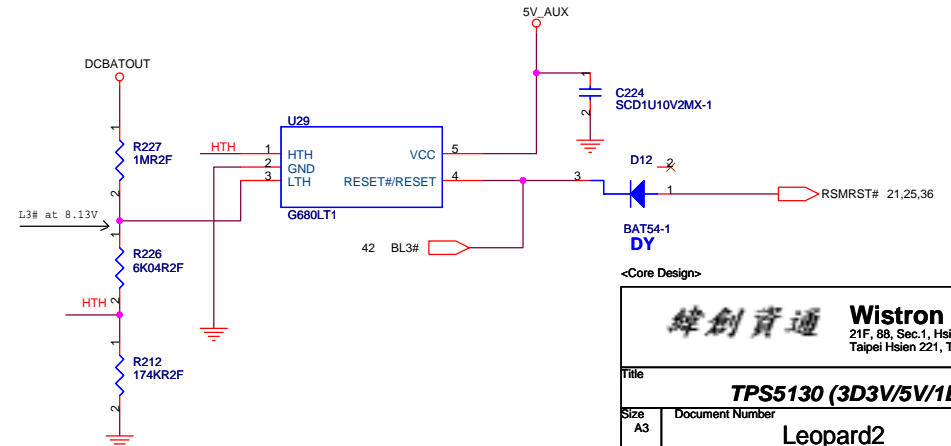
(1D2V=>CH1 , 5V=>CH2 , 3D3V =>CH3)



1.5V_S5 (For ICH6)



L3# circuit



緯創資通 Wistron Corporation
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

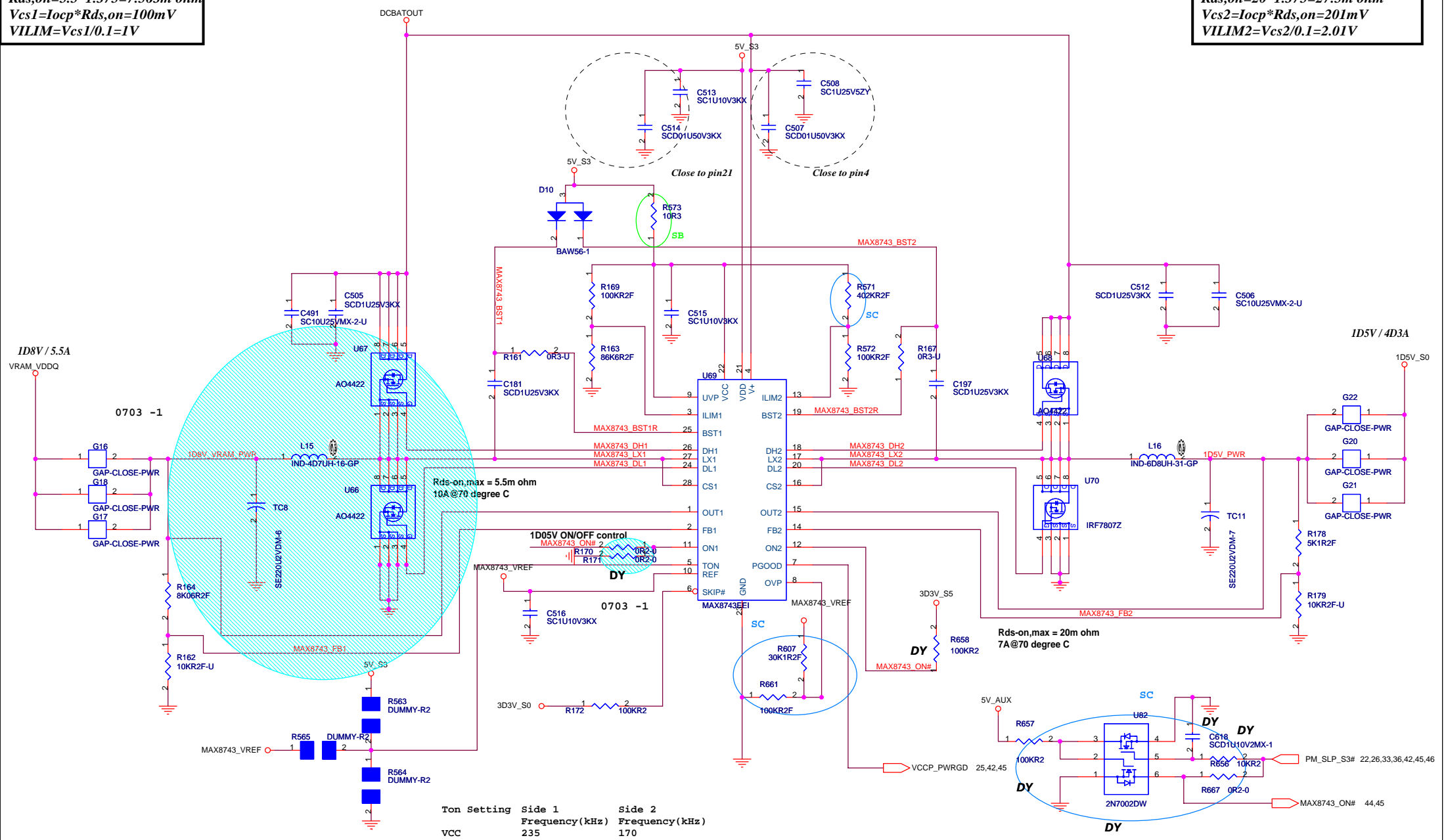
Title: **TPS5130 (3D3V/5V/1D8V/0D9V)**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet: 43 of 47

$I_{ocp} = 7.8 * 1.7 = 13.3A$
 $R_{ds,on} = 5.5 * 1.375 = 7.563m\ ohm$
 $V_{cs1} = I_{ocp} * R_{ds,on} = 100mV$
 $V_{ILIM} = V_{cs1} / 0.1 = 1V$

$I_{ocp} = 4.3 * 1.7 = 7.3A$
 $R_{ds,on} = 20 * 1.375 = 27.5m\ ohm$
 $V_{cs2} = I_{ocp} * R_{ds,on} = 201mV$
 $V_{ILIM2} = V_{cs2} / 0.1 = 2.01V$



Ton Setting

	Side 1	Side 2
Frequency (kHz)	235	170
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

<Core Design>

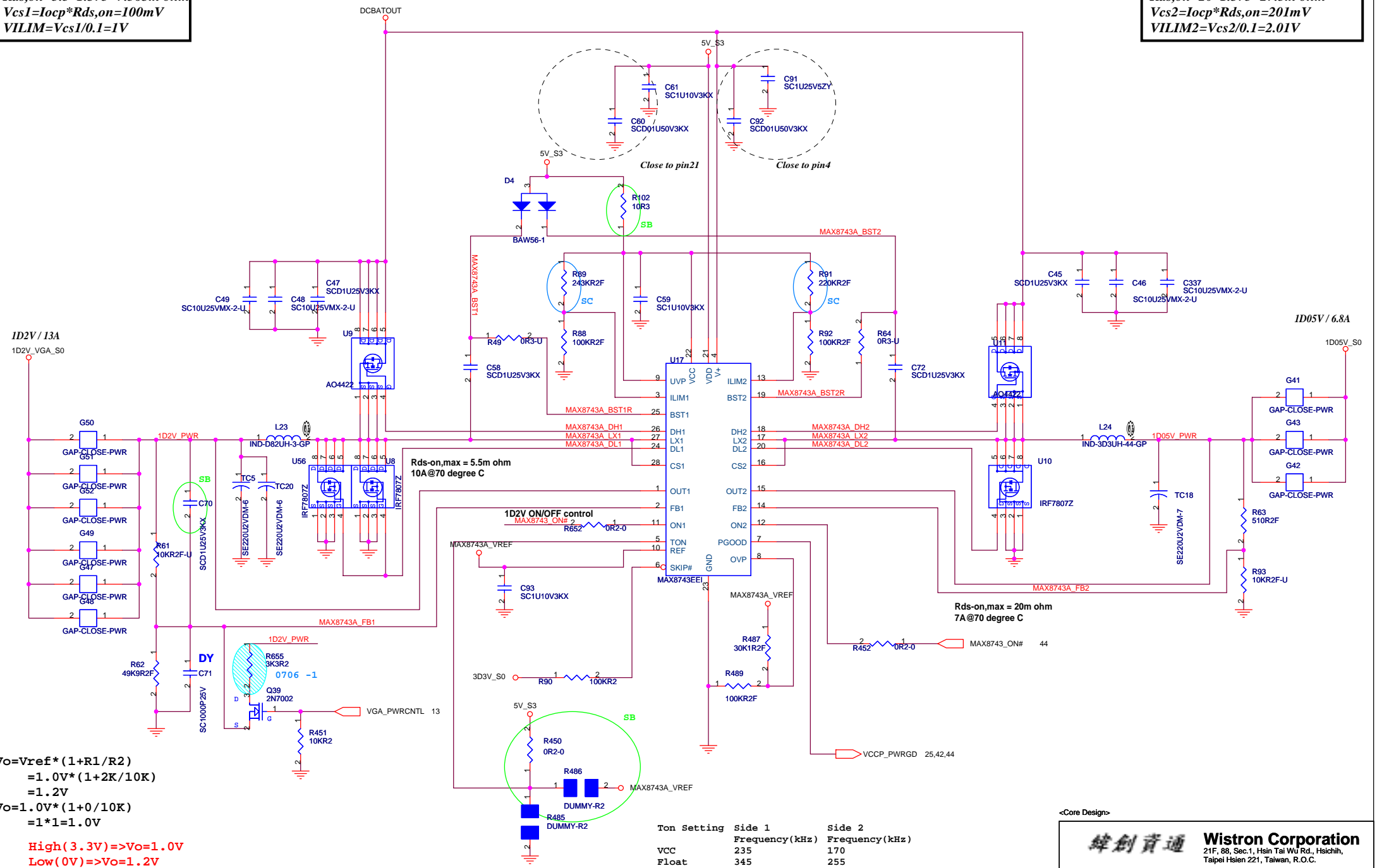
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

MAX8743 (1D8V_S0/1D5V_S0)

File	Document Number	Rev
Size A3	Leopard2	-1
Date: Monday, July 11, 2005	Sheet 44 of 47	

$I_{ocp} = 7.8 * 1.7 = 13.3A$
 $R_{ds,on} = 5.5 * 1.375 = 7.563m\ ohm$
 $V_{cs1} = I_{ocp} * R_{ds,on} = 100mV$
 $V_{ILIM} = V_{cs1} / 0.1 = 1V$

$I_{ocp} = 4.3 * 1.7 = 7.3A$
 $R_{ds,on} = 20 * 1.375 = 27.5m\ ohm$
 $V_{cs2} = I_{ocp} * R_{ds,on} = 201mV$
 $V_{ILIM2} = V_{cs2} / 0.1 = 2.01V$



$V_o = V_{ref} * (1 + R1/R2)$
 $= 1.0V * (1 + 2K/10K)$
 $= 1.2V$
 $V_o = 1.0V * (1 + 0/10K)$
 $= 1 * 1 = 1.0V$

High (3.3V) => $V_o = 1.0V$
Low (0V) => $V_o = 1.2V$

M24/M26 POWER PLAY (VGA_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)

Ton Setting	Side 1 Frequency (kHz)	Side 2 Frequency (kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

<Core Design>

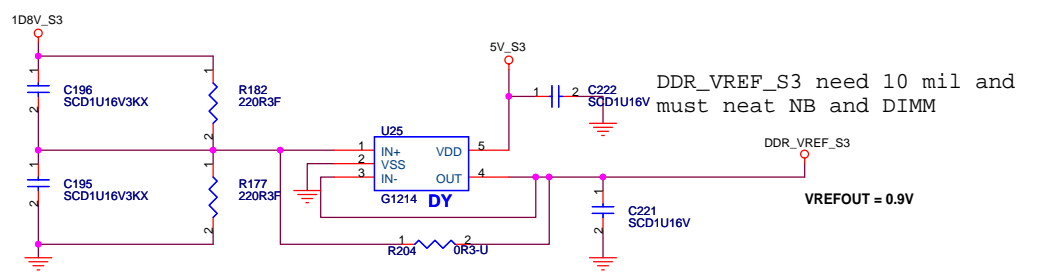
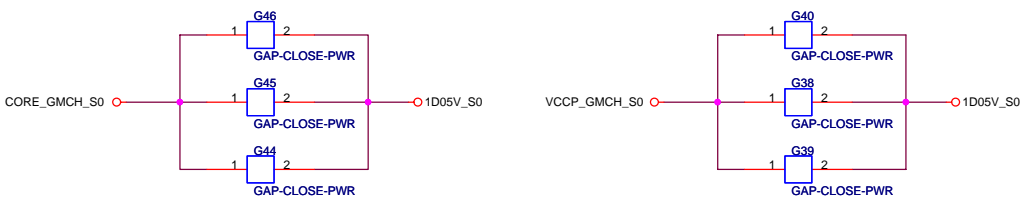
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File: **MAX8743 (1D2V_VGA_S0/1D05V)**

Size A3	Document Number	Rev
	Leopard2	-1

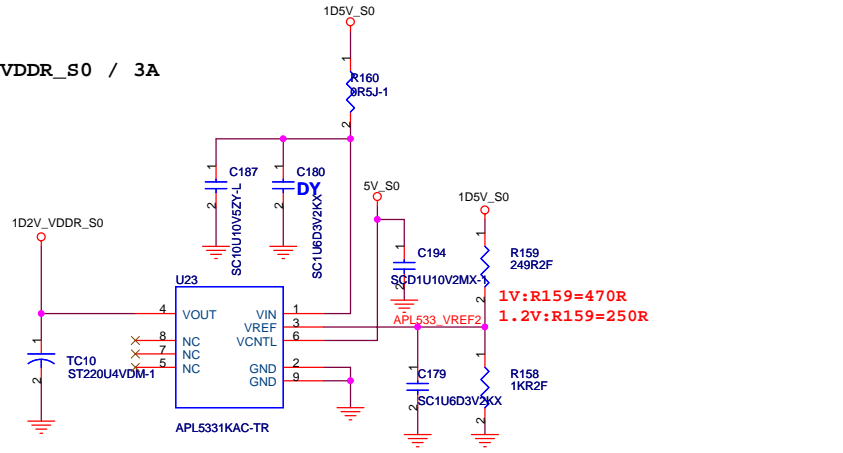
Date: Thursday, July 07, 2005 Sheet 45 of 47

FOR GMCH Power

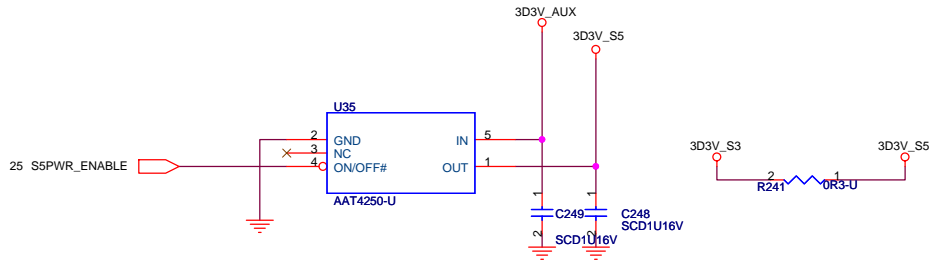


FOR DDR2 Power

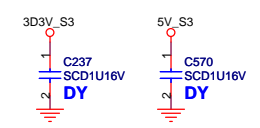
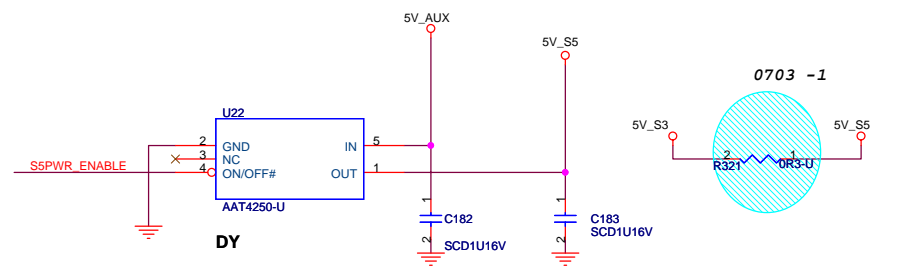
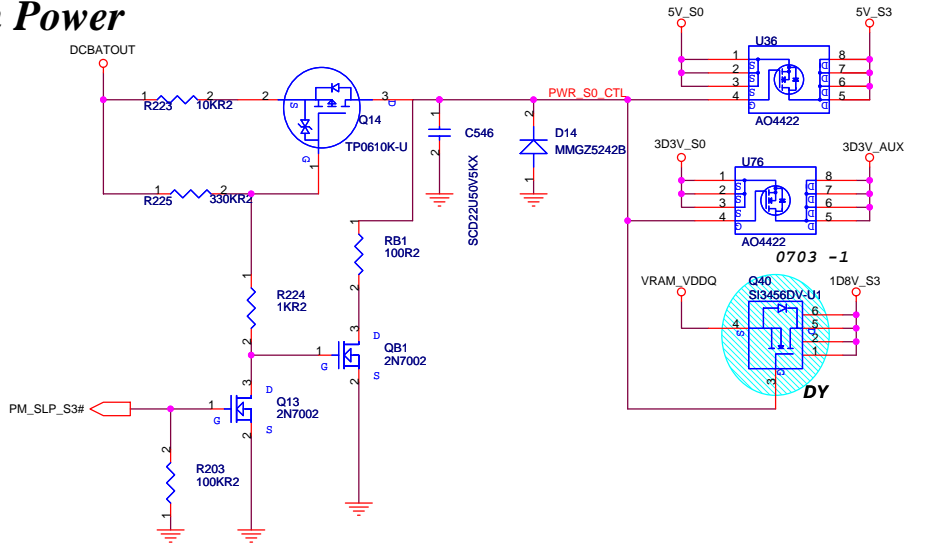
1D2V_VDDR_S0 / 3A



Suspend Power



Run Power



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

Size A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet 46 of 47

www.s-manuals.com