

LLW-1/LGG-1 Schematics

Sandy Bridge

Cougar Point

2010-11-08

REV : SB

DY:None Installed

UMA:UMA platform installed only

PX:Discrete(both Robson and Whistler) SKU installed

RBS:Robson SKU installed only

WTL:Whistler SKU installed only

SAMSUNG:Use SAMSUNG VRAM

Hynix:Use Hynix VRAM

VRAM_1G:Use 1G VRAM

VRAM_2G:Use 2G VRAM

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size

Document Number

Rev

A3

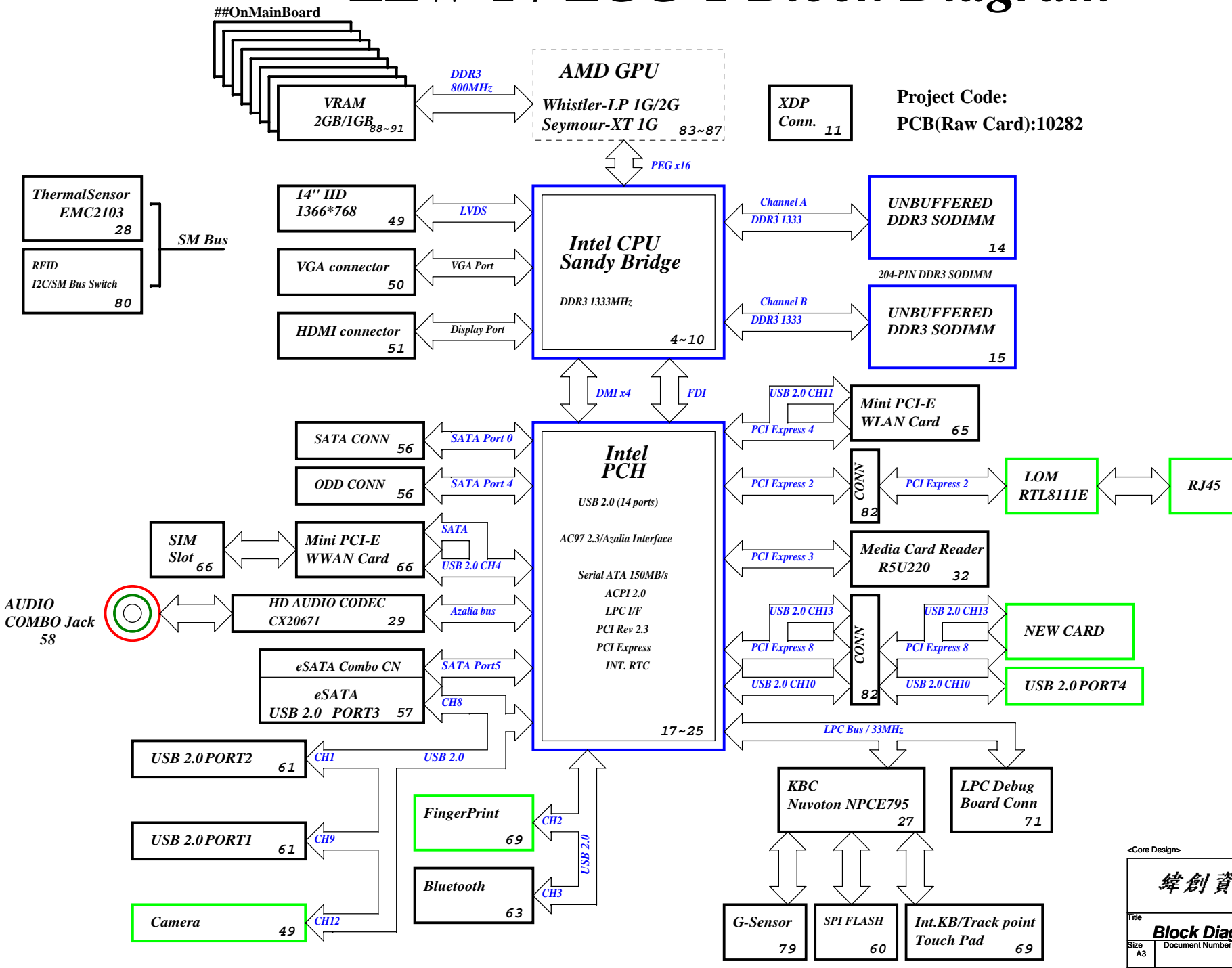
LLW-1 / LGG-1

SB

Date: Tuesday, November 09, 2010

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LLW-1 / LGG-1 Block Diagram



Project Code:
PCB(Raw Card):10282

PCB Layer Stackup	
L1: TOP	L5: VCC
L2: GND	L6: Signal
L3: Signal	L7: GND
L4: Signal	L8: BOTTOM
Battery Charger/Selector	
BQ24745	40
INPUTS	OUTPUTS
DCBATOUT	BT+
System DC/DC	
BD95280	41
PWR_3D3V_DCBATOUT	3D3V_S5
PWR_5V_DCBATOUT	5V_S5
CPU DC/DC	
NCP6131	42~44
DCBATOUT	VCC_CORE
DCBATOUT_VCC_GFXCORE	VCC_GFXCORE
ID05V_VTT	
TPS51218	45
PWR_ID05V_DCBATOUT	ID05V_VTT
ID5V_S3	
TPS51218	46
PWR_ID5V_DCBATOUT	ID5V_S3
0D75V	
RT9026	46
ID5V_S3	DDR_VREF_S3
	0D75V_S0
ID8V_S0	
RT8015	47
3D3V_S5	ID8V_S0
VCCSA	
RT8208B	48
PWR_VCCSA_DCBATOUT	0D85V_S0
GFX CORE	
RT8208B	92
PWR_DCBATOUT_VGA_CORE	VGA_CORE
IV_VGA	
RT9025	93
ID5V_S3	IV_VGA_S0
ID8V_VGA	
RT9025	93
3D3V_S5	ID8V_VGA_S0

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File: **Block Diagram**

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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Leave floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SATA Table

SATA	
Pair	Device
0	HDD
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

PCIE Routing

LANE1	RESERVED
LANE2	LAN
LANE3	CARD READER
LANE4	MiniCard WLAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	RESERVED
LANE8	NEW CARD

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0: connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.75V 0.25V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1				
Battery Capacity Board				KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2				
PCH				KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
MMX				KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
LCD				KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
Thermal Sensor				
PCH SMBus				
CKS05 Clock Generator				PCH_SMBDATA/PCH_SMBCLK
SO-DIMMA (SPD)				PCH_SMBDATA/PCH_SMBCLK
SO-DIMMB (SPD)				PCH_SMBDATA/PCH_SMBCLK
Digital Pot				PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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SSID = CPU

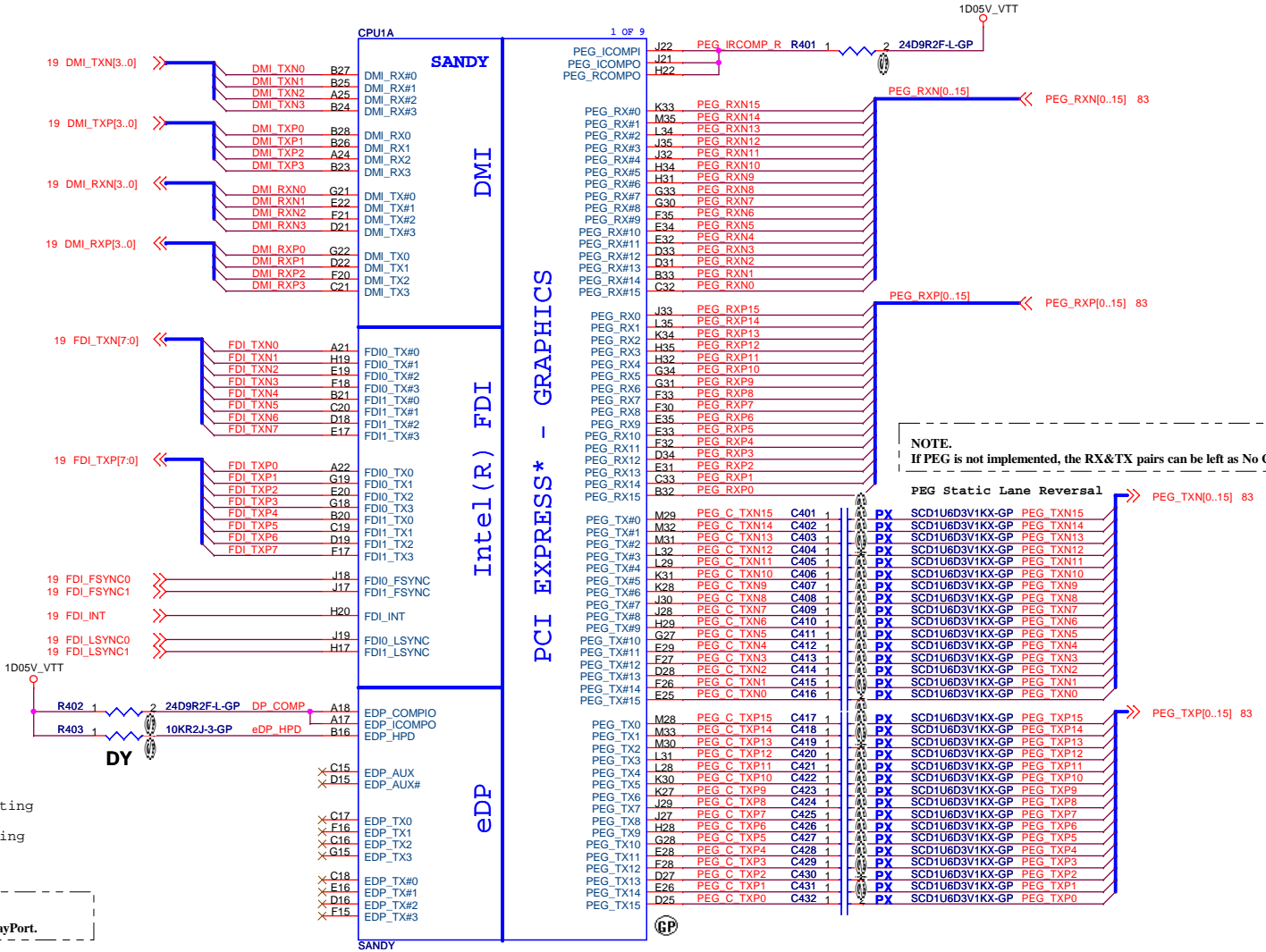
Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.



Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOPMO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

Table 4.1- Central Processing Unit slot multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
FOXCONN	PZ98827-364B-41F	N/A	62.10055.421
TYCO	2-2013620-3	N/A	62.10040.771

<Core Design>

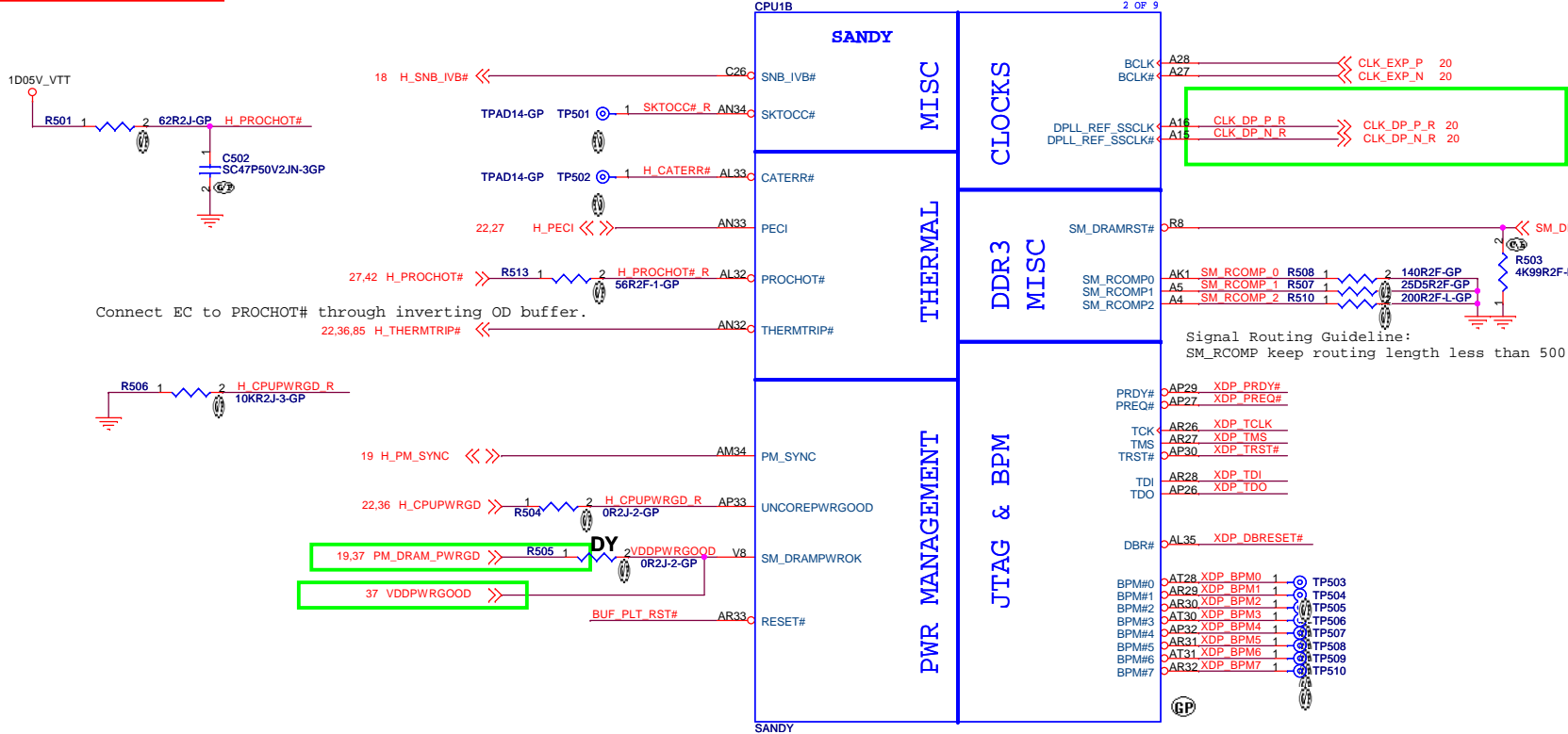
緯創資通 Wistron Corporation
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Title: **CPU (PCIe/DMI/FDI)**

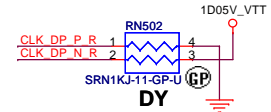
Size: A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

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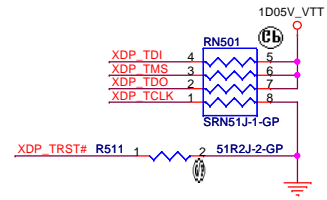
SSID = CPU



Disabling Guidelines:
 If motherboard only supports external graphics:
 Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
 Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor power (~15 mW) may be wasted.



Signal Routing Guideline:
 SM_RCOMP keep routing length less than 500 mils.



- XDP DBRESET# >>> XDP_DBRESET# 11,19
- XDP_PREQ# >>> XDP_PREQ# 11
- XDP_PRDY# >>> XDP_PRDY# 11
- XDP_TDO >>> TP511
- XDP_TDI >>> TP512
- XDP_TRST# >>> TP513
- XDP_TCLK >>> TP514
- XDP_TMS >>> TP515

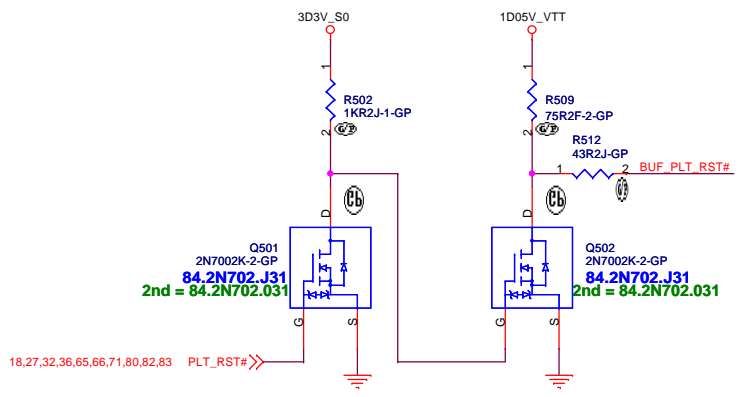
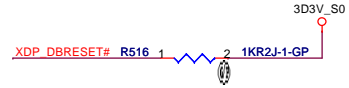


Table 5.1- N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002K	N/A	84.2N702.J31
DIODES	2N7002K	N/A	84.2N702.031
NXP	2N7002BK	N/A	84.07002.I31

<Core Design>

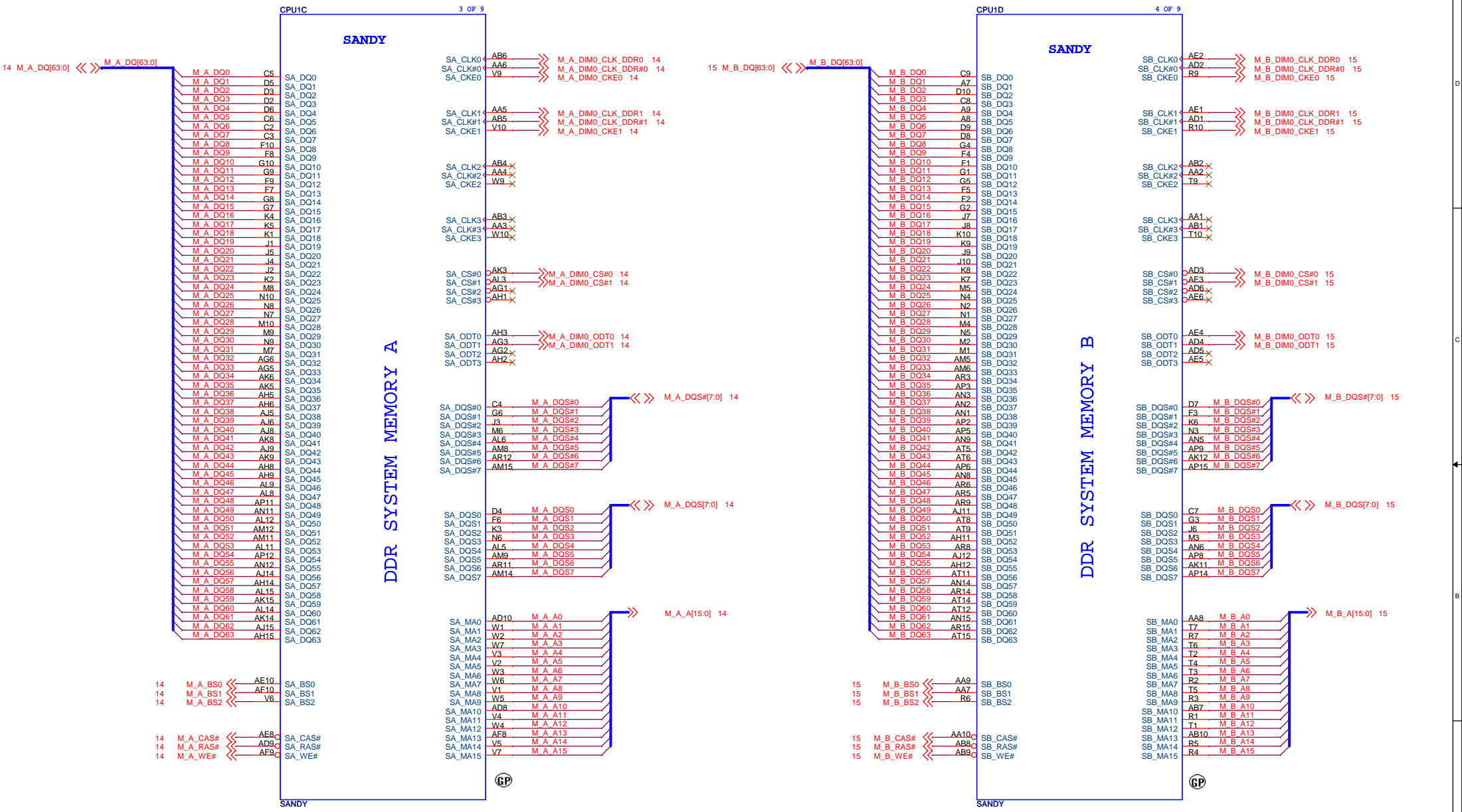
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (Thermal/CLK/PM)**

Size: A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

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SSID = CPU



<Core Design>

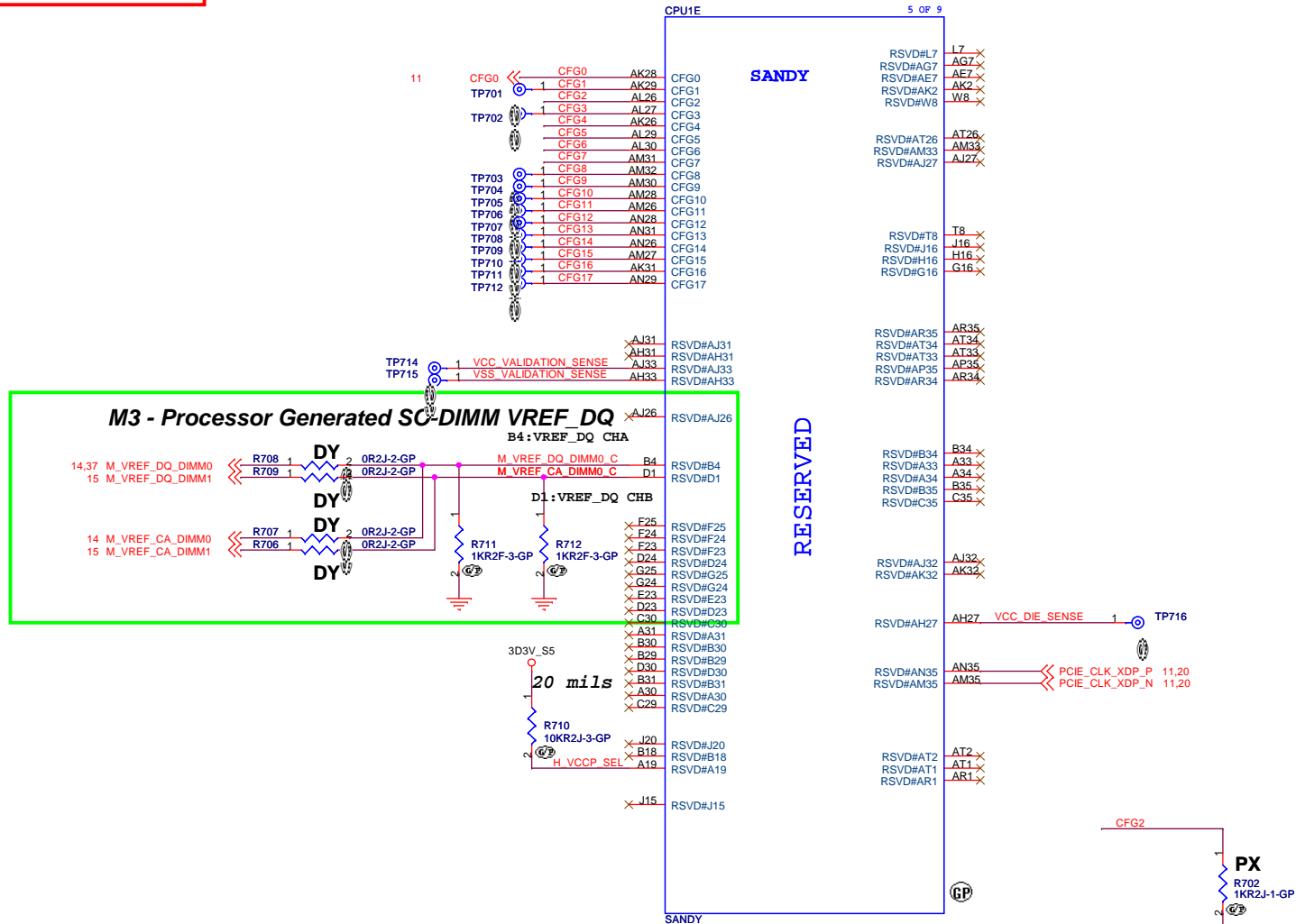
緯創資通 Wistron Corporation
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Title: **CPU (DDR)**

Size: A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

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SSID = CPU



PEG Static Lane Reversal

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
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Display Port Presence Strap

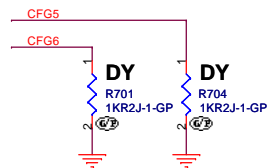
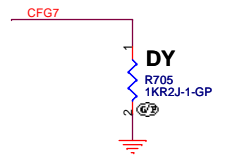
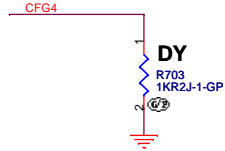
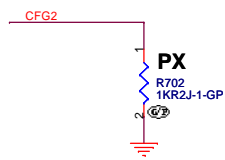
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
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PEG DEFER TRAINING

CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
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PCIe Port Bifurcation Straps

CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled
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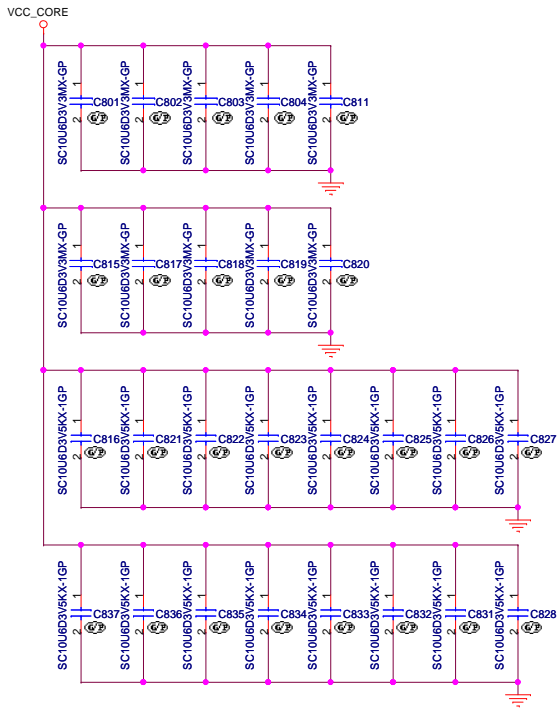
Title: **CPU (RESERVED)**

Size A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

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PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:
 4 x 470 uF at Bottom Socket Edge
 8 x 22 uF at Top Socket Cavity
 8 x 22 uF at Top Socket Edge
 8 x 22 uF at Bottom Socket Cavity

VCC_CORE

SANDY

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- P37 VCC
- P36 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

CORE SUPPLY

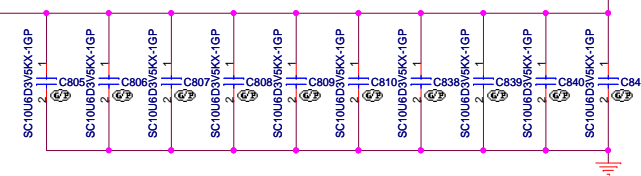
SENSE LINES

PEG AND DDR

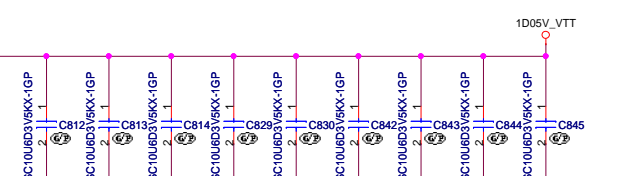
SVID

- VCCIO AH13
- VCCIO AH10
- VCCIO AG10
- VCCIO Y10
- VCCIO U10
- VCCIO P10
- VCCIO J14
- VCCIO J13
- VCCIO J12
- VCCIO J11
- VCCIO H14
- VCCIO H12
- VCCIO H11
- VCCIO G14
- VCCIO G12
- VCCIO F14
- VCCIO F13
- VCCIO F12
- VCCIO E14
- VCCIO E12
- VCCIO E11
- VCCIO D14
- VCCIO D13
- VCCIO D12
- VCCIO D11
- VCCIO C14
- VCCIO C13
- VCCIO C12
- VCCIO C11
- VCCIO B14
- VCCIO B12
- VCCIO A14
- VCCIO A13
- VCCIO A12
- VCCIO A11
- VCCIO J23

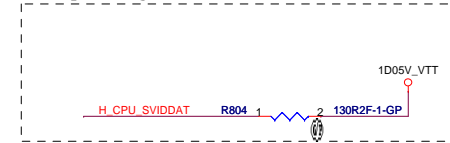
VCCIO Output Decoupling Recommendation:
 2 x 330 uF (3 x 330 uF for 2012 capable designs)
 5 x 22 uF & 5 x 0805 no-stuff at Bottom
 7 x 22 uF & 2 x 0805 no-stuff at Top



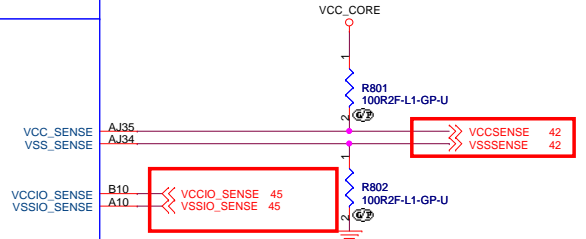
No-stuff sites outside the socket may be removed.
 No-stuff sites inside the socket cavity need to remain.



For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMPV7
 For CRB VIDALERT# need to pull high 75 ohm close to CPU



R801, R802 need to close to CPU



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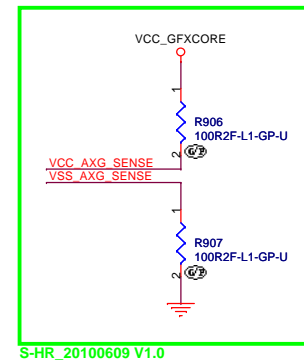
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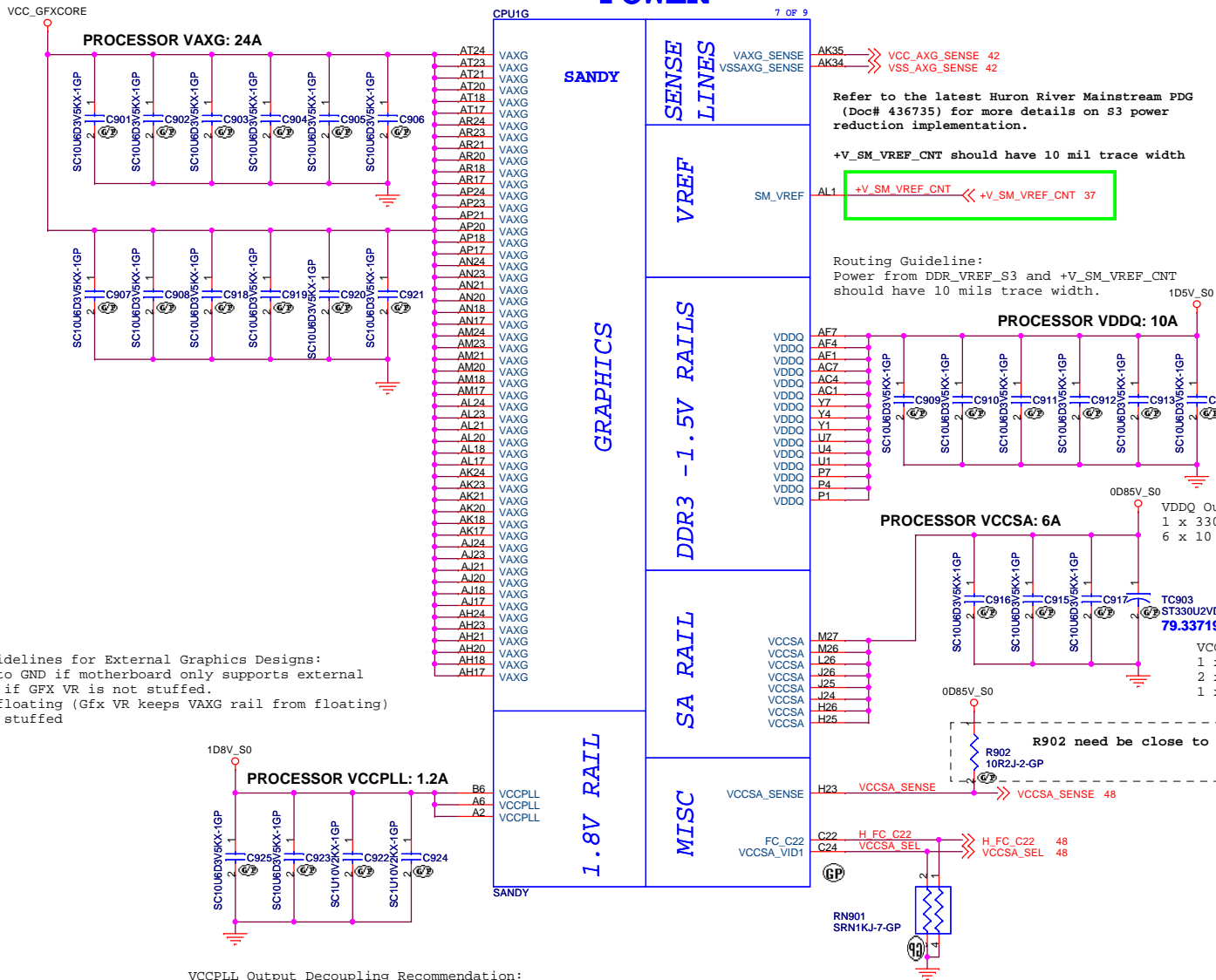
SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU



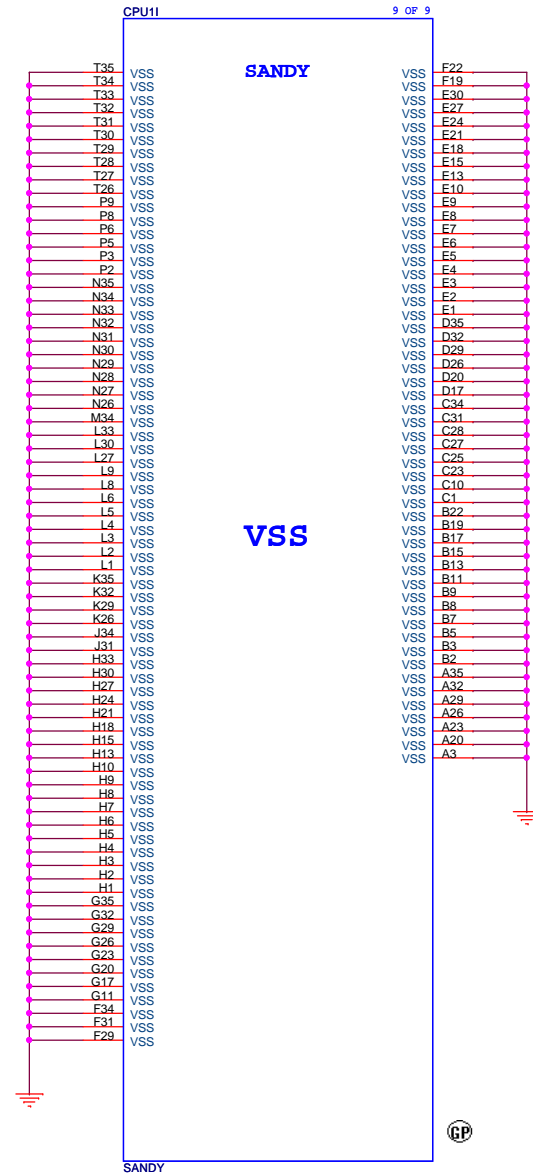
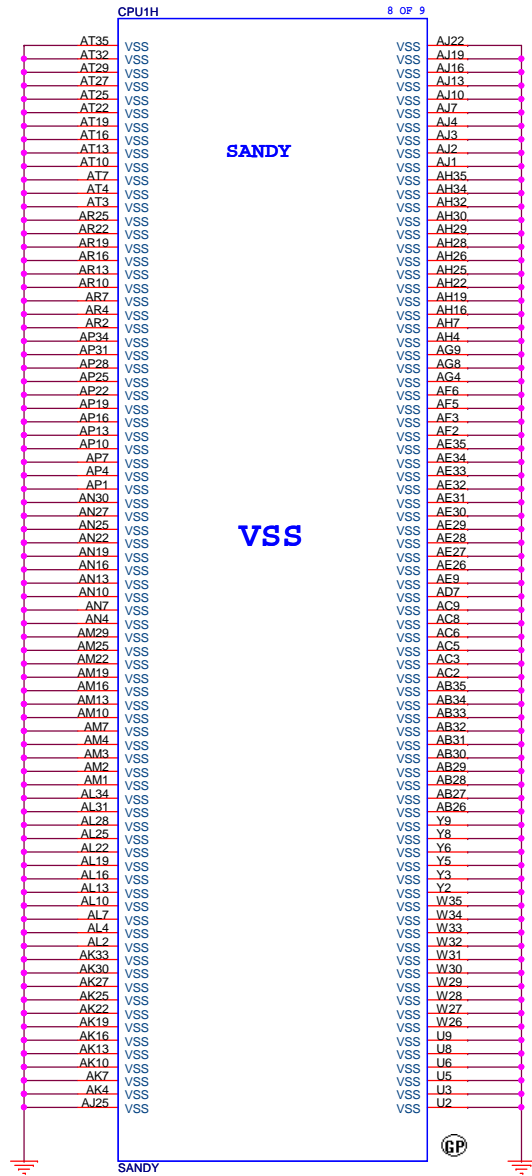
S-HR_20100609 V1.0



Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

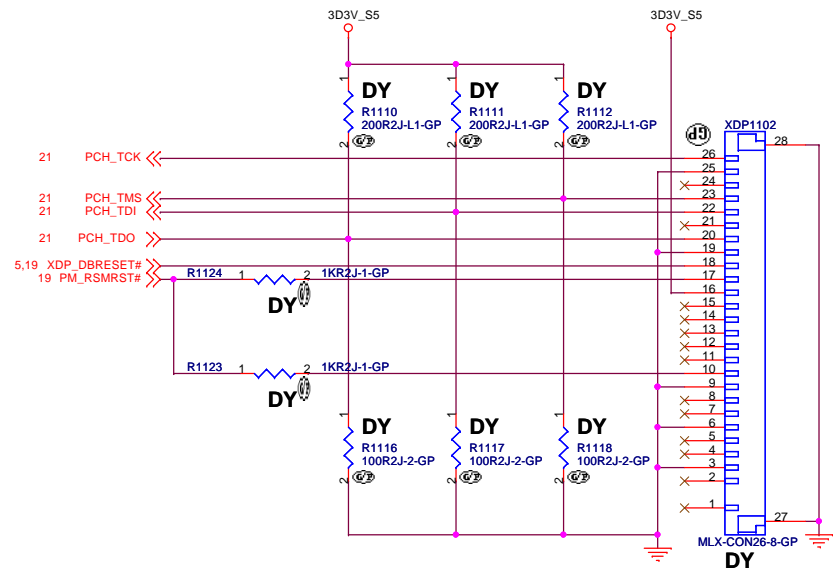
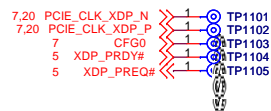
<Core Design>

SSID = CPU



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DEBUG Interface for Processor.

- CPU XDP SFF 26pin IF
- Pin 1 OBSFN_A0 (PREQ#, I/O)
 - Pin 2 OBSFN_A1 (PRDY#, I/O)
 - Pin 3 GND
 - Pin 4 OBSDATA_A0 (Open, I/O)
 - Pin 5 OBSDATA_A1 (Open, I/O)
 - Pin 6 GND
 - Pin 7 OBSDATA_A2 (Open, I/O)
 - Pin 8 OBSDATA_A3 (Open, I/O)
 - Pin 9 GND
 - Pin 10 HOOK0 (PWRGD, In)
 - Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
 - Pin 12 HOOK2 (CFG0, Out)
 - Pin 13 HOOK3 (vr_READYSYS_PWROK, Out)
 - Pin 14 HOOK4 (BCLK#, In)
 - Pin 15 HOOK5 (BCLK#, In)
 - Pin 16 VCCOBS_AB (VCCP Voltage of CPU, In)
 - Pin 17 HOOK6 (RESET#, Out)
 - Pin 18 HOOK7 (DBR#, Out)
 - Pin 19 GND
 - Pin 20 TDO, In
 - Pin 21 TRST#, Out
 - Pin 22 TDI, Out
 - Pin 23 TMS, Out
 - Pin 24 TCK1 (Open)
 - Pin 25 GND
 - Pin 26 TCK0, Out

TABLE

PCH PIN	REF DES	PCH ES1 JTAG		PCH ES2 JTAG		PRODUCTION	
		Enable	Disable	Enable	Disable	Enable	Disable
TDO	R1110	DY	DY	200 Ohms	DY	DY	DY
	R1116	DY	DY	100 Ohms	DY	DY	DY
	R2	DY	DY	DY	DY	51 Ohms	DY
TMS	R1112	200 Ohms	DY	200 Ohms	DY	DY	DY
	R1118	100 Ohms	DY	100 Ohms	DY	DY	DY
	R91	DY	DY	DY	DY	51 Ohms	DY
TDI	R1111	200 Ohms	20K Ohms	200 Ohms	DY	DY	DY
	R1117	100 Ohms	10K Ohms	100 Ohms	DY	DY	DY
	R90	DY	DY	DY	DY	51 Ohms	DY
TCK	R541	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms
TRST#	R953	20K Ohms	DY	DY	DY	DY	DY
	R535	10K Ohms	DY	DY	DY	DY	DY
	R103	DY	DY	DY	DY	DY	DY

DEBUG Interface for PCH.

- PCH XDP SFF 26pin IF
- Pin 1 OBSFN_A0 (Open, I/O)
 - Pin 2 OBSFN_A1 (Open, I/O)
 - Pin 3 GND
 - Pin 4 OBSDATA_A0 (Open, I/O)
 - Pin 5 OBSDATA_A1 (Open, I/O)
 - Pin 6 GND
 - Pin 7 OBSDATA_A2 (Open, I/O)
 - Pin 8 OBSDATA_A3 (Open, I/O)
 - Pin 9 GND
 - Pin 10 HOOK0 (RSMRST#, In)
 - Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
 - Pin 12 HOOK2 (Open)
 - Pin 13 HOOK3 (Open)
 - Pin 14 HOOK4 (Open)
 - Pin 15 HOOK5 (Open)
 - Pin 16 VCCOBS_AB (3.3VSUS, In)
 - Pin 17 HOOK6 (RSMRST#, Out)
 - Pin 18 HOOK7 (DBR#, Out)
 - Pin 19 GND
 - Pin 20 TDO (JTAG, In)
 - Pin 21 TRST# (Open)
 - Pin 22 TDI (JTAG, Out)
 - Pin 23 TMS (JTAG, Out)
 - Pin 24 TCK1 (Open)
 - Pin 25 GND
 - Pin 26 TCK0 (JTAG, Out)

↑
LOGIC

<Core Design>

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Title			
XDP CONN			
Size	Document Number		Rev
A3	LLW-1 / LGG-1		SB
Date:	Tuesday, November 09, 2010		Sheet 11 of 94

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A4

Document Number

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Title

CLOCK GEN

Size
A4

Document Number

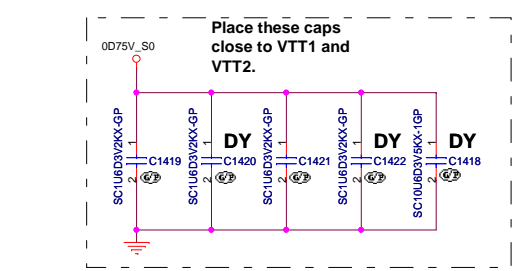
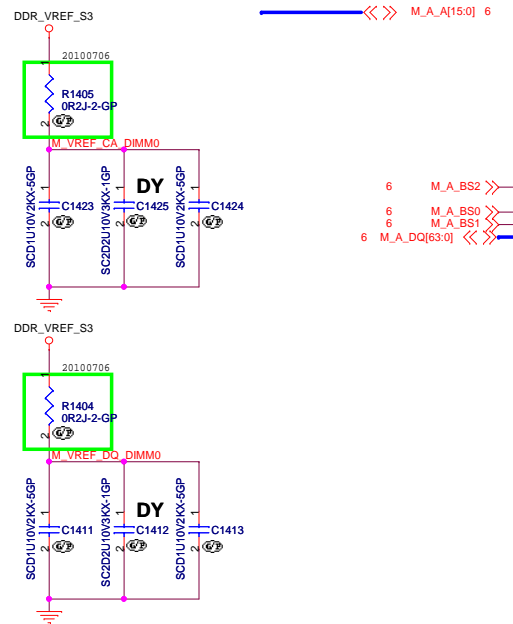
LLW-1 / LGG-1

Rev
SB

Date: Tuesday, November 09, 2010

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SSID = MEMORY

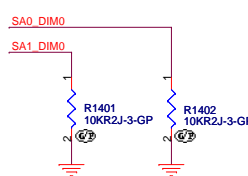
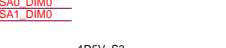
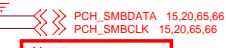
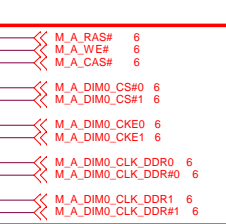


6 M_A_DQS#[7:0] 6
6 M_A_DQS#[7:0] 6

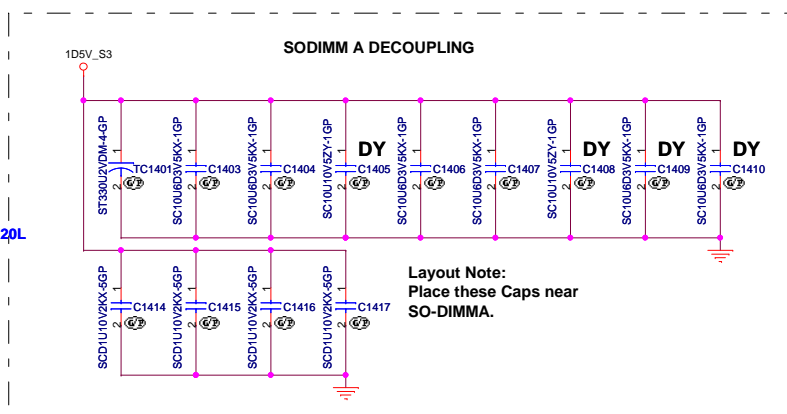
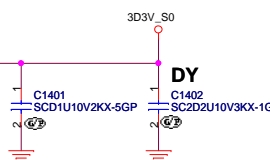
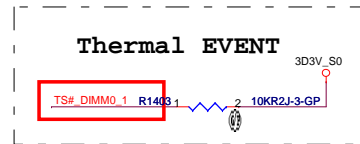
6 M_A_DIM0_ODT0
6 M_A_DIM0_ODT1
7 M_VREF_CA_DIMM0
7.37 M_VREF_DO_DIMM0
15.37 DDR3_DRAMRST#

M_A A0	98	A0	NP1
M_A A1	97	A1	NP2
M_A A2	96	A2	RAS#
M_A A3	95	A3	WE#
M_A A4	92	A4	CAS#
M_A A5	91	A5	CS0#
M_A A6	90	A6	CS1#
M_A A7	89	A7	CKE0
M_A A8	86	A8	CKE1
M_A A9	85	A9	A10/AP
M_A A10	107	A10	A12
M_A A11	84	A11	A14
M_A A12	83	A12	A14
M_A A13	113	A13	A14
M_A A14	80	A14	CK0
M_A A15	78	A15	CK0#
M_A A15	79	A15	CK1
M_A A15	79	A15	CK1#
M_A BA0	109	BA0	DM0
M_A BA1	108	BA1	DM1
M_A DQ0	5	DQ0	DM2
M_A DQ1	7	DQ1	DM3
M_A DQ2	15	DQ2	DM4
M_A DQ3	17	DQ3	DM5
M_A DQ4	4	DQ4	DM6
M_A DQ5	16	DQ5	DM7
M_A DQ6	18	DQ6	DO7
M_A DQ7	21	DQ7	DO8
M_A DQ8	23	DQ8	DO9
M_A DQ9	23	DQ9	DO10
M_A DQ10	23	DQ10	DO11
M_A DQ11	38	DQ11	DO12
M_A DQ12	22	DQ12	DO13
M_A DQ13	24	DQ13	DO14
M_A DQ14	34	DQ14	DO15
M_A DQ15	36	DQ15	DO16
M_A DQ16	39	DQ16	DO17
M_A DQ17	41	DQ17	DO18
M_A DQ18	51	DQ18	DO19
M_A DQ19	53	DQ19	DO20
M_A DQ20	40	DQ20	DO21
M_A DQ21	42	DQ21	DO22
M_A DQ22	50	DQ22	DO23
M_A DQ23	52	DQ23	DO24
M_A DQ24	57	DQ24	DO25
M_A DQ25	59	DQ25	DO26
M_A DQ26	67	DQ26	DO27
M_A DQ27	69	DQ27	DO28
M_A DQ28	56	DQ28	DO29
M_A DQ29	58	DQ29	DO30
M_A DQ30	68	DQ30	DO31
M_A DQ31	70	DQ31	DO32
M_A DQ32	129	DQ32	DO33
M_A DQ33	131	DQ33	DO34
M_A DQ34	141	DQ34	DO35
M_A DQ35	143	DQ35	DO36
M_A DQ36	130	DQ36	DO37
M_A DQ37	132	DQ37	DO38
M_A DQ38	140	DQ38	DO39
M_A DQ39	142	DQ39	DO40
M_A DQ40	147	DQ40	DO41
M_A DQ41	149	DQ41	DO42
M_A DQ42	157	DQ42	DO43
M_A DQ43	159	DQ43	DO44
M_A DQ44	146	DQ44	DO45
M_A DQ45	148	DQ45	DO46
M_A DQ46	158	DQ46	DO47
M_A DQ47	160	DQ47	DO48
M_A DQ48	163	DQ48	DO49
M_A DQ49	165	DQ49	DO50
M_A DQ50	175	DQ50	DO51
M_A DQ51	177	DQ51	DO52
M_A DQ52	168	DQ52	DO53
M_A DQ53	166	DQ53	DO54
M_A DQ54	174	DQ54	DO55
M_A DQ55	176	DQ55	DO56
M_A DQ56	181	DQ56	DO57
M_A DQ57	183	DQ57	DO58
M_A DQ58	191	DQ58	DO59
M_A DQ59	193	DQ59	DO60
M_A DQ60	180	DQ60	DO61
M_A DQ61	192	DQ61	DO62
M_A DQ62	182	DQ62	DO63
M_A DQ63	194	DQ63	DQS0#
M_A DQS#0	10	DQS0#	DQS1#
M_A DQS#1	22	DQS1#	DQS2#
M_A DQS#2	45	DQS2#	DQS3#
M_A DQS#3	62	DQS3#	DQS4#
M_A DQS#4	135	DQS4#	DQS5#
M_A DQS#5	152	DQS5#	DQS6#
M_A DQS#6	168	DQS6#	DQS7#
M_A DQS#7	186	DQS7#	DQS0
M_A DQS0	12	DQS0	DQS1
M_A DQS1	29	DQS1	DQS2
M_A DQS2	47	DQS2	DQS3
M_A DQS3	64	DQS3	DQS4
M_A DQS4	137	DQS4	DQS5
M_A DQS5	154	DQS5	DQS6
M_A DQS6	171	DQS6	DQS7
M_A DQS7	188	DQS7	ODT0
M_A DQS7	188	DQS7	ODT1
M_A DQS7	188	DQS7	VREF_CA
M_A DQS7	188	DQS7	VREF_DO
M_A DQS7	188	DQS7	RESET#
M_A DQS7	188	DQS7	VTT1
M_A DQS7	188	DQS7	VTT2
M_A DQS7	188	DQS7	DDR3-204P-82-GP
M_A DQS7	188	DQS7	62.10017.U01

H = 9.2mm
Part = 62.10017.T11
Part = 62.10017.T61
DDR3-204P-82-GP
62.10017.U01



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Layout Note:
Place these Caps near
SO-DIMMA.

<Core Design>

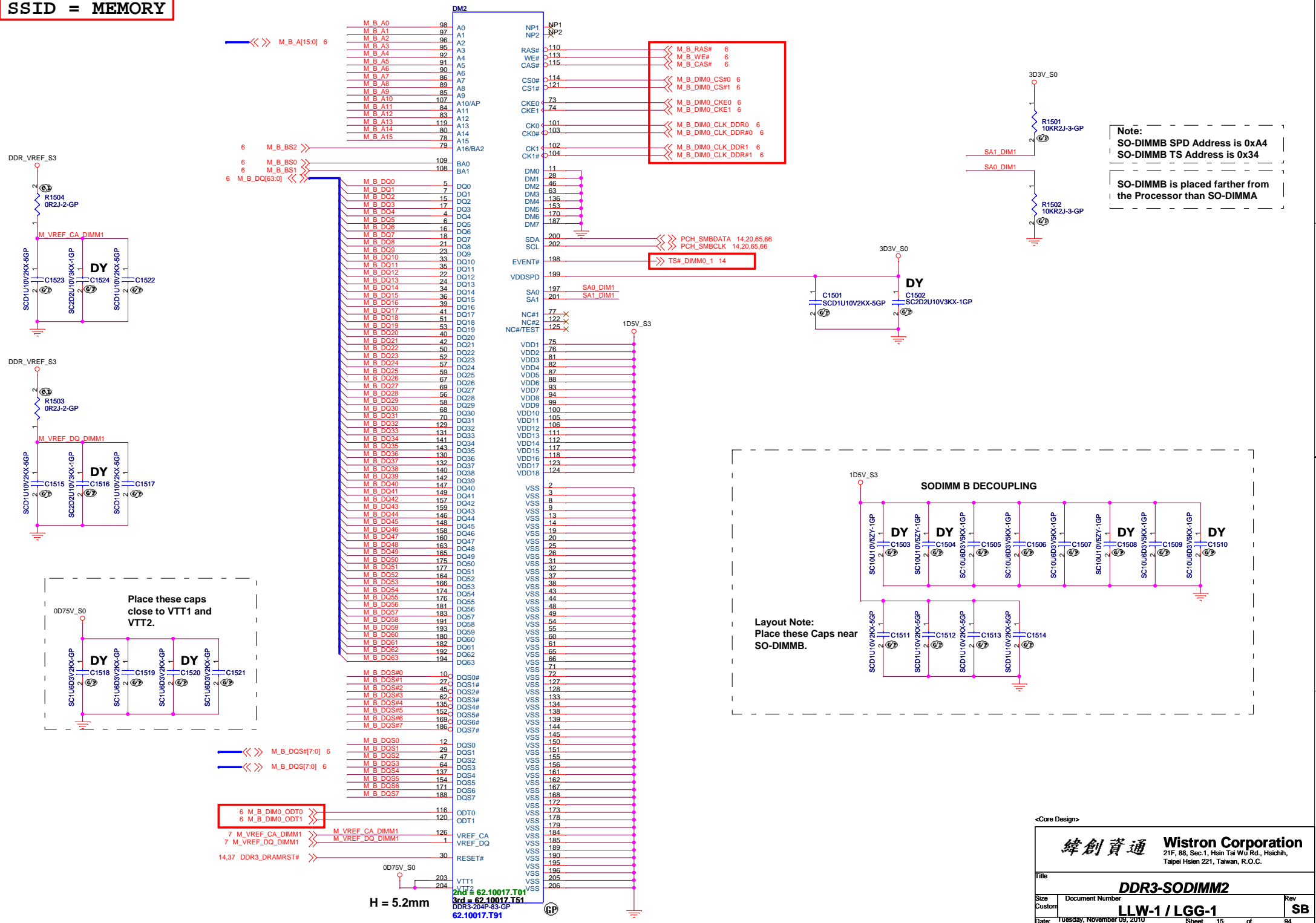
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Title: **DDR3-SODIMM1**

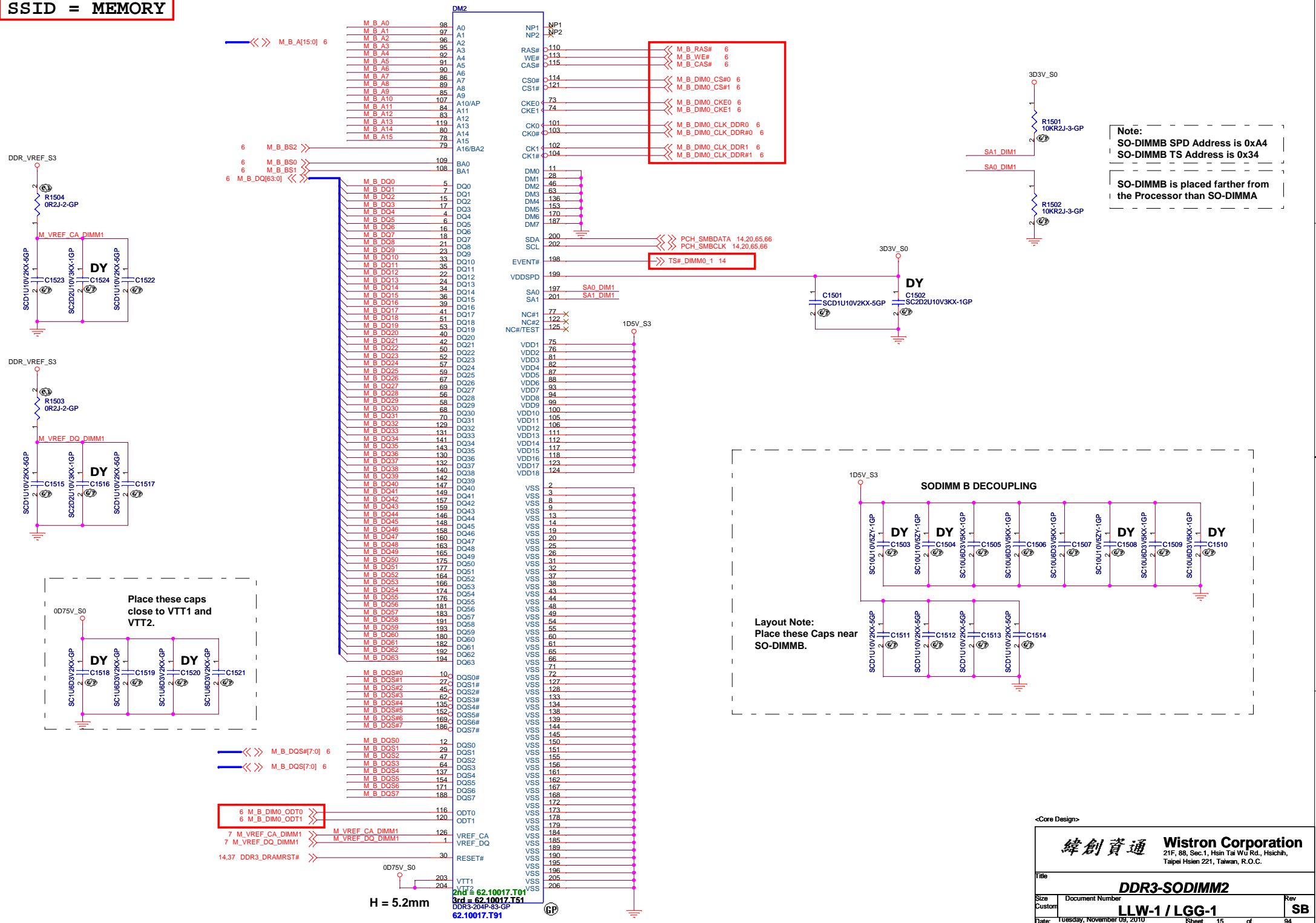
Size: Custom Document Number: **LLW-1 / LGG-1** Rev: **SB**

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SSID = MEMORY



SSID = MEMORY



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Title

DDR3-SODIMM2

Size
A4

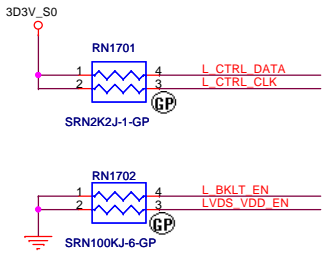
Document Number

LLW-1 / LGG-1

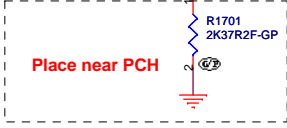
Rev
SB

Date: Tuesday, November 09, 2010

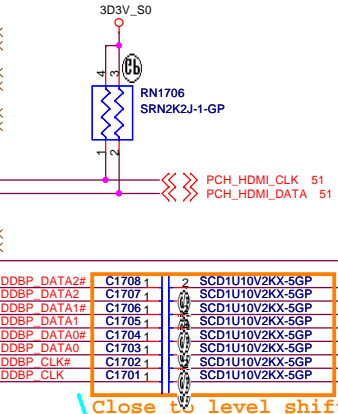
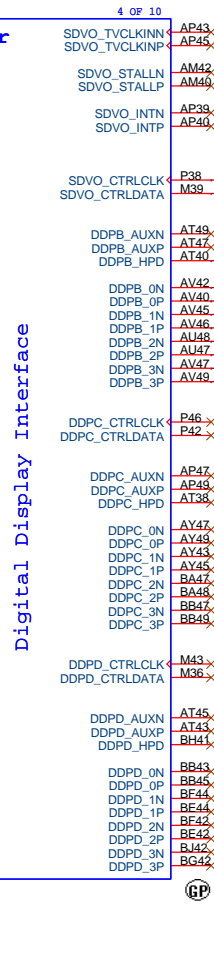
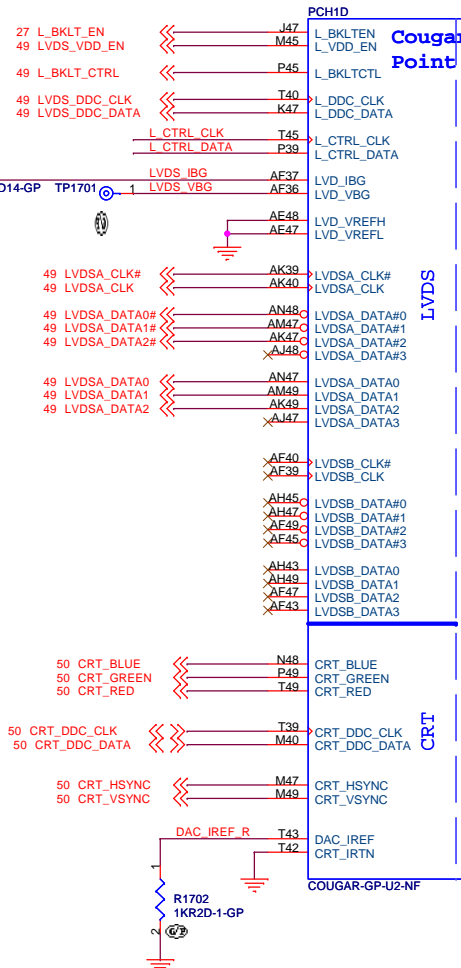
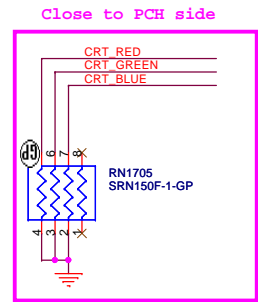
Sheet 16 of 94



L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display



Impedance:90 ohm



DDI Port B Detect:(SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected

Close to level shifter side

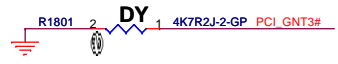
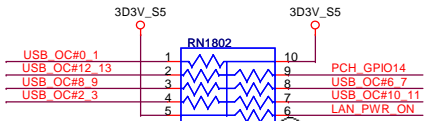
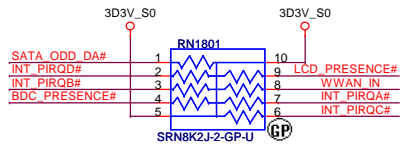
Impedance:90 ohm

Impedance:100 ohm

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

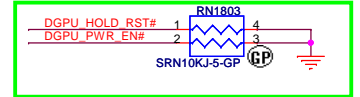
PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI_CTRLCLK	
SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI_CTRLDATA	

SSID = PCH



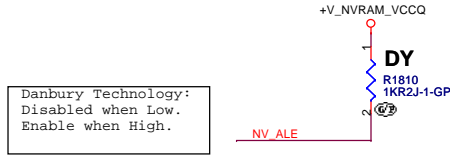
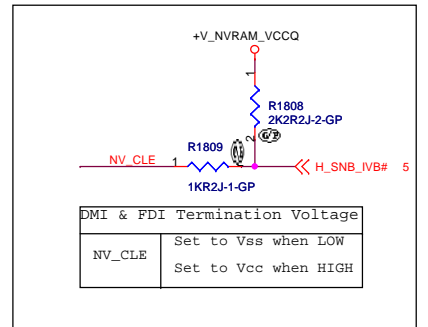
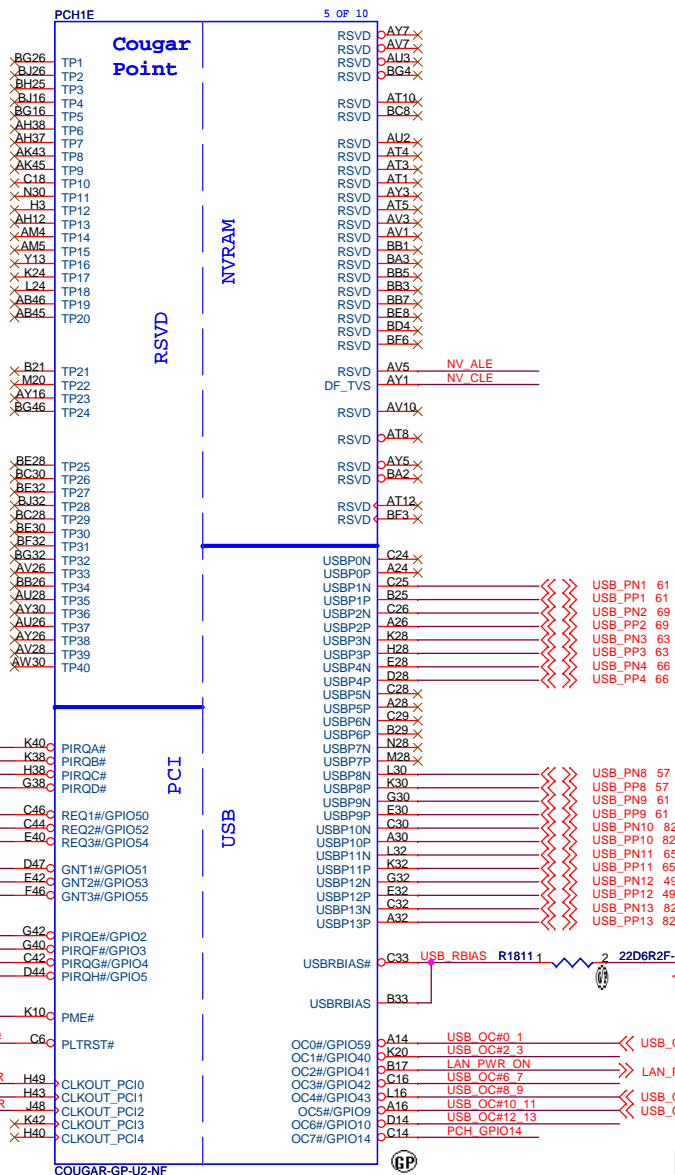
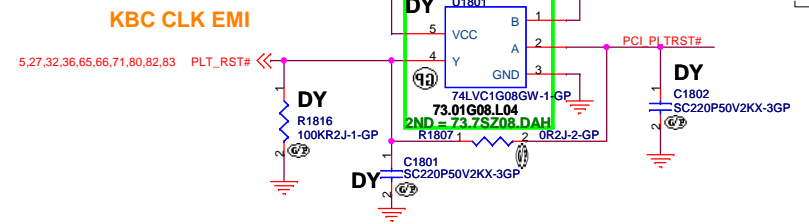
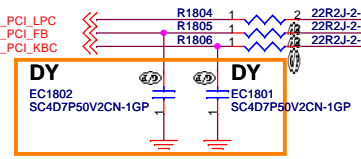
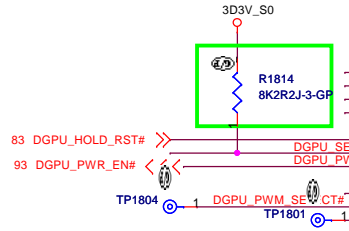
Al6 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default
-----------	---

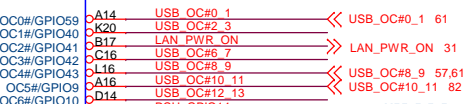


BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



USB	
Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card



USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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File: **PCH (PCI/USB/NVRAM)**

Size A3	Document Number	Rev
	LLW-1 / LGG-1	SB

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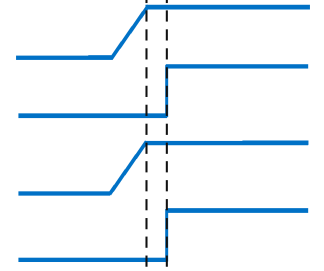
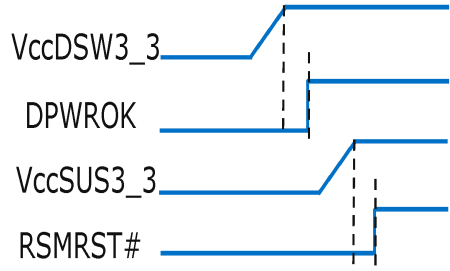
SSID = PCH



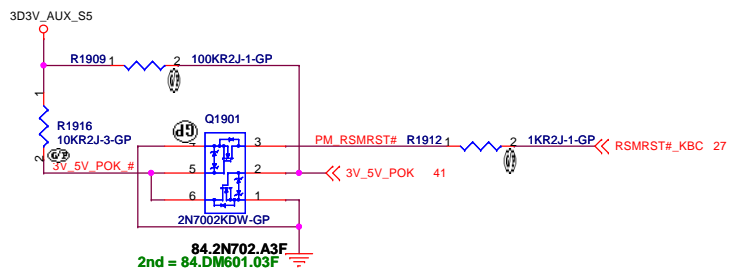
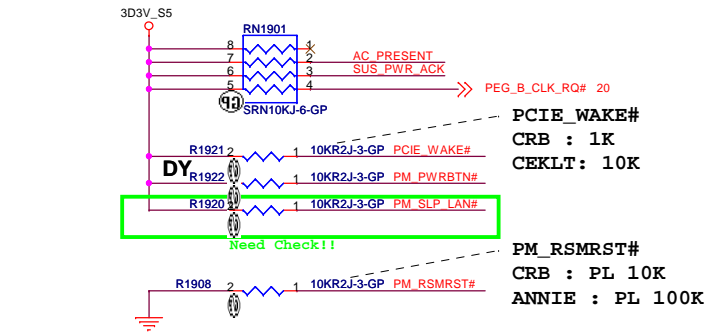
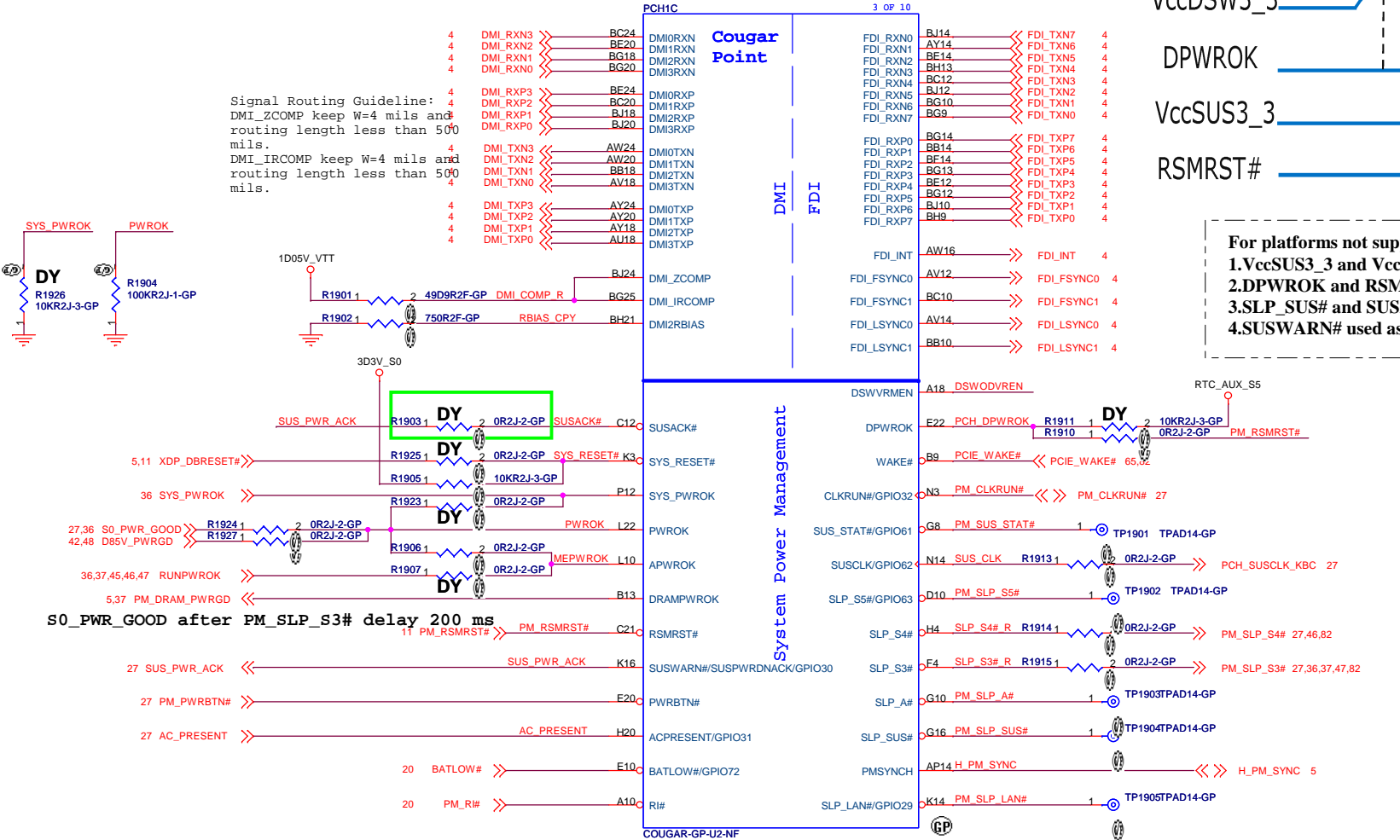
Signal Routing Guideline:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

Deep S4/S5 Supported

Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
 2.DPWROK and RSMRST# will rise at the same time (connected on board)
 3.SLP_SUS# and SUSACK# are left as 'no connect'
 4.SUSWARN# used as SUSPWRDNACK/GPIO30



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SSID = PCH

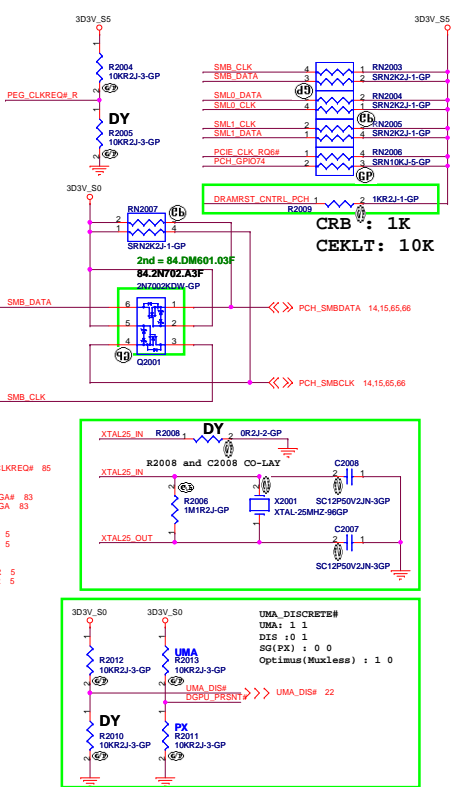
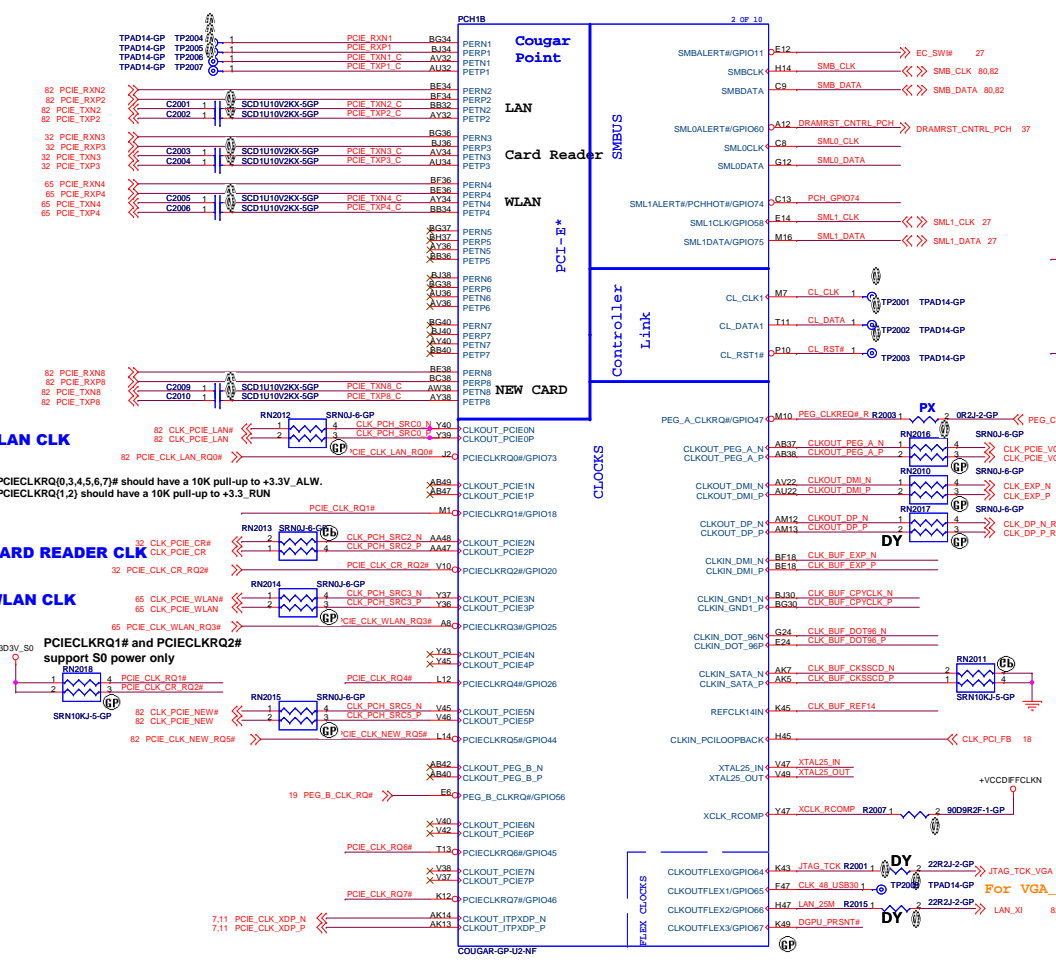


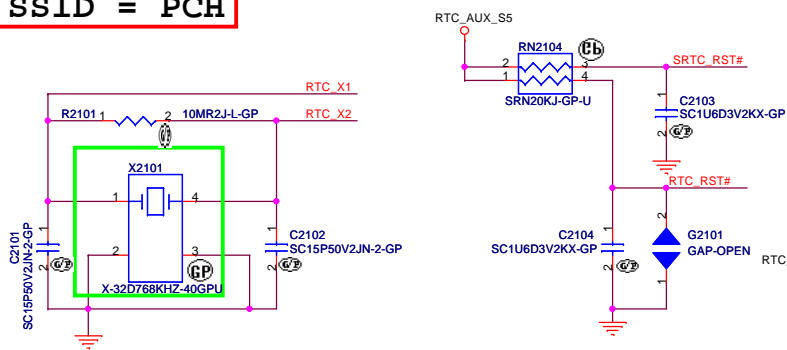
Table 20.1- Dual N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002KDOW	N/A	84.2N702.A3F
DIODES	DMN601DWK-7	N/A	84.DM601.03F
NXP	2N7002BKS	N/A	84.2N702.E3F

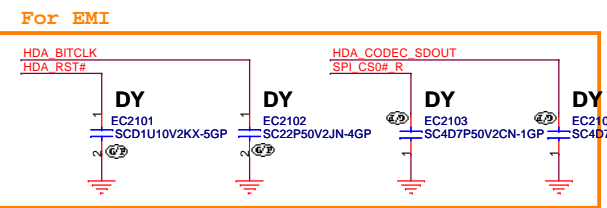
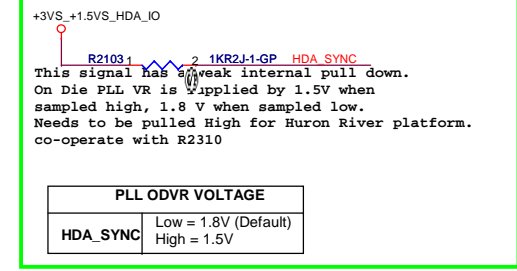
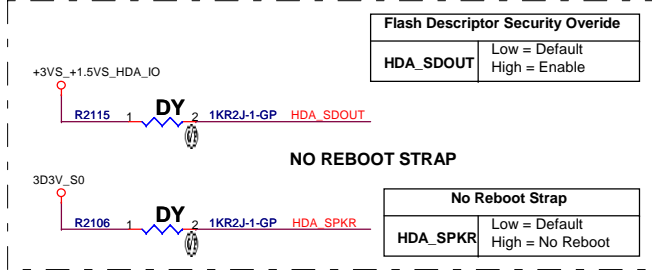
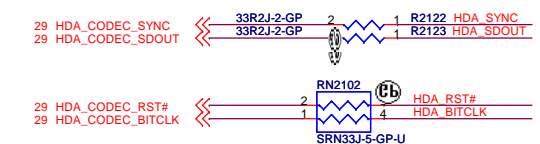
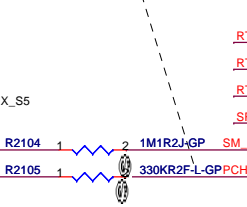
SSID = PCH

Table 21.1 Project_ID

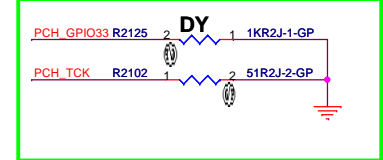
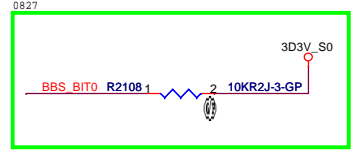
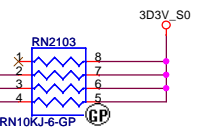
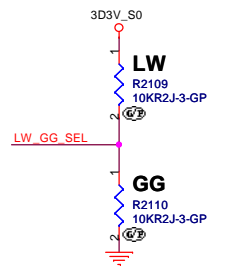
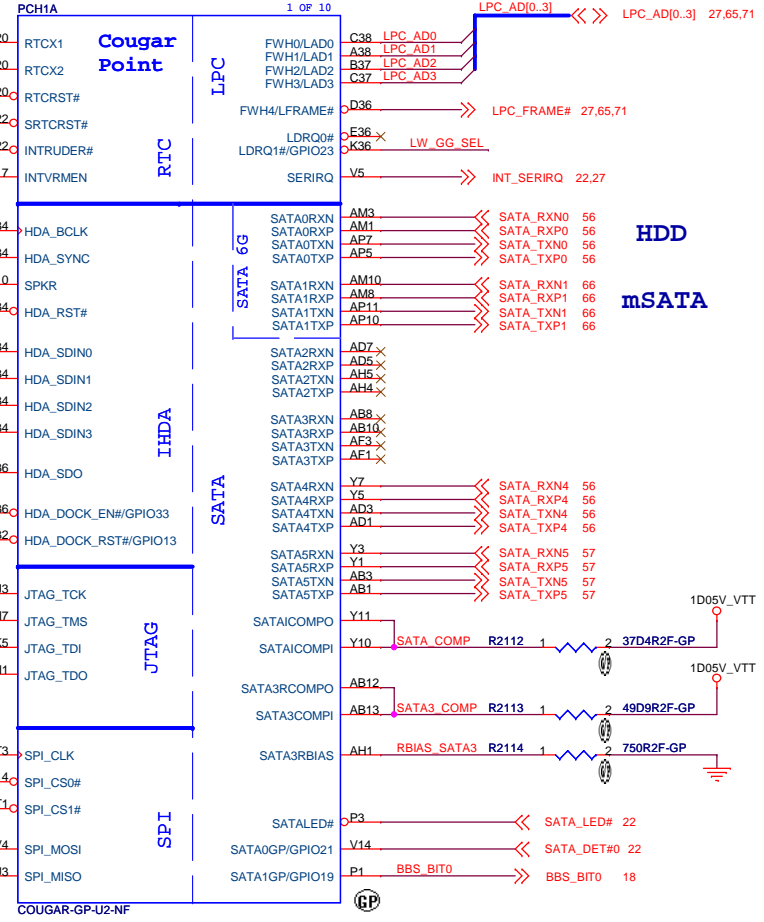
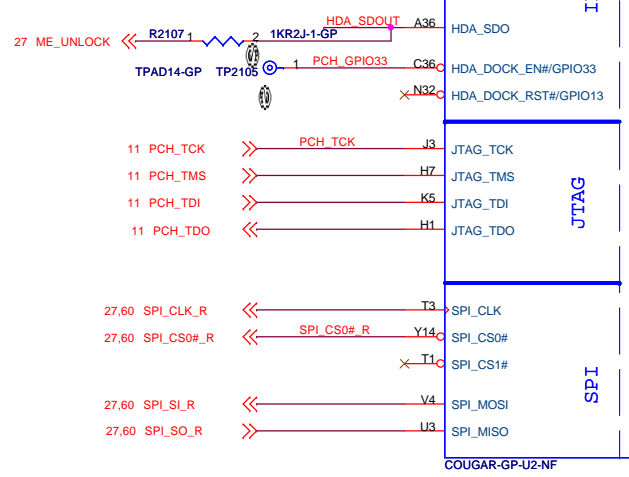
	LW_GG_SEL
LW	High
GG	LOW



INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



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Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

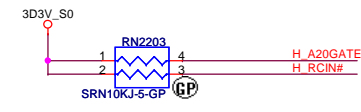
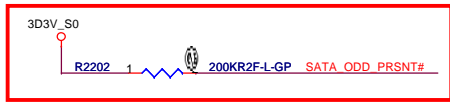
Size: A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

Date: Tuesday, November 09, 2010 Sheet 21 of 94

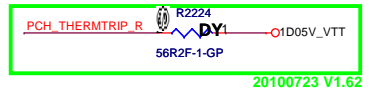
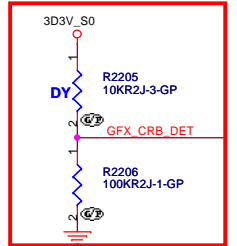
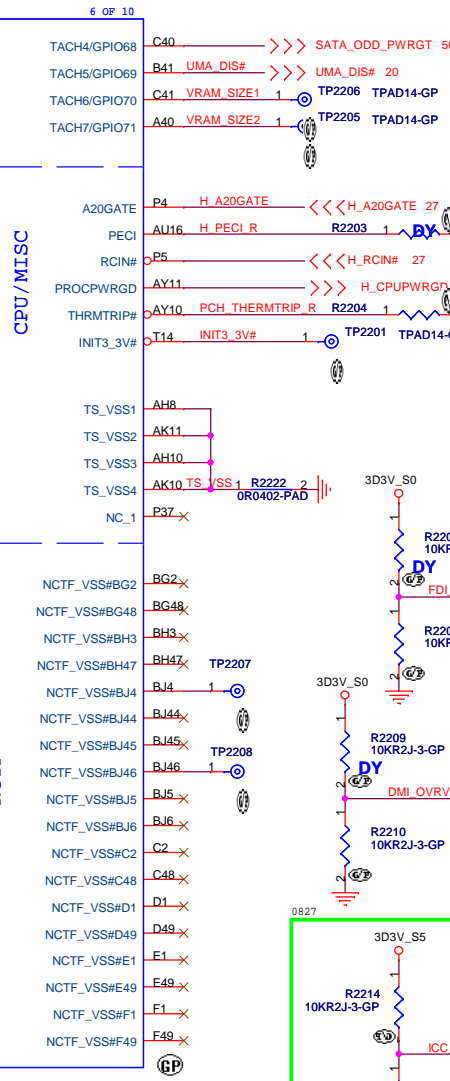
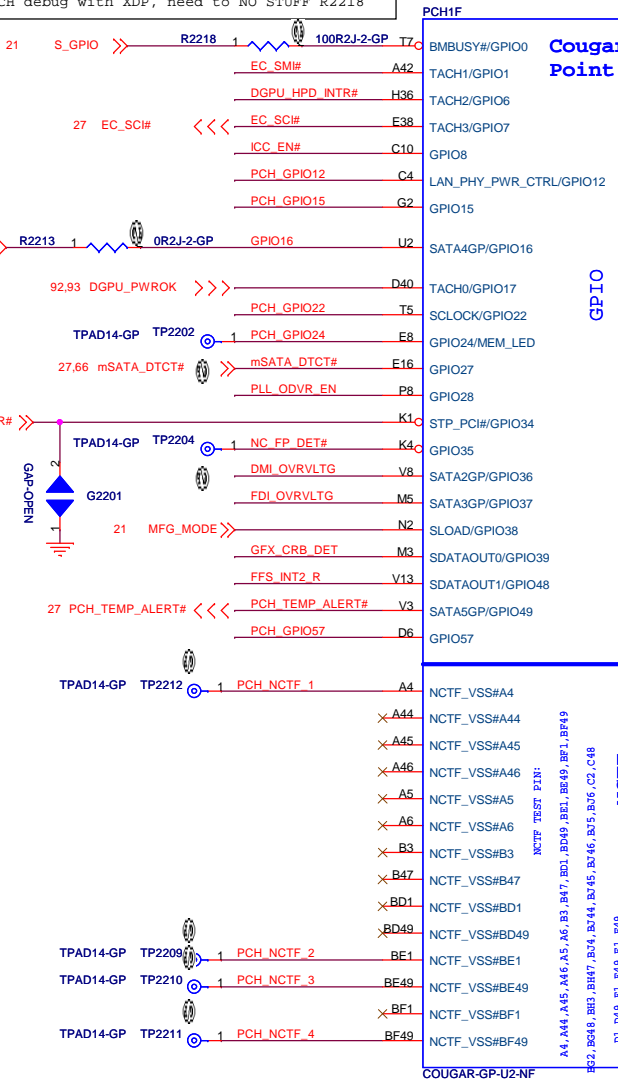
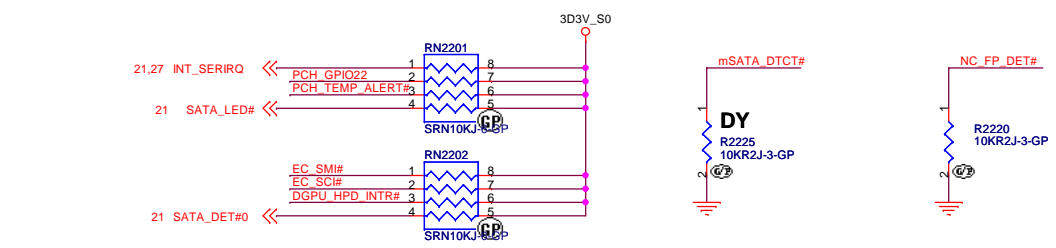
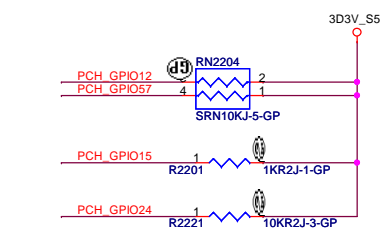
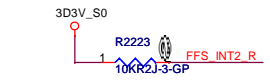
SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regulator, should not place external pull down.

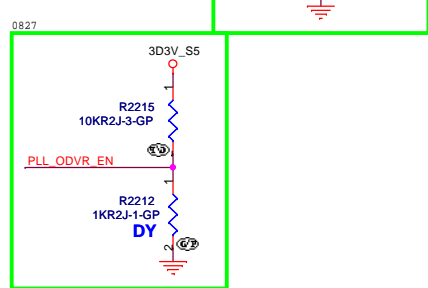


FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT]
	LOW (R2211) - ENABLED

PLL ON DIE VR ENABLE	
ENABLED -- HIGH (R2212 UNSTUFFED)	DEFAULT
DISABLED -- LOW (R2212 STUFFED)	



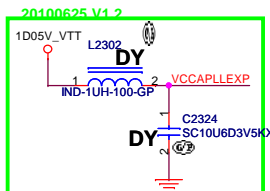
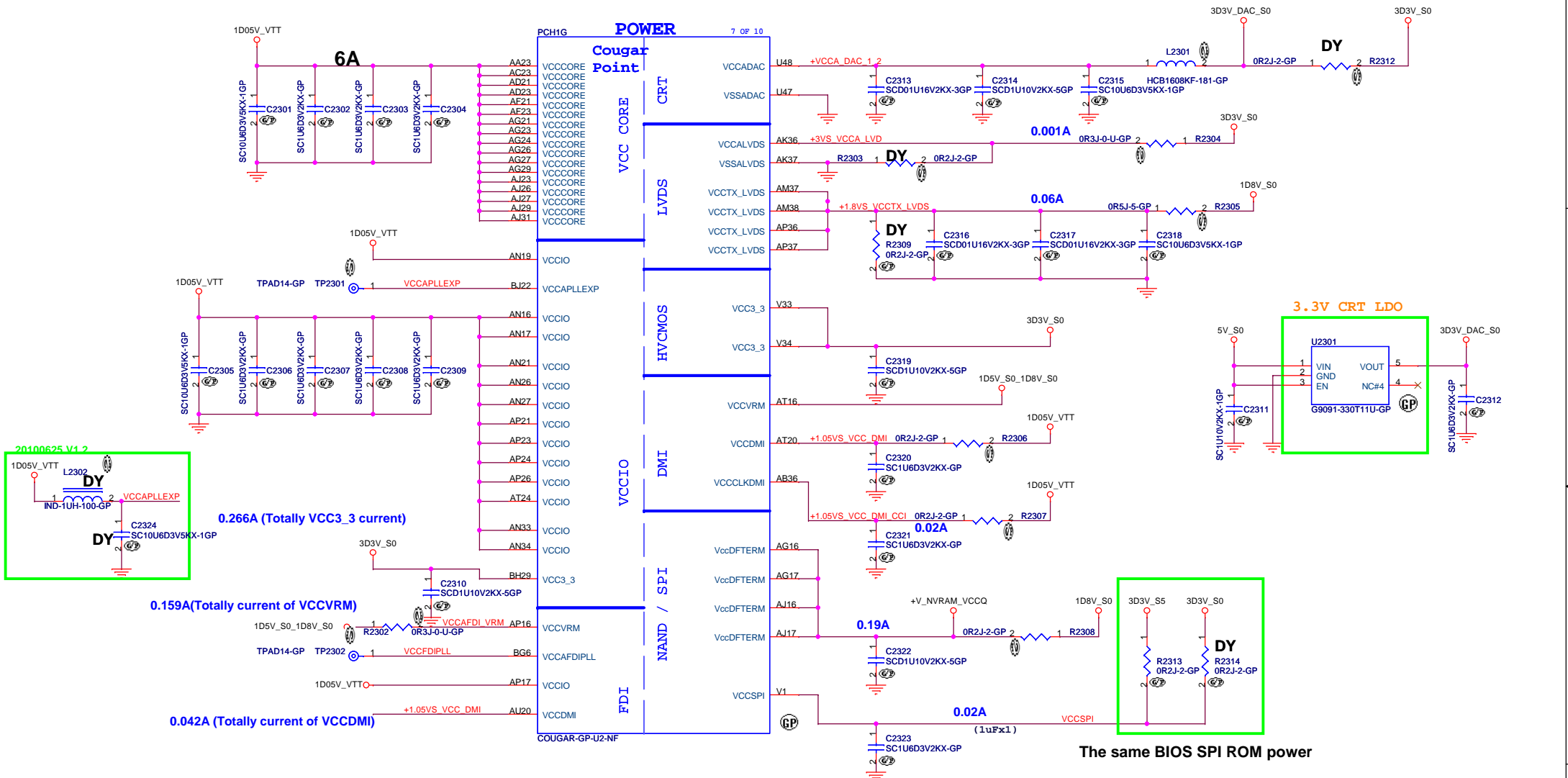
<Core Design>

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PCH (GPIO/CPU)		
Title		
Size A3	Document Number	Rev
	LLW-1 / LGG-1	SB
Date: Tuesday, November 09, 2010	Sheet 22	of 94

SSID = PCH

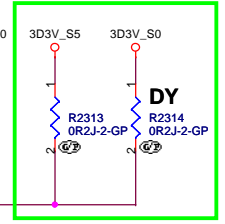
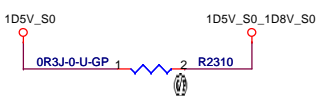


0.266A (Totally VCC3_3 current)

0.159A(Totally current of VCCVRM)

0.042A (Totally current of VCCDMI)

VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
 co-operate with R2103



The same BIOS SPI ROM power

Table 23.1- LDO Regulator multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
GMT	G9091-330T11U	N/A	74.09091.J3F
RICHTEK	RT9198-33GBR	N/A	74.09198.Q7F

<Core Design>

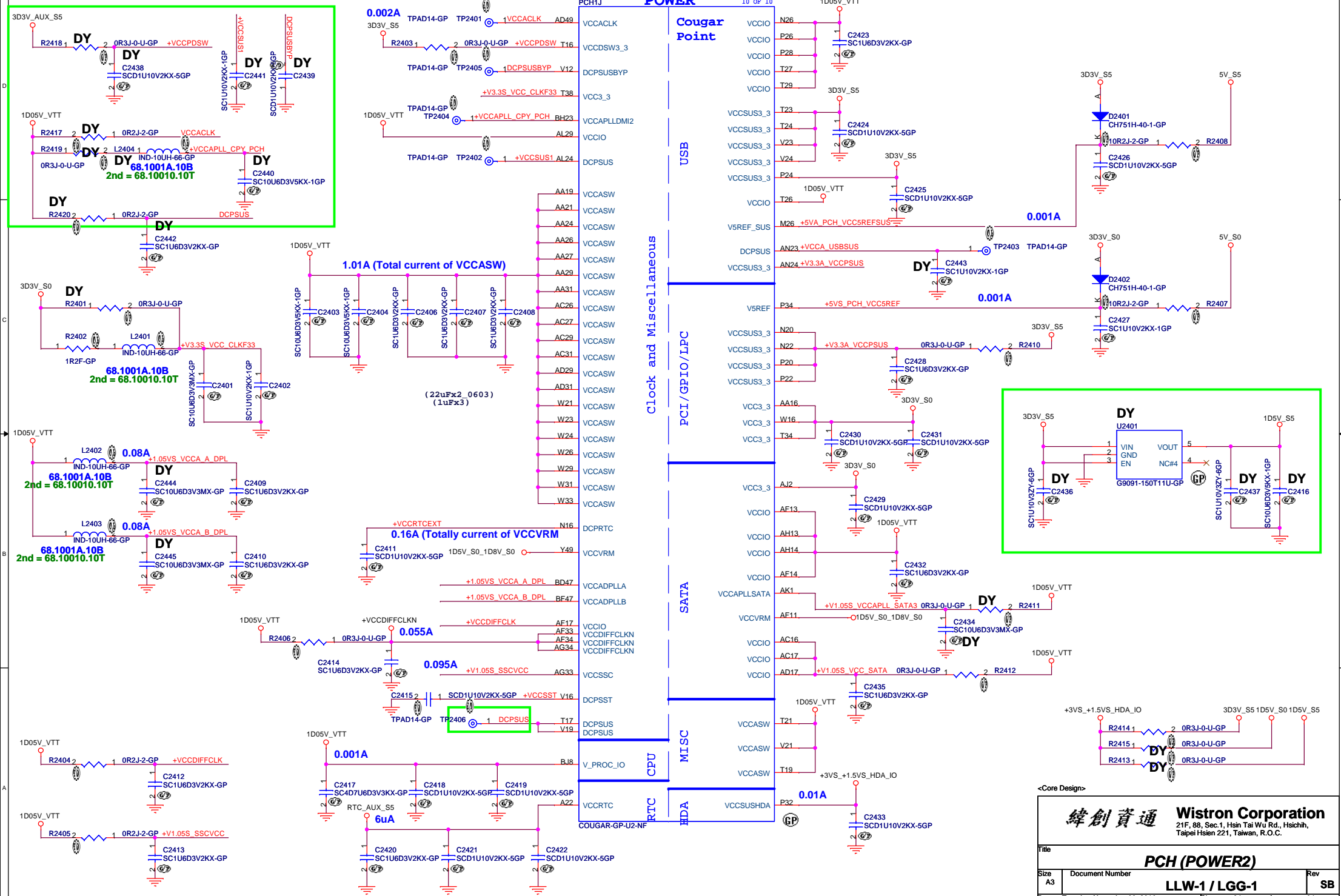
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Title: **PCH (POWER1)**

Size A3	Document Number	Rev
	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 23 of 94

SSID = PCH



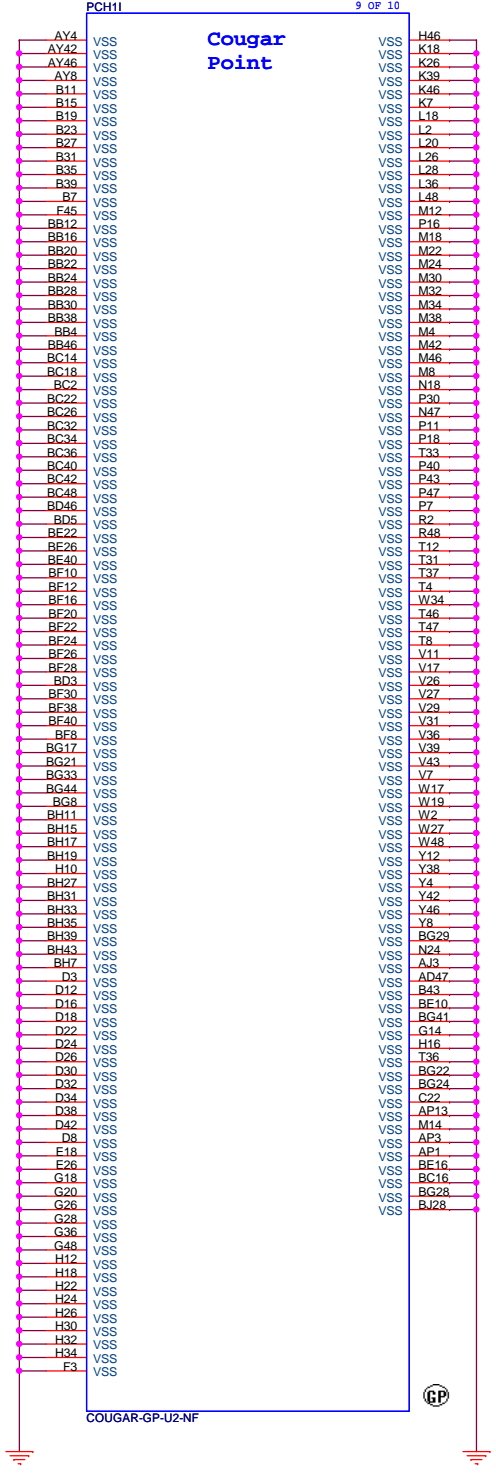
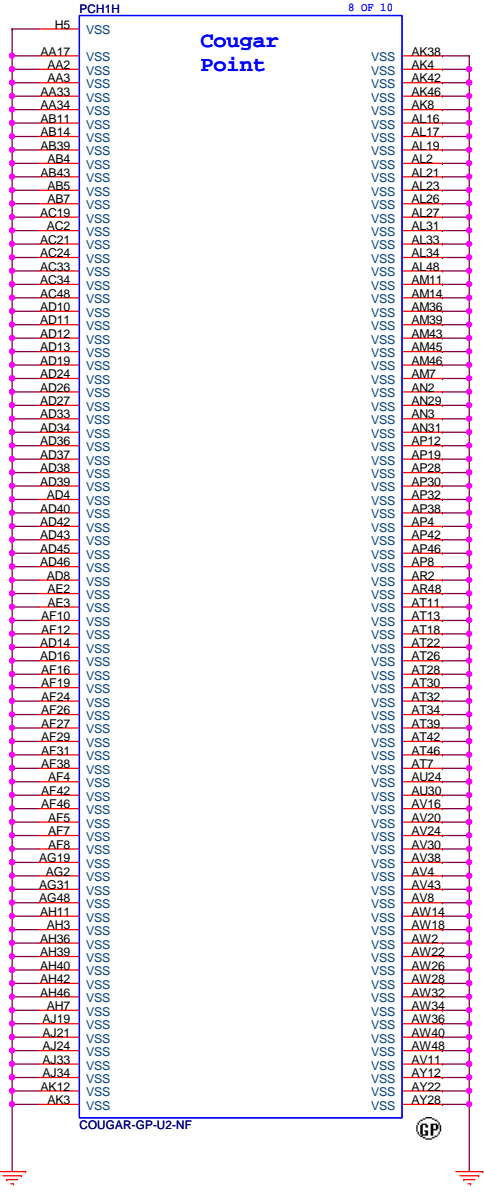
<Core Design>

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Title: **PCH (POWER2)**

Size A3	Document Number	Rev
	LLW-1 / LGG-1	SB
Date: Tuesday, November 09, 2010	Sheet 24 of 94	

SSID = PCH



<Core Design>

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Title: **PCH (VSS)**

Size: A3	Document Number: LLW-1 / LGG-1	Rev: SB
Date: Tuesday, November 09, 2010	Sheet: 25	of 94

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

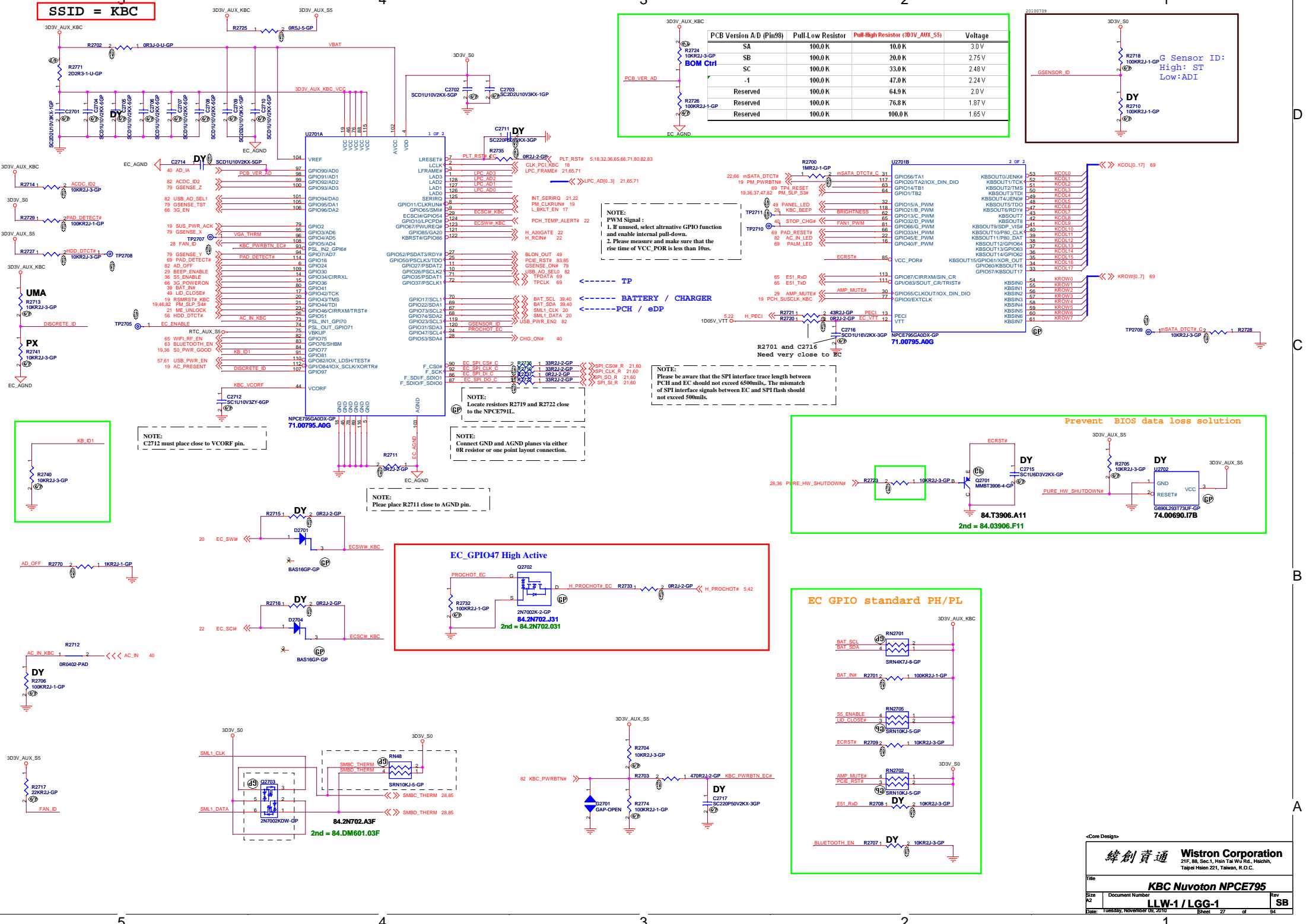
LLW-1 / LGG-1

Rev
SB

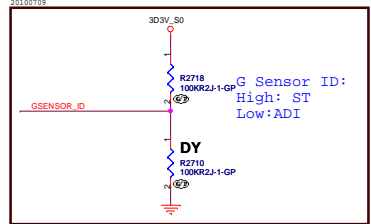
Date: Tuesday, November 09, 2010

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SSID = KBC



PCB Version A/D (Pin#9)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V



NOTE:
PWM Signal:
1. If unused, select alternative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10ns.

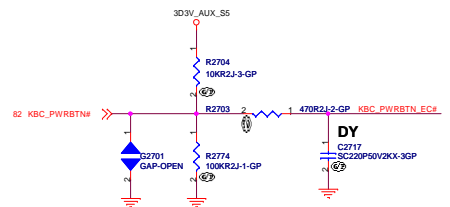
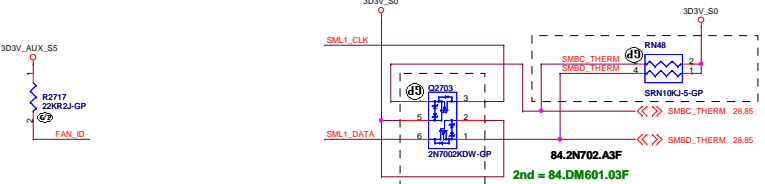
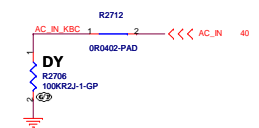
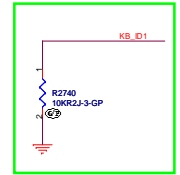
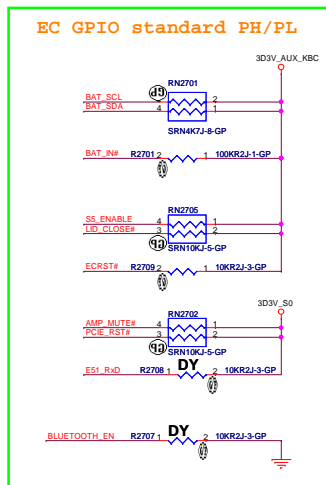
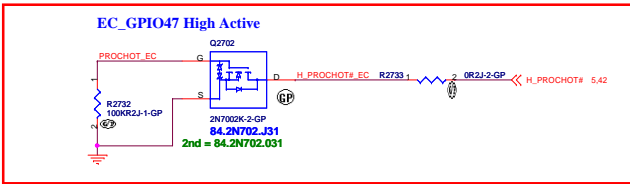
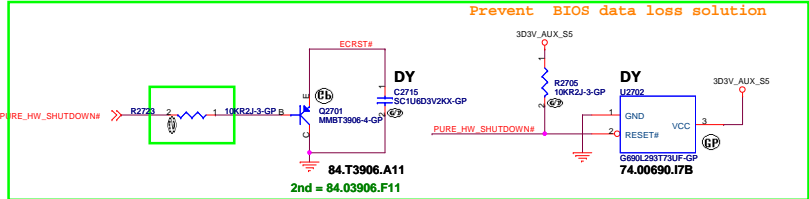
NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE:
Locate resistors R2719 and R2722 close to the NPCE7911L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point jump connection.

NOTE:
Please place R2711 close to AGND pin.

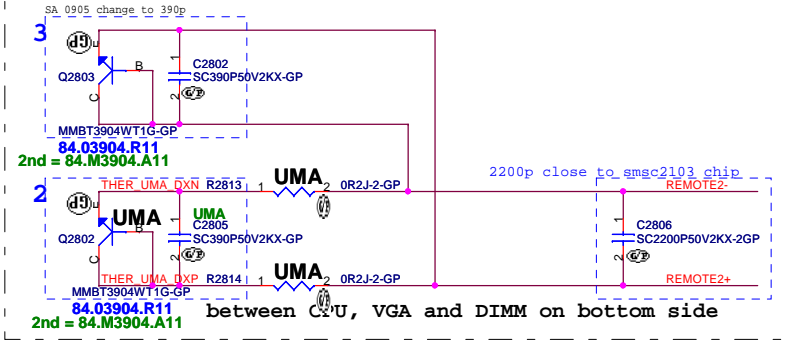
NOTE:
C2712 must place close to VCONF pin.



SSID = Thermal

Thermal sensor

Close to SO-DIMM side.



T8

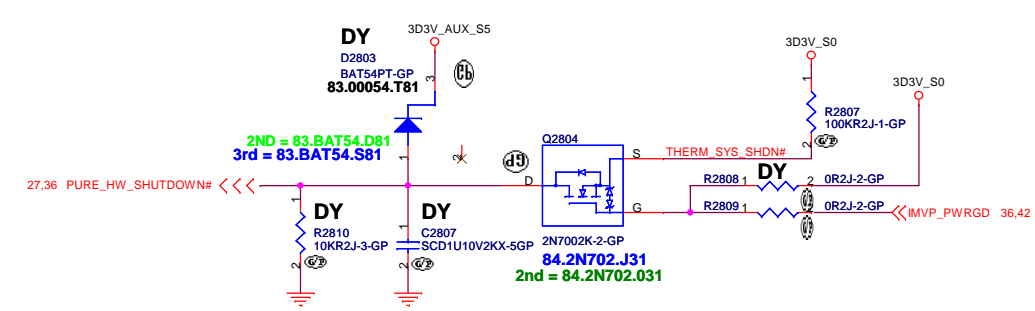
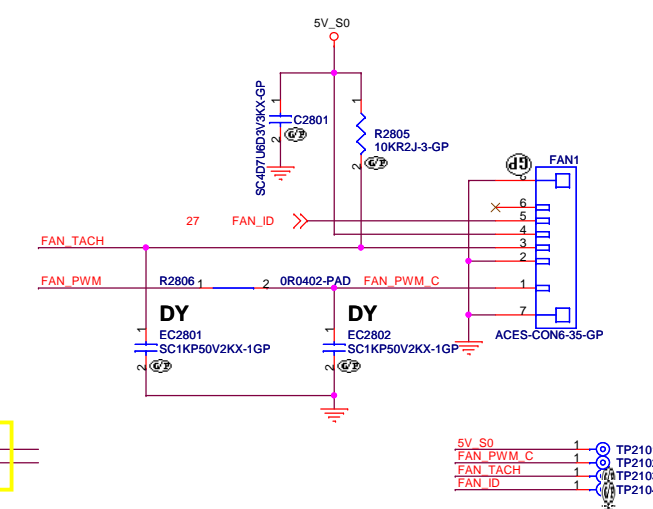
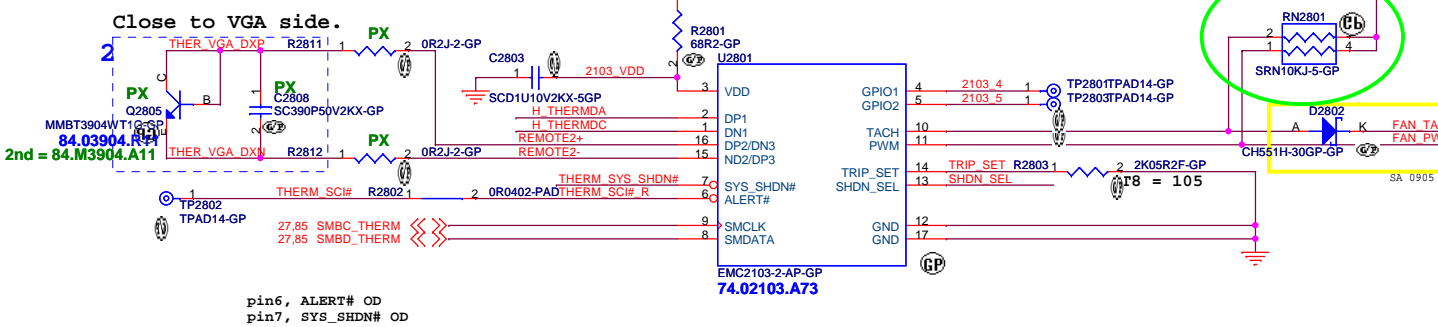
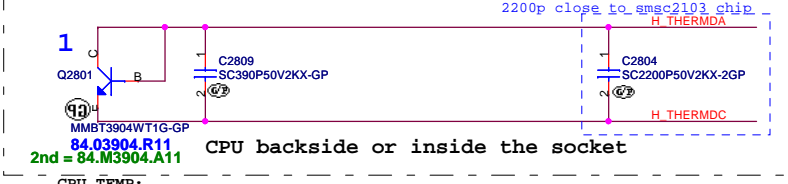


Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11

<Core Design>

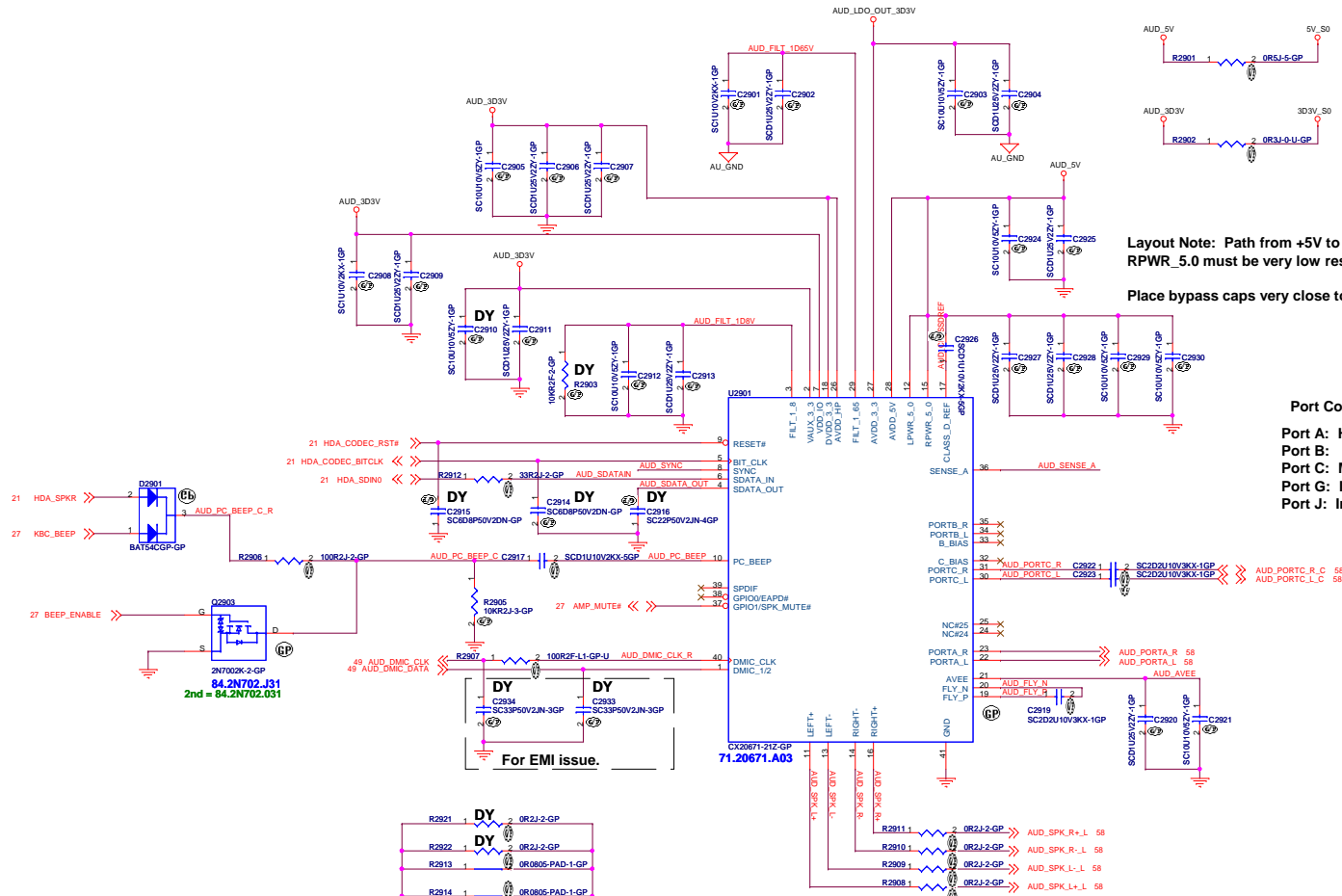
緯創資通 Wistron Corporation
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Title: **THERMAL SENSOR SMSC EMC2103**

Size A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

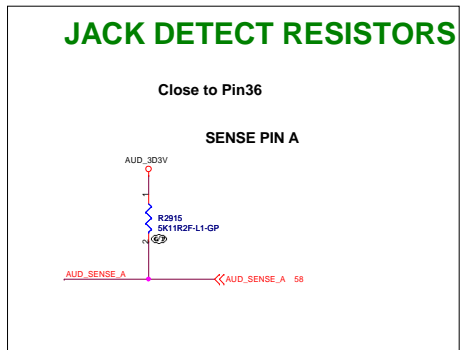
Date: Tuesday, November 09, 2010 Sheet 28 of 94

AUDIO CODEC



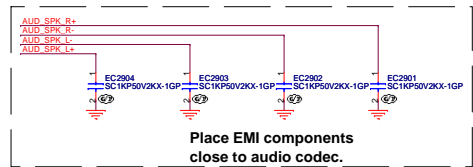
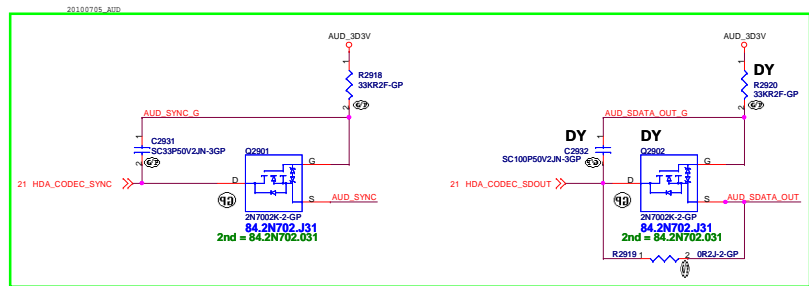
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).
Place bypass caps very close to device.

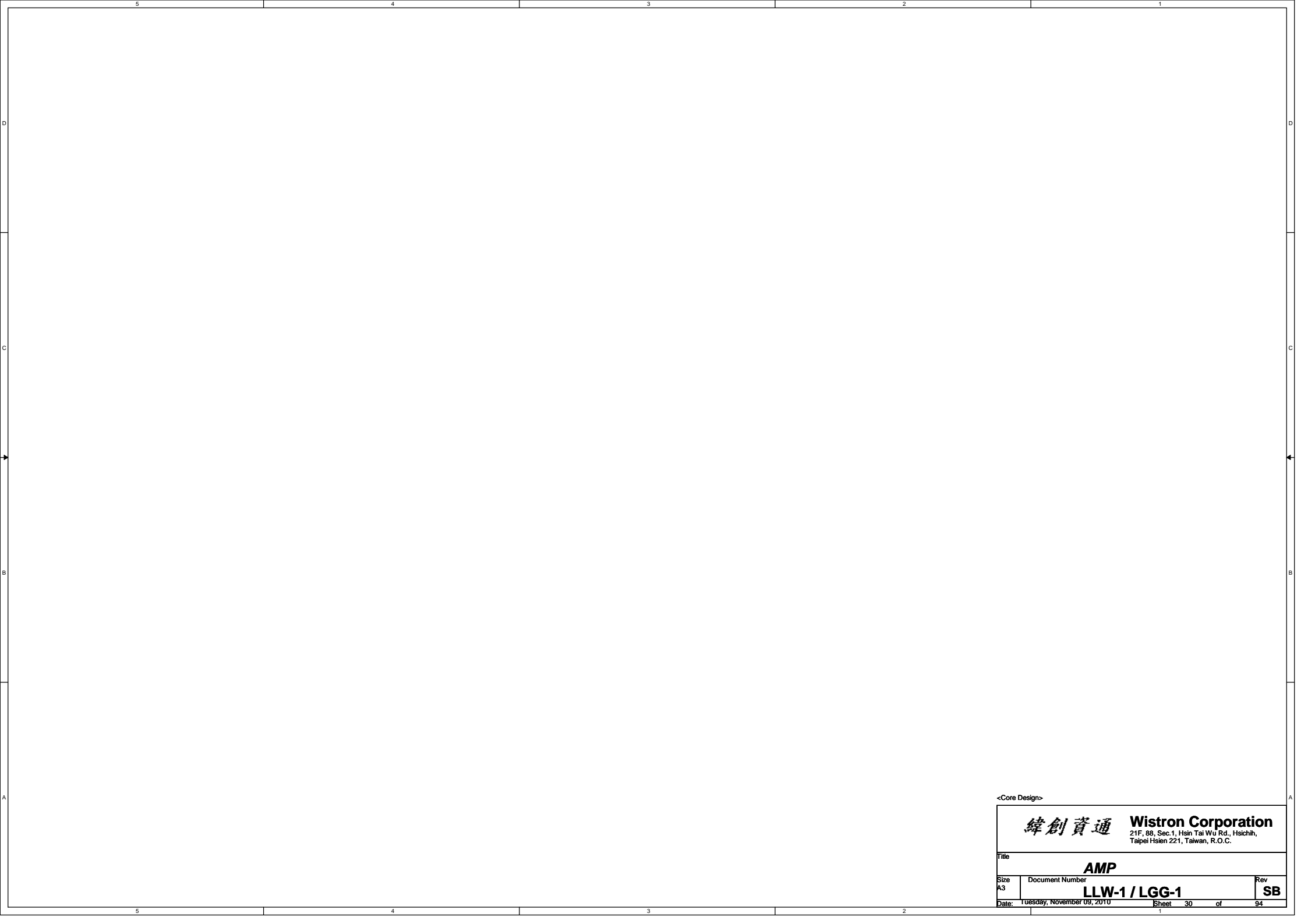
- Port Configuration**
- Port A: Headphone jack
 - Port B:
 - Port C: Microphone jack
 - Port G: Internal stereo speakers
 - Port J: Internal stereo digital mic



Should be used at least 20 MIL width copper line for "AUD_SPK_L+", "AUD_SPK_L-", "AUD_SPK_R+", "AUD_SPK_R-"

Place R2913/R2914 under CODEC, and place R2921/R2922 near CODEC





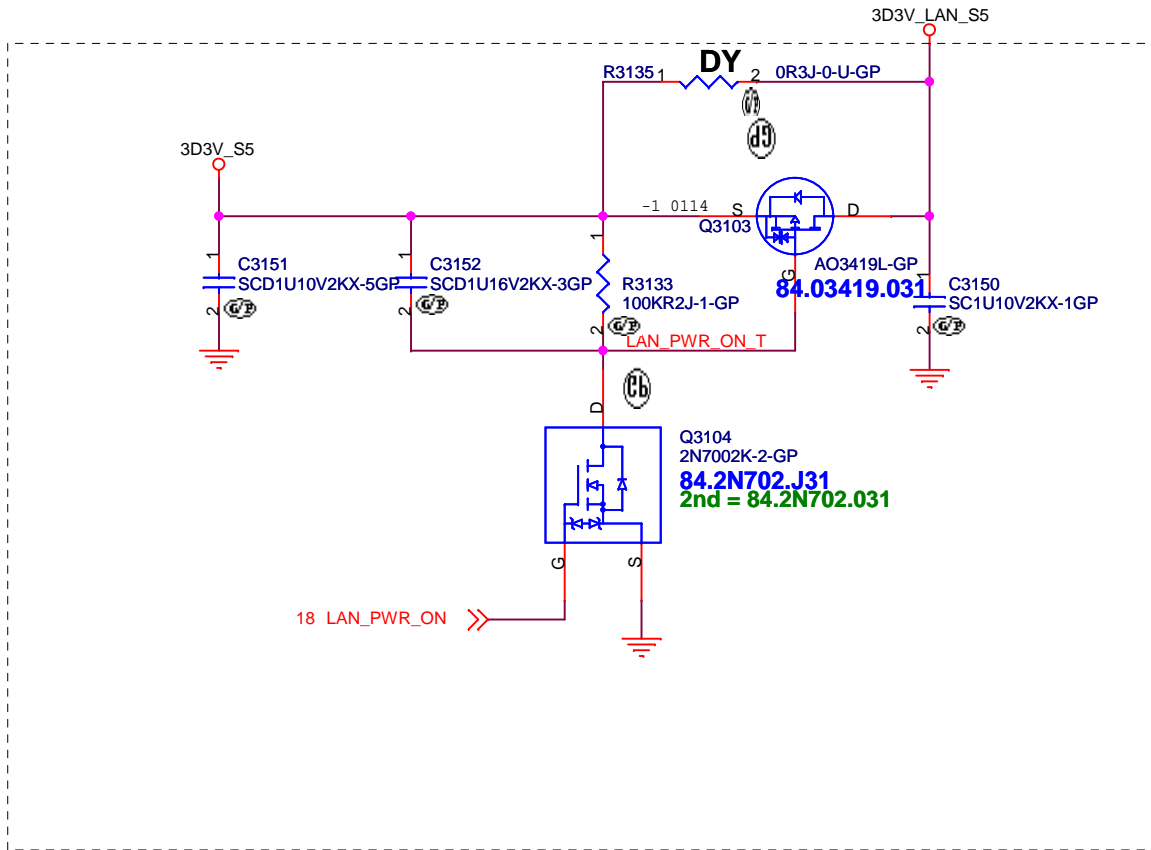
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title **AMP**

Size A3 Document Number **LLW-1 / LGG-1** Rev **SB**

Date: Tuesday, November 09, 2010 Sheet 30 of 94



<Core Design>

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Title

LAN PWR SW

Size

Document Number

Rev

A4

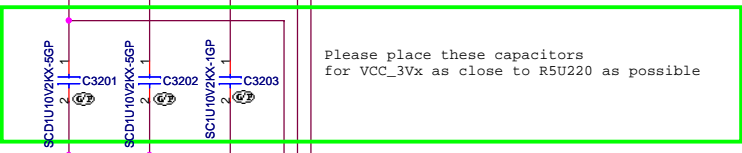
LLW-1 / LGG-1

SB

Date: Tuesday, November 09, 2010

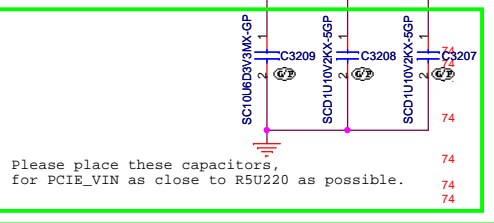
Sheet 31 of 94

Please place these capacitors, for PCIE_VOUT as close to R5U220 as possible.



Please place these capacitors for VCC_3Vx as close to R5U220 as possible

Please apply wide trace for MF_VOUT between R5U220 and SD Card Slot.
- 2A (W=2mm) Recommended.
- Please consider the number of vias when layer of MF_VOUT is changed.



Please place these capacitors, for PCIE_VIN as close to R5U220 as possible.

RICOH recommends strongly, Trace length Difference among these SDXC signals are smaller than 0.5 inches.
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

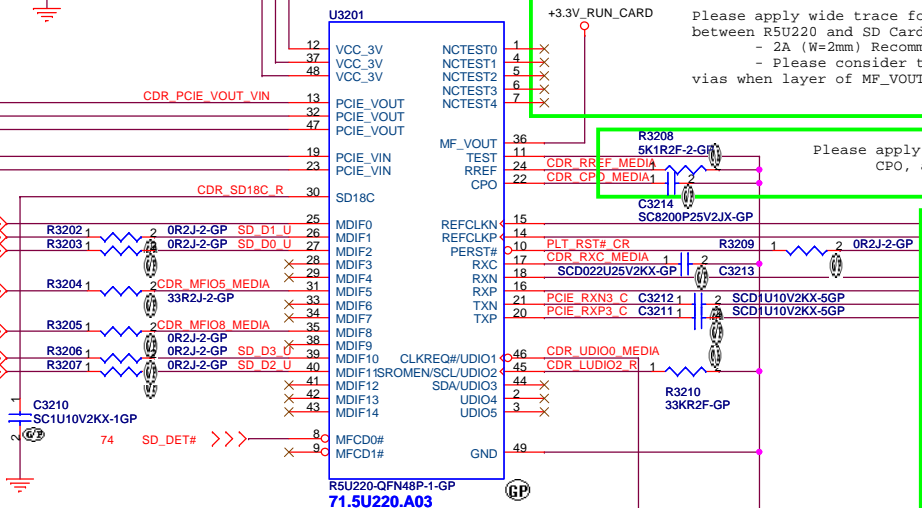
RICOH recommends strongly, the trace length for these SDXC signals are less than 6-inches.
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

Please apply capacitor C3210 for SD18C as close as possible to R5U220.

Please apply 50 ohm impedance control for these SDXC signals;
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

Please use Microstrip trace routing for these SDXC signals
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

MEDIA I/F	SD/MMC	MEMORYSTICK	XD
MFIO00	SDWP#	MSBS	XD_D7
MFIO01	SD_D1		XD_D6
MFIO02	SD_D0	MS_D1	XD_D5
MFIO03	(SD_D7)		XD_D4
MFIO04	(SD_D6)	(MS_D5)	XD_D3
MFIO05	SD_CLK	MSD0	XD_D2
MFIO06			XD_D1
MFIO07	(SD_D5)	(MS_D4)	XD_D0
MFIO08	SD_CDM	MS_D2	XD_WP#
MFIO09	(SD_D4)	(MS_D6)	XD_WE#
MFIO10	SD_D3	MS_D3	XD_ALE
MFIO11	SD_D2		XD_CLE
MFIO12			XD_CE#
MFIO13		(MS_D7)	XD_RE#
MFIO14		MS_CLK	XD_R/B
MFCD0#	SDDC#		XDCD0#
MFCD1#		MSINS#	XDCD1#

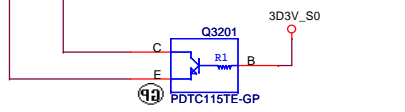


Please apply external parts, R456, C457, R415 for RXC, CPO, and RREF, as close as possible to R5U220.

Please apply AC Coupling capacitors, C455 and C454, for TXP/TXN as close as possible to R5U220.

Please apply equal trace length for these signal pairs:
CLK_PCIE_CR, CLK_PCIE_CR#
PCIE_TXN3, PCIE_TXP3
PCIE_RXN3_C, PCIE_RXP3_C
PCIE_RXN3, PCIE_RXP3

Please apply differential impedance control for these signal pairs in conformity with Motherboard Design Guide;
CLK_PCIE_CR, CLK_PCIE_CR#
PCIE_TXN3, PCIE_TXP3
PCIE_RXN3_C, PCIE_RXP3_C
PCIE_RXN3, PCIE_RXP3



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Title: **R5U220 (CARD READER)**

Size A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

Date: Tuesday, November 09, 2010 Sheet 32 of 94

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<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		1394	
Size A4	Document Number	LLW-1 / LGG-1	Rev SB
Date: Tuesday, November 09, 2010		Sheet 33	of 94

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4

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C

C

B

B

A

A

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<Core Design>

<p>緯創資通</p>	<p>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>
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<p>Title</p>	<p>Smart Card Reader</p>
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<p>Size A4</p>	<p>Document Number LLW-1 / LGG-1</p>	<p>Rev SB</p>
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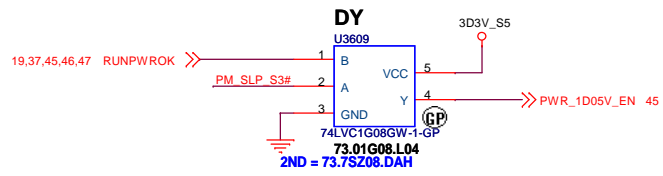
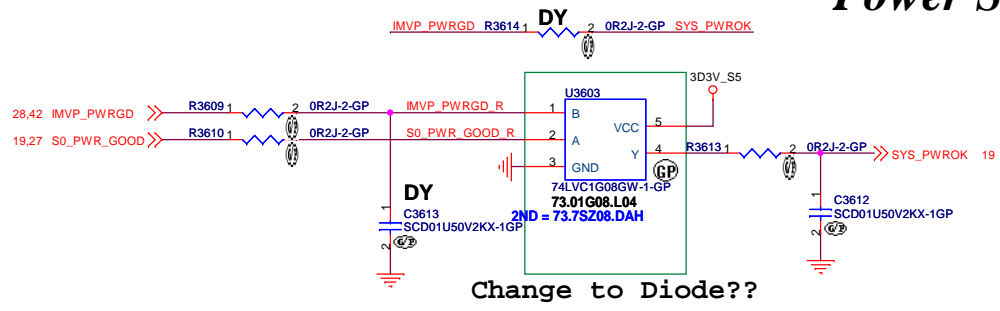
<p>Date: Tuesday, November 09, 2010</p>	<p>Sheet 34 of 94</p>
---	-----------------------

BLANK

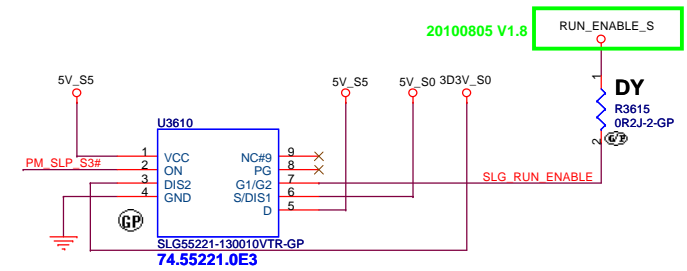
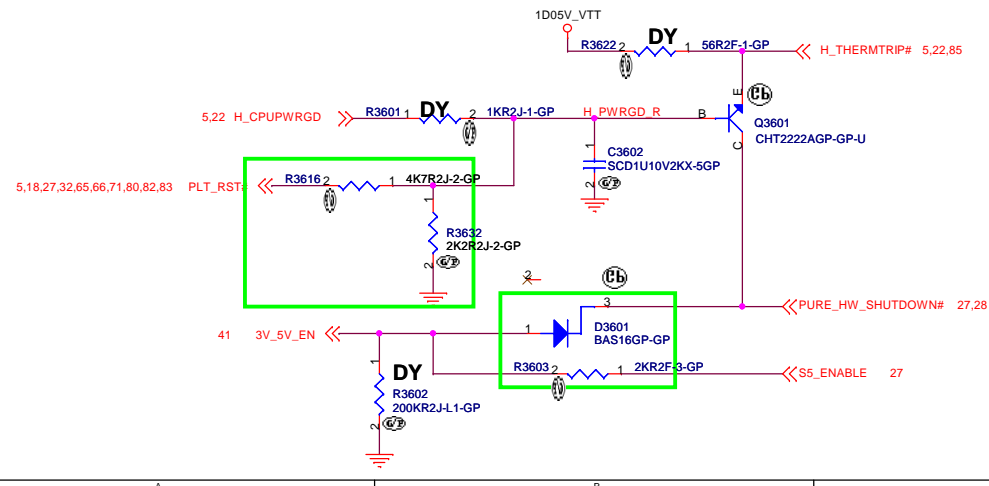
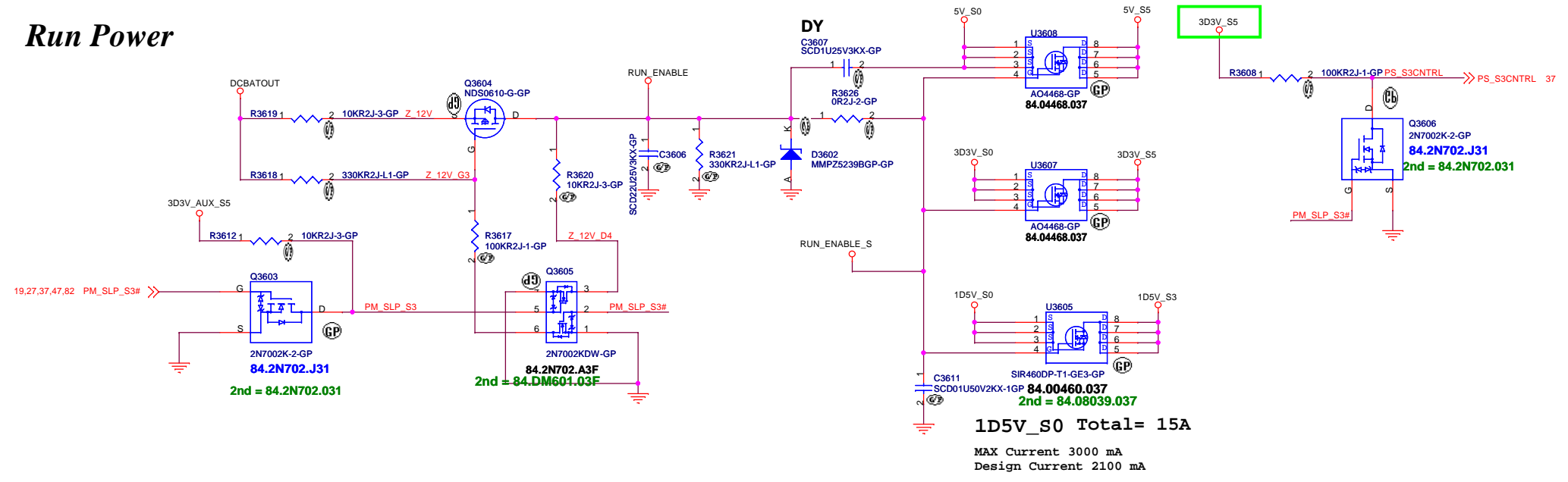
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB3.0			
Size	Document Number	Rev	
A4	LLW-1 / LGG-1	SB	
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Power Sequence



Run Power

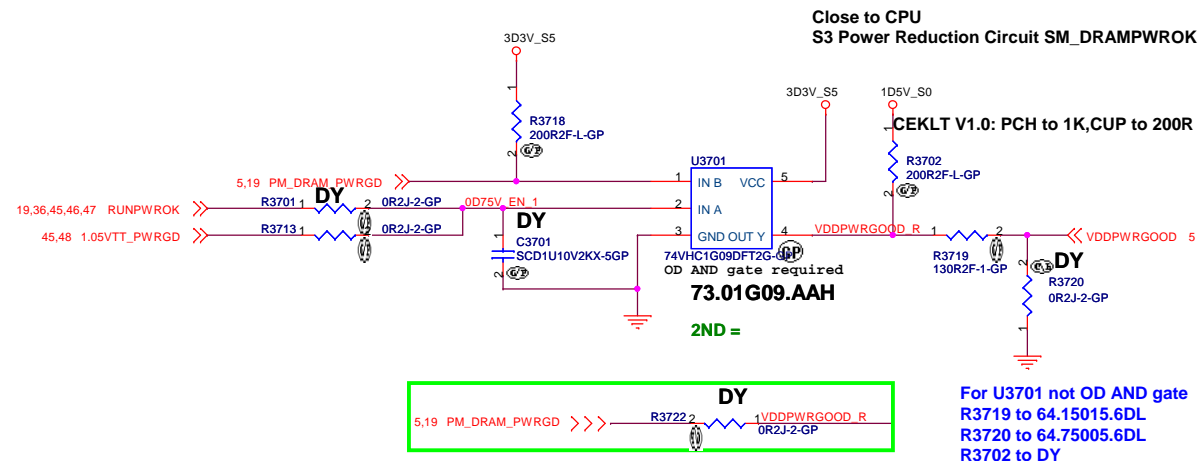
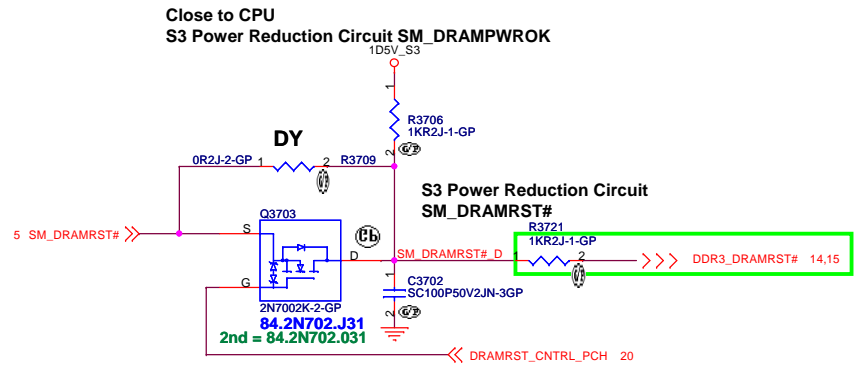
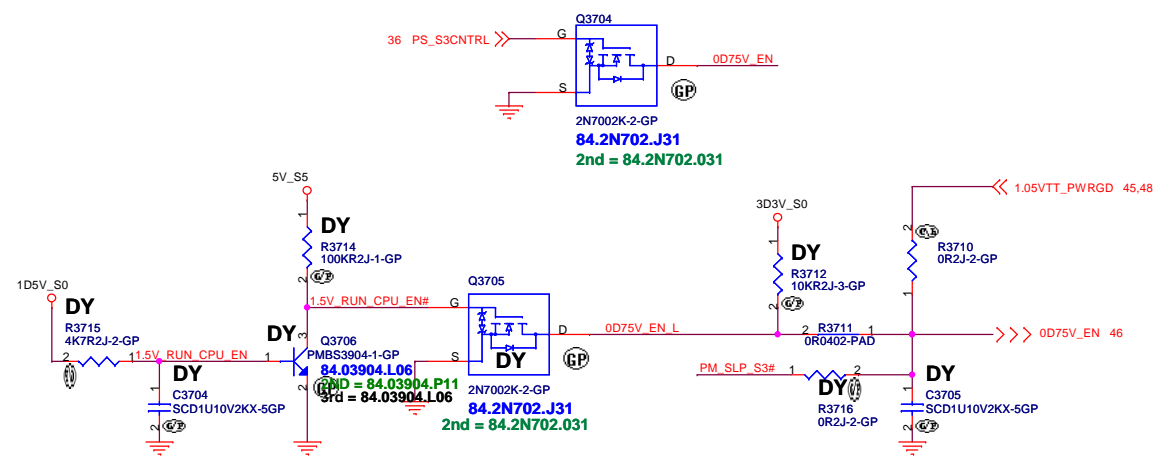
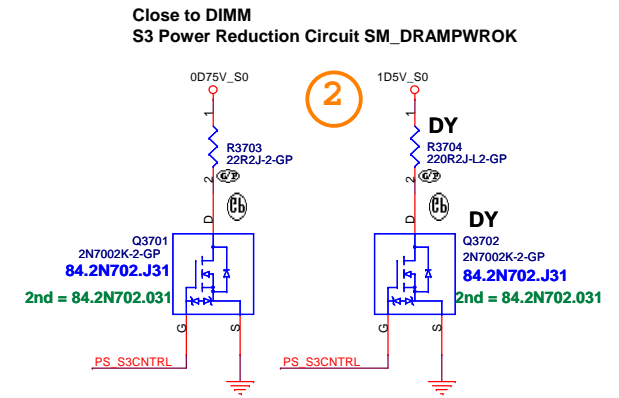
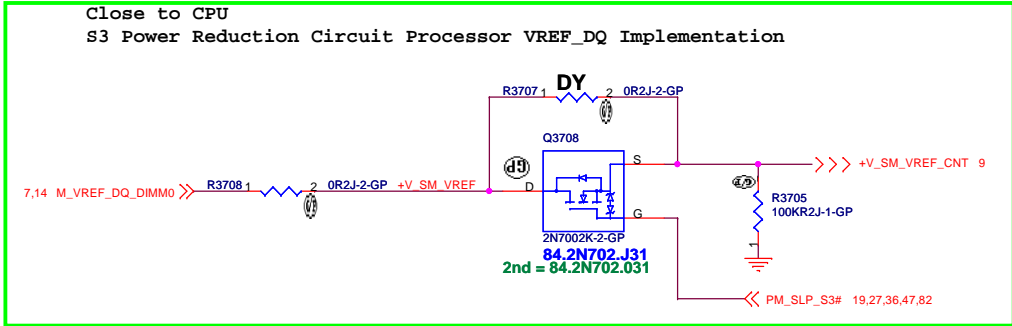


<Core Design>

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Title: **POWER SEQUENCE**

Size: A3	Document Number: LLW-1 / LGG-1	Rev: SB
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DY
5.19_PM_DRAM_PWRGD >>> R3722 2 1VDDPWRGOOD_R 0R2J-2-GP

For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

5

4

3

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D

D

C

C

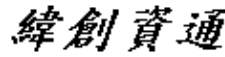
B

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A

A

<Core Design>

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Title	DCIN_JACK
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Size	Document Number	LLW-1 / LGG-1	Rev	SB
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5

4

3

2

1

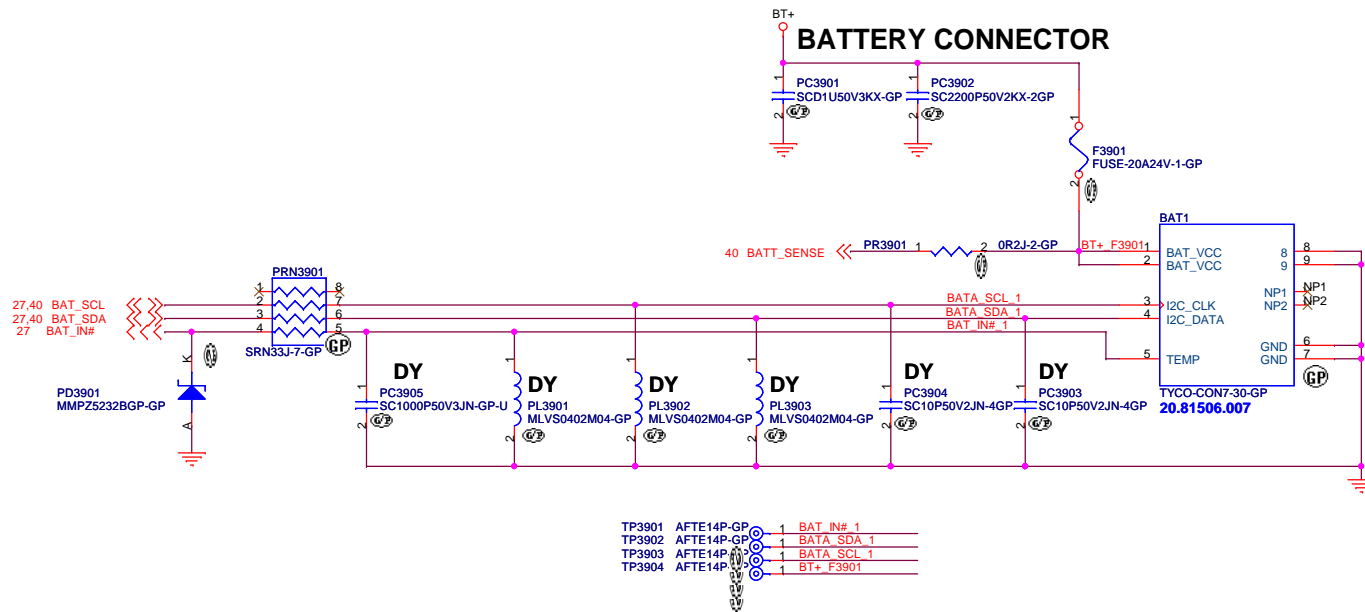
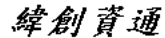


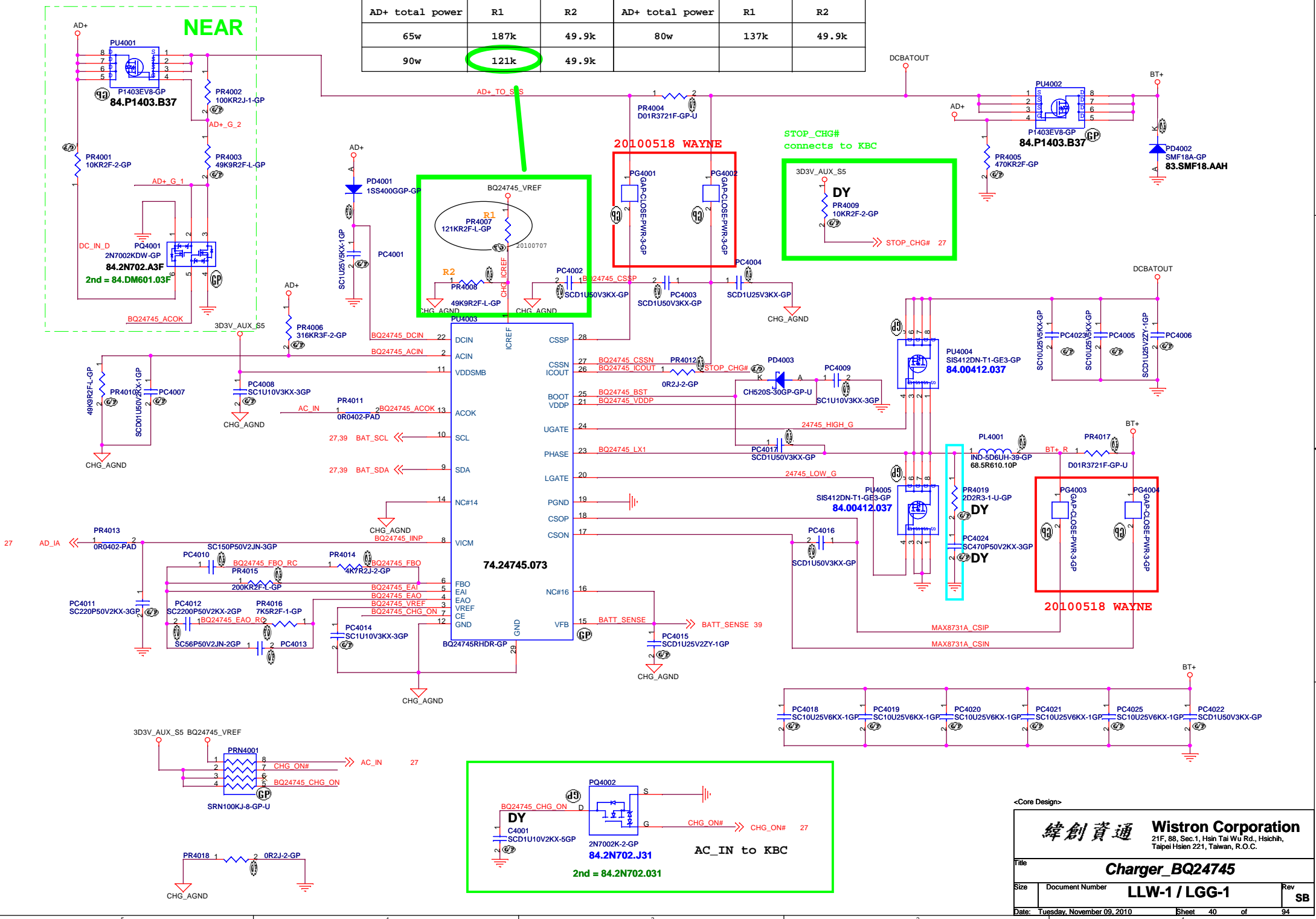
Table 39.1- Surface Mount Zener ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	MMPZ5232BGP	N/A	83.5R603.R3F
DIODES	MMSZ5232BS-7-F	N/A	83.5R603.K3F
PANJIT	MMSZ5232BS	N/A	83.5R603.Q3F

<Core Design>

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Title BATT_CONN	
Size Document Number	LLW-1 / LGG-1
Date: Tuesday, November 09, 2010	Sheet 39 of 94
Rev SB	

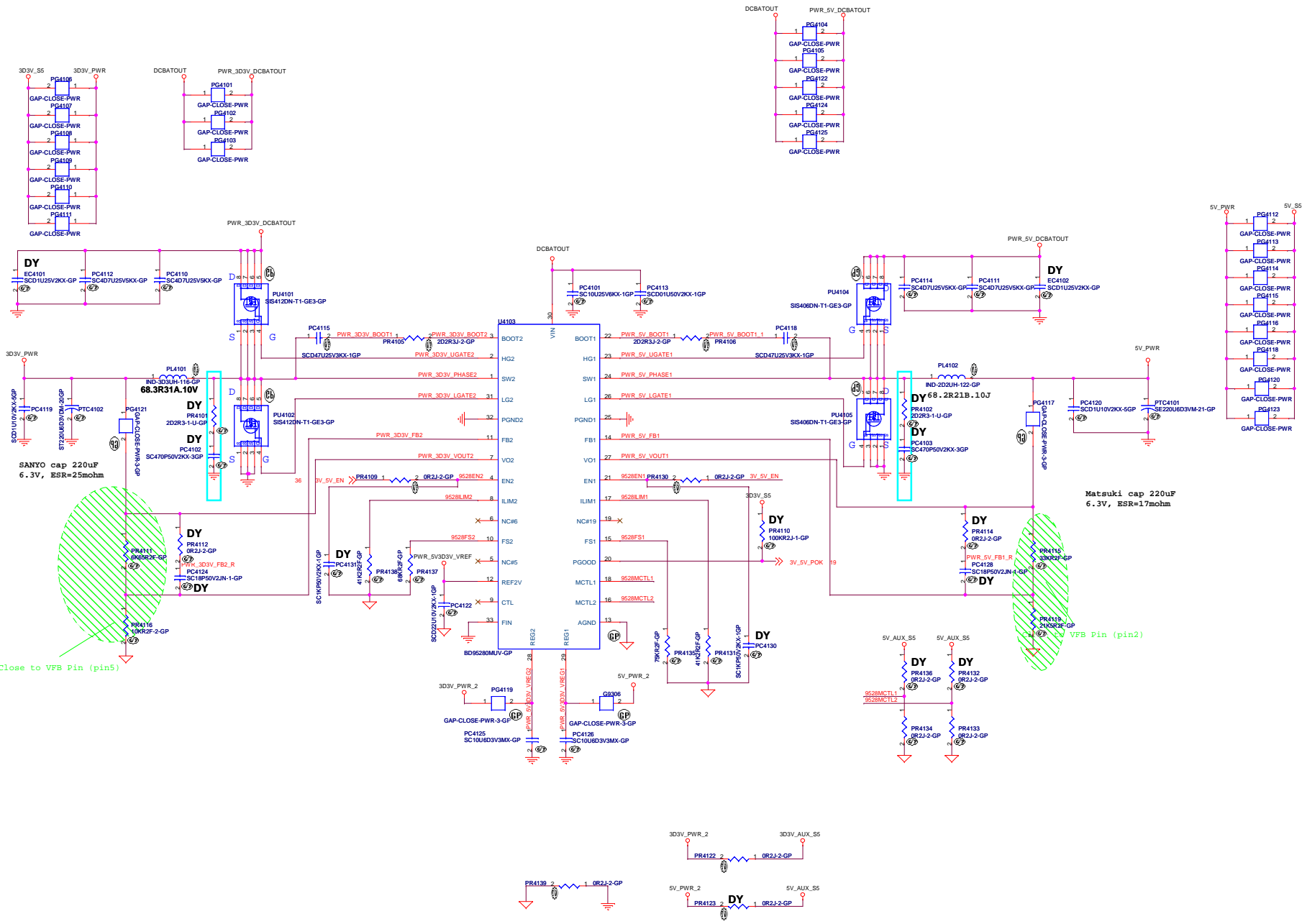
AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Charger_BQ24745			
Size		Document Number	Rev
		LLW-1 / LGG-1	SB
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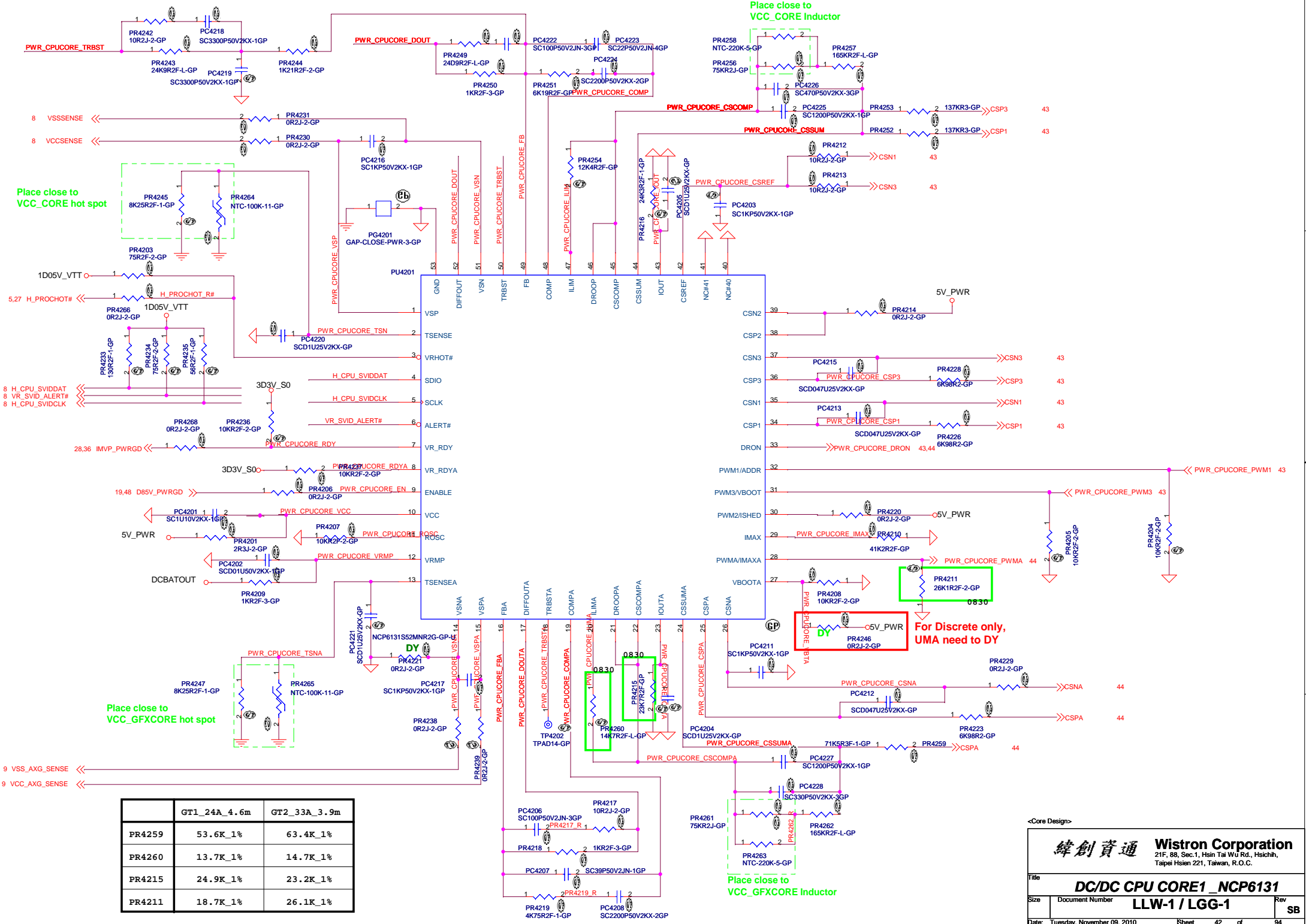
SSID = PWR.Plane.Regulator_5v3p3v



«Core Design»

緯創資通 Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V
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	GT1_24A_4.6m	GT2_33A_3.9m
PR4259	53.6K_1%	63.4K_1%
PR4260	13.7K_1%	14.7K_1%
PR4215	24.9K_1%	23.2K_1%
PR4211	18.7K_1%	26.1K_1%

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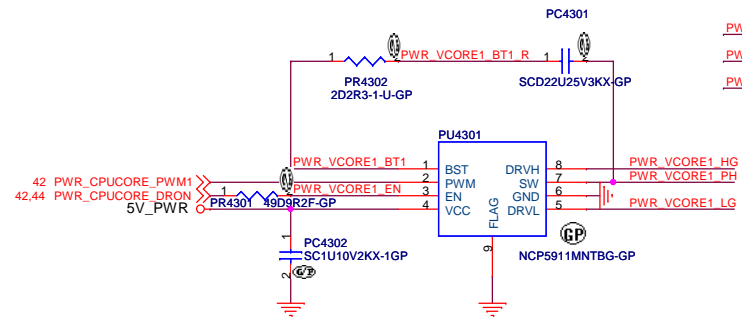
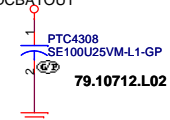
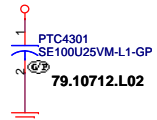
DC/DC CPU CORE1_NCP6131
 LLW-1 / LGG-1

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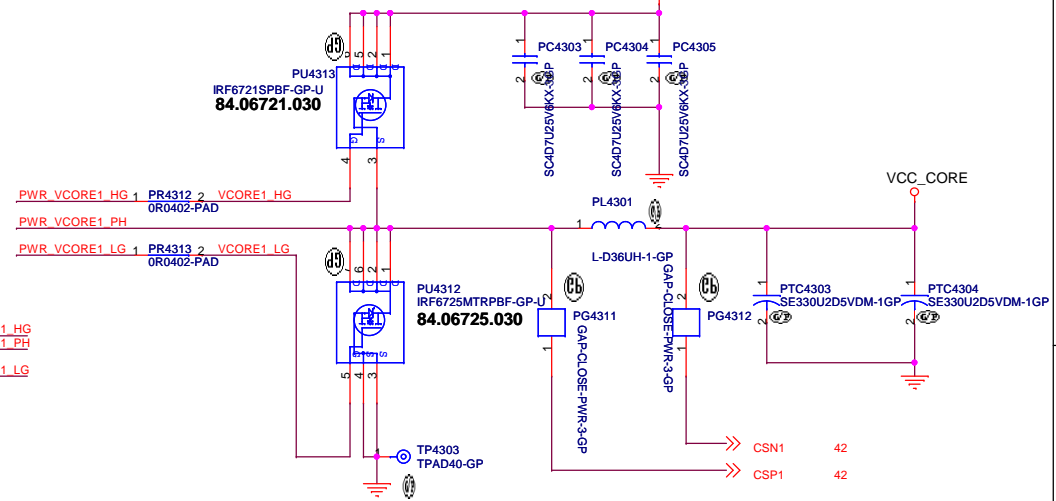
DCBATOUT

DCBATOUT



PWR_VCORE1_HG 1 PR4312 2_VCORE1_HG
 0R0402-PAD
 PWR_VCORE1_PH
 PWR_VCORE1_LG 1 PR4313 2_VCORE1_LG
 0R0402-PAD

DCBATOUT

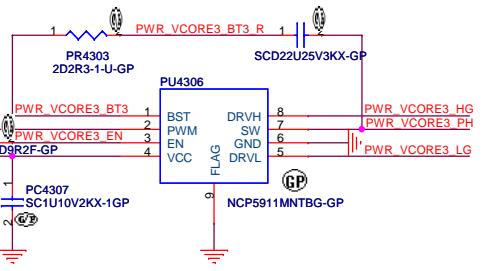


VCC_CORE

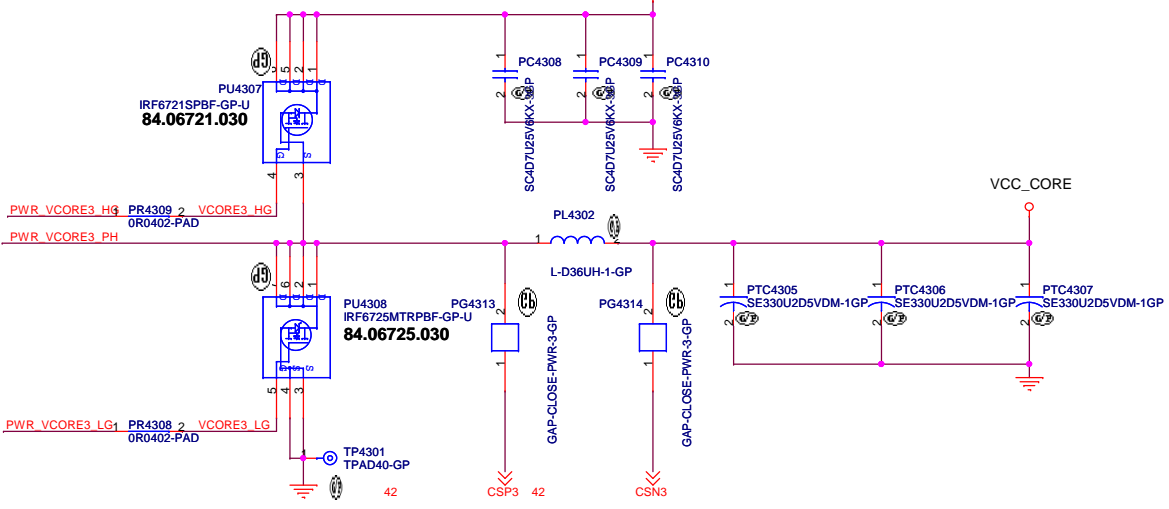
CSN1 42
 CSP1 42

PC4306

42 PWR_CPUCORE_PWM3
 42.44 PWR_CPUCORE_DRON
 5V_PWR



DCBATOUT



VCC_CORE

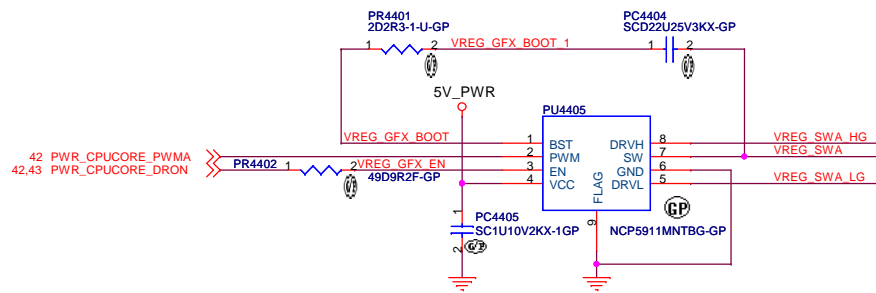
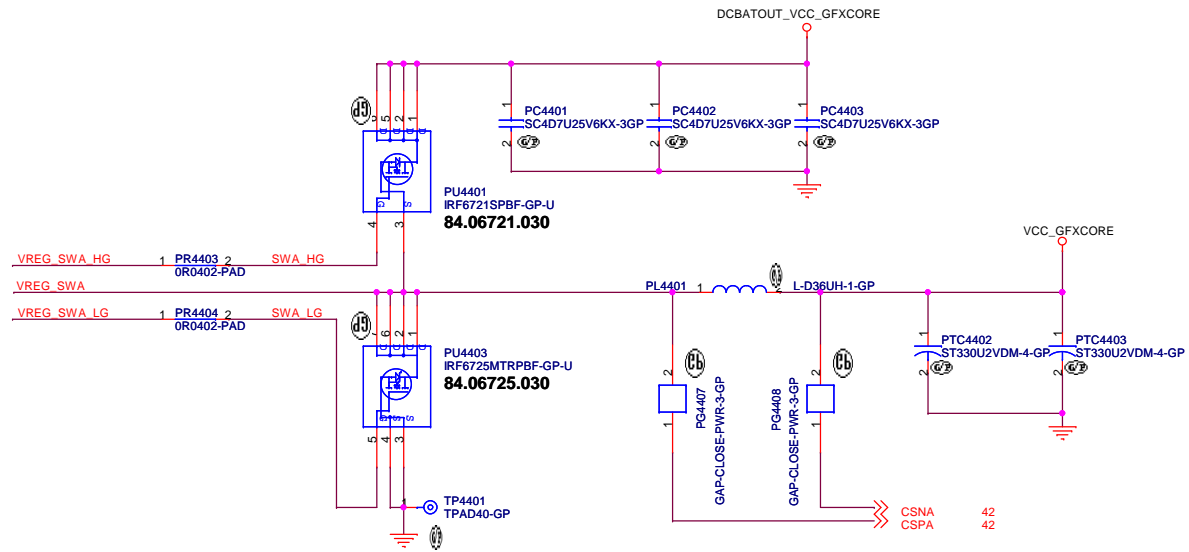
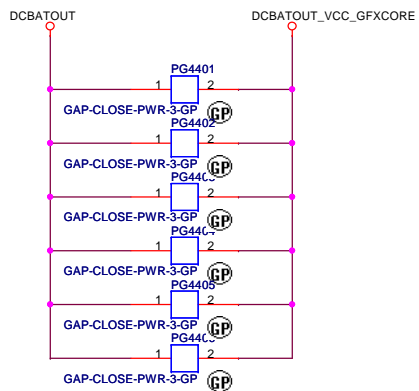
PWR_VCORE3_HG PR4309 2_VCORE3_HG
 0R0402-PAD
 PWR_VCORE3_PH
 PWR_VCORE3_LG1 PR4308 2_VCORE3_LG
 0R0402-PAD

TP4301
 TPAD40-GP
 42

CSP3 42
 CSN3

<Core Design>

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DC/DC CPU CORE2_NCP6131	
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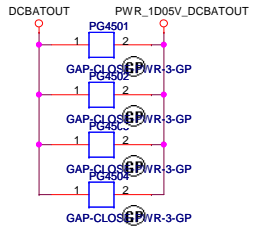
<Core Design>

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

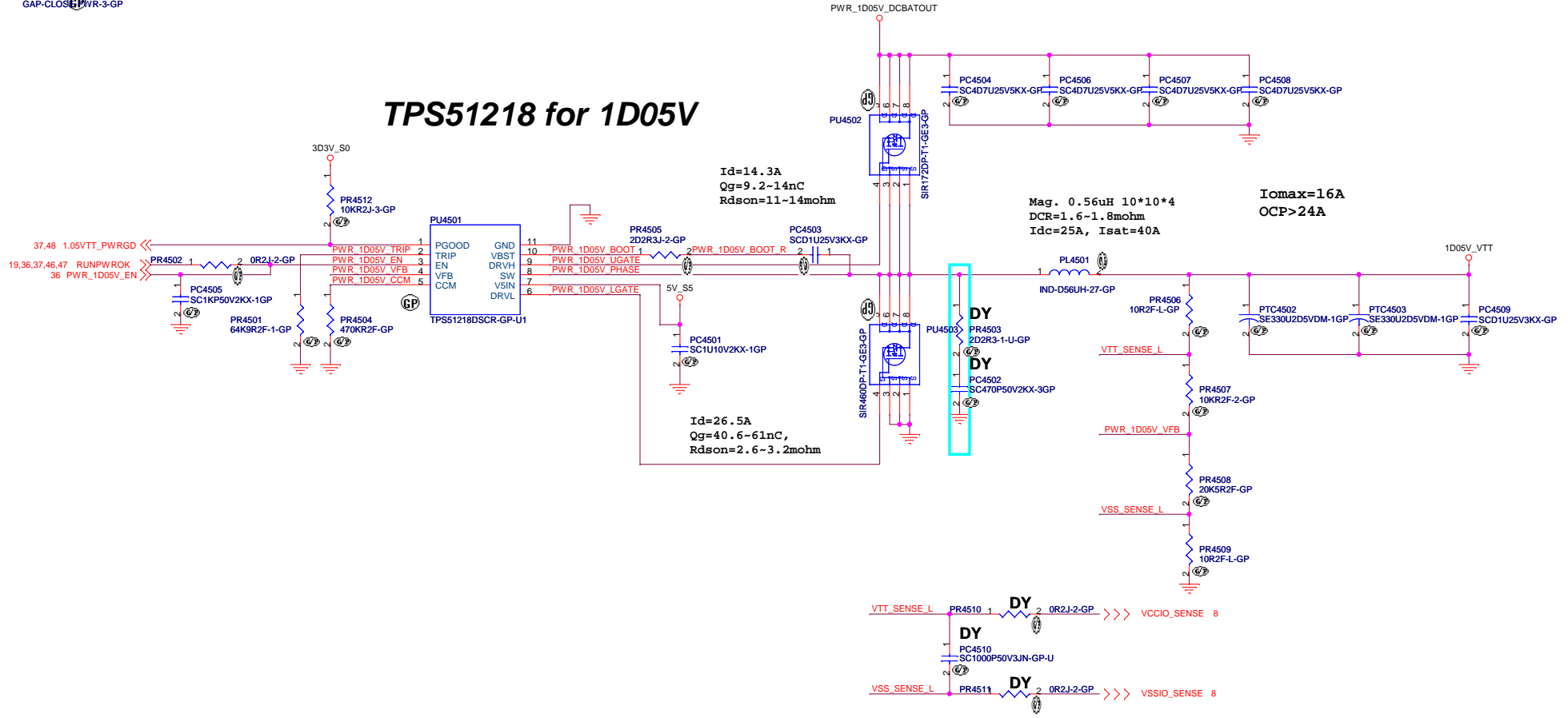
Title **DC/DC CPU CORE3_NCP6131**

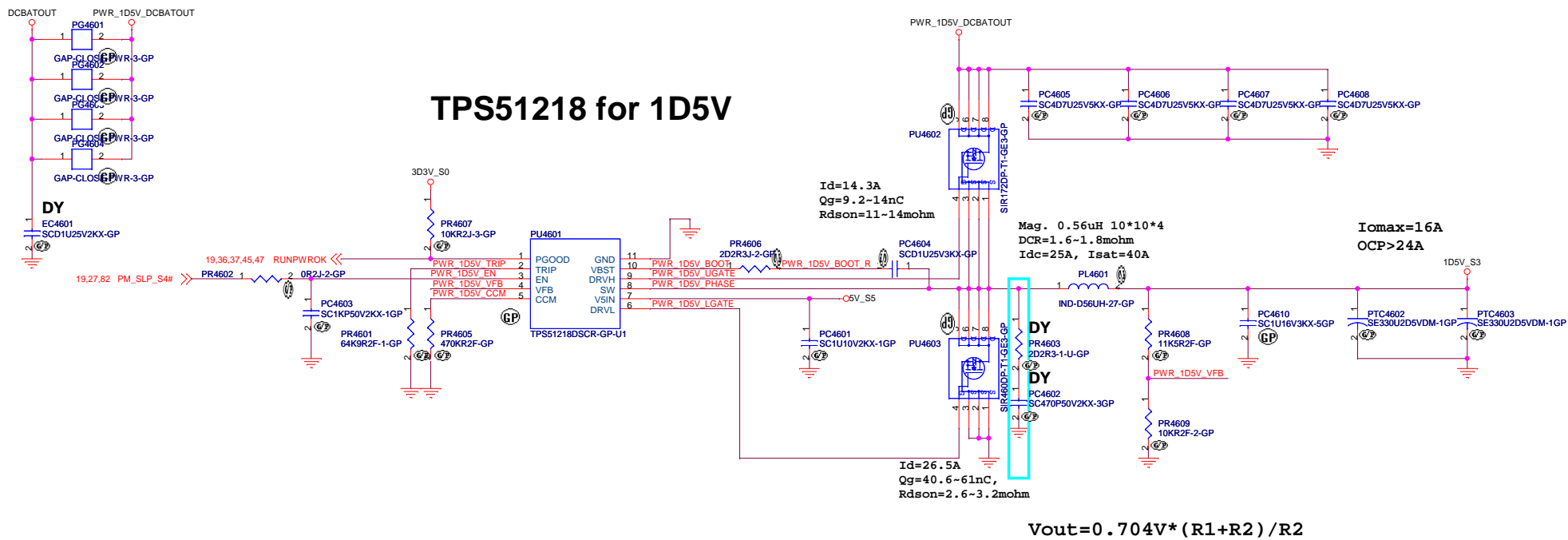
Size Document Number **LLW-1 / LGG-1** Rev **SB**

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TPS51218 for 1D05V

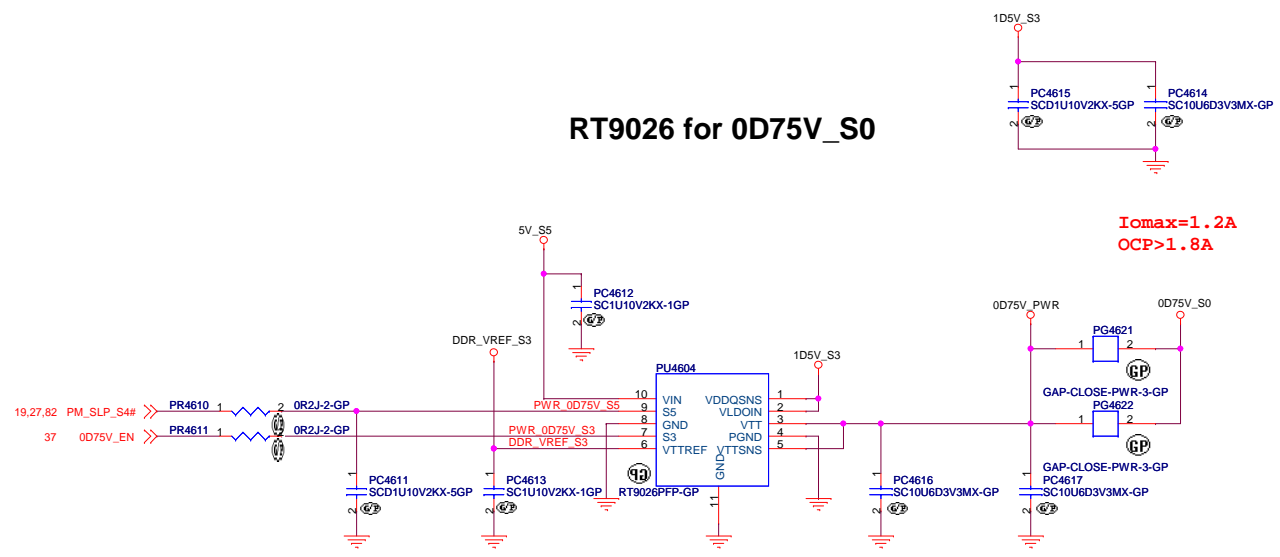




TPS51218 for 1D5V

$$V_{out} = 0.704V \cdot (R1 + R2) / R2$$

RT9026 for 0D75V_S0

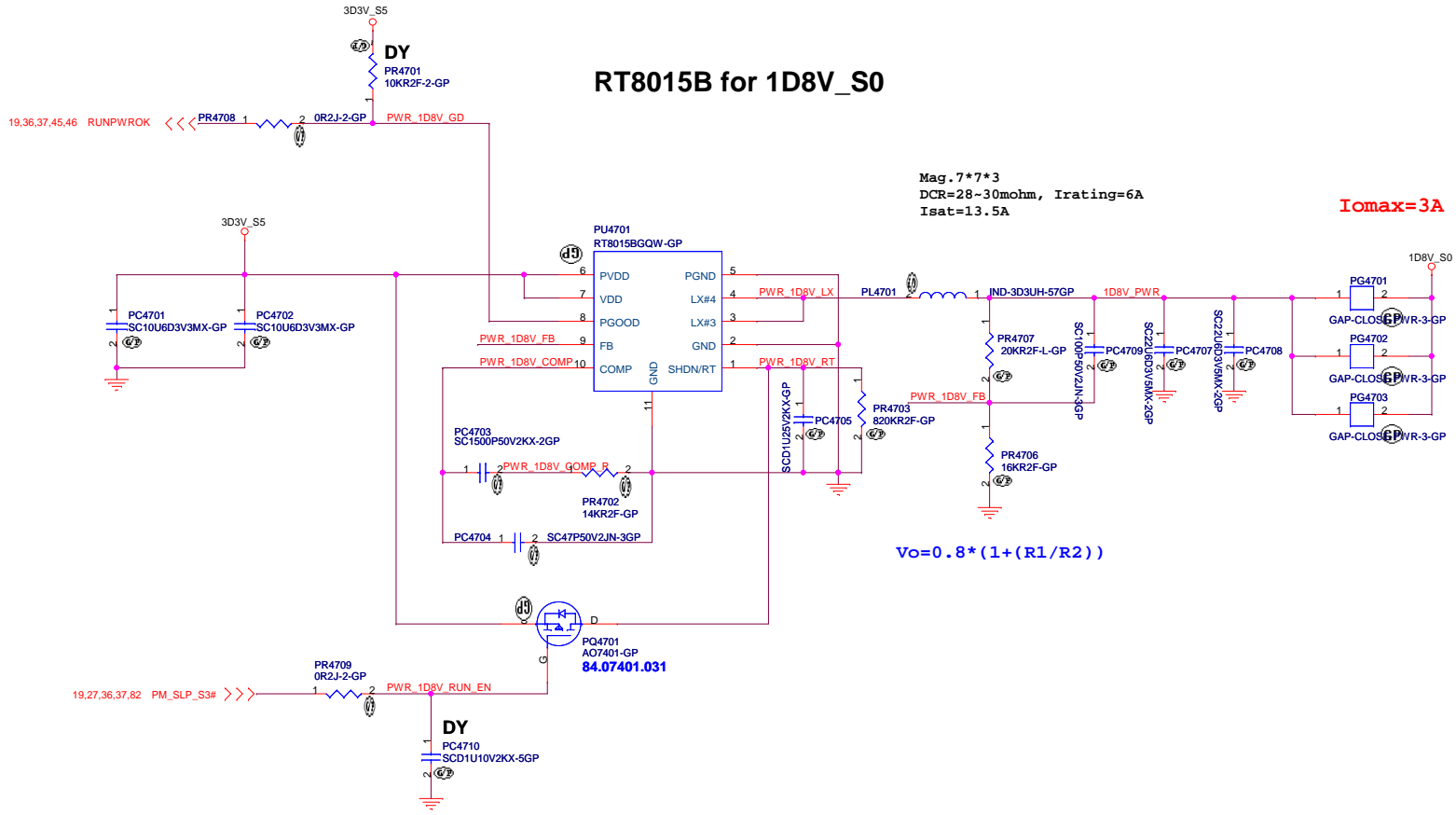


Iomax=1.2A
OCP>1.8A

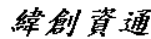
<Core Design>

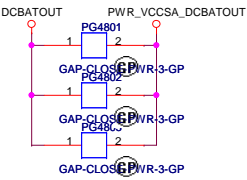
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
TPS51128 1D5V & RT9026 0D75V	
Size	Document Number
LLW-1 / LGG-1	
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RT8015B for 1D8V_S0

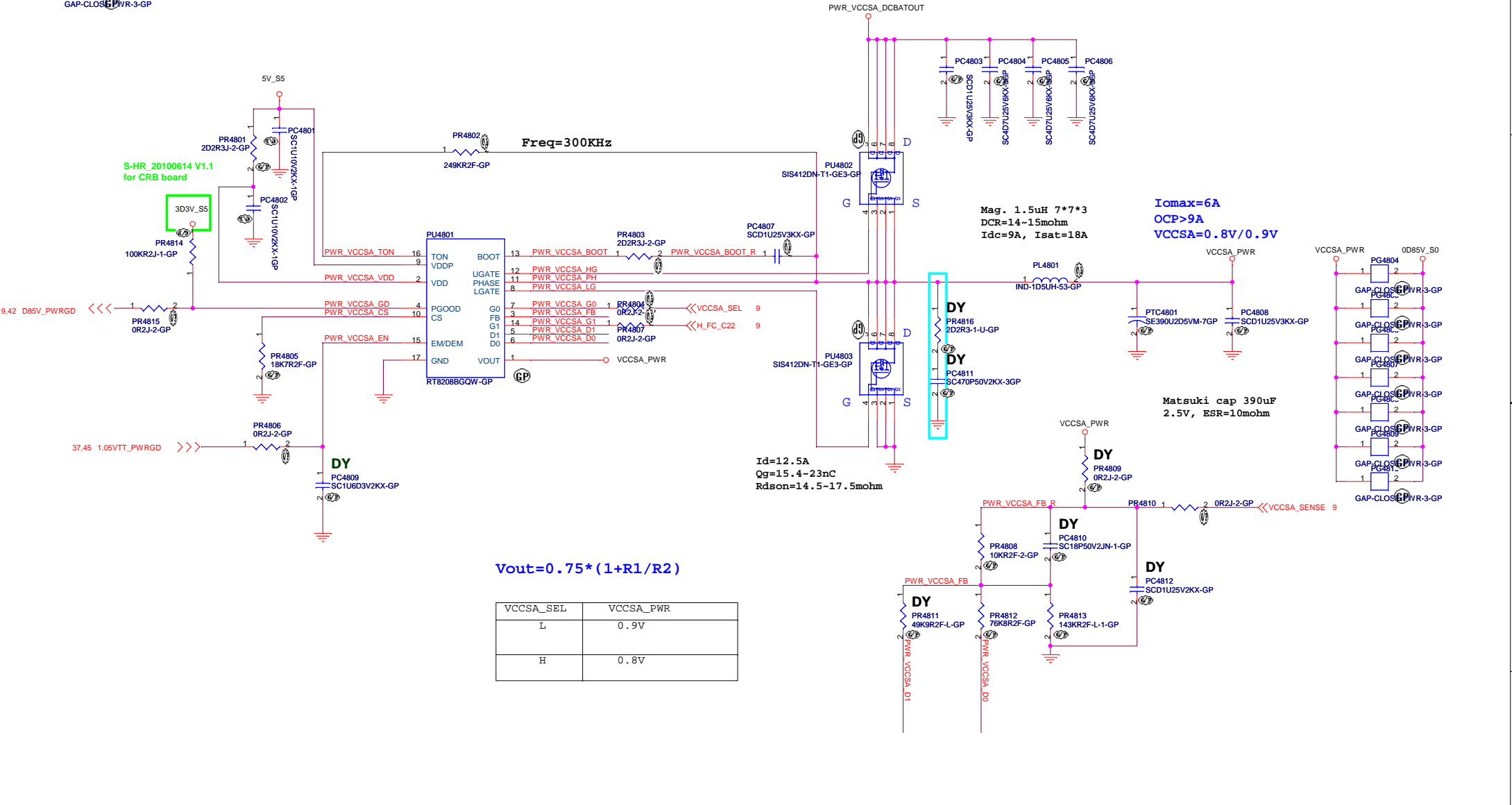


<Core Design>

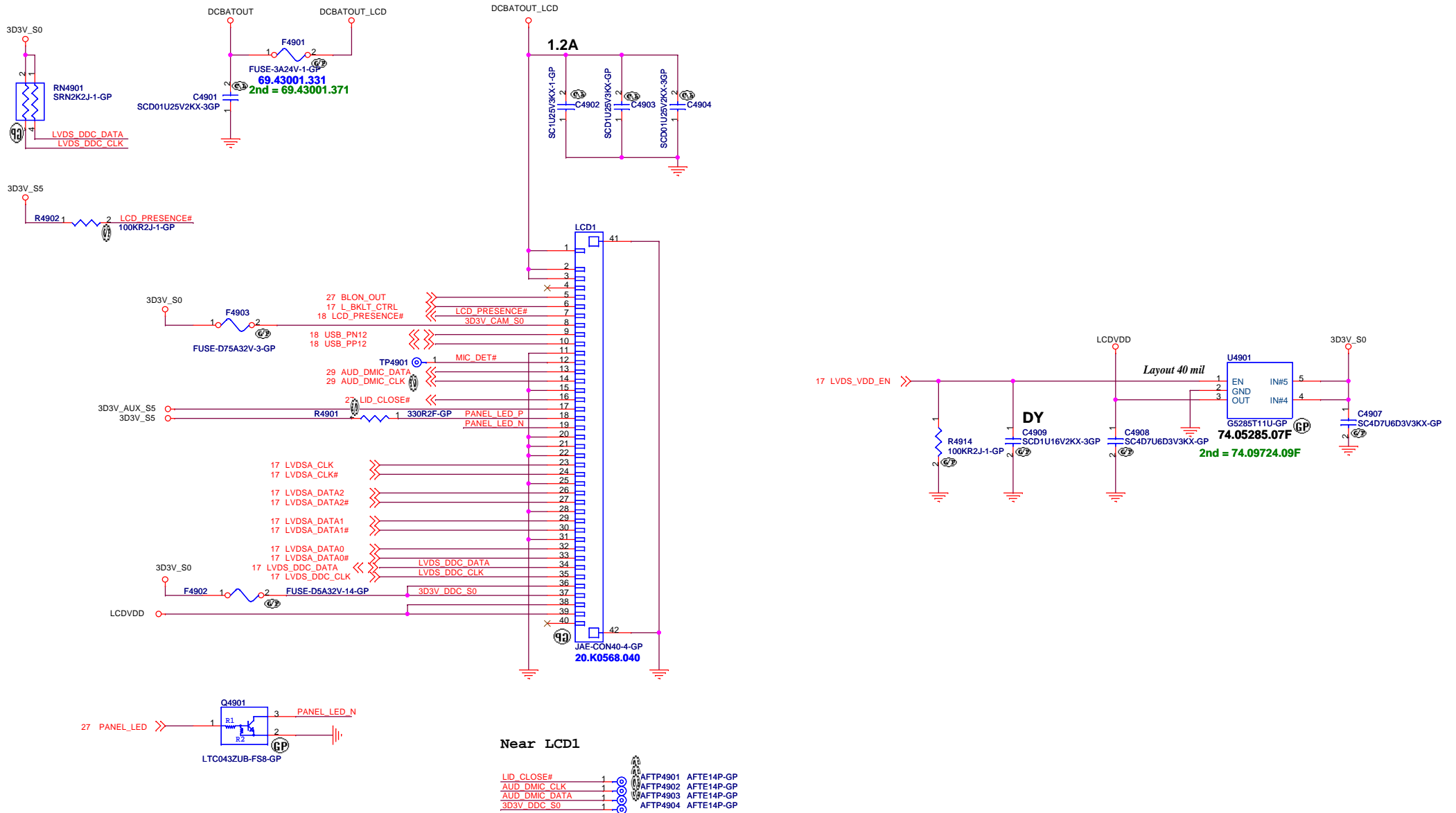
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PWM_1D8V_RT8015B	
Size Document Number	LLW-1 / LGG-1
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RT8208A for VCCSA



LCD / Inverter Connector

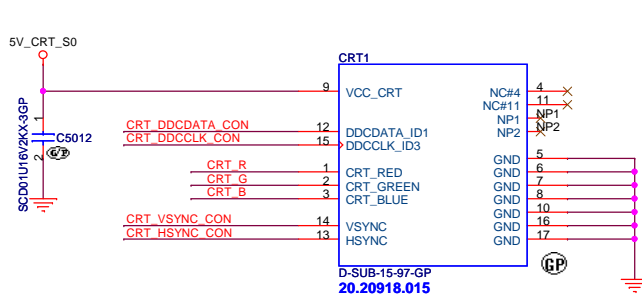


<Core Design>

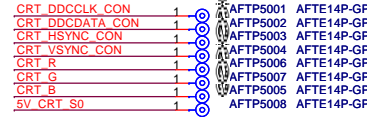
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title LCD CONNECTOR		
Size A3	Document Number LLW-1 / LGG-1	Rev SB
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CRT CONNECTOR

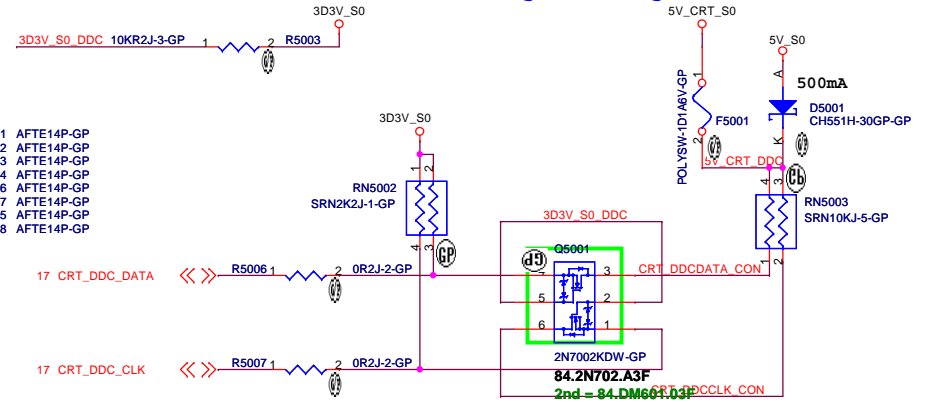


Near CRT1

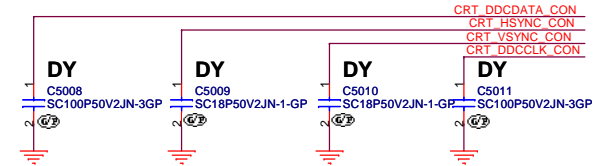
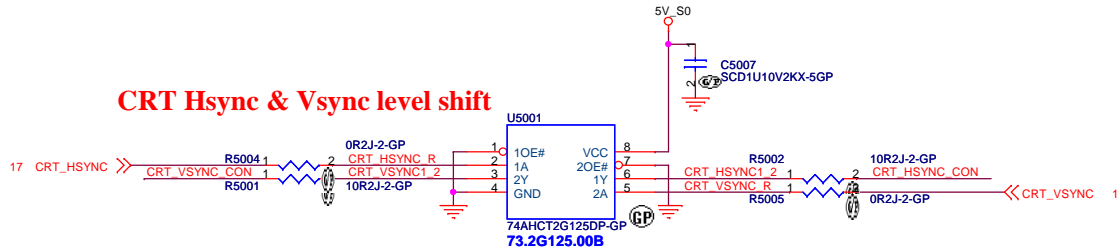


CRT DDCDATA & DDCCLK level shift

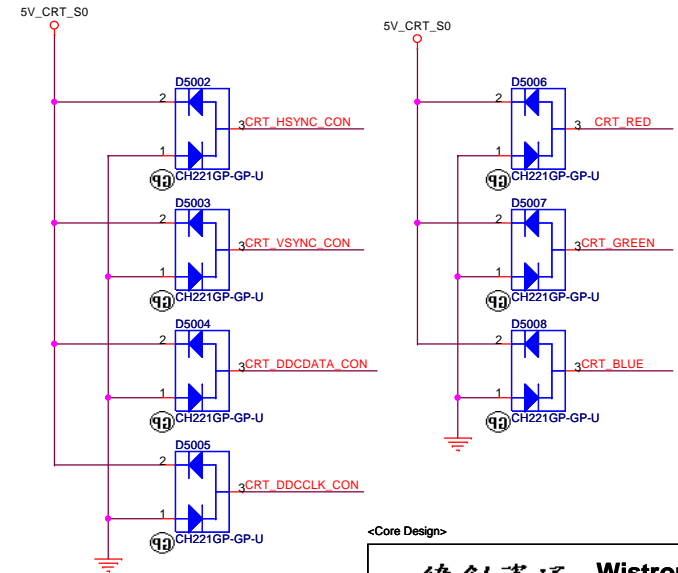
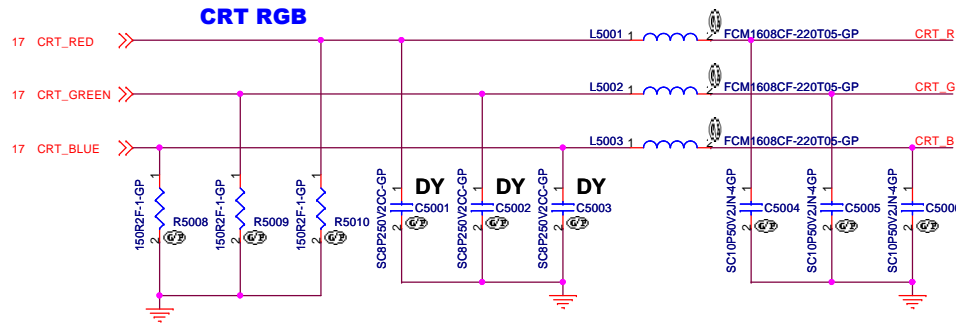
Full High 5V Design on CRT Board



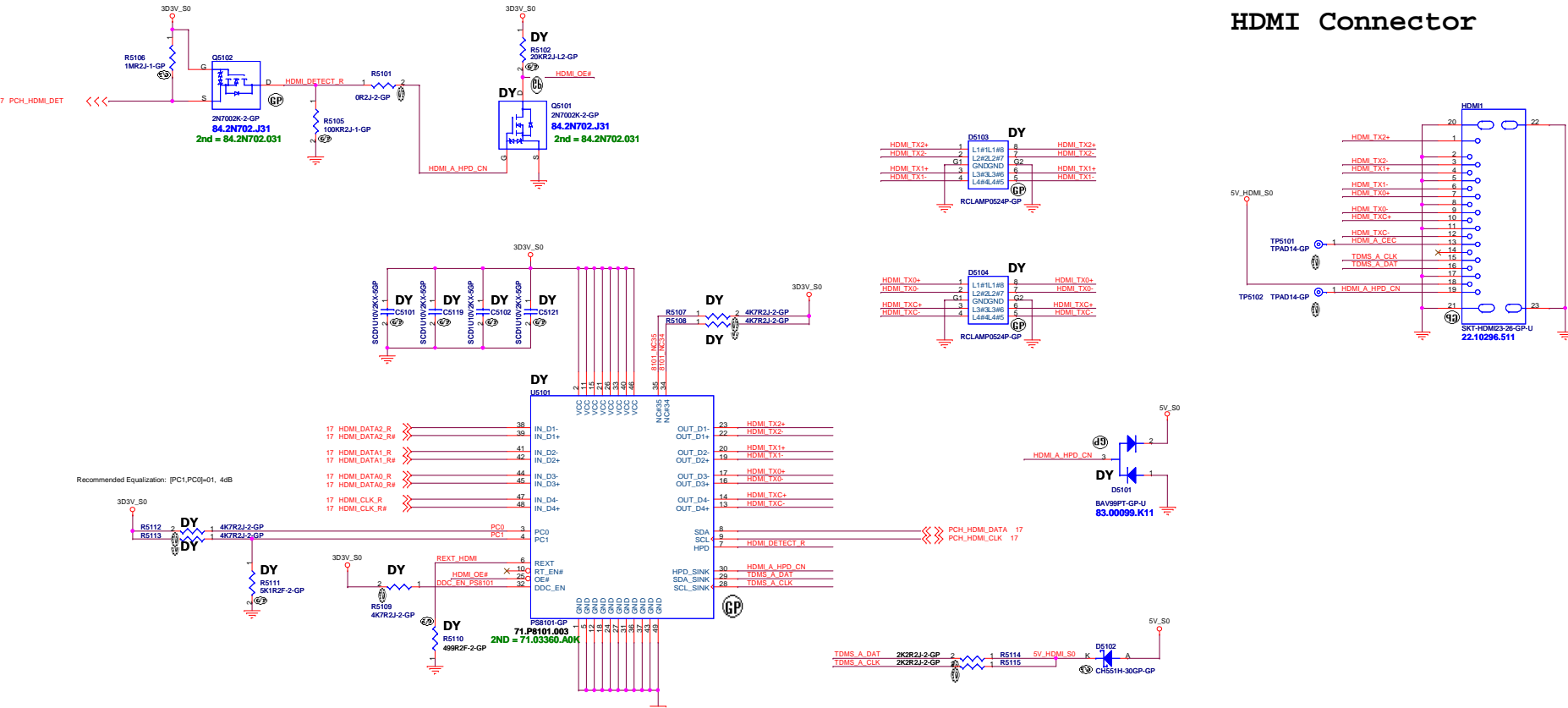
CRT Hsync & Vsync level shift



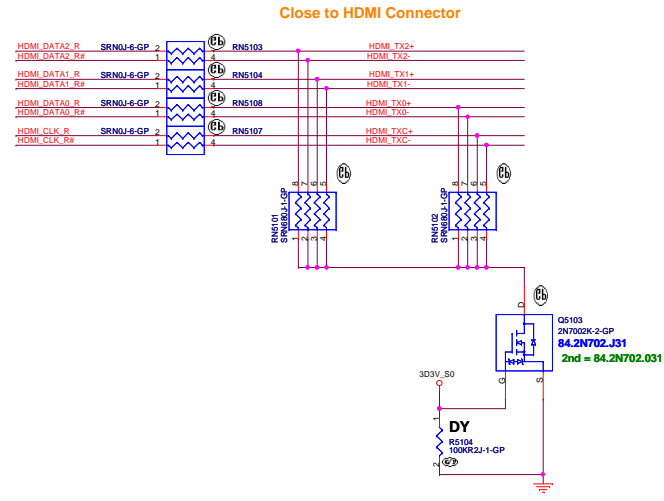
CRT RGB



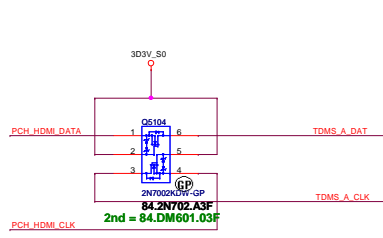
HDMI Connector



HDMI Passive Level Shifter



HDMI DDC Passive Level Shifter



BLANK

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DISPLAY PORT CONNECTOR

Size
A4

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D

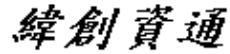
C

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BLANK

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title BLANK	
Size A4	Document Number LLW-1 / LGG-1	Rev SB	
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D

C

B

A

BLANK

<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		BLANK	
Size A4	Document Number	LLW-1 / LGG-1	Rev SB
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A

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

FAN CONTROL

Size
A4

Document Number

LLW-1 / LGG-1

Rev
SB

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A

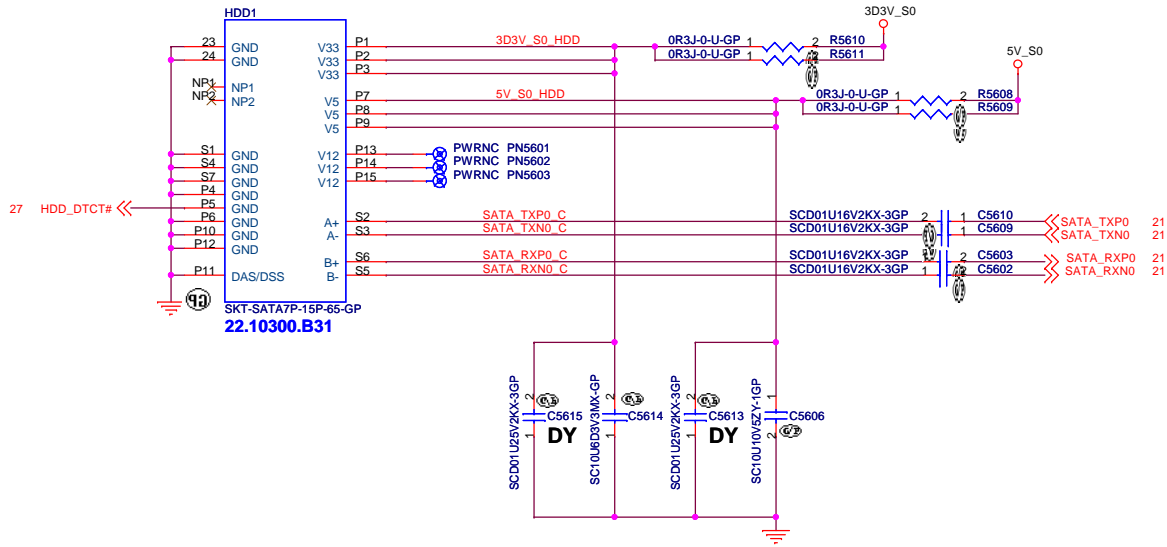
B

C

D

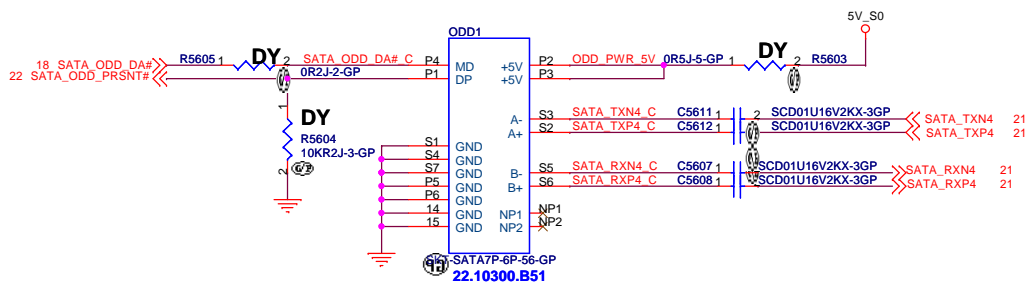
E

HDD Connector

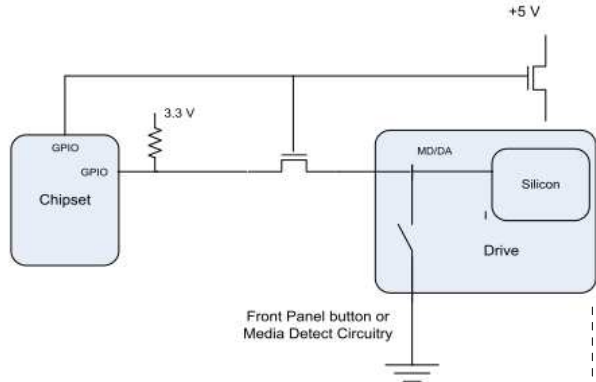
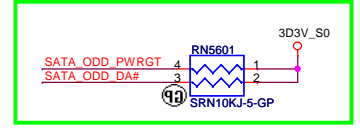


ODD Connector

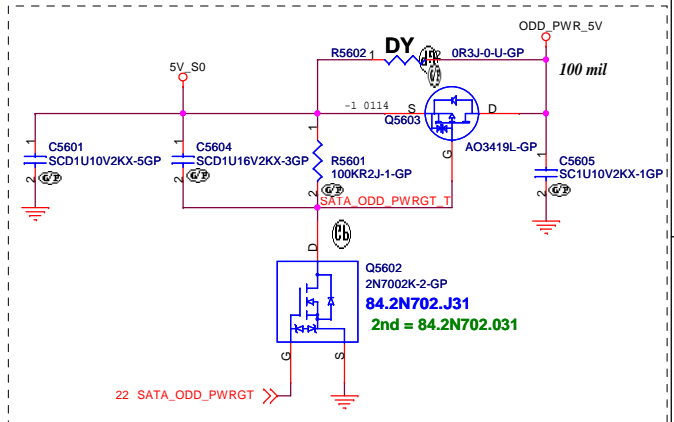
SATA_RX- and SATA_RX+ Trace Length match within 20 mil
 Mars:
 Exchange ODD and ESATA differential pair each other.



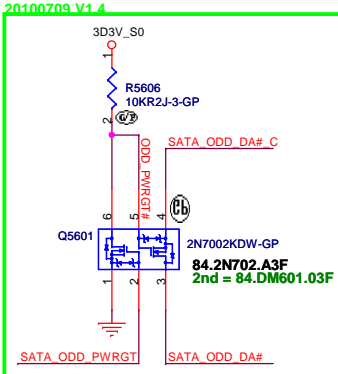
When the drive is powered on, the FET to the MD/DA pin drive is OFF.
 When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD



SUPPORT ZERO SATA ODD



0707 Modify:
 Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCB and ODD.

ESATA Connector

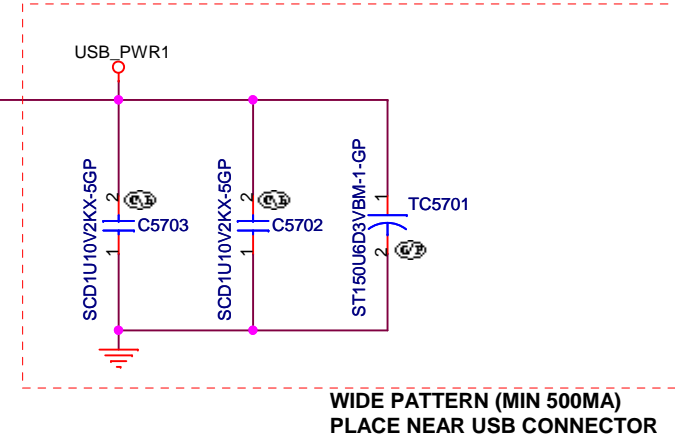
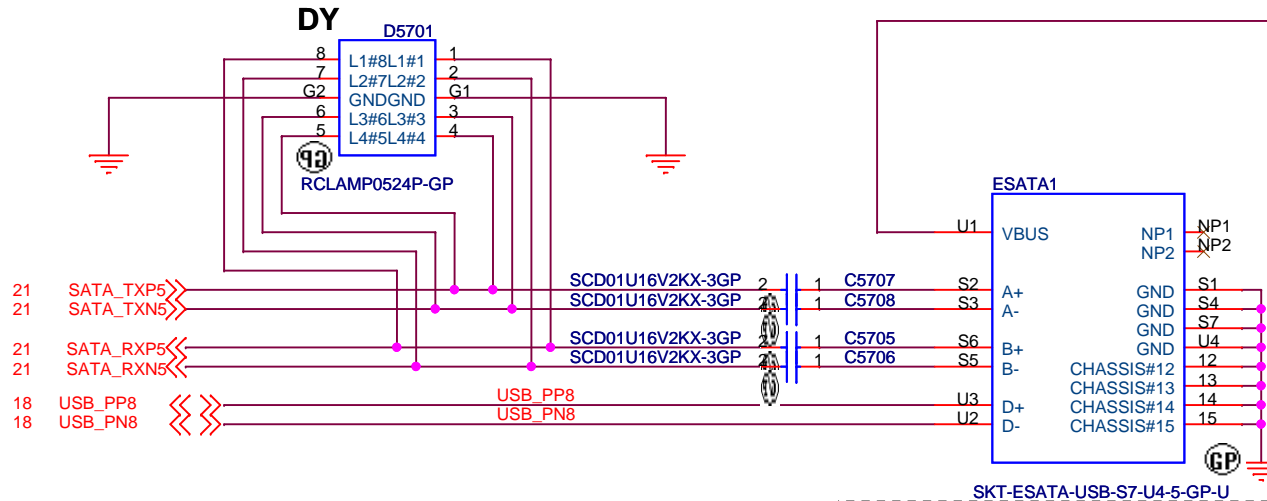


Table 57.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2065DGN4	54Y9024BA	74.02065.079
ROHM	BD8012FVJ	54Y9024AA	74.08012.07G

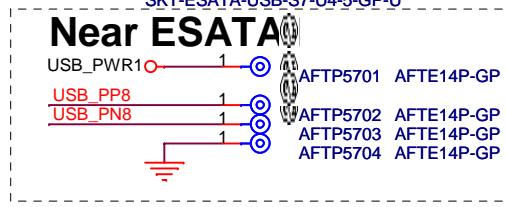
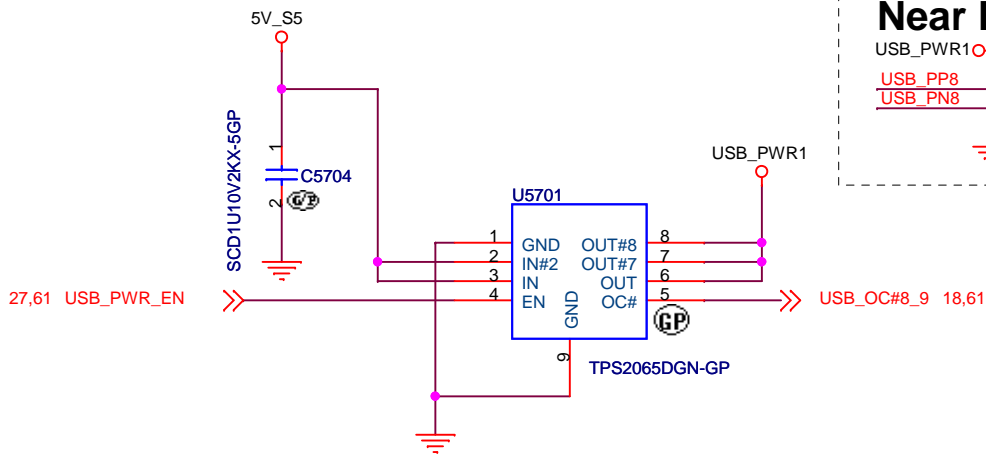
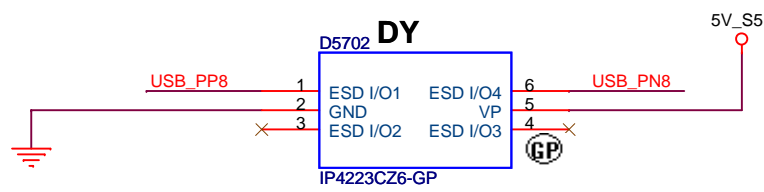


Table 57.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L



<Core Design>

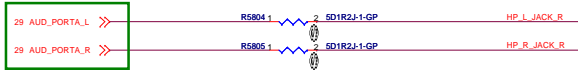
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

ESATA CONNECTOR

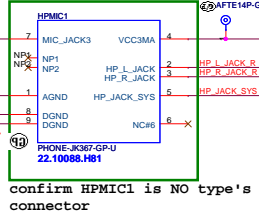
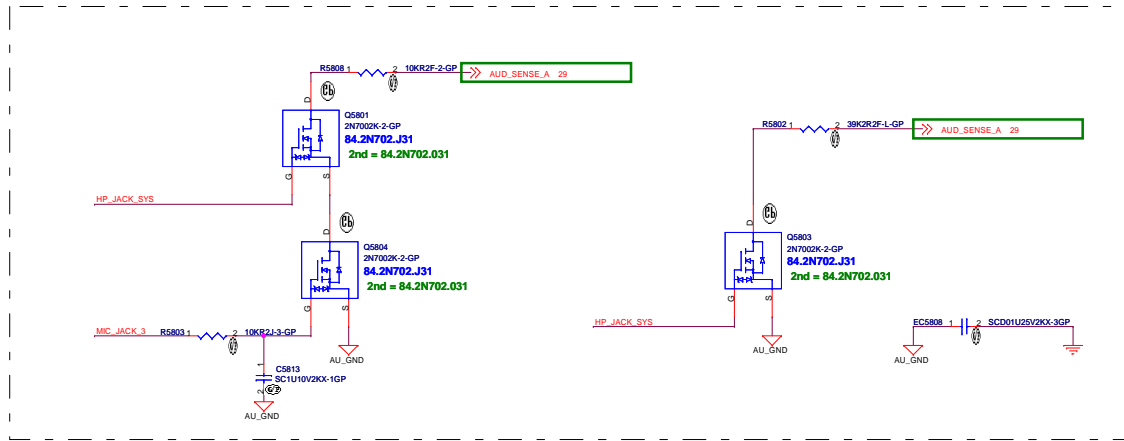
Size A4	Document Number LLW-1 / LGG-1	Rev SB
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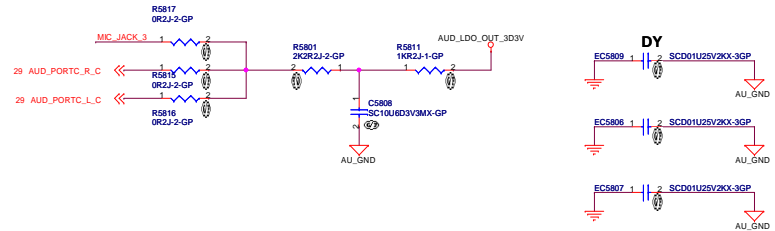
NEAR HEADPHONE CONN



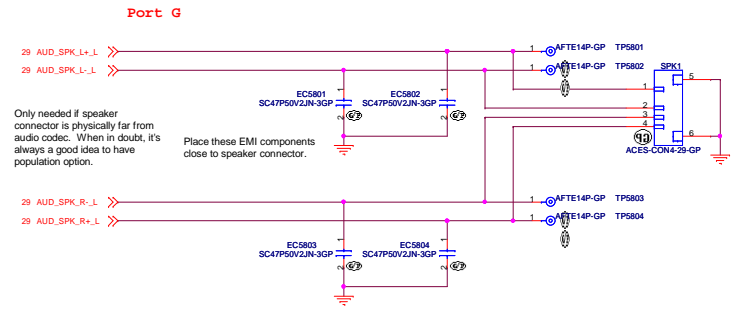
JACK SENSE



confirm HPMIC1 is NO type's connector



INTERNAL STEREO SPEAKERS



Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.

Place these EMI components close to speaker connector.

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<Core Design>			
緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
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Size A3	Document Number	LLW-1 / LGG-1	Rev SB
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SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

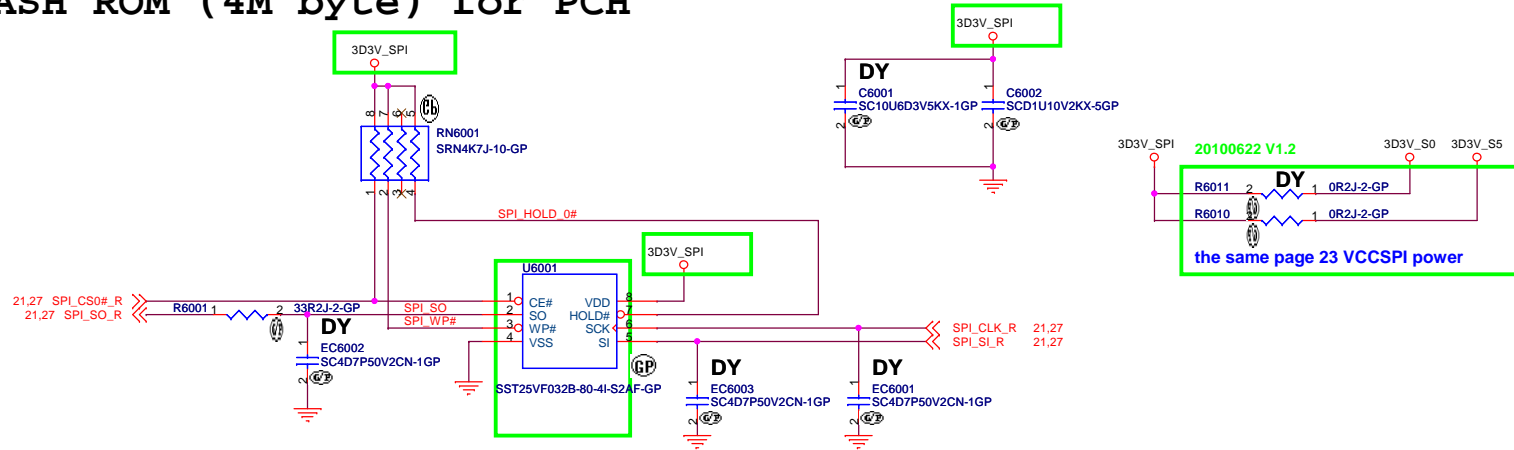


Table 60.1 - SPI Serial Flash Memory multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
SST	SST25VF032B-80-4I-S2A	N/A	72.25032.D01
MXIC	MX25L3206EM2I-12G	N/A	72.25320.C01
WINBOND	W25Q32BVSSIG	N/A	72.25Q32.A01
NUMONYX	M25PX32-VMW6F	N/A	72.25P32.C01

SSID = RBATT

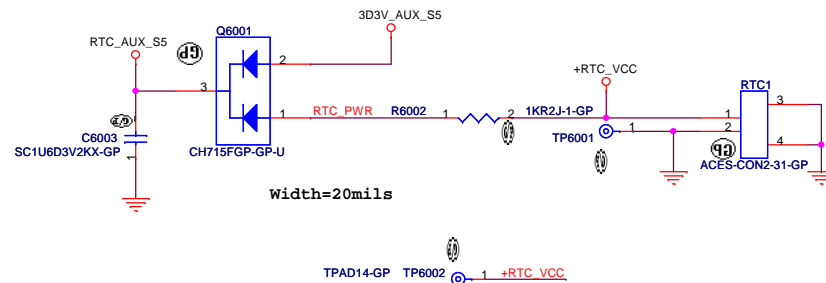


Table 60.2 - Schottky Barrier Diode multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHEMINKO	CH715FGP	N/A	83.R0304.D81
CHEMINKO	BAS40CWGP	N/A	83.00040.R81
PANJIT	BAS40CW	N/A	83.00040.E81

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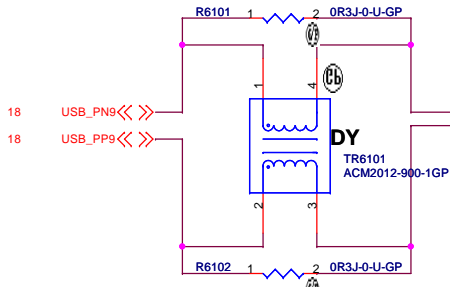
Title: **Flash/RTC**

Size A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

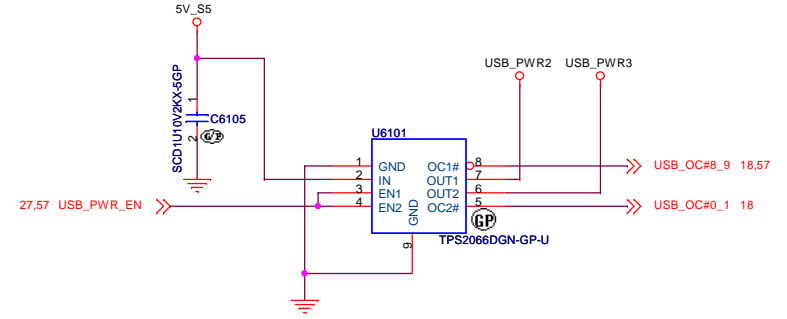
Date: Tuesday, November 09, 2010 Sheet 60 of 94

USB Connector

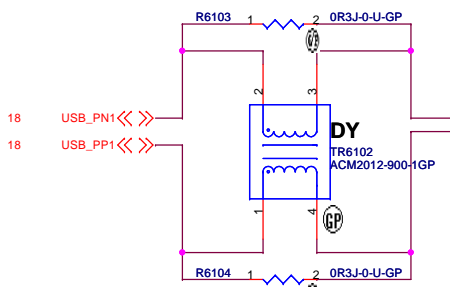
WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR



Left Rear USB Connector



WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR



Left Front USB Connector

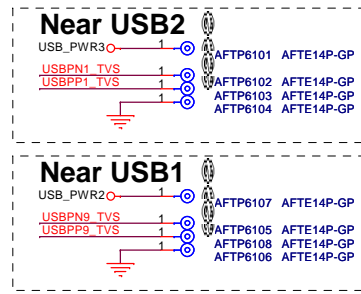
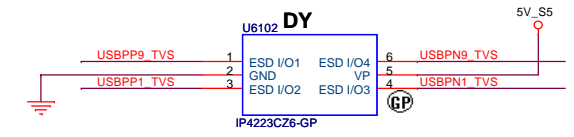
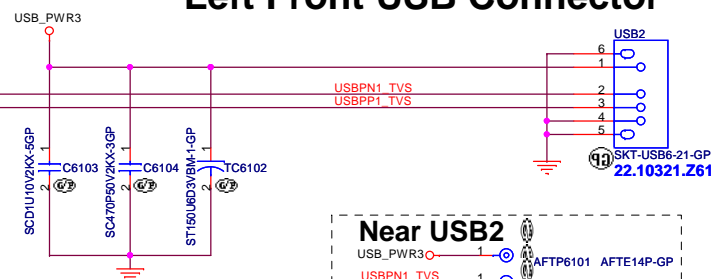


Table 61.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2066DGN	41R0511AA	74.02066.A71
TI	TPS2066DGN-1	N/A	74.02066.B71

Table 61.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

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Title: **USB Connector**

Size A3 Document Number: **LLW-1 / LGG-1** Rev: **SB**

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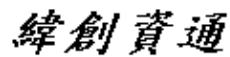
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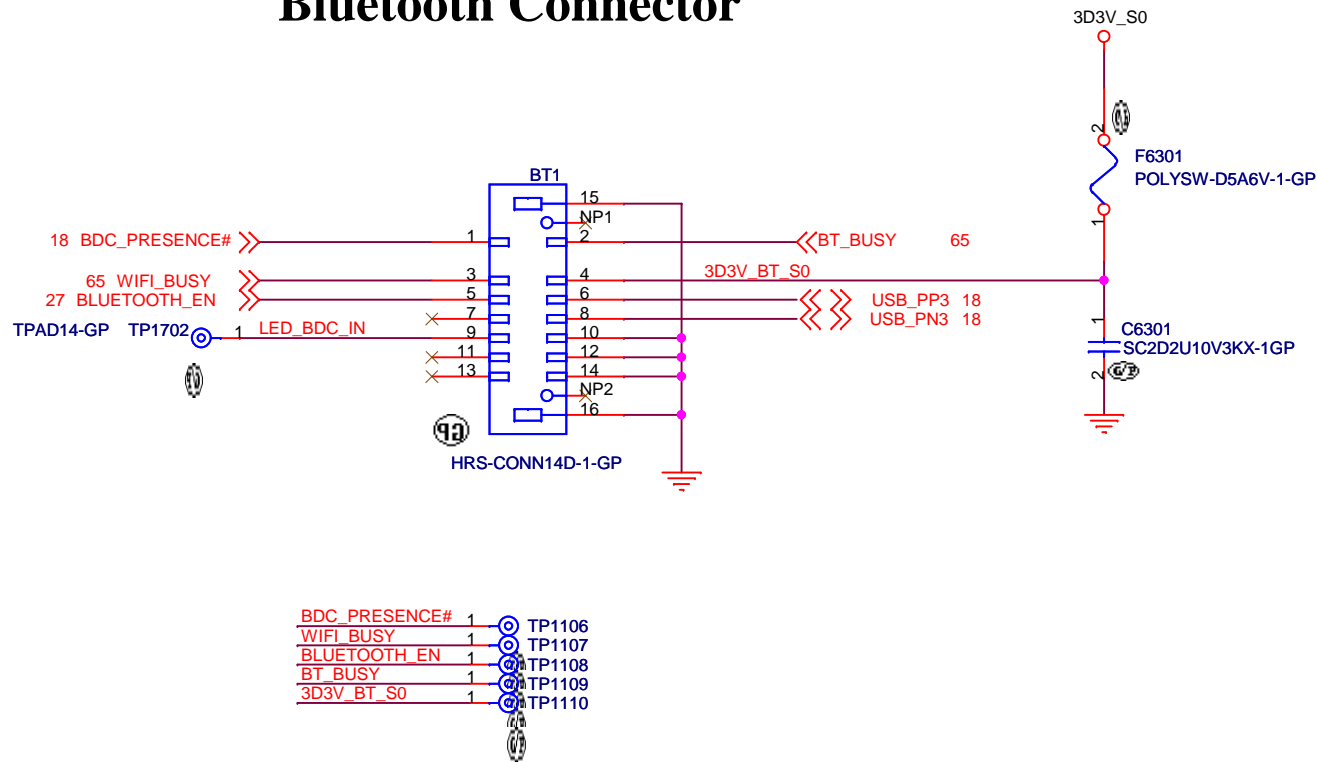
A

BLANK

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		BLANK	
Size A4	Document Number	LLW-1 / LGG-1	Rev SB
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Bluetooth Connector



<Core Design>

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Title **Bluetooth**

Size A4	Document Number LLW-1 / LGG-1	Rev SB
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BLANK

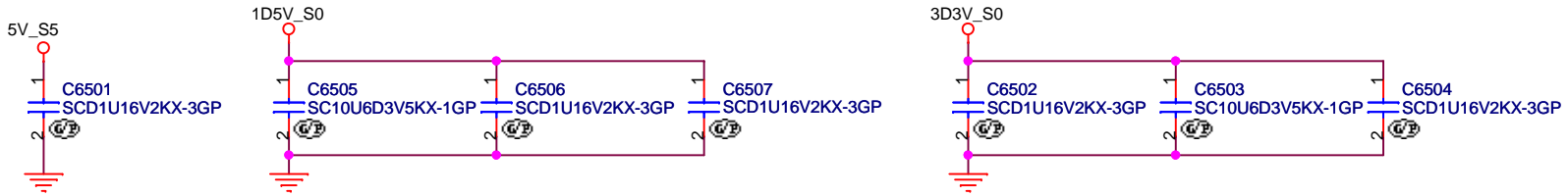
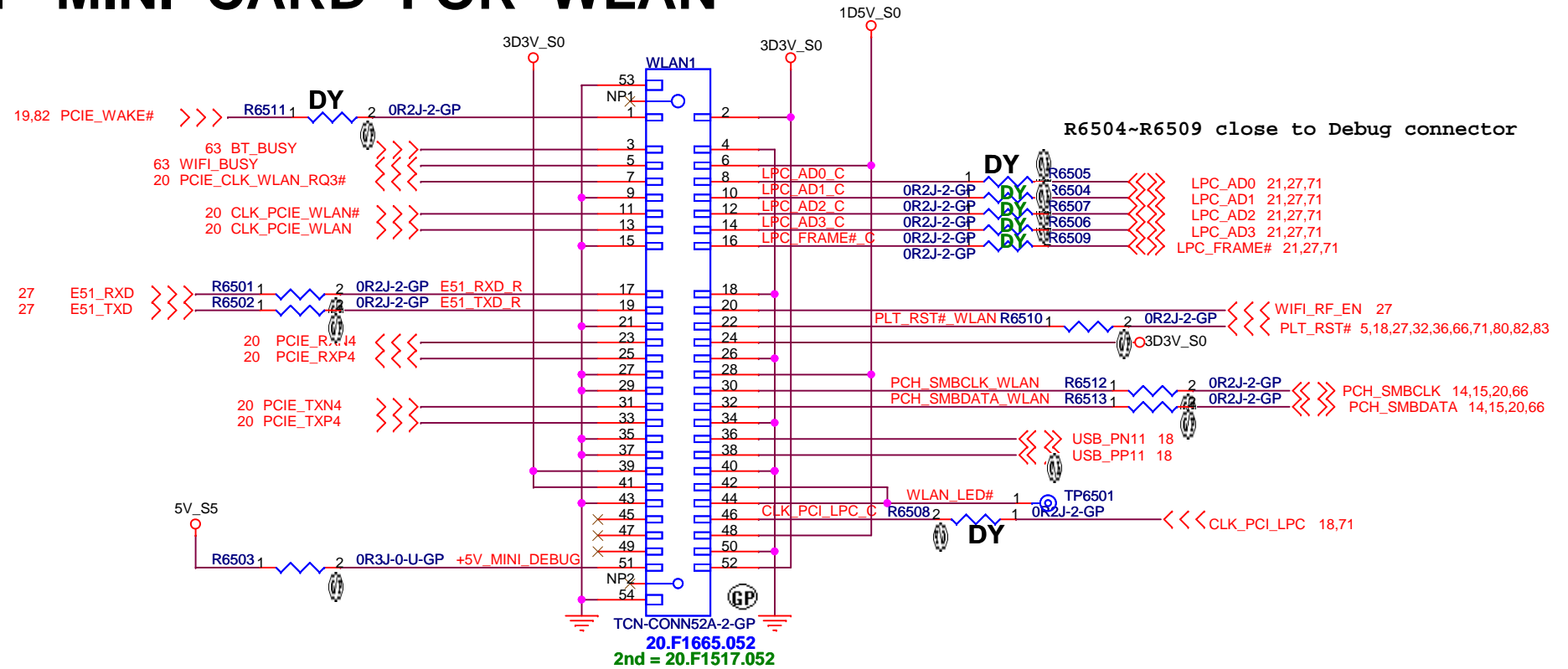
<Core Design>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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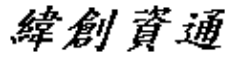
Title		
FingerPrint		

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

HALF MINI CARD FOR WLAN

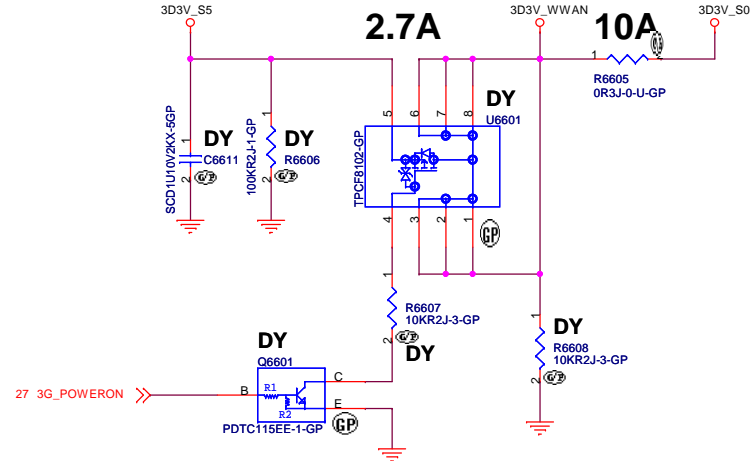
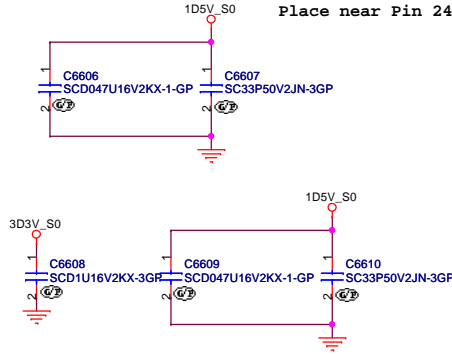
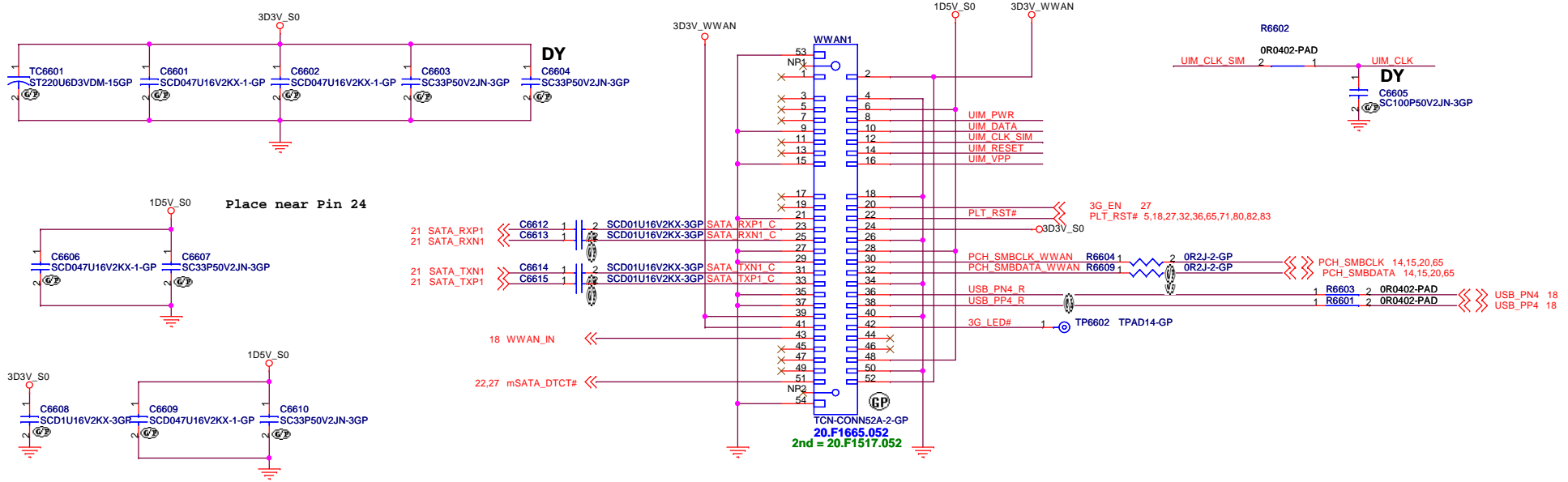


<Core Design>

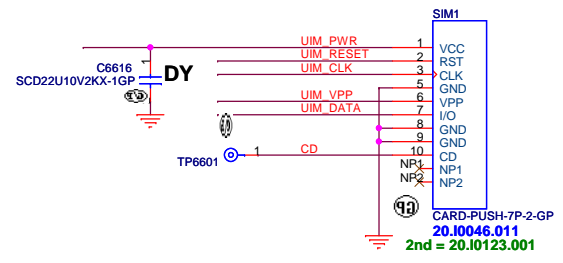
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
MINI CARD SLOT 1		
Size A4	Document Number LLW-1 / LGG-1	Rev SB
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Mini Card Connector(WWAN)

Place near MINI Card CONN



SIM Connector



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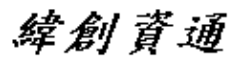
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BLANK			
Size	Document Number		Rev
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		BLANK	
Size A4	Document Number	LLW-1 / LGG-1	Rev SB
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Touch Pad Connector

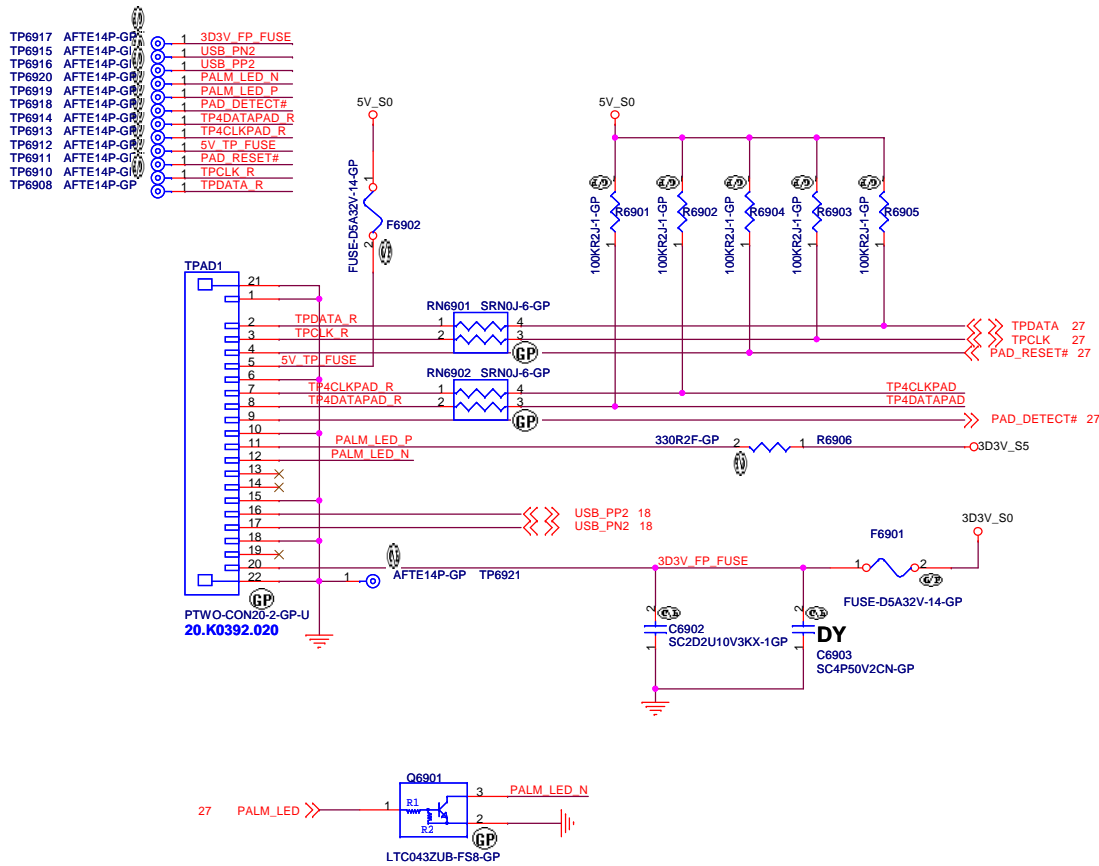
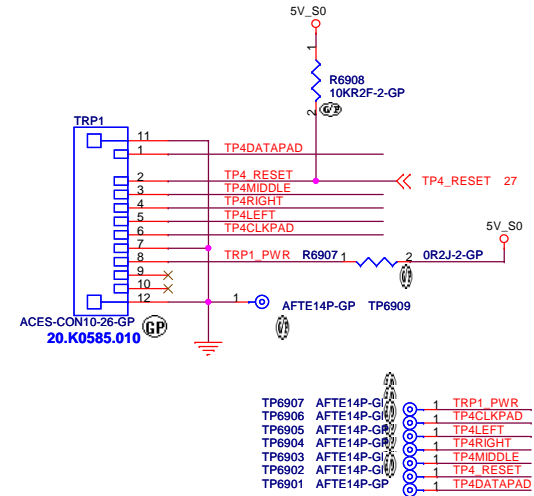


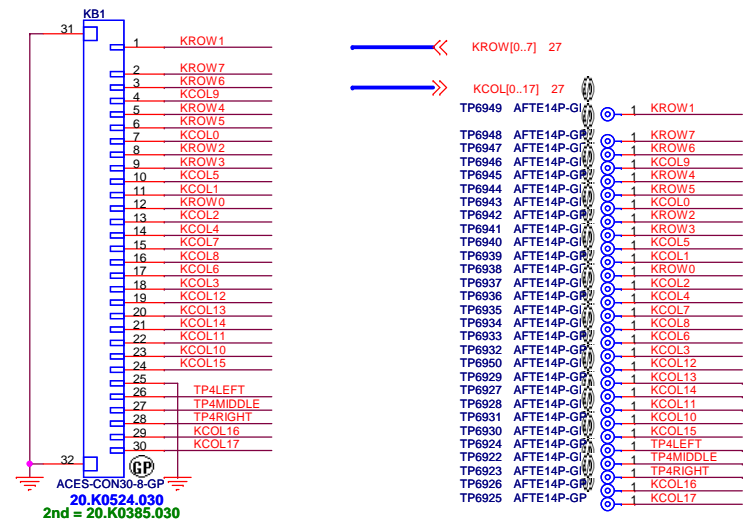
Table 69.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC143ZU	N/A	84.00143.E1K
ON	DTA114EET1G	N/A	84.DT114.B11
ROHM	LTC043ZUB	N/A	84.00043.011
Panasonic	DRC5143Z0L	N/A	84.05143.011

Track Point Connector



KeyBoard Connector



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TOUCH PAD CONNECTOR		
Title	Document Number	Rev
Size A3	LLW-1 / LGG-1	SB
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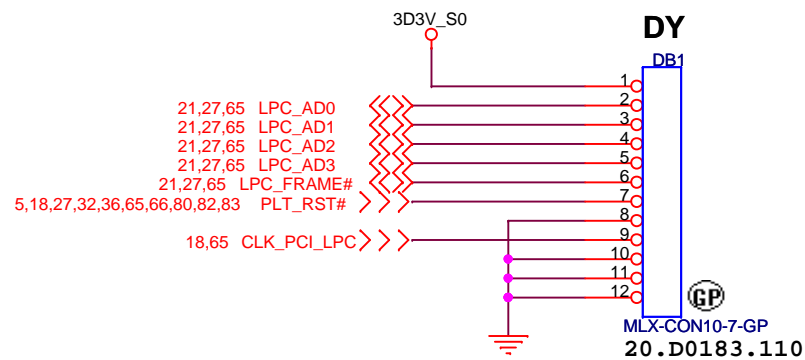
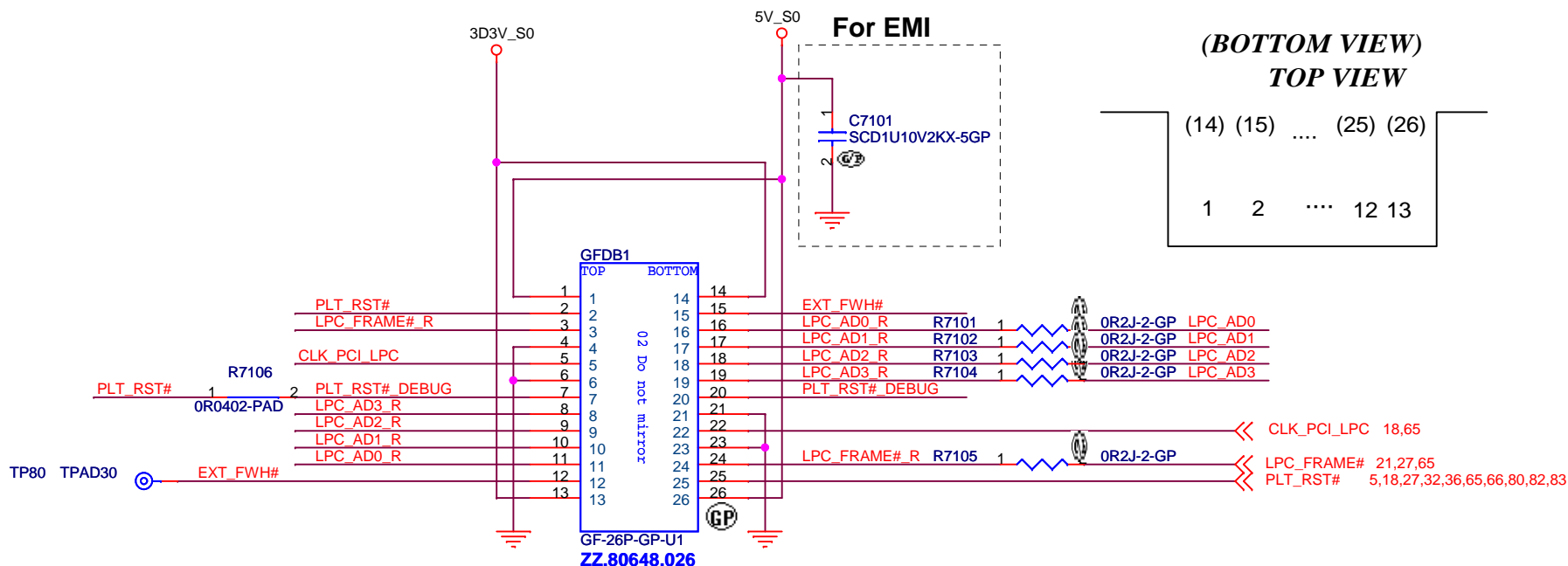
A

BLANK

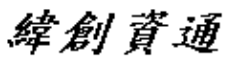
<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Size A4	Document Number	LLW-1 / LGG-1	Rev SB
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Golden Finger for Debug Board



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Title		
DEBUG CONN		
Size	Document Number	Rev
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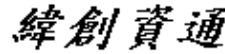
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BLANK

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BLANK			
Size	Document Number		Rev
A4	LLW-1 / LGG-1		SB
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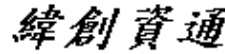
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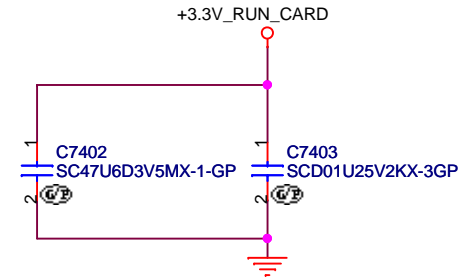
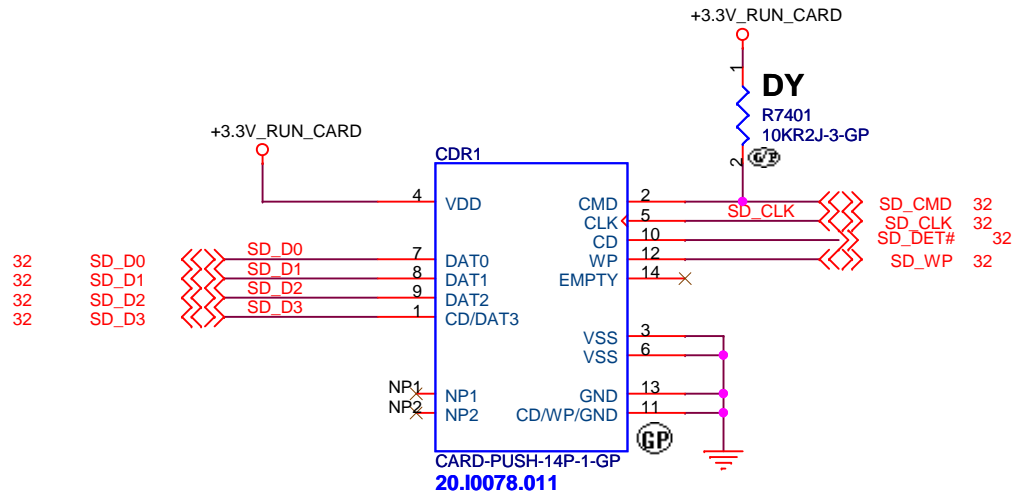
BLANK

<Core Design>

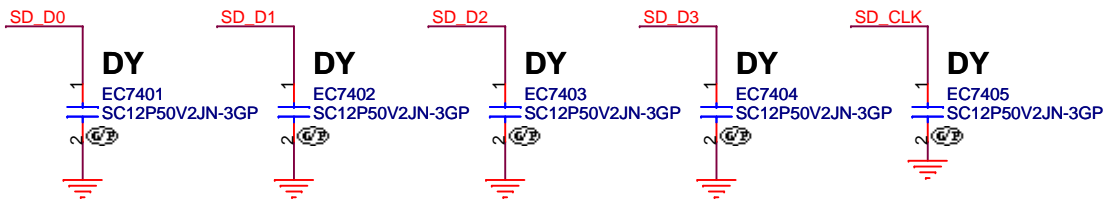
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Size	Document Number		Rev
A4	LLW-1 / LGG-1		SB
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Please apply Shield GND for SD_CLK signal between R5U220 and SD Card Slot to decrease external noise.

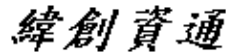
Card Reader Connector



+3.3V_RUN_CARD trace = 40mil
C7402 lose CDR1



<Core Design>

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CARD Reader CONN		
Size A4	Document Number LLW-1 / LGG-1	Rev SB
Date: Tuesday, November 09, 2010		Sheet 74 of 94

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title New Card		
Size A3	Document Number LLW-1 / LGG-1	Rev SB
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BLANK			
Size	Document Number		Rev
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<Core Design>

緯創資通

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Title

TPM

Size

Custom

Document Number

LLW-1 / LGG-1

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SB

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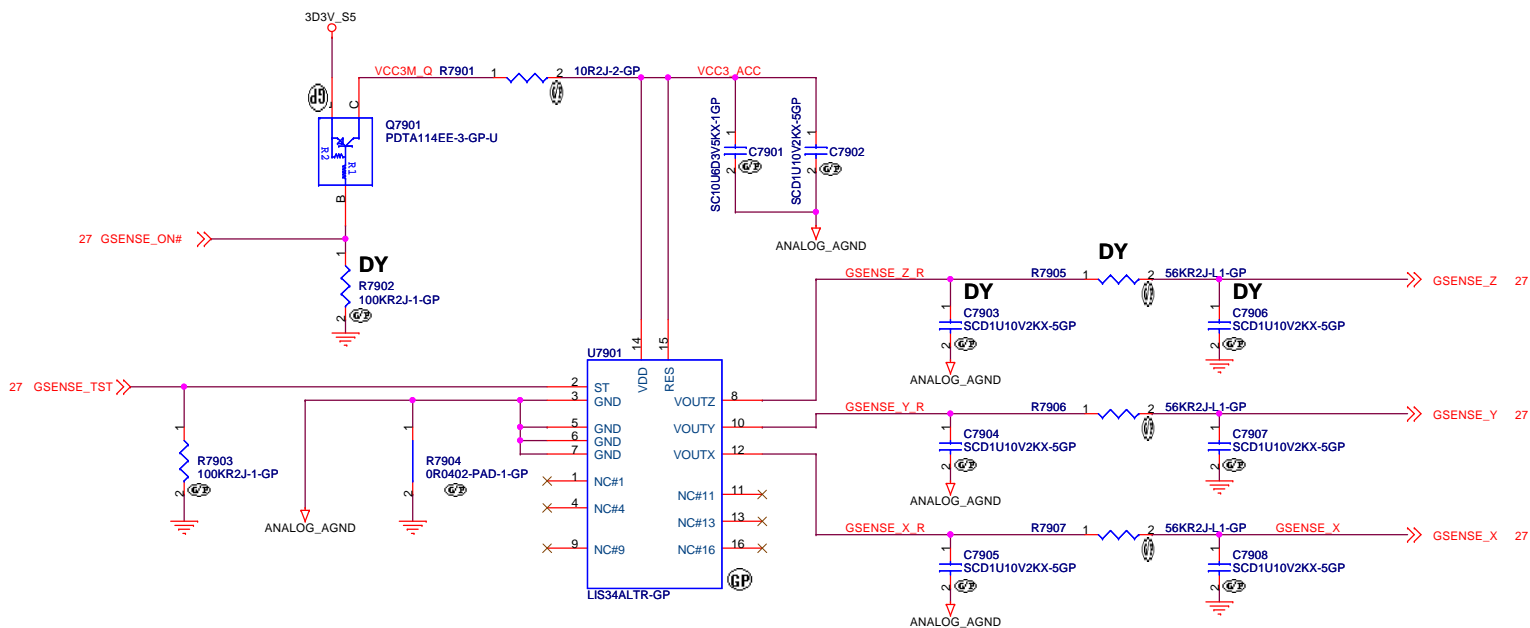
A

BLANK

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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G-Sensor



	LIS34AL	No Accel
	KXTC8-2850	
R7902	NO_ASM	ASM
R7903	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

- (1) Place C7904, C7905, Q7901, R7901, R7902, C7901, C7902, R7903, R508 close to U7901.
- (2) Avoid routing under DCDC switching area.

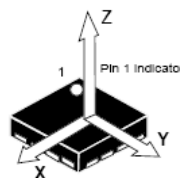


Table 79.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTA114EE	N/A	84.00114.H1K
ON	DTA114EET1G	N/A	84.DT114.B11
ROHM	LTA014EEB	N/A	84.00014.01H
Panasonic	DRA9114E0L	N/A	84.09114.A11

Table 79.2- Accelerometer multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ST	LIS34ALTR-GP	41R0828AA	74.00034.0BZ
ROHM-KIONIX	KXTC8-2850-GP	N/A	74.KXTC8.0BZ

<Core Design>

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Title		
G-Sensor		
Size	Document Number	Rev
Custom	LLW-1 / LGG-1	SB
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RFID

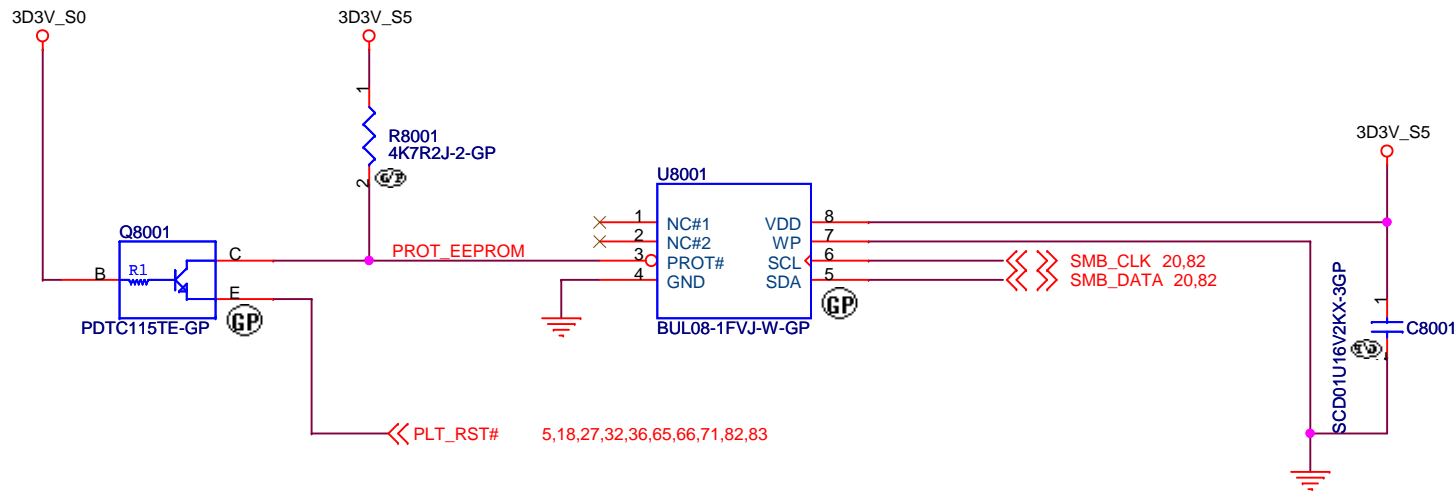


Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015EEB	N/A	84.00015.01H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-W	54Y9016AA	72.BUL08.00Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Core Design>

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RFID			
Size A4	Document Number	Rev	
	LLW-1 / LGG-1	SB	
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Title

Reserved

Size
A3

Document Number

LLW-1 / LGG-1

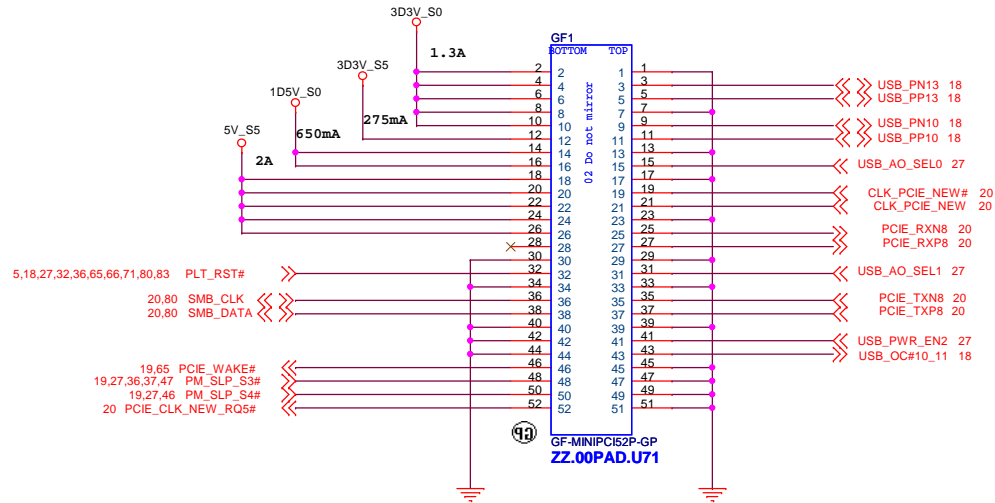
Rev

SB

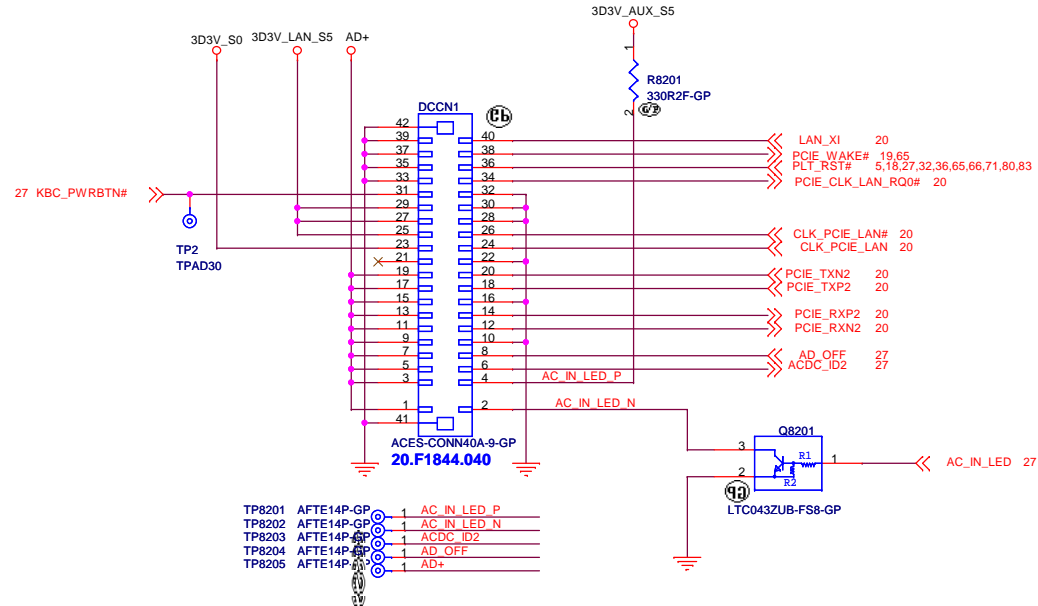
Date: Tuesday, November 09, 2010

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TO EXP BOARD CONN

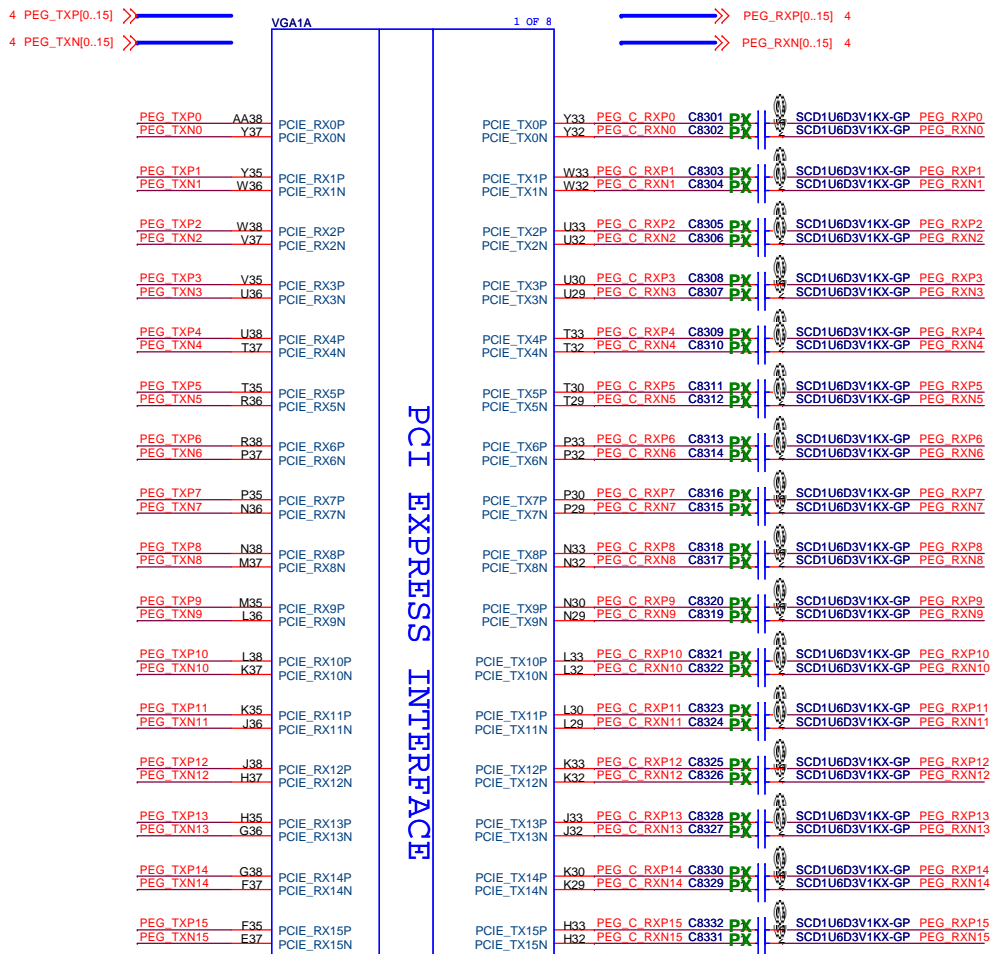


TO DC BOARD CONN



<Core Design>

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Title		
IO Board Connector		
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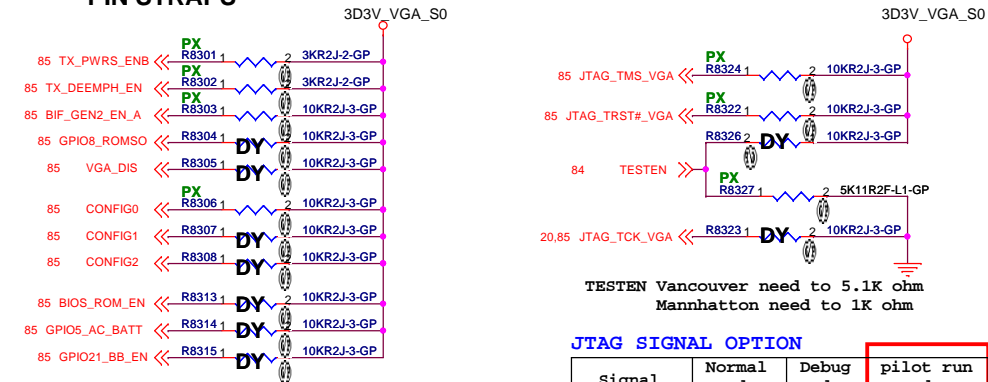


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.5GT/s capable at power on. 1: Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]: 11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS

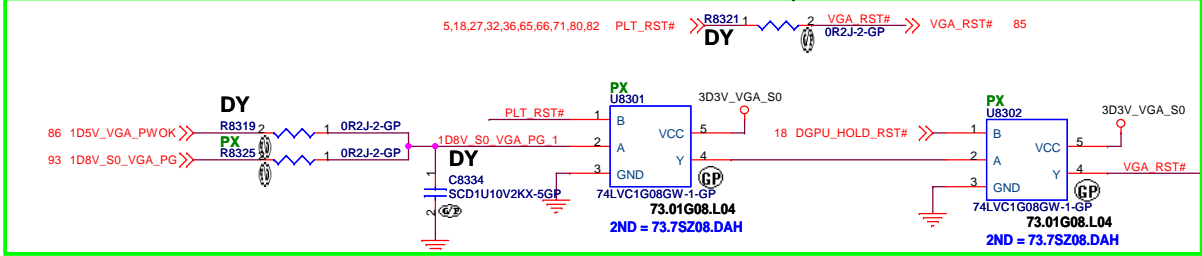


TESTEN Vancouver need to 5.1K ohm
Mannhattan need to 1K ohm

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

dGPU reset for PX/SG transitions



	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACC	H

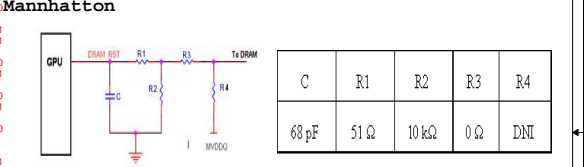
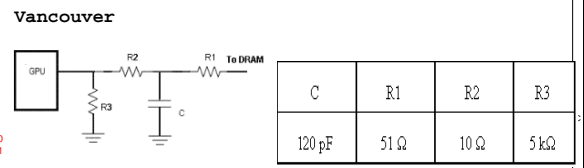
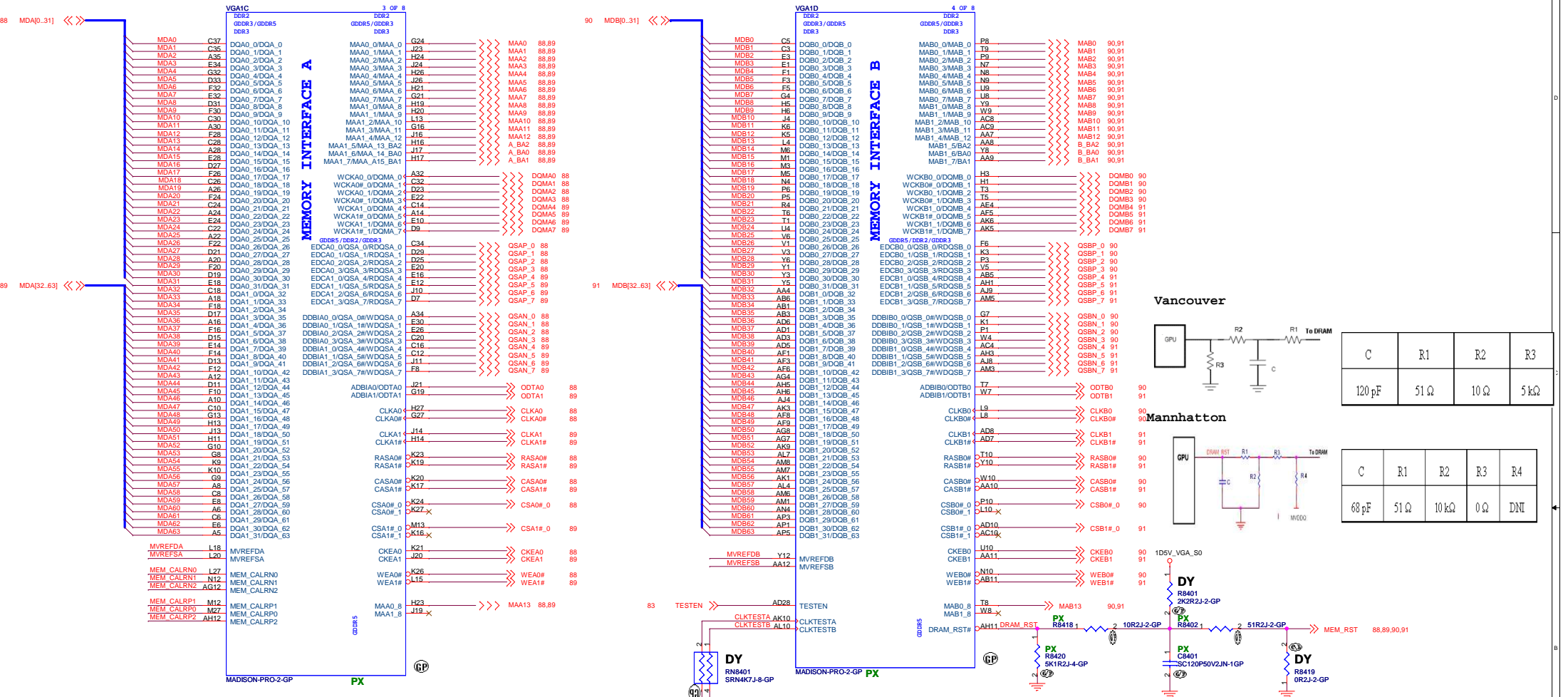
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GPU PCIE/STRAPPING(1/5)

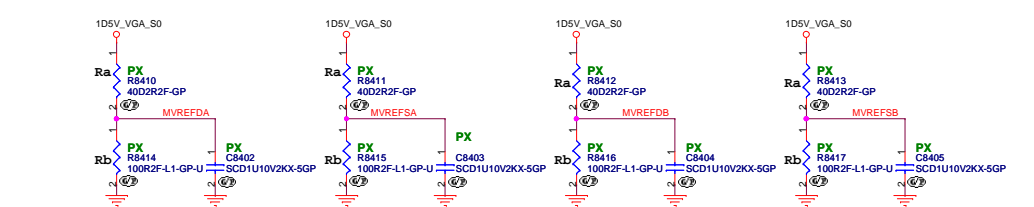
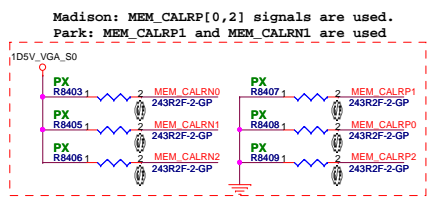
Title: **GPU PCIE/STRAPPING(1/5)**

Size A3 Document Number **LLW-1 / LGG-1** Rev **SB**

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PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



★ This basic topology should be used for DRAM_RST by DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

DDR3/GDDR3 Memory Stuff Option(M92/M96)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	GDDR3	DDR3
MVDDQ	1.8V/1.5V	1.5V
Ra	40.2R	100R
Rb	100R	100R

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GPU Memory(2/5)

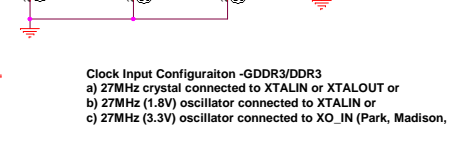
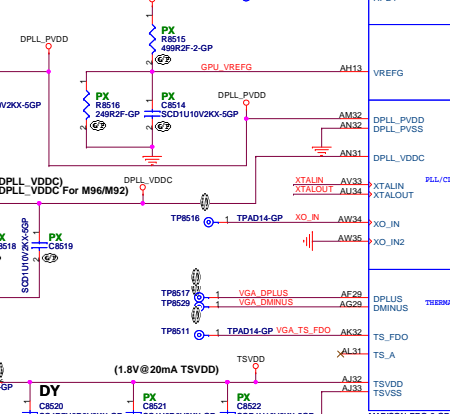
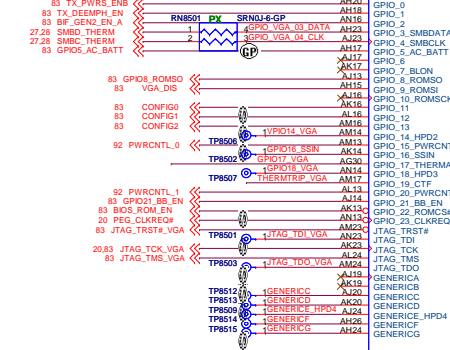
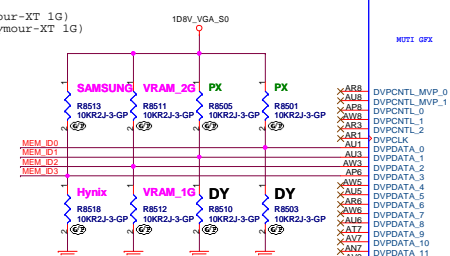
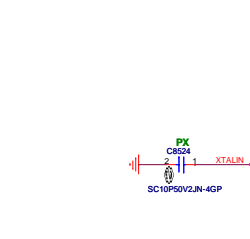
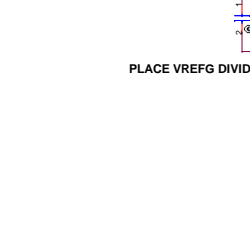
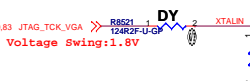
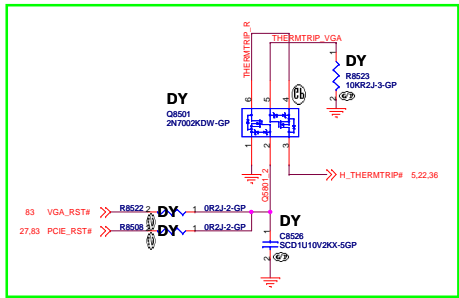
LLW-1 / LGG-1

Rev SB

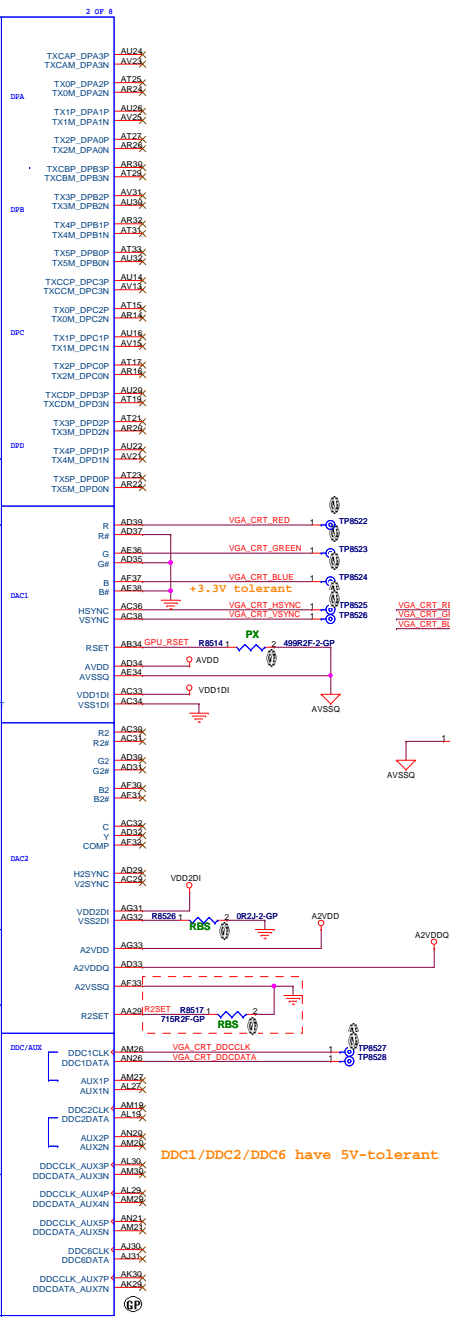
Date: 1uesday, November 08, 2010 Sheet 84 of 94

DVPDATA [3:2:1:0] for VRAM type
 selection H/W strap
 Should provide VRAM Table for VBIOS request

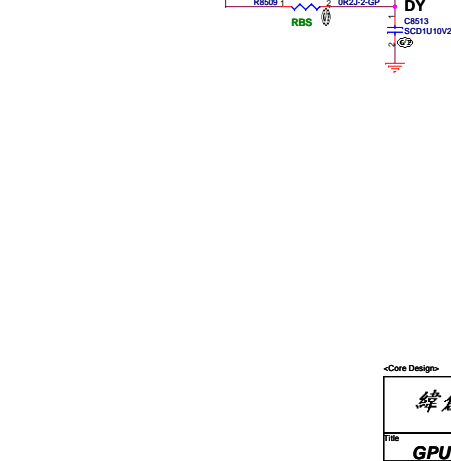
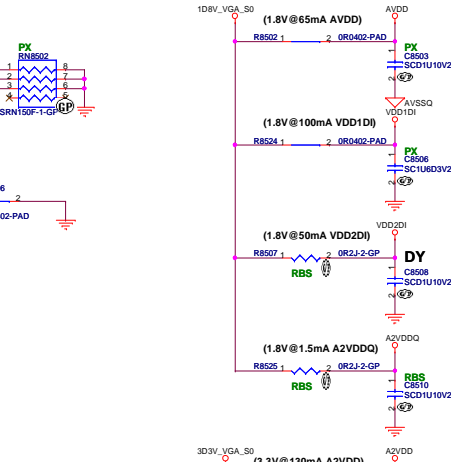
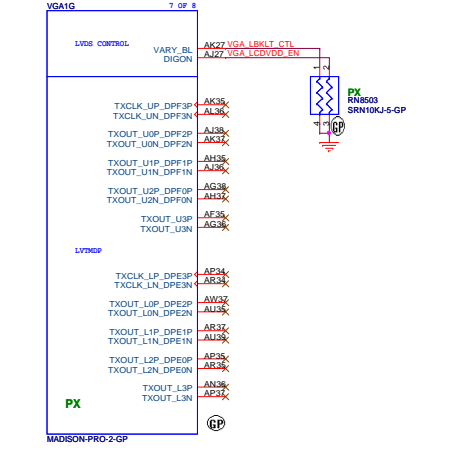
DVPDATA [3:0]
 0111 2Gbit Hynix-H5TQ2G63BFR-12C (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
 1111 2Gbit Samsung-K4W2G1646C-HC12 (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
 0011 1Gbit Hynix-H5TQ1G63BFR-12C (800MHz) (Whistler-LP 1G)
 0011 1Gbit Hynix-H5TQ1G63BFR-12C (800MHz) (Whistler-LP 1G)
 1011 1Gbit Samsung-K4W1G1646E-HC12 (800MHz) (Whistler-LP 1G)



Clock Input Configuration -GDDR3/DDR3
 a) 27MHz crystal connected to XTALIN or XTALOUT or
 b) 27MHz (1.8V) oscillator connected to XTALIN or
 c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

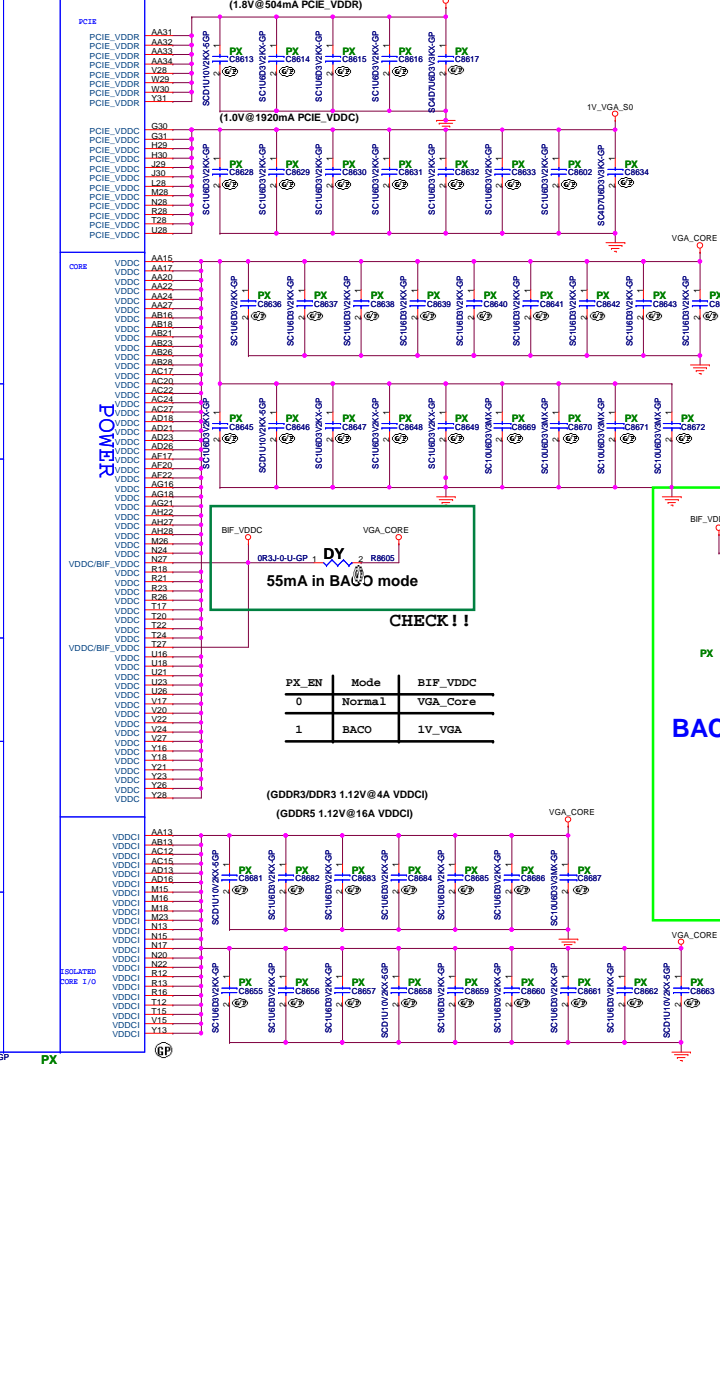
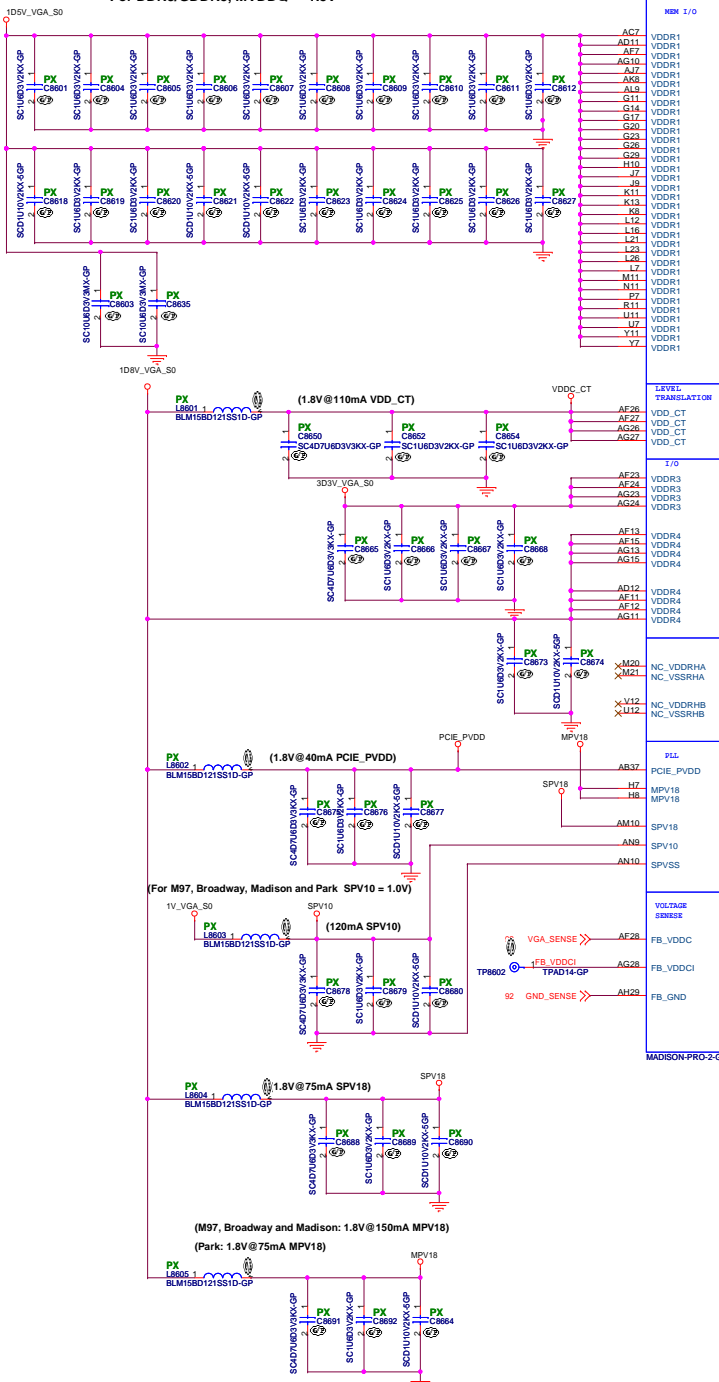


LVDS Interface

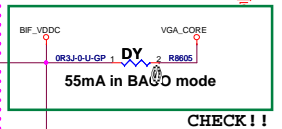


DDC1/DDC2/DDC6 have 5V-tolerant

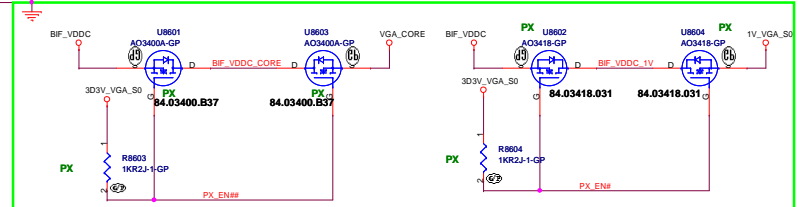
For DDR3/GDDR5, MVDDQ = 1.5V



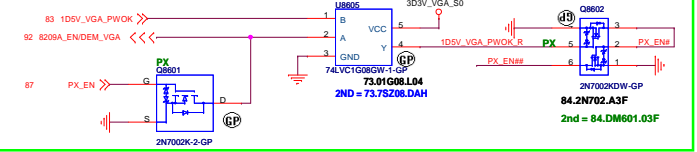
dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIe_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3, and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIe_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85-1.15V	OFF



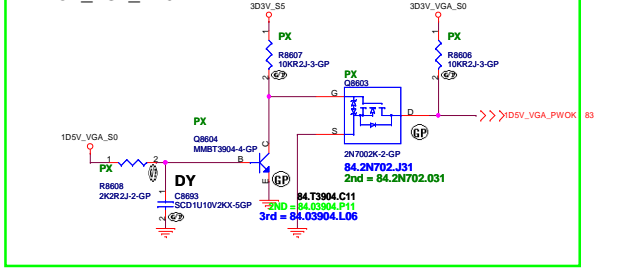
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

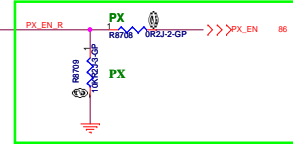
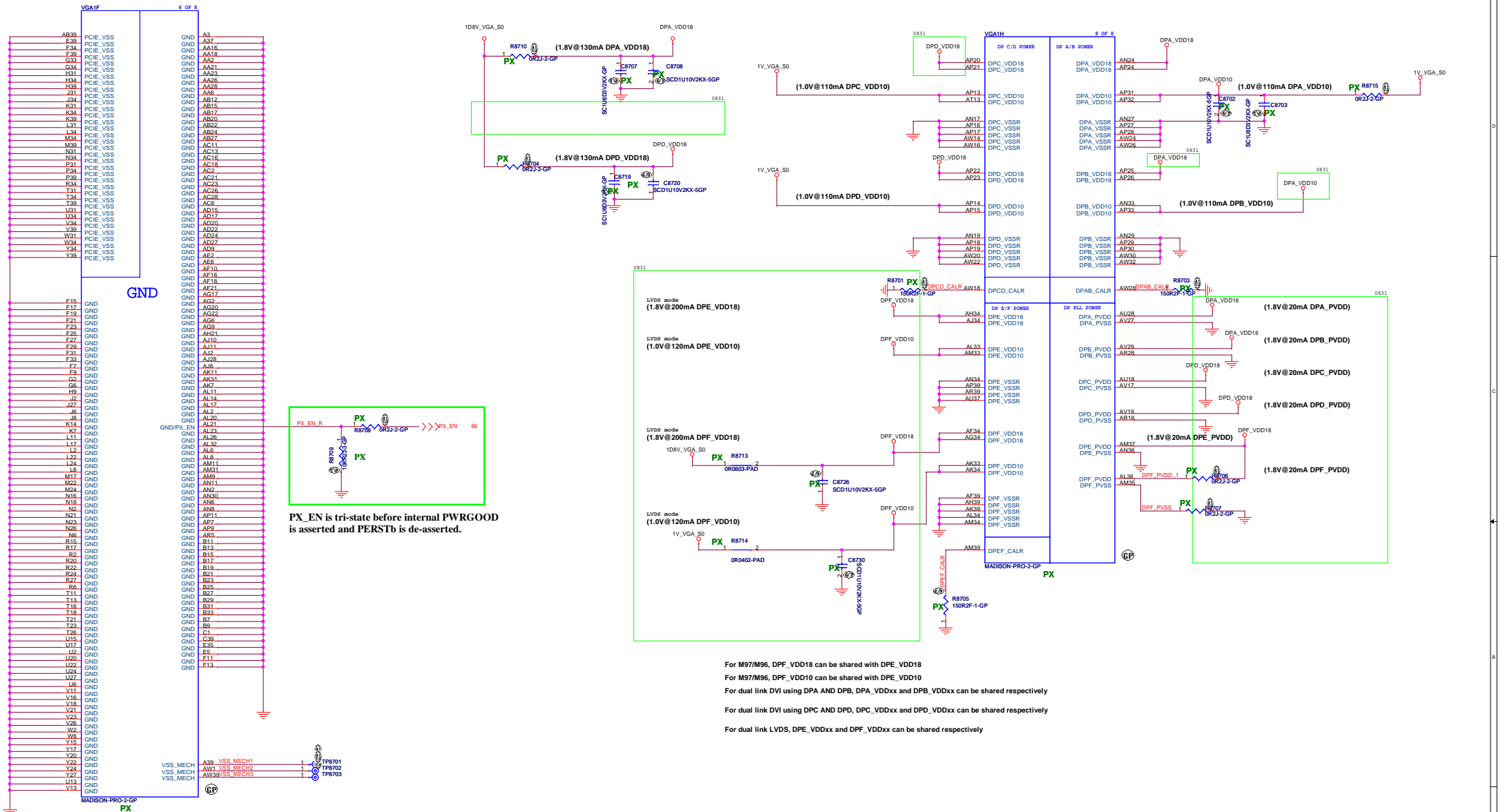


BACO mode



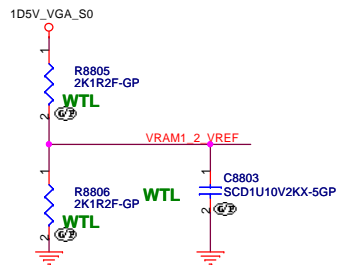
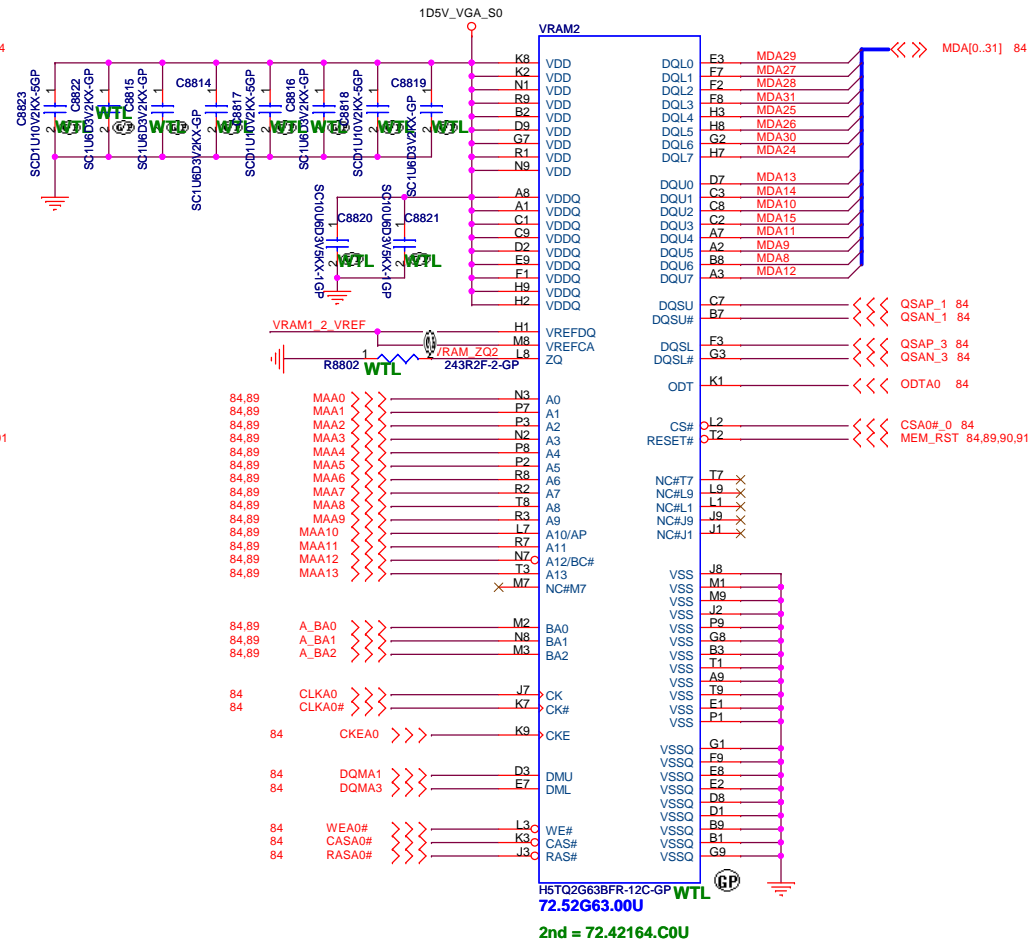
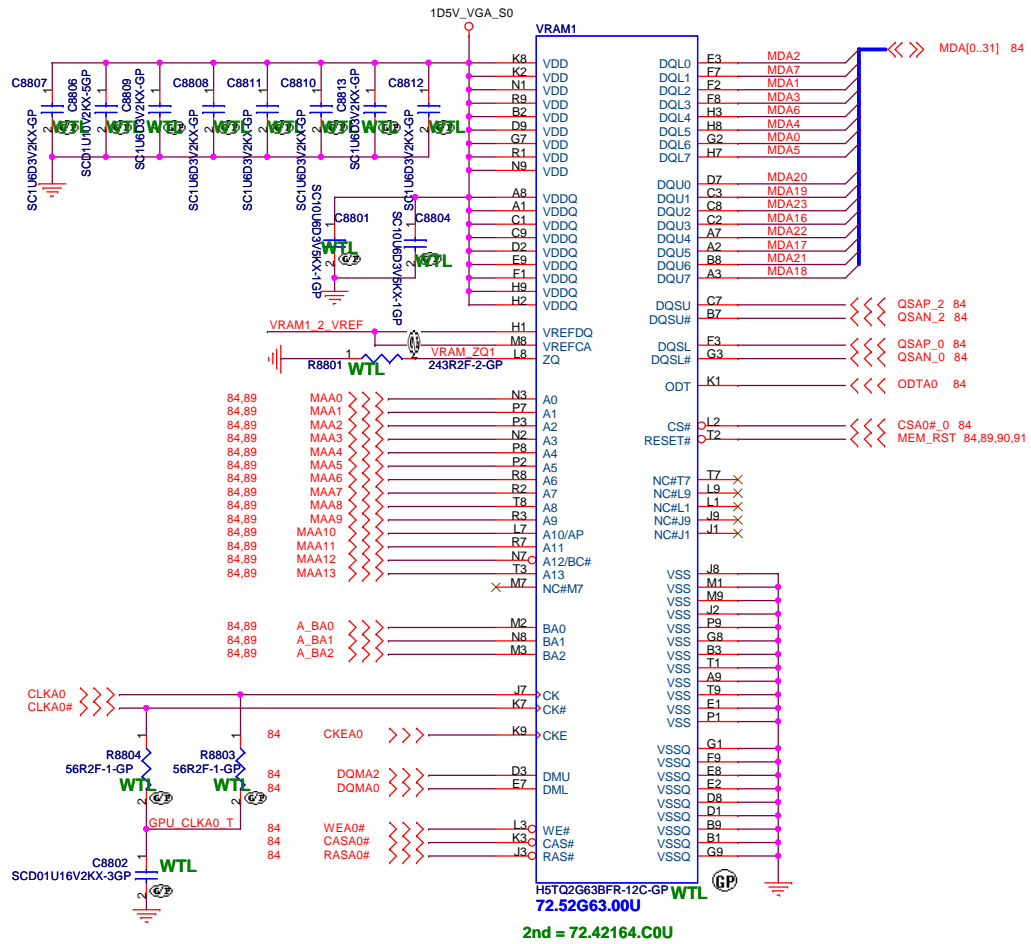
1.5V_VGA_PWOK

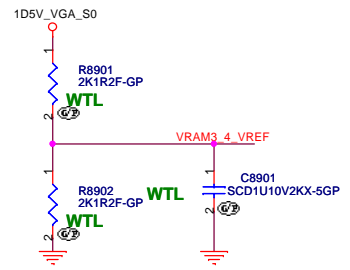
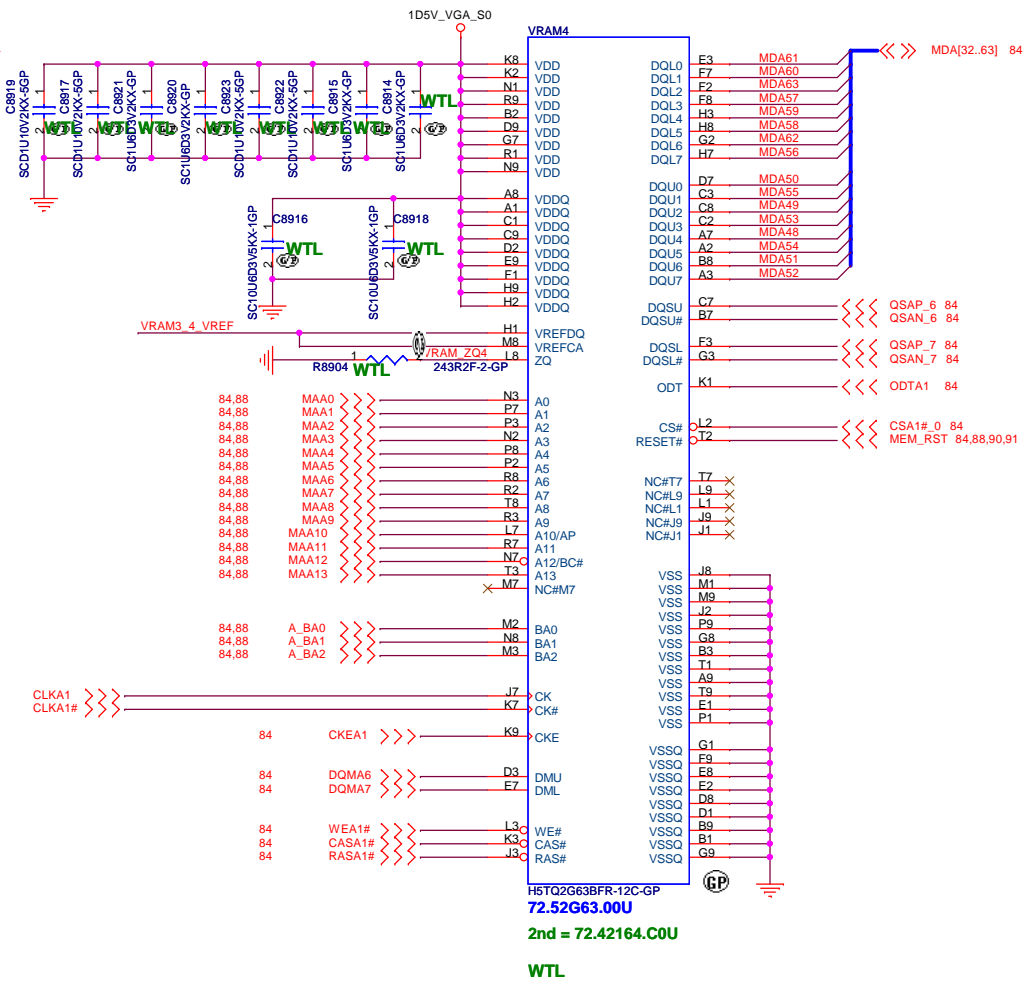
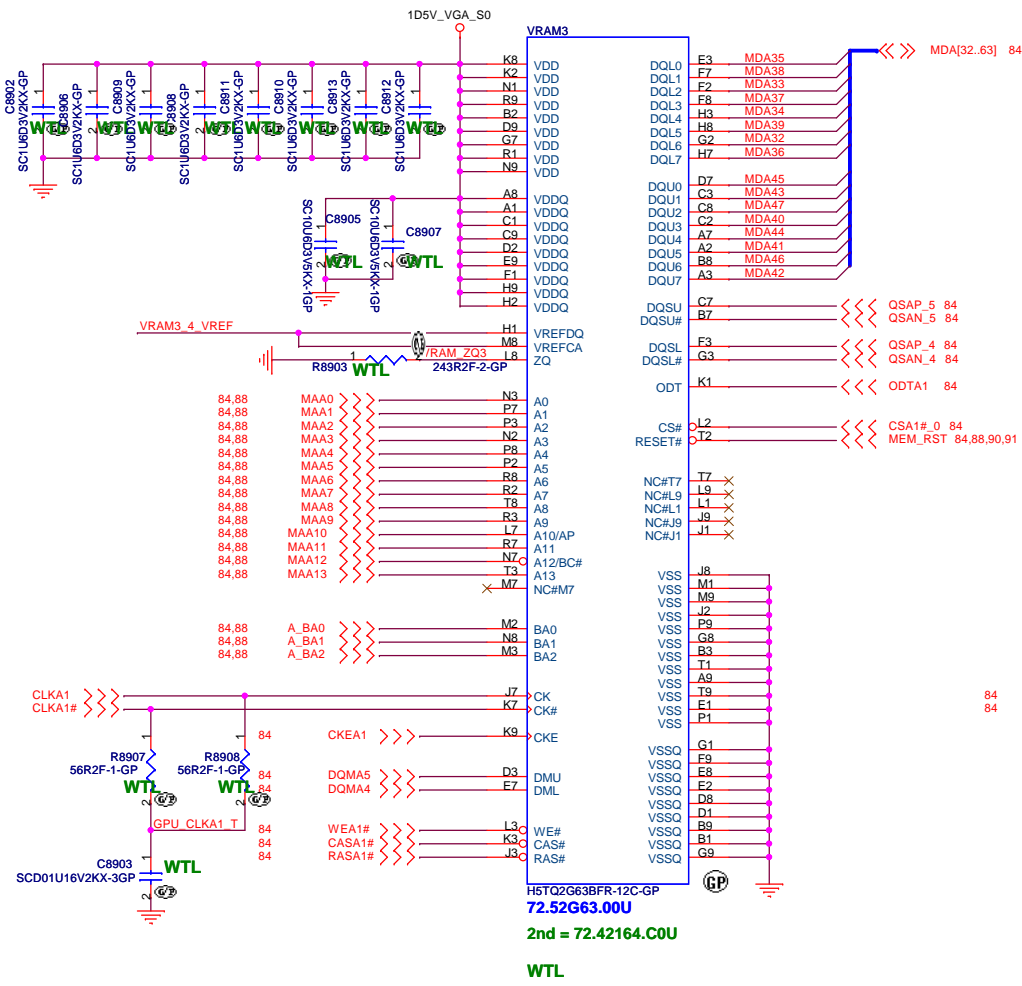


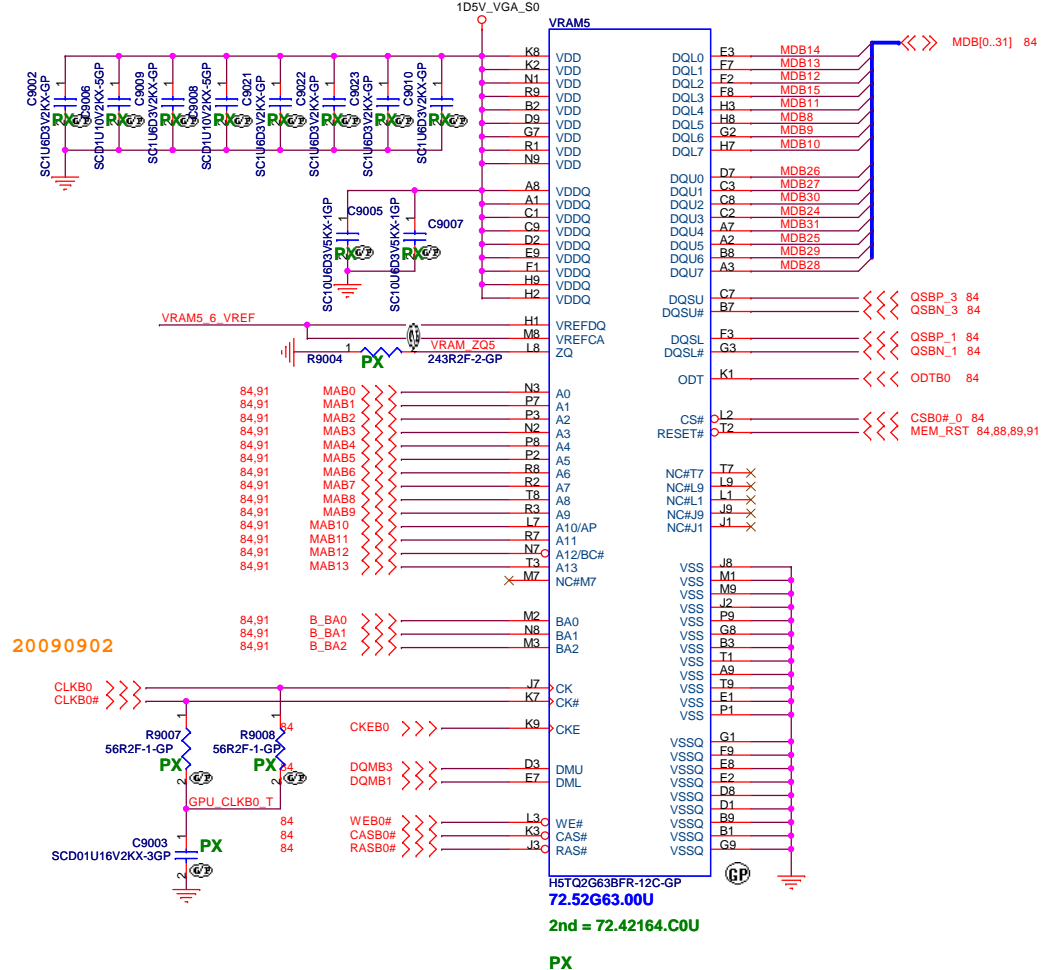


PX_EN is tri-state before internal PWRGOOD is asserted and PERSTb is de-asserted.

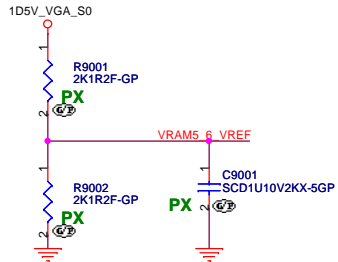
- For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
- For M97/M96, DPF_VDD10 can be shared with DPE_VDD10
- For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
- For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively
- For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively

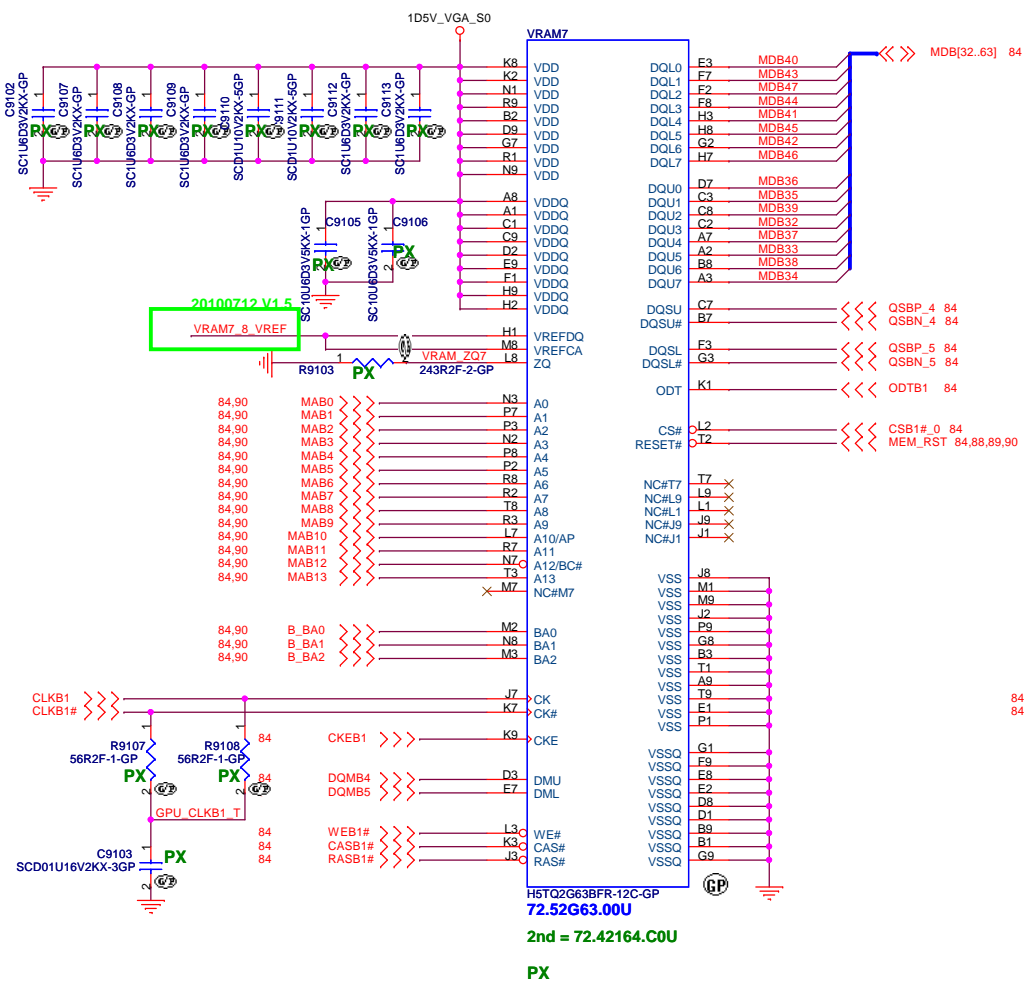






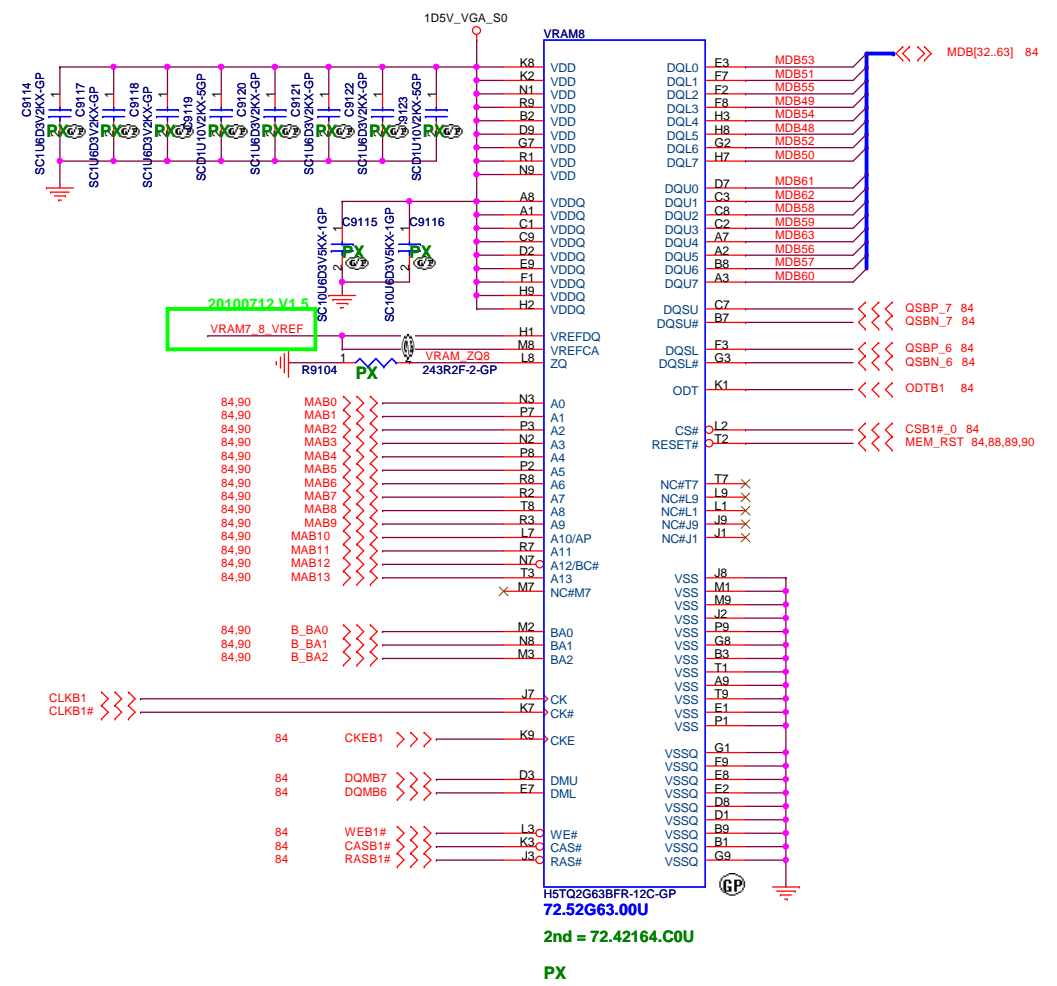
20090902





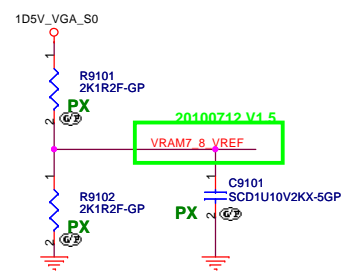
20100712 V1.5
VRAM7 8 VREF

2nd = 72.42164.C0U
PX



20100712 V1.5
VRAM8 8 VREF

2nd = 72.42164.C0U
PX



<Core Design>

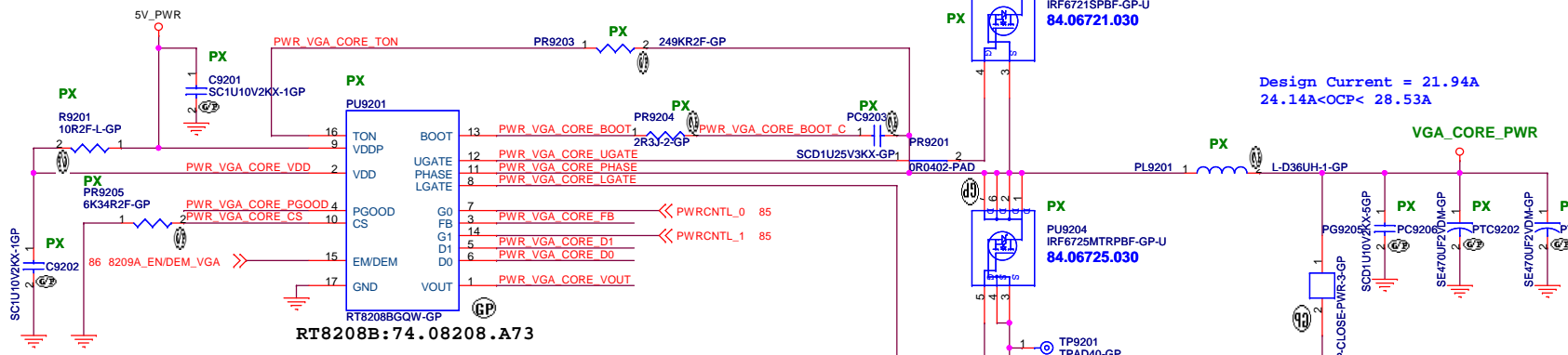
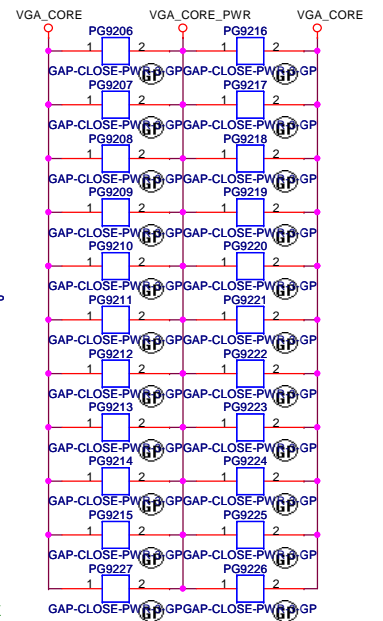
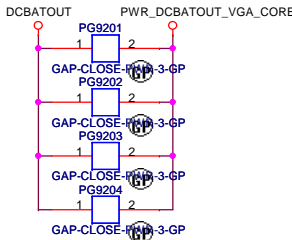
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Title: **GPU-VRAM7,8 (4/4)**

Size A3 Document Number **LLW-1 / LGG-1** Rev **SB**

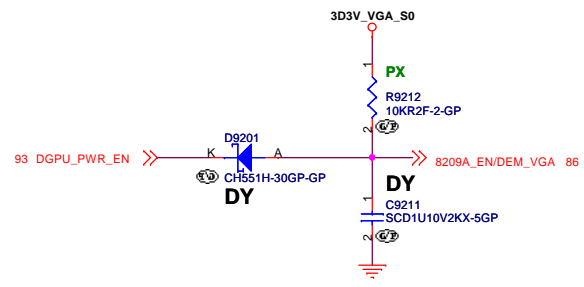
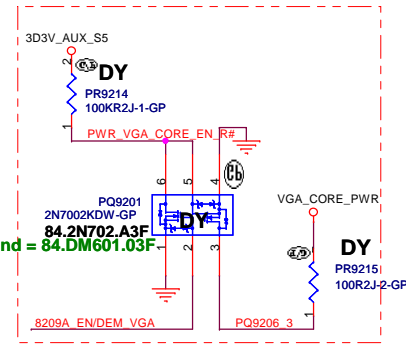
Date: Tuesday, November 09, 2010 Sheet 91 of 94

SSID = PWR.Plane.Regulator_GFX



Design Current = 21.94A
24.14A < OCP < 28.53A

$$V_{out} = 0.75V * (R1 + R2) / R2$$



MADSION PRO

I/O	Inter Pull Low	GPIO TABLE
NVDD_ALTV0	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

I/O	Inter Pull Low	GPIO TABLE
		GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

Park=>R9209=33K (64.33025.6DL)
Madison=>R9209=71.5K (64.71525.6DL)

NVDD_ALTV1	NVDD_ALTV0	+VGA_CORE
H	L	1.12V or 1V
H	H	0.9V

OUT=[R9208+(R9210//R9209)]/(R9210//R9209)
OUT=(R9208+R9210)/R9210

<Core Design>

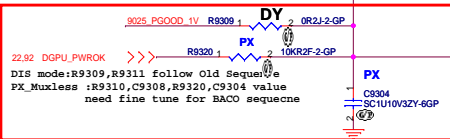
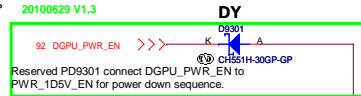
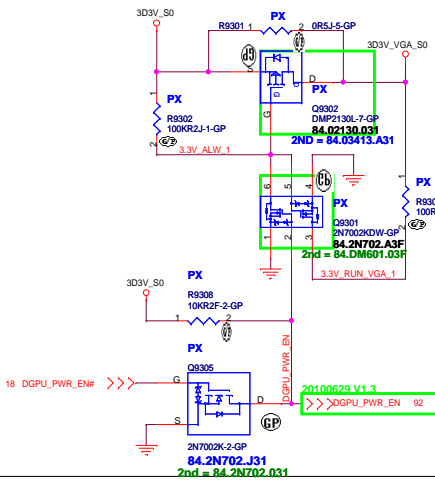
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8208B +VGA CORE**

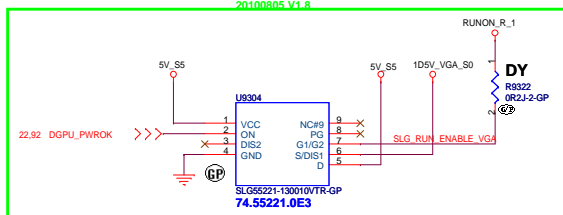
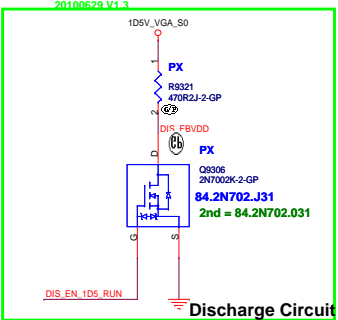
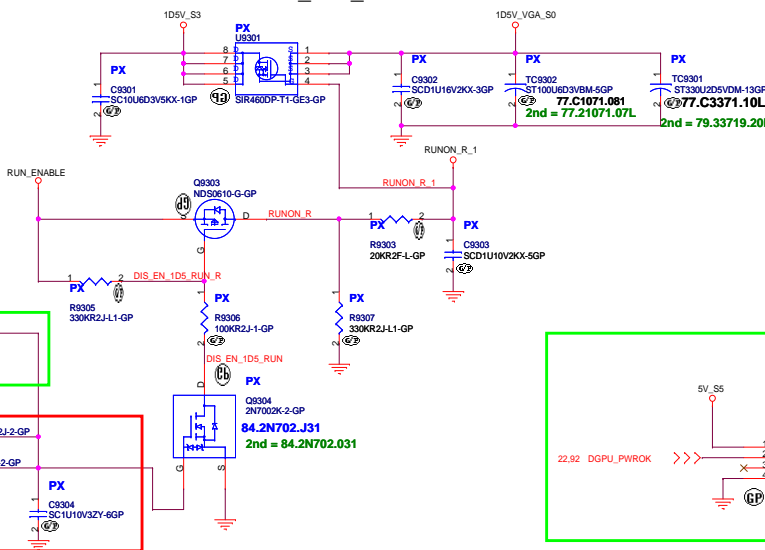
Size A3 Document Number **LLW-1 / LGG-1** Rev **SB**

Date: Tuesday, November 09, 2010 Sheet 92 of 94

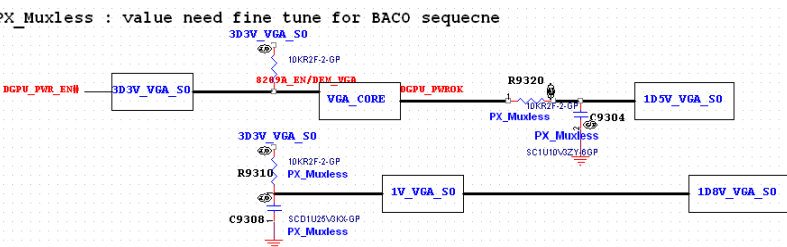
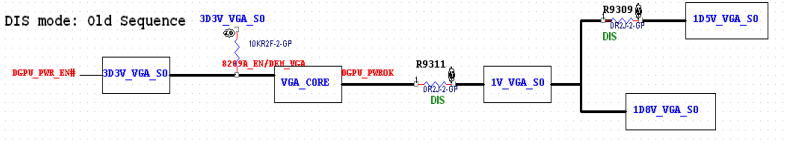
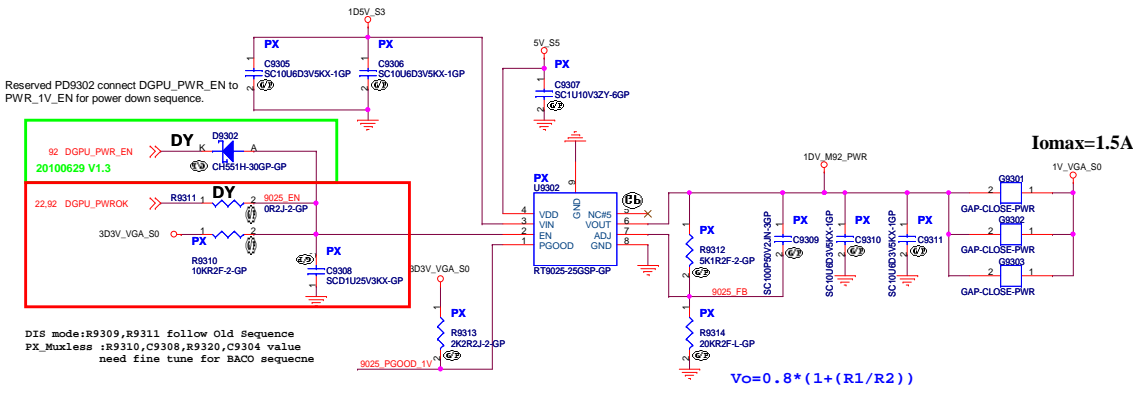
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



RT9025 for 1V_VGA



RT9025 for 1D8V_VGA

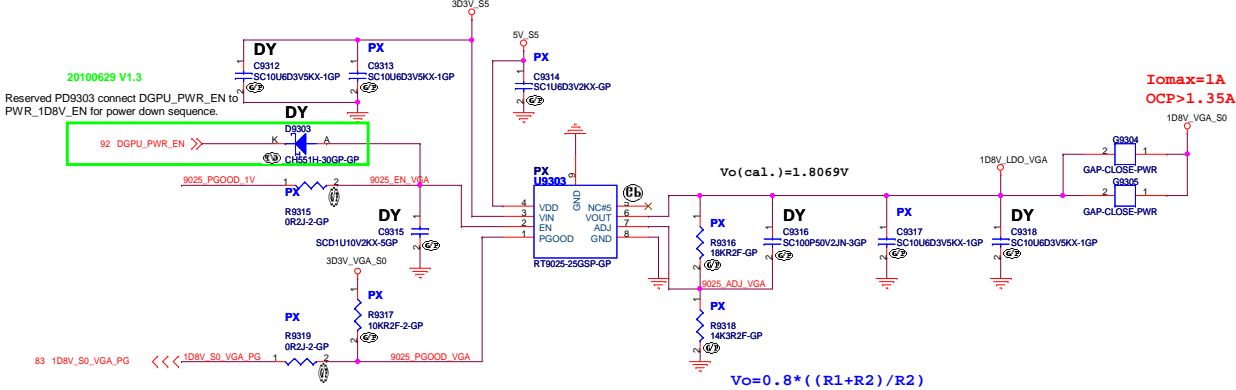


Table 93.1- Adjustable LDO Regulator multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
GMT	G9661-25ADJF11U	N/A	74.09661.07D
RIGHTEK	RT9025-25GSP	N/A	74.09025.A3D

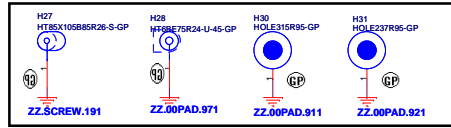
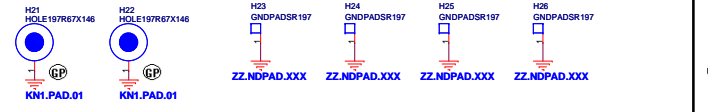
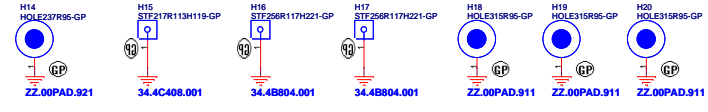
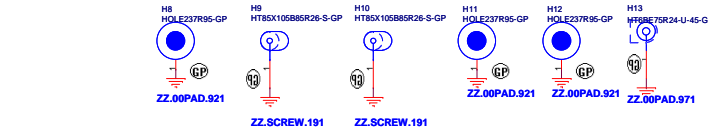
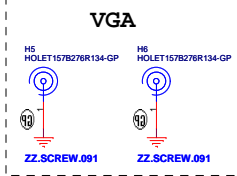
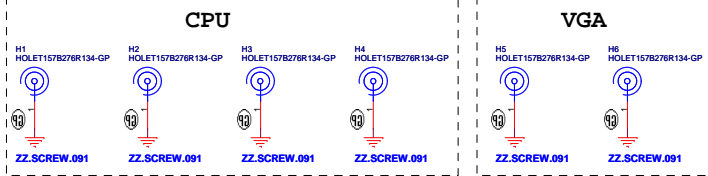
<Core Design>

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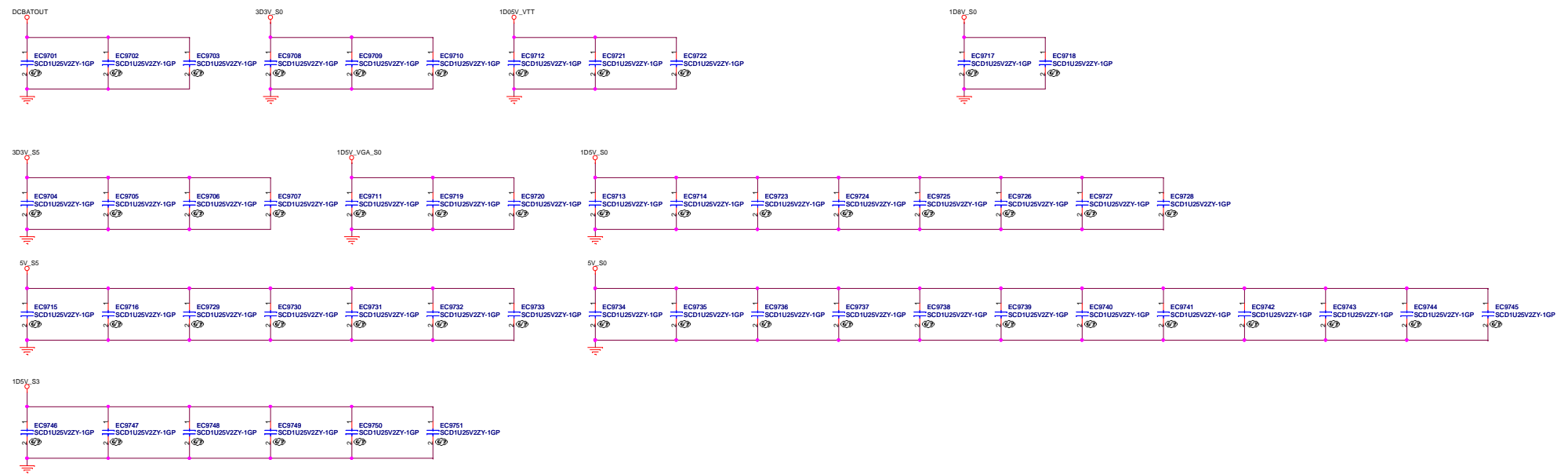
Title: **DISCRETE VGA POWER**

Size C Document Number: **LLW-1 / LGG-1** Rev: **SB**

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EMI CAP



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