

Orta Block Diagram

Project code: 91.4U101.001
 PCB P/N : 48.4U101.0SA
 REVISION : 06245-SA

PCB Layer Stackup

L1: Signal 1
 L2: VCC
 L3: Inner Signal 2
 L4: Inner Signal 3
 L5: GND
 L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

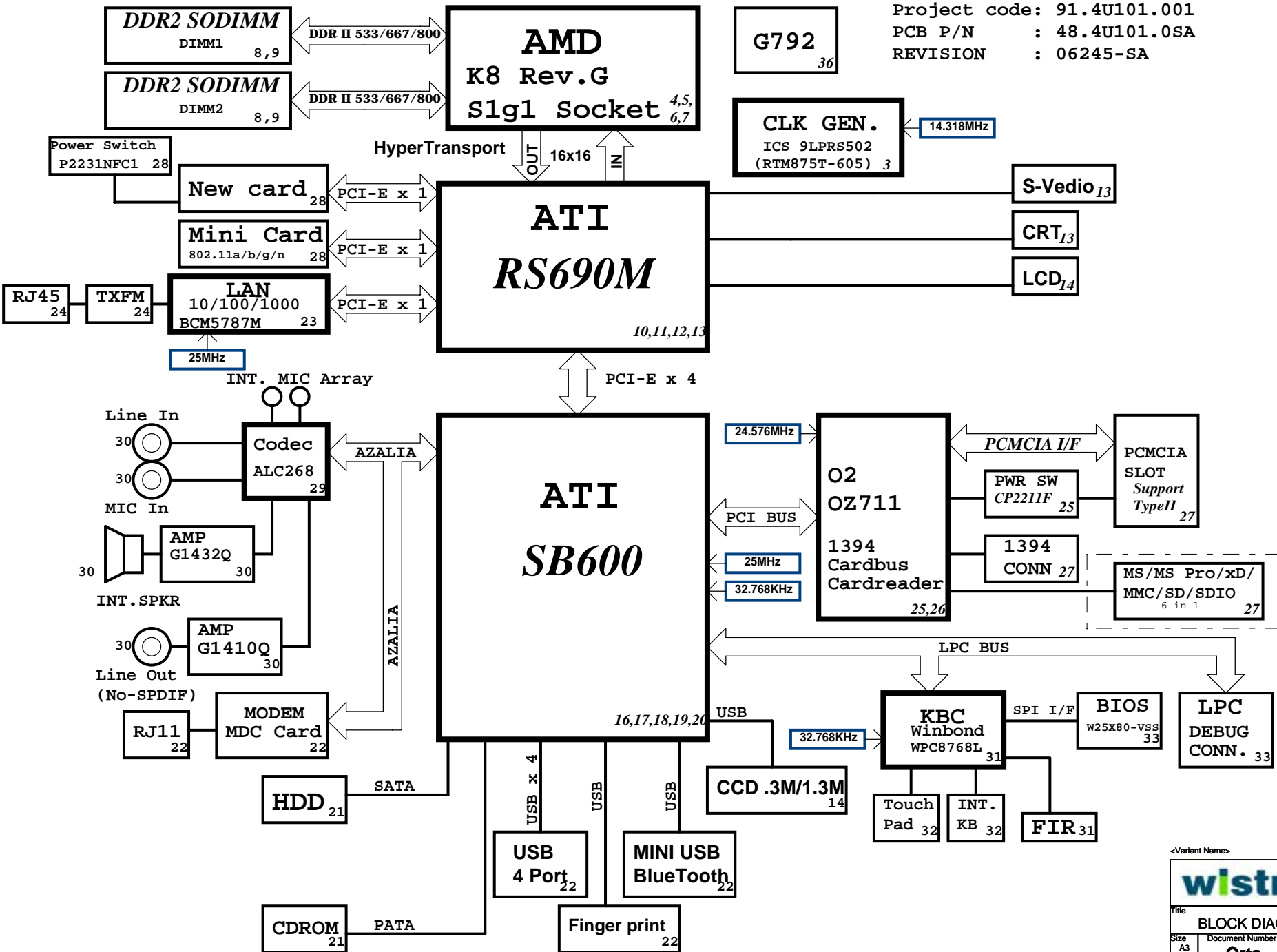
INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT



<Variant Name>

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Title: **BLOCK DIAGRAM**

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SA: 07/31/06 Start

SB change

power team

1.change L7, L9 to 68.1R510.10D

2.changge U12 to 84.04706.037

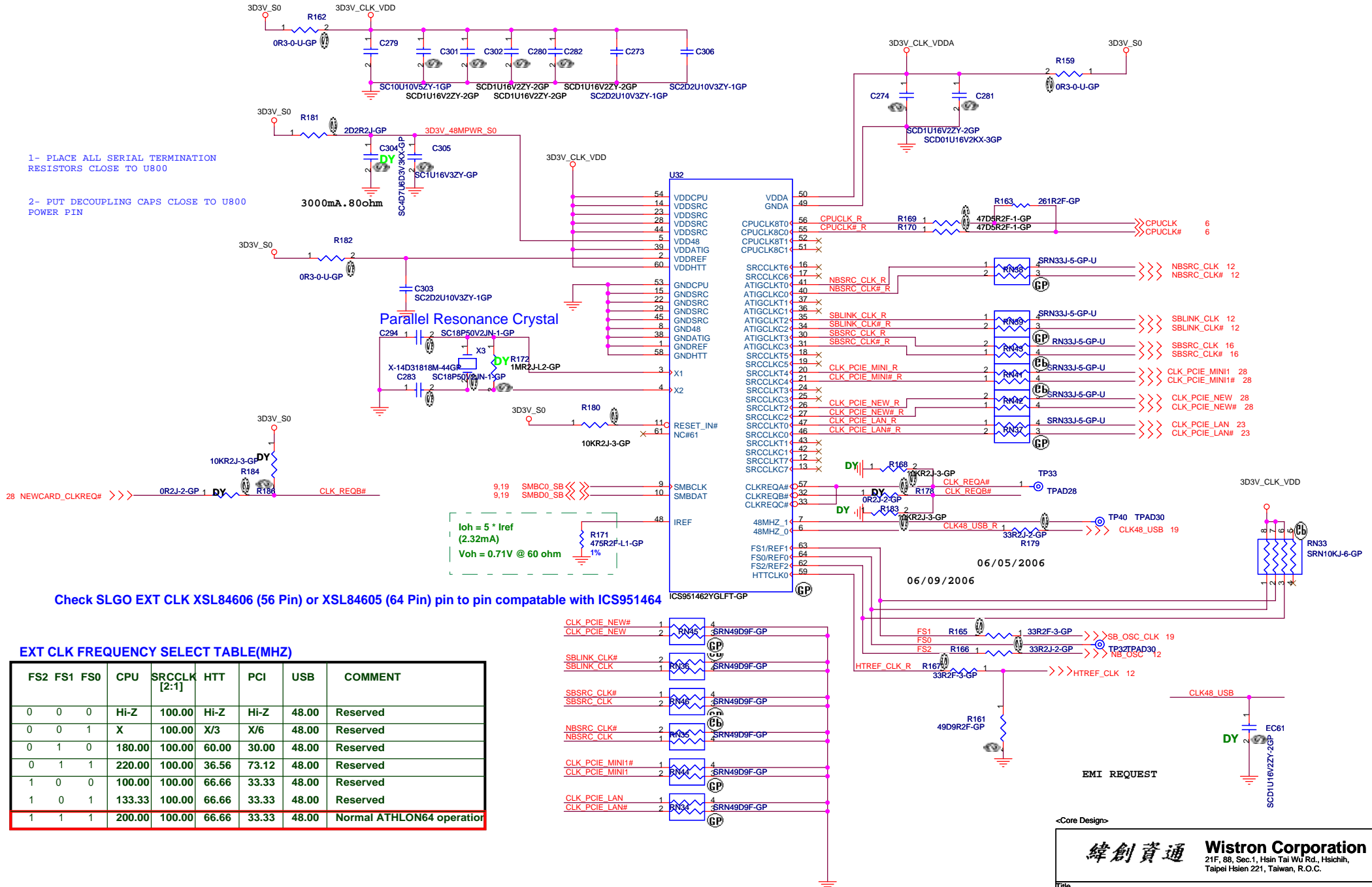
3.change R66 to 10K ohm

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Title		
CHANGE HISTORY		
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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



$$I_{oh} = 5 \cdot I_{ref} \quad (2.32mA)$$

$$V_{oh} = 0.71V @ 60 \text{ ohm}$$

Check SLGO EXT CLK XSL84606 (56 Pin) or XSL84605 (64 Pin) pin to pin compatible with ICS951464

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operator

<Core Design>

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Title: **CLKGEN_ICS951412**

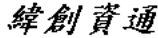
Size A3 Document Number **Orta** Rev SA

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62.10055.111

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CPU(1/4)_HyperTransport I/F		
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9 M_A_DQ[63.0]

U528

M A DQ63 AA12	MA_DATA63	Y16	M A CLK_DDR2 9
M A DQ62 AB12	MA_DATA62	AA16	M A CLK_DDR2# 9
M A DQ61 AA14	MA_DATA61	E16	M A_CLK_DDR1 9
M A DQ60 AB14	MA_DATA60	F16	M A_CLK_DDR1# 9
M A DQ59 W11	MA_DATA59	V19	M_A_CS3# 8,9
M A DQ58 Y12	MA_DATA58	J22	M_A_CS2# 8,9
M A DQ57 AD13	MA_DATA57	Y22	M_A_CS1# 8,9
M A DQ56 AB13	MA_DATA56	T19	M_A_CS0# 8,9
M A DQ55 AD15	MA_DATA55	V20	M_A_ODT1 8,9
M A DQ54 AB15	MA_DATA54	U19	M_A_ODT0 8,9
M A DQ53 AB17	MA_DATA53	U20	M_A_CAS# 8,9
M A DQ52 Y17	MA_DATA52	U21	M_A_WE# 8,9
M A DQ51 Y14	MA_DATA51	T20	M_A_RAS# 8,9
M A DQ50 W14	MA_DATA50	K22	M_A_BS#2 8,9
M A DQ49 W16	MA_DATA49	R20	M_A_BS#1 8,9
M A DQ48 AD17	MA_DATA48	T22	M_A_BS#0 8,9
M A DQ47 Y18	MA_DATA47	J20	M_A_CKE1 8,9
M A DQ46 AD21	MA_DATA46	J21	M_A_CKE0 8,9
M A DQ45 AB21	MA_DATA45	K19	M A A15
M A DQ44 AB21	MA_DATA44	K20	M A A14
M A DQ43 AB18	MA_DATA43	Y20	M A A13
M A DQ42 AA18	MA_DATA42	K24	M A A12
M A DQ41 AA20	MA_DATA41	L20	M A A11
M A DQ40 Y20	MA_DATA40	R19	M A A10
M A DQ39 AA22	MA_DATA39	L19	M A A9
M A DQ38 Y22	MA_DATA38	L22	M A A8
M A DQ37 W21	MA_DATA37	L21	M A A7
M A DQ36 W22	MA_DATA36	M19	M A A6
M A DQ35 AA21	MA_DATA35	M20	M A A5
M A DQ34 AB22	MA_DATA34	M24	M A A4
M A DQ33 AB24	MA_DATA33	M22	M A A3
M A DQ32 Y24	MA_DATA32	N22	M A A2
M A DQ31 H22	MA_DATA31	N21	M A A1
M A DQ30 H20	MA_DATA30	R21	M A A0
M A DQ29 E22	MA_DATA29	W12	M A DQS7
M A DQ28 E21	MA_DATA28	W13	M A DQS#7
M A DQ27 H19	MA_DATA27	Y15	M A DQS6
M A DQ26 H24	MA_DATA26	W15	M A DQS#6
M A DQ25 E22	MA_DATA25	AB19	M A DQS5
M A DQ24 F20	MA_DATA24	AB20	M A DQS#5
M A DQ23 C23	MA_DATA23	AD23	M A DQS4
M A DQ22 B22	MA_DATA22	AC23	M A DQS#4
M A DQ21 F18	MA_DATA21	G22	M A DQS3
M A DQ20 E18	MA_DATA20	G21	M A DQS#3
M A DQ19 E18	MA_DATA19	C22	M A DQS2
M A DQ18 D22	MA_DATA18	C21	M A DQS#2
M A DQ17 C19	MA_DATA17	G16	M A DQS1
M A DQ16 G18	MA_DATA16	G15	M A DQS#1
M A DQ15 G17	MA_DATA15	G13	M A DQS0
M A DQ14 C17	MA_DATA14	H13	M A DQS#0
M A DQ13 E14	MA_DATA13	Y13	M A DM7
M A DQ12 E14	MA_DATA12	AB16	M A DM6
M A DQ11 H17	MA_DATA11	Y19	M A DM5
M A DQ10 E17	MA_DATA10	AC24	M A DM4
M A DQ9 E15	MA_DATA9	F24	M A DM3
M A DQ8 H15	MA_DATA8	E19	M A DM2
M A DQ7 E13	MA_DATA7	C15	M A DM1
M A DQ6 C13	MA_DATA6	E12	M A DM0
M A DQ5 H12	MA_DATA5		
M A DQ4 H11	MA_DATA4		
M A DQ3 G14	MA_DATA3		
M A DQ2 H14	MA_DATA2		
M A DQ1 E12	MA_DATA1		
M A DQ0 G12	MA_DATA0		

MEMORY INTERFACE

9 M_B_DQ[63.0]

U52C

M B DQ63 AD11	MB_DATA63	AF18	M_B_CLK_DDR2 9
M B DQ62 AE11	MB_DATA62	AE17	M_B_CLK_DDR2# 9
M B DQ61 AF14	MB_DATA61	A17	M_B_CLK_DDR1 9
M B DQ60 AE14	MB_DATA60	A18	M_B_CLK_DDR1# 9
M B DQ59 Y11	MB_DATA59	Y26	M_B_CS3# 8,9
M B DQ58 AF11	MB_DATA58	J24	M_B_CS2# 8,9
M B DQ57 AC12	MB_DATA57	W24	M_B_CS1# 8,9
M B DQ56 AE13	MB_DATA56	U23	M_B_CS0# 8,9
M B DQ55 AE15	MB_DATA55	W23	M_B_ODT1 8,9
M B DQ54 AF16	MB_DATA54	W26	M_B_ODT0 8,9
M B DQ53 AC18	MB_DATA53	V26	M_B_CAS# 8,9
M B DQ52 AF19	MB_DATA52	U22	M_B_WE# 8,9
M B DQ51 AD14	MB_DATA51	U24	M_B_RAS# 8,9
M B DQ50 AC14	MB_DATA50	K26	M_B_BS#2 8,9
M B DQ49 AE18	MB_DATA49	T26	M_B_BS#1 8,9
M B DQ48 AD18	MB_DATA48	U26	M_B_BS#0 8,9
M B DQ47 AD20	MB_DATA47	H26	M_B_CKE1 8,9
M B DQ46 AC20	MB_DATA46	J23	M_B_CKE0 8,9
M B DQ45 AE23	MB_DATA45	J25	M B A15
M B DQ44 AE23	MB_DATA44	J26	M B A14
M B DQ43 AE20	MB_DATA43	W25	M B A13
M B DQ42 AE20	MB_DATA42	L23	M B A12
M B DQ41 AD22	MB_DATA41	L25	M B A11
M B DQ40 AC22	MB_DATA40	L25	M B A10
M B DQ39 AE25	MB_DATA39	U25	M B A9
M B DQ38 AD26	MB_DATA38	L24	M B A8
M B DQ37 AA25	MB_DATA37	M26	M B A7
M B DQ36 AA26	MB_DATA36	L26	M B A6
M B DQ35 AE24	MB_DATA35	N23	M B A5
M B DQ34 AD24	MB_DATA34	N24	M B A4
M B DQ33 AA23	MB_DATA33	N25	M B A3
M B DQ32 AA24	MB_DATA32	N26	M B A2
M B DQ31 G24	MB_DATA31	P24	M B A1
M B DQ30 G23	MB_DATA30	T24	M B A0
M B DQ29 D26	MB_DATA29	AF12	M B DQS7
M B DQ28 C26	MB_DATA28	AE12	M B DQS#7
M B DQ27 G26	MB_DATA27	AE16	M B DQS6
M B DQ26 G25	MB_DATA26	AD16	M B DQS#6
M B DQ25 E24	MB_DATA25	AF21	M B DQS5
M B DQ24 F23	MB_DATA24	AF22	M B DQS#5
M B DQ23 C24	MB_DATA23	AC25	M B DQS4
M B DQ22 B24	MB_DATA22	AC26	M B DQS#4
M B DQ21 C20	MB_DATA21	F26	M B DQS3
M B DQ20 B20	MB_DATA20	E26	M B DQS#3
M B DQ19 C25	MB_DATA19	A24	M B DQS2
M B DQ18 D24	MB_DATA18	A23	M B DQS#2
M B DQ17 A21	MB_DATA17	D16	M B DQS1
M B DQ16 D20	MB_DATA16	C16	M B DQS#1
M B DQ15 D18	MB_DATA15	C12	M B DQS0
M B DQ14 C18	MB_DATA14	B12	M B DQS#0
M B DQ13 D14	MB_DATA13	AD12	M B DM7
M B DQ12 C14	MB_DATA12	AC16	M B DM6
M B DQ11 A20	MB_DATA11	M26	M B DM5
M B DQ10 A19	MB_DATA10	AB26	M B DM4
M B DQ9 A16	MB_DATA9	E25	M B DM3
M B DQ8 A15	MB_DATA8	A22	M B DM2
M B DQ7 A13	MB_DATA7	B16	M B DM1
M B DQ6 D12	MB_DATA6	A12	M B DM0
M B DQ5 E11	MB_DATA5		
M B DQ4 G11	MB_DATA4		
M B DQ3 B14	MB_DATA3		
M B DQ2 A14	MB_DATA2		
M B DQ1 A11	MB_DATA1		
M B DQ0 C11	MB_DATA0		

MEMORY INTERFACE

M_A_A[15.0] 8,9

M_B_A[15.0] 8,9

M_A_DQS[7.0] 9

M_B_DQS[7.0] 9

M_A_DQS#[7.0] 9

M_B_DQS#[7.0] 9

M_A_DM[7.0] 9

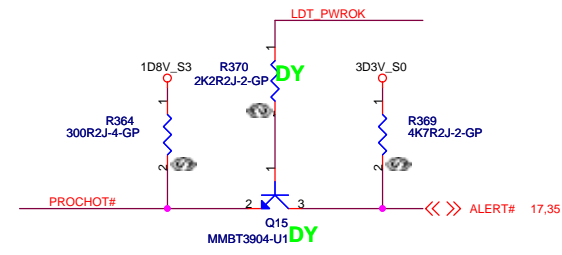
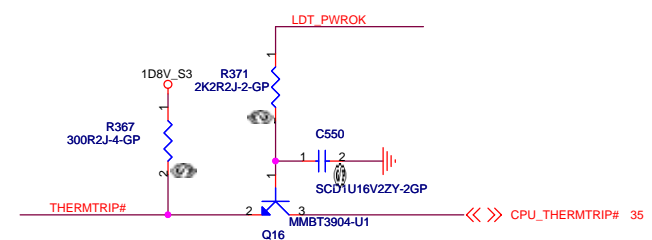
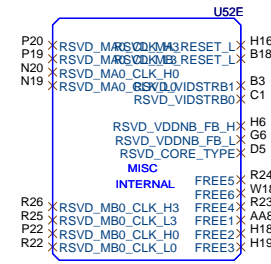
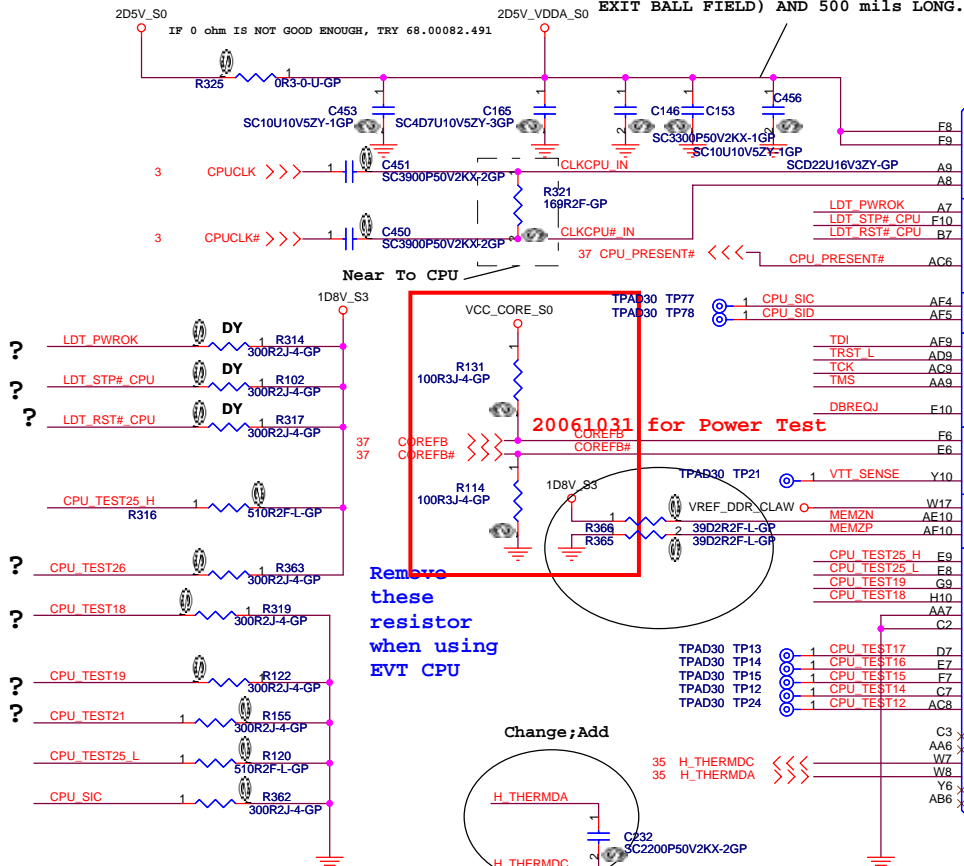
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<Core Design>

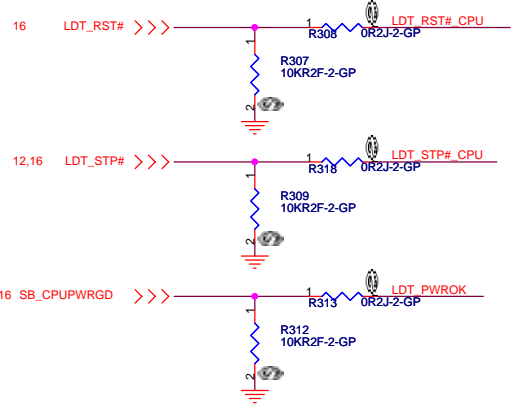
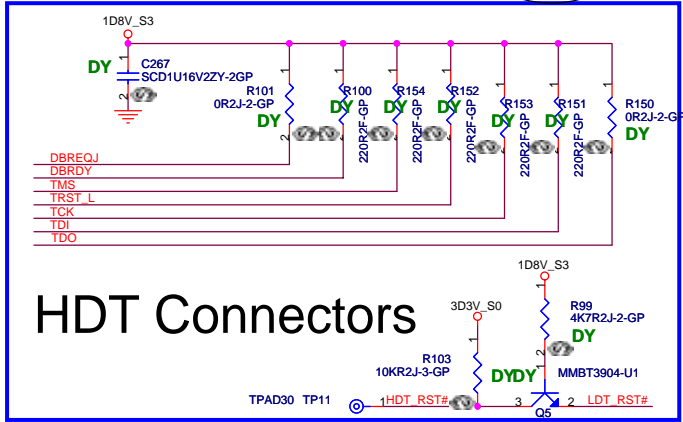
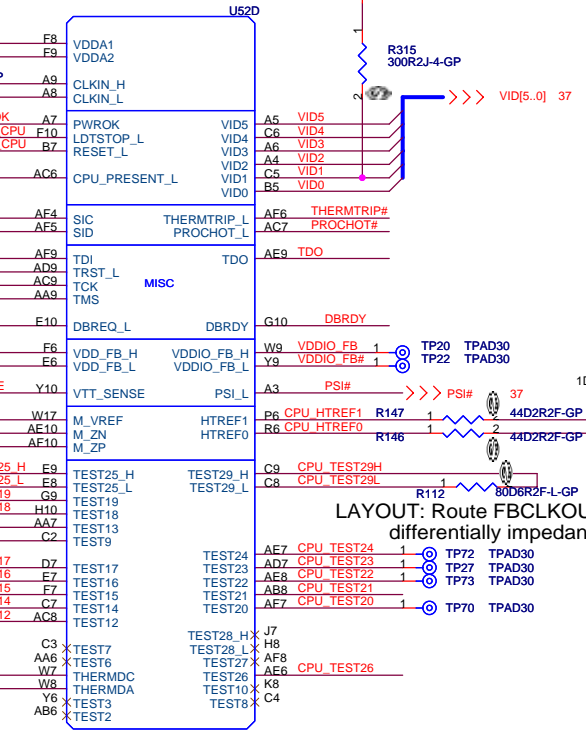
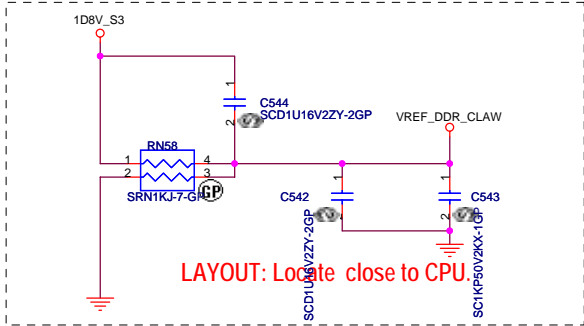
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Title	CPU(2/4) DDR		
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LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



VREF_DDR_CLAW



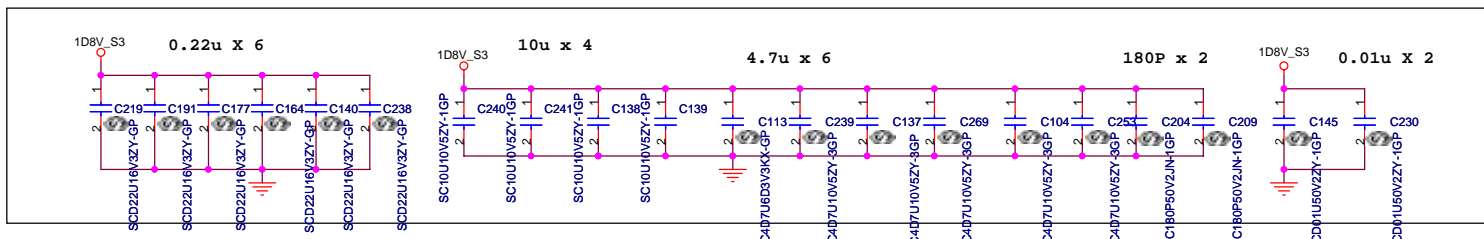
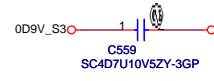
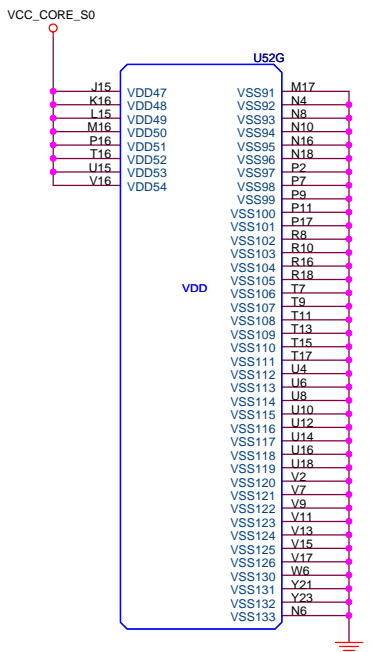
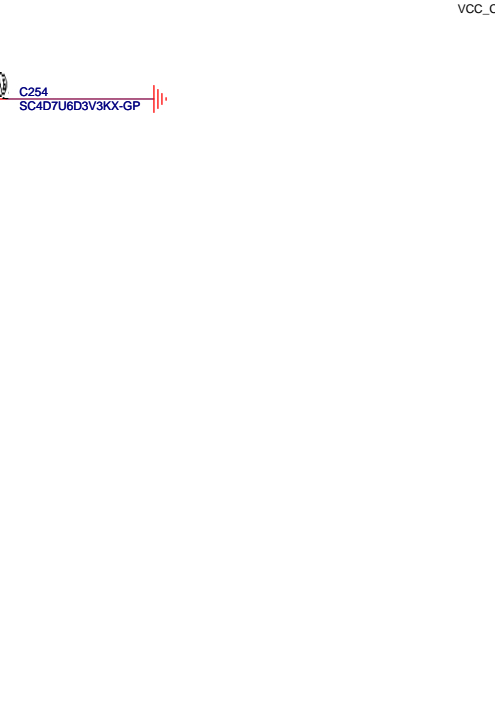
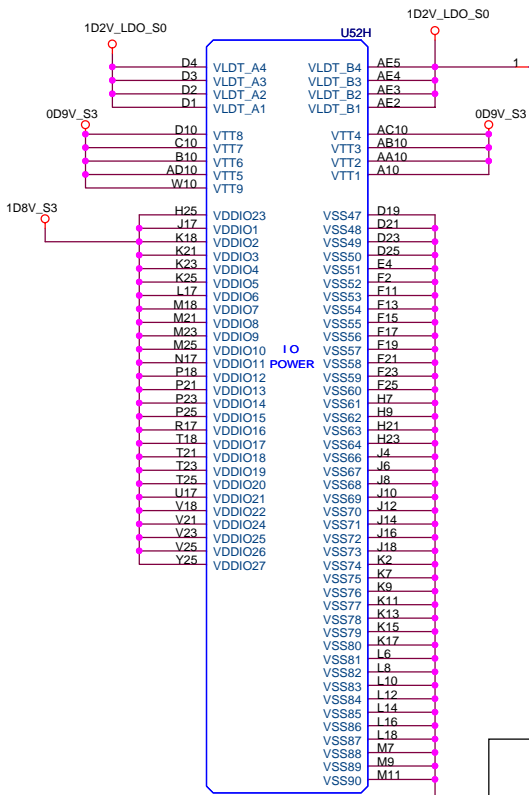
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(3/4)_Control & Debug**

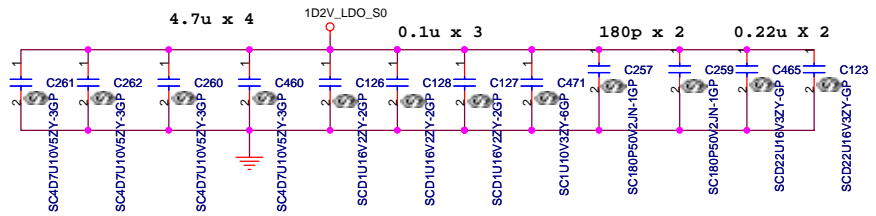
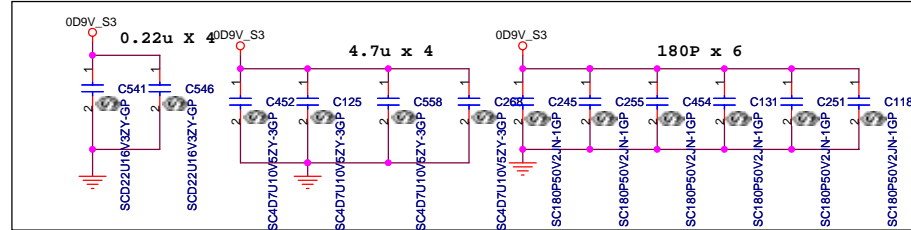
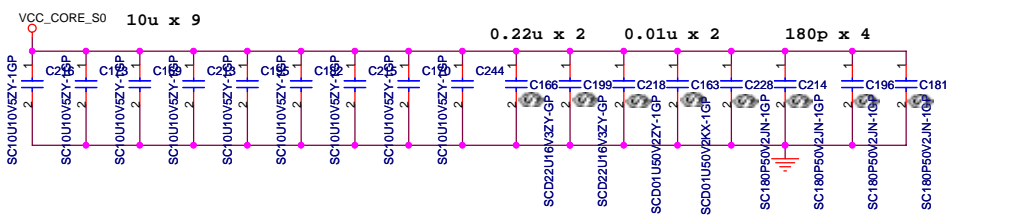
Size: A3 Document Number: **Orta** Rev: SA

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Place near to CPU

LAYOUT: Place on backside of processor.



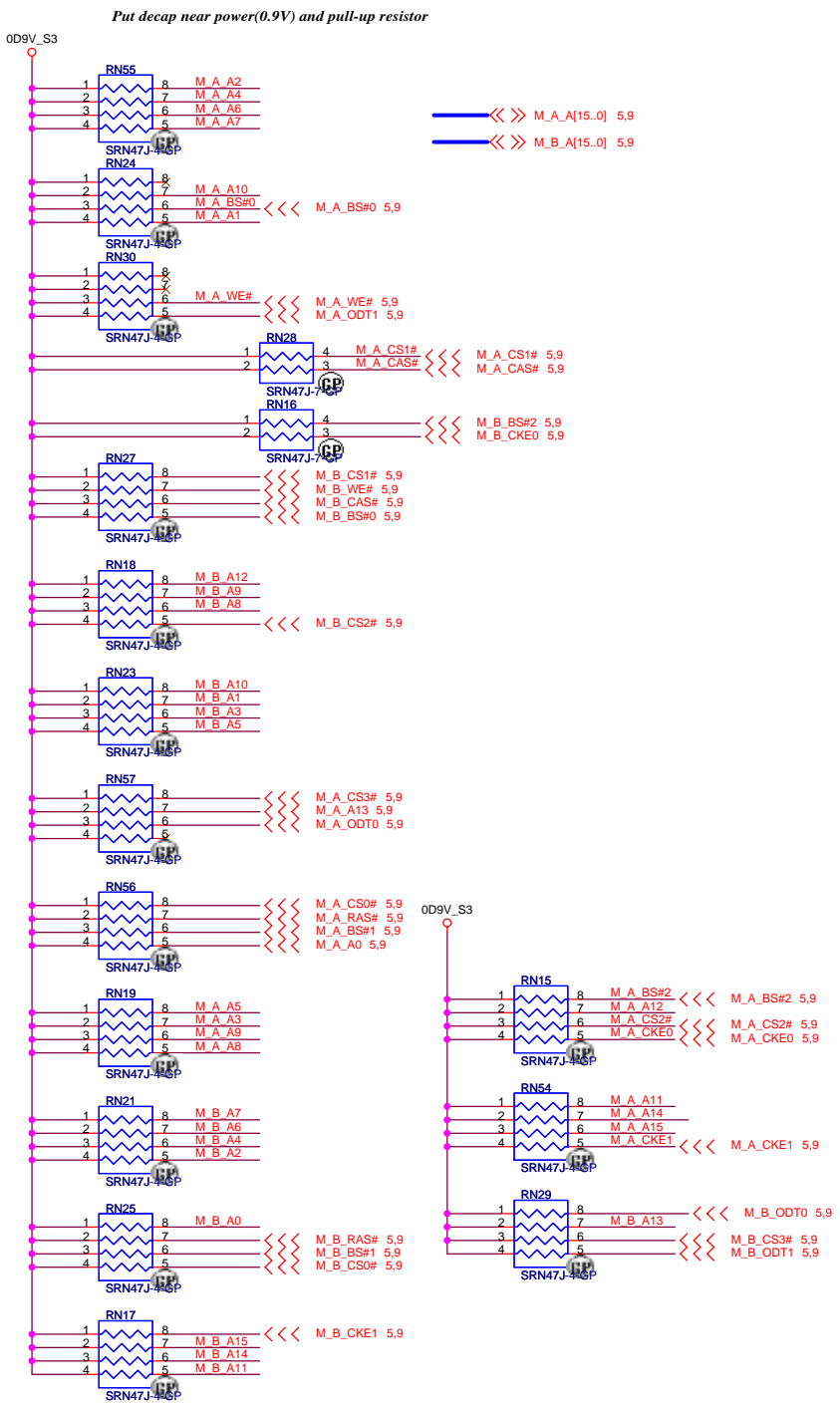
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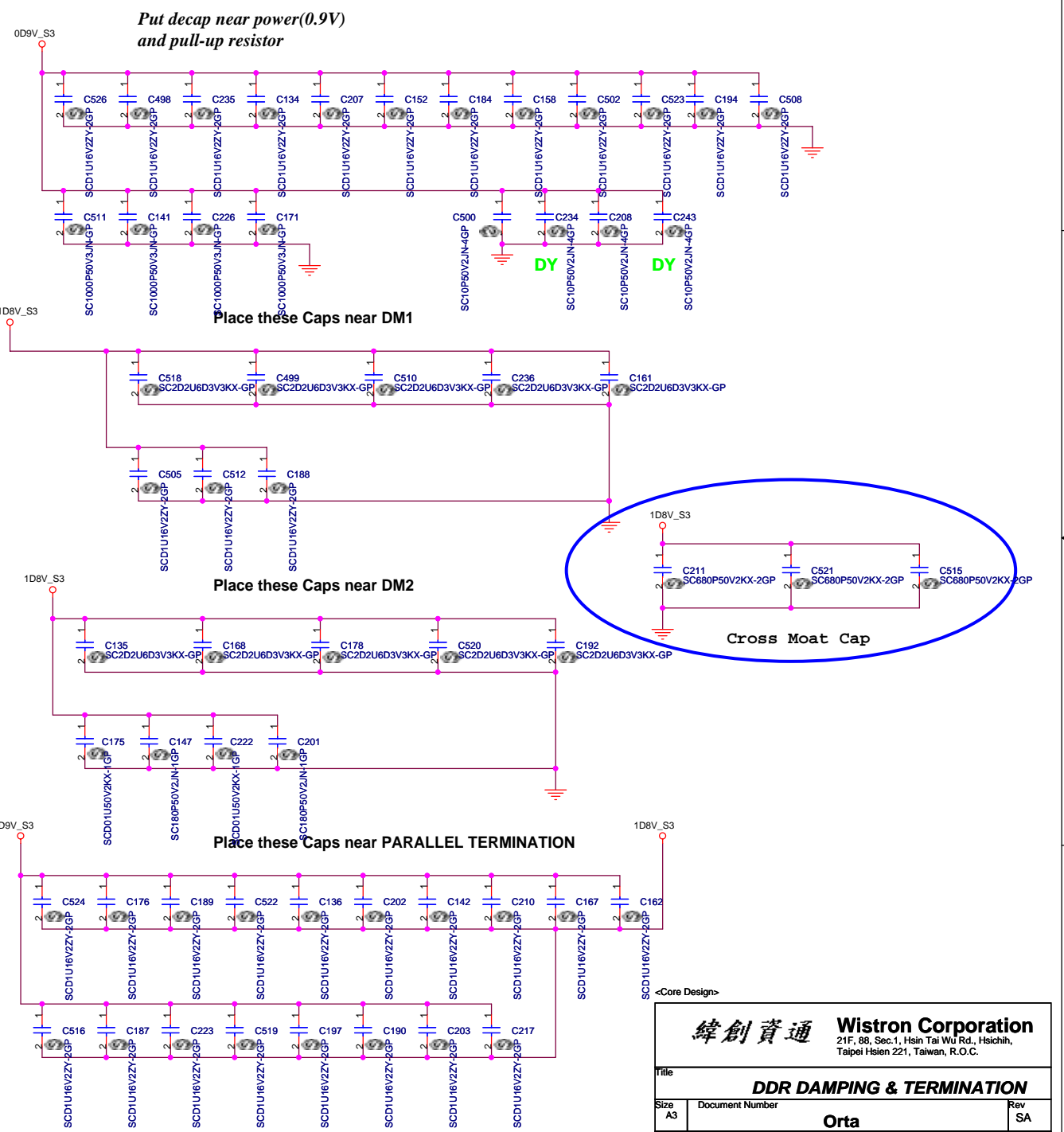
Title: **CPU(4/4)_Power**

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PARALLEL TERMINATION



Decoupling Capacitor

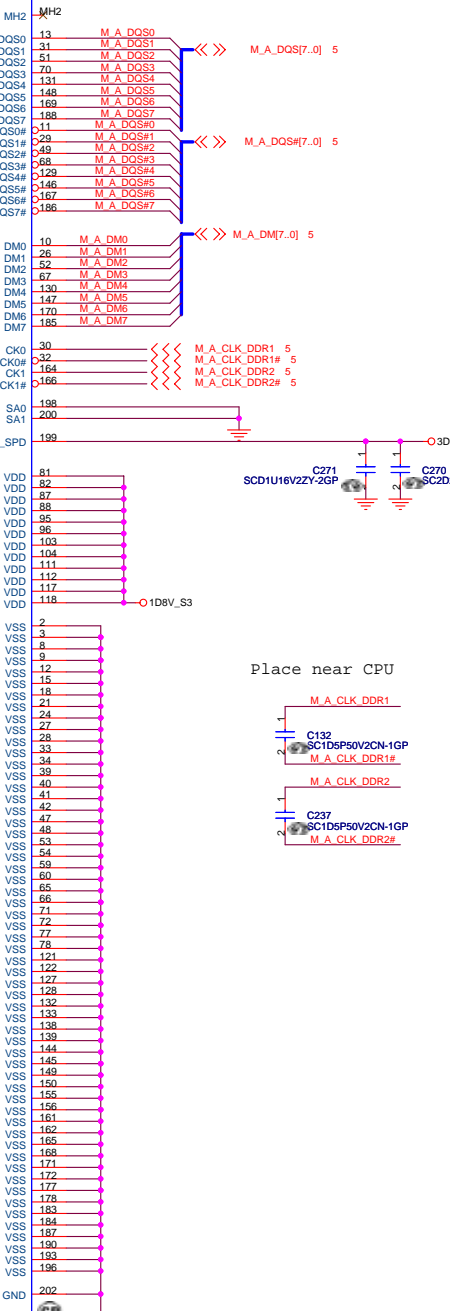
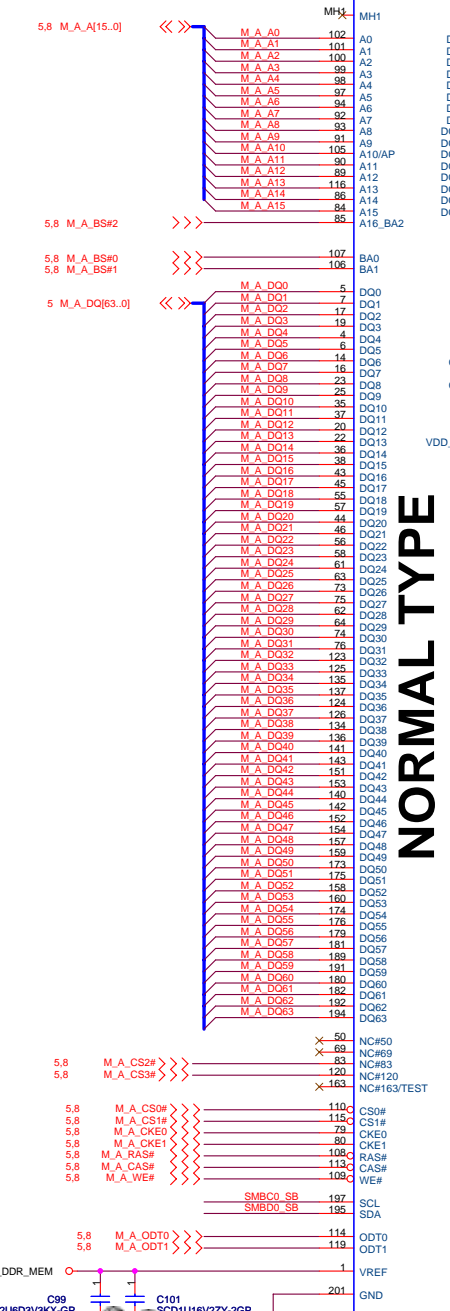
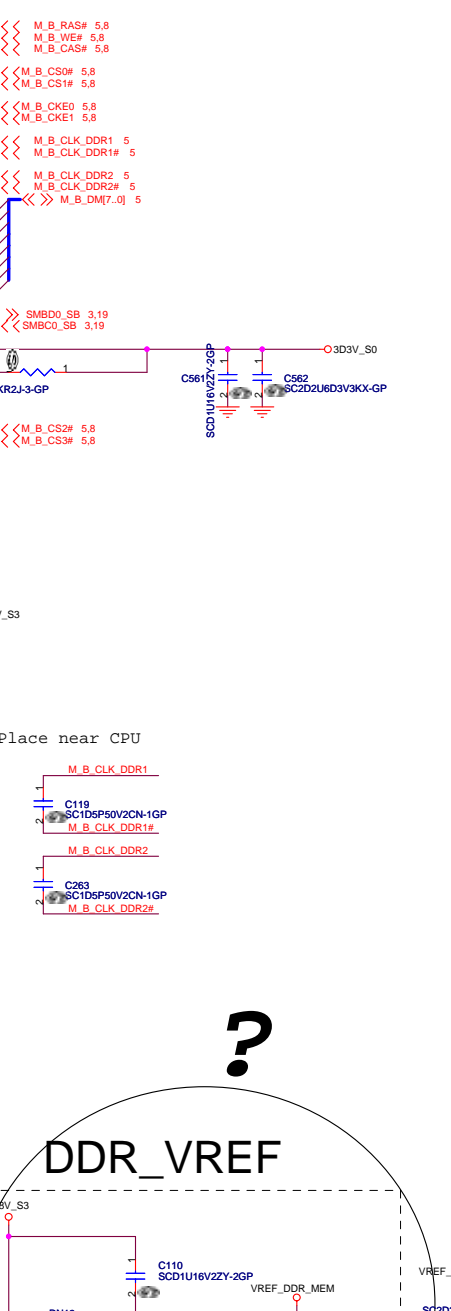
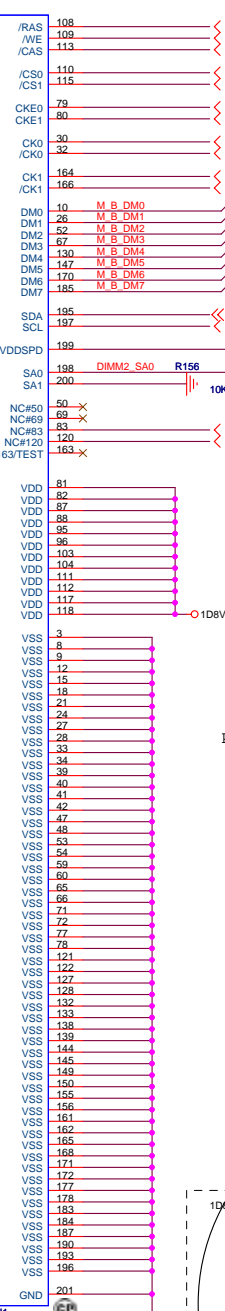
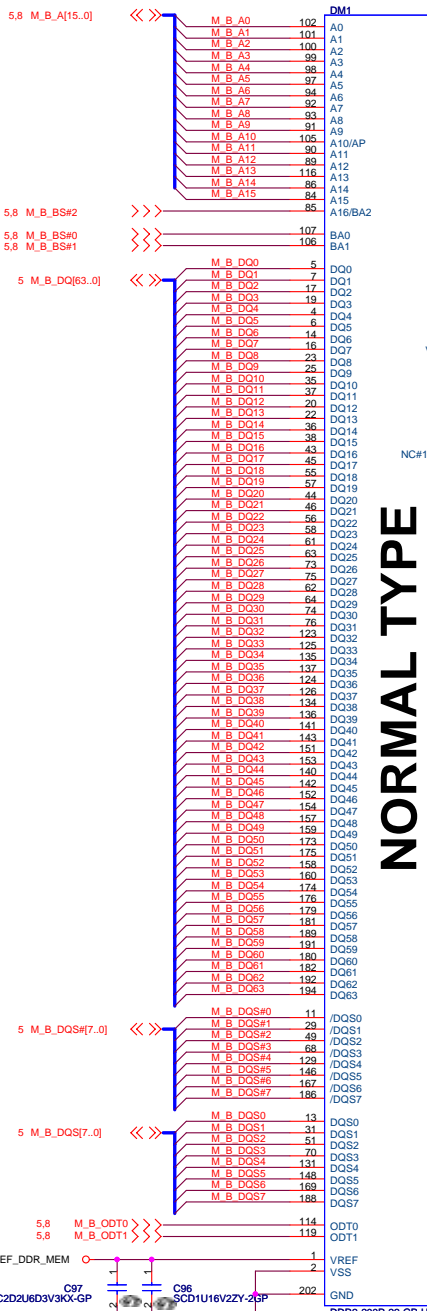


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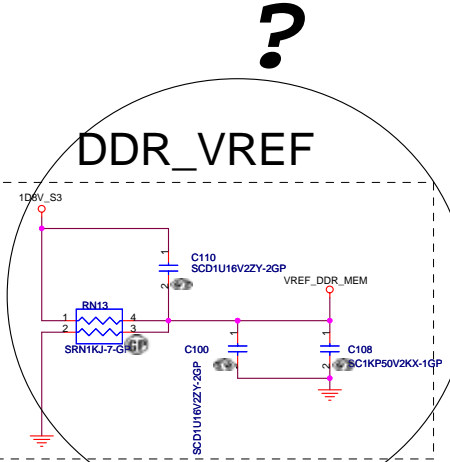
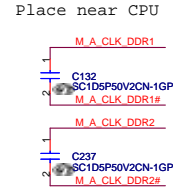
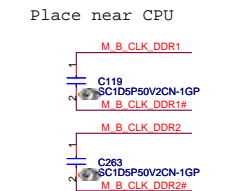
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DDR DAMPING & TERMINATION		
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NORMAL TYPE

NORMAL TYPE



62.10017.A61

High 9.2mm

62.10017.661

Hi 9.2mm High 5.2mm

Main Source: 62.10017.A61

LAYOUT: Locate close to DIMM

<Core Design>

Wistron Corporation

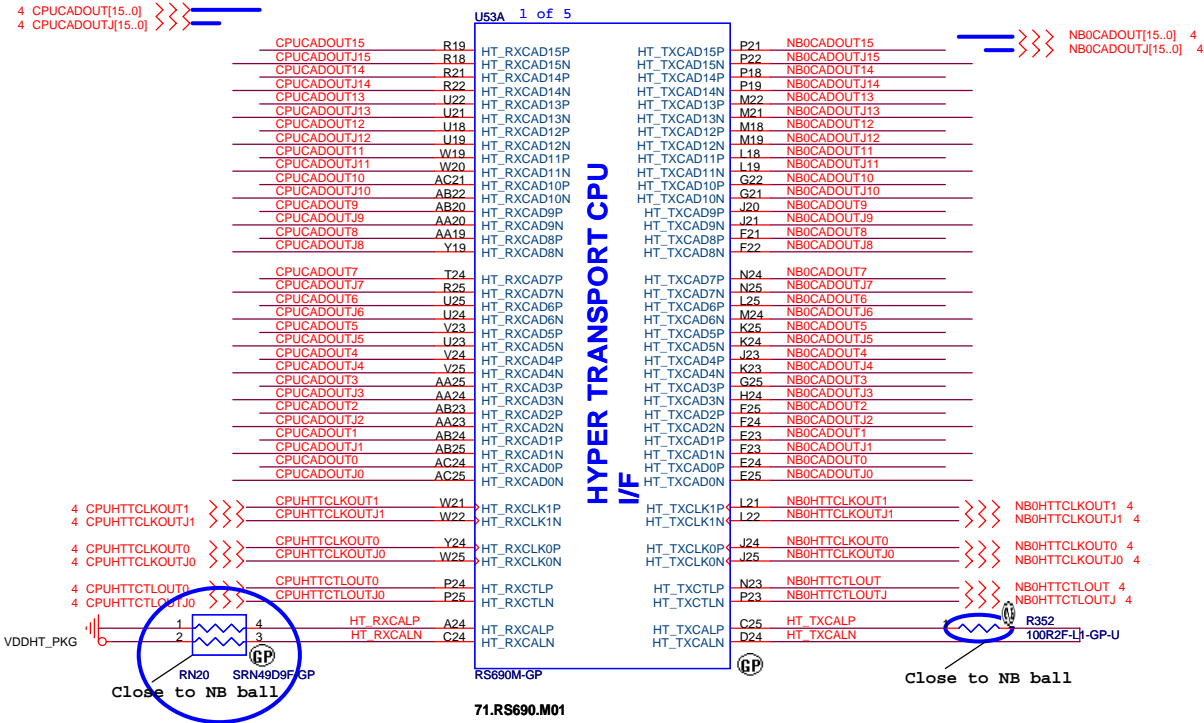
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DDR SO-DIMM SKT

File	Document Number	Rev
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CLAW HAMMER TO NB

NB TO CLAW HAMMER

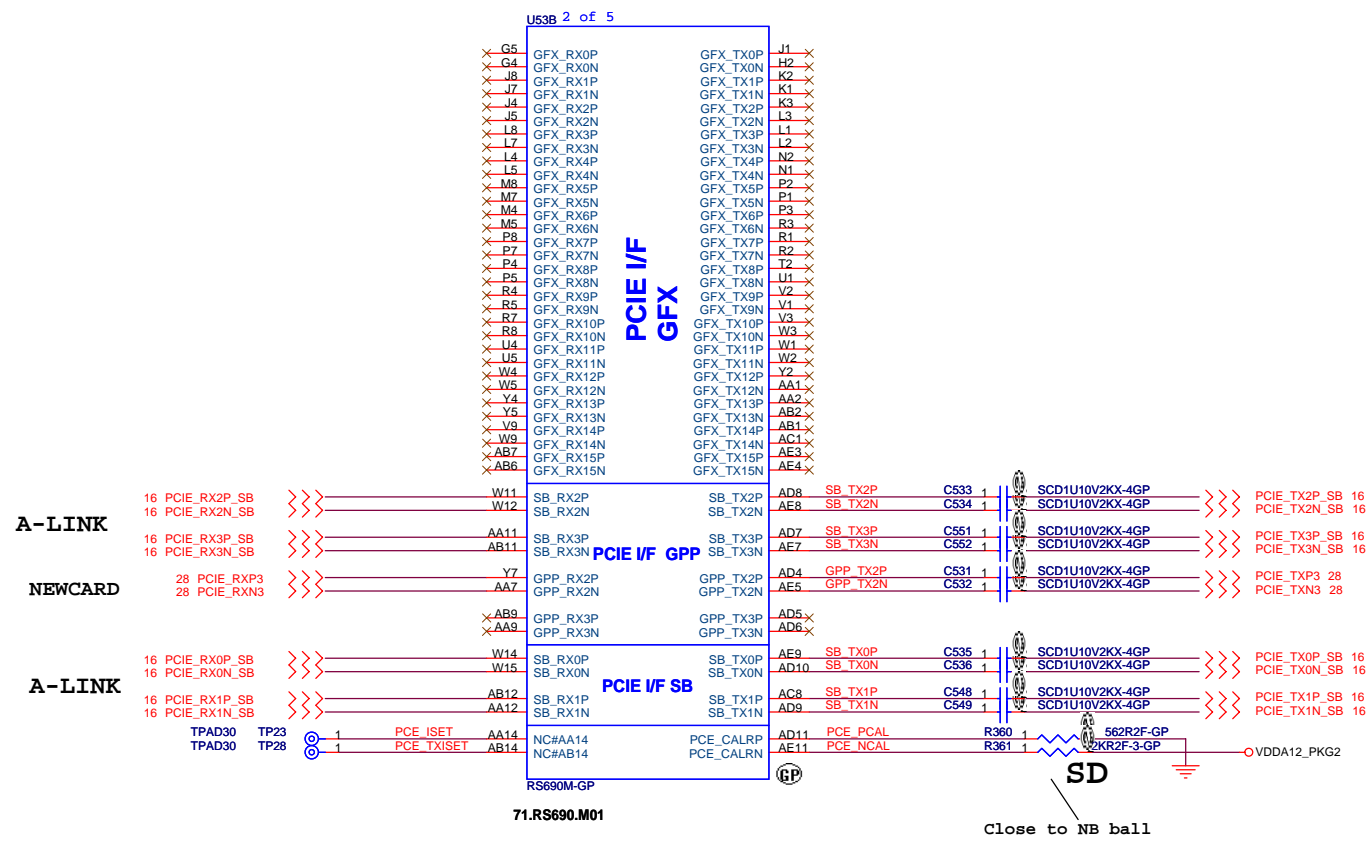


<Core Design>

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Title: **NB-RS690M HT**

Size: A3	Document Number: Orta	Rev: SA
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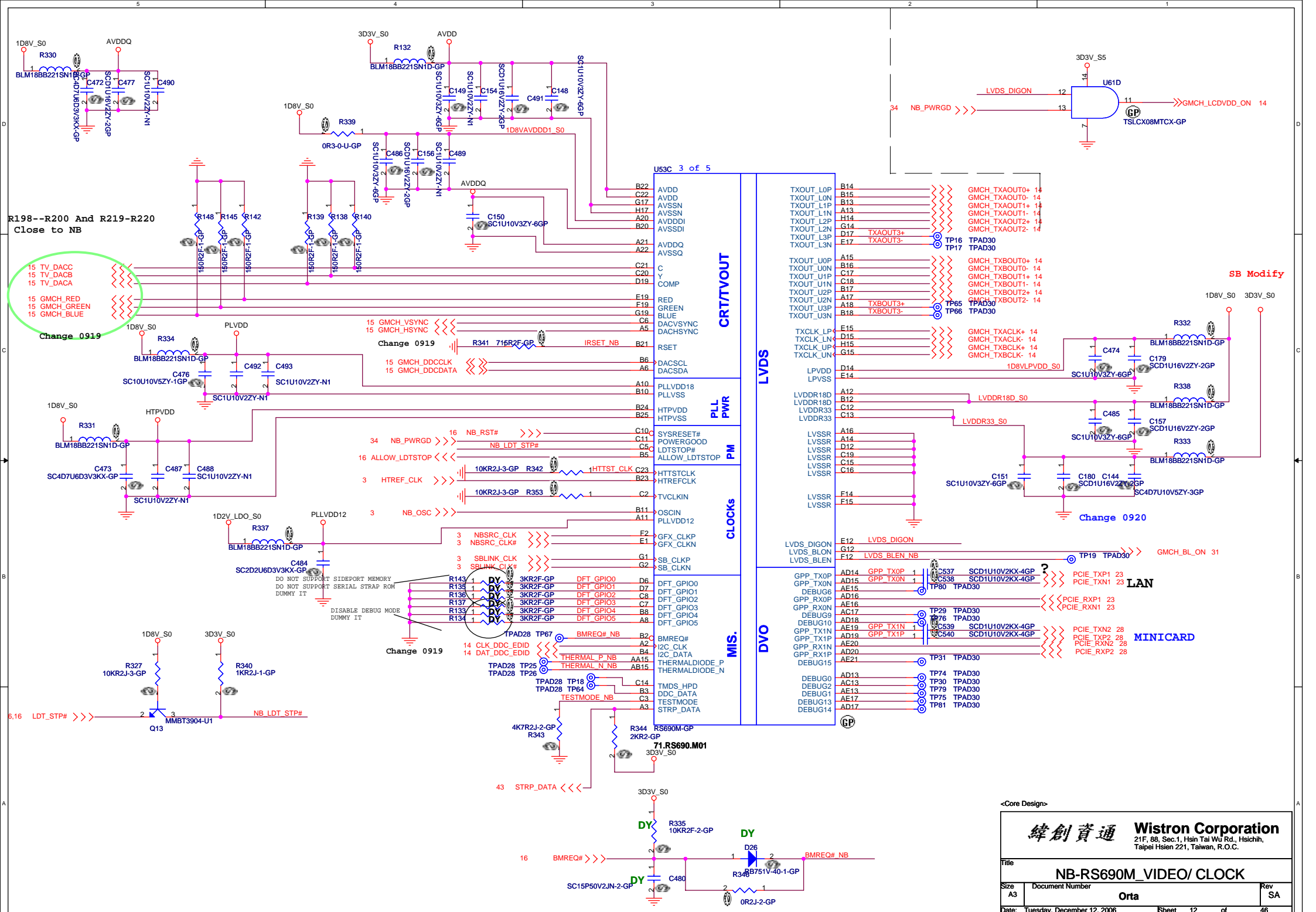


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Title: **NB-RS690M_MEM/PCIE_LINK I/F**

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R198--R200 And R219-R220
Close to NB

- 15 TV_DACB
- 15 TV_DACB
- 15 TV_DACA

Change 0919

6.16 LDT_STP# >>>

Change 0919

Change 0919

Change 0919

DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT

DISABLE DEBUG MODE
DUMMY IT

U53C 3 of 5

CRTC/VOUT

PLL PWR

PM

CLOCKS

MIS.

LVDS

DVO

- B22 AVDD
- C22 AVDD
- G17 AVSSN
- H17 AVSSN
- A20 AVSSN
- B20 AVSSDI
- A21 AVDDQ
- A22 AVSSQ
- C21 C
- C20 Y
- D19 COMP
- F19 RED
- G19 GREEN
- C6 DACVSYNC
- A5 DACHSYNC
- B21 RSET
- B6 DACSCL
- A6 DACSDA
- A10 PLLVDD18
- B10 PLLVSS
- B24 HTPVDD
- B25 HTPVSS
- C10C SYSRESET#
- C11 POWERGOOD
- C5C LDTSTOP#
- B5C ALLOW_LDTSTOP
- C23 HTTSTCLK
- B23 HTREFCLK
- C2 TVCLKIN
- B11 OSCIN
- A11 PLLVDD12
- F2 GFX_CLKP
- E1 GFX_CLKN
- G1 SB_CLKP
- G2 SB_CLKN
- D6 DFT_GPIO0
- D7 DFT_GPIO1
- C8 DFT_GPIO2
- C7 DFT_GPIO3
- B8 DFT_GPIO4
- A8 DFT_GPIO5
- B2C BMREQ#
- A2 I2C_CLK
- B4 I2C_DATA
- AA15 THERMALDIODE_P
- AB15 THERMALDIODE_N
- C14 TMD5_HPD
- B3 DDC_DATA
- C3 TESTMODE
- A3 STRP_DATA

- B14 GMCH_TXAOUT0+ 14
- B15 GMCH_TXAOUT0- 14
- B13 GMCH_TXAOUT1+ 14
- A13 GMCH_TXAOUT1- 14
- H14 GMCH_TXAOUT2+ 14
- G14 GMCH_TXAOUT2- 14
- D17 TXAOUT3+
- E17 TXAOUT3-
- A15 GMCH_TXBOUT0+ 14
- B16 GMCH_TXBOUT0- 14
- C17 GMCH_TXBOUT1+ 14
- C18 GMCH_TXBOUT1- 14
- A17 GMCH_TXBOUT2+ 14
- A18 GMCH_TXBOUT2- 14
- B18 TXBOUT3+
- B18 TXBOUT3-
- E15 GMCH_TXACLK+ 14
- D15 GMCH_TXACLK- 14
- H15 GMCH_TXBCLK+ 14
- G15 GMCH_TXBCLK- 14
- D14 LPVDD
- E14 LPVSS
- A12 LVDDR18D
- B12 LVDDR18D_S0
- C12 LVDDR33
- C13 LVDDR33_S0
- A16 LVSSR
- A14 LVSSR
- D12 LVSSR
- C19 LVSSR
- C15 LVSSR
- C16 LVSSR
- F14 LVSSR
- F15 LVSSR
- E12 LVDS DIGON
- G12 LVDS_BLEN
- F12 LVDS_BLEN_NB

- AD14 GPP_TX0P 1
- AD15 GPP_TX0N 1
- AE15 DEB06
- AD16 GPP_RX0P
- AE16 DEB06
- AC17 GPP_RX0N
- AD18 DEB09
- AE19 GPP_TX1N 1
- AD19 GPP_TX1P 1
- AD20 GPP_RX1N
- AE21 DEB09
- AD13 DEB00
- AC13 DEB00
- AE13 DEB01
- AE17 DEB01
- AD17 DEB01

- AD14 PCIE_TXP1 23
- AD15 PCIE_TXN1 23
- AE15 PCIE_RXP1 23
- AE16 PCIE_RXN1 23
- AD19 PCIE_TXN2 28
- AD19 PCIE_TXP2 28
- AD20 PCIE_RXN2 28
- AE21 PCIE_RXP2 28
- TP29 TPAD30
- TP30 TPAD30
- TP31 TPAD30
- TP74 TPAD30
- TP30 TPAD30
- TP75 TPAD30
- TP81 TPAD30



SB Modify

Change 0920

GMCH_BL_ON 31

LAN

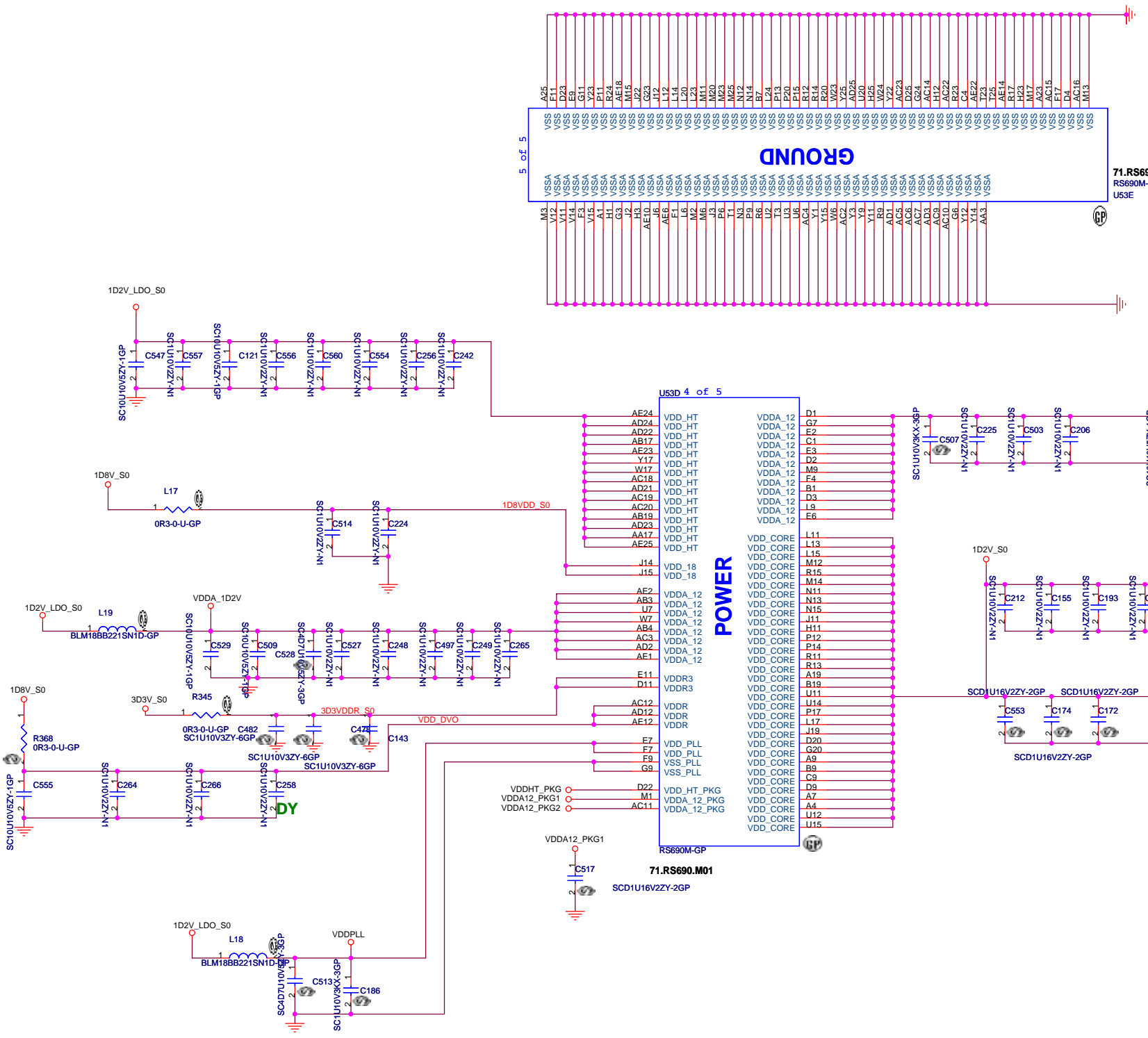
MINICARD

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **NB-RS690_VIDEO/ CLOCK**

Size: A3	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet: 12	of: 46



5 of 5

U53D 4 of 5

POWER

GROUND

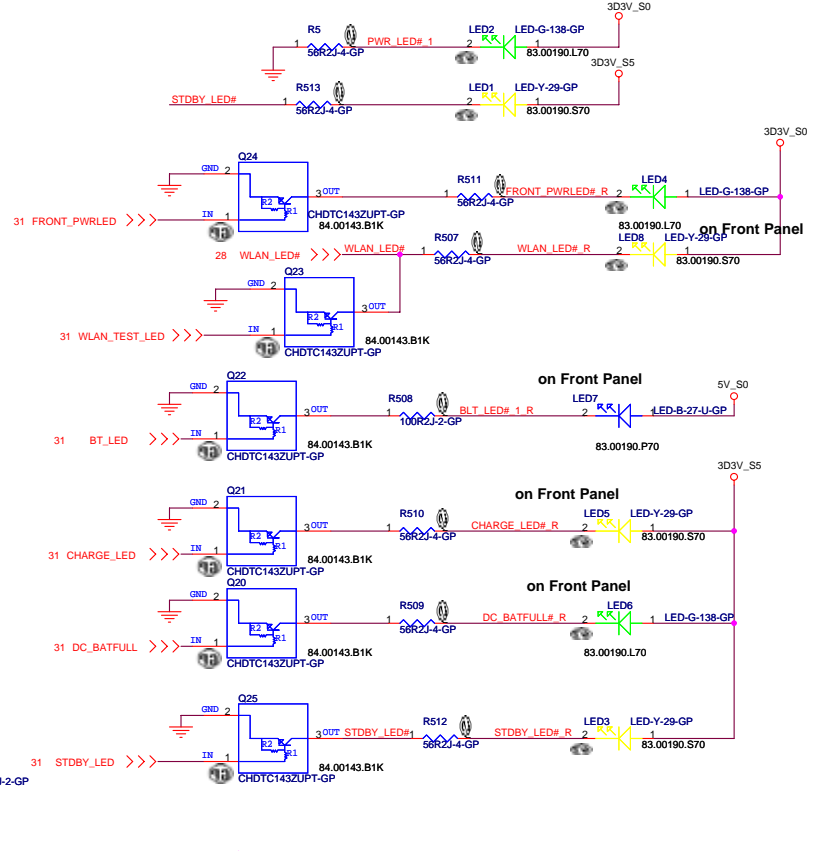
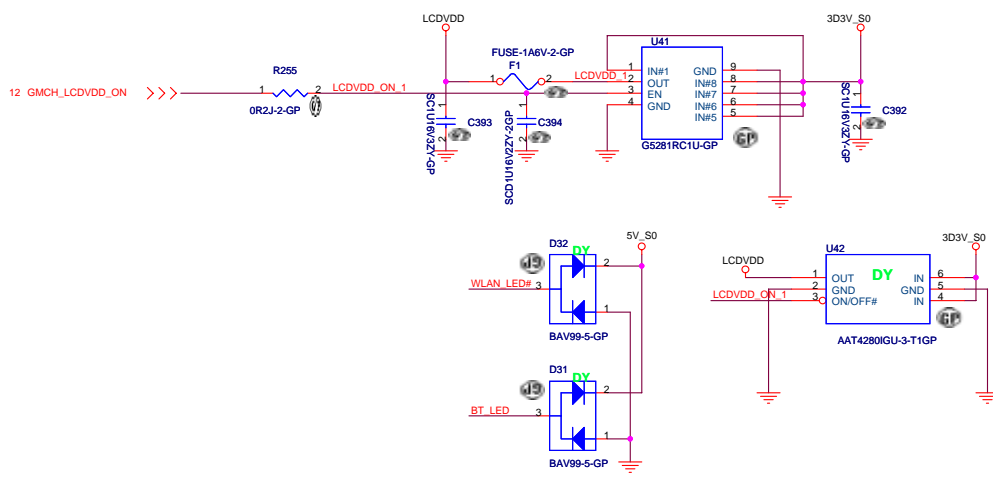
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RS690M-GP
U53E

71.RS690.M01
SCD1U16V2ZY-2GP

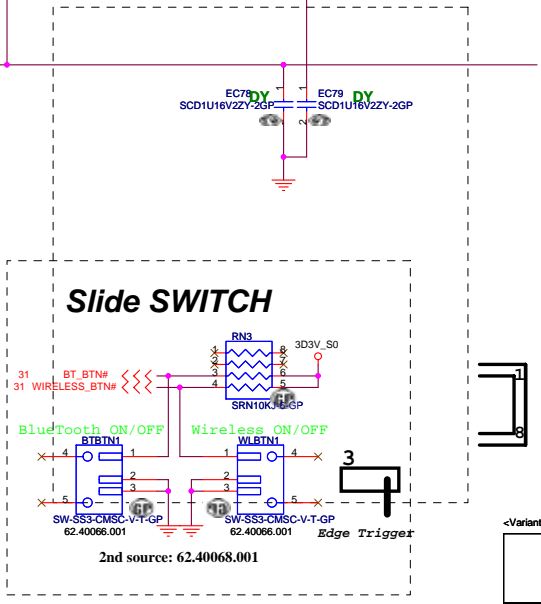
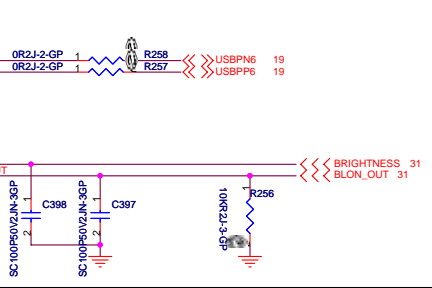
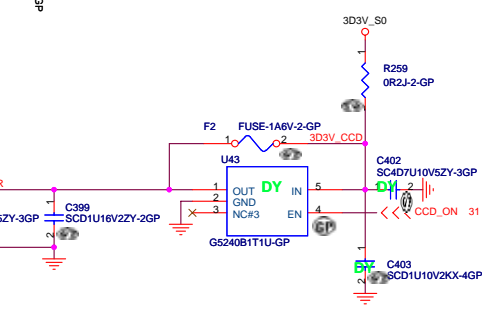
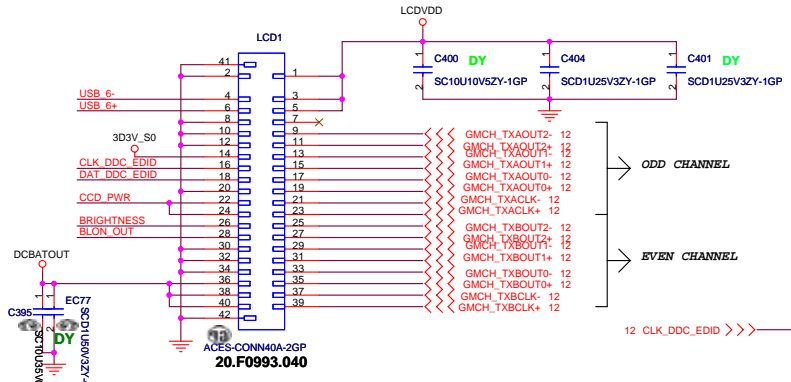
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

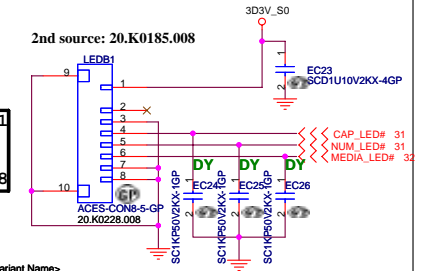
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Size	Document Number	Rev	
A3		Orta	SA
Date:	Tuesday, December 12, 2006	Sheet	13 of 46



LCD/INVERTER CONN

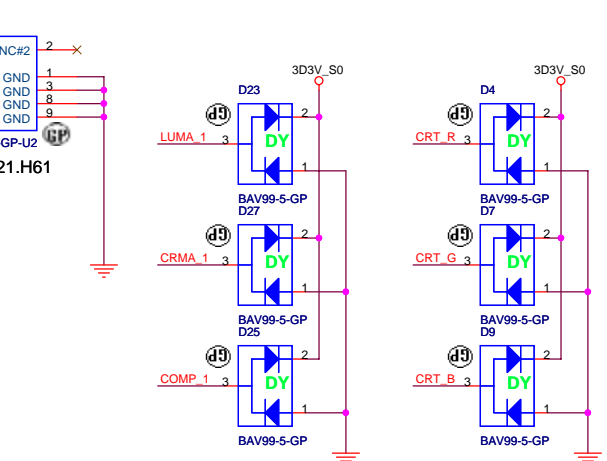
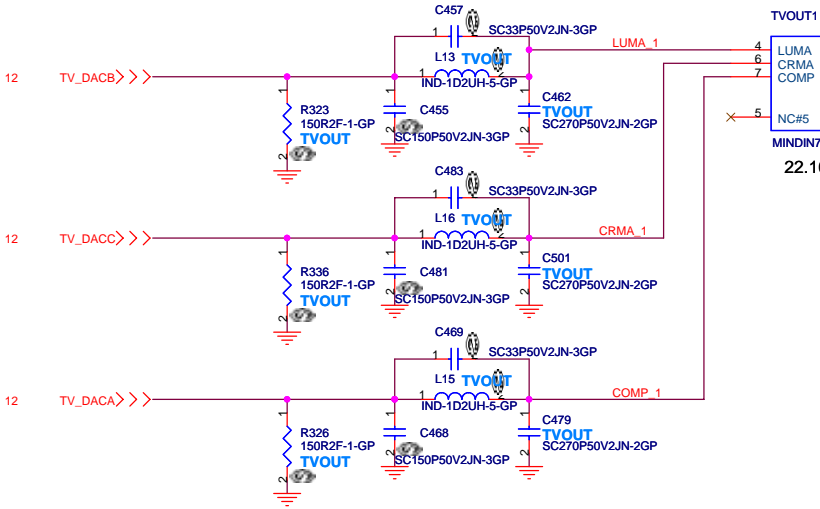
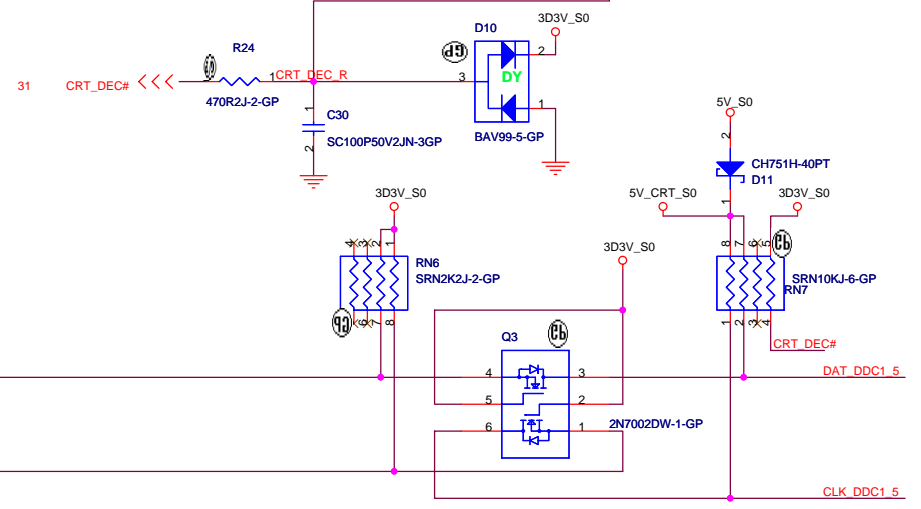
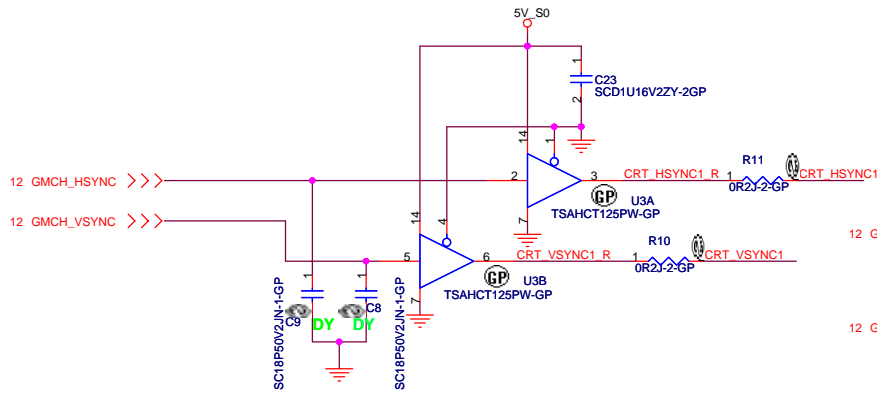
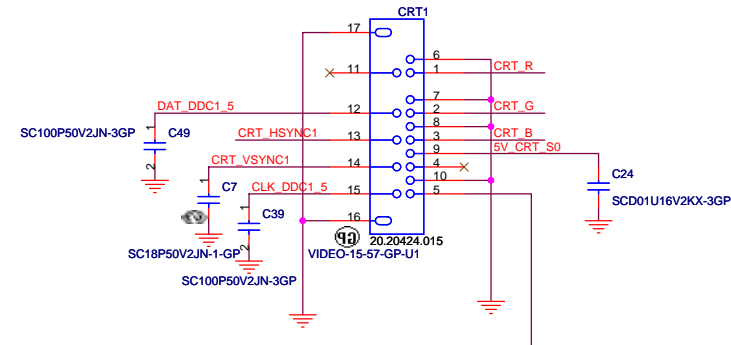
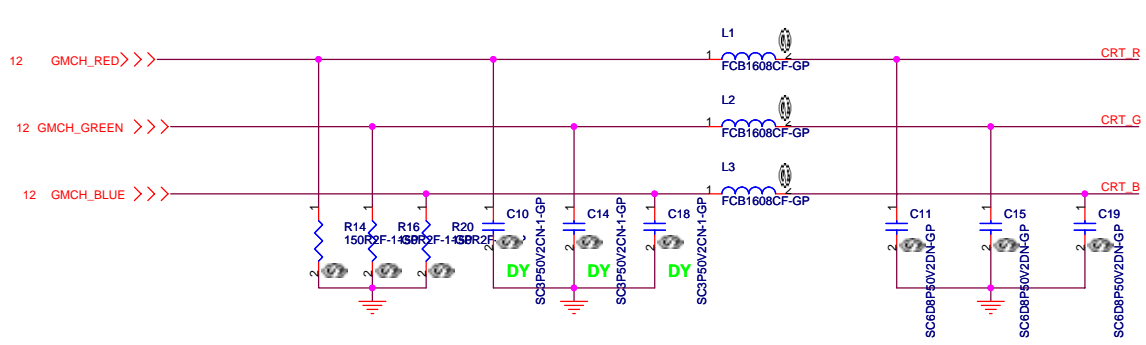


LED BD



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Heien 221, Taiwan, R.O.C.

File: LCD CONN & LED
Size: Document Number: Orta
Date: Tuesday, December 12, 2006 Sheet 14 of 46



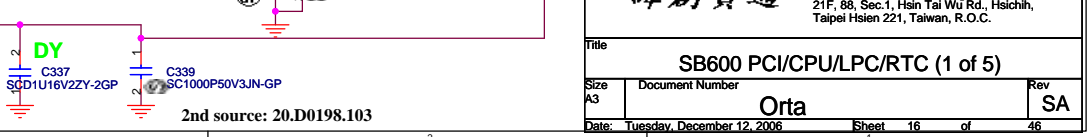
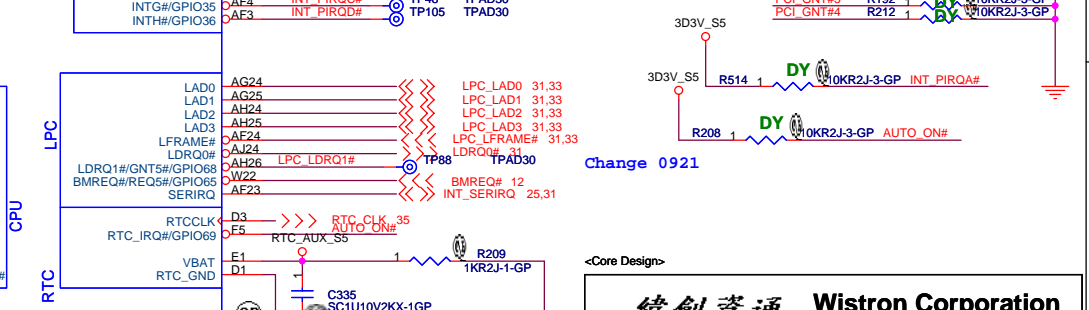
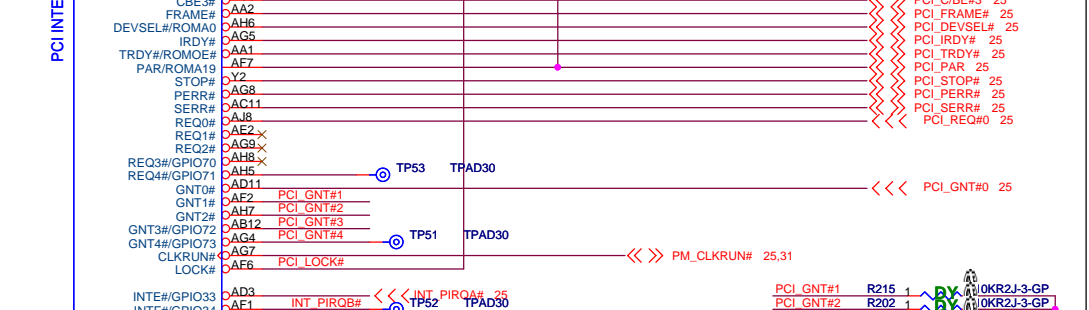
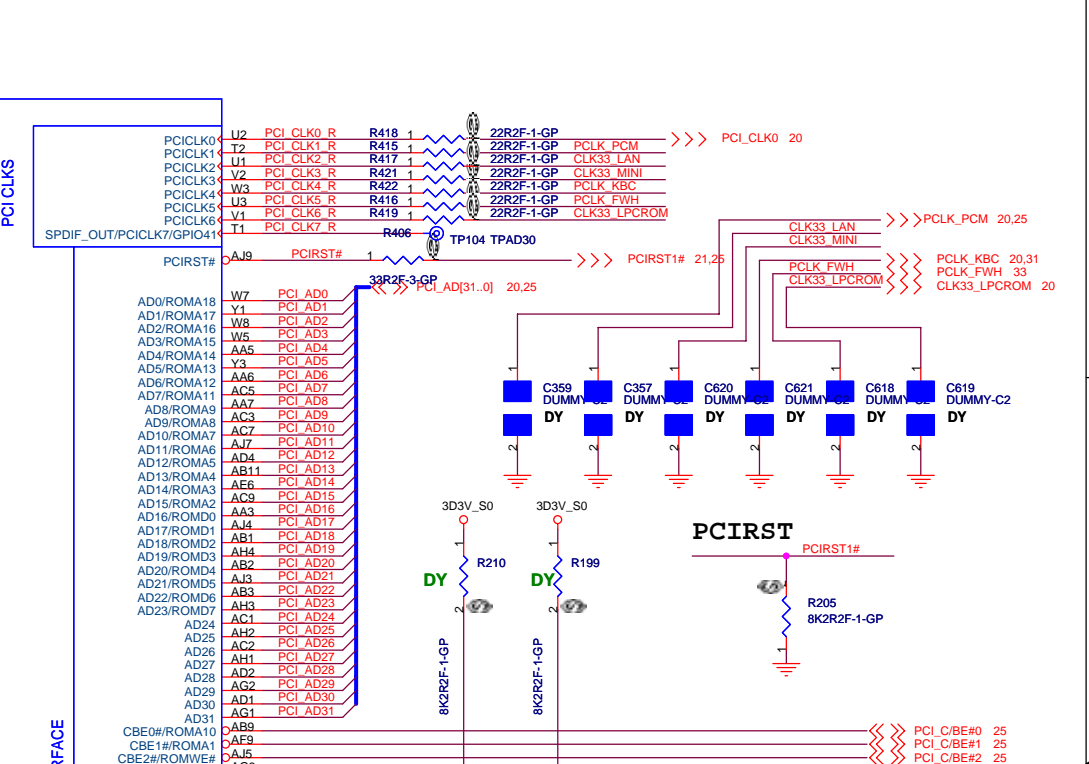
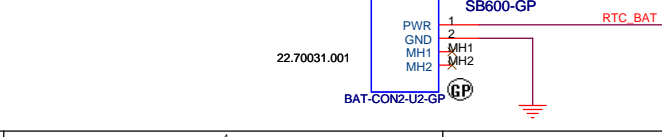
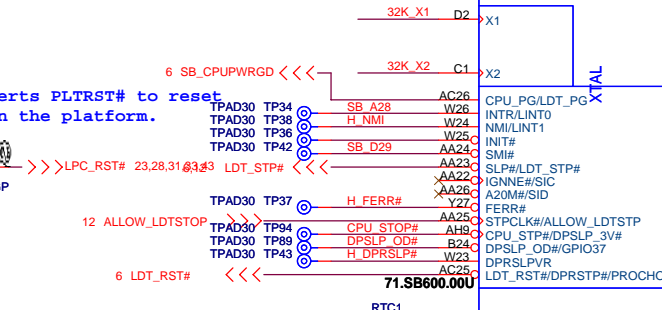
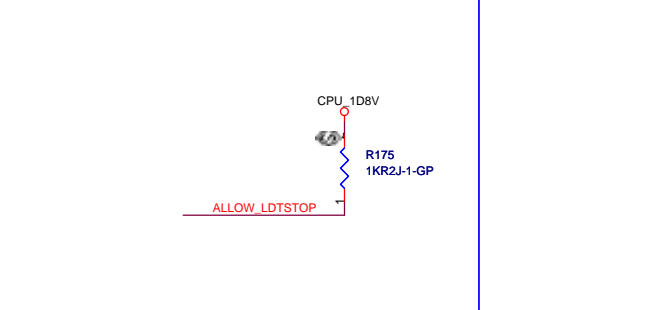
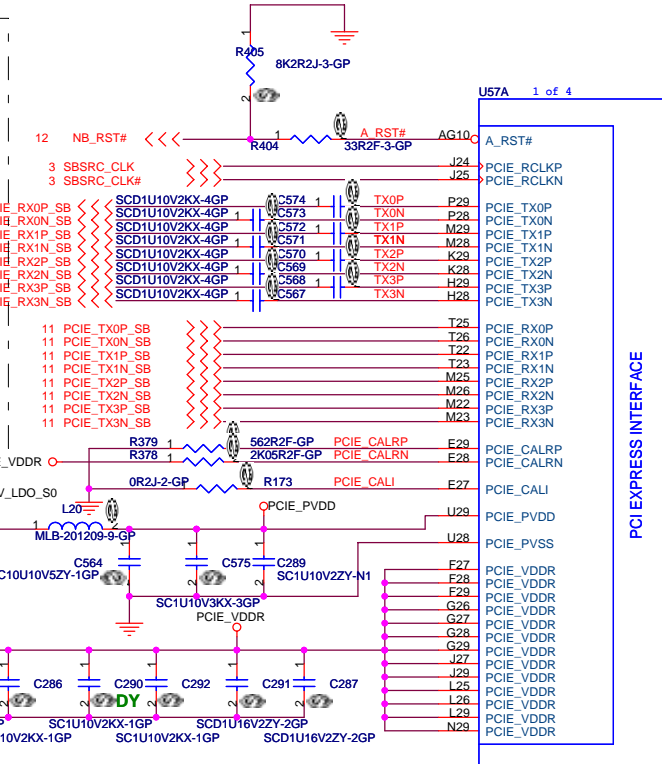
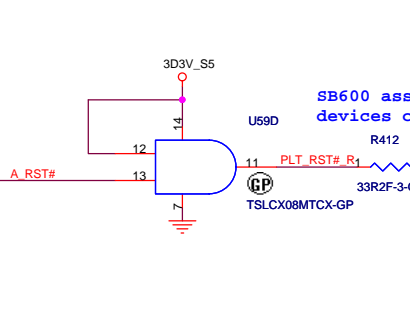
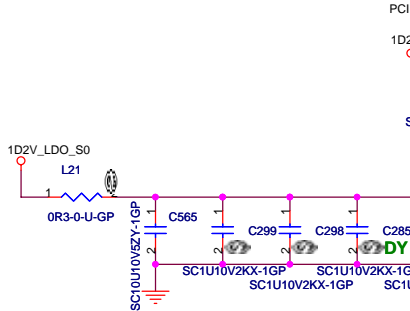
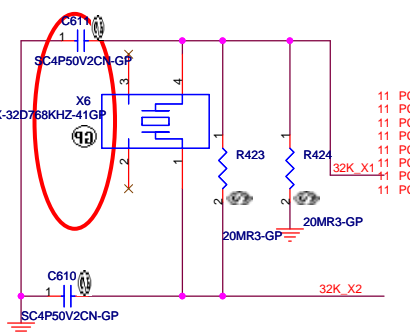
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV Connector**

Size: _____ Document Number: _____ Rev: SA

Date: Tuesday, December 12, 2006 Sheet 15 of 46

Place these components close to U13 and use ground guard for 32K_X1 and 32K_X2.



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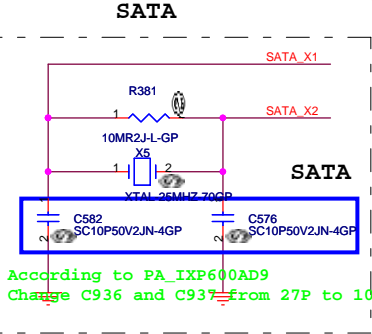
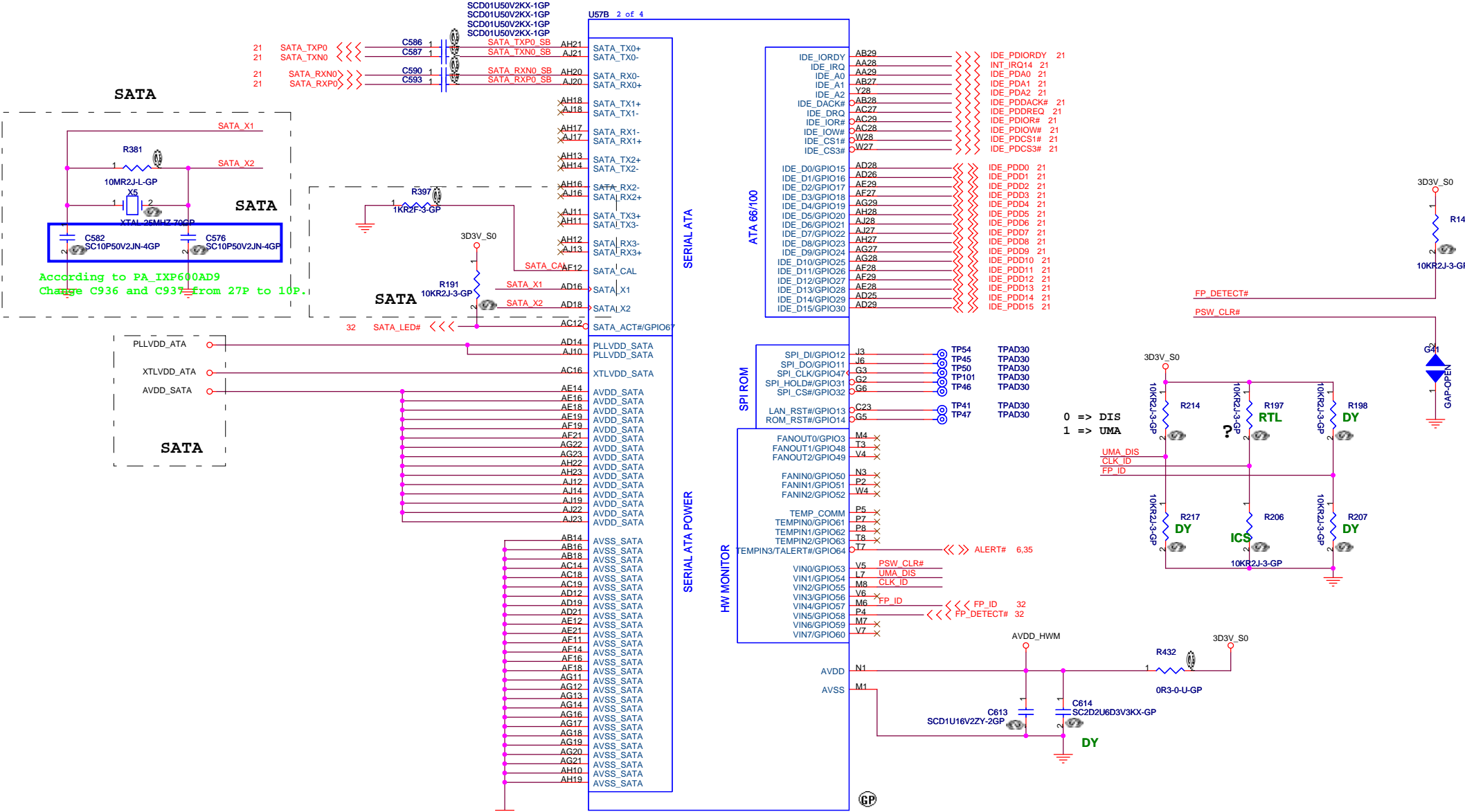
Title: **SB600 PCI/CPU/LPC/RTC (1 of 5)**

Size: A3 Document Number: Orta Rev: SA

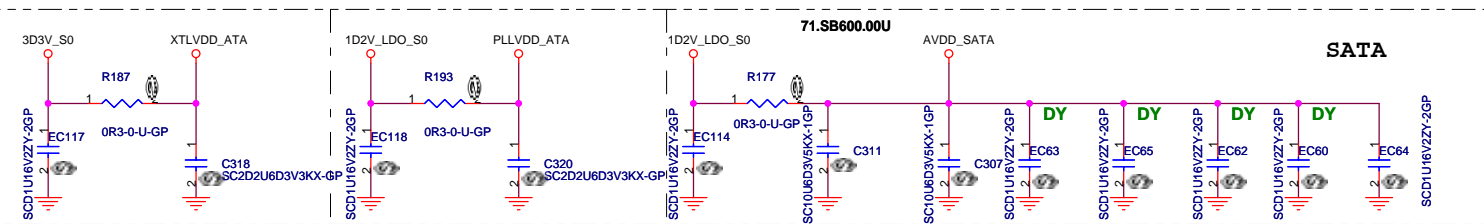
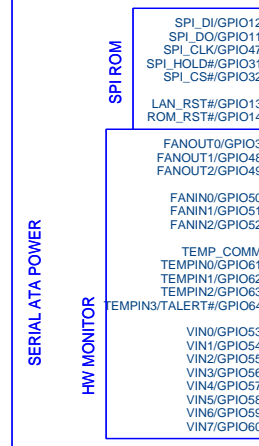
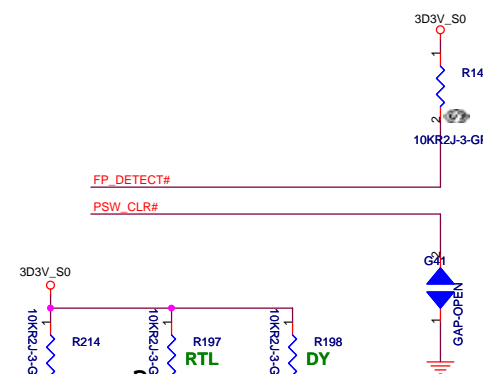
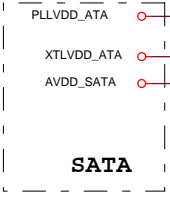
Date: Tuesday, December 12, 2006 Sheet: 16 of 46

2nd source: 20.D0198.103

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB460



According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.



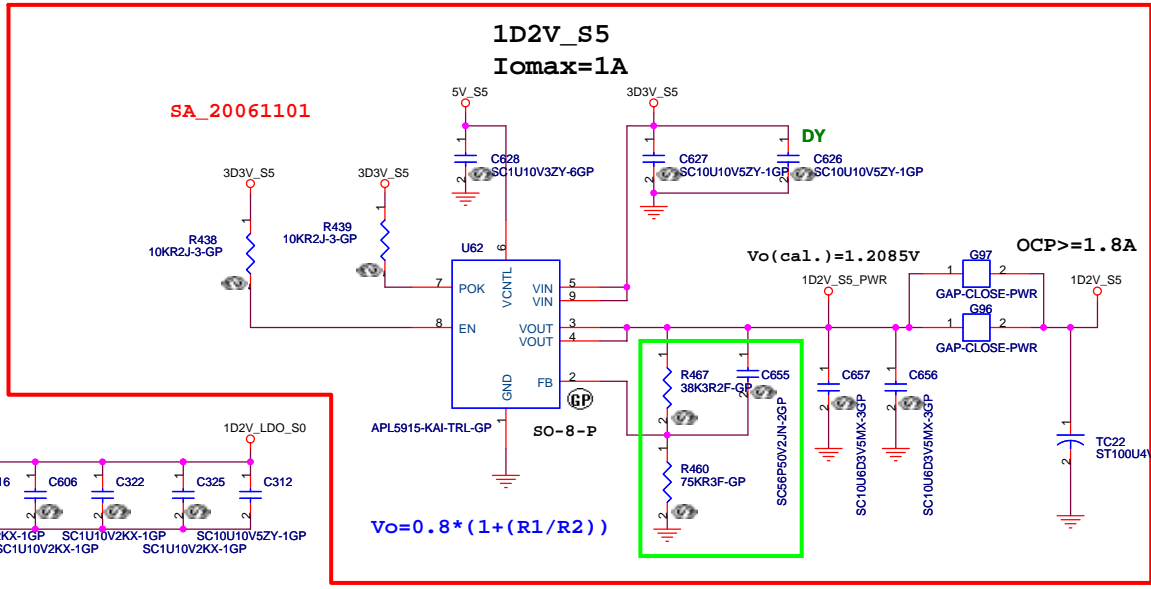
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

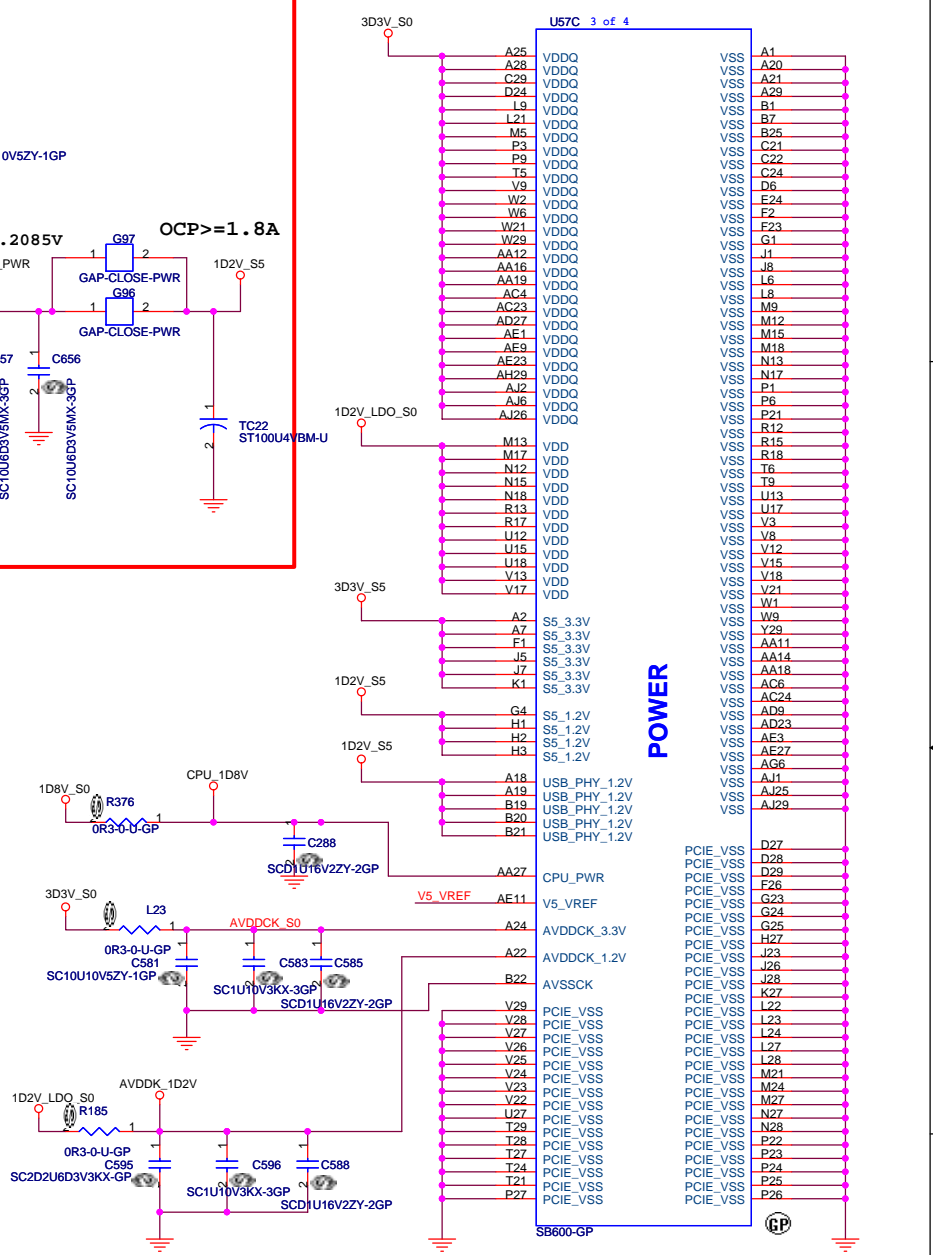
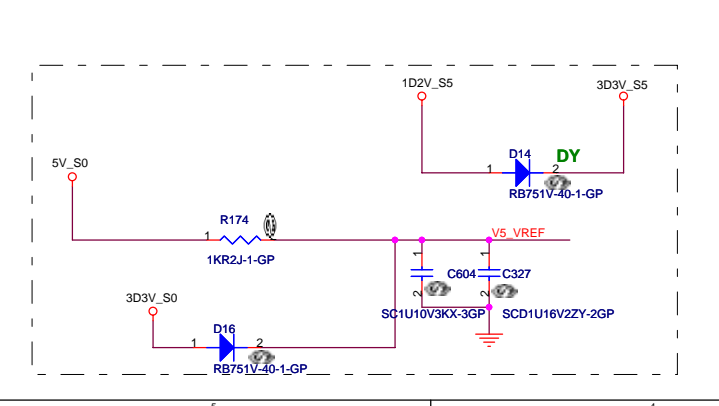
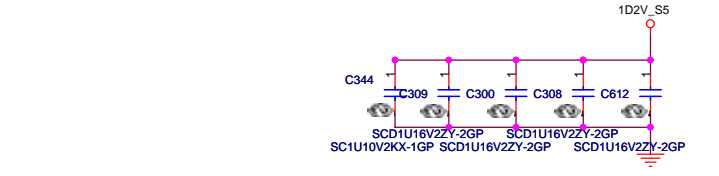
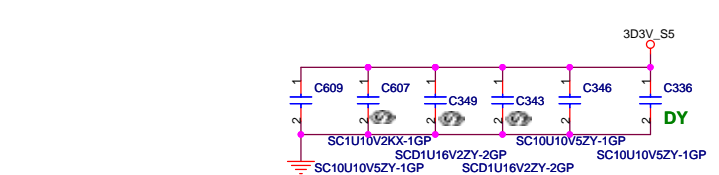
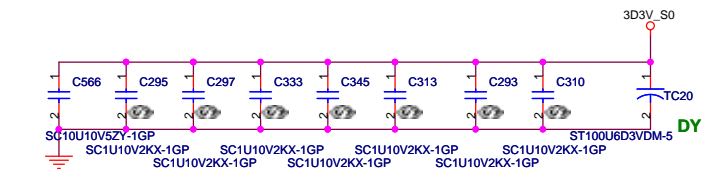
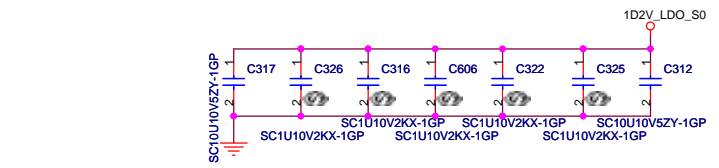
Title: **SB600 ACPI/GPIO/SATA/IDE (2 of 5)**

Size A3 Document Number **Orta** Rev **SA**

Date: Tuesday, December 12, 2006 Sheet 17 of 46



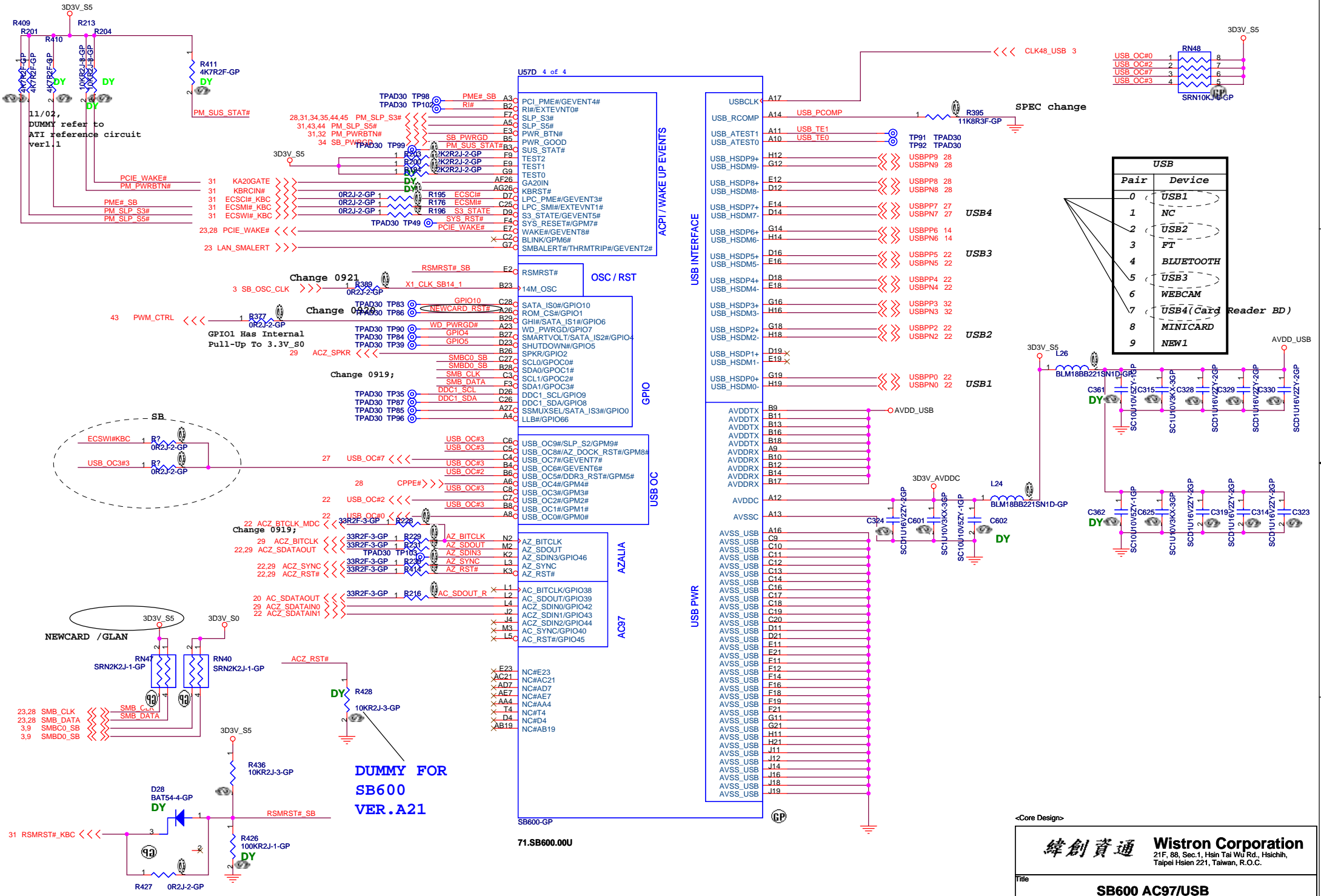
Place near to SB600



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			SB600 POWER/DECOUPLING		
Size	Document Number		Rev		SA
A3	Orta				
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USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	FT
4	BLUETOOTH
5	USB3
6	WEBCAM
7	USB4 (Card Reader BD)
8	MINICARD
9	NEW1

<Core Design>

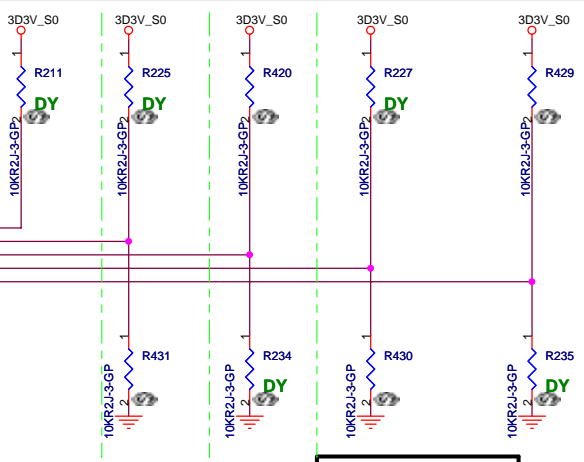
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 AC97/USB**

Size: A3 Document Number: Orta Rev: SA

Date: Tuesday, December 12, 2006 Sheet: 19 of 46

19 AC_SDATAOUT
 16,31 PCLK_KBC
 16,25 PCLK33_LPCROM
 16 PCI_CLK0
 16,25 PCLK_PCM

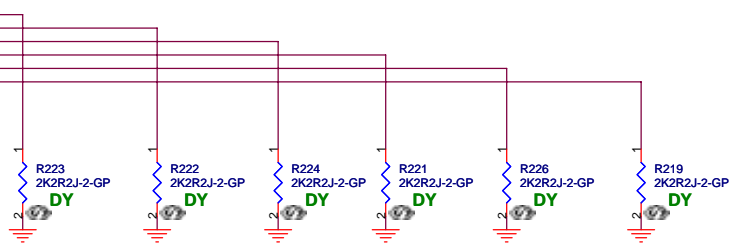


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDATAOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

16,25 PCI_AD28
 16,25 PCI_AD27
 16,25 PCI_AD26
 16,25 PCI_AD25
 16,25 PCI_AD24
 16,25 PCI_AD23



DEBUG STRAPS

STRAP HIGH	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT	
STRAP LOW			USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE	

<Core Design>

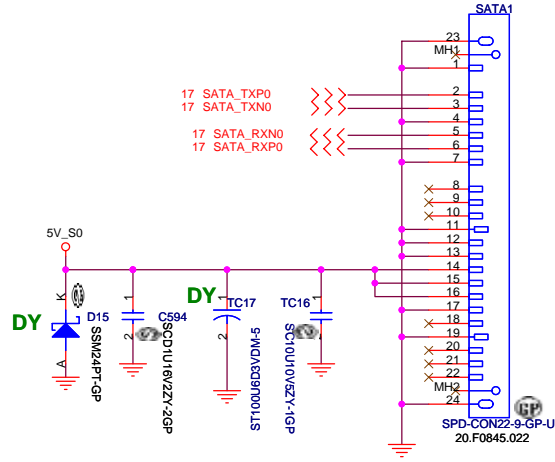
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 STRAPPING PIN**

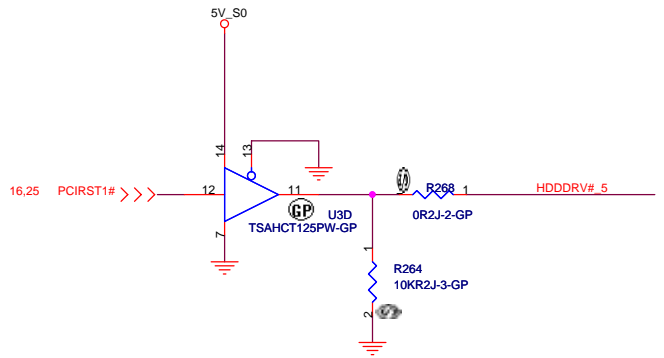
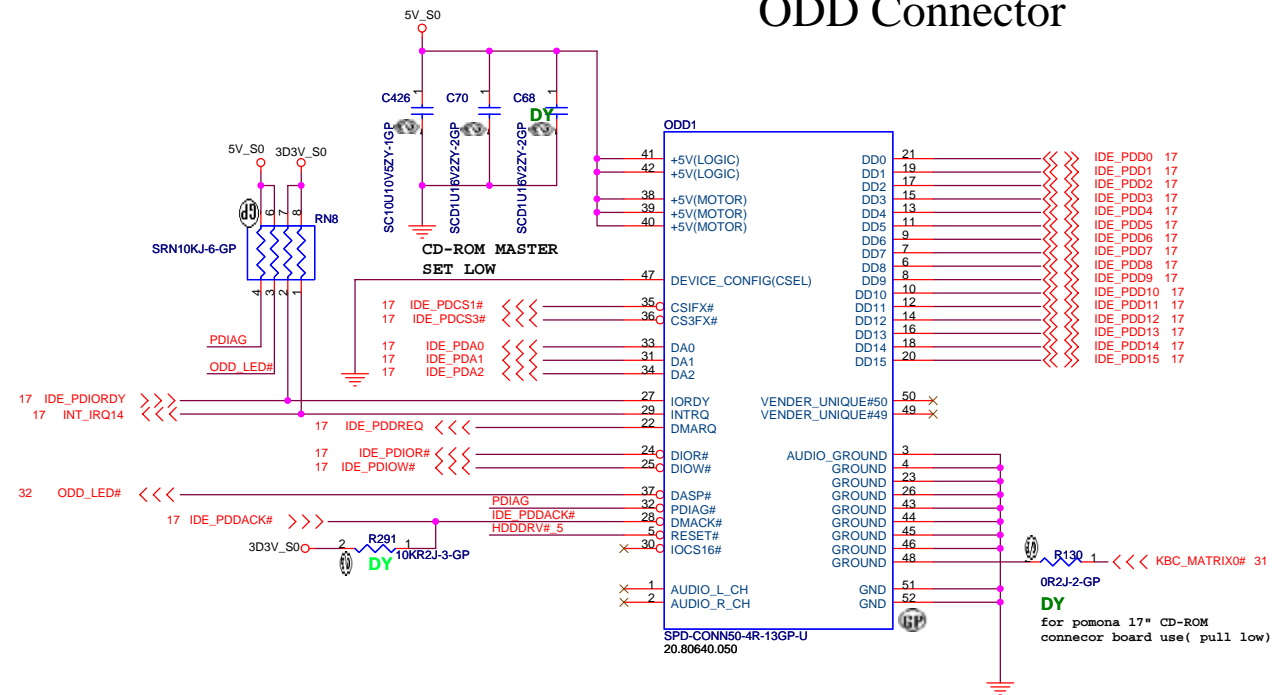
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Date: Tuesday, December 12, 2006 Sheet 20 of 46

SATA HD Connector

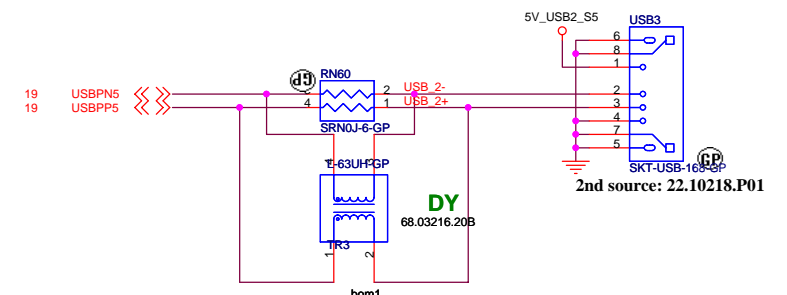
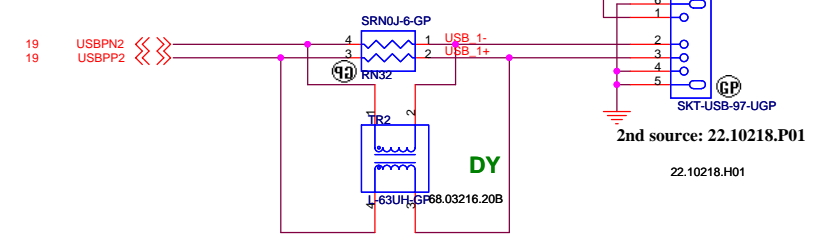
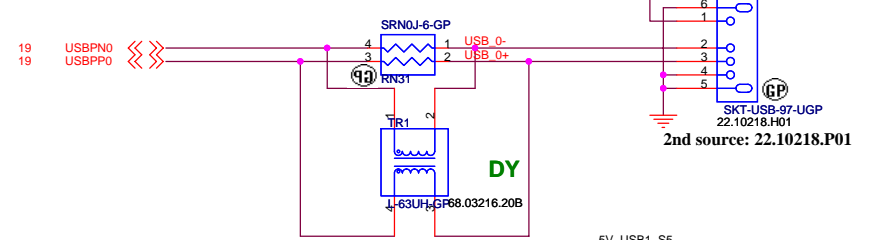
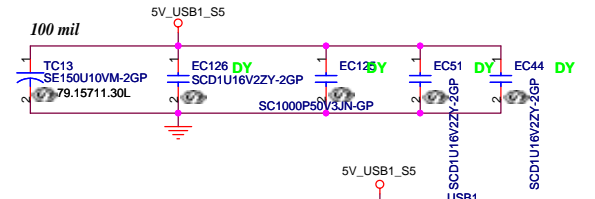
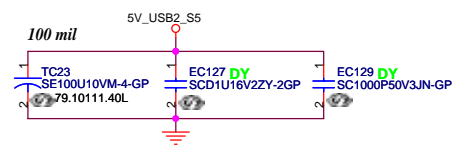
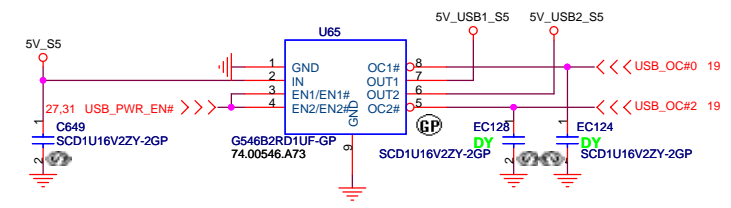


ODD Connector

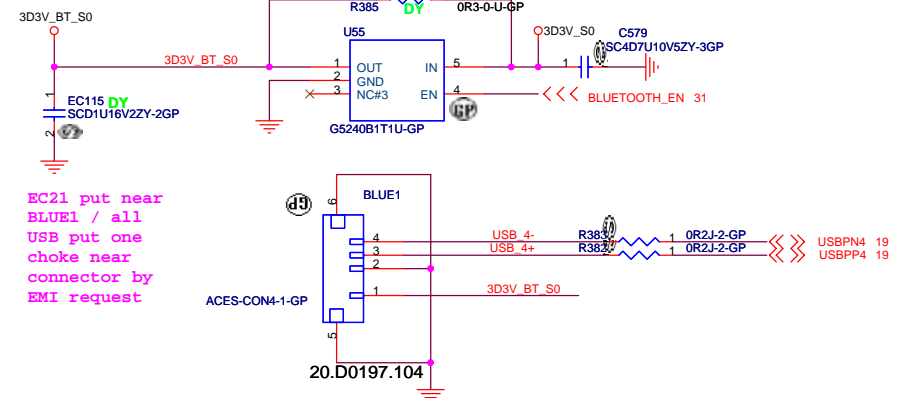


bom1

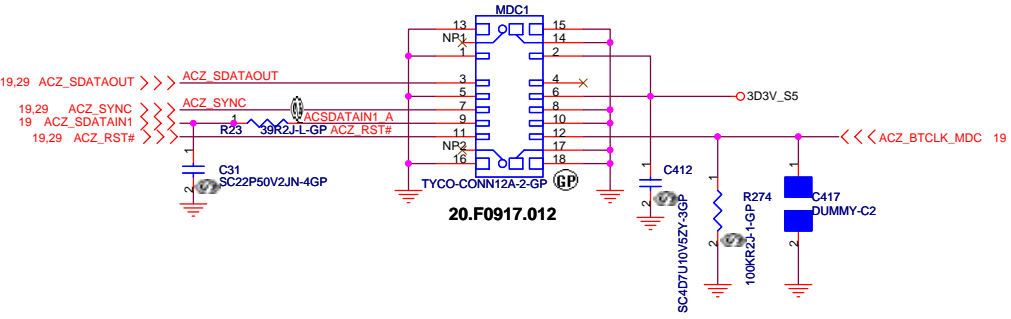
緯創資通		Wistron Corporation	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD and CDROM			
Size	Document Number	Rev	SA
Orta			
Date:	Tuesday, December 12, 2006	Sheet	21 of 46



BLUETOOTH MODULE



MDC 1.5 CONN



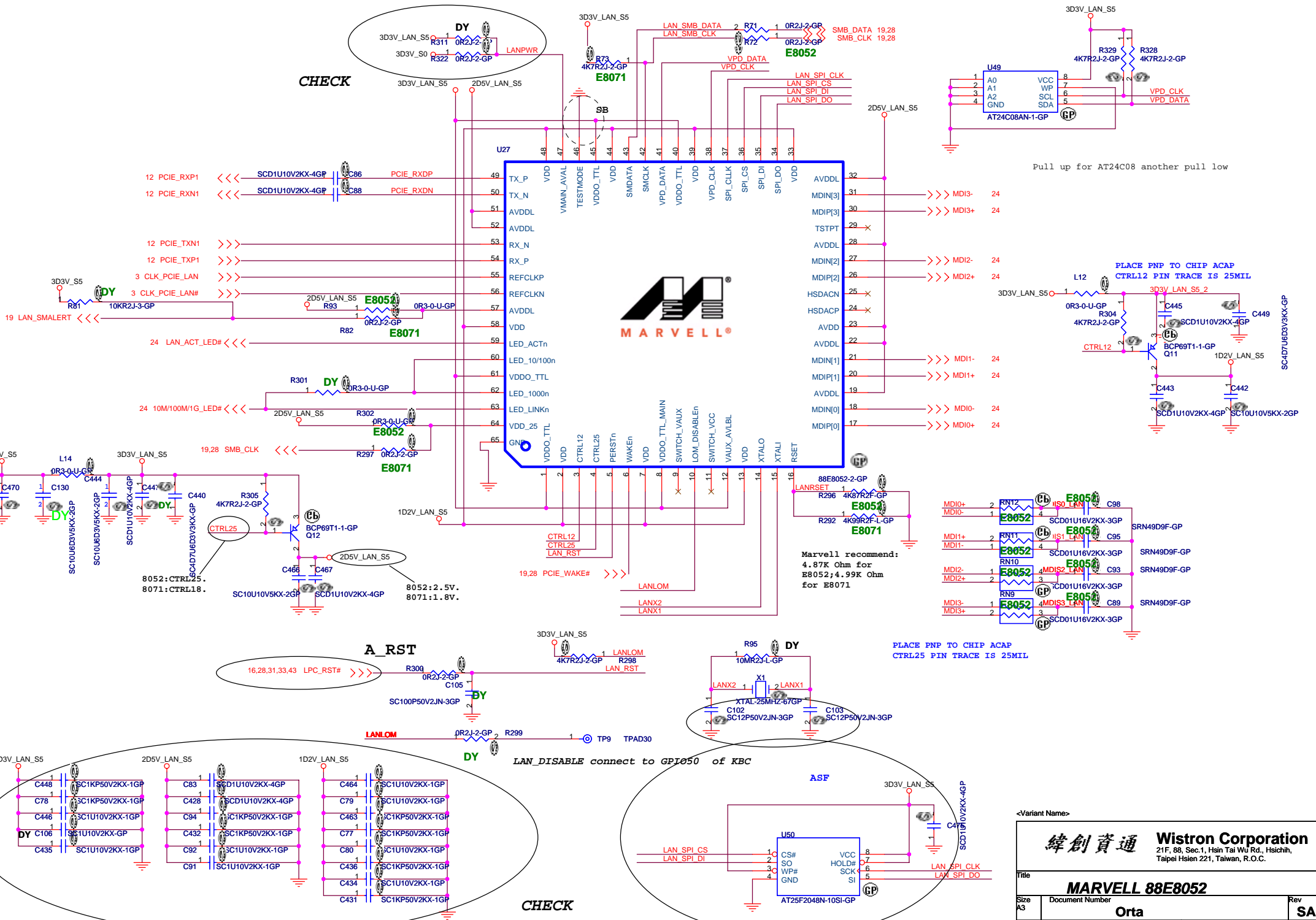
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **USB / MDC / BLUETOOTH**

Size: Document Number **Orta** Rev: SA

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CHECK



Pull up for AT24C08 another pull low

PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL

PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL

Marvell recommend:
4.87K Ohm for E8052; 4.99K Ohm for E8071

LAN_DISABLE connect to GPI050 of KBC

A_RST

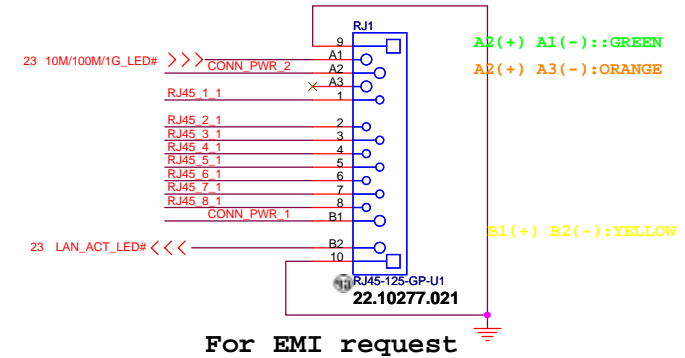
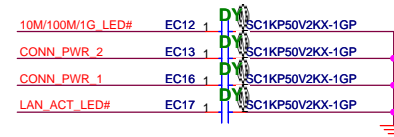
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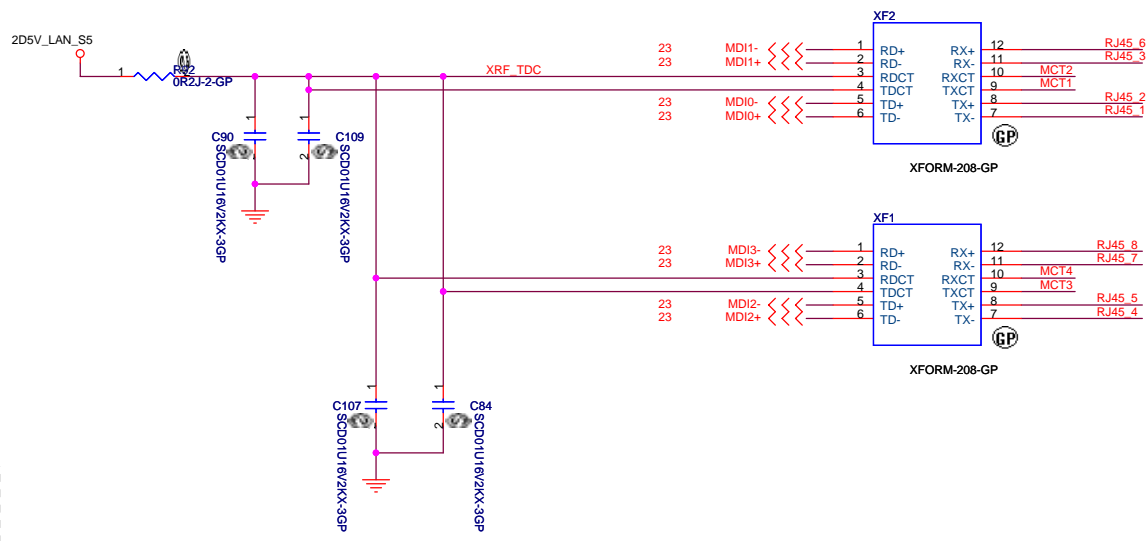
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	MARVELL 88E052		
Size A3	Document Number	Rev	SA
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LAN Connector



GIGA Lan Transformer

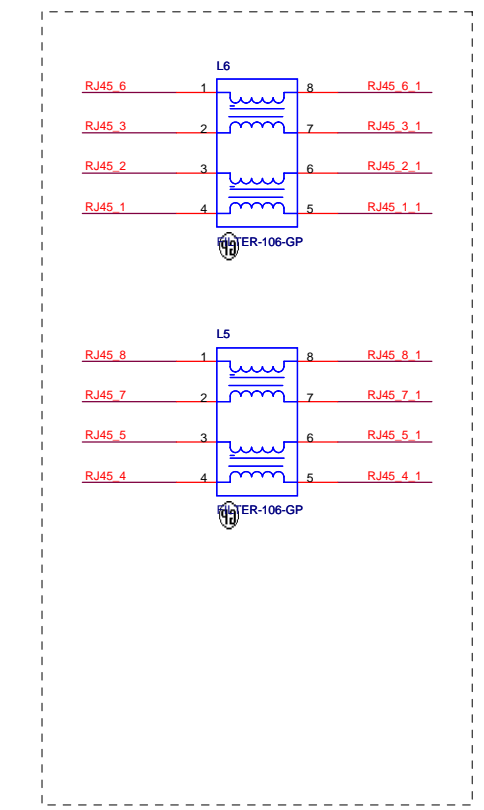
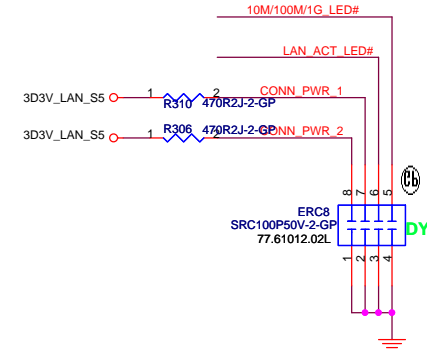
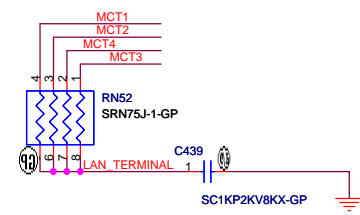


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
 W/S : 10/100 @ Surface layers
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



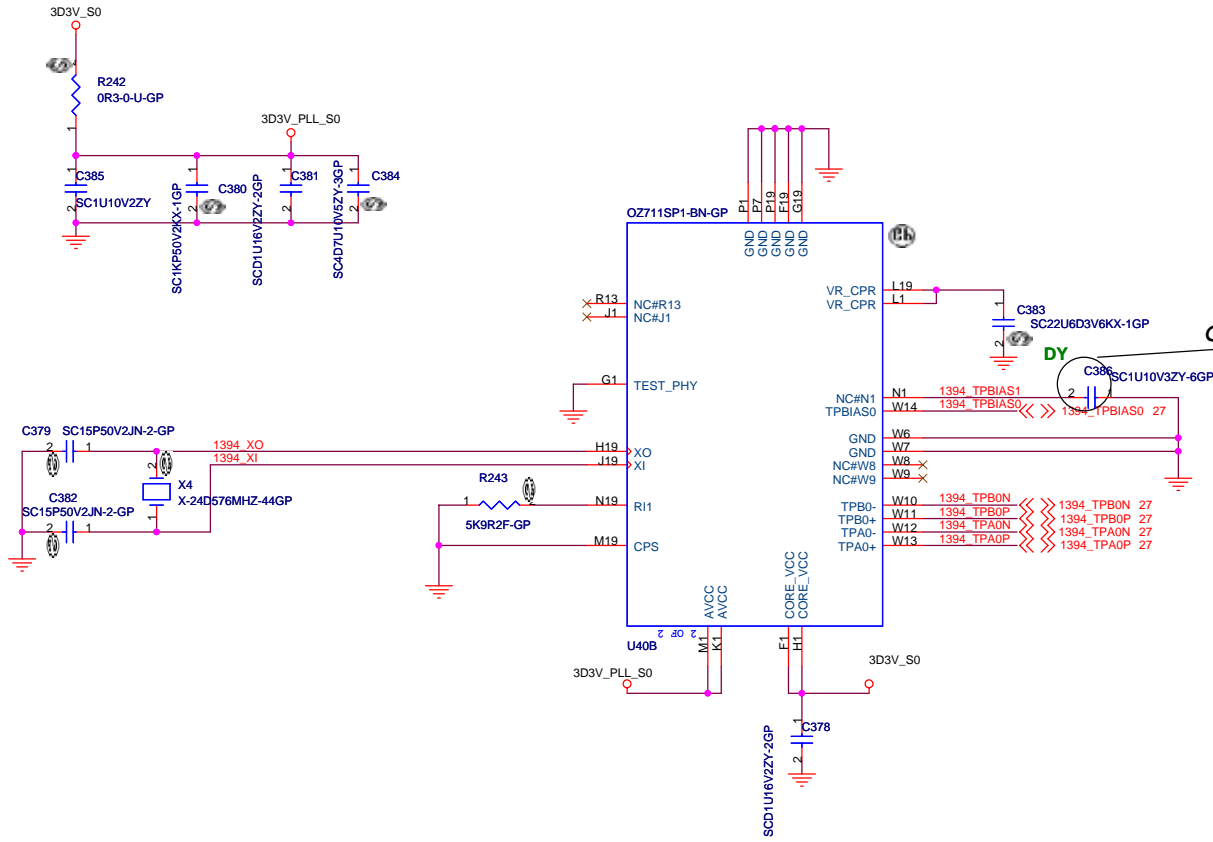
<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size A3 Document Number: **Orta** Rev: **SA**

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CHECK WITH FAE

DY

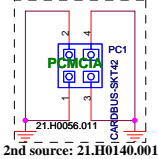
<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
OZ711SP1 (2 of 2)	
Size	Document Number
Orta	
Date: Tuesday, December 12, 2006	Sheet 26 of 46
Rev	SA

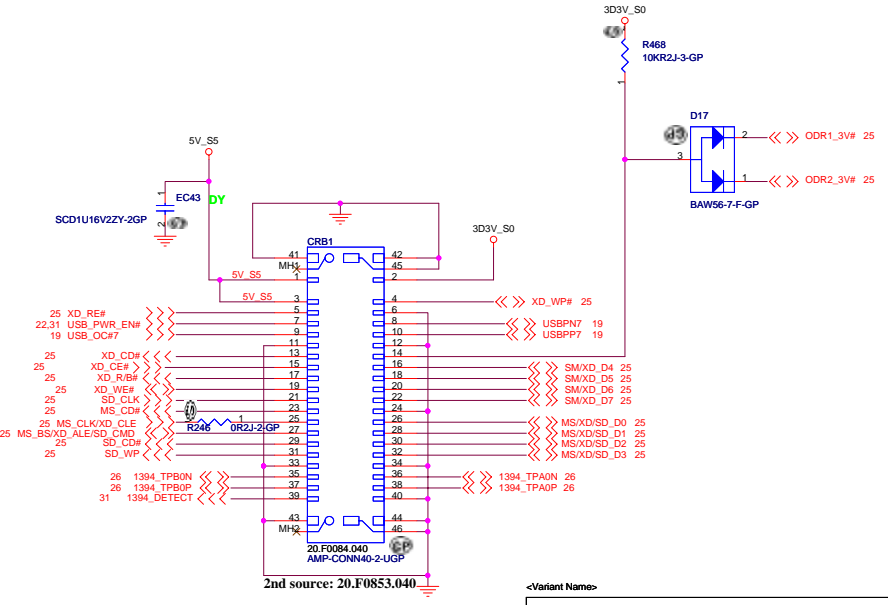
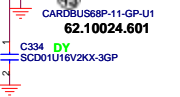
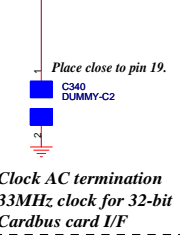
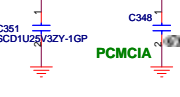
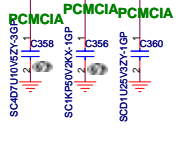
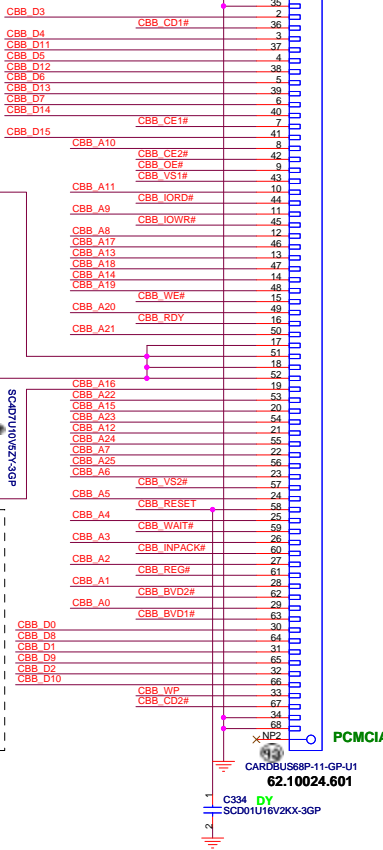
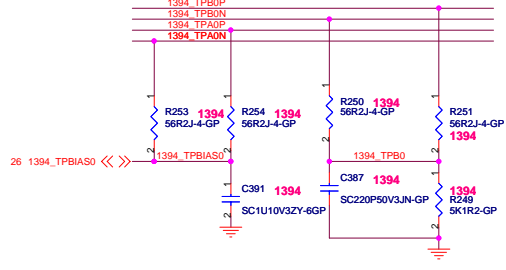
PCMCIA Socket

Cardbus I/F

- CBB_D[15..0] <<>> CBB_D[15..0] 25
- CBB_A[25..0] <<>> CBB_A[25..0] 25
- CBB_IORD# 25
- CBB_IOWR# 25
- CBB_WE# 25
- CBB_REG# 25
- CBB_RDY 25
- CBB_WP 25
- CBB_RESET 25
- CBB_WAIT# 25
- CBB_INPACK# 25
- CBB_CE1# 25
- CBB_CE2# 25
- CBB_BVD1# 25
- CBB_BVD2# 25
- CBB_CD1# 25
- CBB_CD2# 25
- CBB_VS1# 25
- CBB_VS2# 25



CLOSE TO CHIP



XD
MS / MS PRO
SD / SD IO / MMC

<Variant Name>

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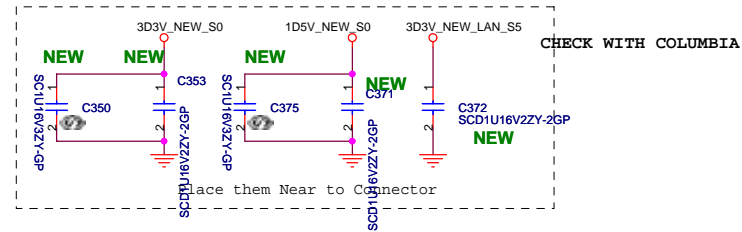
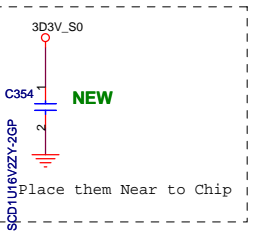
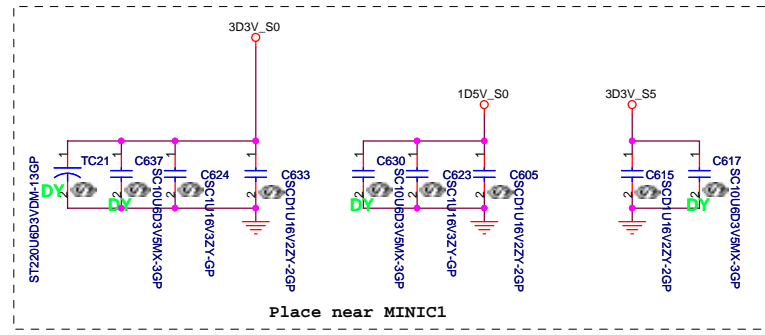
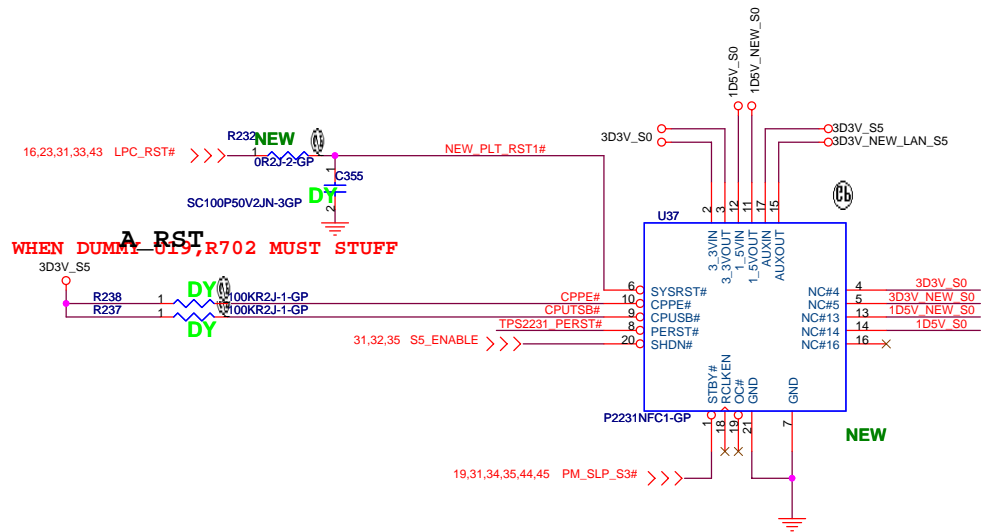
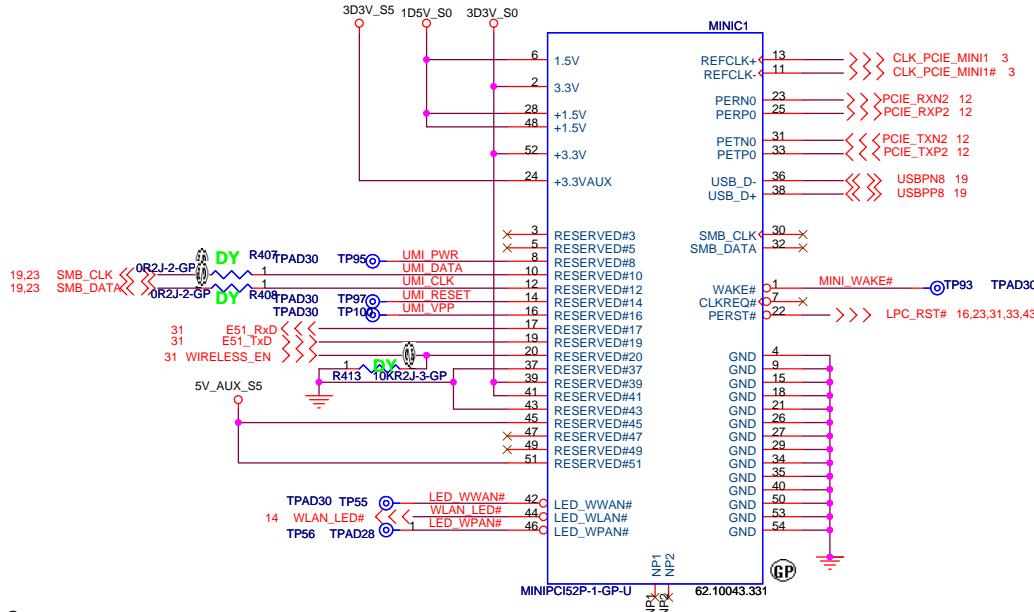
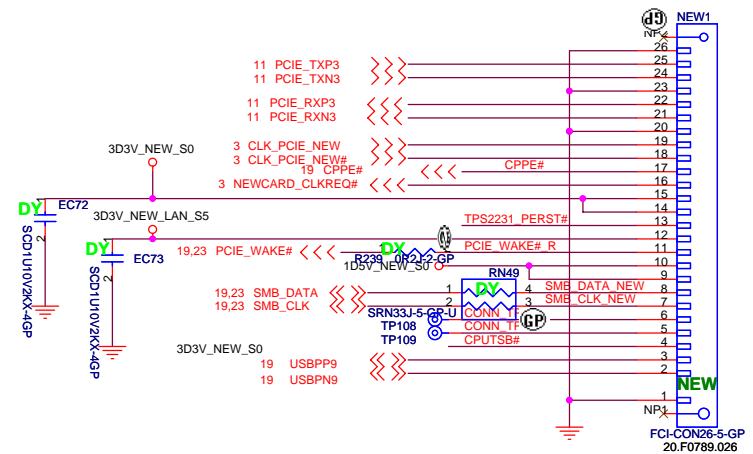
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Size	Document Number	Rev	SA
Orta			
Date: Tuesday, December 12, 2006	Sheet	27	of 46

Mini Card Connector

NEWCARD Connector



Reserve the symbol
for bottom side
connector



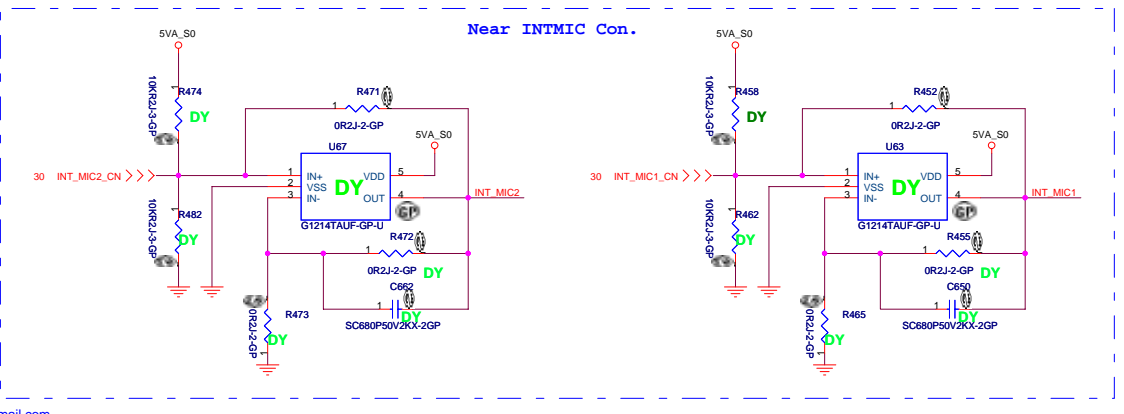
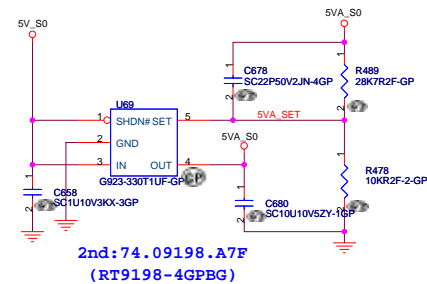
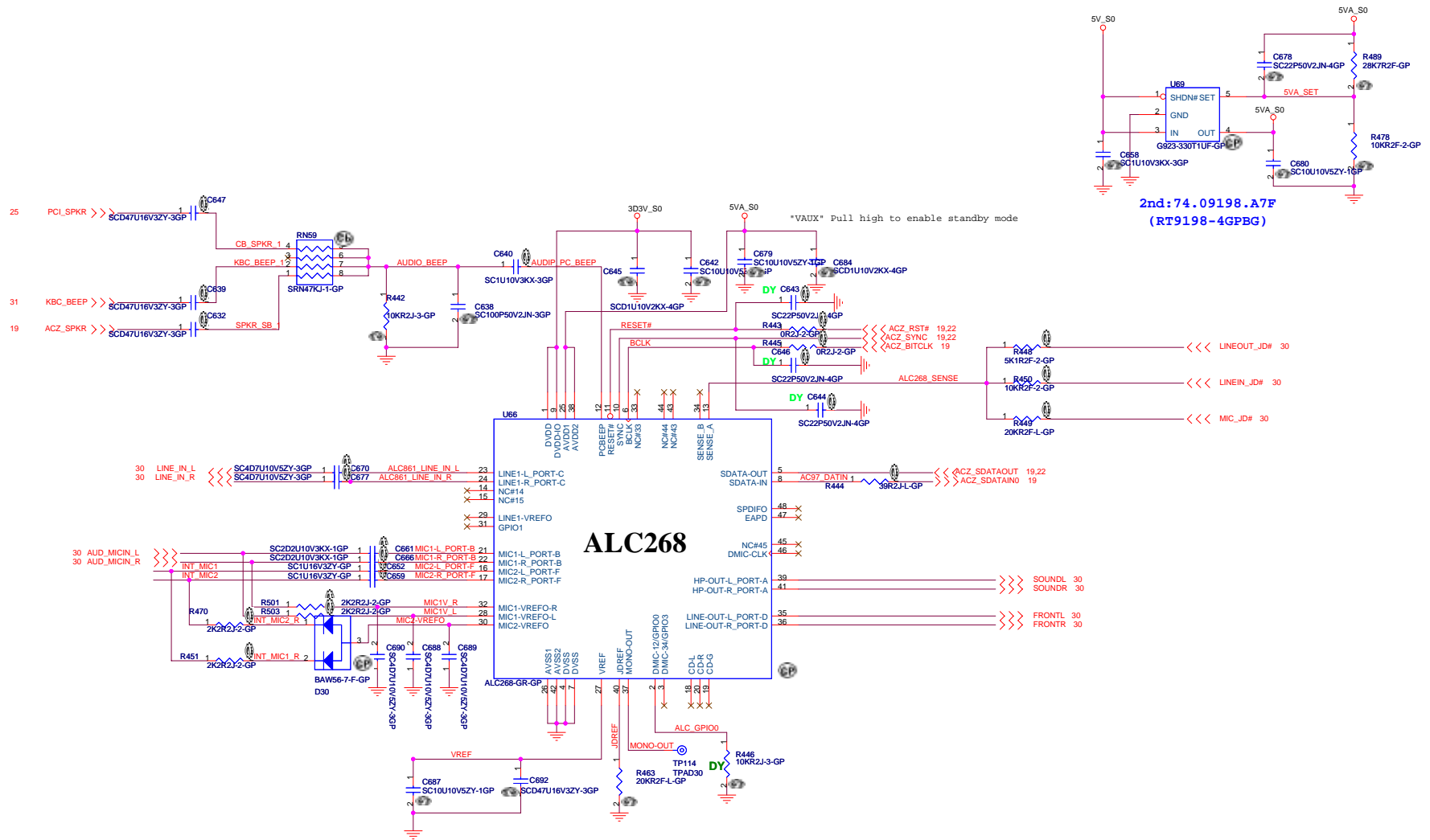
bon1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / NEW CARD**

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Date: Tuesday, December 12, 2006		Sheet	28 of 46

Orta

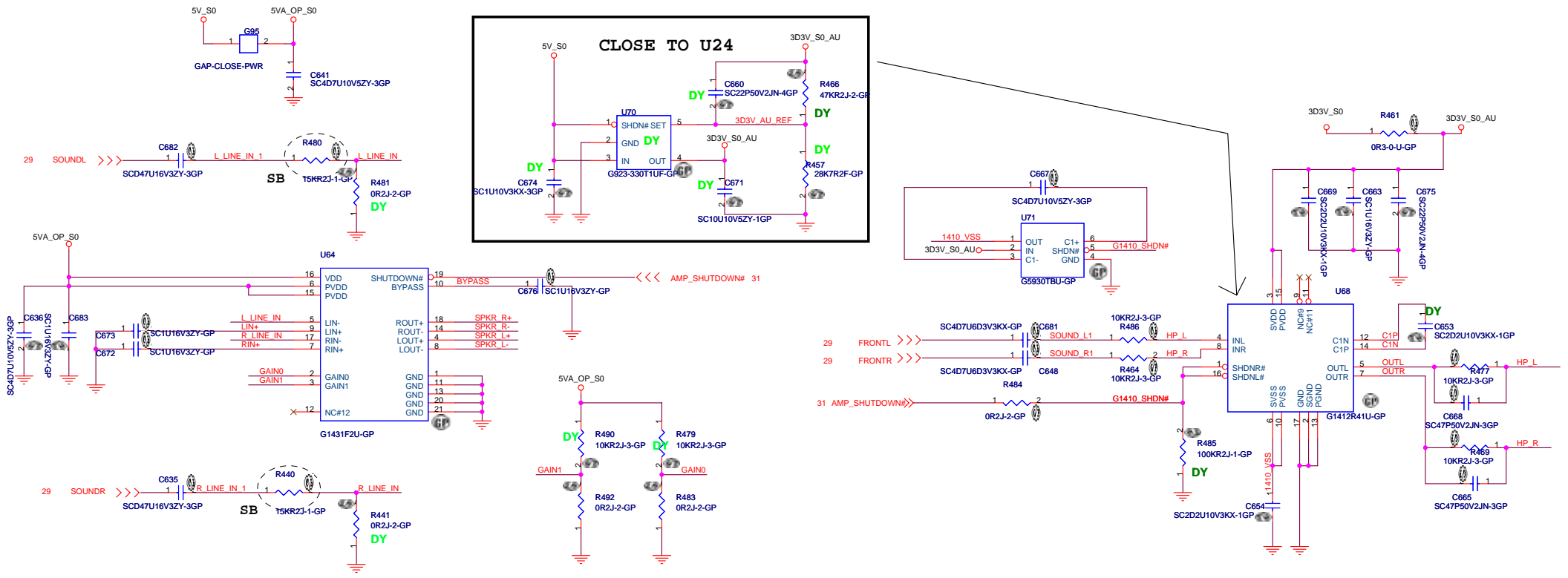
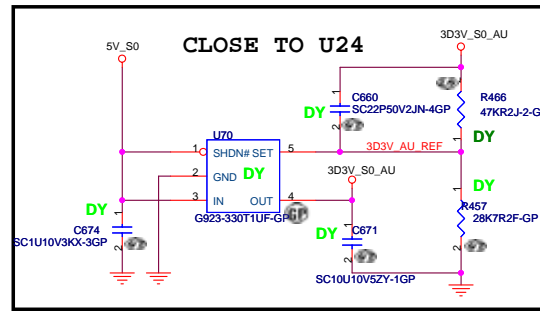


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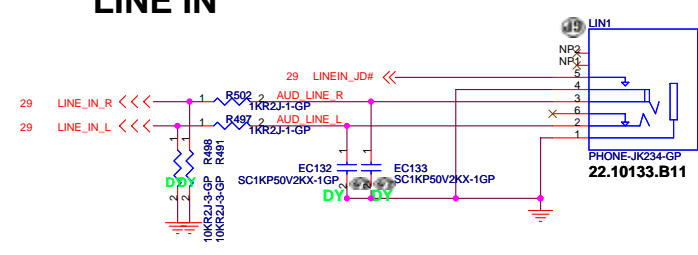
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsin 221, Taiwan, R.O.C.			
Title	AZALIA CODEC - ALC268		
Size	Document Number	Orta	Rev SA
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AUDIO OP AMPLIFIER

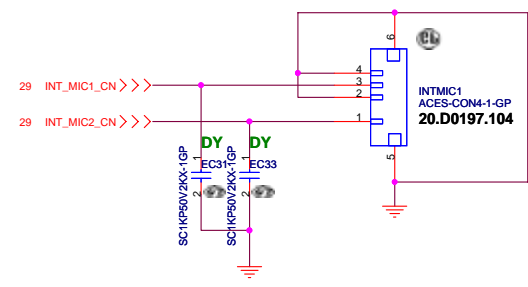
KBC_MUTE_GPIO8



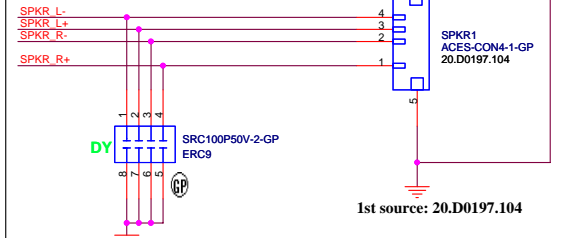
LINE IN



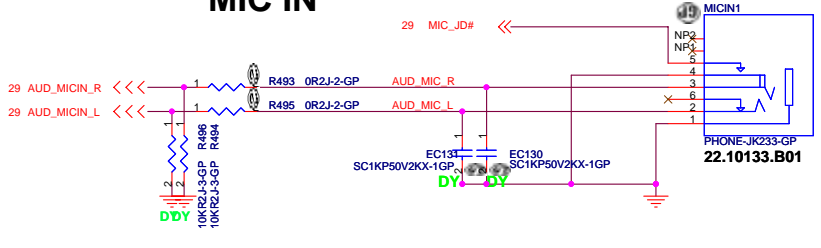
Internal Microphone



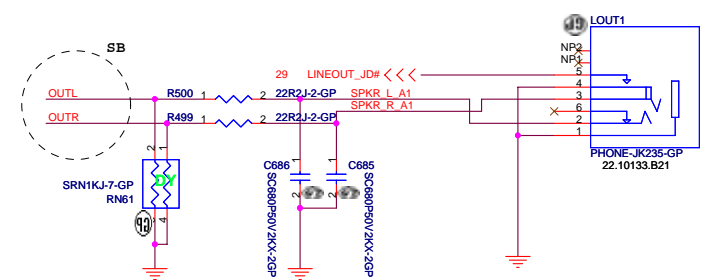
Internal Speaker



MIC IN

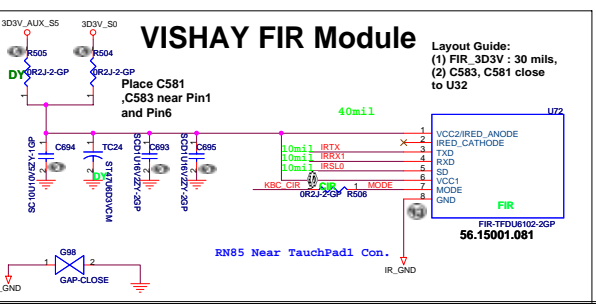
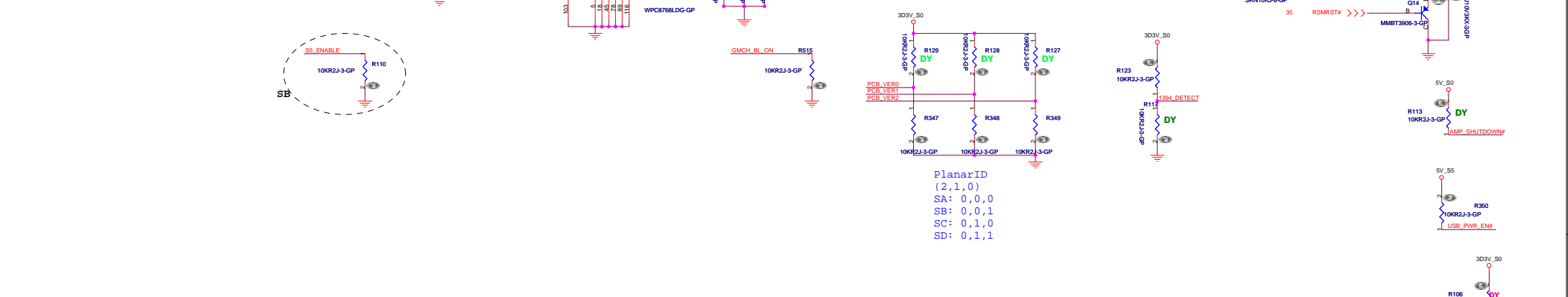
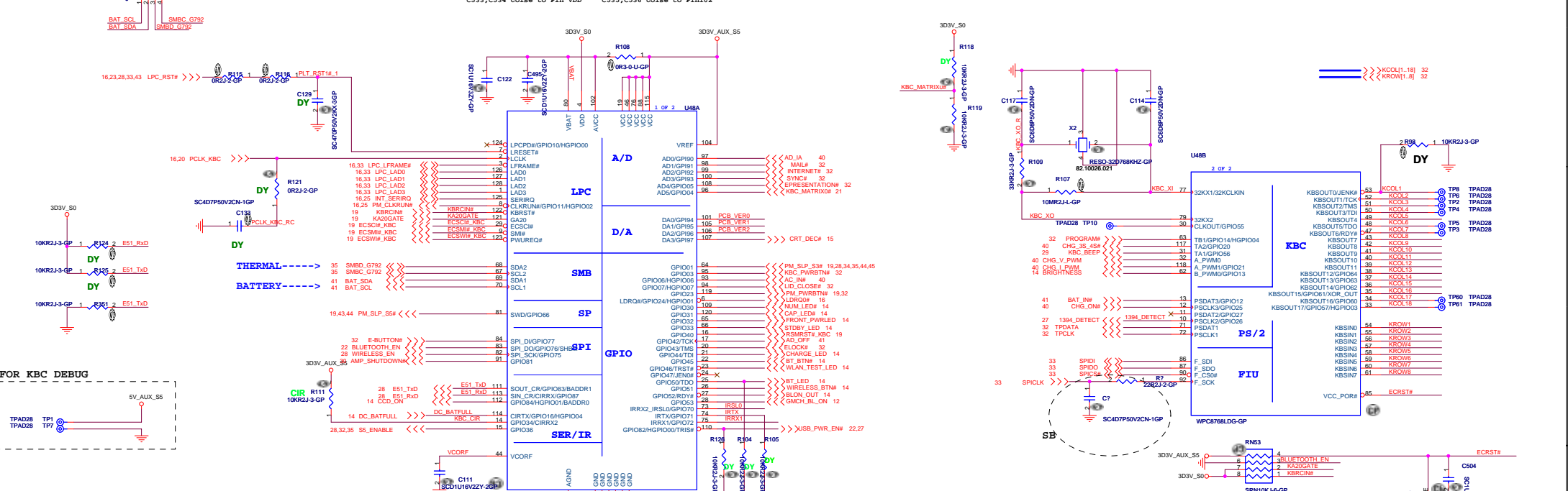
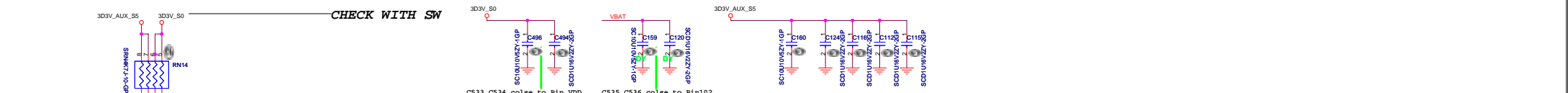


LINE OUT



<Variant Name>

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Title	AUDIO AMP AND JACK	
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	Orta	SA
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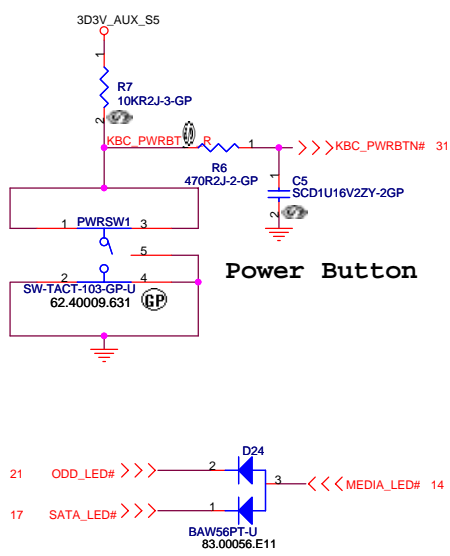
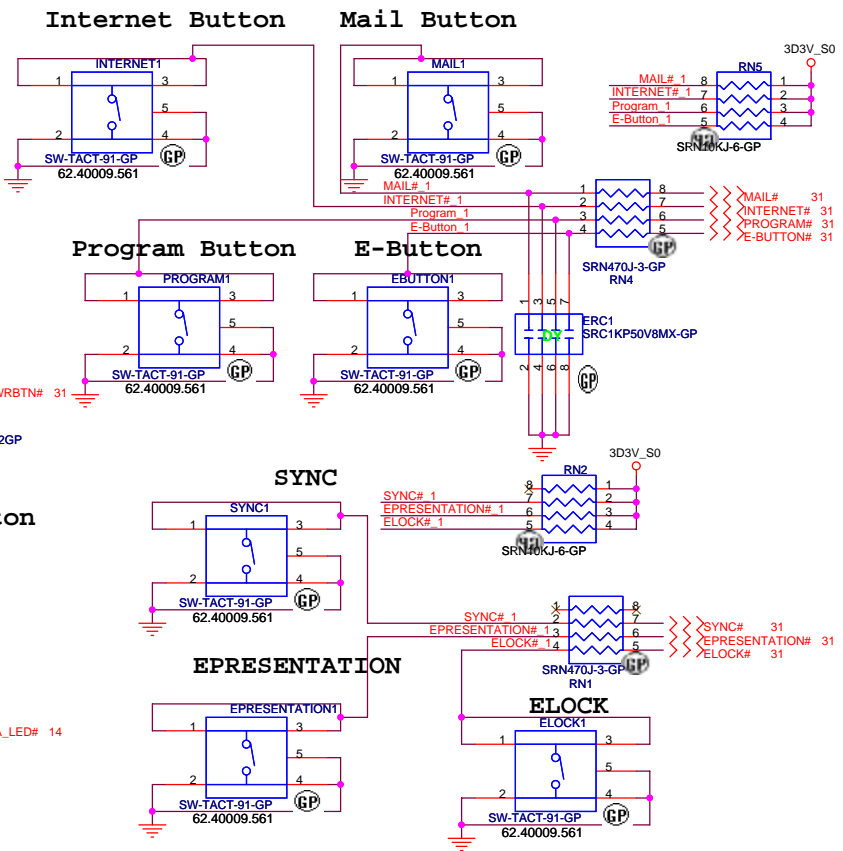
PlanarID
 (2,1,0)
 SA: 0,0,0
 SB: 0,0,1
 SC: 0,1,0
 SD: 0,1,1

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsiehlin, Taipei Hsein 221, Taiwan, R.O.C.

Model: **KBC WPC8768L**

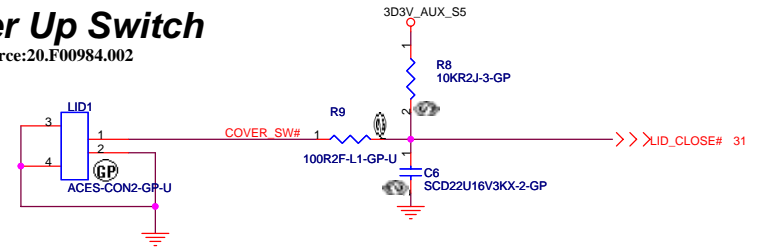
Size: A2 | Document Number: **Orta** | Rev: 46

Date: Tuesday, December 12, 2006 | Sheet: 31 of 46

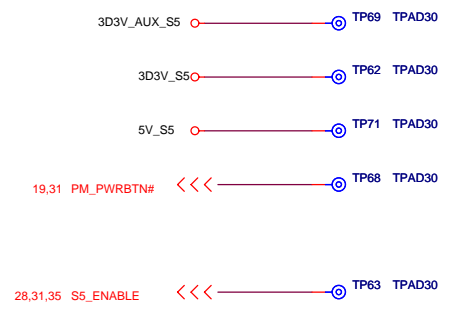


Cover Up Switch

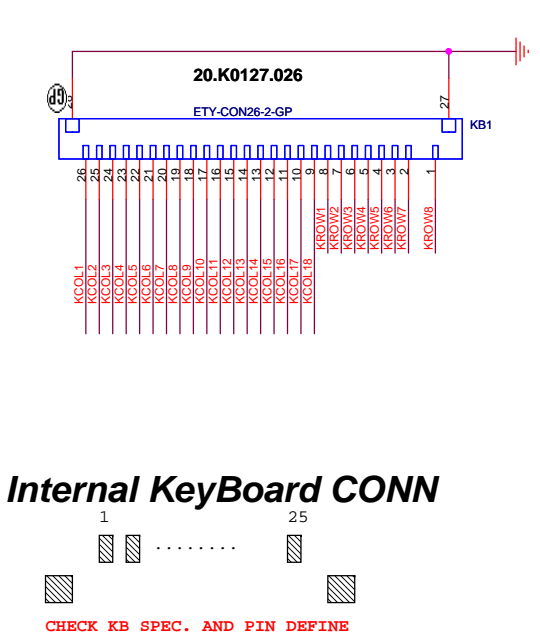
2nd source:20.F00984.002



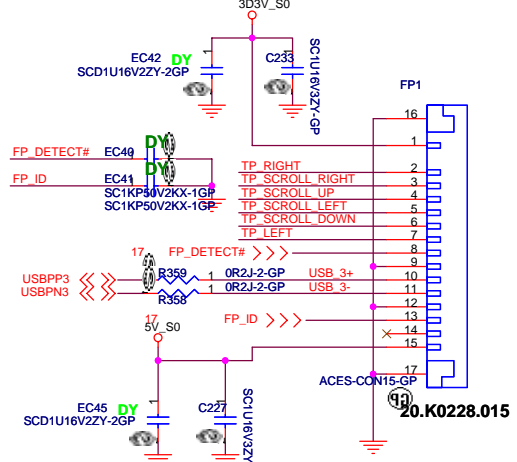
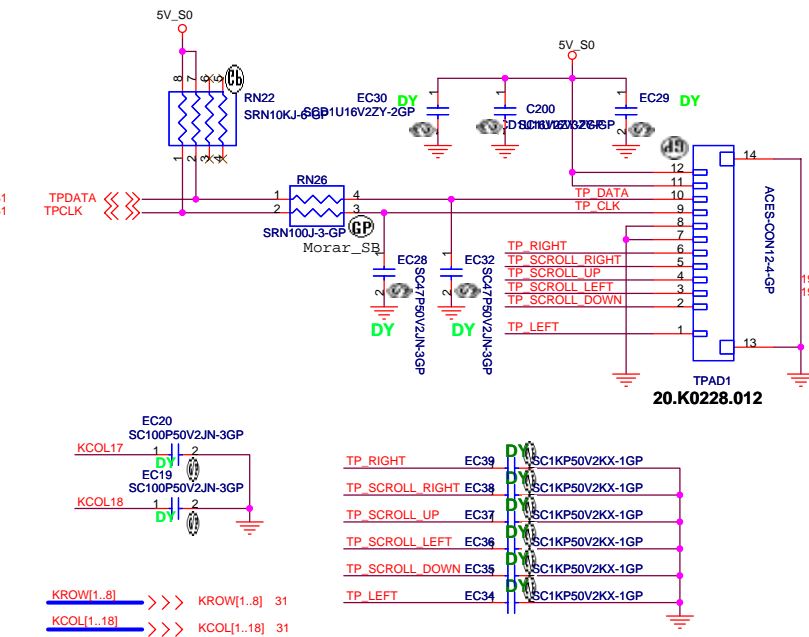
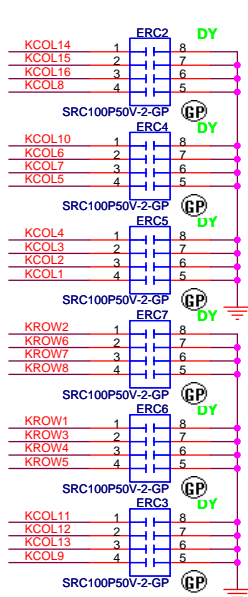
Check test point



Test Point 放在 Dimm Door 打開可量測處



EMI Bypass cap.

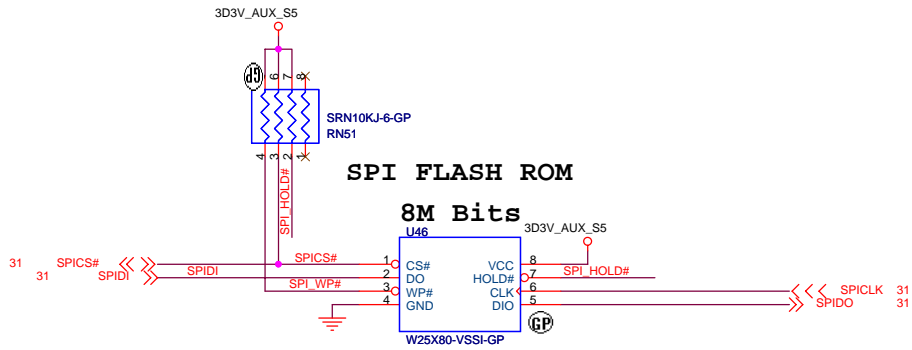


緯創資通 Wistron Corporation
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Title: **BUTTONS / KB / TOUCHPAD**

Size: Document Number: Orta

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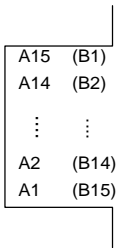
SPI FLASH ROM

8M Bits

U46

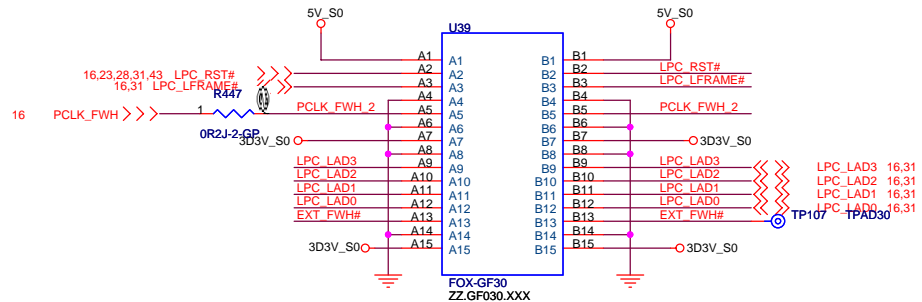
W25X80-VSSI-GP

TOP VIEW

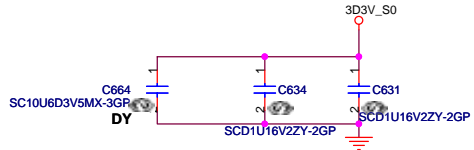


(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46



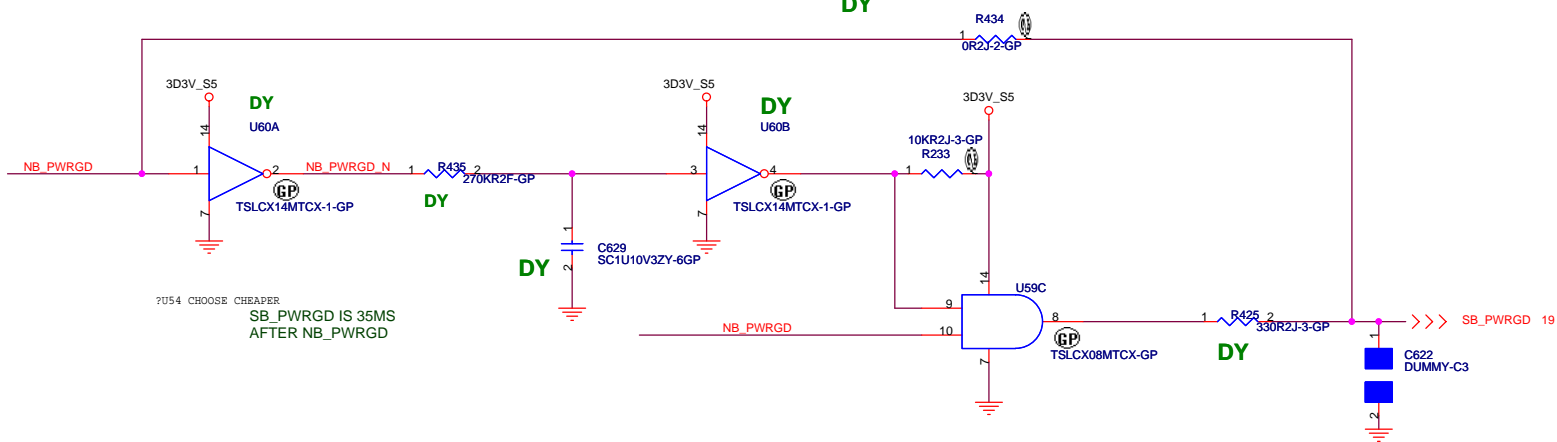
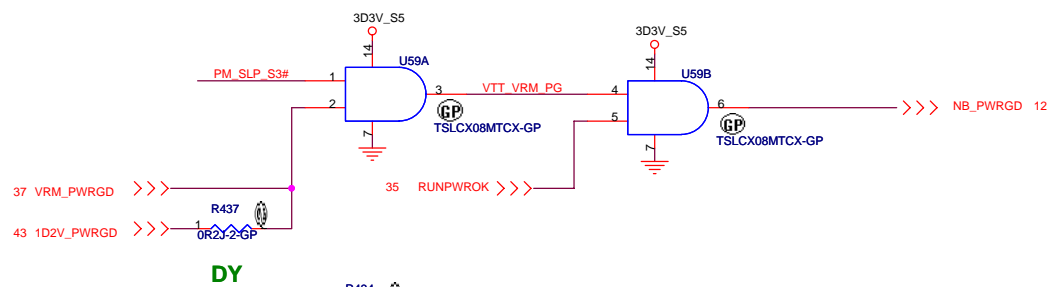
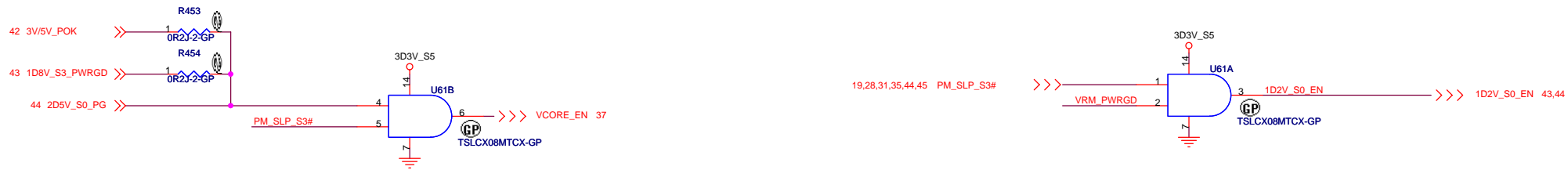
<Core Design>

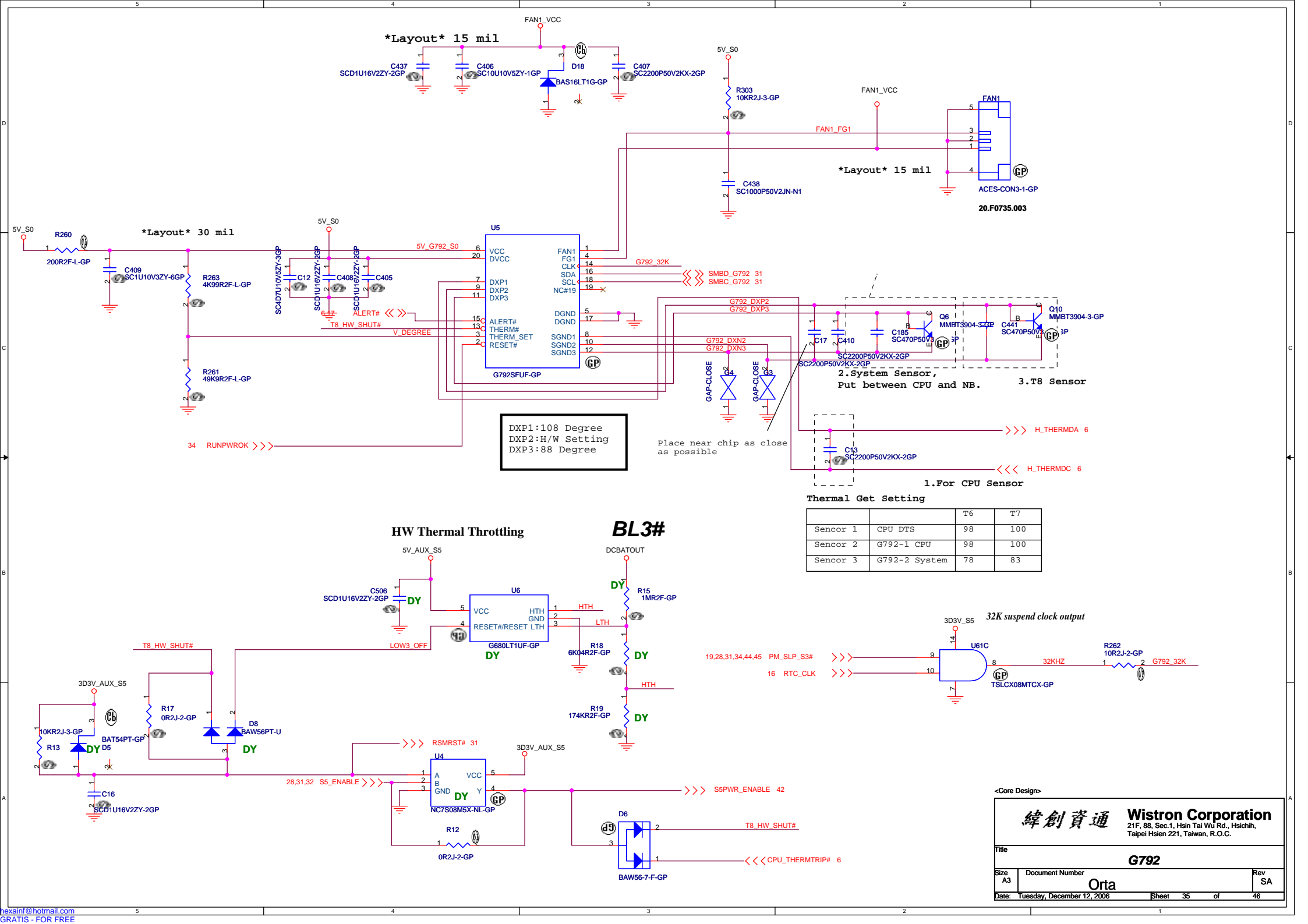
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

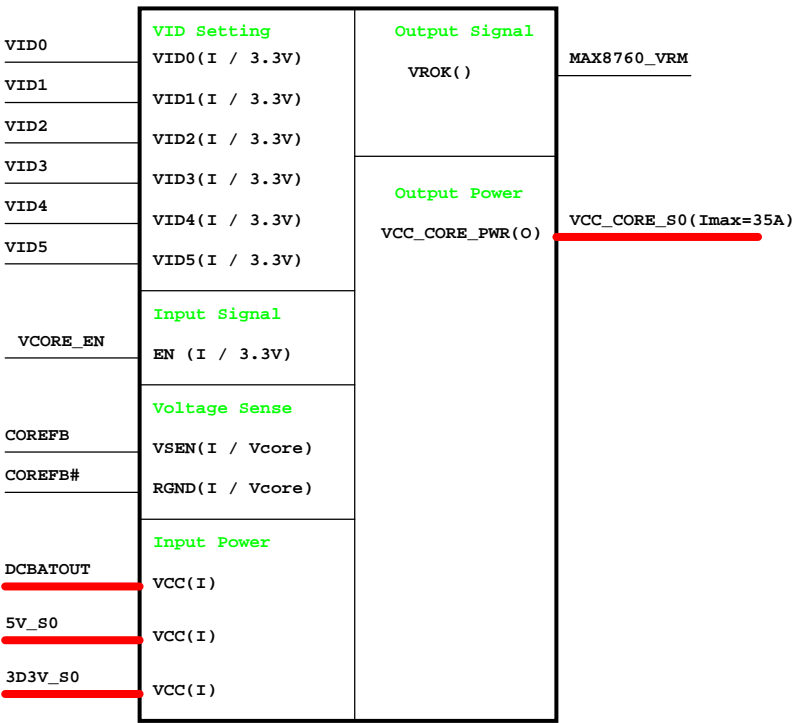
Size: A3 Document Number: Orta Rev: SA

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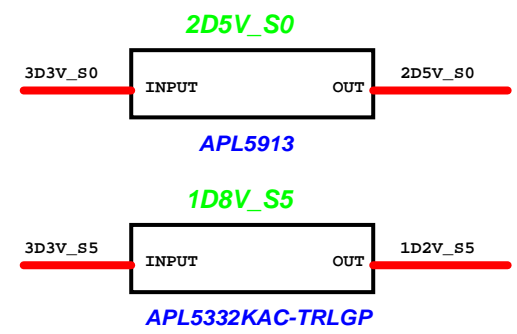
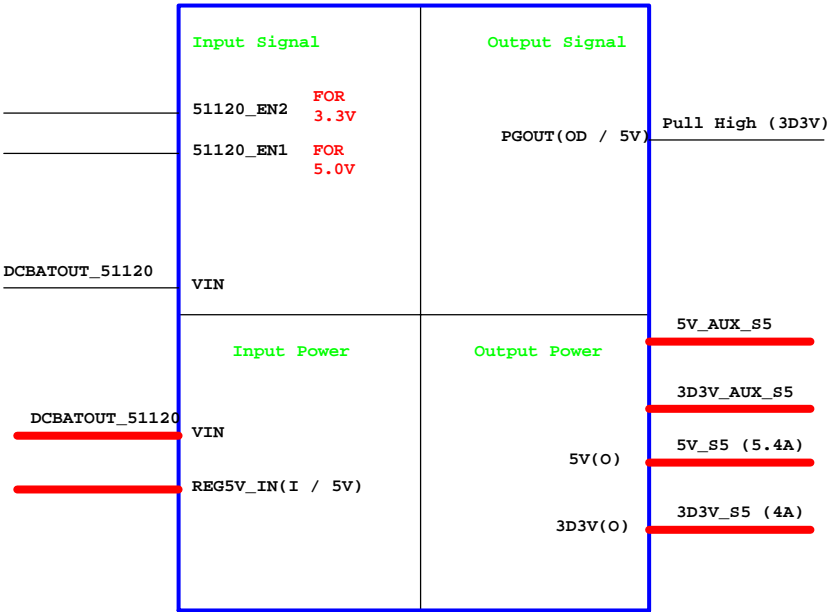




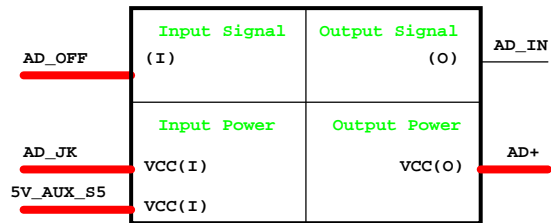
CPU_CORE
ISL6264CRZ



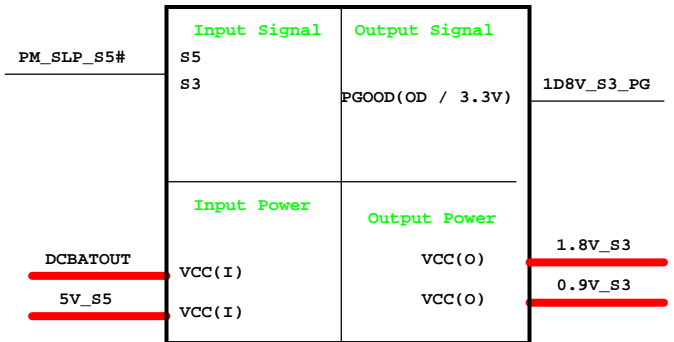
TI TPS51120
3D3V/5V



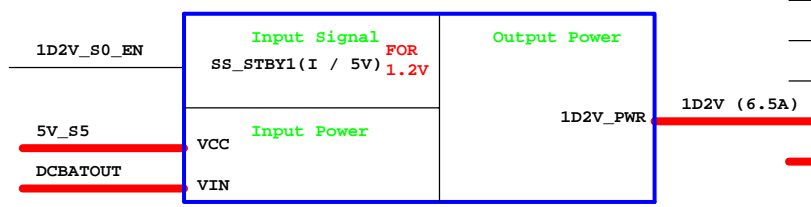
Adapter



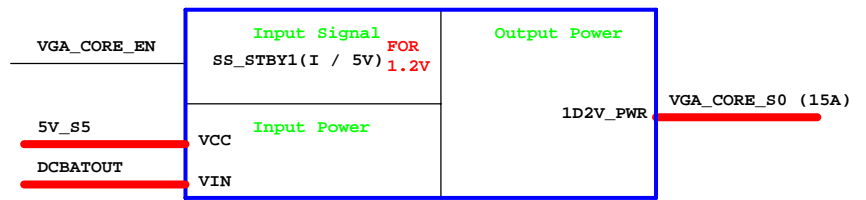
TI TPS51116
1.8V / 0.9V



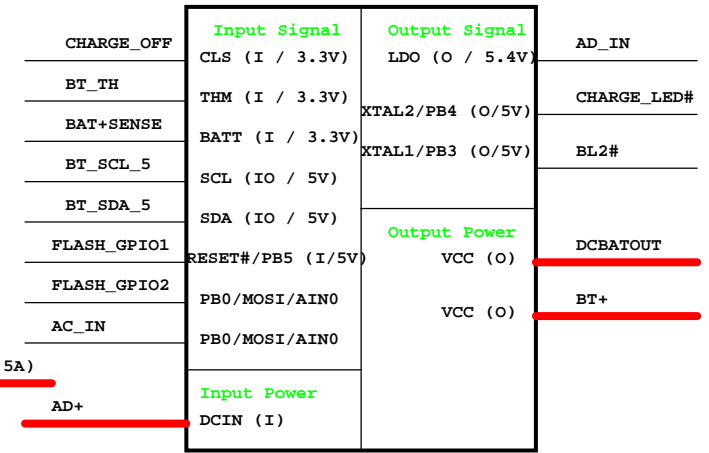
ISL6268_1D2V



ISL6268_VGA_CORE



Charger_ISL6255



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

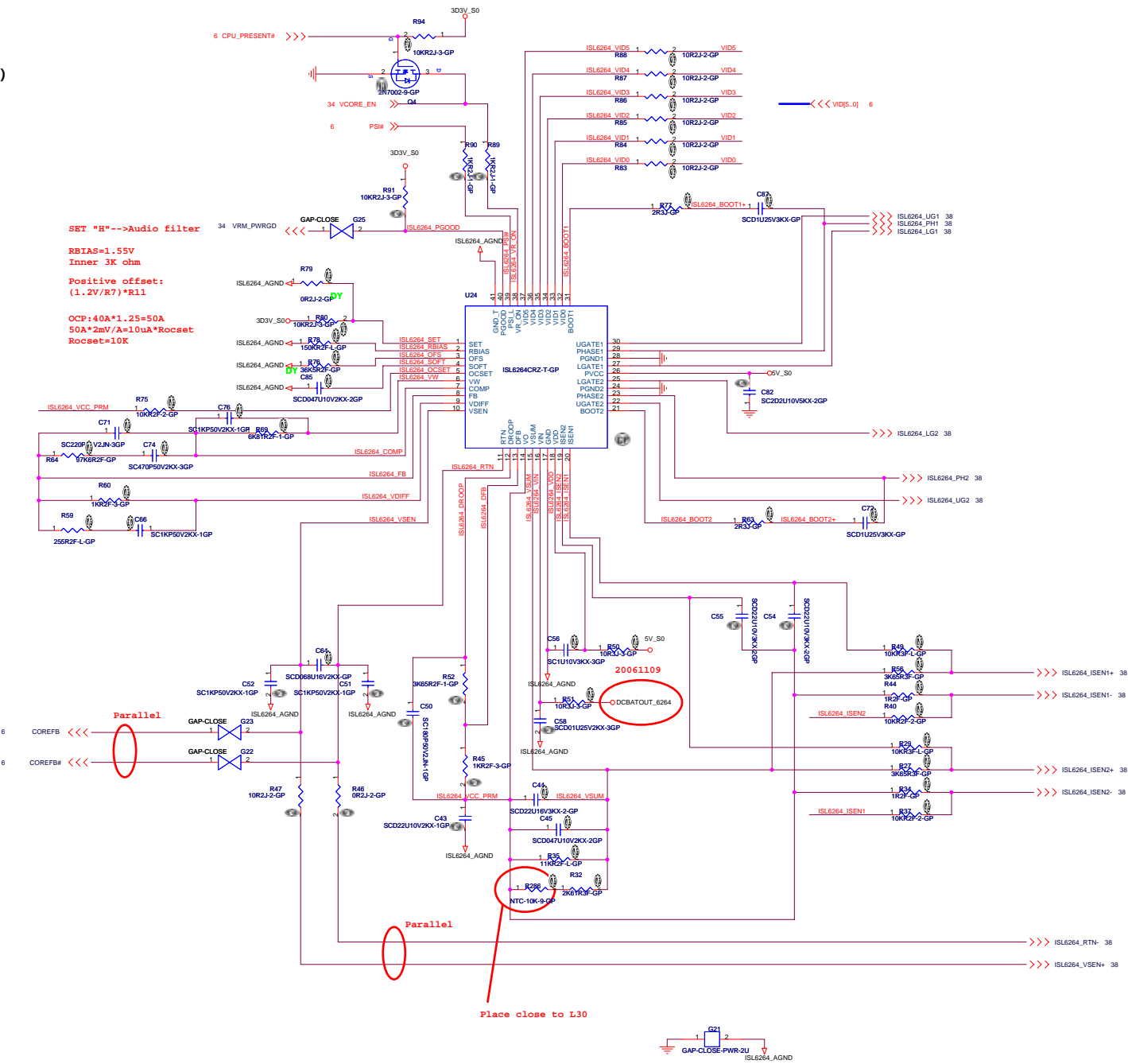
Size: A3 Document Number: Orta Rev: SA

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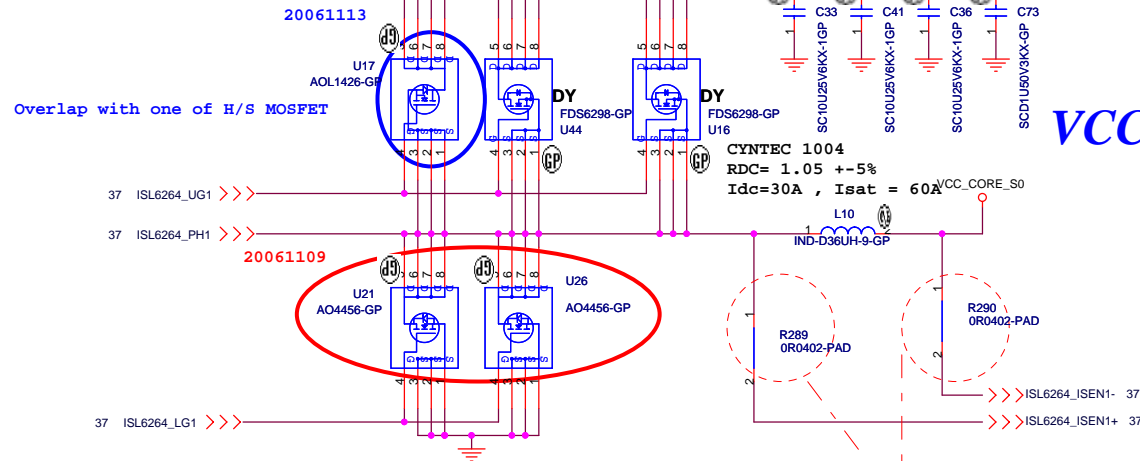
CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A(35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

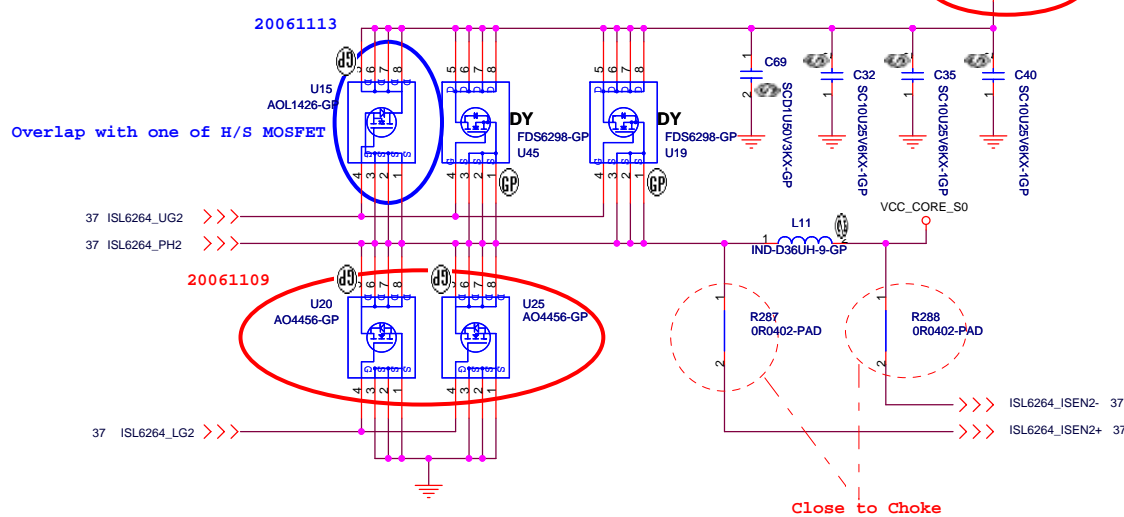
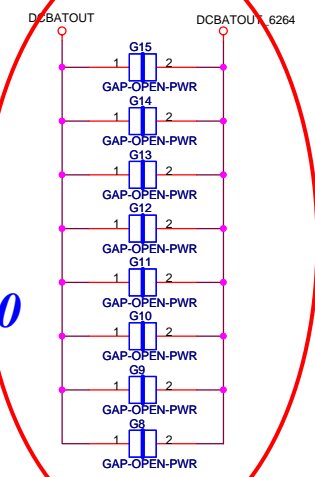
VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	0	1	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	1	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	0	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	1	0	0	0	0	1.175
0	1	0	0	0	1	1.150
0	1	0	0	1	0	1.125
0	1	0	0	1	1	1.100
0	1	0	1	0	0	1.075
0	1	0	1	0	1	1.050
0	1	0	1	1	0	1.025
0	1	0	1	1	1	1.000
0	1	1	0	0	0	0.975
0	1	1	0	0	1	0.950
0	1	1	0	1	0	0.925
0	1	1	0	1	1	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
1	0	0	0	0	0	0.775
1	0	0	0	0	1	0.750
1	0	0	0	1	0	0.725
1	0	0	1	0	0	0.700
1	0	0	1	0	1	0.675
1	0	1	0	0	0	0.650
1	0	1	0	0	1	0.625
1	0	1	1	0	0	0.600
1	0	1	1	0	1	0.575
1	1	0	0	0	0	0.550
1	1	0	0	0	1	0.525
1	1	0	0	1	0	0.500
1	1	0	0	1	1	0.475
1	1	0	1	0	0	0.450
1	1	0	1	0	1	0.425
1	1	0	1	1	0	0.400
1	1	0	1	1	1	0.375



SET "H"-->Audio filter
 RBIAS=1.55V
 Inner 3K ohm
 Positive offset:
 (1.2V/R7)*R11
 OCP:40A*1.25=50A
 50A*2mV/A=100uA*Rocset
 Rocset=10K

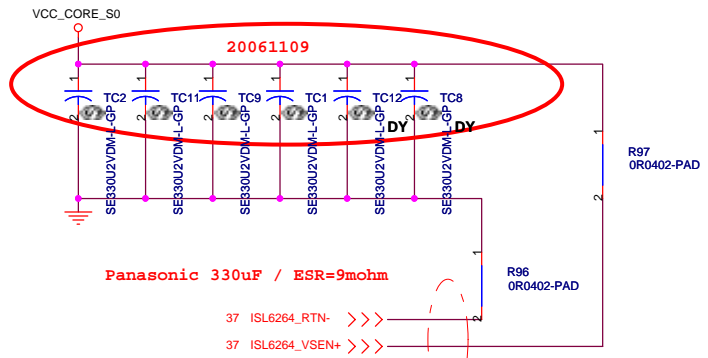


VCC_CORE_S0



Close to Choke

20061109

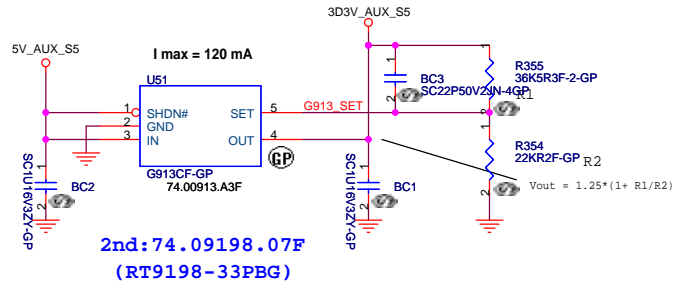


Panasonic 330uF / ESR=9mohm

Parallel

Aux Power

3D3V_AUX_S5



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

3D3V_AUX

Size

Document Number

A3

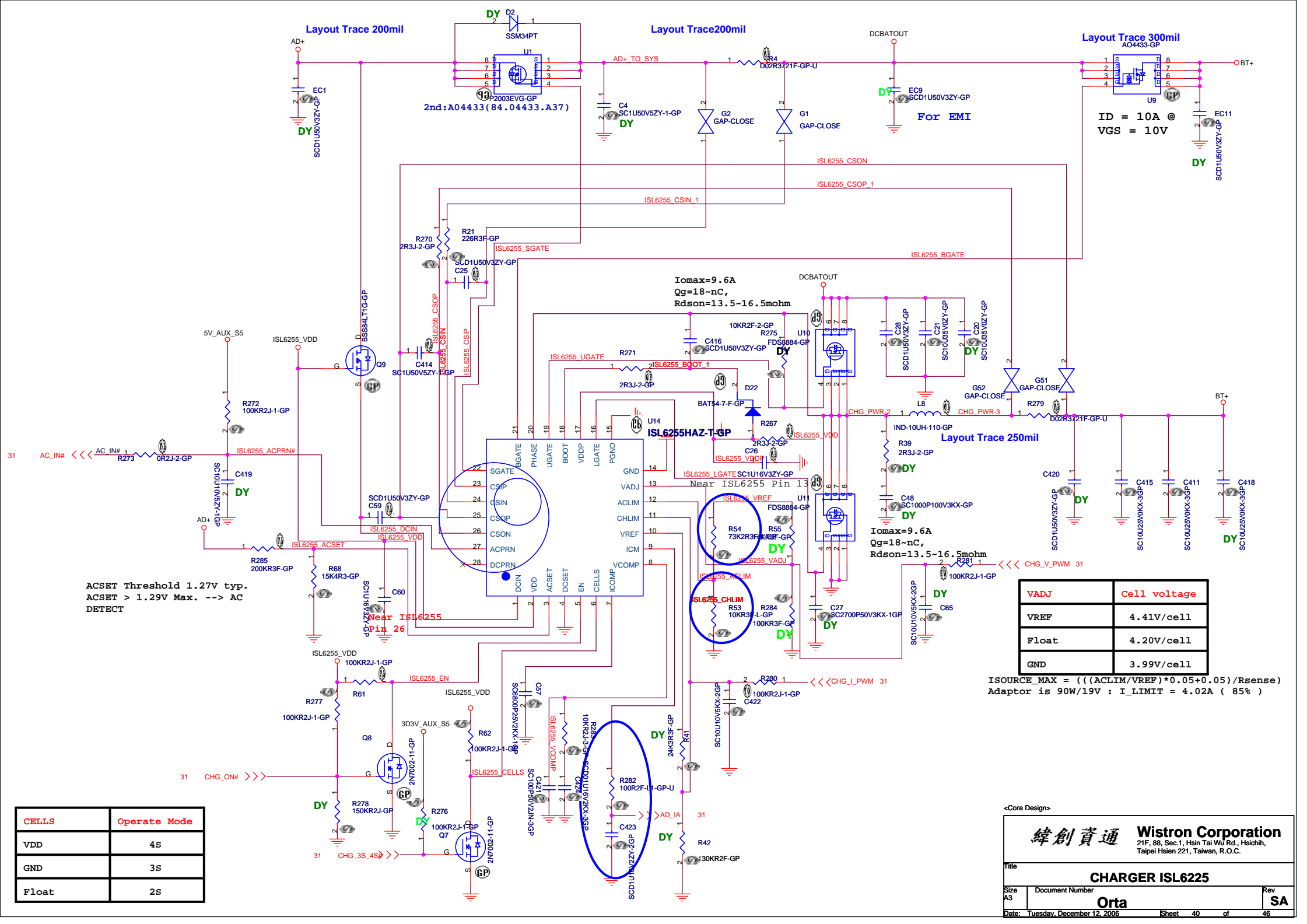
Orta

Rev

SA

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ACSET Threshold 1.27V typ.
 ACSET > 1.29V Max. --- AC
 DETECT

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
 Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

<Core Design>

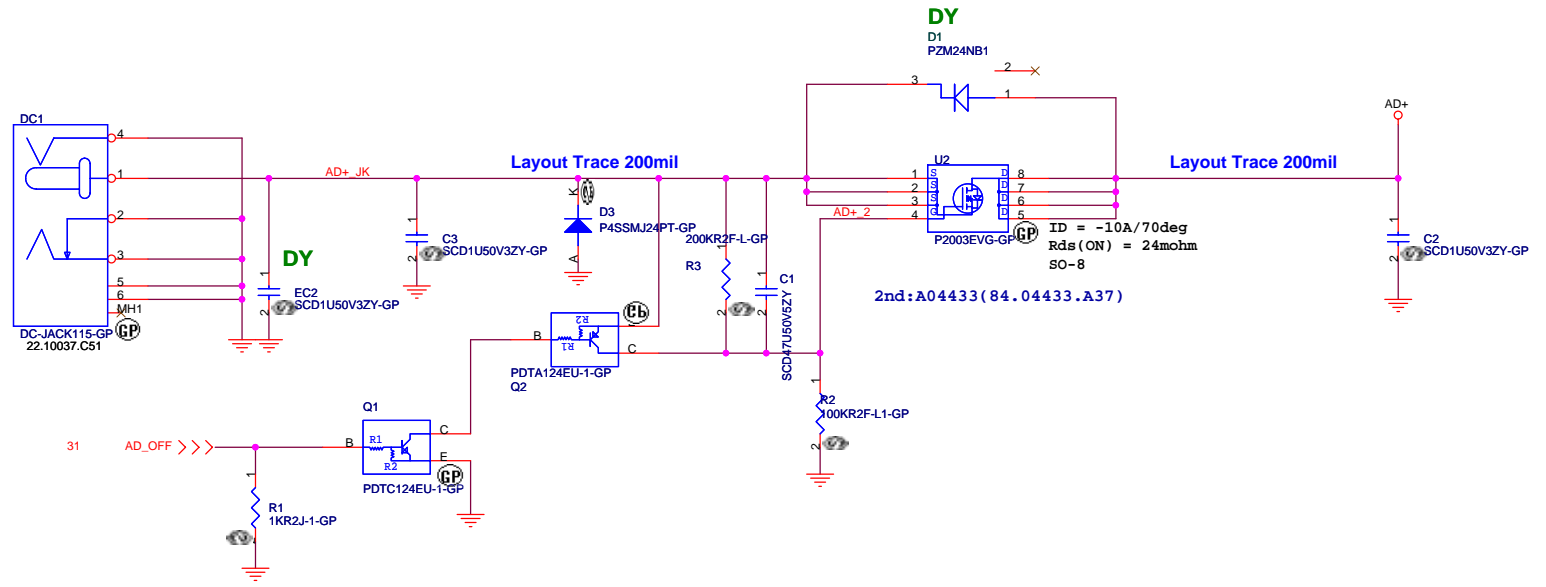
緯創資通 WISTRON CORPORATION
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER ISL6255**

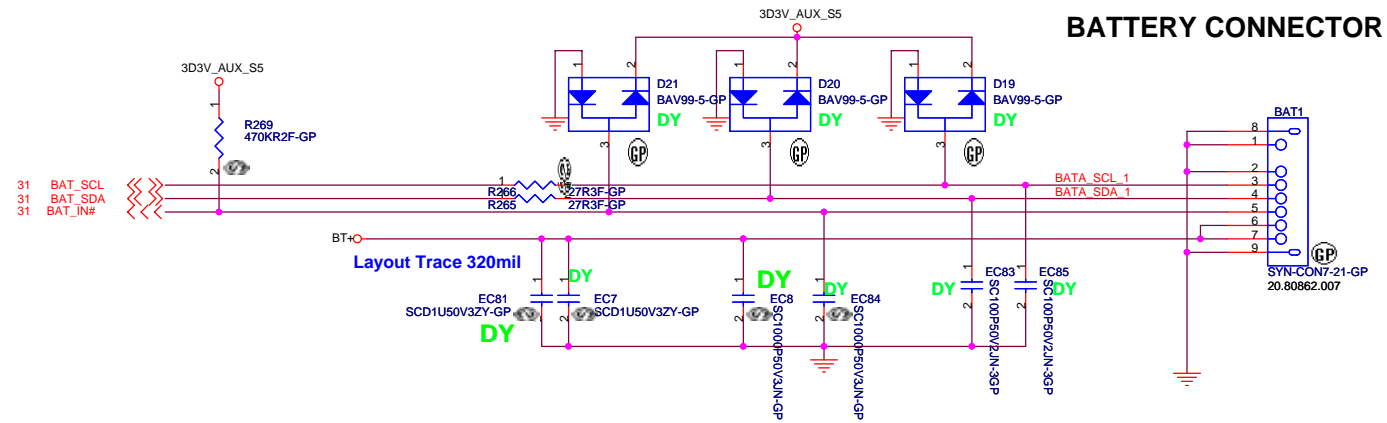
Size A3	Document Number	Rev SA
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



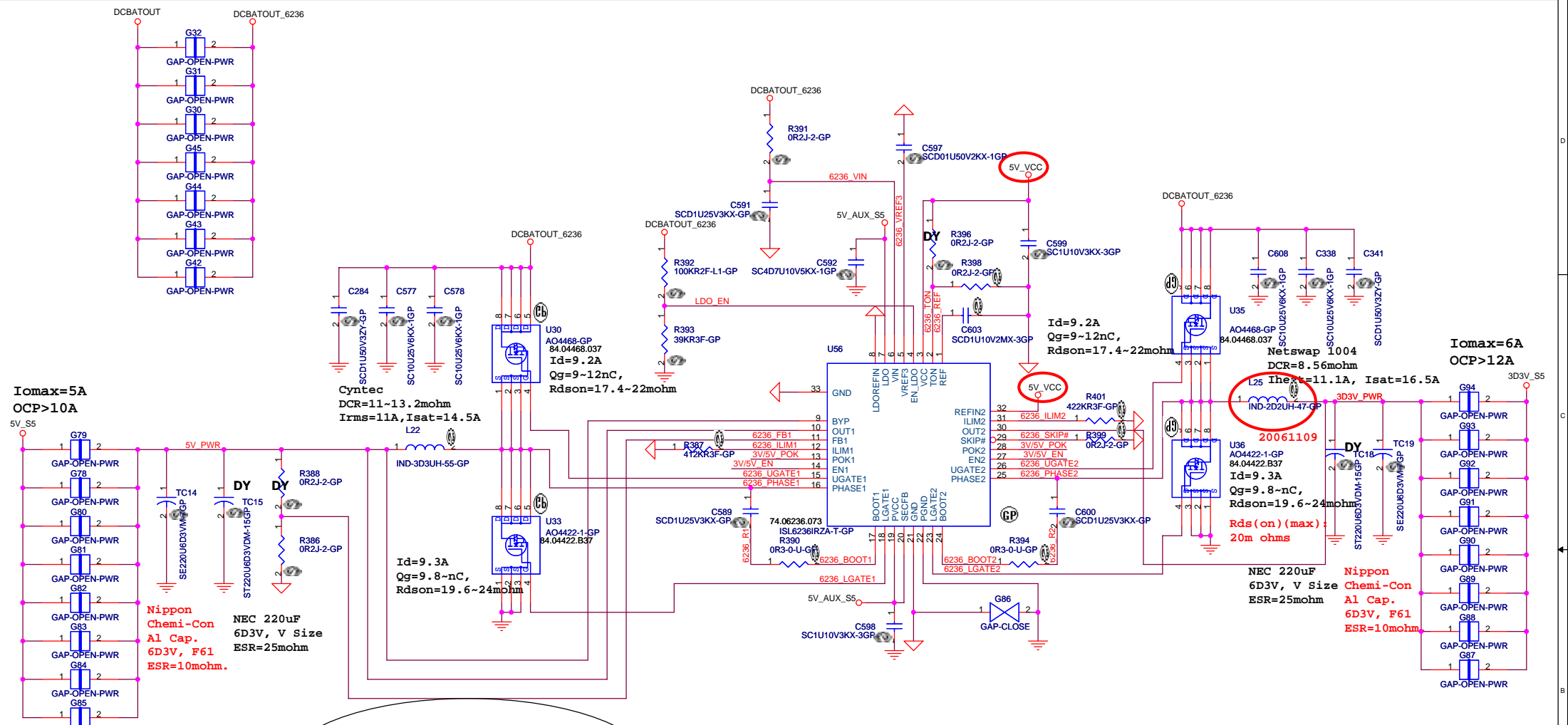
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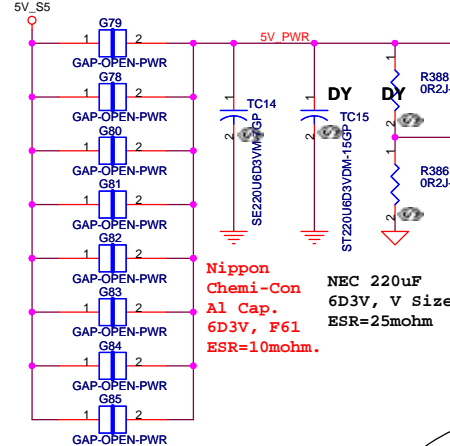
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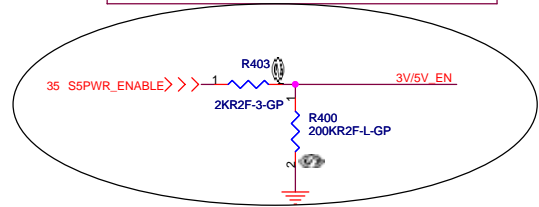


I_omax=5A
OCP>10A

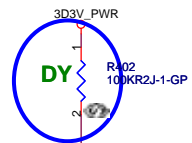


Maximum current:5A
If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 400K$
 $L \sim 3.3\mu H$

OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5uA$
 $\sim 438K \rightarrow 442K$



35 S5PWR_ENABLE >>> 3V/5V_EN



3D3V_PWR >>> 3V/5V_POK 34

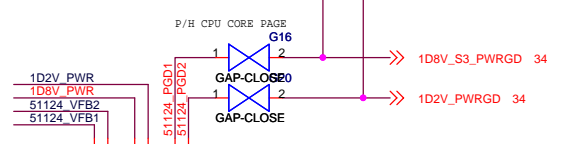
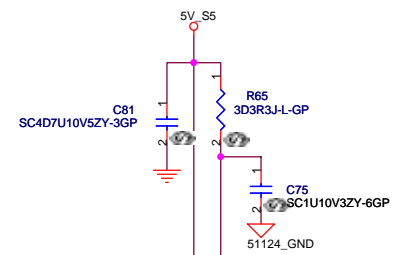
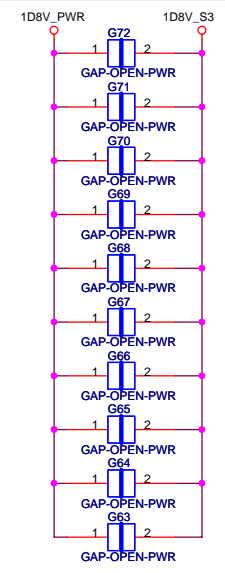
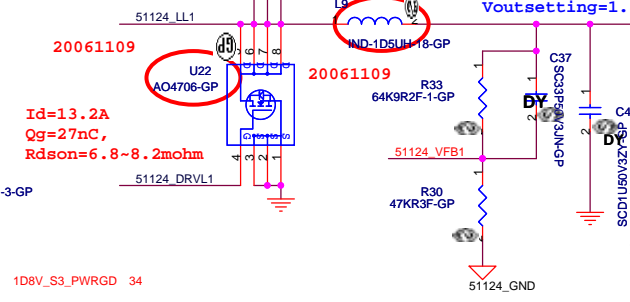
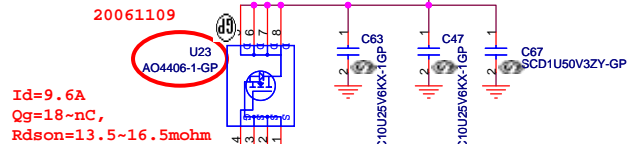
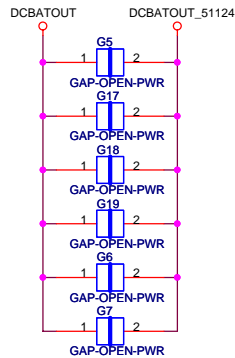
Maximum current:5A
If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 500K$
 $L \sim 2.2\mu H$

OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5uA$
 $\sim 438K \rightarrow 442K$

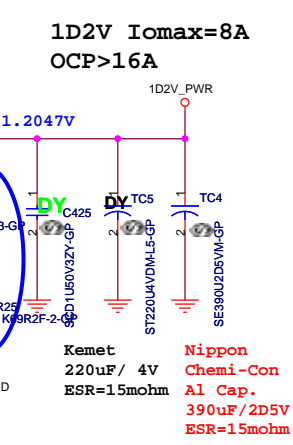
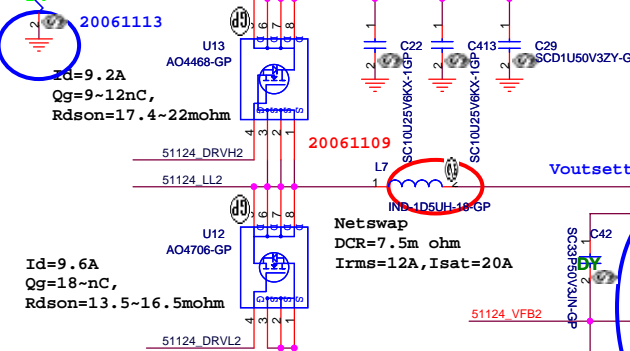
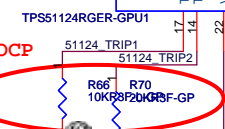
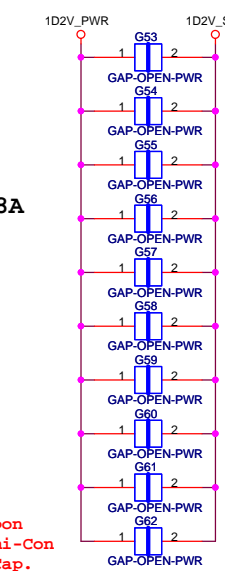
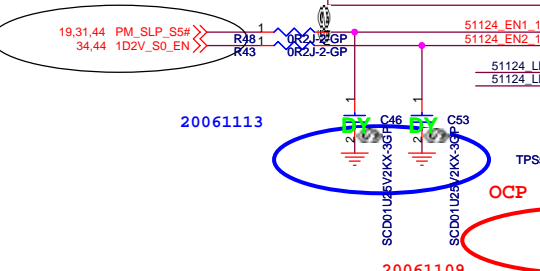
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$$V_{out} = 0.758V * (R1 + R2) / R2$$



$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

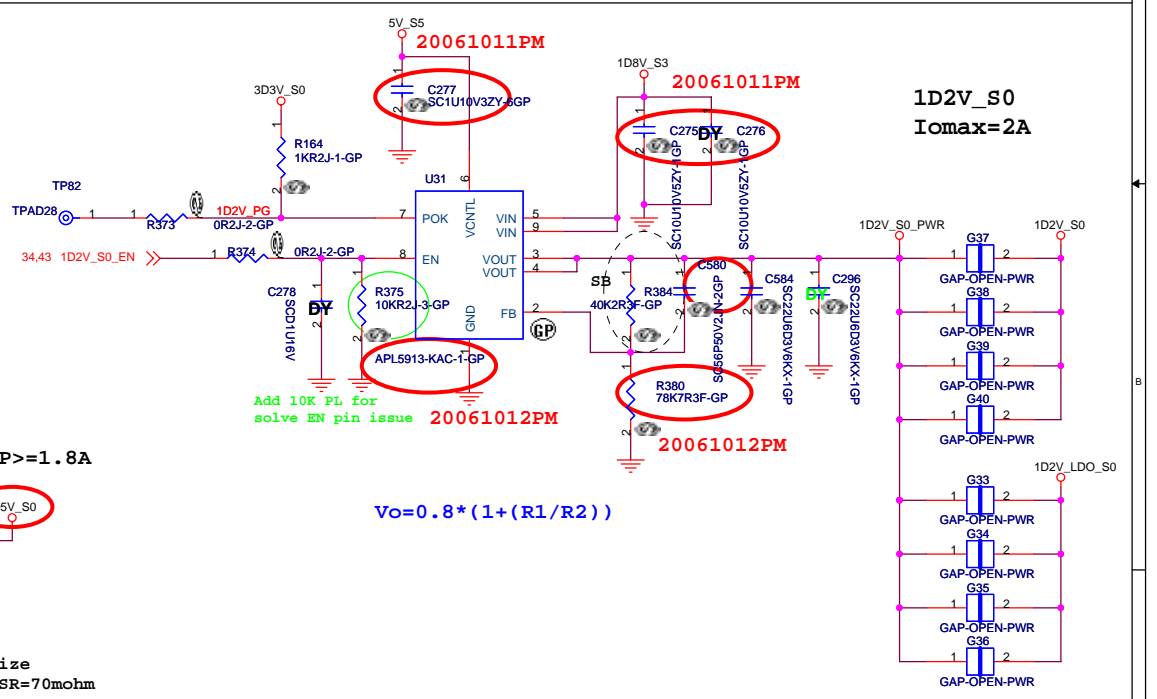
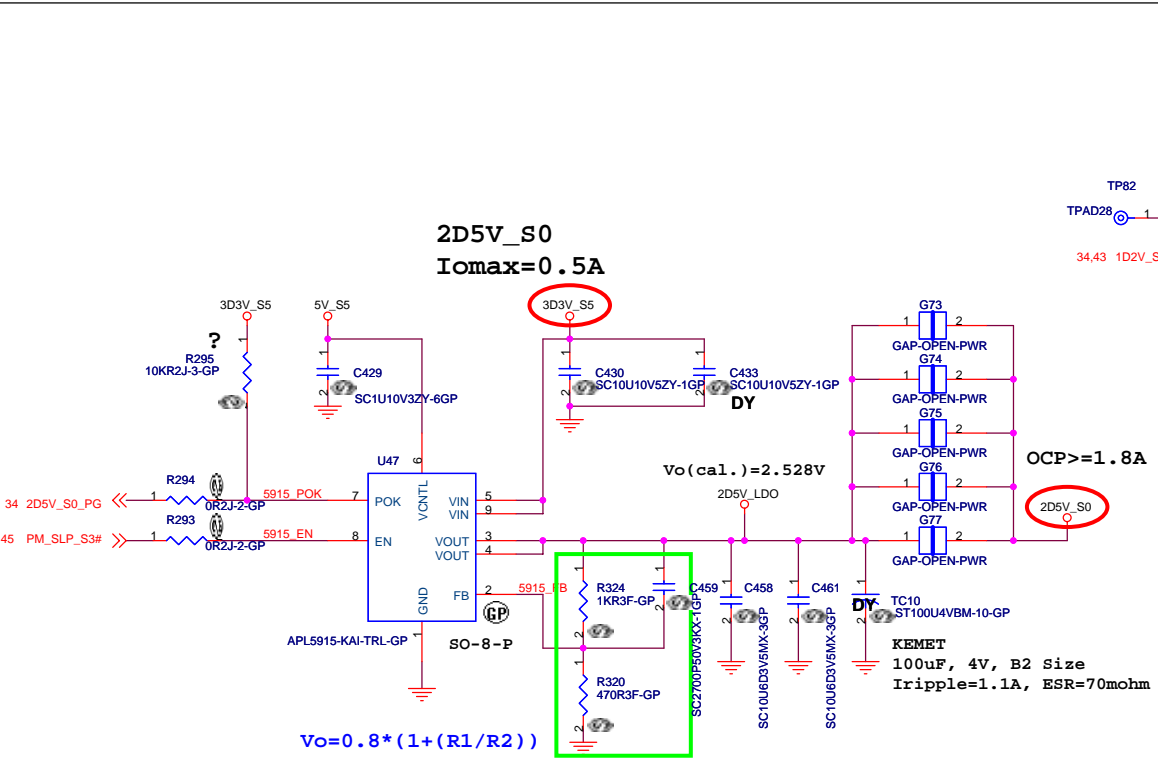
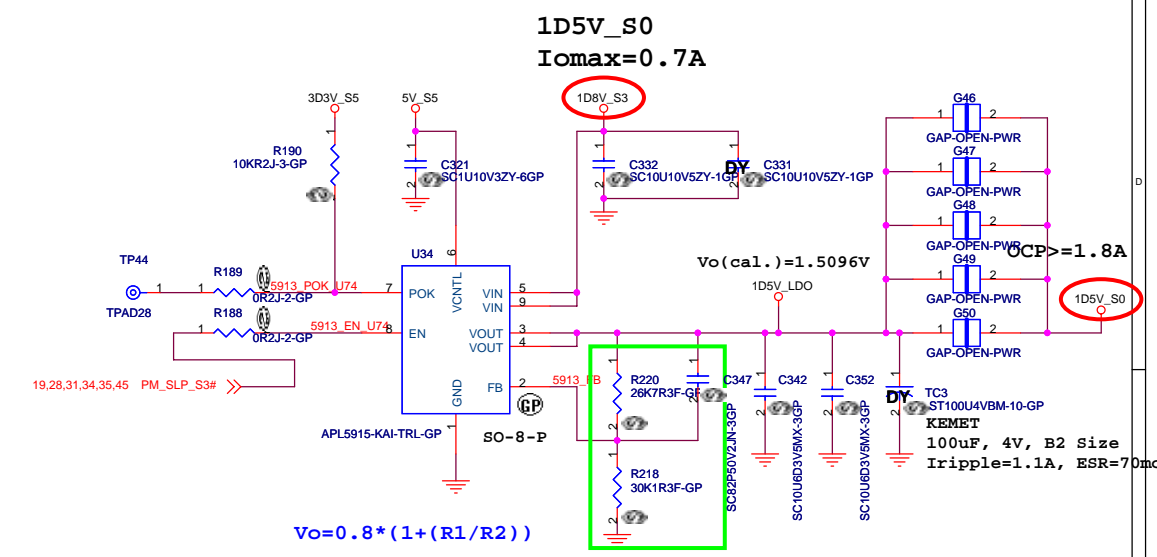
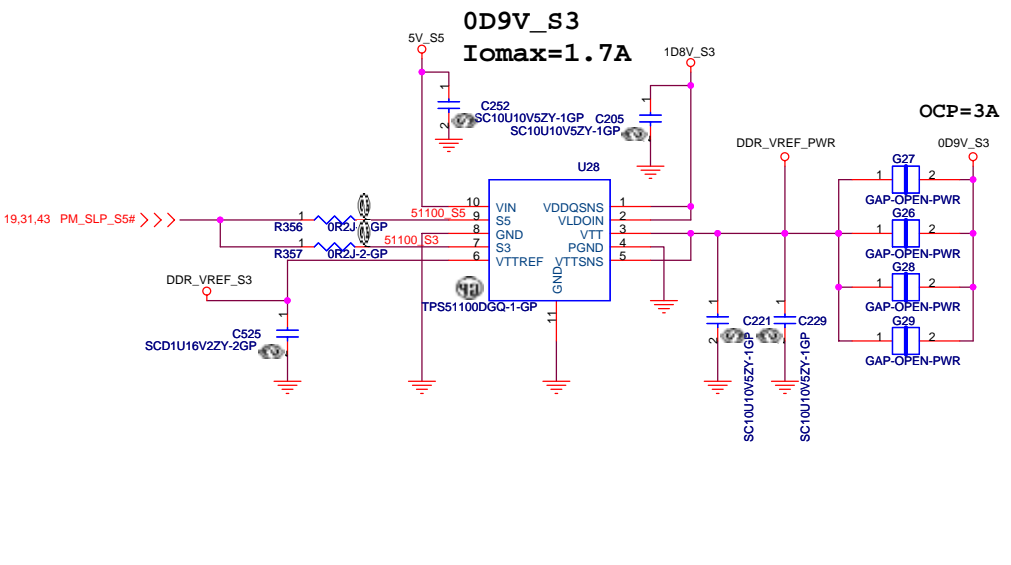
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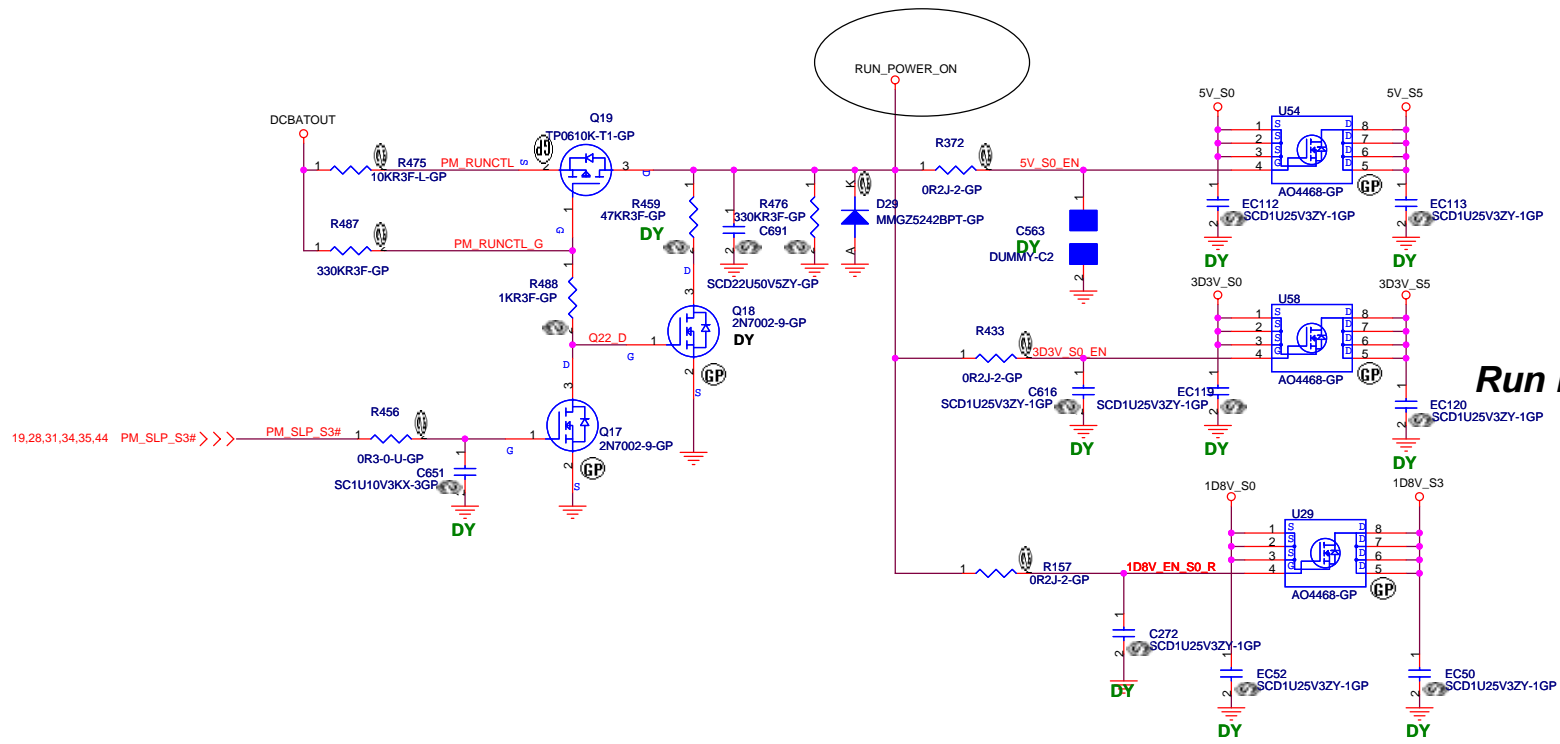
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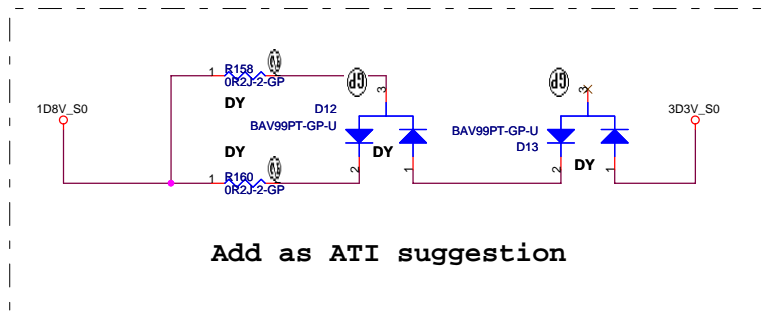
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Title 2D5V/1D5V/0D9V			
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Run Power



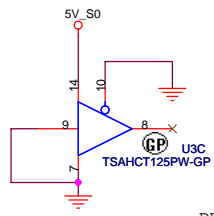
Add as ATI suggestion

Power On Logic

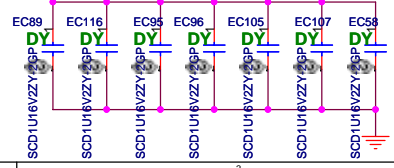
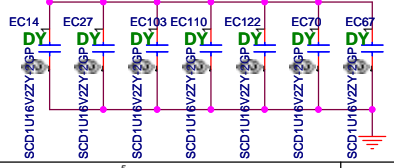
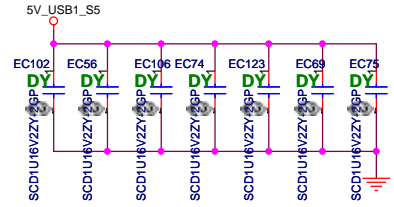
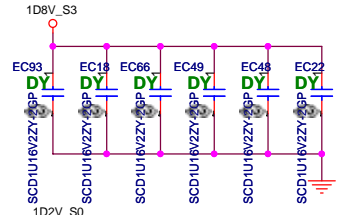
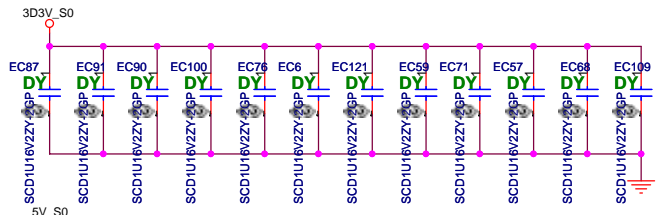
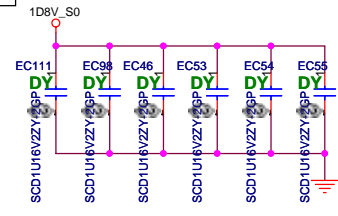
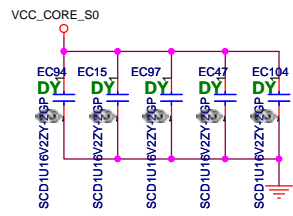
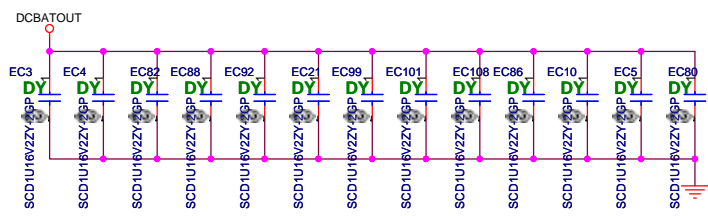
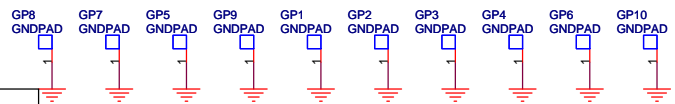
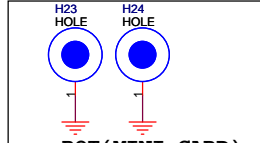
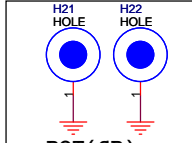
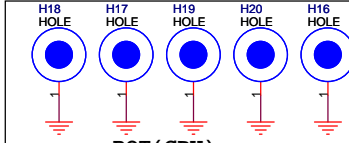
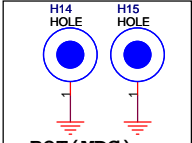
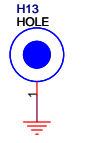
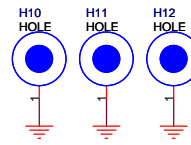
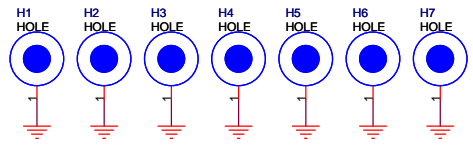
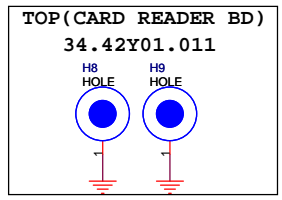
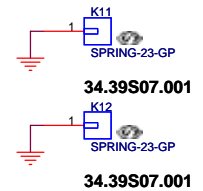
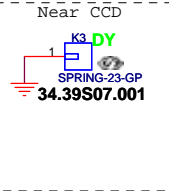
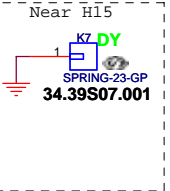
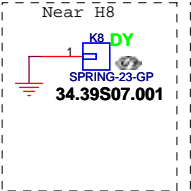
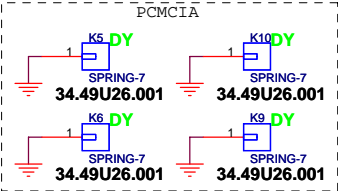
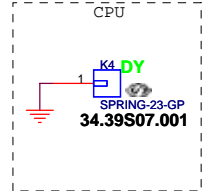
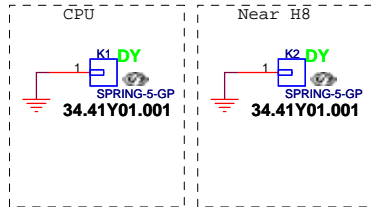
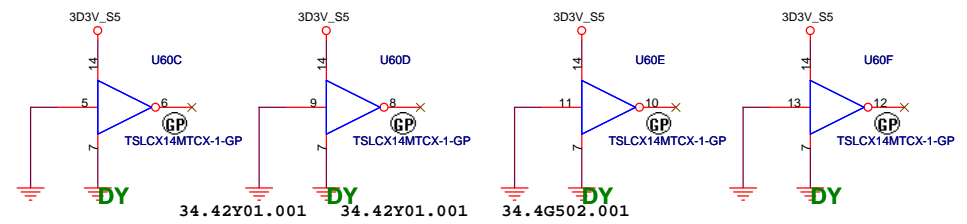
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Title: **EMI/Spring/Boss**

Size: Document Number: **Orta** Rev: SA

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