偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT7525

PC POWER SUPPLY SUPERVISOR

Data Sheet

REV. 0.40 Preliminary release

February 21, 2005

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GENERAL DESCRIPTION

The WT7525 provides protection circuits, power good output (PGO), fault protection latch (FPOB), and a protection detector function (PSONB) control. It can minimize external components of switching power supply systems in personal computer.

The Over / Under Voltage Detector (OVD / UVD) monitors V33, V5, V12A, V12B and V12C input voltage level. The Over Current Detector (OCD) monitor IS33, IS5, IS12A, IS12B and IS12C input current sense. When OVD or UVD or OCD detect the fault voltage level, the FPOB is latched HIGH and PGO go low. The latch can be reset by PSONB go HIGH. There is 3.5 ms delay time for PSONB turn off FPOB.

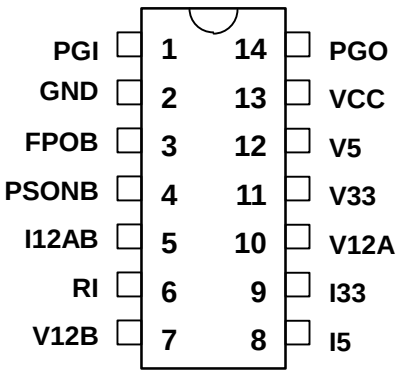
When OVD and UVD and OCD detect the right voltage level, the power good output (PGO) will be issue.

FEATURES

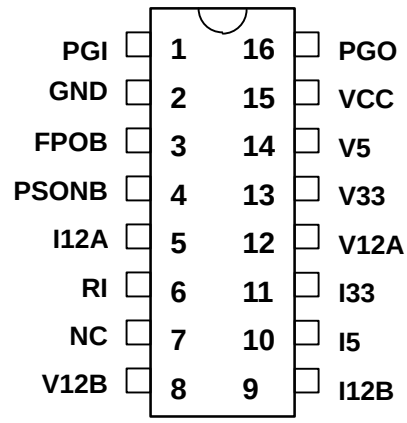
- The Over/Under Voltage Detector (OVD / UVD) monitors V33, V5, V12A, V12B and V12C input voltage.
- The Over Current Detector (OCD) monitors IS33, IS5, IS12A, IS12B and IS12C input current sense.
- Both of the power good output (PGO) and fault protection latch (FPOB) are Open Drain Output.
- 75 / 300 ms time delay for UVD.
- 300 ms time delay for PGO.
- 38 ms for PSONB input signal De–bounce.
- 73 us for PGI/OVD/UVD internal signal De–glitches.
- 1.2 ms for OCD internal signal De–glitches.
- 3.5 ms time delay for PSONB turn-off FPOB.

PIN ASSIGNMENT AND PACKAGE TYPE

WT7525-140



WT7525-160



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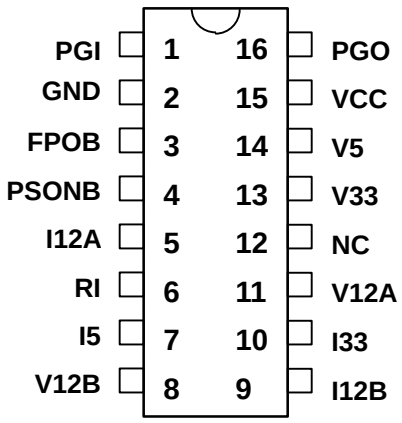

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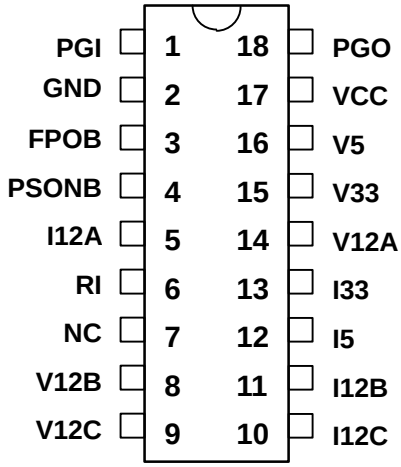

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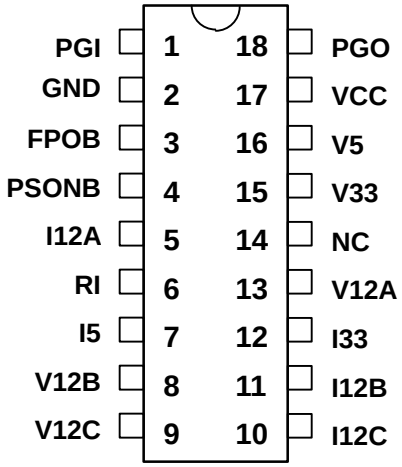


ORDERING INFORMATION

PACKAGE	14–Pin Plastic DIP	14–Pin Plastic SOP
	WT7525–N140	WT7525–S140
Lead–Free（Pb）	WT7525–N140 Pb	WT7525–S140 Pb

PACKAGE	16–Pin Plastic DIP	16–Pin Plastic SOP
	WT7525–N160 WT7525–N161	WT7525–S160 WT7525–S161
Lead–Free（Pb）	WT7525–N160 Pb WT7525–N161 Pb	WT7525–S160 Pb WT7525–S161 Pb

PACKAGE	18–Pin Plastic DIP	18–Pin Plastic SOP
	WT7525–N180 WT7525–N181	WT7525–S180 WT7525–S181
Lead–Free（Pb）	WT7525–N180 Pb WT7525–N181 Pb	WT7525–S180 Pb WT7525–S181 Pb

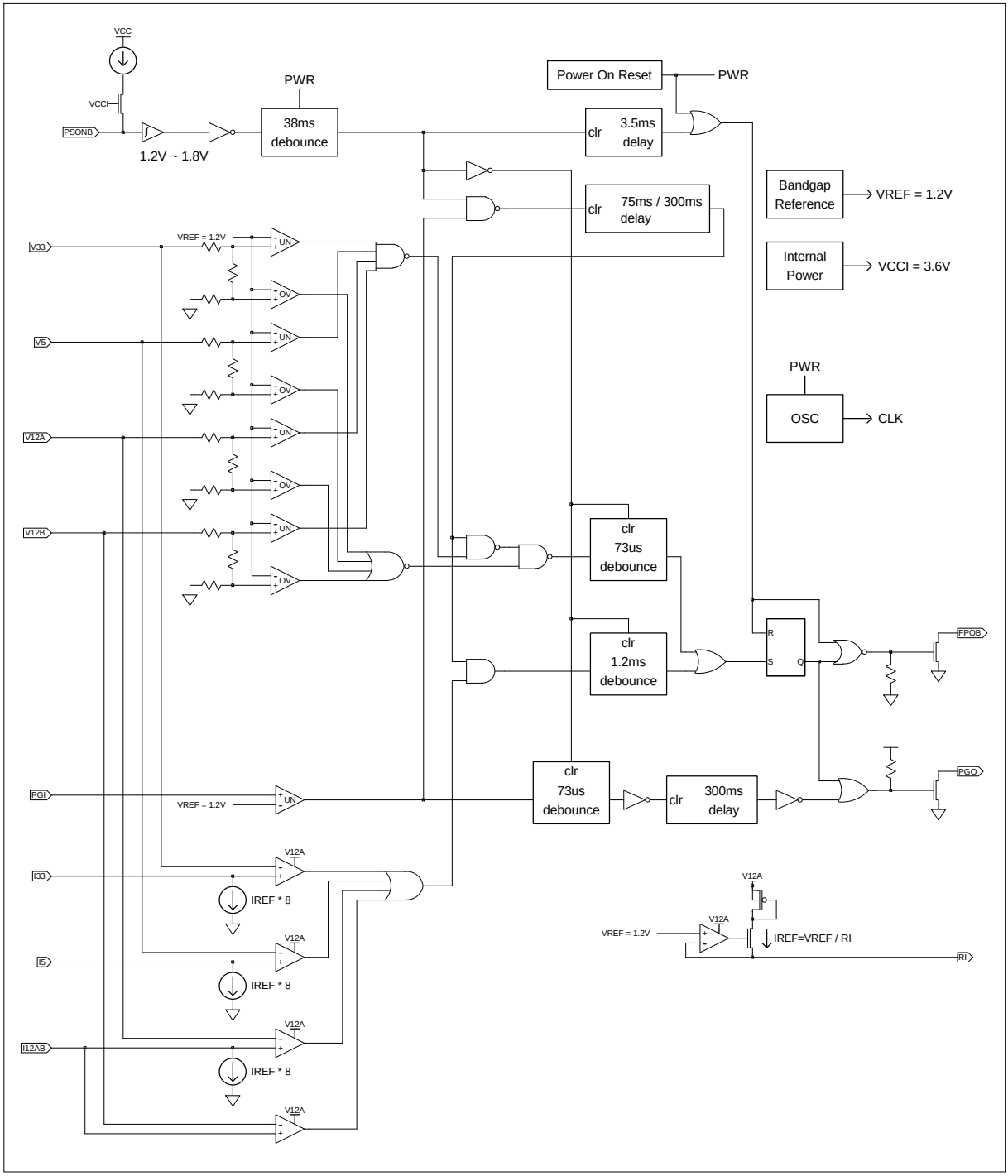
※ **The Top-Side Marking would be added a dot（●）in the right side for lead-free package.**

PIN DESCRIPTION

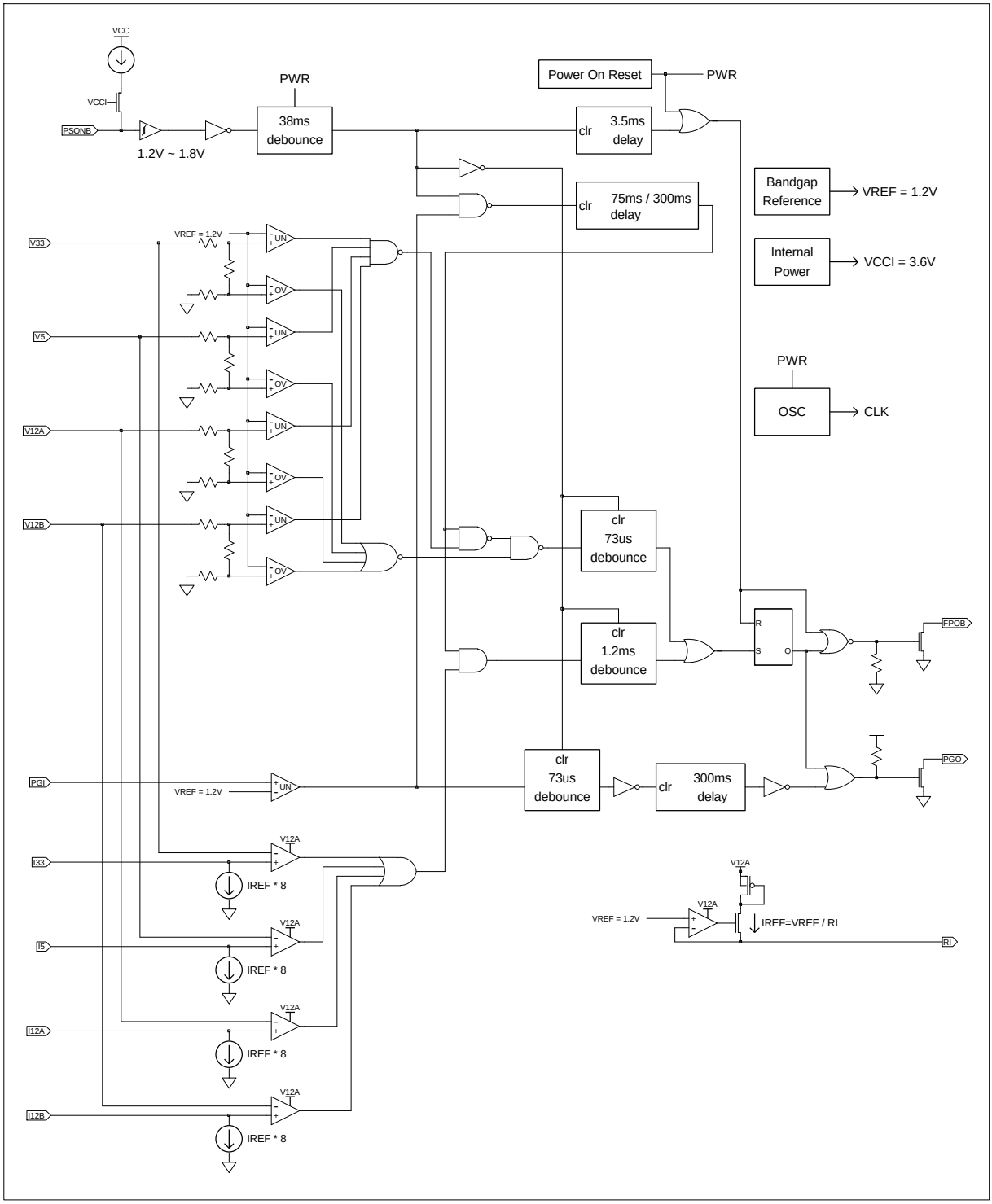
Pin Name	TYPE	Description
PGI	**I**	Power good input signal pin
GND	**P**	Ground
FPOB	**O**	Fault protection output pin, open drain output
PSONB	**I**	On/Off switch input
I12A	**I**	12VA over current protection sense input
I12AB	**I**	12VA / 12VB over current protection sense input (only for 140)
RI	**I**	Current sense adjust input
V12B	**I**	12VB over/under voltage input pin
V12C	**I**	12VC over/under voltage input pin
I12C	**I**	12VC over current protection sense input
I12B	**I**	12VB over current protection sense input
I5	**I**	5V over current protection sense input
I33	**I**	3.3V over current protection sense input
V12A	**I**	12VA over/under voltage input pin
V33	**I**	3.3V over/under voltage input pin
V5	**I**	5V over/under voltage input pin
VCC	**I**	Power supply
PGO	**O**	Power good output signal pin, open drain output

BLOCK DIAGRAM

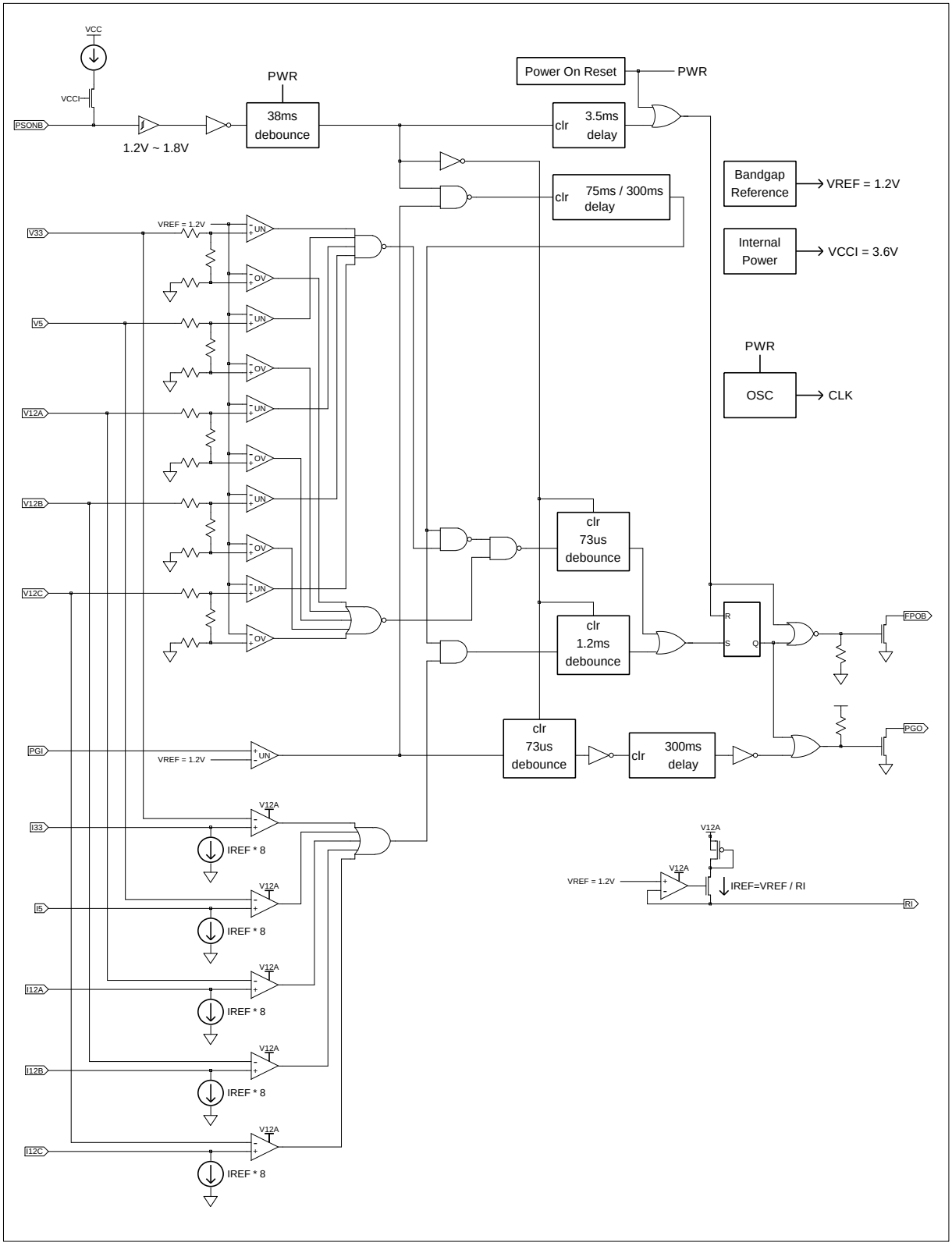
WT7525-140



WT7525-160 / 161



WT7525-180 / 181



ABSOLUTE MAXIMUM RATINGS

Parameter		Min.	Max.	Unit
Supply voltage, VCC, V12A		–0.3	16	V
Input voltage	PGI, PSONB	–0.3	VCC + 0.3（Max. 7V）	V
	V5, V33, I5, I33	–0.3	V12A + 0.3（Max. 7V）	V
	V12B, I12A, I12B, I12AB V12C, I12C	–0.3	V12A + 0.3（Max. 16V）	V
Output voltage	PGO	–0.3	7	V
	FPOB	–0.3	16	V
Operating temperature		-40	125	℃
Storage temperature		-55	150	℃

*Note: Stresses above those listed may cause permanent damage to the devices

RECOMMENDED OPERATING CONDITIONS

Parameter		Conditions	Min.	Typ.	Max.	Unit
Supply voltage, VCC			4	12	15	V
Input voltage	PGI, PSONB, V5, V33				7	V
	V12A, V12B, V12C				15	V
Output voltage	PGO				7	V
	FPOB				15	V
Output sink current	FPOB	0.3V			10	mA
	PGO	0.3V			10	mA
Supply voltage rising time			1			ms
Output current for RI	RI		10		65	uA

ELECTRICAL CHARACTERISTICS, at Ta=25°C and V_{CC}=5V.

Over Voltage Detection

Parameter		Condition	Min.	Typ.	Max.	Unit
Over voltage threshold	V33		3.7	3.9	4.1	V
	V5		5.7	6.1	6.2	V
	V12ABC		13.3	13.8	14.3	V
$I_{LEAKAGE}$ Leakage current (FPOB)		V(FPOB) = 5V		5		uA
V_{OL} Low level output voltage (FPOB)		I_{sink} =10mA			0.3	V

PGI and PGO

Parameter		Condition	Min.	Typ.	Max.	Unit
Under voltage threshold	V33		2.55	2.69	2.83	V
	V5		4.1	4.3	4.47	V
	V12ABC		9.5	10	10.5	V
Input threshold voltage(PGI)			1.16	1.20	1.24	V
$I_{LEAKAGE}$ Leakage current(PGO)		PGO = 5V		5		uA
V_{OL} Low level output voltage(PGO)		I_{sink} =10mA			0.3	V
Offset Voltage of OCP comparators			–6		6	mV

PSONB

Parameter	Condition	Min.	Typ.	Max.	Unit
Input pull-up current	PSONB= 0V		150		uA
High-level input voltage		1.8			V
Low-level input voltage				1.2	V

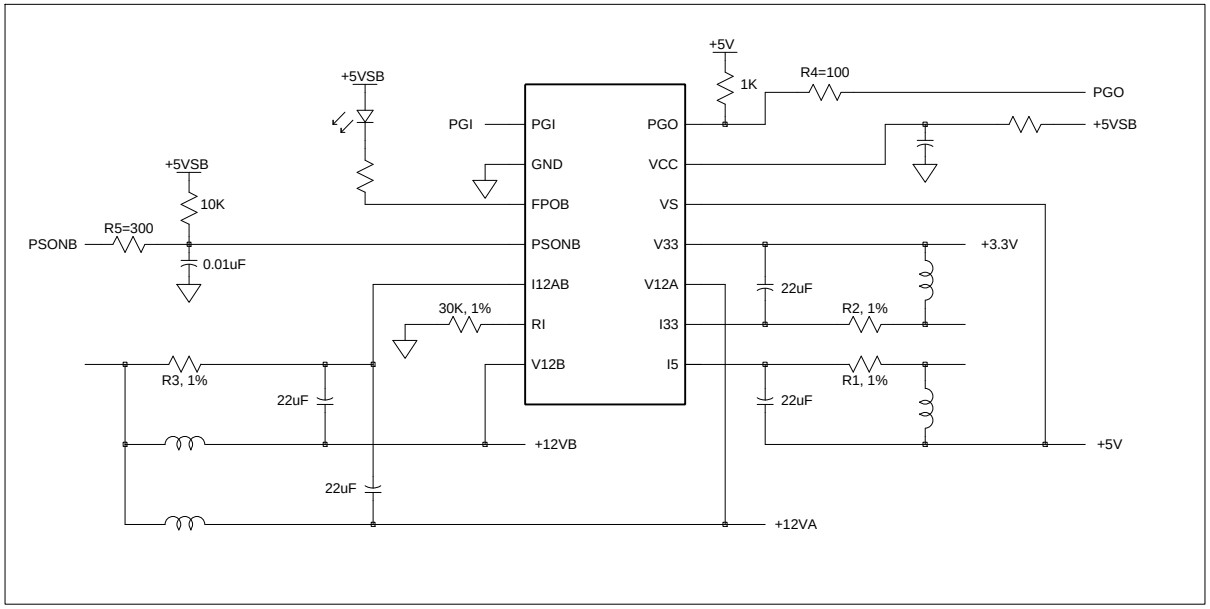
TOTAL DEVICE

Parameter	Condition	Min.	Typ.	Max.	Unit
Icc Supply current	PDON _N= 5V			1	mA
Vcc start-up voltage			3.6		V
Vcc stop voltage after start-up			2.0		V

SWITCHING CHARACTERISTICS, Vcc=5V

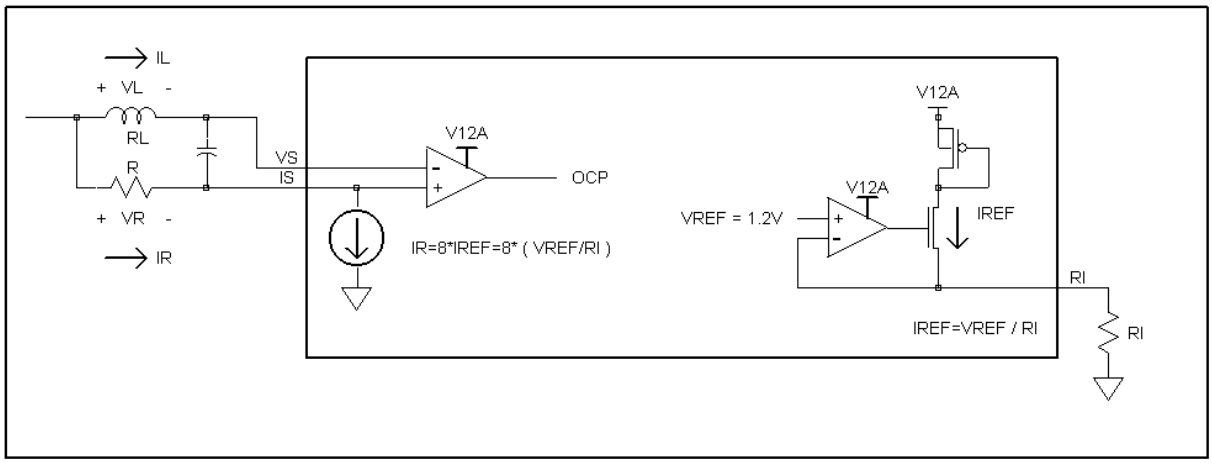
Parameter	Condition	Min.	Typ.	Max.	Unit
t_{db1} De-bounce time (PSONB)		24	38	52	mS
t_{delay1} Delay time (PGI to PGO)		200	300	400	mS
t_{db2} De-bounce time (PSONB)		24	38	52	mS
t_{g1} De-glitch time for PGI		47	73	100	uS
t_{g2} De-glitch time for OVD / UVD		47	73	100	uS
t_{g3} De-glitch time for OCD		0.8	1.2	1.5	mS
t_{delay2} PSONB to FPOB delay time		t_{db2}+2.0	t_{db2}+3.5	t_{db2}+5.0	mS
t_{delay3} Internal UVD/OCD delay time	after FPOB go low & PGI > 1.2V	49	75	100	mS
	after FPOB go low & PGI < 1.2V	200	300	400	mS

APPLICATION CIRCUIT



NOTE1：The series resistor R5 at PSONB can not be omitted. （R0 = 300Ω is suggested）
NOTE2：The series resistor R4 = 100Ω at PGO is suggested.

APPLICATION NOTE



When the current cross inductor raised, inductor voltage raised.
And when inductor voltage exceeded resistor voltage, the OCP active.
We can setup OCP point by the following equation

Let VR = VL
R * IR = RL * IL
∵ IR = 8 * IREF
R * (8 * VREF / RI) = RL * IL
R = (RL * IL) / (8 * VREF / RI) ——— (1)

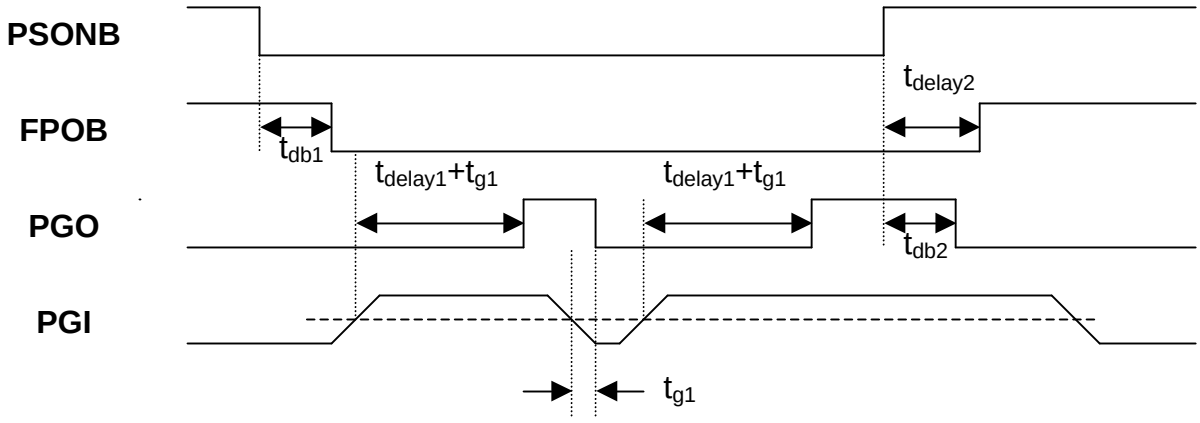
And the capacitor C is used to avoide power on fail or dynamic load fail. We suggest C > 1uF.

EX：How to select the resistor of R? Assume RI=30KΩ, RL=5mΩ, OCP IL=20A。

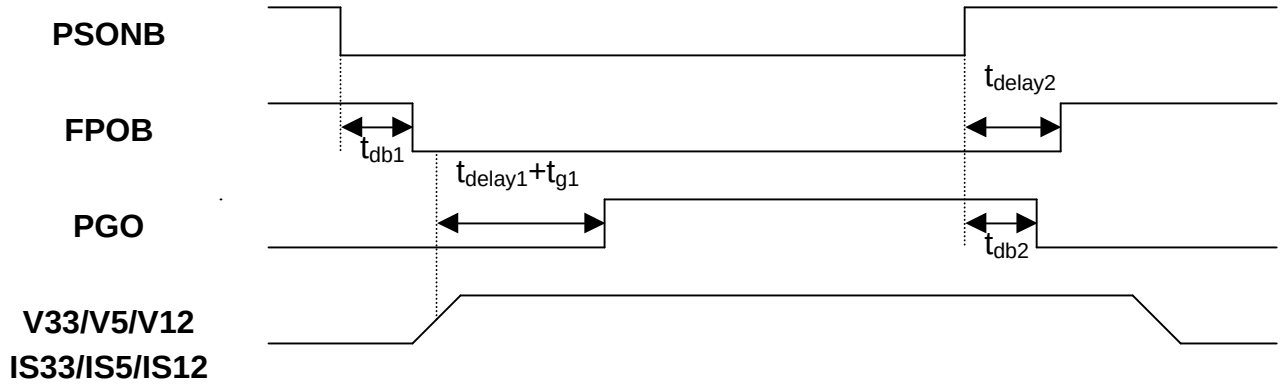
Sol：R = (IL * RL) / (8 * IREF)
= (20A * 5mΩ) / { 8 * (1.2V / 30KΩ)}
= 312.5Ω

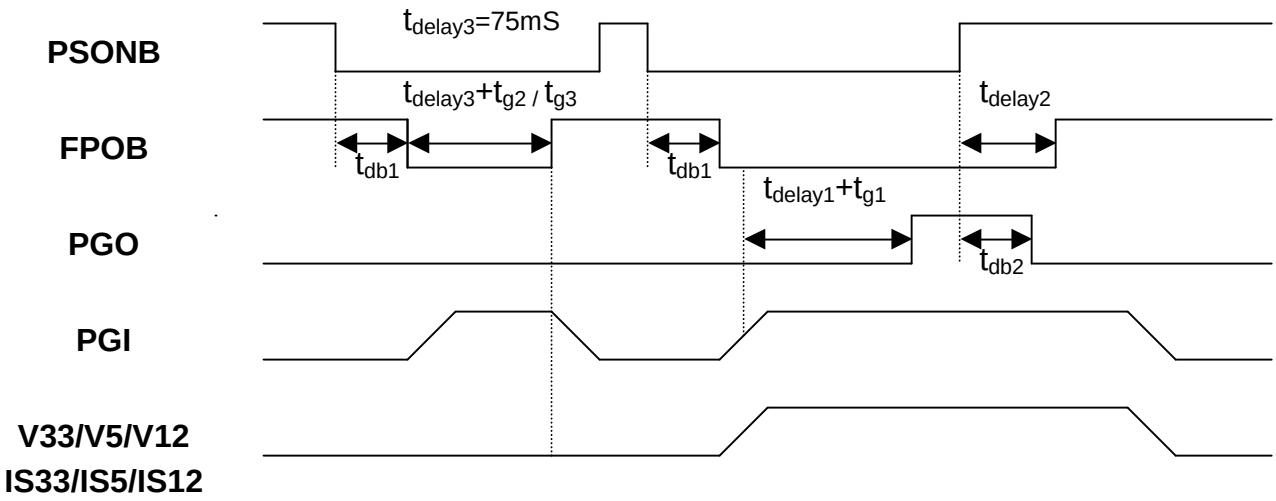
APPLICATION TIMMING

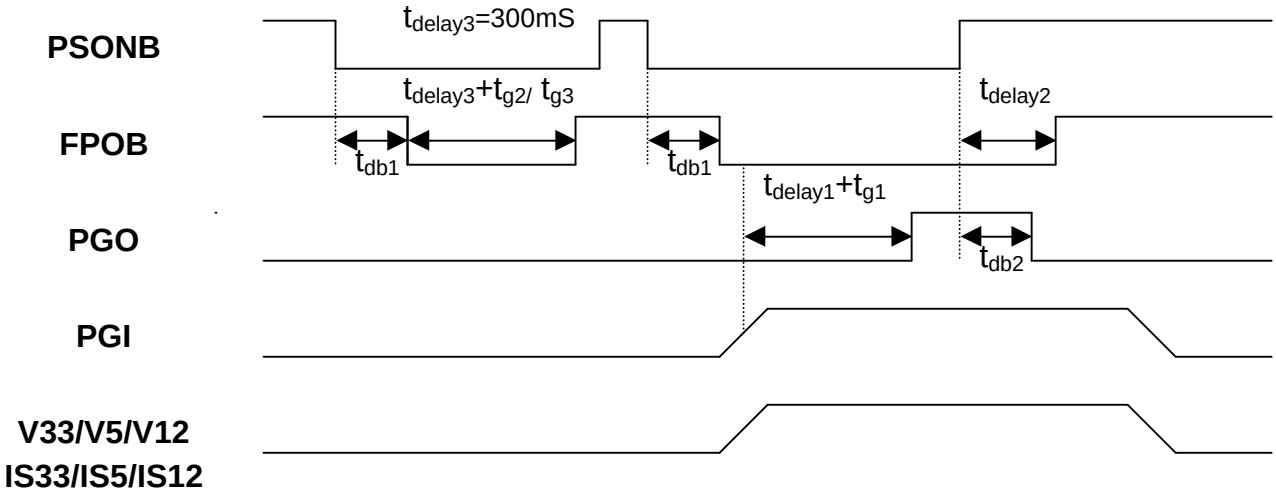
1.) PGI (UNDER_VOLTAGE)：



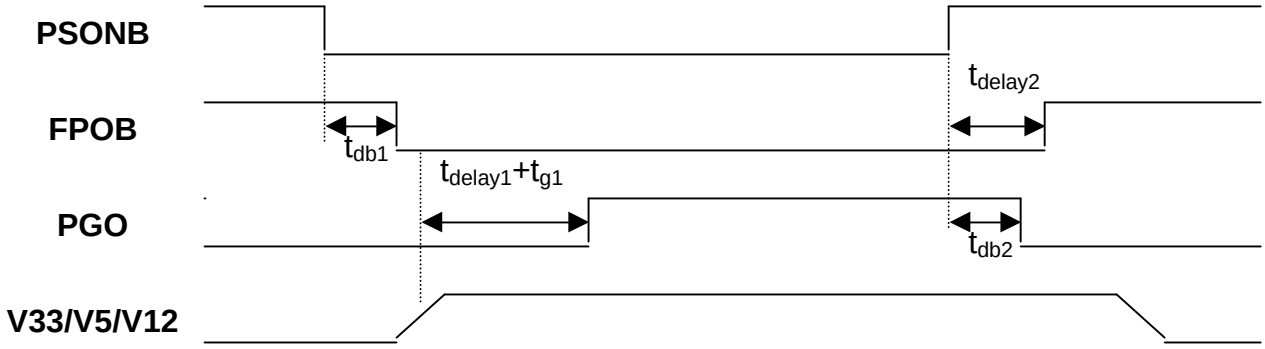
2.) V33, V5, V12 (UNDER_VOLTAGE) or IS33, IS5, IS12 (OVER_CURRENT)：

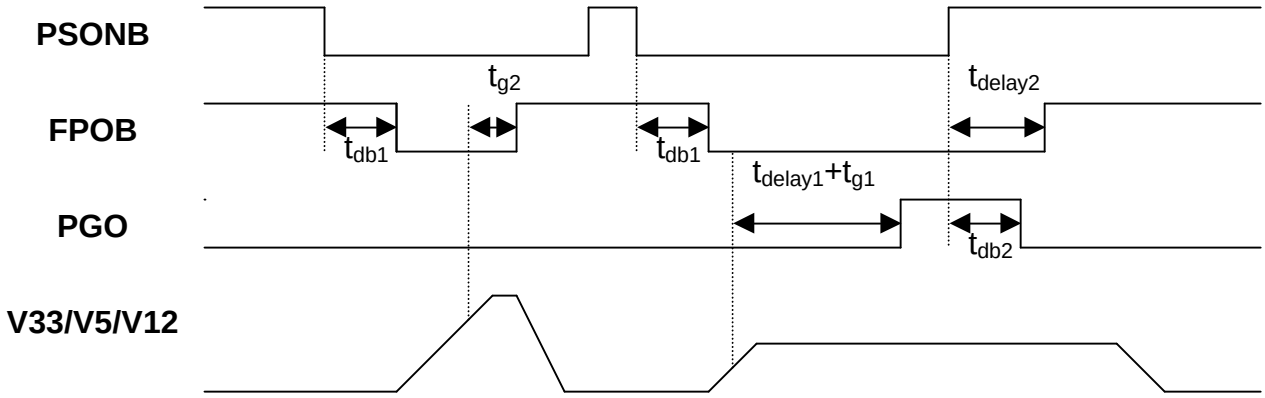






3.) V33, V5, V12 (OVER_VOLTAGE)：

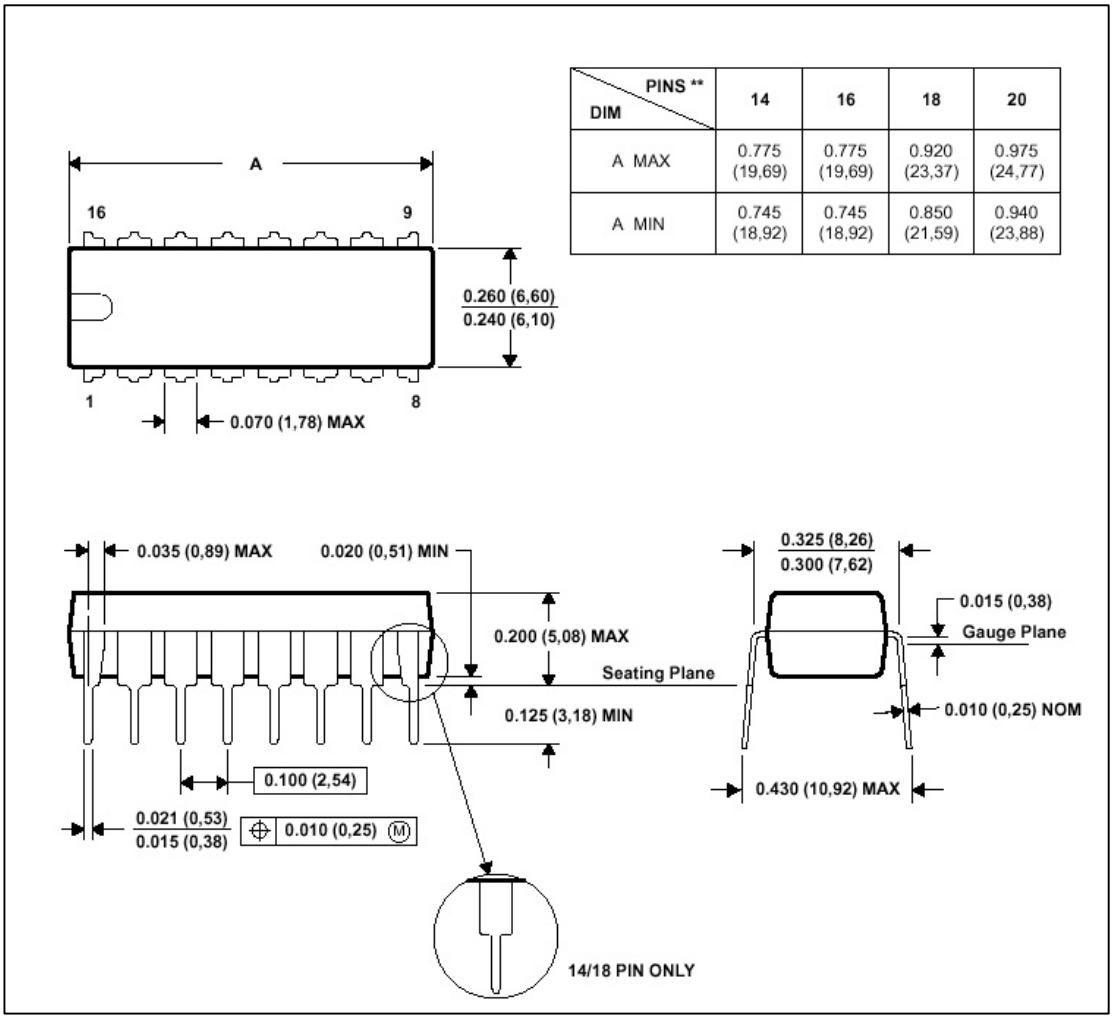




MECHANICAL INFORMATION

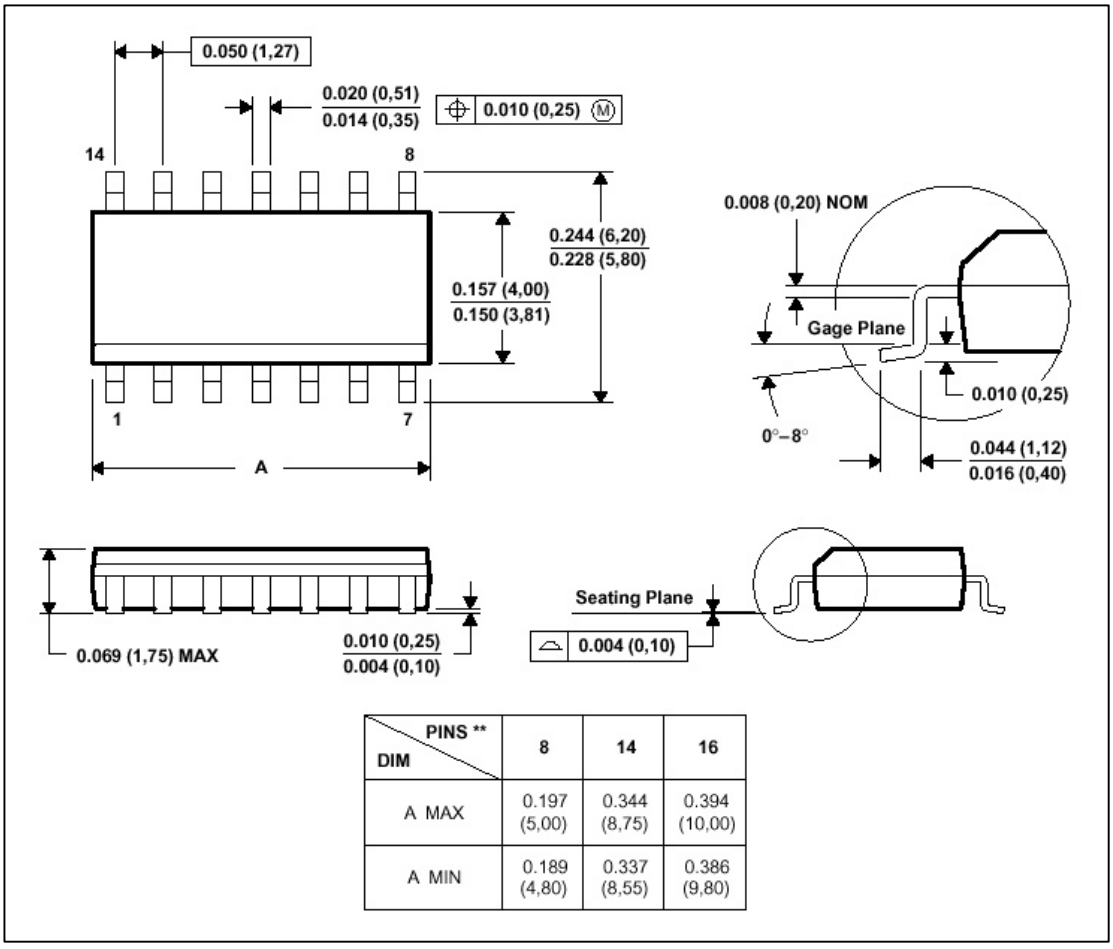
PLASTIC DUAL–IN–LINE 14 / 16 / 18 PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–001

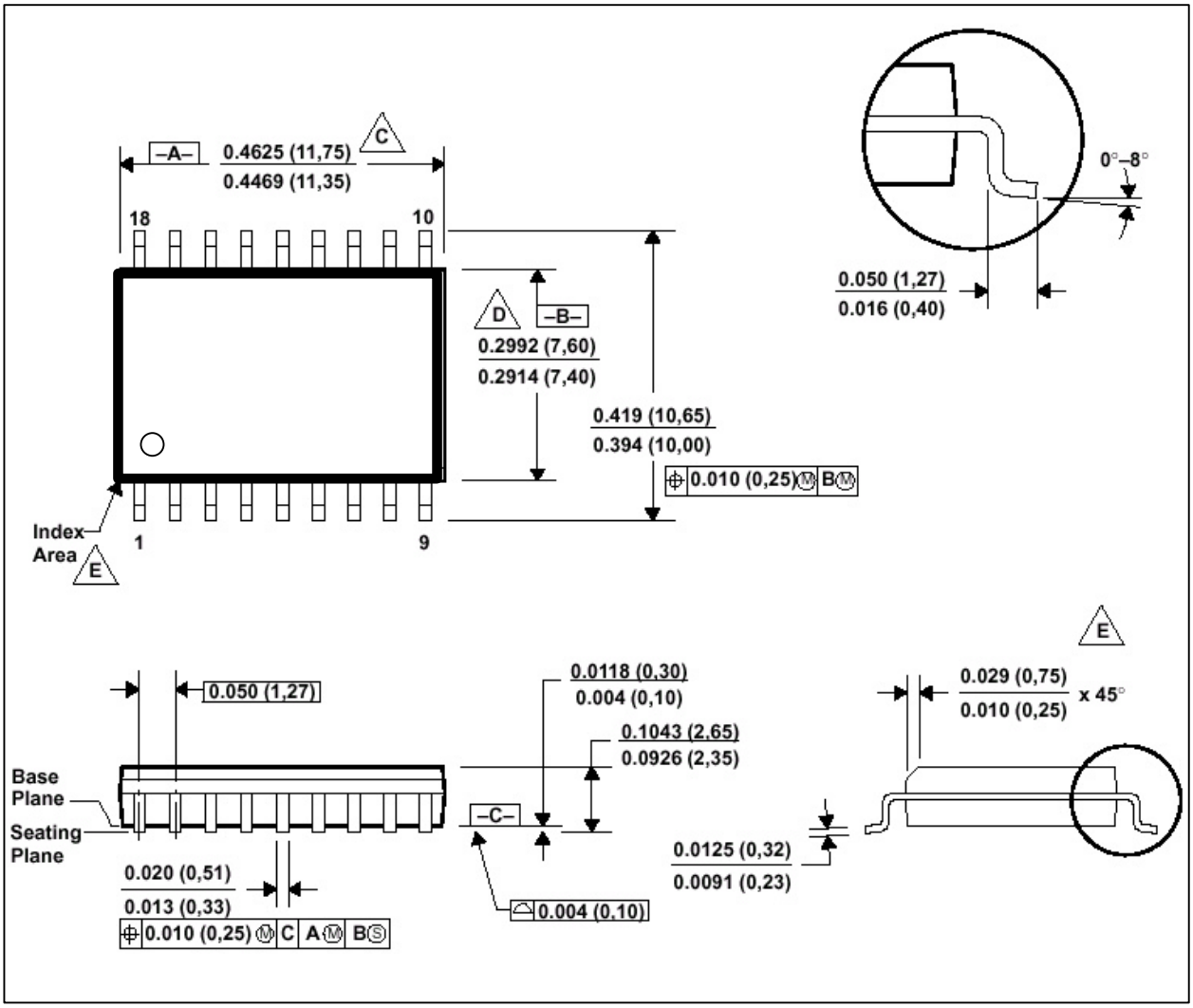
PLASTIC SMALL–OUTLINE 14 / 16 PACKAGE



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–012

PLASTIC SMALL–OUTLINE 18 PACKAGE



NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–013 AB
NOTE 4：Body length dimensions A does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006in (0.15mm) per side.
NOTE 5：Body width dimensions B does not include inter–lead flash or protrusions. Inter–lead flash and protrusions shall not exceed 0.010in (0.25mm) per side.

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