Broadcast Products
P.O. Box 68, White Haven, PA 18661 Phone: (570) 443-9575 FAX: (570) 443-9257

TU1000F V/U

SOLID STATE
1000W UHF TRANSLATOR

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TU1000F V/U

SOLID STATE
1000W UHF TRANSLATOR

02/00

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THE TU1000F V/U TRANSLATOR

SECTION I

THE TU1000F V/U TRANSLATOR

1.1 Introduction:

The EMCEE TU1000F V/U Translator is rated to provide 1000 watts peak visual and 50 watts average aural power on any FCC specified channel extending from 470 to 806MHz. The TU1000F is completely solid-state providing maximum performance and reliability. It is comprised of a Receiver Drawer, a 20 Watt UHF Exciter/Upconverter, two Dual 300W Power Amplifier assemblies and a panel for power distribution and metering. The TU1000F is easy to service and maintain while RF alignment is practically nonexistent. A number of front panel indicators are included which display the results of the translator's diagnostic/control circuitry.

The TU1000F Translator is designed for the express purpose of broadcasting as authorized by the U.S. Federal Communications Commission under Part 74, Subpart G, of the FCC Rules and Regulations.

1.2 Specifications:

Output Power	1000W peak visual 50W average aural
Emissions	5M75C3F visual 250KF3E aural
Color Transmission	NTSC, PAL, or SECAM
Output Frequency Range	470-806MHz
Input Frequency Range	54-88MHz (FCC Ch. 2-60) 174-216MHz (FCC Ch. 7-13) 470-806MHz (FCC Ch. 14-69)
Frequency Stability	±1kHz
Visual Output Power Stability	±0.5dB
Spurious Products	−60dB below peak sync
Harmonics	−60dB below peak sync
In-band Intermodulation (IM_3)	−52dB below peak sync
Differential Gain	5%
Differential Phase	±3°
Frequency Response	±1.0dB

Envelope Delay	±50nsec
Output Impedance	50 ohms (7/8" EIA flange connector)
RF Input Level	−70dBm to −30dBm
RF Input Impedance	50 ohms unbalanced (N connector)
Video Signal to Noise	−50dB @ −47dBm in
Audio Distortion	<1%
Aural FM Noise	<−55dB
Ambient Temperature	−30°C to +50°C
Power Requirements	230Vac ± 15% @ 50/60Hz, 3.8kW
Mechanical Dimensions	69"H x 23"W x 29"D
Weight	350 lb.

1.3 Installation:

Except where otherwise noted, the connectors mentioned in the following instructions are located on the rear of the translator.

1. After unpacking the translator, a thorough inspection should be conducted to reveal any damage which may have occurred during shipment. If damage is found, immediately notify the shipping agency and advise EMCEE Broadcast Products Customer Service or its field representative. Also check to see that any connectors, cables or miscellaneous equipment, which may have been ordered separately, are included.

2. Place the translator in a clean, weatherproof environment providing adequate ventilation for the exhaust fans at the top of the cabinet. It is important to maintain the translator's ambient temperature within the −30°C and +50°C limits. Cooler ambient temperatures will provide increased reliability.

3. Place the translator in its permanent location near a single-phase receptacle that supplies 230Vac at 50/60Hz. The ac source should have a minimum power capacity of 5kW.

> IMPORTANT
>
> Do not apply ac power to the translator at this time since its RF output must be properly terminated before being placed in operation.

4. Set all circuit breakers and switches, including the customer's incoming ac line breaker, to the OFF position. Place an appropriate ac power line protector (surge suppressor) across the ac line that supplies the translator.

5. With the appropriate cables (customer supplied), connect the receiving antenna to the RF IN "N" connector located on the top rear panel of the translator cabinet.

6. Connect the transmitting antenna cable to the 7/8" EIA flange connector marked RF OUTPUT located at the top, rear, right-hand corner of the cabinet (as seen from the front).

7. Verify that the power cords of the Receiver and Exciter drawers are plugged into the receptacle at the bottom of the cabinet inside the rear door. Check all other factory installed RF cables and DC wire harnesses for tight connections.

8. Using the 4-prong, twist lock, female plug supplied with the translator, fabricate an ac power cord and plug it into the translator's AC MAINS connector at the top left rear (as seen facing the front of the cabinet) of the translator's cabinet. Connect the other end of the power cord into an appropriate electrical outlet.

1.4 Operation:

Assuming the installation instructions of Section 1.3 have been completed and the translator is receiving a signal of appropriate frequency and amplitude, proceed with the following steps to place the translator in operation. Except where otherwise noted, the controls, switches, and indicators mentioned in these steps are located on the front of the translator.

1. Close the transmission site's ac mains breaker. Place the Receiver front panel OPERATE/ ALIGN switch to OPERATE and its AC POWER circuit breaker to ON. Verify that the CARRIER PRESENT indicator is illuminated green.

2. Turn the Exciter/Upconverter POWER ADJUST control fully counterclockwise and place its OPERATE/STANDBY switch to STANDBY, its OPERATE/ALIGN switch to OPERATE. Place the Control/Metering Panel's AC POWER circuit breaker and the Exciter POWER ON breaker both to the on/up position. Then verify the following responses of the translator:

    a. The fans of the translator should be operating. The Exciter exhausts air out the rear of the drawer while the Power Amplifier drawer exhausts air through the cabinet top with the aid of cabinet-mounted exhaust fans.

    b. The Exciter's OPERATE, SYNTH LOCK, and DRIVER AMP indicators should be illuminated green.

    c. The Exciter's TEMP EXCITER, ON, FINAL BIAS and VSWR OVLD indicators should be extinguished.

    d. The TEMPERATURE, VSWR OVLD and COLLECTOR BIAS indicators of each Power Amplifier should be extinguished.

    e. The Control/Metering Panel's four Amplifier Status indicators should be illuminated green.

3. Place the Exciter's OPERATE/STANDBY switch to OPERATE. Then verify the following responses of the translator:

   a. The Exciter's OPERATE, SYNTH LOCK and DRIVER AMP indicators should remain illuminated green.

   b. The Exciter's ON and FINAL BIAS indicators should be illuminated green while the VSWR OVLD and TEMP indicators remain extinguished.

   c. The TEMPERATURE indicator of each Power Amplifier drawer should remain extinguished while the COLLECTOR BIAS indicators are illuminated green.

   d. The Control/Metering Panel's AMPL 1 through AMPL 4 indicators should remain illuminated green.

4. Place the Control/Metering Panel's meter switch to FWD and turn the Exciter's POWER ADJUST control clockwise until a 100% indication appears on the Control/Metering Panel's RF POWER meter. Set the Exciter's % meter to display FWD power. Note that the meter may show a reading less than 100%. This is appropriate.

5. Place the Control/Metering Panel's meter switch to REFLD and verify that the meter indicates no more than 10% returned power. If the reflected power is more than 10%, shut down the translator and check the VSWR of the transmitting antenna and its associated cable.

6. Place the Control/Metering Panel's meter switch to FWD for constant monitoring of the translator's final output power.

The translator is now in operation. Check its coverage area for clean, sharp television reception. If the reception or picture quality is unsatisfactory, examine the amount of power delivered to the transmitting antenna (see Section 3.5) and, if necessary, examine the antenna orientation, antenna VSWR, and transmission line VSWR to insure maximum radiation in the proper direction.

1.5 Warranty and Parts Ordering:

Warranty – EMCEE warrants its equipment to be free from defects in material and workmanship for a period of one year after delivery to the customer. Equipment or components returned as defective (prepaid) will be, at our option, repaired or replaced at no charge as long as the equipment or component part in question has not been improperly used or damaged by external causes (e.g., water, ac line transients or lightning). Semiconductors are excepted from this warranty and shall be warranted for a period of not more than ninety (90) days from date of shipment. Equipment or component parts sold or used by EMCEE, but manufactured by others, shall carry the same warranty as extended to EMCEE by the original manufacturer.

Equipment Returns – If the customer desires to return a unit, drawer, or module to EMCEE for repair, follow the procedure described below:

1. Contact EMCEE Customer Service Department by phone or fax for a Return Authorization Number.

2. Provide Customer Service with the following information:

   Equipment model and serial numbers.
   Date of purchase.
   Unit input and output frequencies.
   Part number (PN) and Schematic Diagram designator if a module is being sent.
   Detailed information concerning the nature of the malfunction.

The customer shall designate the mode of shipping desired (e.g., Air Freight, UPS, Fed Ex, etc.). EMCEE will not be responsible for damage to the material while in transit. Therefore, it is of utmost importance that the customer insure the returned item is properly packed.

Parts Ordering – If the customer desires to purchase parts or modules, utilize the following procedure:

1. Contact EMCEE Customer Service by phone or fax indicating the customer's purchase order number. If the purchase order number is provided by phone, written confirmation of the order is required.

2. Also provide:

   The equipment model and serial number.
   The unit input and output frequencies.
   The quantity, description, vendor, number, and designation of the parts needed as found in the Parts Lists subsection of this manual.
   If a module is required, give the part number (PN) and Schematic Diagram designator (e.g., 10331209).
   Designate the mode of shipping desired (e.g., Air Freight, UPS, Fed Ex, etc.).
   Shipping and billing addresses.

Spare and Replacement Parts – The Spare Modules and Components section of this manual provides a detailed listing of the modules and some discrete components contained within the translator. The listing contains those modules or components considered to be essential bench-stock items and should be available to the technician at all times. The Schematic or Interconnection Diagram is the governing document of this manual. Should there be a discrepancy between a modules or components list and a diagram, the diagram takes precedence. Such a discrepancy is possible since manufacturing changes cannot always be incorporated immediately into the instruction manual.

Component Referencing – The translator consists of a number of modules and components mounted in four drawers, a number of components mounted on panels, and several cabinet-mounted components and modules. Components mounted in a module which is included in a drawer take the drawer number and the module number in addition to a component number. Thus the reference designator A2A1Q1 means transistor Q1 in module A1 of drawer A2. Components mounted in a drawer take only the drawer number and a component number (e.g., A2M1 designates meter M1 of drawer A2). Components mounted directly to a panel take only the panel number and a component number. Components and modules mounted directly to the cabinet take only a component or module number.

For EMERGENCY technical assistance, EMCEE offers a toll free, 24-hour, 7-day-a-week customer service hot line: 1-800-233-6193.

SECTION II

CIRCUIT DESCRIPTION

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CIRCUIT DESCRIPTION

2.1 Receiver Drawer:

Interconnection Diagram 30383094/Rev 54 ⋆ A1 (Vectron Oscillator with Multiplier)
Interconnection Diagram 30383104/Rev 55 ⋆ A1 (Synthesizer)

RF IN	−70dBm to −30dBm peak visual
IF OUT	−6dBm
LO SAMPLE	0dBm

The Receiver drawer provides highly selective VHF or UHF to IF signal conversion, IF amplification, and prevention of unauthorized radiation if the proper input signal is not received. Signal conversion is accomplished via a VHF or UHF Bandpass Filter (FL1), and a Downconverter/ Preamplifier (A1). The LO for downconversion is provided by one of six sources depending upon the application. A high stability crystal oscillator (G1) with a X2, X4 or X16 Multiplier (A4) is used when a frequency offset is required when receiving VHF Low Band (Ch.2-6), VHF High Band (Ch.7-13) or UHF (Ch.14-69) respectively. If no frequency offset is required, the corresponding Synthesizer (A4) and 10MHz Reference Oscillator (A5) are used. IF amplification and filtering are furnished through the IF Amplifier w/SAW Filter (A2) and the IF AGC Amplifier (A3). The Aural Notch Filter (FL2) allows for attenuation of the aural carrier to facilitate a reduction of in-band third order intermodulation products or to maintain the minimum visual to aural carrier ratio. Finally, a 6dB attenuator reduces the IF signal to a level that is within the input range of the Exciter/ Upconverter (A2).

The Receiver drawer also insures that the translator does not exceed or deviate from its rated output power while receiving signal variations of up to 40dB (−70dBm to −30dBm). This function is accomplished through a complex gain control system employing the IF AGC Amplifier's variable pin diode attenuator and a Limiter/Output AGC (PC1). The IF AGC Amplifier's variable pin diode attenuator is controlled by the input AGC circuit of the IF AGC Amplifier and the output AGC circuit of the Limiter/Output AGC. As the received signal increases, the input AGC circuit of the IF AGC Amplifier provides an increase in the AGC voltage applied to the variable pin diode attenuator. This condition causes an increase in the attenuation provided by the variable pin diode attenuator. As a result, the IF output of the Receiver drawer is held constant at approximately −6dBm (±1dB) throughout the 40dB variation in the received signal.

The input AGC circuit alone does not provide for controlling changes in amplifier gain occurring after the IF section of the Receiver. (An amplifier's gain may change during warm-up, over long periods of time, and under varying temperatures.) The output gain control circuit of the Limiter/ Output AGC is incorporated to monitor and correct any changes in the translator's output power. The output AGC circuit controls the gain of the IF AGC Amplifier by monitoring the dc voltage that drives the translator's % Power meter. Any deviation from the translator's correct output power will shift the metering voltage, causing the output AGC circuit to vary the biasing on the IF AGC Amplifier's variable pin diode attenuator. The attenuation will vary in such a way that any power fluctuations at the output of the translator will be counteracted.

Should the Receiver drawer experience a temporary loss of signal (fading, etc.), the limiter circuit of the Limiter/Output AGC serves to prevent overdriving the translator's power amplifier modules. (A decrease in the received signal reduces the AGC voltage and consequently increases the gain

of the IF AGC Amplifier.) When the received signal regains its strength, the limiter circuit will momentarily attenuate (–20dB) the IF output of the Receiver drawer until adequate AGC voltage is developed to control the Receiver's overall gain.

In the event of a significant reduction or loss of the Receiver's input signal for more than 30 seconds, an Automatic-On circuit (PC2) will prevent the radiation of noise by shutting down the Receiver. Should the VHF or UHF input signal to the Receiver fall below the minimum acceptable level of –70dBm, the accompanying AGC voltage will fall below a preset Auto-On Threshold voltage. This in turn causes Auto-On relay K1 to de-energize which opens the interlock loop and shuts down the translator.

2.1a VHF/UHF Remote Preamplifier: (OPTIONAL)

Scala Model 8000

Specifications	See Data Pak

2.1b VHF Bandpass Filter:

Schematic A280-92/Rev 1 (Ch.2-6) ★ A1FL1
Schematic A280-89/Rev 1 (Ch.7-13) ★ A1FL1

Frequency Response (J1-J2)	7MHz @ 1dB
Insertion Loss (J1-J2)	2dB Max.

The high band VHF bandpass filter is a two-section overcoupled circuit that rejects all frequencies other than the single VHF channel to which it is tuned. The bandpass filter is adjusted to provide a 7MHz @ 1dB frequency response with an insertion loss of approximately 2dB or less. In the filter, inductors L3 and L4, in conjunction with stagger-tuned capacitors C1 through C4, provide the required bandpass response. Capacitor C5 also effects the response by changing the effective coupling between the two circuits. Impedance matching is accomplished by inductors L1 and L2 along with variable capacitors C1 and C2.

2.1c UHF Bandpass Filter:

Schematic 10331209/Rev 52 (Ch.14-83) ★ A1FL1

Frequency Response	7MHz @ 1dB
Insertion Loss	3dB Max.

The filter is composed of three overcoupled, 1/4 wave coaxial cavities that reject all frequencies other than the single UHF channel to which it is tuned. The UHF Filter provides a 7MHz bandwidth at 1dB and has an insertion loss of 3dB or less. In the filter, components L2, L3 and L4 are solid brass rods acting as 1/4 wave shorted transmission lines. The length of these lines, controlled by variable capacitors C1, C2 and C3, dictates the resonant frequency of the filter. Inductors L1 and L5 link couple the UHF signal into and out of the filter. The position of these two inductors in relation to the 1/4 wave brass rods determines the filter's input and output impedance, as well as

skirt selectivity and insertion loss. The Variable Coupling Barriers regulate the amount of signal passed between the coaxial cavities and therefore control the bandwidth of the filter.

2.1d Crystal Oscillator:

Vectron CO-254D57 ⋆ A1G1

Supply Voltage	28V
Output Power	+7dBm
Operating Temperature	−30°C to +70°C
Stability	±5 x 10^{-7}

The CO-254D57 is a high stability, temperature-compensated crystal oscillator (TCXO) manufactured by Vectron Laboratories, Inc. This oscillator, in conjunction with a X2, X4 or X16 Multiplier, is used in place of the EMCEE Synthesizer when ±10kHz precision offset is required. See the Data Pak for further information.

2.1e X2 Multiplier and X4 Multiplier:

Schematic B280-35/Rev E (Ch.2-6) ⋆ A1A4 (X2 Multiplier)
Schematic C331-24/Rev D (Ch.7-13) ⋆ A1A4 (X4 Multiplier)

	Multiplier	Q1	Q2	Q3
Collector V		25	15	15
Output Power	10-40mW			
Output Frequency	Osc. 2nd/4th Harmonic			

The VHF Multiplier consists of an amplifier and two doubler stages fed by the fundamental frequency of the crystal oscillator. Transistor Q1 is an untuned class A VHF amplifier coupled to a resonated idler loop tuned to the fundamental frequency (series circuit L3 and C7). Transistor Q2 is a class AB X2 frequency multiplier that feeds an LC series circuit (L5, C12) tuned to the second harmonic. Capacitors C13 through C17 and inductors L6 through L8 make up a three-section bandpass filter which passes only the second harmonic frequency. If the multiplier is a X4 type, transistor Q3 is a class C frequency doubler with both input and output tuning. Tuning consists of a second harmonic idler circuit (L9 and C19) at the input and an output network (L12, C22 and C23) that is tuned to the oscillator's 4th harmonic. C26 through C29 and inductors L13 and L14 make up a two-section bandpass filter tuned to pass the oscillator's fourth harmonic. An LO sample (≈1mW) port (J3) is provided on the front panel of the translator drawer for convenient monitoring or mixing.

2.1f X16 Multiplier:

Schematic Diagram 30367226/Rev A ★ A1A4

INPUT power	0 to +10dBm Typical +7dBm
LO OUT (J2)	
Output power	+15dBm Min.
Output frequency	16th harmonic of input

The X16 Multiplier provides three sections of frequency multiplication to generate the LO necessary for downconverting UHF channels to IF.

Section 1 consists of a frequency multiplier (A1), a bandpass filter (FL1), and an amplifier (U1). A1 produces harmonics from the input signal of the crystal oscillator. The desired harmonic from A1 is the fourth, whose level should typically be 30dB below the oscillator level. FL1 is a narrow bandpass filter, which also employs two tunable notch filters. When properly tuned, FL1 has a typical insertion loss of 2 to 2.5dB. The notch filters are tuned to the 3rd and 5th harmonics providing an additional minimum attenuation of 15dB to these harmonics. Output level from FL1 is approximately –28 to –32dBm. U1 is a monolithic amplifier with a typical gain of 33dB at these frequencies. U1 provides the nominal level of 0dBm for the next section of frequency multiplication.

Section 2 consists of a frequency multiplier (A2), a filter FL2, and a two-stage amplifier (U2, U3). A2 produces harmonics of the signal taken from the previous section. The desired frequency from this section is the 2nd harmonic of the input (8th harmonic of OSC.). The output level of A2 at the 2nd harmonic is typically –15dBm. FL2 is a tunable microstrip bandpass filter. The filter has a frequency range of 250-470MHz, an insertion loss of 2dB and is tuned to pass the 2nd harmonic of A2. The output level from FL2 is a nominal –17dBm. U2 and U3 are monolithic amplifiers with a combined typical gain of 25dB. These are used to produce an input level of +8dBm to the third section.

Section 3 consists of a frequency multiplier (A3), two different stages of amplification (U4 and U5, U6), and two filters (FL3, FL4). A3 is used to produce harmonics of the frequency from Section 2. The desired frequency from A3 is the second harmonic of its input (16th of OSC.). Output level of the second harmonic from A3 is typically –6dBm. U4 is used to amplify the output of A3 before filtering by FL3. The output level of U4 at the 2nd harmonic of A3 is at a nominal 2dBm level. FL3 is a tunable microstrip bandpass filter with a frequency range of 500-940MHz and an insertion loss of 2dB. The filter is tuned to the 2nd harmonic of A3. The output level of FL3 is 0dBm. U5 is a monolithic amplifier with a 12dB gain. U5 is run into compression allowing the oscillator level to vary while the output of U5 remains constant. The output of U5 drives U6, another monolithic amplifier with a gain of 11.5dB. This amplifier is also operated in compression for the same reason as U5. The output of U6 is +18 to +20dBm. FL4 is tuned for the second harmonic from A3 and provides additional filtering to suppress the undesired harmonics from previous frequency multiplication. Secondly, the filter removes any additional undesired signals caused by compressing amplifiers U5 and U6. The output level from FL4 is typically +16dBm to +18dBm.

2.1g 10MHz Reference Oscillator:

Schematic Diagram 10368037/Rev B ★ A1A4A2

10MHz REF. OUT (J1, J2)	3.5V P/P square wave

The Reference Oscillator provides a 10MHz reference signal for the Synthesizer (A4A1). This module is centered around a 10MHz temperature-compensated crystal oscillator (G1). The output from G1 is applied to two exclusive-OR gates used as inverting buffers. The output signal from each gate is a 10MHz low-level square wave with a frequency stability of 0.3 parts per million (PPM).

2.1h VHF Synthesizer Low Band:

Schematic Diagram 30362427/Rev C ★ A1A4A1

10MHz REF. IN (J1)	3.5V P/P square wave
LO OUT (J2)	+15.25dBm min.
SYNTH. LOCK (Pin A of J4)	logic high (locked) logic low (unlocked)

The VHF Synthesizer is a phase-lock loop type and uses one of the 10MHz reference signals from the Reference Oscillator (A4A2) and develops a programmable LO signal for the Mixer (MX1) in the Downconverter/Preamplifier (A1). The frequency of the LO signal is calculated as the sum of the visual IF carrier and the visual VHF carrier of the specified input channel. The LO signal's frequency is programmed by the setting of switches S1 through S4 which are accessible through the module's cover. The relationship between the setting of these switches and the resulting LO frequency is provided in Table 2–3 for each VHF channel.

A 10MHz reference signal is brought in from the Reference Oscillator (A4A2) through J1, 10MHz IN. Both sections of U4 perform binary divide-by-5 counting to provide a 400kHz signal to the OSC_{in} input of U1, pin 27. To create U1's internal 50kHz reference signal, U1 performs a binary divide-by-8 operation on the OSC_{in} signal.

Controlling the VCO, G1, is the output of op-amp U3. U3 compares and integrates the $\emptyset_V$ and $\emptyset_R$ phase detector outputs of U1. The output of U3 is filtered to create the dc control voltage for the VCO. The output of G1, RF OUT, is amplified by U5 and available as the Receiver's LO at J2, OUT.

The output of G1 is also amplified by U6 and then fed to a ÷32/÷33 prescaler, U2. After prescaling, the signal is connected to U1 pin 1, F_{in}, from U2 pin 4, OUT, completing the loop. The prescaling factor of U2 is selected by the MOD CONTROL, pin 9, of U1. Switches S1 to S4 set two divide-by-ratios, counters A and N, within U1. When divide-by-A is being performed on the signal at F_{in}, MOD CONTROL is set high, selecting ÷32 in the prescaler, U2. MOD CONTROL goes low for divide-by-N selecting ÷33 in U2.

The A and N counters form a binary number from A0 to N9 with A0 being the LSB and N9 being the MSB. The decimal equivalent of this number, when multiplied by the internal reference frequency 50kHz, gives the synthesizer's output frequency. Hence, for NTSC operation, A0 and A1, pins 21 and 23 on U1, are grounded. For PAL operation, A0 and A1 are made high by cutting

the traces from pins 21 and 23 to ground thereby adding the 150kHz to the LO that is characteristic of the PAL system.

When the synthesizer is locked onto a frequency, LD is high. This saturates Q1 and puts a low on SYNTH LOCK. C28 provides a time delay to ensure that the synthesizer has successfully locked before indicating so on the SYNTH LOCK line. For an unlocked condition, LD pulses low preventing C28 from charging and saturating Q1. +5V is therefore present on the SYNTH LOCK line for the unlocked condition.

2.1i VHF Synthesizer High Band:

Schematic Diagram 30362003/Rev D ★ A1A4A1

10MHz REF. IN (J1)	3.5V P/P square wave
LO OUT (J2)	+15.25dBm min.
SYNTH. LOCK (Pin A of J4)	logic high (locked) logic low (unlocked)

The VHF Synthesizer is a phase-lock loop type and uses one of the 10MHz reference signals from the Reference Oscillator (A4A2) and develops a programmable LO signal for the Mixer (MX1) in the Downconverter/Preamplifier (A1). The frequency of the LO signal is calculated as the sum of the visual IF carrier and the visual VHF carrier of the specified output channel. The LO signal's frequency is programmed by the setting of switches S1 through S4 which are accessible through the module's cover via access holes. The relationship between the setting of these switches and the resulting LO frequency is provided in Table 2–2 for each VHF channel.

A 10MHz reference signal is brought in from the Reference Oscillator (A4A2) through J1, 10MHz IN. Both sections of U4 perform binary divide-by-5 counting to provide a 400kHz signal to the OSC_{in} input of U1, pin 27. To create U1's internal 50kHz reference signal, U1 performs a binary divide-by-8 operation on the OSC_{in} signal.

Controlling the VCO, G1, is the output of op-amp U3. U3 compares and integrates the ϕ_V and ϕ_R phase detector outputs of U1. The output of U3 is filtered to create the dc control voltage for the VCO. The output of G1, RF OUT, is amplified by U5 and available as the Receiver's LO at J2, OUT.

The output of G1 is also amplified by U6 and then fed to a ÷64/÷65 prescaler, U2. After prescaling, the signal is connected to U1 pin 1, F_{in}, from U2 pin 4, OUT, completing the loop. The prescaling factor of U2 is selected by the MOD CONTROL, pin 9, of U1. Switches S1 to S4 set two divide-by-ratios, counters A and N, within U1. When divide-by-A is being performed on the signal at F_{in}, MOD CONTROL is set high, selecting ÷64 in the prescaler, U2. MOD CONTROL goes low for divide-by-N selecting ÷65 in U2.

The A and N counters form a binary number from A0 to N9 with A0 being the LSB and N9 being the MSB. The decimal equivalent of this number, when multiplied by the internal reference frequency 50kHz, gives the synthesizer's output frequency. Hence, for NTSC operation, A0 and A1, pins 21 and 23 on U1, are grounded. For PAL operation, A0 and A1 are made high by cutting the traces from pins 21 and 23 to ground thereby adding the 150kHz to the LO that is characteristic of the PAL system.

When the synthesizer is locked onto a frequency, LD is high. This saturates Q1 and puts a low on SYNTH LOCK. C28 provides a time delay to ensure that the synthesizer has successfully locked before indicating so on the SYNTH LOCK line. For an unlocked condition, LD pulses low preventing C28 from charging and saturating Q1. +5V is therefore present on the SYNTH LOCK line for the unlocked condition.

2.1j UHF Synthesizer:

Schematic Diagram 30367094/Rev B ★ A1A4A1

10MHz REF. IN (J1)	3.5V P/P square wave
LO OUT (J2)	+15.25dBm min.
SYNTH. LOCK (Pin A of J4)	logic high (locked) logic low (unlocked)

The UHF Synthesizer is a phase-lock loop type and uses one of the 10MHz reference signals from the Reference Oscillator (A4A2) and develops a programmable LO signal for the Mixer in the Downconverter/Preamplifier (A1). The frequency of the LO signal is calculated as the sum of the visual IF carrier and the visual UHF carrier of the specified output channel. The LO signal's frequency is programmed by the setting of switches S1 through S4 which are accessible through the module's cover via access holes. The relationship between the setting of these switches and the resulting LO frequency is provided in Table 2–1 for each UHF channel.

A 10MHz reference signal is brought in from the Reference Oscillator (A4A2) through J1, 10MHz IN. Both sections of U4 perform binary divide-by-5 counting to provide a 400kHz signal to the OSC_{in} input of U1, pin 27. To create U1's internal 50kHz reference signal, U1 performs a binary divide-by-8 operation on the OSC_{in} signal.

Controlling the VCO, G1, is the output of op-amp U3. U3 compares and integrates the $\emptyset_V$ and $\emptyset_R$ phase detector outputs of U1. The output of U3 is filtered to create the dc control voltage for the VCO. The output of G1, RF OUT, is amplified by U5 and available as the Receiver's LO at J2, OUT.

The output of G1 is also amplified by U6 and then fed to a ÷64/÷65 prescaler, U2. After prescaling, the signal is connected to U1 pin 1, F_{in}, from U2 pin 4, OUT, completing the loop. The prescaling factor of U2 is selected by the MOD CONTROL, pin 9, of U1. Switches S1 to S4 set two divide-by-ratios, counters A and N, within U1. When divide-by-A is being performed on the signal at F_{in}, MOD CONTROL is set high, selecting ÷64 in the prescaler, U2. MOD CONTROL goes low for divide-by-N selecting ÷65 in U2.

The A and N counters form a binary number from A0 to N9 with A0 being the LSB and N9 being the MSB. The decimal equivalent of this number, when multiplied by the internal reference frequency 50kHz, gives the synthesizer's output frequency. Hence, for NTSC operation, A0 and A1, pins 21 and 23 on U1, are grounded. For PAL operation, A0 and A1 are made high by cutting the traces from pins 21 and 23 to ground thereby adding the 150kHz to the LO that is characteristic of the PAL system.

When the synthesizer is locked onto a frequency, LD is high. This saturates Q1 and puts a low on SYNTH LOCK. C28 provides a time delay to ensure that the synthesizer has successfully locked before indicating so on the SYNTH LOCK line. For an unlocked condition, LD pulses low

preventing C28 from charging and saturating Q1. +5V is therefore present on the SYNTH LOCK line for the unlocked condition.

2.1k Downconverter/Preamplifier:

Schematic A331-29/Rev B ★ A1A1

Gain with Conversion (J1-J2)	3.0dB
Collector V (Q1)	7.9V
LO Input (Min.) (J3)	+7dBm

The Downconverter preamplifier (A1) consists of a single stage, low noise, broadband amplifier with a double balanced mixer. The VHF or UHF input signal is coupled to Q1 where it is amplified before driving the mixer. The mixer combines the composite VHF or UHF television signal from Q1 with a constant amplitude unmodulated RF signal (LO) from the reference oscillator/synthesizer pair or the crystal oscillator/multiplier pair. Both signals are heterodyned in the mixer where their sum and difference frequencies are developed. Capacitors C10 through C13 along with inductors L4 through L7 comprise a low-pass filter network allowing only the modulated difference frequency (IF) to pass.

2.1l IF SAW Filter/Amplifier:

Schematic B331-21/Rev D ★ A1A2

	Q1	Q2	Q3	J1-J2
Gain				21dB
Collector V	15V	18V	11V	
Collector I	16mA	56mA	16mA	

The IF Surface Acoustic Wave (SAW) Filter/Amplifier is a three-stage amplifier. Transistors Q1/Q2 amplify the IF input signal while their associated feedback networks maintain a flat passband response. The SAW filter provides high selectivity with no need for tuning or alignment. Transistor amplifier Q3 overcomes the loss associated with the SAW filter. Its feedback circuitry is also designed to compensate for nonlinear gain characteristics (i.e., lower gain at the higher frequencies).

2.1m IF AGC Amplifier:

Schematic C331-37/Rev G ★ A1A3

	Q1	Q2	Q3	J1-J2
Gain				10-50dB
Collector V	+20.5Vdc	+25Vdc	+23.4Vdc	
Collector I	4.5mAdc	27mAdc	60mAdc	
Power Output				≈0dBm

The IF AGC Amplifier is a variable gain amplifier with its own automatic gain control and limiter sections. The IF AGC Amplifier is calibrated to provide a constant IF output of approximately 0dBm with a range of −70dBm to −30dBm received signal. The amplifier section consists of three common-emitter RF transistor stages (Q1, Q2, Q3) that produce a combined gain of ≈50dB. Overall gain is adjustable by varying the amount of Q1's emitter bypass via potentiometer R15 (GAIN ADJ). Q2 and Q3 are fixed bias amplifiers separated by a 9dB, 50 ohm-to-50 ohm matching pad (R22, 23, 24). Q3's feedback network, consisting of TILT ADJ potentiometer R31, inductor L2, and capacitor C12, is designed to compensate for the overall frequency characteristics of the module (lower gain at higher frequencies). TILT ADJ potentiometer R31 controls the amplifier's frequency response by varying the amount of Q3's negative feedback.

The automatic gain control section consists of an input AGC circuit (L3, C14, CR8, U1, and surrounding components) and a variable pin diode attenuator (CR1, 2, 4, and surrounding components). The input AGC circuit is centered around operational amplifier U1. A portion of the IF signal is coupled off of Q3 to a tank circuit (C14, L3) tuned to the visual IF carrier frequency (45.75MHz). The tank energy forward biases detector diode CR8 and then becomes filtered by an RC network (C13, R29) which results in a negative dc voltage proportional to the peak value of the visual IF signal. This negative dc voltage is buffered by operational amplifier U1B and then supplied to the Limiter/Output AGC Control (PC1) as the LIMITER REFERENCE OUT voltage. The buffered negative dc voltage is also supplied to operational amplifier U1A where it is inverted and summed with the negative OUTPUT AGC IN reference voltage from PC1, resulting in a positive dc voltage (AGC) proportional to the visual IF signal level. This AGC voltage is used to control the biasing (thus attenuation) of the variable pin diode attenuator and to activate the Automatic-On circuit (PC2).

NOTE: When the front panel OPERATE/ALIGN switch of the Receiver drawer is in the ALIGN position, the IF AGC Amplifier's PRIMARY AGC OUT voltage is replaced by a +5Vdc reference voltage at pin J3-1.

The main function of the limiter circuit is to prevent overdriving the amplifier modules in the translator's Upconverter and Power Amplifier drawers when the input signal to the Receiver returns after periods of reception fading. For example, following a temporary reduction (fading, etc.) in the received signal, the AGC voltage decreases which reduces the attenuation provided by the IF AGC Amplifier's variable pin diode attenuator. However, once the received signal regains its strength, the variable pin diode attenuator cannot attenuate this signal fast enough. The limiter circuit is used to overcome this characteristic of the variable pin diode attenuator. Notice that with an increase in the received signal, the AGC voltage increases while the limiter reference voltage decreases. The variable pin diode attenuator will eventually respond to the increase in the AGC voltage by increasing its attenuation. The limiter control circuit on PC1 quickly responds to a 3dB or greater instantaneous increase in the IF AGC Amplifier's LIMITER REFERENCE OUT voltage J3-3 by pulling the LIMITER ENABLE IN J3-4 low, turning off transistor Q4 of the IF AGC Amplifier.

With Q4 turned off, the dc forward bias is removed from pin diode CR9, thus reducing momentarily the IF output of the IF AGC Amplifier by approximately 20dB. The momentary attenuation in the IF output by the limiter circuit allows sufficient time for the variable pin diode attenuator to adjust itself to the change in the AGC voltage. Overdriving can also occur when the translator is first turned on. To compensate, Q6 is on, turning on Q5. This shuts off Q4, increasing the attenuation of CR9, as above, until C32 charges. Q6 and Q5 then turn off, allowing LIMITER ENABLE IN, which is normally high, to turn on Q4. This forward biases CR9 by providing a dc path to ground through it for the +15V from pin J3-5.

2.1n Automatic-On:

Schematic B331-44/Rev C ⋆ A1PC2

The Automatic-On circuit uses differential amplifier U1A to compare the AGC voltage, developed by the IF AGC Amplifier, to a preset reference voltage set by THRESHOLD ADJUST potentiometer R4. An input signal above the minimum acceptable Receiver input level of –60dBm will produce an AGC voltage above the Auto-On Threshold potential. As the AGC voltage (pin 3 of U1A) exceeds the Auto-On Threshold reference voltage (pin 2 of U1A), differential amplifier U1A saturates in the positive mode charging capacitor C1. Once C1 charges above the reference potential at pin 6 of U18, differential amplifier U1B will also saturate in the positive mode turning on transistor Q1. With Q1 forward biased, a ground is provided for relay K1 which energizes the device. The closed contacts of K1 place +5Vdc on the INTLK (VIDEO SENSE) line going to the Exciter's Control Board (A2PC1). An Auto-On delay network consisting of R8, R9, and C1 slows down the turn-on and turn-off activation time. This delay of approximately 30 seconds prevents on/off cycling from occurring during periods of weak reception lasting for less than 30 seconds.

2.1o Limiter/Output AGC Control:

Schematic B331-34/Rev C ⋆ A1PC1

The Limiter/Output AGC Control board monitors and controls the IF AGC Amplifier (A3) and controls the CARRIER PRESENT LED (DS1) on the Receiver front panel.

The AGC negative reference voltage is placed on pin 3, OUTPUT AGC, by inverting op-amp U1B. Potentiometer R9, AGC REF, sets this voltage. Keep the PRE AGC REF ADJ potentiometer fully clockwise because it and the POWER REFERENCE portion of the AGC circuit, from pin 1 to pin 2, are not used in this application.

LIMITER REFERENCE IN is brought in from A3 on pin 12 and is compared to an 11.8V reference by U2B. When a carrier greater than –60dB is received, the output of U2B will saturate by approximately +15V turning on Q3. This provides a path to ground through current limiting resistor R23 on pin 10 for the CARRIER PRESENT LED (DS1) on the Receiver drawer front panel, illuminating it green. If the received carrier level drops below –60dBm, U2B saturates to –15V turning off Q3. The LIMITER ADJUST potentiometer, R13, voltage divides the LIMITER REFERENCE INPUT and passes it through unity gain follower U2A and unity gain follower U2C. U2D takes the difference between the 8.7V reference, from CR2, and the output U2C. For the nominal level of the carrier being received, the output of U2C is less than 8.7V and U2D puts approximately +15V on LIMITER ENABLE OUT, pin 9. The LIMITER ADJ is set so that, if

LIMITER REFERENCE IN increases by 3dB, the output of U2C will be greater than 8.7V and U2D will saturate to approximately −15V pulling down LIMITER ENABLE OUT.

2.1p Aural Notch Filter:

Schematic Diagram 10383097/Rev 51 ★ A1FL2

Insertion Loss (J1-J2) 0.4dB Max.

The Aural Notch Filter provides a means of attenuating the aural carrier 3dB which can be useful for reducing the effects of in-band and out-of-band intermodulation. Variable capacitor C3 tunes the notch to the aural IF frequency in an NTSC system, 41.25MHz. This capacitor is preset by the EMCEE Test Department. R1 sets the amount of attenuation; up to 3.5dB of attenuation can be attained. The filter is a very high Q type and does not have an appreciable effect on the visual carrier or color subcarrier.

2.1q Multi-Output Power Supply:

Interconnection Diagram B326-18/Rev C ★ A1PS1

Voltage	Rated Current
+25Vdc	1Adc
±15Vdc	1Adc
±5Vdc	1Adc

As shown on the Interconnection Diagram, the Multioutput Power Supply consists of surge suppressor E1, transformer T1, and printed circuit boards PC1 and PC2. PC1 is the +25V Power Supply, and PC2 is the ±15V/±5V Power Supply. Surge suppressor E1 provides voltage-transient protection for the step-down transformer T1 and the +25V Power Supply.

+25V Power Supply:

Schematic B326-15/Rev C ★ A1PS1PC1

The secondary voltage of step-down transformer A1PS1T1 is applied to bridge rectifier CR1. After filtering, the rectified voltage (≈36V) is regulated by U1 to the +25Vdc level. The output voltage of U1 is fixed by resistors R1, R2, and R3. +25Vdc is supplied to various modules in the Receiver drawer.

±15V/±5V Power Supply:

Schematic B326-12/Rev D ★ A1PS1PC2

120Vac is placed across the primary of step-down transformer T1. Surge suppressor E1 provides voltage-transient protection for this supply. Transformer T1 supplies a secondary voltage to bridge rectifier CR1. The output of CR1 is divided, with the negative voltage applied to –15Vdc regulator U2 and the positive potential fed to +15Vdc regulator U1. Voltage regulators U3 and U4 tap off of the 15V lines to provide +5Vdc and –5Vdc, respectively. The capacitors provide filtering for the different regulators. ±15Vdc is supplied to the IF AGC Amplifier (A3), the Limiter/Output AGC circuit (PC1), and the Automatic-On circuit (PC2). +5Vdc is supplied to the IF AGC Amplifier (A3).

2.1r Digital Code ID Unit: (OPTIONAL)

Schematic 20258029/Rev A ★ A1PC3

According to FCC Rules and Regulations, Section 74.783, each television broadcast transmitter in the United States of over 1 watt peak visual power must transmit its call sign in International Morse Code every 60 minutes or arrange for the primary station to visually or aurally identify the transmitter and its location. The Digital Code Identification Unit is available for the customer who wishes to identify a transmitter station with Morse Code. The ID unit is a sixteen word by eight bit sequencer which generates a series of pulses used to shift the frequency of the transmitted carriers by frequency shift keying (FSK) the transmitter's Upconverter Oscillator.

The Digital Code ID Unit is composed of four integrated circuits: a Dual Timer (U4), a Dual 4 Bit Counter (U3), a Programmable Read Only Memory (U2) and an 8 to 1 Line Multiplex (U1). The Dual Timer or master clock contains two sections which control the operation of the ID unit by dictating when and at what rate pulses will be fed to the Upconverter oscillator. The first section of the timer is a gated astable oscillator or bit clock which produces square-wave pulses at a rate of approximately 20Hz. The bit rate is controlled by U4 resistors R11, R12 and capacitor C2. The second section of U4 is a 20 minute timer controlled by resistors R9, R10 and capacitor C1. When C1 charges to 63% of its capacity (after 20 minutes), pin 9 of U4 will go low, reverse biasing transistor Q3 which presents a high (4Vdc) at pin 4. This high gates on the bit generator which feeds the 20Hz pulses to pin 1 of the Dual 4 Bit Counter (U3).

As each clock pulse reaches pin 1 of U3, the 4 Bit Counter "counts" the number of pulses entering the chip and displays that count in binary code at its own pins 3, 4 and 5. For example, as the first pulse is fed to U3, pin 3 goes high representing the decimal number 1 in binary code (001). With the second clock pulse, U3 pin 4 goes high and pin 3 goes low representing the binary number 2 (010). This counting process will continue up to the number 7 (111) and, as the eighth pulse is fed to the counter, pins 3, 4, and 5 will all go low (000) to begin the sequence over again. During this time integrated circuit U2, the Programmable Read Only Memory (PROM), has a series of high and low voltages present at its pins 1 through 9 (excluding pin 8 which is ground). These voltages are bits which make up the first word (Morse code letters or numbers) of the transmitter's call sign. (The transmitter's call sign is programmed into the PROM by the EMCEE test department.) In order for this information to be delivered to the Upconverter oscillator, it must be converted from parallel form to serial form by the 8 Line to 1 Line Multiplexer (U1). The binary numbers developed by the Dual 4 Bit Counter are fed to pins 9, 10, and 11 of the 8 to 1 Line Multiplexer. Each binary number (or voltage fluctuation) presented to U1 signals the multiplexer circuit to individually read (take) the parallel bits presented by the PROM and deliver them serially to the oscillator via transistor Q4. Therefore, as the Dual 4 Bit Counter (U3) feeds the binary numbers 1 (001) to pins

9, 10 and 11 of the Line Multiplexer (bit address), the Multiplexer reads the bit at pin 1 of the PROM (U2) and delivers it to the base of transistor Q4. With each subsequent binary number (010, 011, 100, 101, 110, 111, 000) provided by the Dual Counter, the Line Multiplexer will read each individual PROM bit present at U2 pins 2 through 9 (exclude pin 8) until the Dual Counter reaches 111. The next pulse then resets the count to 0 (000). The transition from high to low (1 to 0) at pin 5 of the counter is seen by pin 13, causing pin 11 of U3 to go high. This binary number 1 (0001) seen by pins 10, 11, 12 and 13 (word address) of U2 causes the PROM to present the second set (word) of eight bits to the Line Multiplexer. The Dual Counter (U3 – pins 3, 4, 5) presents another binary eight count to the Line Multiplexer (U1 – pins 9, 10, 11) which individually reads the eight new PROM bits (U2 – pins 1 through 9) and delivers them to transistor Q4. At the end of the second eight count, pin 13 of U3 again sees a high to low transition which causes pin 10 of U3 to go high while pin 11 goes low (binary number 2 = 0010). With U2 pins 10 through 13 receiving a binary number 2, a third word is presented to the Line Multiplexer by the PROM. This entire process occurs so that the PROM delivers 16, eight bit words to the Upconverter oscillator via the Line Multiplexer. After word 16, pins 8 through 10 of U3, which were all high (binary number 16 = 1111), drop to zero. The negative going transition at pin 8 of U3 is coupled to transistor Q1 via C3. This action forward biases transistor Q2 which discharges capacitor C1. As the voltage at pin 12 of the Dual Timer drops, pin 9 goes high causing pin 4 of U4 to go low. The Dual Timer's bit clock is gated off, disabling the Digital Code Identification Unit for 20 minutes until capacitor C1 recharges.

2.2 Exciter/Upconverter Drawer:

Interconnection Diagram 40383113/Rev 55 ★ A2 TTU20F

Composite IF IN (J1)	≈–8dBm peak visual
RF OUT (J2)	+43dBm peak visual +33dBm average aural
LO SAMPLE (J3)	+9dBm ± 2dBm

The Exciter/Upconverter drawer converts the composite IF signal from the Receiver to the desired UHF channel, then amplifies the RF signal to the desired output level. This drawer is used to drive the two Dual 300W Final Amplifier Drawers (A3, A4). The Linearizer provides precorrection to the composite IF signal. Upconversion is performed by the IF Upconverter (A1) along with the UHF Synthesizer (A4). The UHF Synthesizer provides a programmable LO to the IF Upconverter module where the LO and IF signal from the Receiver are mixed to create the desired UHF frequency. The IF Upconverter also provides AGC and precorrector functions. The UHF signal from the Upconverter module is passed through a UHF Bandpass Filter (FL1) to remove the unwanted products from the conversion process while passing the desired signal with a minimal loss. The RF is then amplified approximately 50dB by a 2W Driver Amplifier (A2) and then amplified another 12dB by a 20W UHF Amplifier (A3). The output signal is passed through the Metering Coupler (DC1). The Metering Coupler provides samples for the Metering Detector (A5) while passing the signal to the output of the drawer.

Metering and control functions are provided by the Metering Detector, the Metering Switch (PC2), and the Control Board (PC1). The Control Board also has several status and diagnostic LED indicators. Power is supplied to the drawer by two power supplies, a ±15V/+5V linear supply (PS2) and a +28V switching supply (PS1).

2.2a Linearizer:

Schematic Diagram 30367078/Rev 60 ★ A2A6

Gain with S1 OFF (J1-J2)	3dB min./6dB max.
Gain with S1 ON (J1-J2)	6dB min./12dB max.
Emitter of Q1/Q2	+4.8Vdc @ 13mAdc/+13Vdc @ 30mAdc
Emitter of Q3/Q4	+3.3Vdc @ 11mAdc/+15Vdc @ 45mAdc
Emitter of Q5	+8.7Vdc @ 22mAdc

The Linearizer is a five-stage circuit which compensates for linearity distortions generated by the translator's Class AB power amplifiers. Transistors Q1 through Q5 are all amplifier stages with the Q1/Q2 combination providing approximately 20dB of gain. 8dB of gain is provided by transistors Q3/Q4. Q2, Q4, and Q5 are used as low impedance emitter followers. Variable gain expansion networks which furnish linearity correction are centered around diodes CR1 through CR8, slope potentiometers SL1 through SL4 (i.e., R10, R11, R21, R22), unity gain inverting amplifiers U1 and U2, threshold potentiometers TH1 through TH4 (i.e., R37, R38, R39, R40), and switch S1. When S1 is in the OFF position, each diode pair is continuously reverse biased throughout the positive and negative cycles of the visual IF carrier. Due to the high reverse resistance provided by CR1 through CR8, each network essentially represents a resistive L-pad with the composite IF signal attenuated by a fixed amount. As a result, no linearity correction is provided. However, when S1 is in the ON position and the Linearizer is properly adjusted, the four diode pairs form a nonlinear circuit where each diode pair is biased to turn on at different points of the positive and negative cycles of the visual IF carrier envelope. Each diode pair is initially reverse biased by equal but opposite polarity dc voltages established by U1 and U2. L1 through L8, shunted by R29 through R36, isolate the visual IF carrier from the diode biasing circuitry. When the positive and negative peaks of the visual IF carrier are sufficient to forward bias a diode pair, the diode pair turns on placing the resistance of its respective slope potentiometer either in parallel or in shunt to ground with its respective series arm resistance. As a result of switching additional resistance in parallel or shunt with the series arm of the L-pad, the attenuation of the visual IF carrier is reduced. Threshold potentiometers TH1 through TH4 determine the turn-on point of each diode pair while slope potentiometers SL1 through SL4 vary the amount of gain expansion achieved during the turn-on period of each diode pair. Threshold controls TH1, TH2, and TH3 are used to adjust the differential gain of the white to black region while TH4 adjusts the sync amplitude. When properly adjusted, the Linearizer provides sync amplitude, differential gain, and intermodulation correction to the RF output signal.

2.2b IF/Upconverter:

Schematic Diagram 30383013/Rev 55 ★ A2A1

IF INPUT (J1)	−8dBm peak visual
RF OUTPUT (J2)	−13.5dBm minimum
LO SAMPLE (J3)	+9dBm ± 2dB
LO INPUT (J4)	+13dBm minimum

The IF/Upconverter performs three tasks in this translator. It provides signal precorrection, AGC level control, and it upconverts the IF signal to the desired UHF channel. This module also provides a sample of the LO signal to the Exciter’s front panel.

The IF input at J1 is attenuated by AT1, an adjustable attenuator which can be tuned to compensate for different input levels. A monolithic amplifier (U1) provides approximately 12dB of gain to the signal passed through the attenuator. U1 is biased by R1 with L1 providing impedance matching and isolation. C2 is an RF bypass capacitor, while C1 and C3 are coupling capacitors. T1 steps up the signal's voltage to drive the precorrector circuit made up of CR1, C4 to C6, C8 to C12, R2 through R10, L4, L5, U2, and S1. This circuit compensates for linearity distortions generated by the wideband power amplifiers or created by the Receiver. When switch S1 is in the off position (open), this circuit reduces to a simple attenuator formed by R2 and R3; therefore, no precorrection is provided. When S1 is on, the precorrector becomes a nonlinear circuit that provides less attenuation for the positive and negative peaks of the IF signal, thereby stretching the waveform. CR1 is biased by U2 A and B, with each op amp biasing one half of CR1. The amount of bias provided by U2 is determined by R7 through R10. R9 allows the bias level to be adjusted. This adjustment determines at which point on the waveform precorrection begins. R5, R6, C8 through C11, L4, and L5 provide isolation between CR1 and U2. C4 to C6 are dc blocking capacitors. The precorrector operates by placing R4 in parallel with R2 when the IF signal is positive or negative enough to forward bias half of CR1. Adjusting R4 determines the amount of precorrection provided. At the output of the precorrector, a second monolithic amplifier provides +12dB of gain to the IF signal. C7 and C14 are coupling capacitors while C13 acts as an RF bypass. L2 is an RF choke and R11 provides the correct bias voltage for U3.

The next circuit in the Upconverter is the AGC circuit. Three PIN diodes, CR2, CR3, and CR4, form a voltage controlled attenuator along with R14 and C17. C14, C16, and C18 serve as dc blocking capacitors. Bias is provided to this attenuator by R12, VR1, and R13, as well as R15, L3, and the three operational amplifiers U4(A), U5(A), and U5(B). C15, C32, and C19 are bypasses. The control voltage for the AGC is generated by U5(B). A dc voltage proportional to the output power is connected to pin 6 of U5 by R26. A reference voltage from the Control Board's Power Adjust circuit is supplied to pin 5 of U5 by R22. U5(B) compares these two voltages and provides a control voltage at pin 7 of U5. R27 sets the gain of U5(B) to unity. U5(A) is an integrator that provides a smooth transition for the changing control voltage. Input to U5(A) is provided by R20, with C22 as the integration capacitor. A reference voltage is provided to pin 3 of U5 by R21 and CR5 through CR7. The output of U5(A) is passed through an attenuator formed by R18 and R19 before driving the unity gain buffer amplifier formed by U4(A) R16 and R17. When the OPERATE/ ALIGN switch is in the ALIGN position, pin 3 of U4A is grounded. This defeats the AGC circuit and allows minimum attenuation of the IF signal. Q1, R35-R37 and C33 make up a soft start circuit that retards the spike in output power that normally would occur when the translator is turned ON and the OPERATE/STANDBY switch is placed in the OPERATE position. The circuit places approximately +13Vdc on pin 3 of U4A, putting the AGC circuit into a condition of maximum attenuation. As C33 charges, this imposed voltage on pin 3 decreases giving the AGC circuit time to stabilize before Q1 turns off and the output of U5A takes control of the AGC. Whenever +28V switched is removed from the drawer (OFF or STANDBY), CR8 forward biases and C33 discharges through it and R38 to ground. The output of U4(A) is the AGC control voltage.

The IF output of the AGC circuit connects to mixer MX1 where it is combined with the LO signal from the synthesizer to produce the desired UHF channel frequency at the RF output port, J2. The LO is brought to the mixer by R29 and R30 (which provide isolation) and U7, an amplifier that provides about 12dB of gain to the signal. U7 is biased by R28. A sample of the LO is also supplied to connector J3 via U6, the input of which is attenuated by R31 to R33. U6, biased by R34, provides 12dB of gain. C24 to C27 are coupling capacitors, while all remaining capacitors are RF bypasses.

2.2c UHF Synthesizer:

Schematic Diagram 30367094/Rev B ★ A2A4A1

10MHz REF. IN (J1)	3.5V P/P square wave
LO OUT (J2)	+15.25dBm min.
SYNTH. LOCK (Pin A of J4)	logic high (locked)
	logic low (unlocked)

The UHF Synthesizer is a phase-lock loop type and uses one of the 10MHz reference signals from the Reference Oscillator (A4A2) and develops a programmable LO signal for the Mixer (MX1) in the IF Upconverter (A1). The frequency of the LO signal is calculated as the sum of the visual IF carrier and the visual UHF carrier of the specified output channel. The LO signal's frequency is programmed by the setting of switches S1 through S4 which are accessible through the module's cover via access holes. The relationship between the setting of these switches and the resulting LO frequency is provided in Table 2–1 for each UHF channel.

A 10MHz reference signal is brought in from the Reference Oscillator (A4A2) through J1, 10MHz IN. Both sections of U4 perform binary divide-by-5 counting to provide a 400kHz signal to the OSC_{in} input of U1, pin 27. To create U1's internal 50kHz reference signal, U1 performs a binary divide-by-8 operation on the OSC_{in} signal.

Controlling the VCO, G1, is the output of op-amp U3. U3 compares and integrates the $\emptyset_V$ and $\emptyset_R$ phase detector outputs of U1. The output of U3 is filtered to create the dc control voltage for the VCO. The output of G1, RF OUT, is amplified by U5 and available as the Exciter/Upconverter's LO at J2, OUT.

The output of G1 is also amplified by U6 and then fed to a ÷64/÷65 prescaler, U2. After prescaling, the signal is connected to U1 pin 1, F_{in}, from U2 pin 4, OUT, completing the loop. The prescaling factor of U2 is selected by the MOD CONTROL, pin 9, of U1. Switches S1 to S4 set two divide-by-ratios, counters A and N, within U1. When divide-by-A is being performed on the signal at F_{in}, MOD CONTROL is set high, selecting ÷64 in the prescaler, U2. MOD CONTROL goes low for divide-by-N selecting ÷65 in U2.

The A and N counters form a binary number from A0 to N9 with A0 being the LSB and N9 being the MSB. The decimal equivalent of this number, when multiplied by the internal reference frequency 50kHz, gives the synthesizer's output frequency. Hence, for NTSC operation, A0 and A1, pins 21 and 23 on U1, are grounded. For PAL operation, A0 and A1 are made high by cutting the traces from pins 21 and 23 to ground thereby adding the 150kHz to the LO that is characteristic of the PAL system.

When the synthesizer is locked onto a frequency, LD is high. This saturates Q1 and puts a low on SYNTH LOCK. C28 provides a time delay to ensure that the synthesizer has successfully locked before indicating so on the SYNTH LOCK line. For an unlocked condition, LD pulses low preventing C28 from charging and saturating Q1. +5V is therefore present on the SYNTH LOCK line for the unlocked condition.

2.2d Reference Oscillator:

Schematic Diagram 10368037/Rev B ★ A2A4A2

10MHz REF. OUT (J1, J2)	3.5V P/P square wave

The Reference Oscillator provides a 10MHz reference signal for the UHF Synthesizer (A4A1). This module is centered around a 10MHz temperature-compensated crystal oscillator (G1). The output from G1 is applied to two exclusive-OR gates used as inverting buffers. The output signal from each gate is a 10MHz low-level square wave with a frequency stability of 0.3 parts per million (PPM).

2.2e UHF Bandpass Filter:

Schematic Diagram 10331209/Rev 52 ★ A2FL1

1dB Bandwidth (J1-J2)	7MHz
Insertion Loss (J1-J2)	3dB Max.

The UHF Bandpass Filter (FL1) consists of three tunable resonant cavities, with the three tuning capacitors of the filter adjusted to provide the frequency response, shown in Figure 3–5, selecting the appropriate UHF channel. FL1 is tuned to select the desired UHF mixer products from the lower sideband or difference signal found at the RF OUTput (J2) of the IF/Upconverter (A1) module.

2.2f 2W UHF Amplifier:

Schematic Diagram 30367002/Rev A ★ A2A2

Gain (J1-J2)	50dB
Power Output	≈+33dBm peak visual
	≈+23dBm average aural
Flatness (J1-J2)	±1dB from 470-860MHz
U1, PIN 3	+3.9Vdc @ 29mA
U2, PIN 3	+5.3Vdc @ 58mA
U3, PIN 4	+20Vdc @ 100mA
Q1, Collector	+25Vdc @ 600mA

The 2W UHF Amplifier (A2) provides amplification to the selected UHF channel. The Amplifier is a four-stage, class A, microstrip design. The first three stages are centered around broadband monolithic amplifiers U1 through U3 which provide a combined gain of 40dB. The fourth stage is an RF transistor amplifier Q1 which provides a gain of approximately 10dB. Q1 is biased by a dc current regulator consisting of Q2, R4, R5, R6, R7, and R9. This circuit continuously maintains the collector voltage and current of Q1 over a wide variation of load and temperature. The required collector voltage and current of Q1 is established by potentiometer R5. Input matching for Q1 is provided by C9, C10, C11, C12, and C24 while output matching is accomplished by C13, C14 and C30. Capacitor C10 is tuned for maximum gain with a flat frequency response from 470 to 860MHz. C1, C3, C5, C8, and C14 provide signal coupling while all other capacitors are used for

bypassing. Coils L1 through L4 function as RF chokes while R1 through R3 are used as biasing resistors.

2.2g 20W UHF Amplifier:

Schematic Diagram 40383053/Rev 52 ★ A2A3

Gain (J1-J2)	12dB min.
Power Output	≈+44.5dBm peak visual/ ≈+34.5dBm average aural
Flatness (J1-J2)	±1dB from 470-860MHz
Collector of Q1 & Q2	+26.8Vdc @ 1.2Adc (each side)

The 20W UHF Amplifier is a class A, broadband, microstrip design consisting of two RF transistor stages centered around push-pull devices Q1 and Q2. These two stages are connected in parallel via splitter CP1 and combiner CP2. Q1 and Q2 are biased by separate dc current regulators which continuously maintain each collector voltage and current, over a wide variation of temperature and signal level. Each current regulator is made up of PNP transistors Q3 and Q4 working with potentiometers R4 and R11 to provide the required collector voltage and current for each side of Q1 and Q2. CP1 and CP2 are Wireline quadrature 3dB,90° hybrid couplers which split and combine power equally with resistors R5/R12 used to terminate the isolated port of each. The function of R5/R12 is to absorb any imbalance that develops in either hybrid as well as to establish a 50 ohm input/output impedance. Baluns Z1/Z3 transform the unbalanced signal into a balanced input to drive the push-pull transistor pair of Q1/Q2. Baluns Z2/Z4 act in the opposite manner to transform the balanced output from Q1/Q2 into an unbalanced output. Input matching for transistors Q1/Q2 is provided by capacitors C1-3, C32, C65, C76/C18-C21, C66, C77, C80 while output matching is accomplished by capacitors C43, C68-C70, C72, C81/C48, C53-C55, C74, C82. Variable capacitors C79, C32, C80, and C18 are tuned for maximum gain with a flat frequency response. Coils L1 through L8 function as RF chokes while capacitors C1, C2, C20, C21, C68, C69, C54 and C55 are used for signal coupling. All other capacitors are used for bypassing.

Fault Circuit:

The Fault Circuit board (PC3) detects the presence of either an open or shorted RF device in the 20W UHF Amplifier. Under normal operation, the collector voltage on both sides of each push-pull transistor in the 20W UHF Amplifier is typically +26.8Vdc. Under this condition, Q1 through Q3 of the fault circuit are turned on, the diodes identified by pins 1 and 3 in CR2 and CR3 are turned on, the diodes identified by pins 2 and 3 are turned off, and the diodes identified by pins 1/14 and 7/8 of CR1 are turned on while those identified by pins 2/13 and 3/12 are turned off. Hence, for normal operation of each push-pull RF transistor, the FAULT line (pin C of connector J3) is set at a logic low (approximately 0Vdc) by the pull-down resistor (R10) or the Control Board (A2PC1). However, if either side of one of the push-pull transistors opens, its collector voltage rises from +26.8Vdc to about +27.4Vdc. This action results in turning off Q3 and Q2 as well as the diode identified by pins 7 and 8 of CR1. With these components turned off, the diode identified by pins 3 and 12 of CR1 turns on applying a logic high (approximately +4.7Vdc) to the FAULT line. On the other hand, if either side of one of the push-pull transistors shorts, the shorted transistor collector falls from +26.8Vdc to about +0.2Vdc causing the diode identified by pins 2 and 3 of either CR2 or CR3 to turn on. This action results in turning off Q1 and the diode identified by pins 1 and 14 of CR1. With these components turned off, the diode identified by pins 2 and 13 of CR1 turns on

applying a logic high to the FAULT line. The information on the FAULT line is processed by the fault monitoring/display section of the Control board (A2PC1).

2.2h Metering Coupler:

Schematic Diagram 10199178/Rev 52 ★ A2DC1

Insertion Loss (J1-J2)	<0.5dB
FWD Coupling (J1-J3)	30dB
REFL Coupling (J1-J4)	30dB

The Metering Coupler is a four-port device designed to provide forward and reflected RF samples to the Metering Detector (A5) with minimal loss to the output signal. The RF signal is applied to the coupler's input port (J1) and exits the coupler with a maximum of 0.5dB of loss at J2. A –30dB sample of the signal's forward power is provided at J3, and a –30dB sample of the reflected power is provided at J4. These two signals are connected to the Metering Detector (A5) which then provides DC signals proportional to the output signal to the Control Board (PC1), the AGC circuits, and the Metering Switch (PC2).

2.2i Metering Detector:

Schematic Diagram 30368024/Rev P ★ A2A5

The Metering Detector contains three circuits for monitoring signal levels. Each of these circuits can take an RF signal at its input and provide a DC voltage at its output proportional to the input signal's strength. Only two of the detector circuits are used in this application. A sample of the output signal is supplied to the VISual port of the detector, and a sample of the reflected power is provided at the REFLected input of the detector. These signals are provided by the Metering Coupler (DC1). The front end or detector portion of each circuit is basically the same. Diodes CR2 and CR4, together with their surrounding components, convert the sampled on-channel RF signals to positive dc voltages proportional to the detected RF power. Detection of the sampled visual output carrier is accomplished by CR2 in conjunction with R4 and C2 which form a time constant of 1 second. R4 is the dc load while C1 and C11 form the RF ground of the visual power detector. Detection of the sampled reflected signal is the same except for a faster time constant. R22/C6 forms a time constant of 1 millisecond. The positive dc voltages from the visual and reflected power detectors are processed by buffer amplifiers U1 and U2 which provide voltage gains of 1V/V and 2V/V, respectively. These buffer amplifiers also provide isolation between the % POWER meter and the detectors. The settings of potentiometers R9 and R27 determine the voltage level applied to the % POWER meter when the meter switch (PC2) is in its FWD or REFL positions, respectively. The aural detector circuit is not used in this application.

A dc voltage proportional to the Exciter's output power is available at pin 5 of connector J4, designated VISUAL POWER REFERENCE.

2.2j Control Board:

Schematic Diagram 40383016/Rev 62 ★ A2PC1

The Exciter's Control Board (PC1) is mounted to the inside of the Exciter/Upconverter's front panel. It provides various monitoring and control functions for the Exciter while displaying the results on front panel indicators and the metering display. The circuitry can be divided into three sections:

(1) Interlock Monitoring/Display
(2) Amplifier Fault Monitoring/Display
(3) Miscellaneous Control/Display

The Interlock section monitors the VIDEO SENSE from the modulator (optional), SYNTH LOCK, the 20W amplifier TEMP SENSOR, VSWR OVLD, the +28V FINAL PS and OPERATE/STANDBY switch. When these signals are of the appropriate level with the OPERATE/STANDBY switch set to OPERATE and the POWER circuit breaker ON, the contactor (K1) closes placing the translator on line. The FINAL BIAS, ON and SYNTH LOCK indicators are now illuminated green and the TEMP EXCITER and VSWR OVLD indicators are unlit when the interlock is closed.

With baseband video present, the optional VIDEO SENSE line (J1-3) from the modulator is high. The SYNTH LOCK line at J1-8 is low when the synthesizer is locked on frequency. This forces the outputs of U1D and U1F high. U1F saturates Q9, illuminating the SYNTH LOCK LED (DS5) green. If video is lost, the VIDEO SENSE line will go low. An unlocked synthesizer puts a high on the SYNTH LOCK line causing the outputs of U1D and U1F to go low and Q9 to cut off, extinguishing DS5. Should either of these situations occur, the output of U3A, which is normally high, will be driven low. Note that the VIDEO SENSE line can be left unconnected and R30 will hold it high so that the translator will operate.

The 20 WATT TEMP SENSOR line (J1-7) connects to ground through thermostat S1 mounted to the heat sink of the 20 Watt UHF Amplifier, A3. When the temperature of the thermostat is below 150°F, the thermostat is closed. This pulls the 20 WATT TEMP SENSOR line low, driving inverter U1H high and buffer U2H low. Temperatures in excess of 150°F cause the thermostat to open and the 20 WATT TEMP SENSOR line goes high. This high drives U1H low and U2H high shutting transistor Q8 off and extinguishing TEMP EXCITER LED DS4. DS4 is illuminated yellow when U2H is forced high causing Q8 to conduct.

The FINAL AMPL TEMP SENSOR line (J1-24) in the Exciter monitors the momentary (10 second) VSWR OVLD signal from the main Control Board (A5PC1)mounted behind the Front Panel (A5) at the top of the translator cabinet. This line is normally low, driving U1B high and reverse biasing CR1. When a VSWR OVLD occurs at the output of the translator, a high is present at J1-24 driving U1B low. A low at the output of U1H or U1B forward biases CR1 or CR4, respectively, and places a low on pin 5 of U3B which is normally high.

The final VSWR OVLD signal from the main Control Board (A5PC1) is applied to pin J1-5. Under normal operation with the forward and reflected powers correctly set, this line is low. This turns Q1 off and Q2 on. U4A is set to have a high at $\overline{Q}$/pin 6, and a low at Q/pin 5. The low at pin 5 turns off Q5 and the red VSWR OVLD indicator (DS7). If the reflected power exceeds the reference level set in the translator's output Metering Detector (A5A7), the VSWR OVLD line goes high, turning on Q1 and providing a discharge path for C11. C11, R22, and CR2 provide a quick on/ slow off circuit so that a transient does not trigger the VSWR OVLD circuit. When C11 has discharged sufficiently, Q2 will shut off. This causes the CLK input, pin 3, of U4A to go from low to high triggering the flip-flop action of U4A. Q is now high turning on Q5 and the red section of DS7. $\overline{Q}$ is now low and places a low at pin 4 of U3B. The VSWR OVLD line returns to

approximately –0.6Vdc when this occurs. The Exciter's momentary VSWR RESET switch (S2) resets U4A by grounding the CLR input/pin 1 when depressed. The REMOTE VSWR OVLD RESET (J1-21) allows the VSWR overload circuit to be reset from a remote location through the REMOTE MONITOR jack J4.

The output of U3B is normally high; however, if a low appears at either input of U3B, its output will be driven low. The output of U3B connects to one input of U3D while the output of U3A connects to the other input through the OPERATE/STANDBY switch. Under normal operating conditions, the output of U3D is also high. If U3A goes low while S1 is in the OPERATE (closed) or STANDBY (open) position or if U3B goes low, the output of U3D will be pulled low. When U3D is high, Q6 and the green section of the FINAL BIAS indicator (DS6) are turned on, Q3 is off and the FINAL PS INHIBIT line at J1-4 is floating. If U3D goes low, Q6 and DS6 turn off while Q3 turns on, grounding the FINAL PS INHIBIT line which shuts down the power supplies of each 300 Watt UHF Power Amplifier placing the translator in standby.

The output of U3C is normally high with U3D connected to one input of U3C. RF DRIVE CONTROL J1-9 will also be high provided that all the +28V Power Supplies (A3PS1, A3PS2, A4PS1, A4PS2) contained in the Dual 300W UHF Power Amplifier drawers are functioning properly. If this is not the case or if U3D goes low, U3C will trip low turning off transistors Q7, Q4 and the ON indicator (DS8). With Q4 off, ground is removed from the CONTACTOR CONTROL line (J1-11) and it is left floating. This deenergizes the contactor and removes +28V from the IF Upconverter (A1), the 2 Watt UHF Amplifier (A2) and the 20 Watt UHF Amplifier (A3). During normal operation U3C is high, turning on transistors Q7, Q4 and the green portion of LED DS8. The CONTACTOR CONTROL line is pulled to ground through Q4. (Note that J1-9 cannot be left unconnected or U3C will never go high.) Once the output of U3C goes low, it will remain in that state until the condition which caused the low at either of U3C's inputs is corrected.

The Amplifier Fault Monitoring/Display section monitors the 20W AMPL FAULT line (J1-13) which is low when the 20 WATT UHF AMPLIFIER module (A3) is functioning properly. A fault is represented by a high on the line. For normal operation of the 20 WATT UHF AMPLIFIER, U1E is high illuminating the green section of the DRIVER AMP indicator (DS1). At the same time, U2E is low bypassing the red section of DS1. For a fault, the opposite occurs. U1E goes low extinguishing the green section of DS1 and U2E goes high illuminating the red section of DS1.

There are three Miscellaneous Control/Display circuits. The POWER ADJUST potentiometer, which is accessible through the front panel of the Exciter, sends a DC voltage to the AGC circuit in the IF Upconverter (A1) to control the final output power of the translator. The OPERATE/ ALIGN switch engages or defeats the AGC circuit. In the ALIGN position, J1-23 is grounded and the OPERATE indicator (DS9) is unlit. In the OPERATE position DS9 is illuminated green and the OP/ALIGN line is an open circuit on the Control Board. The voltage on the METER line (J1-15) is selected by the METERING SWITCH (PC2) mounted below the 30-segment LED bar graph display on the front panel. Forward power (FWD), reflected power (REFL), +28V or +5V meter indications can be chosen. The voltage level is decoded by three voltage level-indicator drivers (U5-U7) and the appropriate number of LEDs are lit on the bar graph display (DS10-DS12).

2.2k Power Supplies:

Schematic Diagrams N/A ★ A2PS1, A2PS2

±15V/+5V Power Supply Outputs	±15Vdc @ 400mA maximum +5Vdc @ 2A maximum
+28V Power Supply Output	+28Vdc @ 9A maximum

Two DC power supplies are used in the Exciter/Upconverter drawer to provide power to the modules. A +28V supply is used to power the 2 Watt UHF Amplifier (A2) and the 20 Watt UHF Amplifier (A3) while all other modules are powered by a ±15V/+5V supply. The ±15V/+5V unit is a fully regulated, multiple output, linear power supply. The +28V supply is a high efficiency, single output, switching power supply.

2.3 Power Splitter:

Schematic Diagram N/A ★ CP1

Insertion Loss (INPUT-OUTPUT)	6.25dB
Frequency	450-810MHz

The Power Splitter is a low-loss Wilkinson design which divides the output signal from the Exciter drawer into four signals of equal magnitude and phase. These four in-phase signals are used to separately drive the four parallel amplifier modules (A3A1, A3A2, A4A1, A4A2) contained in the Dual 300W UHF Power Amplifier drawers.

2.4 Dual 300W Power Amplifier Drawer:

Interconnection Diagram 40386003/Rev 56 ★ A3, A4

VISUAL RF IN (J1, J4)	≈+36.7dBm peak visual
VISUAL RF OUT (J2, J5)	≈+55.0dBm peak visual
Visual Gain (J1-J2, J4-J5)	16dB min.

For final amplification this translator is composed of two Dual 300W Power Amplifier drawers (A3, A4) containing two 300W amplifier assemblies in each drawer. Each amplifier assembly amplifies an equal portion of the divided signal from the Power Splitter and provides approximately 300 watts of peak visual power. The individual 300W amplifier unit includes a 60W UHF Amplifier pallet (A1), a two-way Splitter (CP1), two 200W UHF Amplifier pallets (A2, A3), and a two-way Combiner (CP2). The Diagnostic/Control circuitry consists of a Current Monitor board (A1PC1) and a 150°F thermostat (A1S1). Power is supplied to each 300W amplifier assembly by a Single Output +28V, 750W Power Supply (PS1, PS2). Each drawer contains a Status Display board (PC1), which drives the LED indicators on the drawer's front panel showing power supply and temperature status.

2.4a 300W UHF Amplifier:

Schematic Diagram 40386003/Rev 56 ★ A3A1, A3A2, A4A1, A4A2

Gain (J1-J2, J4-J5)	16dB min.
Flatness (J1-J2, J4-J5)	±1dB from 470-860MHz

Each 300W UHF Amplifier consists of a 60W UHF Amplifier (A1), a Splitter (CP1), two 200W UHF Amplifiers (A2, A3), a Combiner (CP2), a Circulator (HY1), a Current Monitor (PC1), and a 150°F thermostat (S1). The 60W UHF Amplifier and the two 200W UHF Amplifiers are class AB, microstrip designs that provide at least 8dB and 7.5dB of gain, respectively. Each amplifier's gain variation from 470 to 860MHz is typically ±0.75dB. The Splitter and Combiner are both two-section Wilkinson couplers which separately contribute about 0.1dB of insertion loss. The Splitter divides the signal from the 60W UHF Amplifier into two signals of equal amplitude and phase. These two in-phase signals are used to separately drive the two 200W UHF Amplifiers. The Combiner joins the amplified signals to form the output of the drawer. The Current Monitor is a Hall Effect sensor which monitors the current drawn by the 60W UHF Amplifier and the two 200W UHF Amplifiers, while applying a signal to the CURRENT SENSE line at pin 6 of connector J3. The information on this line is processed by the fault monitoring/display section of the Control Board (PC1) located behind the Front Panel (A5), which is mounted in the top rack position of the translator cabinet. The thermostat monitors the temperature of the 300W UHF Amplifier's heat sink by grounding pin B of A1PC1J2. If the temperature rises above 175°F, the thermostat opens, placing +5V on pin 10 of CONTROL plug J3 or J6. In turn, the Control Board (A5PC1) responds by placing 5V on Pin 9 of CONTROL plug J3 or J6 disabling the corresponding 28V power supply (PS1 or PS2). As a result, +28Vdc is removed from the 60W UHF Amplifier and the two 200W UHF Amplifiers while the appropriate TEMPERATURE indicator of the Status Display (PC1DS4 or PC1DS8) illuminates yellow. At the same time the COLLECTOR BIAS indicator for that amplifier will extinguish.

2.4b Status Display:

Schematic Diagram 30386105/Rev 52 ★ A3PC1, A4PC1

On each Dual Power Amplifier drawer the Status Display board monitors the +28Vdc voltages from the corresponding Power Supply (PS1/PS2) as well as the status of each thermostat (A1S1/A2S1). The results are displayed on the COLLECTOR BIAS (DS1/DS5) and TEMPERATURE (DS4/DS8) indicators. When the translator's interlock circuit and the thermostats are closed, each power supply provides +28Vdc to the corresponding 300W UHF Amplifier assemblies while the corresponding DS1 and DS5 indicators are illuminated green and DS4 and DS8 are extinguished. When the interlock circuit is opened, each Power Supply is disabled, +28Vdc is removed from each 300W UHF Amplifier, and the corresponding DS1 and DS5 indicators are extinguished while DS4 and DS8 remain out. However, if the circuit breaker on the Front Panel (A5) is in the ON position and the circuit breaker on the Front Panel of the Exciter drawer (A2) is in the OFF position, COLLECTOR BIAS indicators DS1 and DS5 will illuminate green. If either thermostat opens due to high ambient temperature or an amplifier problem, each Power Supply is again disabled. This is indicated by the corresponding DS1 or DS5 indicators being extinguished, and TEMPERATURE indicators DS4 or DS8 illuminating yellow as appropriate.

2.4c +28V Power Supply:

Schematic Diagram N/A ⋆ A3PS1, A3PS2, A4PS1, A4PS2

The+28V Power Supply provides +28Vdc at up to 750W or 27A for the three amplifiers when the translator's interlock circuit is closed. The power supplies are high efficiency, switching types with power factor correction and remote inhibit lines. These power supplies provide the supply voltage to the 60W and 200W UHF amplifier pallets within each 300W UHF Amplifier assembly. The supplies are energized from the Front Panel Control Board (A5PC1) which provides a +5Vdc enable signal to J1-2 of each supply via CONTROL plugs J3-9 and J6-9 of the amplifier drawers. This occurs only when the translator's interlock circuits are closed.

2.5 Power Combiner:

Schematic Diagram N/A ⋆ CP2

Insertion Loss (INPUT-OUTPUT)	0.25dB
Frequency	450-810MHz

The 4-way Power Combiner is a Wilkinson design that combines the four 300 watt amplified signals from each of the Dual 300W UHF Power Amplifier Drawers (A3, A4). The recombined signal is then applied to the Output Bandpass Filter (FL1) and Metering Coupler (DC1).

2.6 Metering Coupler:

Schematic Diagram N/A ⋆ DC1

Insertion Loss (J1-J2)	<0.5dB
FWD Coupling (J1-J3)	45dB
REFLD Coupling (J2-J4)	45dB

The Metering Coupler is a four-port directional coupler that provides samples of the translator's forward and reflected output power. These samples are used by the Metering Detector (A7) to drive the output % POWER meter.

2.7 Front Panel:

Interconnection Diagram N/A ⋆ A5

Located in the top rack position, the Front Panel holds the AC POWER circuit breaker, the Metering Detector (A7) and the Control Board (PC1).

2.7a Metering Detector:

Schematic Diagram 30368024/Rev P ★ A5A7

The Metering Detector contains separate but similar circuitry for monitoring the peak forward and average reflected power at the output of the translator. Samples of these two RF signals are supplied by the Directional Coupler mentioned above.

The front end or detector portion of each circuit is basically the same. Diodes CR2 and CR4, together with their surrounding components, convert the sampled on-channel RF signals to positive dc voltages proportional to the detected RF power. Detection of the sampled output carrier is accomplished by CR2 in conjunction with R4 and C2 which form a time constant of 1 second. R4 is the dc load while C1 and C11 form the RF ground of the visual power detector. Detection of the sampled reflected signal is the same except for a faster time constant furnished by R22/C6 (1 millisecond). The positive dc voltages from the visual and reflected power detectors are processed by buffer amplifiers U1 and U2 which provide voltage gains of 1V/V and 2V/V, respectively. These buffer amplifiers also provide isolation between the % POWER meter and the detector. The settings of potentiometers R9 and R27 determine the voltage level applied to the % POWER meter when the meter switch (PC1S1) is in its VISUAL or REFL positions, respectively. The aural power detector is not used in this application.

A dc voltage proportional to the translator's forward output power is applied to pin 5 of connector J4, designated VIS PWR REF. This voltage is fed back to the Exciter drawer's Control Board (A2PC1). When the OUTPUT AGC switch (A2S2) is in its ON position, this voltage ultimately controls the attenuation of the visual IF signal so that the translator's forward output power is automatically maintained at its rated value.

A dc voltage proportional to the translator's reflected output power is fed to pin 10 of comparator U2. This voltage is compared to a reference voltage at pin 9 whose magnitude is determined by potentiometer R30. With R30 properly set (see paragraph 3.5b), the voltage on pin 10 will be greater than the reference voltage whenever the translator's reflected power is more than 10% of its rated forward power. As a result, the output of the comparator saturates in the positive mode applying approximately +4Vdc to the VSWR OVLD line. This voltage instructs the Control Board (PC1) that a VSWR overload condition has been detected. If the translator's reflected power is less than 10% of its rated forward power, the voltage on pin 10 of comparator U2 will be less than the reference voltage. As a result, the comparator saturates in the negative mode, diode CR1 is forward biased, and approximately −0.7Vdc is applied to pin 7 of connector J4. This voltage instructs the Control Board that no VSWR overload condition exists and, therefore, no action is taken.

2.7b Control Board:

Schematic Diagram 40386012/Rev 55 ★ A5PC1

The Control Board provides various monitoring, control and display functions in conjunction with an interface for remote monitoring. The circuitry of this board can be divided into four sections:

(1) VSWR OVLD Monitoring/Interlock Control
(2) 300 Watt UHF Power Amplifier Fault Monitoring/Display
(3) 300 Watt UHF Power Amplifier Temperature Monitoring/DC Control
(4) Metering Display

The VSWR OVLD Monitoring/Interlock Control section is made up of two separate circuits. One monitors the VSWR OVLD and the Remote ON/OFF. This circuit is centered around two one-shot multivibrator circuits, U1A and U1B, and a two-bit binary counter formed by flip-flops U2A and U2B. The other circuit is comprised of three OR gates U16A, C, D, and monitors the Fault lines for the four 300 Watt Power Amplifiers.

Under normal operating conditions the VSWR OVLD line (J2-14) is low and Q1 is turned off with +5V at its collector. The OUTput of U1A (pin 5) is low and becomes inverted by U10D before being ANDed with the REMOTE ON/OFF (J2-1) signal at U4A. The high output of U4A is inverted by U10E, placing a low at J1-1 which is fed to the Control Board of the Exciter (A2PC1). The REMOTE ON/OFF line is high for an ON condition and low for an OFF condition. If the REMOTE ON/OFF is not connected, R12 holds the line high simulating a REMOTE ON. U4D ANDs together the normally low Q outputs (pins 5 and 9) of U2A and U2B producing a low at its output. When the Exciter drawer's POWER circuit breaker is set to ON, the outputs of U2A and U2B are cleared as Q2 provides a ground to the CLR pins 1 and 13. Q2 is turned on because the +15V supply rises to +5Vdc before the +5V supply does producing a negative voltage at the output of U7A. After the +5V supply reaches +5Vdc, +0.3V higher than the inverting input is clamped by zener diode VR1, the output of U7A goes high turning off Q2. The low output of U4D is ANDed with the normally low OUTput of U1B at U4C which delivers a low to the Exciter drawer on pin J1-19, EXCITER VSWR OVLD.

When REFLected power exceeds 10% of the FWD power (or whatever ratio the trip point was set at), the VSWR OVLD line (J2-14) from the Metering Detector is pulled high. This action turns on Q1 grounding the TRIG inputs of U1A and U1B and the CLR input of U2A. The OUTput of U1A goes high for 10 seconds, placing a high on J1-1 and shutting down the translator. For 4 1/2 minutes the OUTput of U1B will also be high. When the translator is shut down, there is no output power and the VSWR OVLD line goes low turning off Q1. The resulting low to high transition at the collector of Q1 triggers the clock input of U2A, flip-flopping its outputs so that Q is now high. If the reflected power exceeds 10% a second time within four minutes of the first, U1A will again shut the translator down for 10 seconds and then bring it back up. U1B will continue to be high and the Q outputs of U2A and U2B will count up one. A third occurrence of a VSWR overload within approximately four minutes of the first will have the same results as the previous occurrence except that, when U1A brings the system back on line, the flip-flop counter will reach binary three; the Q outputs of U2A and U2B will both be high. This causes the output of U4D to go high which, together with the high OUTput of U1B, drives U4C high placing 5V on J1-19, the EXCITER VSWR OVLD line.

The AMPL FAULT lines from the four 300 Watt UHF Power Amplifiers are monitored by OR gates U16A and U16C. These lines are normally high, driving the output of U16D high and holding the RF DRIVE CONTROL line at +5V which connects back to the interlock section of the Exciter's Control Board (A2PC1). Provided the power amplifier's +28V Power Supply is turned on and operating correctly, this line will stay high. Otherwise, it will go low and the Interlock circuit will open placing the translator in standby.

The 300 Watt UHF Power Amplifier Fault Monitoring/Display section gets its input signals from the four CURRENT SENSE lines (J1-21, J1-3, J1-2, and J1-22) furnished by the Hall Effect CURRENT MONITORS (A1PC1 and A2PC2) mounted with each amplifier. Each of these signals is passed through its own unity gain amplifier (U20A through U20D) and is sent out on the REMOTE CURRENT SENSE lines to an optional REMOTE MONITOR via J1-5, J1-6, J1-23 and J1-24.

The four U6 op-amps, in conjunction with U7C, produce a voltage that is the average of the four CURRENT SENSE voltages. With the four U6 op-amps wired as unity gain amplifiers, the voltage at pin 10 of U7C is equal to one half of the average input to U6A, U6B, U6C and U6D. Normally the voltage at pin 8 of U7C is near 0V and negligible. The U8 op-amps compare each of the

buffered CURRENT SENSE input signals to 86% of the average. When the translator is ON and the 300 Watt UHF Power Amplifiers are operating normally, the outputs of U6A, U6B, U6C, and U6D are each greater than 86% of their average causing U8A, U8B, U8C, and U8D to saturate to +15V. The resistive voltage divider at the output of each U8 op-amp divides the +15V down to 4.2V, a TTL level, for input to the inverters and buffers – U9 and U10. This causes the associated U9 buffers to be high, illuminating the green section of indicators AMPL 1 (DS1), AMPL 2 (DS2), AMPL 3 (DS3), and AMPL 4 (DS4). At the same time the U10 inverters are low, forward biasing diodes CR9, 11, 13 and 15 while extinguishing the red section of the indicators.

If a CURRENT SENSE voltage from one of the 300W Amplifiers drops by more than 14%, the output of its corresponding U8 comparator will go to –15V and the inputs of the associated inverter and buffer will go to 0.5V. This extinguishes the green section of the associated AMPL indicator and illuminates the red section.

Because the four 300W Power Amplifiers (A3A1, A3A2, A4A1, A4A2) may not all draw the same current, the CURRENT SENSE circuit sometimes can indicate that a fault has occurred when the amplifiers are actually operating within tolerance. To prevent this, each input has a balance potentiometer, R20, R25, R29 and R34. These can be adjusted so that the inputs to each of the four U6 op-amps are the same level. Section 3.7 explains the procedure for adjusting these potentiometers.

The 300 Watt UHF Power Amplifier Temperature Monitoring/DC Control section takes the THERMAL MONITOR lines from the Power Amplifiers as its inputs. Normally these lines (J1-15, J1-34, J1-16, and J1-35) are low. The circuit containing U7D and Q3 is identical to the U7A/Q2 circuit in the VSWR OVLD section. When the translator is turned on, Q3 conducts clearing flip-flops U12A, U12B, U11A, and U11B. This sets the flip-flop outputs to their normal states where Q is low and $\overline{Q}$ is high. The Q outputs drive the THERMAL OVLD INDICATOR lines along with the U19 buffers which drive the REMOTE THERMAL OVLD INDICATOR lines connector to REMOTE MONITOR plug J4 (pins 14 thru 17). Each $\overline{Q}$ output connects to a U14 NAND gate and, being normally low, the output of each NAND gate holds its connected transistor (Q4 through Q7) in the on condition so that the DC CONTROL lines are high.

If the translator's Interlock system opens, the FINAL PS INHIBIT at pin J1-29 will go low, driving U14A, B, C, and D high. This will turn off their respective transistors (Q4 thru Q7) thereby grounding the DC CONTROL lines and shutting off each 300 Watt UHF Power Amplifier +28V Power Supply. With the +28V Power Supply off in each Power Amplifier, the voltage on the CURRENT SENSE lines will be 0V. This could cause one or more of the AMPLIFIER STATUS indicators to illuminate red incorrectly indicating a fault in an amplifier. Inverter U10C corrects this. A low on the FINAL PS INHIBIT line drives U10C high placing a small positive voltage on pin 9 of U7C. This voltage is approximately 0.1V and is sufficient to keep the outputs of the U8 op-amps saturated at +15V and the AMPLIFIER STATUS indicator illuminated green. The FINAL PS INHIBIT line is normally high and originates on the Exciter's Control Board (A2PC1).

When an amplifier's heat sink temperature exceeds 150°C, its THERMAL MONITOR line goes high triggering the associated flip-flop and driving the corresponding THERMAL OVLD INDICATOR line high. The REMOTE THERMAL OVLD INDICATOR line is also forced high along with NAND gate U14, which shuts down the PNP transistor supplying +5V to the amplifier's DC CONTROL line. 0V on one of the DC CONTROL lines shuts off the appropriate +28V Power Supply and its associated Power Amplifier. The affected amplifier and power supply will remain off until the MOMENTARY TEMP RESET switch is depressed triggering the CLR inputs on the U11 and U12 flip-flops. (Removing and reapplying AC POWER to the translator will also clear the flip-flops.) Because this type of fault places an amplifier's power supply in standby, its CURRENT SENSE level drops to 0V causing the appropriate AMPL fault indicator to illuminate red.

The RF ENABLE IN line at J2-8 takes the switched +28V from the EXCITER drawer (A2) and voltage divides it to a high TTL logic level for the RF ENABLE OUT pin at J2-7. This provides a logic signal to the REMOTE MONITOR plug J4 (pin 23) indicating that RF drive has been enabled (high) or disabled (low).

The Metering Display section consists of three 10-segment LED bar graphs (DS6, DS7 and DS8) and their drivers (U13, J17 and U18). Switch S1 selects the FORWARD or REFLected voltage directly from the Metering Detector at J1-36 or J1-17 and delivers it to the LED drivers. Unity gain op-amps U21C and U21A provide FORWARD METER and REFLected METER signals to the REMOTE MONITOR plug (J4) via pins J1-37 and J1-18 respectively.

2.8 Output Filter:

Schematic Diagram N/A ★ FL1

Insertion Loss (J1-J2) <0.5dB

The Output Filter, located in the bottom of the translator cabinet, is a multisection bandpass resonant cavity type. This filter is tuned to channel by the EMCEE test department and is not field serviceable. If it becomes necessary to have the filter retuned, contact the EMCEE Customer Service Department for a return authorization.

UHF SYNTHESIZER PROGRAMMING CHART (NTSC)

Channel	Visual Frequency (MHz)	LO Freq (MHz)	S4	S3	S2	S1
14	471.25	517	0	A	1	9
15	477.25	523	0	A	3	7
16	483.25	529	0	A	5	5
17	489.25	535	0	A	7	3
18	495.25	541	0	A	9	1
19	501.25	547	0	A	A	F
20	507.25	553	0	A	C	D
21	513.25	559	0	A	E	B
22	519.25	565	0	B	0	9
23	525.25	571	0	B	2	7
24	531.25	577	0	B	4	5
25	537.25	583	0	B	6	3
26	543.25	589	0	B	8	1
27	549.25	595	0	B	9	F
28	555.25	601	0	B	B	D
29	561.25	607	0	B	D	B
30	567.25	613	0	B	F	9
31	573.25	619	0	C	1	7
32	579.25	625	0	C	3	5
33	585.25	631	0	C	5	3
34	591.25	637	0	C	7	1
35	597.25	643	0	C	8	F
36	603.25	649	0	C	A	D

Table 2–1

UHF SYNTHESIZER PROGRAMMING CHART (NTSC)

Channel	Visual Frequency (MHz)	LO Freq (MHz)	S4	S3	S2	S1
37	609.25	655	0	C	C	B
38	615.25	661	0	C	E	9
39	621.25	667	0	D	0	7
40	627.25	673	0	D	2	5
41	633.25	679	0	D	4	3
42	639.25	685	0	D	6	1
43	645.25	691	0	D	7	F
44	651.25	697	0	D	9	D
45	657.25	703	0	D	B	B
46	663.25	709	0	D	D	9
47	669.25	715	0	D	F	7
48	675.25	721	0	E	1	5
49	681.25	727	0	E	3	3
50	687.25	733	0	E	5	1
51	693.25	739	0	E	6	F
52	699.25	745	0	E	8	D
53	705.25	751	0	E	A	B
54	711.25	757	0	E	C	9
55	717.25	763	0	E	E	7
56	723.25	769	0	F	0	5
57	729.25	775	0	F	2	3
58	735.25	781	0	F	4	1
59	741.25	787	0	F	5	F

Table 2–1

UHF SYNTHESIZER PROGRAMMING CHART (NTSC)

Channel	Visual Frequency (MHz)	LO Freq (MHz)	S4	S3	S2	S1
60	747.25	793	0	F	7	D
61	753.25	799	0	F	9	B
62	759.25	805	0	F	B	9
63	765.25	811	0	F	D	7
64	771.25	817	0	F	F	5
65	777.25	823	1	0	1	3
66	783.25	829	1	0	3	1
67	789.25	835	1	0	4	F
68	795.25	841	1	0	6	D
69	801.25	847	1	0	8	B

Table 2–1

UHF SYNTHESIZER PROGRAMMING CHART (PAL)

Channel	Visual Frequency (MHz)	LO Freq (MHz)	S4	S3	S2	S1
21	471.25	510.15	0	9	F	6
22	479.25	518.15	0	A	1	E
23	487.25	526.15	0	A	4	6
24	495.25	534.15	0	A	6	E
25	503.25	542.15	0	A	9	6
26	511.25	550.15	0	A	B	E
27	519.25	558.15	0	A	E	6
28	527.25	566.15	0	B	0	E
29	535.25	574.15	0	B	3	6
30	543.25	582.15	0	B	5	E
31	551.25	590.15	0	B	8	6
32	559.25	598.15	0	B	A	E
33	567.25	606.15	0	B	D	6
34	575.25	614.15	0	B	F	E
35	583.25	622.15	0	C	2	6
36	591.25	630.15	0	C	4	E
37	599.25	638.15	0	C	7	6
38	607.25	646.15	0	C	9	E
39	615.25	654.15	0	C	C	6
40	623.25	662.15	0	C	E	E
41	631.25	670.15	0	D	1	6
42	639.25	678.15	0	D	3	E
43	647.25	686.15	0	D	6	6
44	655.25	694.15	0	D	8	E

For PAL operation the grounds to Pins 21 and 23 of U1 (MC145152) must be removed.

Table 2–1

UHF SYNTHESIZER PROGRAMMING CHART (PAL)

Channel	Visual Frequency (MHz)	LO Freq (MHz)	S4	S3	S2	S1
45	663.25	702.15	0	D	B	6
46	671.25	710.15	0	D	D	E
47	679.25	718.15	0	E	0	6
48	687.25	726.15	0	E	2	E
49	695.25	734.15	0	E	5	6
50	703.25	742.15	0	E	7	E
51	711.25	750.15	0	E	A	6
52	719.25	758.15	0	E	C	E
53	727.25	766.15	0	E	F	6
54	735.25	774.15	0	F	1	E
55	743.25	782.15	0	F	4	6
56	751.25	790.15	0	F	6	E
57	759.25	798.15	0	F	9	6
58	767.25	806.15	0	F	B	E
59	775.25	814.15	0	F	E	6
60	783.25	822.15	1	0	0	E
61	791.25	830.15	1	0	3	6
62	799.25	838.15	1	0	5	E
63	807.25	846.15	1	0	8	6
64	815.25	854.15	1	0	A	E
65	823.25	862.15	1	0	D	6
66	831.25	870.15	1	0	F	E
67	839.25	878.15	1	1	2	6
68	847.25	886.15	1	1	4	E

For PAL operation the grounds to Pins 21 and 23 of U1 (MC145152) must be removed.

Table 2–1

SECTION III

MAINTENANCE

SECTION III

MAINTENANCE

3.1 Periodic Maintenance Schedule:

CHECK	RECOMMENDATION
ALIGNMENT	Upon installation and at one-year intervals thereafter (see section 3.4).
OUTPUT POWER CALIBRATION	SAME AS ABOVE (see section 3.5).
FANS	Inspect as often as possible (at least monthly) and clean when necessary. No lubrication needed.

3.2 Recommended Test Equipment:

EQUIPMENT	MANUFACTURER	MODEL #
Digital Multimeter	HEWLETT PACKARD	E2378A
Oscilloscope	TEKTRONIX	2232
Sweep Generator	WAVETEK	2001
50 Ohm RF Detector	TELONIC BERKELEY	8553
20dB Attenuator	NARDA	766-20
20dB Directional Coupler	NARDA	3001-20
50 Ohm, 1000W Dummy Load	BIRD	8833
Power Meter	HEWLETT PACKARD	435B
Step Attenuator	KAY	1/432
Frequency Counter	HEWLETT PACKARD	5386A
Spectrum Analyzer	HEWLETT PACKARD	8594E
NTSC Video Generator	TEKTRONIX	TSG100

3.3 Troubleshooting:

If the output signals from the translator appear distorted, noisy or nonexistent, consider the following procedure as a troubleshooting aid. This procedure assumes the translator wiring as well as the cabling and connectors are trouble free. It also assumes the Receiver drawer is receiving the appropriate input signal while providing the required visual and aural IF carriers. The general problem area will be indicated by simply checking the front panel diagnostic lights as well as the % POWER meters. The diagnostic indicators are located on the front panels of the UHF Exciter/ Upconverter (A2), the Front Panel (A5) and the Dual 300W Power (Final) Amplifier drawers (A3, A4).

3.3a Front Panel Control Board Indicators:

1. Under normal operation all indicators will be lit green and the RF POWER meter will furnish a 100% indication with the meter switch placed to FWD.

2. Under standby conditions, all indicators will be lit green.

3. Any AMPLIFIER STATUS/AMPL 1, 2, 3 or 4 indicator which turns red during normal operation signifies an amplifier module or power supply malfunction within the drawer specified. Typically the COLLECTOR BIAS LED associated with the failed amplifier or power supply will extinguish unless the announced amplifier failure is an open. In either case, replace the malfunctioning Final Amplifier drawer. If the operator has the appropriate technical experience to locate the malfunction, he may repair the Final Amplifier drawer by replacing its power supply or its power amplifier heat sink assembly instead of replacing the entire drawer.

3.3b Dual 300W Power (Final) Amplifier Drawer Indicators:

COLLECTOR BIAS indicator monitors the voltage applied to the 60 watt driver and two 200 watt final amplifier pallets within the 300W amplifier module. If the power supply malfunctions, this green indicator will turn off. When a COLLECTOR BIAS indicator goes out, the associated Front Panel Control Board (A5PC1) AMPLIFIER STATUS/AMPL 1, 2, 3 or 4 indicator will turn red.

The TEMPerature indicator monitors the thermostat fixed to the heat sink of the drawer's amplifier section. If the heat sink temperature exceeds 150°F due to high ambient temperature or because of an amplifier malfunction, the thermostat will open shutting off the amplifier's power supply and illuminating the yellow TEMP indicator. Since the 28Vdc power supply is now off, the COLLECTOR BIAS LED will have turned off and the related Control Board AMPLIFIER STATUS (1, 2, 3 or 4) indicator will turn red. If any of the above malfunctions occur, the Final Amplifier drawer should be substituted or, depending on the problem's location, the drawer's power supply or amplifier section should be replaced.

3.3c UHF Exciter/Upconverter Indicators:

Under normal operating conditions, the OPERATE/ALIGN and STBY/OPERATE switches will be in the OPERATE position, the FINAL BIAS, ON, OPERATE, SYNTH LOCK and DRIVER AMP indicators should be illuminated green and the VSWR OVLD and TEMP EXCITER LEDs should be extinguished.

If the DRIVER AMP LED is lit red, the 20 watt amplifier has failed. Replace the 20 watt amplifier module.

The green SYNTH LOCK indicator turns off when the Exciter's frequency synthesizer is not properly locked. Also, the green FINAL BIAS and ON LEDs will turn off. If the problem persists, the synthesizer should be replaced.

An extinguished ON LED with all other LEDs remaining in their normal states indicates a fault in the Exciter's +28V power supply. Replace the power supply.

The TEMP indicator monitors the thermostat fixed to the heat sink of the drawer's 20 Watt Amplifier. If the heat sink temperature exceeds 150°F due to high ambient temperature or because of an amplifier malfunction, the thermostat will open, illuminating the Exciter's yellow TEMP indicator. This will also cause the FINAL BIAS and ON LEDs to turn off indicating that the +28V has been removed from the Exciter's 2 watt and 20 watt amplifiers. Replace any faulty modules and ensure that fans are operational and have adequate room to ventilate the drawer.

If the FINAL BIAS and ON LEDs are extinguished for 10 seconds and then come back on with all other LEDs remaining in their normal states, the system was in a state of temporary VSWR overload. If this occurs two more times within a 4 1/2 minute period, the VSWR OVLD indicator will illuminate and the translator will be placed in a permanent standby mode. This condition is accompanied by the FINAL BIAS and ON indicators remaining off, indicating that the +28V has been removed from the Exciter's 2 watt and 20 watt amplifiers. Under this condition, the cause of the VSWR problem at the translator's output must be cleared before lifting the VSWR OVLD RESET switch to reactivate the unit. If the FINAL BIAS and ON LEDs are extinguished and do not come back on and all other LEDs remain in their normal states, this indicates that the appropriate receive signal is not being detected at the input of the Receiver drawer. Check the receive antenna, preamplifier (if used) and the down lead cabling to ensure that the receive signal is present. If the receive signal is present, troubleshoot the Receiver.

The OPERATE indicator will be green if the position of the OPERATE/ALIGN switch is up. This is the appropriate position when the translator is on the air. The OPERATE/ALIGN switch should only be in the ALIGN position (down) while performing sweep alignment of the Exciter. This switch position sets the AGC for minimum signal attenuation.

3.3d Receiver Drawer Indicators:

The CARRIER PRESENT green LED indicates that the Receiver is seeing an input signal of appropriate frequency and amplitude necessary to develop the IF AGC voltage which places the translator in operation.

3.3e TU1000F V/U Troubleshooting Chart:

The following chart is meant as an aid for uncovering faults that have developed in this translator. During normal operation, all indicator LEDs are green, except the VSWR OVLD LED which is normally extinguished. This chart lists the LEDs that are indicating a fault (i.e., are not in their normal state). If a problem develops, note the state of the indicator LED and compare it to the chart.

TU1000F V/U TROUBLESHOOTING CHART

PROBLEM	INDICATORS	CAUSE	SOLUTION
NO OUTPUT POWER	ALL EXCITER INDICATORS UNLIT	+5VDC Power Supply faulty or shorted	Check Meter reading for 5V. Replace power supply if necessary.
	SYNTH LOCK UNLIT ON UNLIT FINAL BIAS UNLIT	Defective Synthesizer	Check synthesizer for correct output level and frequency. Replace if faulty.
	FINAL BIAS UNLIT ON UNLIT	Operate/Standby switch on Standby	Place switch to Operate.
		Turned off by Remote	Ensure translator has not been turned off by remote.
		No signal detected at input of Receiver	Check cabling. Trouble-shoot Receiver if faulty.
		Temporary VSWR overload	Will return after 10 seconds.
	ON UNLIT	+28V Exciter Supply faulty	Replace power supply.
	DRIVER AMP RED	20 Watt Amplifier faulty	Replace module.
	TEMP YELLOW FINAL BIAS UNLIT ON UNLIT	High ambient temperature	Ensure fans are operational and have adequate room ventilation. If problem persists, check for faulty operation of amplifier and replace if necessary.

TU1000F V/U TROUBLESHOOTING CHART

PROBLEM	INDICATORS	CAUSE	SOLUTION
NO OUTPUT POWER	VSWR OVLD RED ON UNLIT FINAL BIAS UNLIT	VSWR overload has occurred.	Check the transmission line and antenna for high VSWR. Repair or replace any component with a high VSWR. Clear problem at translator's output, then lift the VSWR OVLD RESET switch.
	No fault indicated	Receiver failure Bad cable	Repair Receiver. Check cabling between the Receiver and Exciter.
LOW OUTPUT POWER OR DISTORTED OUTPUT	No Fault indicated	Output Power Calibration is incorrect Receiver malfunction High loss in one of the modules RF chain misaligned Precorrector improperly adjusted or not turned on	See Section 3.5. Repair Receiver. Test each module for correct gain/loss. See Signal Flow Diagram (Fig. 3–2) for gains/ losses. See Section 3.4. See Section 3.6.
	TEMPERATURE YELLOW COLLECTOR BIAS UNLIT AMPL 1,2,3 or 4 UNLIT	Heat sink temperature too high due to high ambient temperature Heat sink temperature too high due to amplifier mal-function	Ensure fans are opera-tional and have adequate room ventilation. Replace faulty amplifier assembly.
	COLLECTOR BIAS UNLIT AMPL 1,2,3 or 4 RED	Faulty +28V Power Supply Power supply exceeded current limit due to mal-functioning amplifier module	Replace power supply. Replace amplifier assembly.

TU1000F V/U TROUBLESHOOTING CHART

PROBLEM	INDICATORS	CAUSE	SOLUTION
LOW OUTPUT POWER OR DISTORTED OUTPUT	AMPL 1,2,3 or 4 RED	Faulty 300W Amplifier	Replace amplifier assembly.
CONTACTOR CYCLES	28VDC reading on Exciter % power meter will cycle	Internal Short on 28V	Unplug each module and check for a short. Replace module(s) or amplifier assembly as needed.
		Power Supply folds back when under a load	Replace Power Supply.
HIGH OUTPUT POWER AND DISTORTED	Several red bars on % RF POWER meter lit and POWER ADJUST does not reduce output	AGC loop is broken	Ensure OPERATE/ALIGN set to OPERATE.
		Misaligned AGC trap in IF AGC Amplifier	Readjust visual IF trap inductor core.
		IF AGC Amplifier or Limiter/Output AGC circuit failure	Replace IF AGC Amplifier or Limiter/Output AGC PC board.
		Failure in Exciter IF Converter	Replace IF Converter module.

3.4 Translator Alignment:

3.4a Receiver Alignment:

1. Remove the four screws on the front panel of the Receiver drawer, carefully pull out the drawer, and remove the top cover. Set up the test equipment as shown in Figure 3–4. Place the Receiver's front panel AC POWER switch (S2) to ON and place the Exciter's front panel AC POWER switch (A2CB1) to OFF.

2. Disconnect the coaxial cable from the output connector of the Vectron Oscillator. Connect a power meter to the output of the oscillator (point **A** of Figure 3–4). An indication of 3mW to 6mW should be present. (If the oscillator's output power is low or nonexistent, return the oscillator to EMCEE for repair or replacement as this is not a field repairable item.)

3. Connect a frequency counter to the oscillator output and wait approximately fifteen (15) minutes for the oscillator to heat or until the frequency stabilizes.

4. If the measured frequency differs by more than 50Hz from the oscillator's designated frequency, proceed to step #5. If the measured frequency is within 50Hz of the designated frequency, then remove the frequency counter from the output of the oscillator, reconnect this module to the input of the multiplier and proceed to step #7.

5. Remove the cover screw from the side of the oscillator exposing the access hole and, with a small tuning tool, slowly vary the frequency adjust potentiometer for the correct frequency.

6. Remove the frequency counter from the output of the oscillator and reconnect this module to the input of the multiplier (A3).

7. Remove the retaining screws and lift the multiplier module off the Receiver's chassis. Connect a spectrum analyzer to the output connector (J2) of the multiplier (point **B** of Figure 3–4). Tune the spectrum analyzer to either the second, fourth, or sixteenth harmonic of the oscillator frequency depending on whether a X2, X4, or X16 Multiplier is being used. (The X2 Multiplier is used for VHF channels 2-6, the X4 Multiplier is used for VHF channels 7-13, and the X16 Multiplier is used for UHF channels 14-69). Carefully "touch up" the capacitors accessible through the bottom cover of the module for maximum power (10 to 30mW) at the proper harmonic of the oscillator frequency. If power is low or nonexistent, proceed to step #8, #9, or #10 depending on whether a X2, X4, or X16 Multiplier is being used. Otherwise, proceed to step #11.

8. **X2 Multiplier (Ch.2-6)**

   a. Remove the module's bottom cover and tune capacitors C7, C12, C13, C14, C15, C16, C17 and inductors L6, L7, L8 for a minimum of 10mW at the oscillator's second harmonic (see Schematic B280-35). Insure that the fundamental and other harmonics are at least 20dB below the second harmonic.

      NOTE: If the X2 Multiplier's output power is low or nonexistent, troubleshoot the circuit and repeat the tuning procedure given in step #8a.

b. Replace the bottom cover and slightly readjust capacitors C12, C13, C14, C15, C16, and C17 for the specifications stated in step #8a. When these specifications are obtained, proceed to step #11.

9. **X4 Multiplier (Ch.7-13)**

a. Remove the bottom cover of the module and disconnect the jumper wire attached to terminal post D on the X4 Multiplier's PC board (see Schematic C331-24).

b. Solder an open-ended 50 ohm coaxial cable to terminal posts D (center conductor) and K (shield) and connect a spectrum analyzer to the opposite end of the coaxial cable.

c. Tune the spectrum analyzer to the second harmonic of the oscillator's output frequency and adjust capacitors C7, C12 through C17 and inductors L6, L7, and L8 for maximum power (25 to 55mW) at the second harmonic of the oscillator's output frequency. Insure that the other harmonics are at least 40dB below the second harmonic by tuning capacitors C14 and C16 near minimum coupling (least capacitance) without sacrificing power.

d. Remove the coaxial cable from terminal posts D and K. Resolder the jumper wire which connects terminal posts D and E.

e. Disconnect the jumper wire attached to terminal post M on the X4 Multiplier's PC board (see Schematic C331-24).

f. Solder the open-ended 50 ohm coaxial cable to terminal posts M (center conductor) and N (shield). Connect a spectrum analyzer to the opposite end of the coaxial cable.

g. Tune the spectrum analyzer to the frequency of the oscillator's fourth harmonic and adjust capacitors C19, C22, and C23 for maximum power (75 to 100mW) at that frequency. Insure that all other harmonics are at least 20dB lower.

h. Remove the coaxial cable from terminal post M and ground. Resolder the jumper wire to terminal post M.

i. Attach the spectrum analyzer to the output connector (J2) of the X4 Multiplier module (point **B** of Figure 3–4).

j. Tune the spectrum analyzer to the frequency of the oscillator's fourth harmonic and adjust capacitors C19, C22, C23, C26, C27, and C29 for maximum power (10 to 30mW) at the same frequency. Insure that all other harmonics are at least 20dB down from the fourth harmonic.

NOTE: If the output power of any section of the X4 Multiplier is low or nonexistent, troubleshoot the circuit responsible and repeat the alignment procedure.

k. Replace the bottom cover and slightly readjust capacitors C19, C22, C23, C26, C27, and C29 for the specifications stated in step #9j. When the specifications are obtained, proceed to step #11.

10. **X16 Multiplier (Ch.14-69)**

a. For tuning this multiplier fabricate a test cable by soldering a .01μF capacitor to the center conductor of an open-ended 50 ohm cable. Ensure that there is enough outer conductor (braid) available for soldering at the open end and attach a good RF connector (BNC, N, SMA) to the opposite end.

b. Turn the multiplier module over and solder the open capacitor lead of the test cable to the output side of coupling capacitor C8 (see Schematic 30367226) and connect the opposite end of the cable to a spectrum analyzer. Make sure that the test cable outer conductor is soldered to the PC board's ground plane.

c. Adjust the spectrum analyzer to view the fourth harmonic of the oscillator and tune multiplier capacitors C1, C2, C3, C4, C5 and C33 for maximum power at that frequency.

d. Remove the cable from C8 and solder the capacitor lead to the output side of coupling capacitor C17. Remember to solder the braid to ground.

e. Adjust the analyzer to observe the eighth harmonic of the oscillator and tune capacitors C9, C10 and C11for maximum amplitude at that frequency.

f. Unsolder the test cable from C17 and ground and attach a cable to the multiplier output connector J2 (SMA) and connect the opposite end to the spectrum analyzer.

g. Readjust the spectrum analyzer to observe the sixteenth harmonic of the oscillator and tune multiplier capacitors C21, C22, C23, C30, C31 and C32 for maximum power.

h. Carefully retune all the multiplier capacitors for maximum power at the sixteenth harmonic. The multiplier should furnish 20 to 25mW of power.

NOTE: If the output power of any section of the X16 Multiplier is low or nonexistent, troubleshoot the circuit responsible and repeat the tuning procedure.

11. Reconnect the output of the Multiplier to the LO port (J3) of the Downconverter/Preamplifier and secure the module to the bottom of the Receiver drawer.

RF Amplifier Chain

12. Place the Receiver's front panel OPERATE/ALIGN switch (S1) to ALIGN and set up the test equipment as shown in Figure 3–5 with the 10dB attenuator connected to the output of either the VHF or UHF Bandpass Filter (point **A** of Figure 3–5).

13. Adjust the sweep and marker generator for an oscilloscope display width of 15MHz at the input frequency of the Receiver. To prevent overdriving any amplifiers, set the oscilloscope for maximum sensitivity.

14. a. For a VHF input: Adjust capacitors C1 through C5 of the VHF Bandpass Filter (FL1) to obtain a frequency response as that shown in Figure 3–6A. There should be less than 2dB of insertion loss.

b. For a UHF input: Tune capacitors C1, C2, and C3 of the UHF Bandpass Filter (FL1) for a frequency response as that shown in Figure 3–6A with less than 3dB of insertion loss. Only if absolutely necessary, adjust the Variable Coupling Barriers and inductors L1 and L4 for the correct response (see Schematic 10331209).

15. Remove the attenuator from the output of either the VHF or UHF Bandpass Filter (FL1) and connect the attenuator to the output of the Downconverter/Preamplifier module (point **B** of Figure 3–5). Reconnect either the VHF or UHF Bandpass Filter to the input of the Downconverter/Preamplifier (A1).

16. Check the output of the Downconverter/Preamplifier for a gain (with conversion) of 3dB and a frequency response as shown in Figure 3–6A. Correct any slight frequency response variations (tilt) with either the VHF or UHF Bandpass Filter as explained in step #14 of this section. If there are any major frequency response or gain problems (>±1dB), sweep and troubleshoot the Downconverter/Preamplifier by itself.

17. Remove the attenuator from the output of the Downconverter/Preamplifier and connect the attenuator to the output of the IF Amplifier w/SAW Filter (point **C** of Figure 3–5). Reconnect the output of the Downconverter/Preamplifier to the input of the IF Amplifier w/SAW Filter (A2).

18. Check for a frequency response as shown in Figure 3–6B and a minimum gain of 20dB. If there is a major discrepancy in frequency response or gain (±2dB), sweep and troubleshoot the IF Amplifier w/SAW Filter by itself.

19. Disconnect the attenuator from the output of the IF Amplifier w/SAW Filter and connect the attenuator to the output of the Receiver drawer (point **D** of Figure 3–5). Reconnect the output of the IF Amplifier w/SAW Filter to the input of the IF AGC Amplifier (A3).

20. With the Receiver's front panel OPERATE/ALIGN switch in the ALIGN position, adjust the IF AGC Amplifier's TILT ADJ control (R31) to obtain a flat frequency response as shown in Figure 3–6B. The TILT ADJ potentiometer is accessible through the top of the IF AGC Amplifier module. Check the IF AGC Amplifier for a gain of approximately 25dB. (This gain is dependent on the +5Vdc reference voltage provided to the IF AGC Amplifier's variable pin diode attenuator when the Receiver's OPERATE/ALIGN switch is in the ALIGN position.)

Limiter/Output AGC Calibration:

21. Connect an IF modulator to the input of the IF AGC Amplifier (point **C** of Figure 3–5). Adjust the modulator to deliver the visual carrier frequency (45.75MHz) at –39dBm peak power. Place the Receiver's front panel OPERATE/ALIGN switch (S1) to OPERATE.

22. Connect a power meter or spectrum analyzer to the output of the Receiver drawer (point **D** of Figure 3–5).

23. Adjust the AGC REF potentiometer (PC1R8) fully CW and adjust the LIMITER ADJ potentiometer (PC1R13) fully CCW. These two potentiometers are located on the Limiter/ Output AGC board (see Schematic B331-34).

24. Adjust the IF AGC Amplifier's GAIN ADJ potentiometer (A3R15) for a +2dBm signal at the output of the Receiver drawer (see Schematic C331-37). The GAIN ADJ control is accessible through the top of the IF AGC Amplifier module.

25. Recalibrate the modulator so that it now delivers a +1dBm peak visual signal at 45.75MHz to the IF AGC Amplifier module. Slowly adjust IF AGC Amplifier inductor L3 of the visual tank circuit so that a minimum power indication is seen on the external power meter or spectrum analyzer. Inductor L3 is accessible through the top of the IF AGC Amplifier module.

26. Place the Receiver's front panel AGC ON/OFF switch to OFF. Adjust the AGC REF potentiometer (PC1R8) for a –6dBm output level from the Receiver drawer.

27. Slowly adjust the LIMITER ADJ potentiometer (PC1R13) CW until the –6dBm output level begins to fluctuate (i.e., as the limiter circuit begins to activate).

28. Readjust the AGC REF potentiometer to bring the output level from –6dBm down to –9dBm.

29. Short capacitor C2 on the Limiter/Output AGC board.

    NOTE: K1 on the Limiter/Output AGC board will deenergize causing the AGC voltage to be replaced by the PRE AGC REF voltage. This voltage is set by the PRE AGC REF ADJ potentiometer (PC1R25).

30. Adjust the PRE AGC REF ADJ potentiometer (PC1R25) for –8dBm at the output of the Receiver drawer. This potentiometer is located on the Limiter/Output AGC board.

31. Remove the short from across C2.

32. Monitor test point TP1 (OUTPUT AGC) on the Limiter/Output AGC board and vary the Receiver's front panel AGC ADJUST potentiometer (R3) for a 0Vdc reading at TP1.

33. Place the Receiver's front panel AGC ON/OFF switch to ON.

34. If necessary, adjust the Receiver's output power level for –6dBm using the front panel AGC ADJUST potentiometer.

35. Disconnect the power meter or spectrum analyzer from the output of the Receiver drawer. Reconnect the Receiver drawer's IF OUTput to the Exciter/Upconverter drawer's IF INput. Reconnect the IF AGC Amplifier's input to the output of the IF Amplifier w/SAW Filter.

36. Reinstall the top cover to the translator's Receiver drawer. Carefully slide the drawer back into the cabinet and secure it properly.

3.4b Exciter/Upconverter Alignment:

1. If the Exciter is operating, place the Exciter's OPERATE/STANDBY switch to STANDBY and the OPERATE/ALIGN switch to ALIGN. Remove the four screws on the front panel of the Exciter/Upconverter drawer, carefully pull out the drawer, and remove its top cover. Leave the Power Adjust control as it would be for normal operation.

2. Remove the Receiver cable attached to the IF INPUT connector, J1. Set up the test equipment as shown in Figure 3–7. Connect the VHF sweep generator's RF output to the IF INPUT connector of the Exciter. Set the VHF sweep generator to sweep from 36 to 50MHz. (Use 45.75MHz and 41.25MHz markers if available.) Tune the spectrum analyzer

to the UHF Synthesizer's LO frequency. The frequency corresponds to the translator's output channel as shown in Table 2–1.

3. Place the OPERATE/STANDBY switch to OPERATE. Adjust C1, C2, and C3 on the UHF Bandpass Filter to obtain the frequency response shown in Figure 3–6A.

4. If the translator's output channel is being changed to one that is 40MHz or more from the factory preset, connect a spectrum analyzer to the 30dB attenuator in Figure 3–7 to ensure that the sweep appears on the **low side** of the LO. Tune the spectrum analyzer to the UHF Synthesizer's LO frequency as shown in Table 2–1, UHF Synthesizer Programming Chart. Program the synthesizer for the new channel and look for the LO carrier on the analyzer. Tune the analyzer 45.75MHz (38.9MHz for PAL B/G) **below** the LO frequency and tune C1, C2 and C3 of the UHF Bandpass Filter for maximum amplitude of the sweep generator signal on the spectrum analyzer. Replace the analyzer with the sweeper diode detector and adjust the UHF Bandpass Filter for the response of Figure 3–6A as shown on the oscilloscope.

5. Remove the sweep generator cable from the Exciter drawer IF INput connector (J1) and disconnect the RF detector from the drawer's RF OUTput (J2). Replace the Exciter's top cover and push the drawer into the rack replacing the four front panel screws. Reconnect the Receiver cable to the IF INput connector (J1) and the Splitter's RF cable to the IF OUTput connector (J2).

3.5 Output Power Calibration:

To ensure proper transmission, the output power level and % RF Power meter calibration should be checked once every year. With the meter switch in the FWD position, the % RF Power meter has been factory calibrated for 100% with the translator providing 1000 watts peak visual and 50 watts average aural. The average power measurements in this calibration procedure assume that the composite signal from the translator has the aural carrier 13dB down from the visual with the visual carrier having 87.5% video modulation and 0% (sync only) average picture level (APL). Average power levels employing 50% APL (stairstep/ramp/flat field) are included in brackets following the power levels at 0% APL. It is also assumed that the setup in Figure 3–8 is being used and the output of the receiver drawer has been currently calibrated. If the received broadcast channel frequency is in the VHF band (Ch.2-13), the mixer may be removed and the VHF output of the agile modulator can be connected directly to the RF INput (J1) of the Receiver drawer.

3.5a Forward Power:

1. With the Exciter OPERATE/STANDBY switch on STANDBY, set up the test equipment as shown in Figure 3–8.

2. Verify that the modulator is providing 87.5% video modulation and the aural carrier is 13dB down from the visual carrier. With the Receiver OPERATE/ALIGN switch in the OPERATE position and the Meter Switch on FWD, place the Exciter OPERATE/STANDBY switch to OPERATE.

3. To set the output power, adjust the Exciter's POWER ADJUST control for an external power meter reading of 645W [430W]. Note that 1000W peak visual at 0% [50%] APL plus 50 watts average aural for a 13:1 peak visual to average aural ratio equals 645W [430W].

4. To check or adjust visual to aural ratio, replace the power meter in Figure 3–8 with a spectrum analyzer. Adjust the aural carrier level on the modulator for the desired ratio. Remove the spectrum analyzer and return the power meter to the setup to reset the output power. Set the POWER ADJUST again for an external power meter reading of 595W [380W] visual plus the average aural carrier level for the set ratio. Modulators are preset by EMCEE test department.

5. With the external power meter reading correctly, place the Front Panel (A5) meter switch to FWD and check the translator's % RF Power meter for a 100% indication. If this reading is not obtained, adjust potentiometer R9 of the Metering Detector located behind the Front Panel (A5) and accessible through the METER ADJUST hole marked FWD.

3.5b Reflected Power (Optional):

6. Through the METER ADJUST access hole marked VSWR OVLD, adjust potentiometer R30 of the Metering Detector fully clockwise to disable the VSWR overload detection circuit. Place the % RF POWER meter switch to REFL.

7. Place the Exciter's OPERATE/STANDBY switch to STANDBY and the OPERATE/ALIGN switch to ALIGN. Disconnect and reverse the FWD (J3) and REFLD (J4) coupling port cables on the Metering Coupler (DC1). J3 (REFLD) of the Metering Detector (A5A7) should now be connected to J3 (FWD) of the Metering Coupler (DC1). This simulates an open circuit at the translator's RF OUTput (J2) delivering maximum returned power to the reflected power detector. Insert a 1dB step attenuator between the Receiver and the Exciter's IF INput connector and set the attenuator for 10dB of attenuation.

8. Place the OPERATE/STANDBY switch to OPERATE. Remove attenuation from the step attenuator until an external power meter reading of 645W [430W] is reached. Check the front panel % RF POWER meter for a 100% [70%] reading. If the meter is incorrect, adjust it using potentiometer R27 of the Metering Detector found behind the METER ADJUST hole marked REFL.

9. Decrease the translator's power to 10% using the step attenuator (an external power meter reading of 64.5W [43W]). This power level is used for setting the trip point of the VSWR overload detection circuit. Adjust R30 of the Metering Detector, found through the METER ADJUST access hole marked VSWR OVLD, slowly counterclockwise until the front panel VSWR OVLD indicator illuminates red and the translator's output power drops to zero.

10. Check the VSWR OVLD trip point by adding an additional 1dB of attenuation in the step attenuator. Press the momentary VSWR RESET switch to reactivate the translator and remove an additional 1or 2dB of attenuation from the step attenuator. The VSWR OVLD circuit should again trip. If it does not, repeat this section beginning at step #6.

11. Place the Exciter's OPERATE/STANDBY switch to STANDBY. Return the metering cables to their original coupler ports. Place the OPERATE/ALIGN switch to OPERATE, remove the test equipment, properly load the translator output and place the OPERATE/STANDBY switch to OPERATE.

3.6 Precorrection Adjustment:

Adjustment of the precorrection is accomplished with two potentiometers in the IF Upconverter and eight potentiometers in the Linearizer which should not be realigned unless absolutely necessary. (The IF Upconverter and Linearizer can produce unwanted distortion if adjusted incorrectly.) The test equipment which should be available for readjustment of the precorrector is a spectrum analyzer which provides demodulated video for measurement of sync and intermodulation or a waveform monitor and television demodulator for sync and differential gain measurements. Acquire as much of this test equipment as possible since the precorrection accuracy will depend on equipment versatility. It is assumed that the translator's overall frequency response is correct, allowing the unit to operate with maximum efficiency.

1. To the output of the translator connect the test equipment available for monitoring intermodulation, sync amplitude and differential gain.

2. Remove the four screws on the front panel of the 20W Exciter drawer, pull out the drawer, and remove its top cover. Insure switch S1 of the IF Upconverter is in the ON (right) position and S1 of the Linearizer is in the ON position.

3. Place the translator in operation with the system providing its rated output. After demodulating video, slowly adjust R9 and R4 of the IF Upconverter and/or R37, R38, R39, R40, R10, R11, R21 and R22 of the Linearizer for 100% horizontal sync.

4. While looking at the spectral waveform, adjust R4 and R9 of the IF Upconverter and/or R10, R11, R21, R22, R37, R38, R39, and R40 of the Linearizer for minimum in-band intermodulation products. This can be accomplished using a modulated ramp video signal and 100kHz resolution bandwidth on the spectrum analyzer.

5. Check and, if necessary, correct the translator's output power with the front panel POWER ADJUST.

6. Repeat steps #3 through #5 to find the appropriate trade-off for 100% horizontal sync and minimum in-band intermodulation products.

7. Reinstall the top cover to the 20W Exciter drawer, slide the drawer back into the cabinet, secure it, remove the test equipment, and properly load the translator output before reactivation.

3.7 Control Board Setup:

The TU1000F V/U CONTROL BOARD (A5PC1) circuit allows the fault voltages to be balanced preventing fault indications due to gain variations in the 300W Amplifier modules. To set up the CONTROL BOARD the translator must have four 300W amplifier assemblies in good working condition.

1. To set CONTROL BOARD, turn off the translator, remove the four screws on the Front Panel (A5) and pull the panel out.

2. Make sure the board is properly fastened to the panel and both dc plugs properly connected. Turn the four potentiometers at the top of the board (R58, R60, R62, and R64) fully clockwise.

3. Place the translator into operation. Make sure the translator is providing 1000W peak visual (100% on the % RF POWER meter) with a 0% APL video signal and proper depth of modulation.

4. Using a voltmeter, check the voltages at test points TP1, TP2, TP3, and TP4. (NOTE: TP5 is a ground point.) Note which test point has the lowest voltage.

5. Place the voltmeter on the test point with the lowest voltage as noted in the previous step. Adjust the corresponding potentiometer to reduce this voltage by 0.25V to 0.5V. (R58 corresponds to TP1, R60 to TP2, R62 to TP3, and R64 to TP4.)

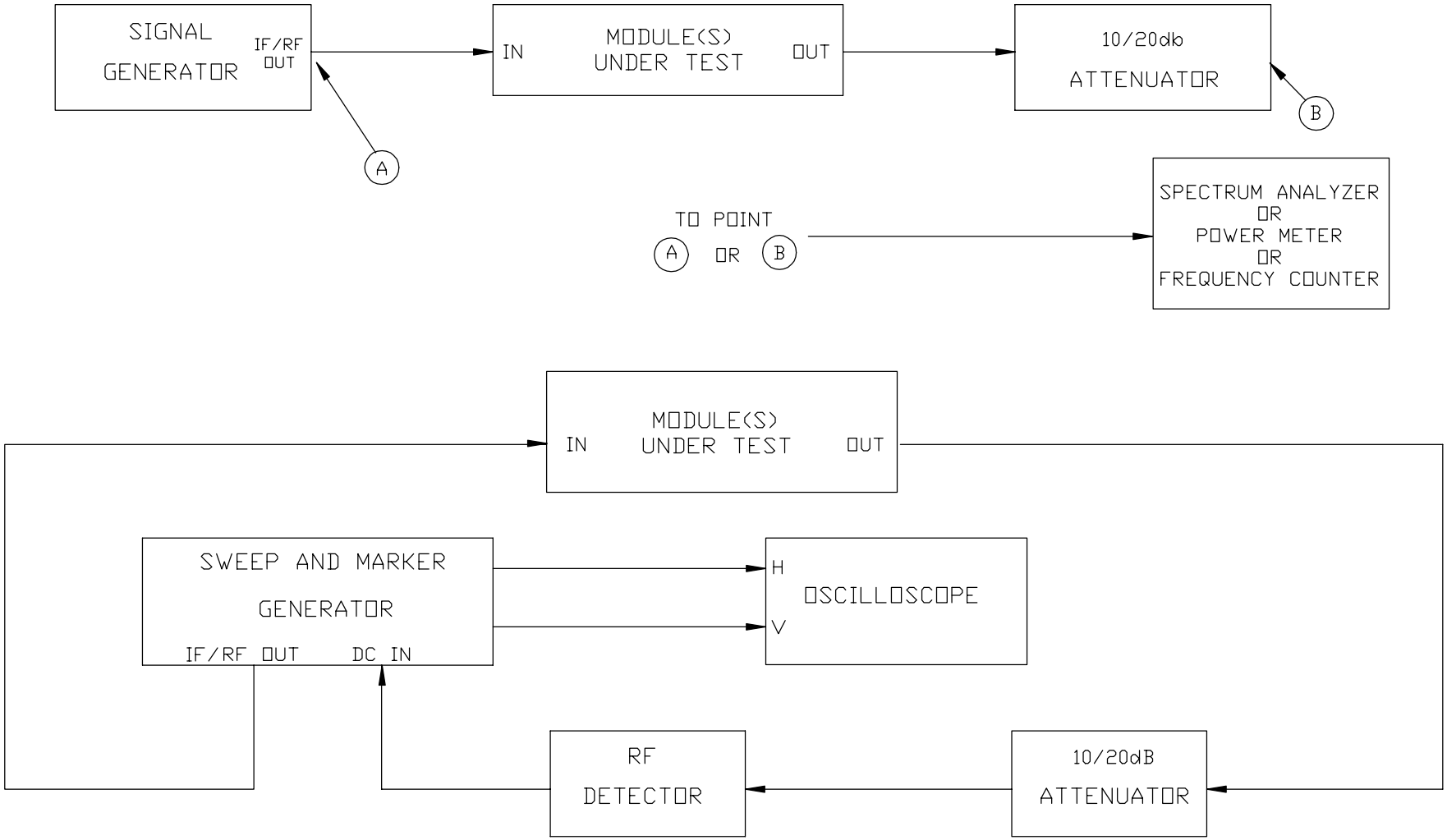
6. Adjust the remaining three potentiometers so that the voltage of the corresponding test point is within ±0.1V of the voltage set in step #5.

7. Disconnect the voltmeter and replace the Front Panel, securing it properly.

3.8 Remote Monitor Signal Levels:

This table lists the signal type and levels provided on the REMOTE MONITOR 25-pin cabinet connector (J4).

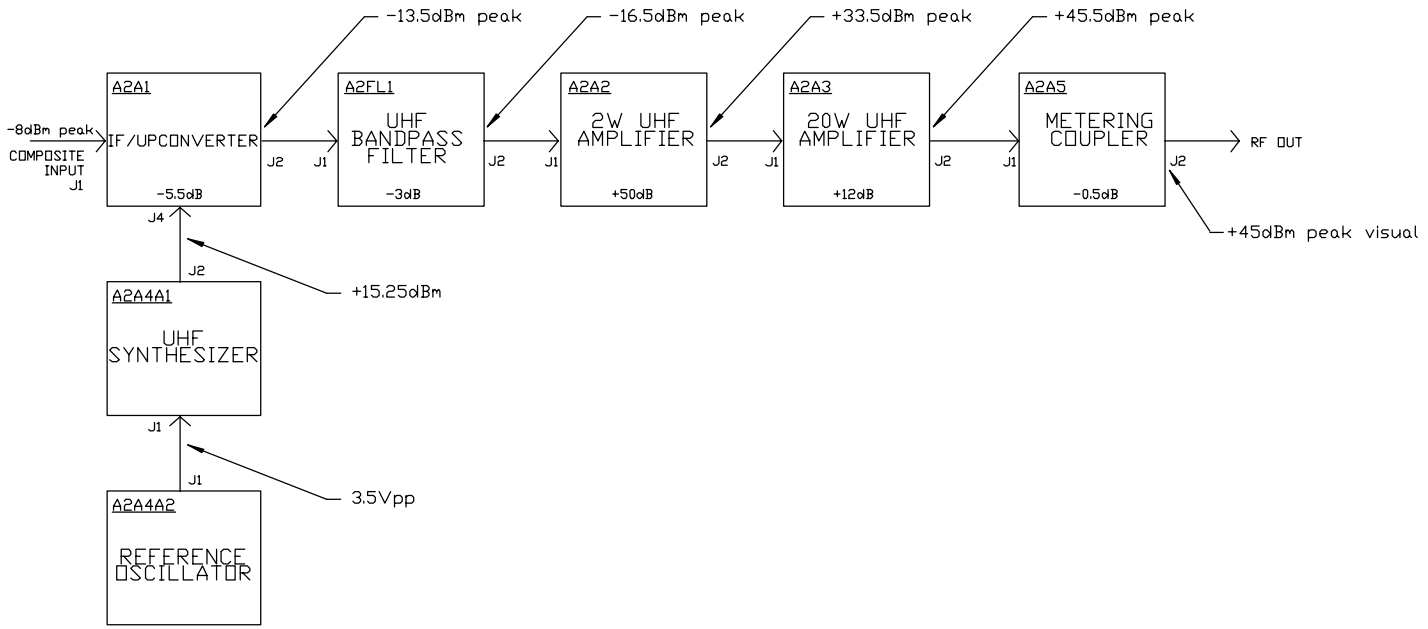
NAME	PIN	I/O	TTL	TYPICAL LEVEL (VOLTS)
FWD POWER	18	O		+5
REFL POWER	19	O		0
RF ENABLE	23	O	X	+5
REMOTE ON/OFF	24	I	X	+5
REMOTE VSWR OVLD RESET	20	I	X	+5
PS FAULT AMPL 1	6	O	X	+5
PS FAULT AMPL 2	7	O	X	+5
PS FAULT AMPL 3	8	O	X	+5
PS FAULT AMPL 4	9	O	X	+5
I SENSE AMPL 1	10	O		+4.5
I SENSE AMPL 2	11	O		+4.5
I SENSE AMPL 3	12	O		+4.5
I SENSE AMPL 4	13	O		+4.5
THERM OVLD AMPL 1	15	O	X	0
THERM OVLD AMPL 2	14	O	X	0
THERM OVLD AMPL 3	16	O	X	0
THERM OVLD AMPL 4	17	O	X	0
+5V POWER SUPPLY	2	O		+5
+15V POWER SUPPLY	3	O		+15
–15V POWER SUPPLY	4	O		–15
+28V POWER SUPPLY	5	O		+28
GND	1, 25			0



TEST EQUIPMENT SETUPS FOR MEASURING THE GAIN OR LOSS OF THE MODULES COMPRISING THE RF AMPLIFIER CHAIN

FIGURE 3-1

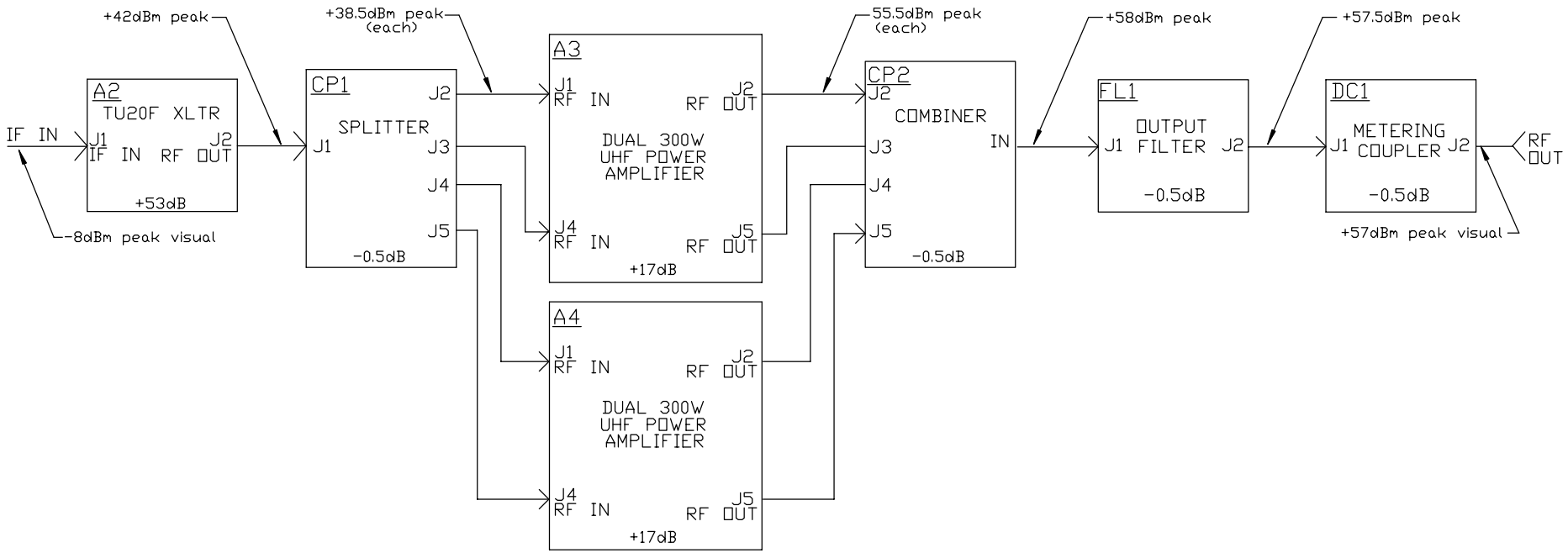
10129783



SIGNAL FLOW DIAGRAM OF THE TU20F EXCITER/UPCONVERTER AMPLIFIER DRAWER

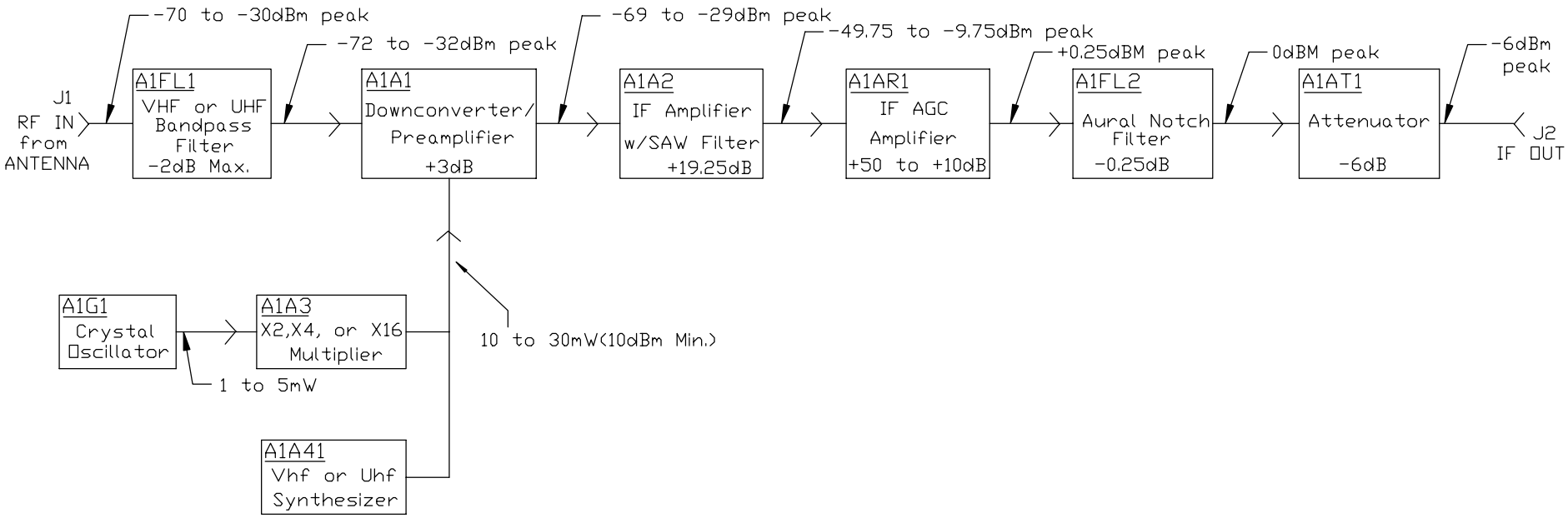
FIGURE 3-2

00300



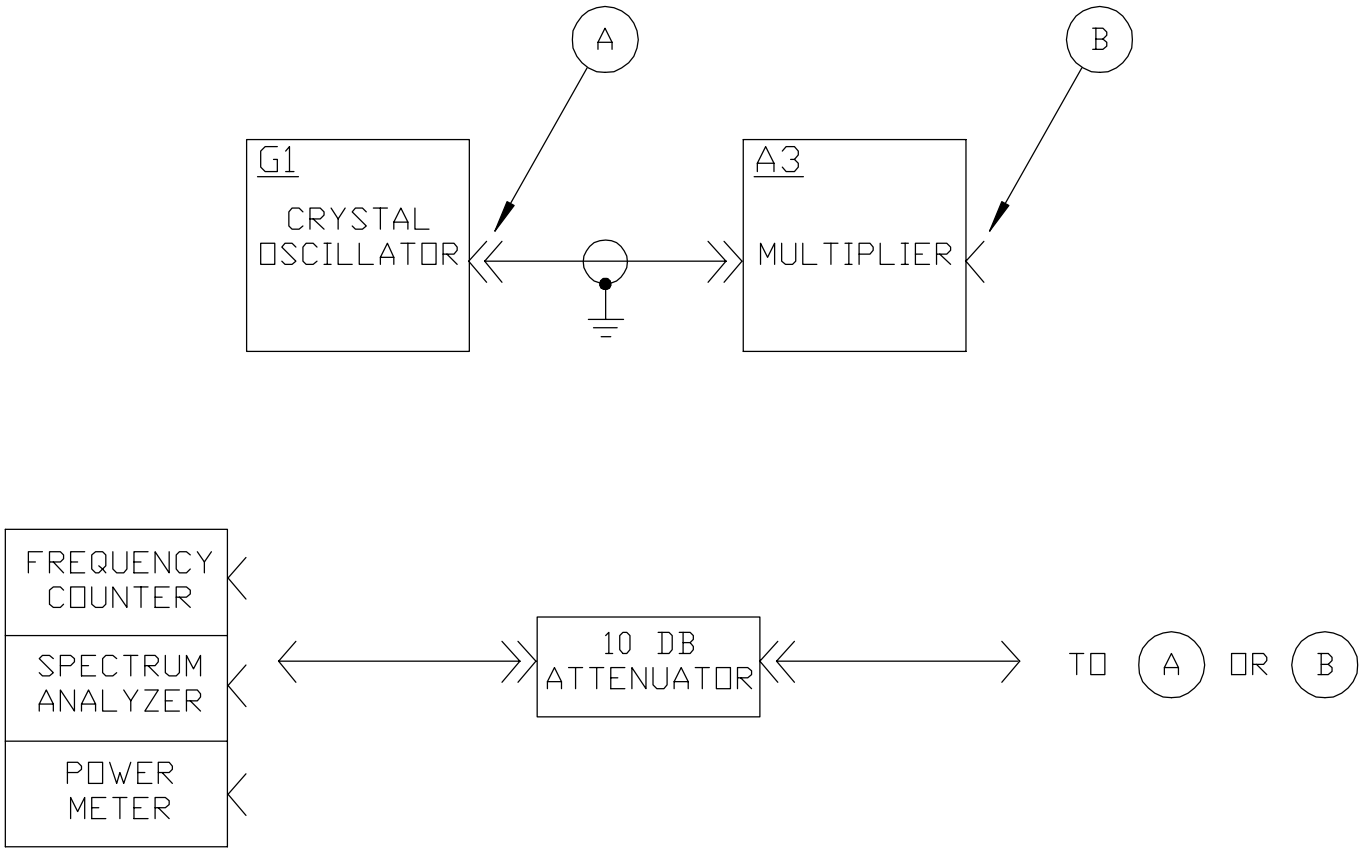
SIGNAL FLOW DIAGRAM OF THE TU1000F TRANSLATOR
FIGURE 3-2A

00301



SIGNAL FLOW DIAGRAM OF THE TU20F RECEIVER DRAWER
FIGURE 3-3

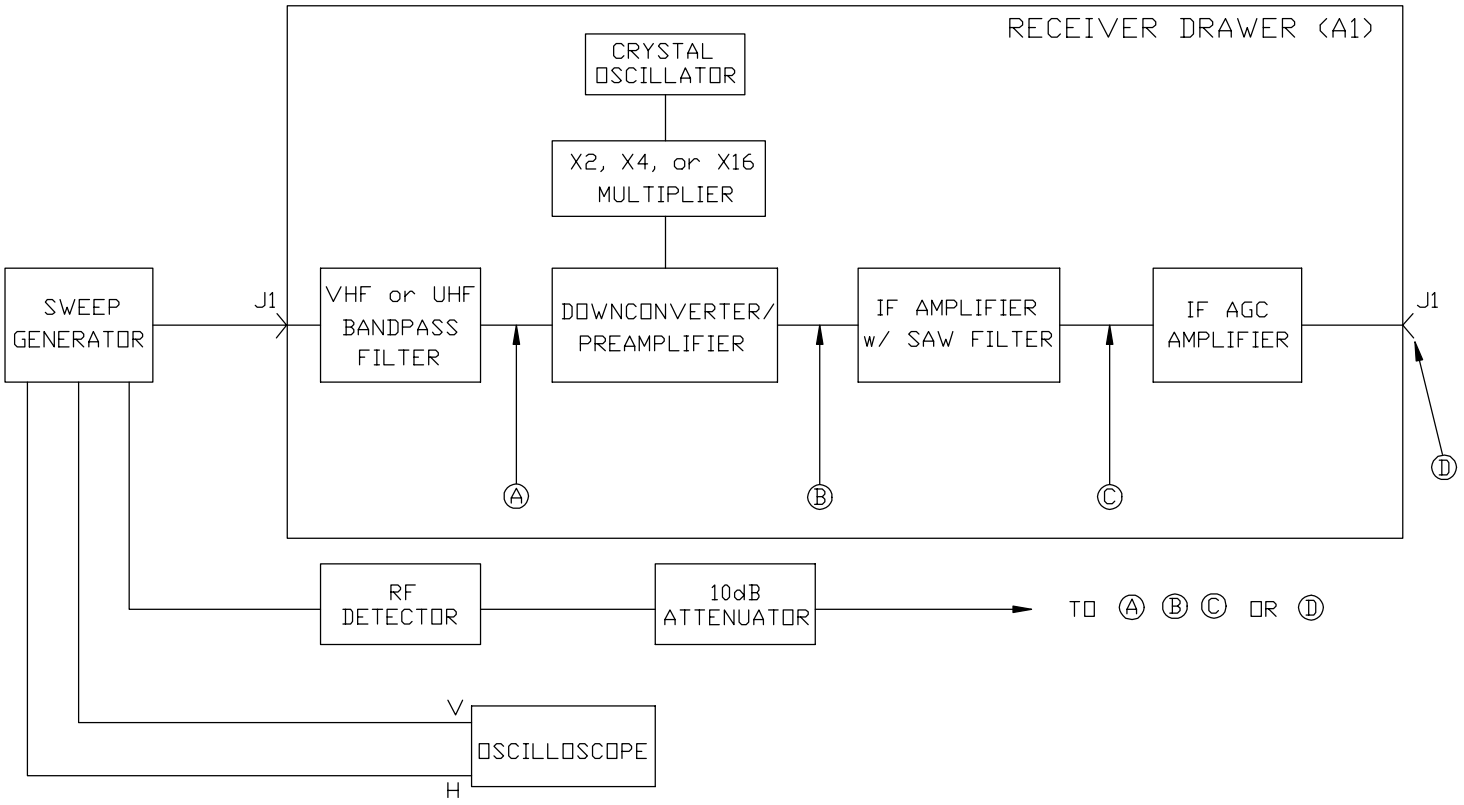
00227



RECEIVER DRAWER LOCAL OSCILLATOR CHAIN ALIGNMENT

FIGURE 3-4

00228



RECEIVER ALIGNMENT

FIGURE 3-5

00003
12-18-89

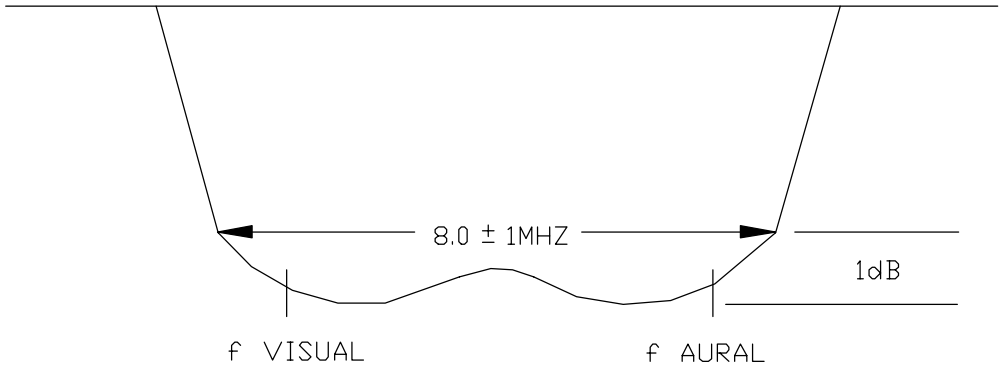


FIGURE 3-6A

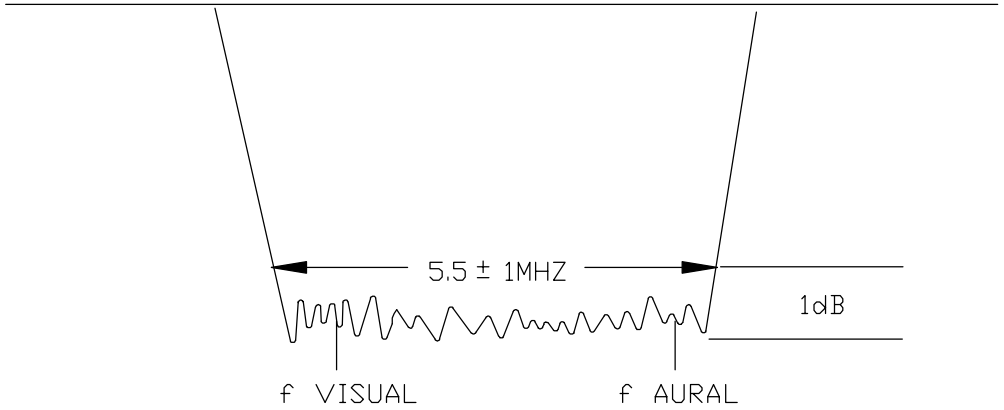
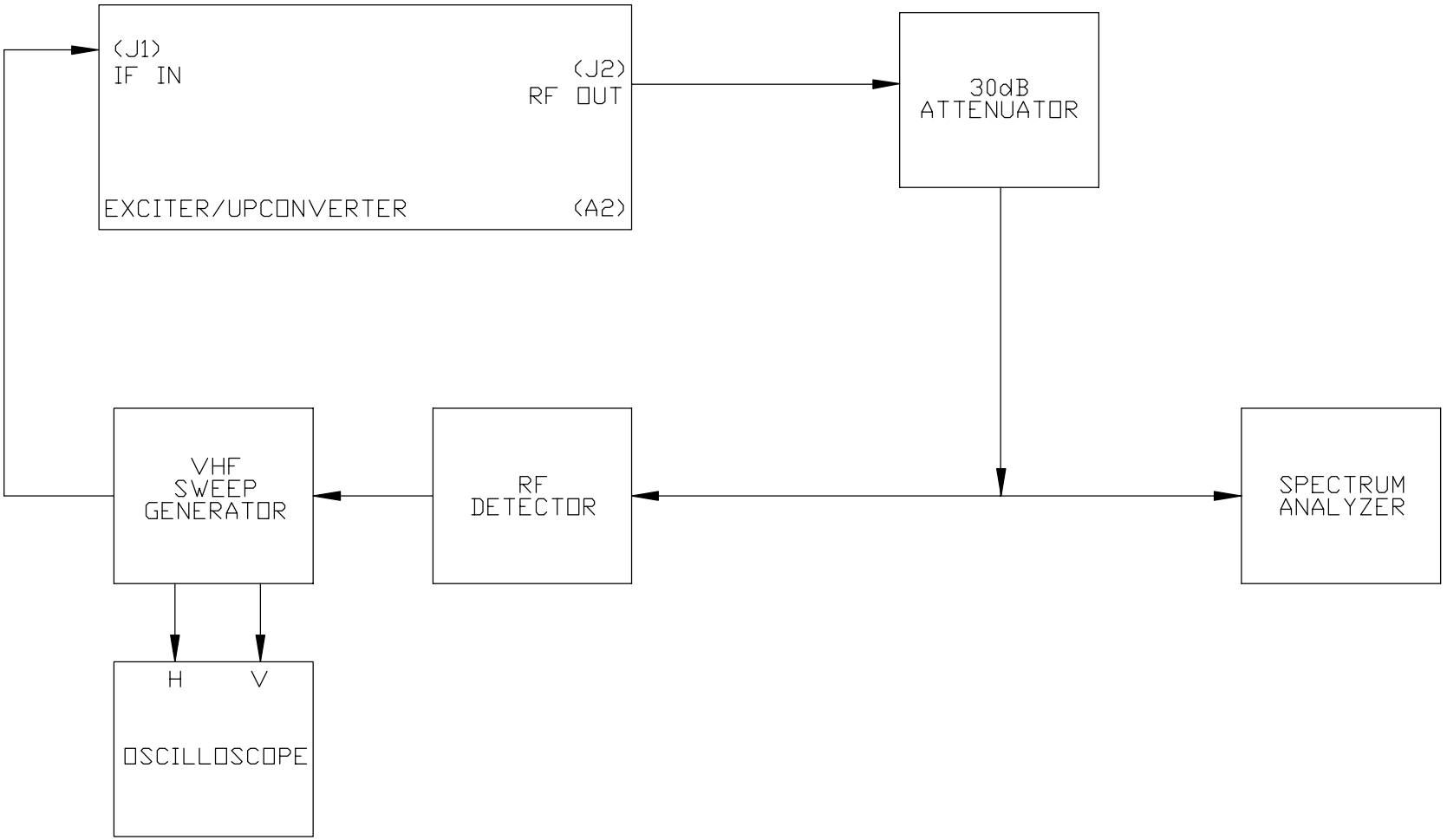


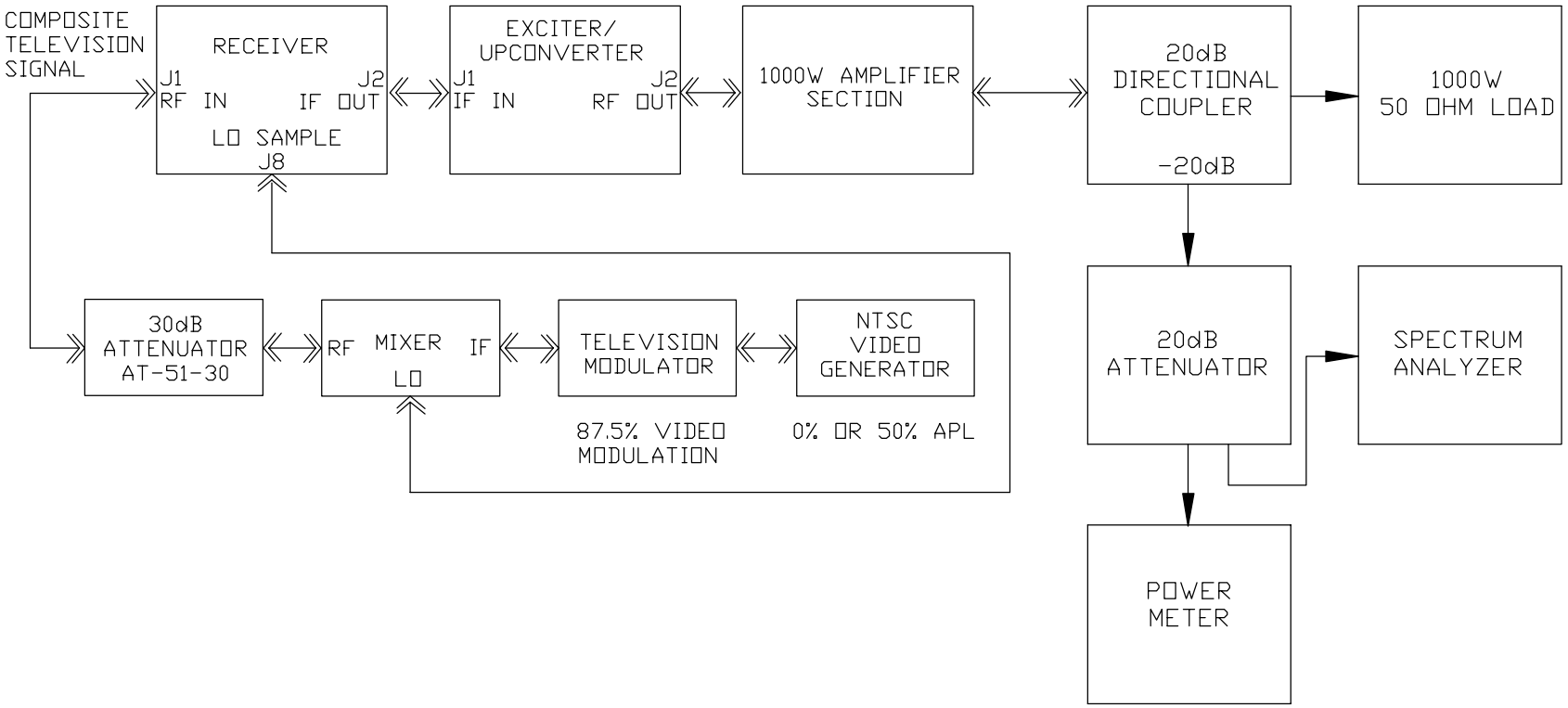
FIGURE 3-6B



ALIGNMENT OF RF AMPLIFIER CHAIN

FIGURE 3-7

00302



TU1000F TRANSLATOR OUTPUT POWER CALIBRATION TEST EQUIPMENT SETUP

FIGURE 3-8

00303

3.9 Spare Modules and Components:

The following contains the description, vendor, part number, and designator of each module found in the TU1000F V/U Translator which EMCEE considers to be essential bench-stock items. These modules should be available to the technician at all times.

TU1000F V/U
INTERCONNECTION DIAGRAM 40386002

DESCRIPTION	VENDOR/PART #	DESIGNATOR
Fans 10" 560CFM 220Vac	EMCEE/4C829	B1, B2
Control Board	EMCEE/40386014-1	A5/PC1
Splitter/Combiner	EMCEE/40367291-1	CP1, CP2
Metering Detector	EMCEE/60386050-1	A5/A7

DUAL 300W UHF AMPLIFIER
INTERCONNECTION DIAGRAM 403860003

DESCRIPTION	VENDOR/PART #	DESIGNATOR
Fans 4.5" 106CFM 220Vac	EMCEE/A30135-10	A3B1, A3B2, A4B1, A4B2
300W UHF Amplifier	EMCEE/40386007-1	A3A1, A3A2, A4A1, A4A2
Status Display	EMCEE/20386107-1	A3PC1, A4PC1
+28V Power Supply	TODD/SPF-750-28	A3PS1, A3PS2, A4PS1, A4PS2

TU20F EXCITER
INTERCONNECTION DIAGRAM 40383113

DESCRIPTION	VENDOR/PART #	DESIGNATOR
Linearizer	EMCEE/60367083-1	A2A6
IF Upconverter	EMCEE/70383030-1	A2A1
2 Watt UHF Amplifier	EMCEE/70367080-1	A2A2
20 Watt UHF Amplifier	EMCEE/80383011-1	A2A3
UHF Synthesizer	EMCEE/60367103-1	A2A4A1
Reference Oscillator	EMCEE/60368055-1	A2A4A2
Metering Detector	EMCEE/60368050-1	A2A5
+28V Power Supply	TODD/SC28-9	A2PS1
±15V/+5V Power Supply	Deltron/W300A	A2PS2
Control Board	EMCEE/80383018-1	A2PC1
Contactor	Telemecanique/LP1-EC03	A2K1
Voltage Regulator	Motorola/MC7812CT	A2U1
Fans 4.5" 106CFM 220Vac	EMCEE/A30135-10	A2B1, A2B2

RECEIVER DRAWER (A1) SPARE MODULES LIST
INTERCONNECTION DIAGRAM 30383094 (OSC/MULT)

DESCRIPTION	VENDOR/PART #	DESIGNATOR
Limiter/Output AGC Control	EMCEE/B331-36-1	PC1
Automatic-On	EMCEE/B331-46-1	PC2
IF AGC Amplifier	EMCEE/B331-42-1	A3
IF Amplifier with SAW Filter	EMCEE/B331-27-1	A2
Downconverter/Preamplifier	EMCEE/B331-47-1	A1
+25V Power Supply	EMCEE/B326-17-1	PS1PC1
±15V, ±5V Power Supply	EMCEE/70326117	PS1PC2
Oscillator	Vectron/CD254D57	G1
***** SELECT APPROPRIATE MULTIPLIER AND FILTER *****		
VHF Bandpass Filter CH 2-6	EMCEE/A280-90-2	FL1
VHF Bandpass Filter CH 7-13	EMCEE/A280-90-1	FL1
UHF Bandpass Filter CH 14-69	EMCEE/ P/LC331-218-1	FL1
X2 Multiplier	EMCEE/B280-76-1	A4
X4 Multiplier	EMCEE/B331-19-1	A4
X16 Multiplier	EMCEE/70367248	A4

RECEIVER DRAWER (A1) SPARE MODULES LIST
INTERCONNECTION DIAGRAM 30383104 (SYNTH)

DESCRIPTION	VENDOR/PART #	DESIGNATOR
Limiter/Output AGC Control	EMCEE/B331-36-1	PC1
Automatic-On	EMCEE/B331-46-1	PC2
IF AGC Amplifier	EMCEE/B331-42-1	A3
IF Amplifier with SAW Filter	EMCEE/B331-27-1	A2
Downconverter/Preamplifier	EMCEE/B331-47-1	A1
+25V Power Supply	EMCEE/B326-17-1	PS1PC1
±15V, ±5V Power Supply	EMCEE/70326117	PS1PC2
Reference Oscillator	EMCEE/60368055-1	A4A2
***** SELECT APPROPRIATE SYNTHESIZER AND FILTER *****		
VHF Bandpass Filter CH 2-6	EMCEE/A280-90-2	FL1
VHF Bandpass Filter CH 7-13	EMCEE/A280-90-1	FL1
UHF Bandpass Filter CH 14-69	EMCEE/ P/LC331-218-1	FL1
VHF Synthesizer High Band	EMCEE/60367103-2	A4A1
VHF Synthesizer Low Band	EMCEE/60367103-3	A4A1
UHF Synthesizer	EMCEE/60367103-1	A4A1