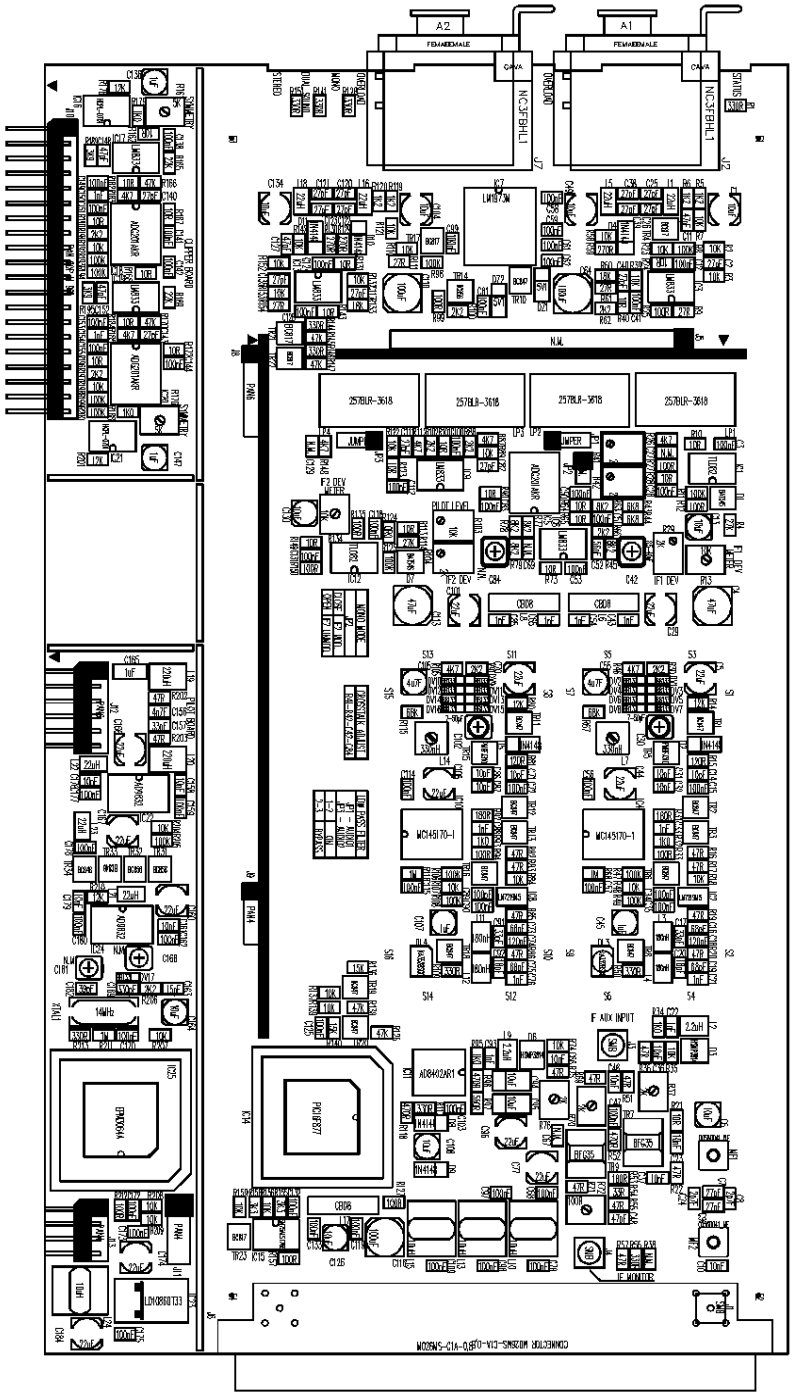
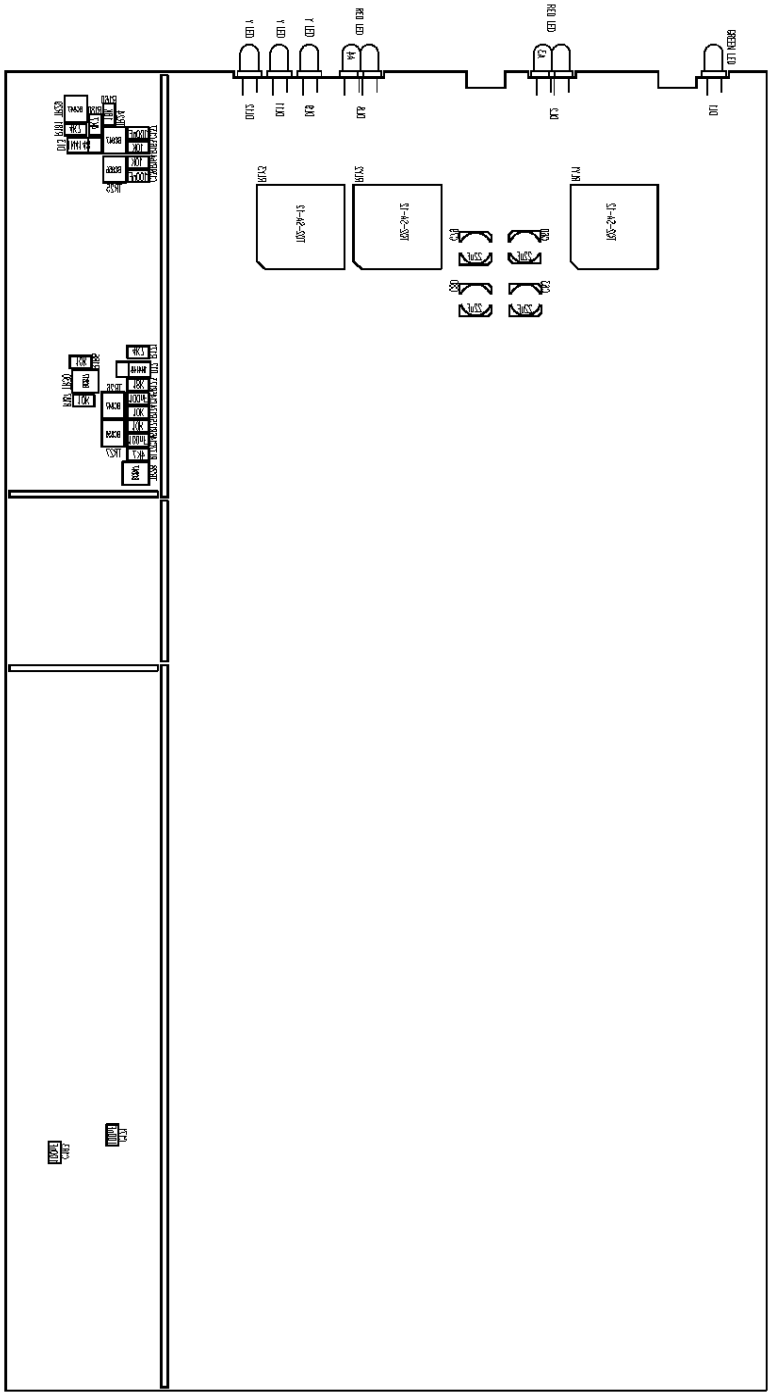
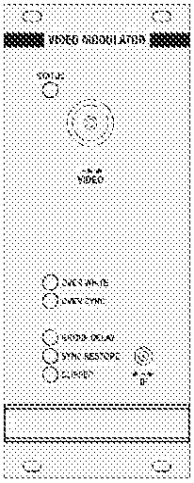
Component layout SCH0210AR1 - Bot layer



Component layout SCH0210AR1 - Top layer





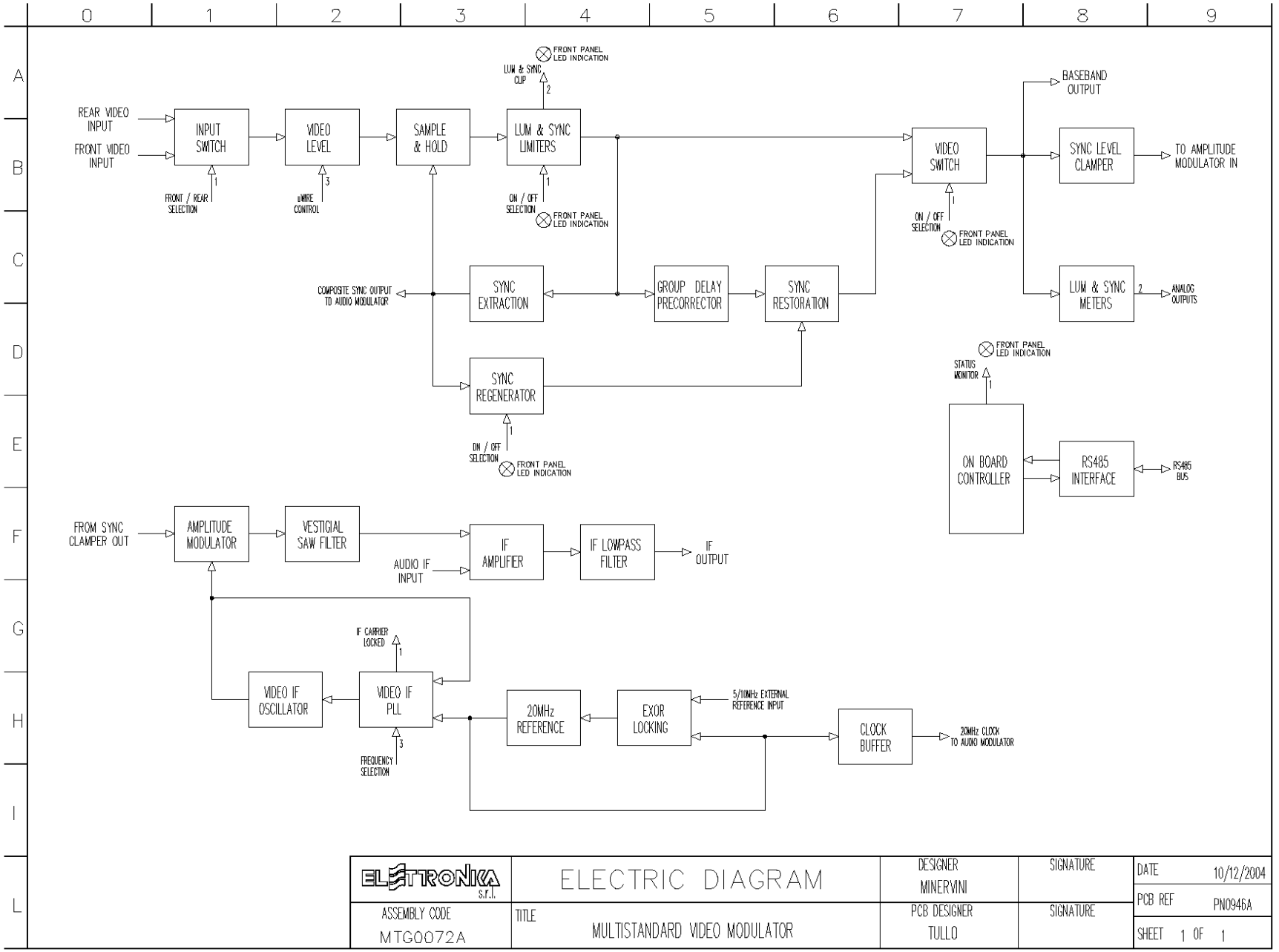
DESCRIPTION

The video signal enters the module trough a 75Ω BNC connection which can be selected via software on either the front or rear panel of the apparatus, and is conditioned to the standard value of 1 Vpp by a digital power-meter with a maximum dynamic of +/-6dB. A sample&hold system allows to set the black level independently from the video information in order to perform clipping operations of the synchronism and luminance levels (which can be disabled via software).
An electronic switch (selectable via software) allows to add the video pre-correction stage, made up by the synchronism regenerator and the video group delay pre-corrector. The former allows to regenerate a normal synchronism level for remarkably degraded video signals, while the latter allows to correct the shape of the audio trap contained in the TV receivers. If the synchronism regenerator is not needed, it can be disabled even if the video pre-correction stage is enabled, but it cannot be used without the latter. The processed video signal modulates the amplitude of the audio carrier generated by an internal local oscillator and controlled by a PLL which locking frequency can be selected via software in accordance with the transmission standard.
The amplitude modulation of the carrier is performed by a Gilbert dell controlled in current to obtain an effective modulation linearity. After this, there are the vestigial filter and an UF gain stage which also sums the audio subcarriers, if any. The whole modulation system is locked to an internal 20MHz reference made up by a VCTCXO, which may in turn be locked to an external 5/10MHz reference present on the control bus, in case the precision offset support is needed.
This 20MHz reference is also used in the audio modulation module in order to obtain the perfect distance between the audio and video carriers even without the external precision reference.

TECHNICAL CHARACTERISTICS

Input impedance	75Ω - ROS>25dB
Nominal level	1Vpp ±6dB
Input	Front and back selectable BNC
Group delay	< 50nsecpp
Frequency response	<±0.5dB
Differential gain	<±1%
Differential phase	<±2°
Luminance non-linearity	<±2%
k-Factor	<1%
Tilt	<1%
ICPM	<2°
S/HUM	>48dB
S/Nunwgt	>60dB
S/Nwgt	>68dB
Clamping	S/H to backporch

Clipper intervention	On synchronism and luminance
Synchronism regenerator	Effective within ±6dB
Group delay pre-corrector	8-celle, excludible
Analog measures	Synchronism and luminance level
Carrier frequency synthesis	PLL
Frequency reference	Internal TCXO externally lockable
External interface	Microprocessor with RS485 protocol
Firmware	Riconfigurabile tramite RS485


0 1 2 3 4 5 6 7 8 9
A B C D E F G H I L
REAR VIDEO INPUT
FRONT VIDEO INPUT
INPUT SWITCH
FRONT / REAR SELECTION
VIDEO LEVEL
uWIRE CONTROL
SAMPLE & HOLD
LUM & SYNC LIMITERS
LUM & SYNC CLIP
ON / OFF SELECTION
FRONT PANEL LED INDICATION
VIDEO SWITCH
ON / OFF SELECTION
FRONT PANEL LED INDICATION
BASEBAND OUTPUT
SYNC LEVEL CLAMPER
TO AMPLITUDE MODULATOR IN
LUM & SYNC METERS
ANALOG OUTPUTS
GROUP DELAY PRECORRECTOR
SYNC RESTORATION
SYNC EXTRACTION
COMPOSITE SYNC OUTPUT TO AUDIO MODULATOR
SYNC REGENERATOR
ON / OFF SELECTION
FRONT PANEL LED INDICATION
ON BOARD CONTROLLER
STATUS MONITOR
FRONT PANEL LED INDICATION
RS485 INTERFACE
RS485 BUS
FROM SYNC CLAMPER OUT
AMPLITUDE MODULATOR
VESTIGIAL SAW FILTER
AUDIO IF INPUT
IF AMPLIFIER
IF LOWPASS FILTER
IF OUTPUT
IF CARRIER LOCKED
VIDEO IF OSCILLATOR
VIDEO IF PLL
FREQUENCY SELECTION
20MHz REFERENCE
EXOR LOCKING
5/10MHz EXTERNAL REFERENCE INPUT
CLOCK BUFFER
20MHz CLOCK TO AUDIO MODULATOR
ELETTRONIKA s.r.l.
ELECTRIC DIAGRAM
DESIGNER MINERVINI
SIGNATURE
DATE 10/12/2004
ASSEMBLY CODE MTG0072A
TITLE MULTISTANDARD VIDEO MODULATOR
PCB DESIGNER TULLO
SIGNATURE
PCB REF PN0946A
SHEET 1 OF 1

The module contains the following blocks:

1. **Input relay** – chooses the video source between the BNC on the front panel of the module and the one on the back of the apparatus; the switching is managed by the software.
2. **Video level regulation stage** – regulates the level of the video signal by means of a digital potentiometer which can be programmed trough a uWIRE interface.
3. **Clamping stage** – uses the timing information of the synchronism extraction stage (see below) to perform the sample & hold of the black level at backporch.
4. **Synchronism and luminance limitation** – clips the synchronism and luminance levels without distorting the crominance signal; the intervention is handled by the software and shown by a yellow LED on the frontal panel, the intervention of the clipper, if any, is shown by two red LEDs (one for synchronism and one for luminance) on the front panel.
5. **Synchronism extraction stage** – extracts from the video signal the synchronism timing to perform the clamping, the regeneration and the lock of the pilot tone of the stereo audio modulator (see MTG0078).
6. **Synchronism regeneration stage** – starting from the timing information extracted by the previous stage, this processes a new synchronism pulse corrected both in level, timing and shape (rising and lowering times); the intervention is handled by the software and signalled by a yellow LED on the frontal panel.
7. **Group delay pre-corrector** – performs the pre-correction of the notch filter on the audio carrier in the demodulator of the receiver in order to equalise its group delay.
8. **Synchronism insertion stage** – 'cuts' the existing synchronism of the video signal and superimposes the regenerated one; due to the need of a delay in the video signal to perform the cut compared to the extraction timing of the synchronism, this stage is related to the insertion of the group delay pre-corrector which inserts this delay.
9. **Video switch** – this stage chooses between the processed video signal (pre-corrected and regenerated in synchronism if needed) and the non-processed one, at this stage there is the monitor for the video base band with 75Ω output with SMB connector on the frontal panel; the choice is handled by the software and signalled by a yellow LED on the front panel.
10. **Video signal level measurement** – this stage detects the peak of the synchronism and luminance levels providing two analog voltages for the A/D conversion; the voltages will be processed by the microcontroller of the display board (see MTG0079) to be displayed as VU-METERS.
11. **Synchronism level clamper** – once all needed processing have been performed with the clamping at black level, a new clamping operation at the synchronism level is made in order to perform the subsequent negative AM modulation.
12. **Amplitude modulator** – converts to the intermediate frequency the video signal referring to the synchronism

peak with a modulation depth of 90% at white level.

13. **Vestigial SAW filter** – filters the double side-band to the broadcast carrier in order to obtain a vestigial modulation (the upper side-band is partially broadcast).
14. **IF Amplifier** – performs the amplification after the vestigial filtering and sums the audio subcarrier(s) coming from the audio modulator module (see MTG0071/78).
15. **Output low pass filter** – filters the presence of harmonics of the audio and video carriers.
16. **IF video oscillator** – generates the video carrier by performing the PLL frequency synthesis; the selectable standards and the lock indication are handled by the software.
17. **Riferimento a 20MHz** – the frequency reference for the PLL synthesis of the video carrier is generated by a TCXO which may be locked to a more precise 5/10MHz external reference (see MTG0076), this reference is buffered and used as reference by the audio modulator (see MTG0071 /78) to synthesise the frequency of the audio carrier so that there are no frequency offsets between the two carriers, even when there is no common external reference.
18. **Controller** – all of the described operations are managed by a microcontroller communicating to the user interface board (see MTG0079) by RS485 protocol; the local controller stores the status of the module and a reprogramming of the firmware (possible via RS485 from the display board) does not alter its contents.

CALIBRATION PROCEDURE

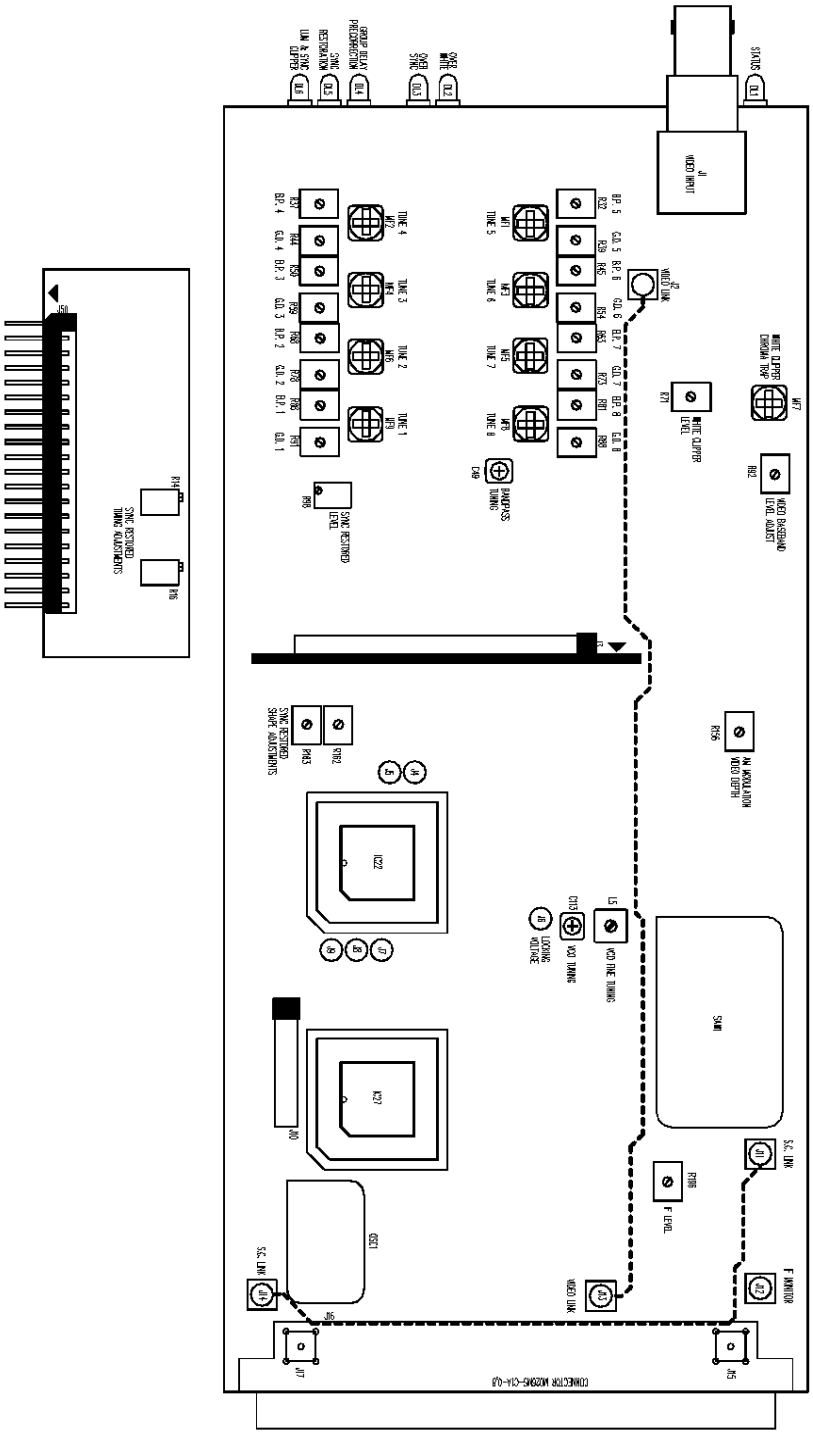
- *Instrument list*

MEASURE	INSTRUMENT
Lock of the carriers and reference	- *Spectrum analyser* - *Oscilloscope* - *Tester*
Calibration of the video parameters in base band and after the AM modulation	- *Video generator with VITS* - *AM Video receiver* - *Video parameters analyser*

- Description of the adjustment points

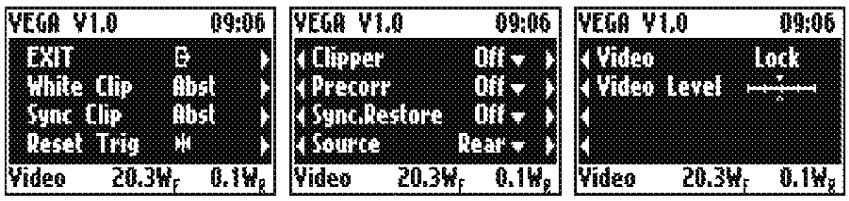
COMPONENT	DESCRIPTION
R71	White clipper level
R92	Level of the video signal in base band (0dB on dig. pot.)
R156	AM modulation depth (90%)
R196	Video carrier level (-6dBm)
R32, R45, R63, R81, R37, R50, R68, R86	Control of the passing band of the pre-corrector cells
R39, R54, R73, R88, R44, R59, R78, R91	Control of the group delay of the pre-corrector cells
R98	Level of the regenerated synchronism
R14, R16	Timing of the cut window of the synchronism
R162, R163	Shape adjustment of the synchronism
C49	Control of the passing band of the pre-corrector
C113	Tuning of the local oscillator of the video carrier
MF1, MF3, MF5, MF8, MF2, MF4, MF6, MF9	Tuning of the group delay pre-corrector cells
MF7	Tuning of the filter on the chrome carrier of the white limiter
L5	Fine tuning of the local oscillator of the video carrier
J4	IF video testpoint (50kHz)
J5	Unused
J6	VCO control voltage testpoint (7...8V)
J7	TCXO testpoint (50kHz)
J8	Unused
J9	External reference testpoint (100kHz)
J1	Video input (panel)
J2-J13	Video link for rear input
J11-J14	IF link for audio carrier input
J12	IF monitor (panel)

Component layout for adjustment points



The calibration procedure of the module requires a complete structure of display board (see MTG0079) and extension module (see MTG0095) in order to perform the software selection which will be referred to later and power the module itself.

- Menu of the Multistandard Video Modulator Module



Verification of the video base-band section – connect a video source with VITS to **J1** and a video parameter measurer to the video base-band output and check the sections included:

- ❑ Configure the module with ***Video Level*** at ½ of the scale, ***Clipper*** *off*, ***Precorr*** *off*, ***Sync.Restore*** *off* and ***Source*** *front.*
- ❑ Calibrate **R92** to obtain the correct levels of synchronism (Fig.1), luminance (Fig.2) and color burst (Fig.3).
- ❑ Increase ***Video Level*** to ¾ of the scale and set ***Clipper*** to *on*, calibrate R71 for the intervention of the white limitation circuit, check that the over LEDs light up and that ***White Clip*** and ***Sync Clip*** are on *Pres*, restore ***Video Level*** to ½ of the scale and check that the LEDs become unlit and that ***White Clip*** and ***Sync Clip*** are on *Trig*, if needed reset this indication by means of ***Reset Trig*** anc check that ***White Clip*** and ***Sync Clip*** are on *Abst.*
- ❑ Configure the module with ***Precorr*** *on* and calibrate **R39**, **R54**, **R73**, **R88**, **R44**, **R59**, **R78** and **R91** to obtain the desired group delay mask, if needed calibrate **R32**, **R45**, **R63**, **R81**, **R37**, **R50**, **R68**, **R86** and **C49** to make the passing band flat; in case this cannot be done in the base band (the video parameters analyser has no group delay mask for the required standard) the calibration of the IF pre-corrector can be made using the AM receiver set with the trap on the audio carrier enabled, equalising the group delay in order to make it flat as in Fig.10 (thus automatically compensating the trap on the audio carrier of the receiver).
- ❑ Configure the module with ***Sync.Restore*** *on* and calibrate **R14** and **R16** for the correct timing of the synchronism pulse (Fig.5) and color burst (Fig.6) and **R98** for the correct level of the synchronism (Fig.1); only if needed, calibrate **R162** and **R163** to equalise the rising and lowering time of the synchronism pulse.

Verification of the IF oscillator section – connect a spectrum analyser on the monitor of the **J12** module and check the sections within:

- ❑ Calibrate **C113** and **L5** to lock the video carrier to the intermediate frequency of the set standard (to change the standard refer to the standard change procedure) and obtain a lock voltage between *7V* and *8V* on **J6** checking that ***Video*** is on *Lock* in the display menu.
- ❑ In case of problems in obtaining the lock, check that on **J4**, **J7** and **J9** there are the frequencies listed in the table of the description of the adjustment points.

Verification of the AM modulation section – connect a video source with VITS to **J1,** a spectrum analyser to the monitor of the **J12** module and an AM video receiver with video parameters analyser to the output of the **J15** module, anc check the sections within:

- ❑ Calibrate **R196** for a level of *–6dBm* of the video carrier and check that the video parameters described in the technical specifications table are obtained (see Fig.1 to Fig.14).

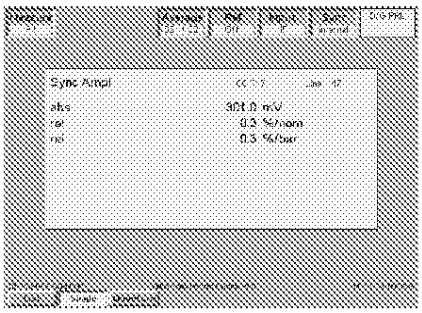


Fig. 1

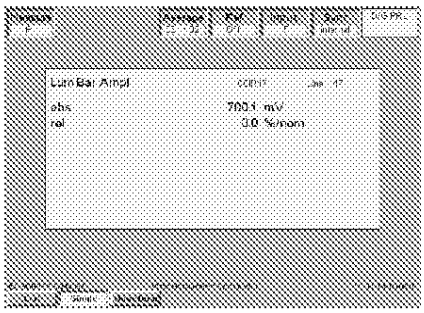


Fig. 2

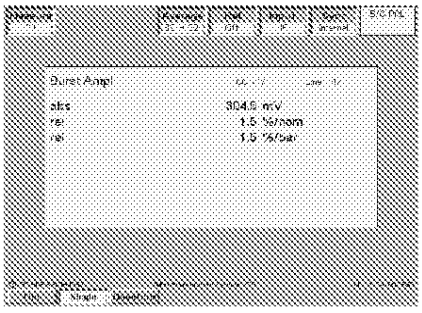


Fig. 3

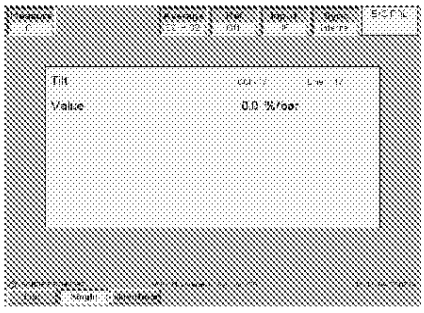


Fig. 4

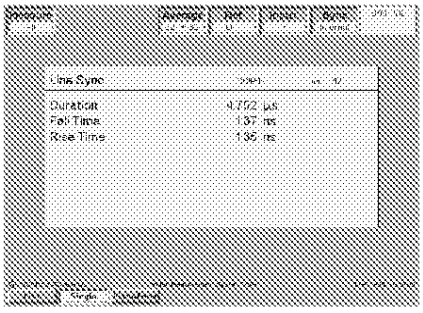


Fig. 5

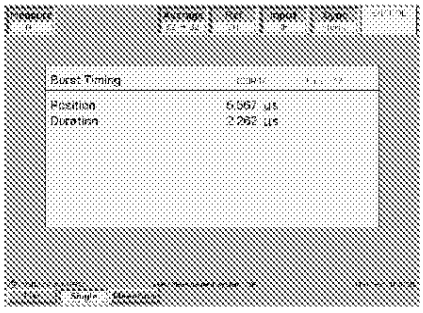


Fig. 6

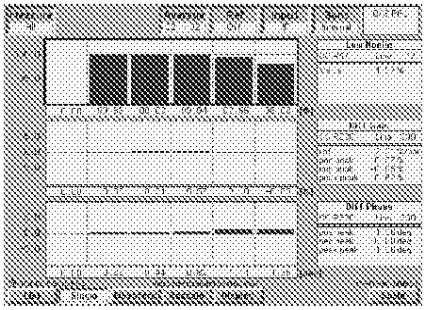


Fig. 7

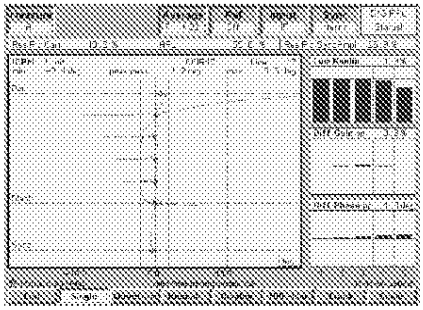


Fig. 8

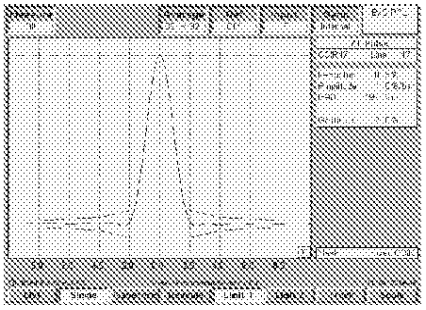


Fig. 9

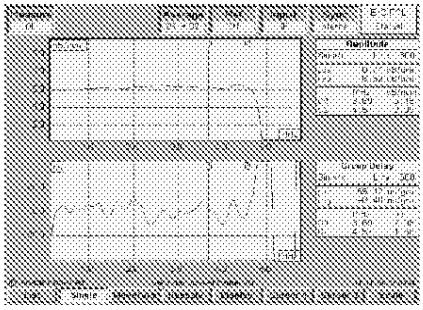


Fig. 10

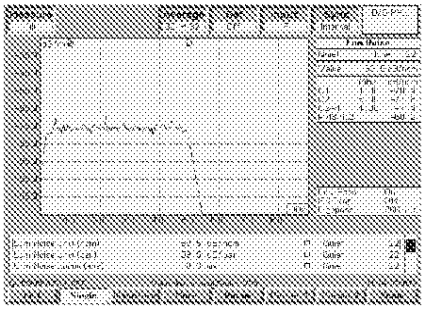


Fig. 11

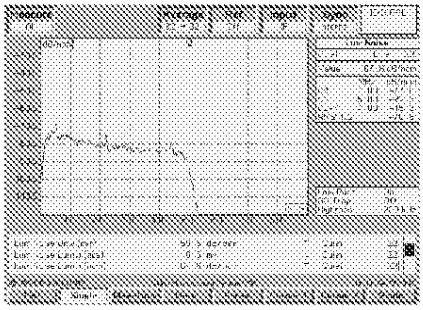


Fig. 12

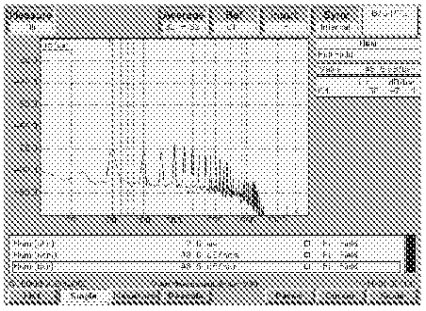


Fig. 13

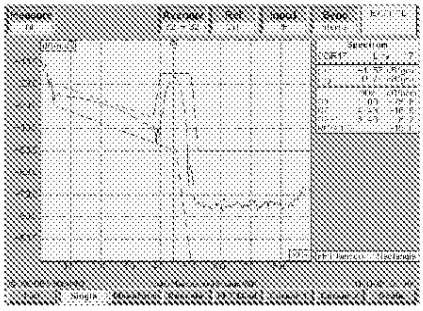
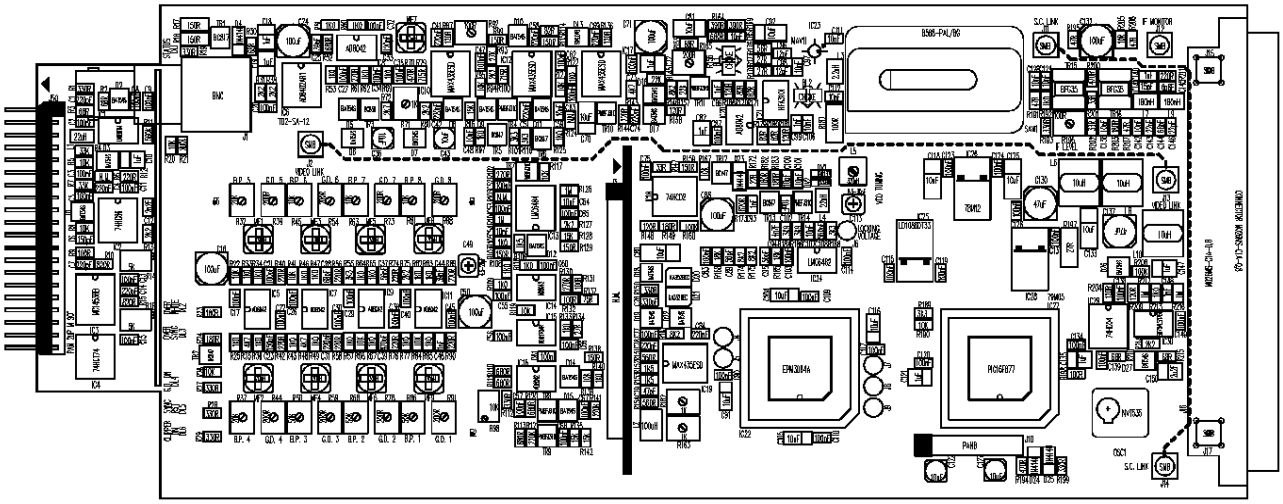
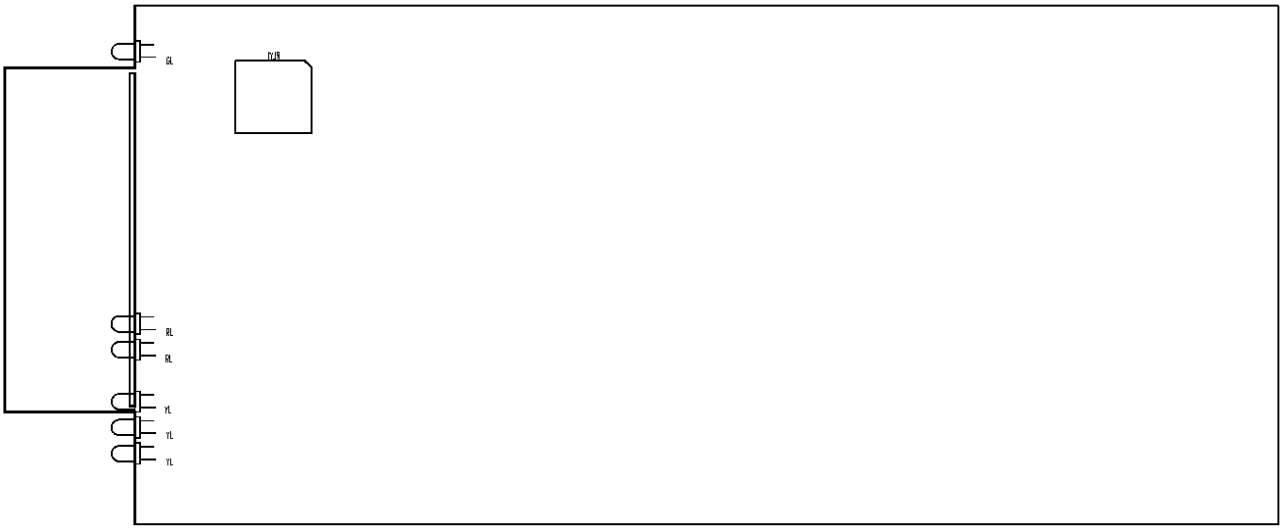


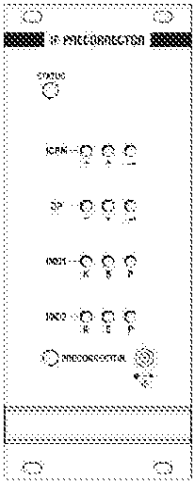
Fig. 14

Component layout SCH0172AR2 - Bot Layer



Component layout SCH0172AR2 - Top Layer



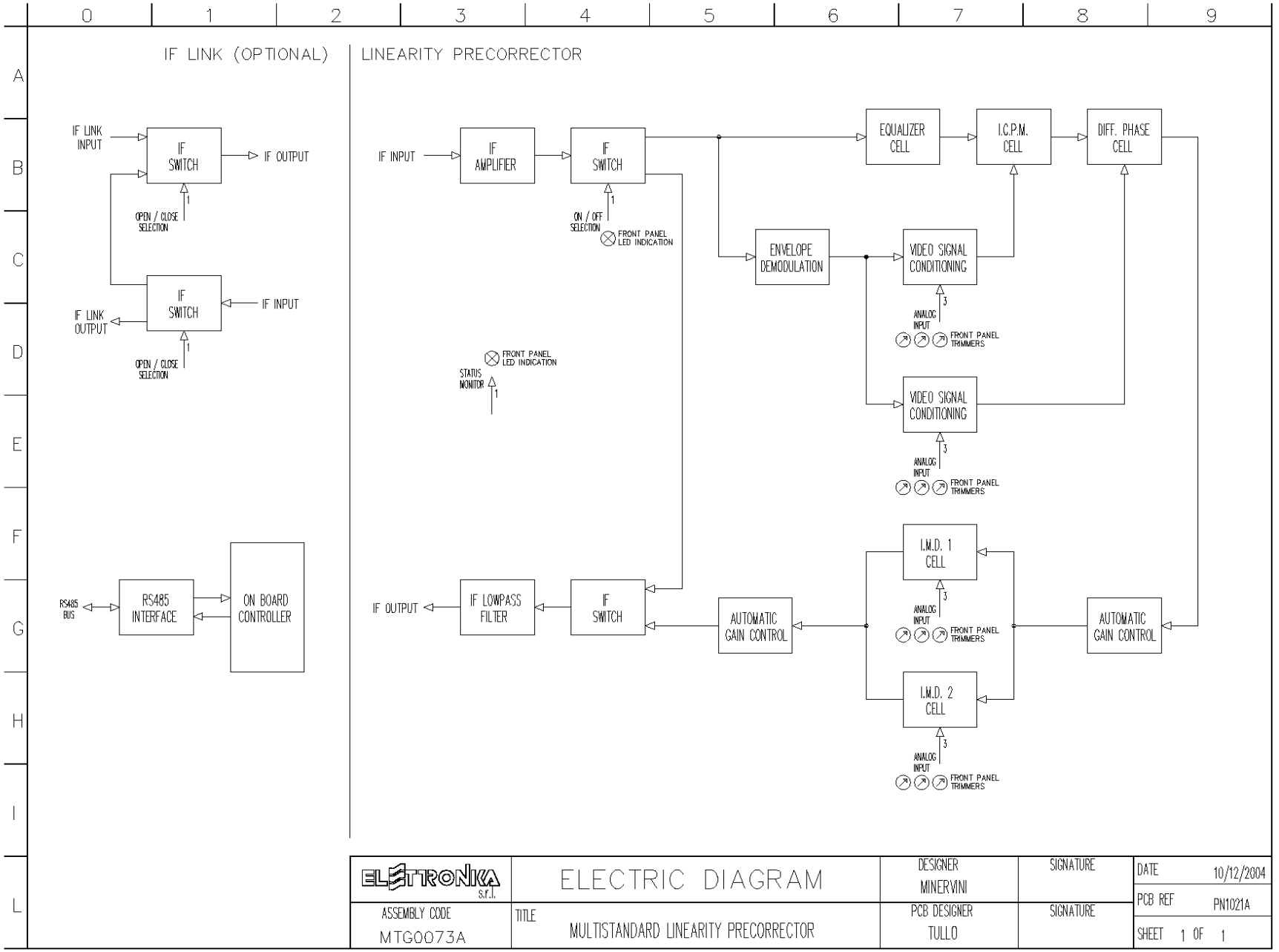


DESCRIPTION

The non-linearity IF pre-correction is performed by two distinct stages which act on different characteristics of the signal. The first stage works on ICPM and differential phase and gain (DGDP) of the video signal, which are small signal characteristics and thus need a pre-correction based on "adapted" filtering cells.
The second stage works on intermodulation, which is a large signal characteristic and needs a pre-correction based on the intervention on non-linear stages.
In consideration of this, the work of the second stage is assured by am automatic gain control system which comes before and after the correction cells, and which is needed to have the system work correctly for each type of pre-correction adopted.
The whole pre-correction stage can be enabled and disabled via software with a switching system which prevents the overshoot at IF-level, dangerous for the final stages.

TECHNICAL CHARACTERISTICS

Input impedance	50Ω - ROS > 25dB
Output impedance	50Ω - ROS > 25dB
Nominal level	-6dBm
Group delay	< 10nsecpp
Frequency response	<±0.2dB
I.C.P.M. pre-correction	3 cells: (-) (+) (level)
D.P. pre-correction	3 cells: (-) (+) (level)
IMD1 pre-correction	3 cells: (knee) (slope) (phase)
IMD2 pre-correction	3 cells: (knee) (slope) (phase)
Video signal for ICPM and DP	Internal envelopment demodulator
Automatic gain control	Before and after the IMD1 cells, 2
Pre-correction	Excludible via software
Pre-corrector intervention	Can be enabled even when powered, without overshoot
Analog measures	—



ELETTRONIKA S.r.l.	ELECTRIC DIAGRAM	DESIGNER MINERVINI	SIGNATURE	DATE 10/12/2004
ASSEMBLY CODE MTG0073A	TITLE MULTISTANDARD LINEARITY PRECORRECTOR	PCB DESIGNER TULLO	SIGNATURE	PCB REF PN1021A
				SHEET 1 OF 1

The module contains the following blocks:

1. **Input amplifier** – de-couples the input of the module from the internal pre-correction sections.
2. **Input/output relay** – inserts or excludes the pre-corrector from the IF chain with the timing needed to avoid power overshoot due to the internal AGC stages; the switch is handled by the software and signalled by a yellow LED on the frontal panel.
3. **Envelopment demodulation stage** – extracts the video information from the AM modulation in order to process the interventions on the pre-correction of ICPM and DP.
4. **Conditioning stages of the video signal (2)** – these use the information extracted by the demodulator and process it by inserting some deformation stages of the video signal which parameters (lower cut, upper cut and level) depend on the controls on the frontal panel.
5. **Equalisation cell** – equalises the passing band of the IF pre-corrector by inserting a band-pass filter cell between the ICPM (set on the video carrier) and DP (set on the audio carrier) pre-correction cells.
6. **ICPM pre-correction cell** – performs the intervention set by the ICPM conditioning stage on the band-pass filter cell set on the video carrier.
7. **DP pre-correction cell** – performs the intervention set by the DP conditioning stage on the band-pass filter cell set on the audio carrier.
8. **Automatic gain control stage (in)** – performs the gain control on the IF signal in order to have the IMD pre-correction cells always work on the optimal point.
9. **Intermodulation pre-correction cells (2)** – pre-correct the three-tones intermodulation by inserting two non-linearity stages which parameters (knee, slope and phase) depend on the controls on the frontal panel.
10. **Automatic gain control stage (out)** – performs the gain control on the IF signal in order to obtain an output signal which level does not depend on the inserted pre-correction.
11. **Output low-pass filter** – filters the presence of harmonics inserted by the linearity pre-corrector.

CALIBRATION PROCEDUE

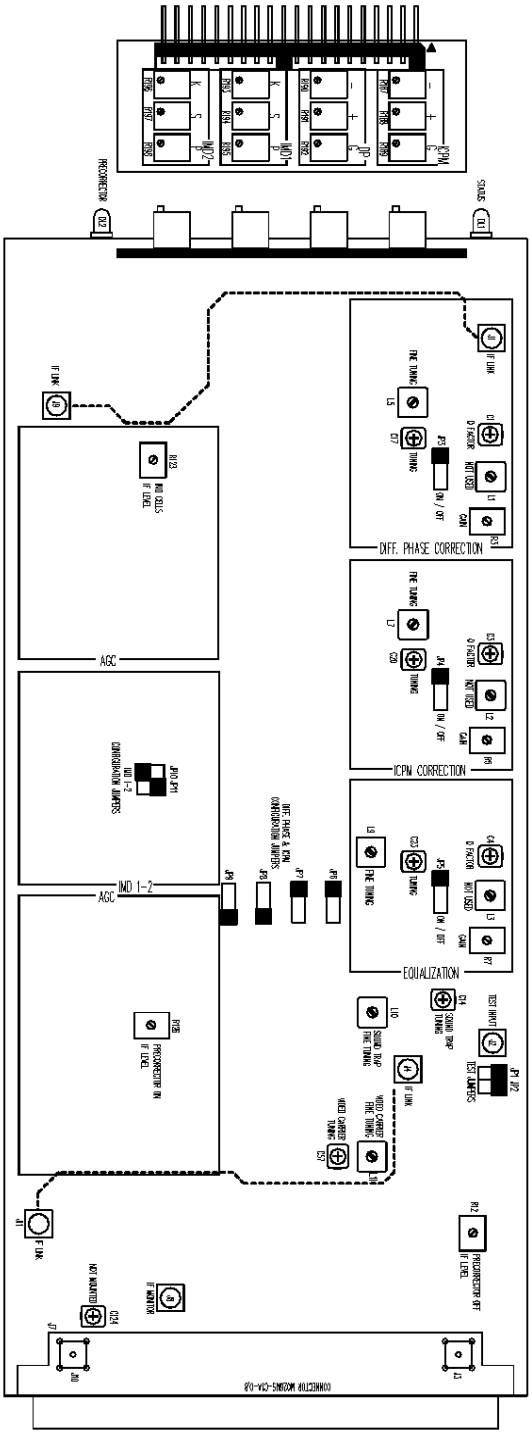
- List of instruments

MEASURE	INSTRUMENT
Calibration of the pre-correction cells and envelopment demodulator	*- Spectrum analyser with tracking* *- Oscilloscope*
Calibration of the video parameters after the pre-correction	*- Video generator with VITS* *- AM Video receiver* *- Video parameters analyser*

- Description of the adjustment points

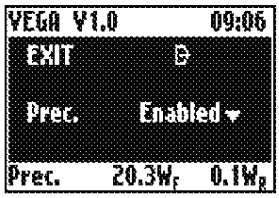
COMPONENT	DESCRIPTION
R12	IF level without pre-correction (-6dBm)
R123	IF level before the IMD pre-corrector (0dBm)
R126	IF level after the IMD pre-corrector (-6dBm)
C57, L11	Band-pass filter on the video carrier of the envelopment demodulator
C14, L10	Notch filter on the audio carrier of the envelopment demodulator
C23, L9	Tuning of the equalisation band-pass filter
R7, C4	Merit and gain factor of the equalisation band-pass filter
C20, L7	Tuning of the ICPM band-pass filter
R5, C3	Merit and gain factor of the ICPM band-pass filter
C17, L5	Tuning of the DP band-pass filter
R3, C1	Merit and gain factor of the DP band-pass filter
L1, L2, L3	Need no calibration
R187, R188, R189	Calibration of the ICPM parameters
R190, R191, R192	Calibration of the DP parameters
R193, R194, R195	Calibration of the IMD1 parameters
R196, R197, R198	Calibration of the IMD2 parameters
JP1, JP2	Jumpers to calibrate the IF filter concerning the ICPM and DP cells
J2	IF input of the filter concerning the ICPM and DP cells
JP3, JP4, JP5	Jumpers to esclude the cells of the ICPM and DP IF filters
J1, J9	IF link (J1 is also the output of the ICPM and DP filter)
JP10, JP11	Configuration jumpers of the IMD cells (do not use)
J4, J11	IF link
J8	IF monitor (panel)
JP6, JP9	Configuration jumpers of the intervention of the DP pre-correction
JP7, JP8	Configuration jumpers of the intervention of the ICPM pre-correction

Component layout for adjustment points



The calibration procedure of the module requires a complete structure of display board (see MTG0079) and extension module (see MTG0095) in order to perform the software selection which will be referred to later and power the module itself. Besides a video modulator module (see MTG0072) and an audio modulator module (see MTG0071/78) already calibrated are needed to calibrate, if neededm the envelopment demodulator (only for the first calibration or to change the standard).

- Menu of the Multistandard IF Precorrector Module



Verification of the ICPM and DP pre-correction section – connect a spectrum analyser with tracking between **J2** and **J1** and check the sections therein:

- ❑ Calibrate **C20** and **L7** to tune the cell of I.C.P.M. to the frequency of the video carrier summing about *750kHz* (Fig.1) with **JP4** *on* and **JP3** and **JP5** *off*.
- ❑ Calibrate **C17** and **L5** to tune the cell of D.P. to the frequency of the audio carrier subtracting about *750kHz* (Fig.2) with **JP3** *on* and **JP4** and **JP5** *off*.
- ❑ Calibrate **C23, L9** to tune the equalisation cell to the middle of the intermediate frequency (Fig.3) with **JP5** *on* and **JP3** and **JP4** *off*.
- ❑ Set **JP3, JP4** and **JP5** *on* and check the response of the filter curve (Fig.4) to the desired passing band, if needed retouch **R3, R5** and **R7** to correct the ripple in band and **C1, C3** and **C4** to equalise the group delay of the filter obtaining a frequency response as in Fig.5.

Verification of the envelopment demodulator section – connect the module to the frame provided with video modulator by means of the extension board and check the sections therein:

- ❑ Calibrate **C57** and **L11** to obtain the best demodulation of the video signal by connecting an oscilloscope to **C44** (only if changing the IF standard).
- ❑ Calibrate **C14** and **L10** to obtain the best attenuation of the audio signal superimposed to the video signal connecting an oscilloscope to **C44** (only if changing the IF standard and with at least one audio module in the frame).

Verification of the IMD1, 2 pre-correction sections – connect a spectrum analyser with tracking between **J9** and **J10** and check the sections therein:

- ❑ Configure the module with ***Prec*** *enabled.*
- ❑ Calibrate **R123** to an IF level of *0dBm* on **R178** and calibrate **R126** to an IF level of *-6dBm* on **J10** with the tracking on *-6dBm.*
- ❑ Check that the passing band of the section is similar as the one in Fig.6 and able to cover the whole IF band from *30MHz* to *50MHz.*

Verification of the module without pre-correction – connect a spectrum analyser with tracking between **J3** and **J10** and check the sections therein:

- ❑ Configure the module with ***Prec*** *disabled.*
- ❑ Calibrate **R12** to an IF level of *-6dBm* on **J10** with the tracking on *-6dBm.*
- ❑ Check that the passing band of the section is flat within *0.2dB* on the whole IF from *30MHz* to *50MHz.*

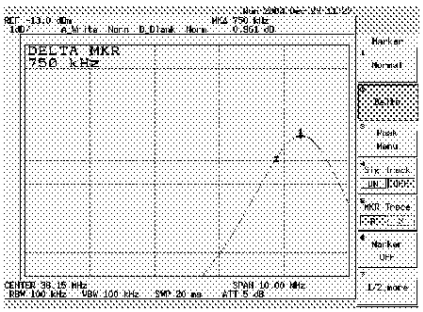


Fig. 1

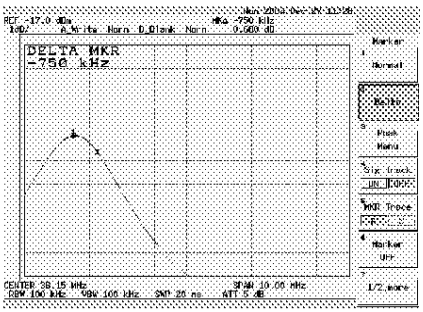


Fig. 2

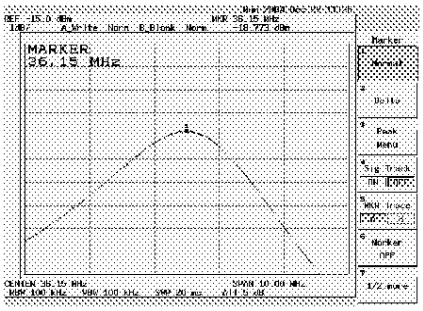


Fig. 3

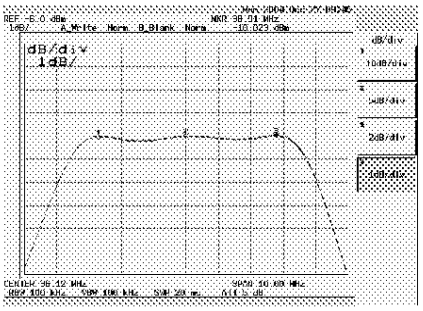


Fig. 4

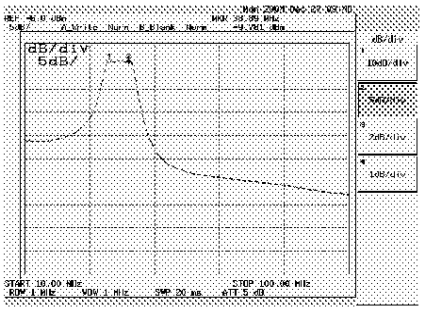


Fig. 5

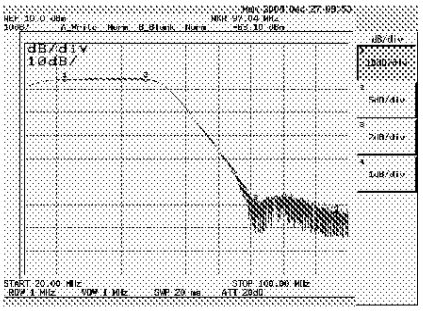
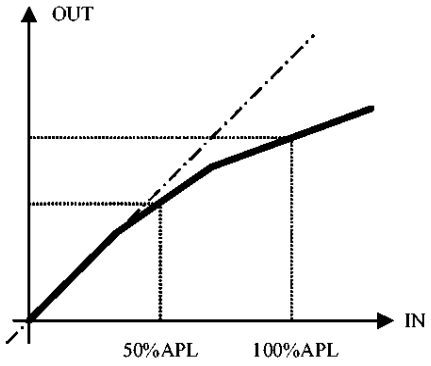


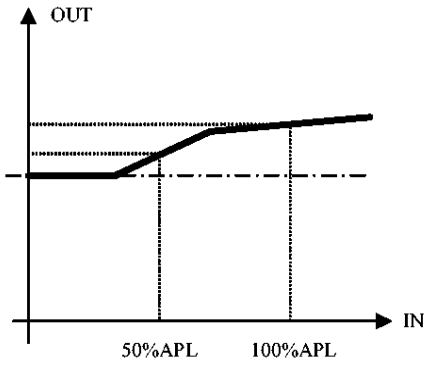
Fig. 6

The testing procedure of the linearity pre-corrector is the consequence of a series of subsequent interventions on the pre-corrector cells in order to achieve a good compromise of the video parameters of the amplifier at the working power.
A calibration technique for the cells allowing to satisfy these requirements is proposed below; the choice of the good compromise on the video parameters is anyway entrusted to the skill of the tester.

IMD1, 2 pre-correction - the intermodulation pre-correction inserts distortions in the negative Am modulation linear characteristic of the video signal in order to compensate the distortions due to the power amplifier.
These are characterised by three parameters: ***Knee***, ***Slope*** and ***Phase***, and introduce some deviations from the input/output linear characteristic of the pre-corrector.
For a more complete possibility of shaping the non-linearity characteristic, there are two pre-correction cells in two particular regions of the characteristic: **50% APL** (cell 1) and **100% APL** (cell 2).



AM-AM



AM-PM

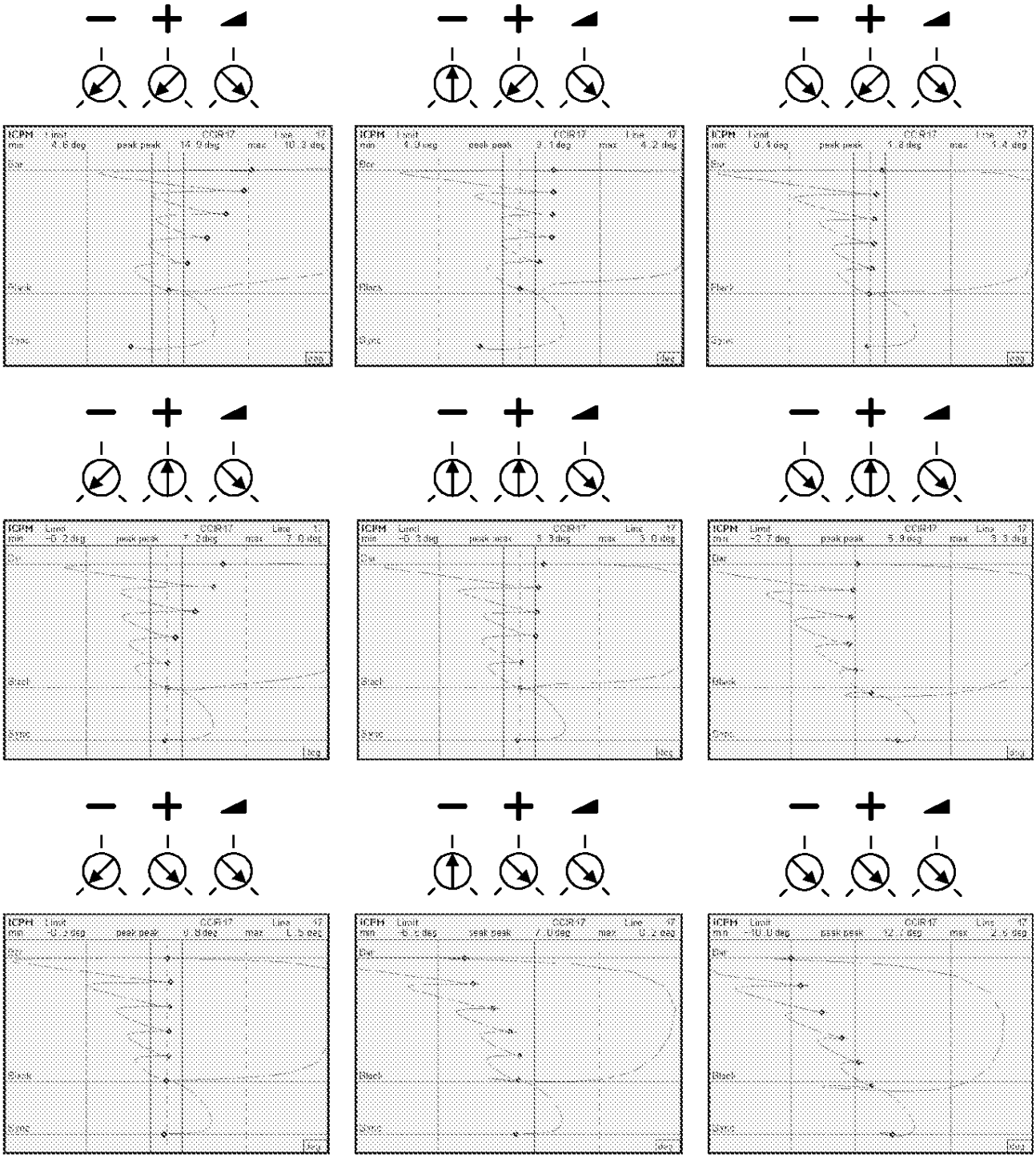
The suggested procedure to compensate the characteristic of the final power stage is to start 'positioning' cell 1 (by acting on the K and S trimmers) in order to find a minimum point for the intermodulation, then 'position' cell 2; retouch the P trimmer if needed to refine the pre-correction.
Usually cell 1 only is needed to pre-correct A-class final stages, while for AB-class ones both cells are needed.
In order to exclude one of the cells (or both at the beginning of the pre-correction procedure) it only takes decreasing the K, S and P trimmers to the minimum.
Perform the pre-correction procedure for the intermodulation with the *red bar* video signal and repeat it for the other colours if needed, refining the pre-correction.

ICPM pre-correction – a catalogue of the different kinds of pre-correction which can be introduced on the ICPM parameter is given below. Once the measure has been taken, the situation which better approximates

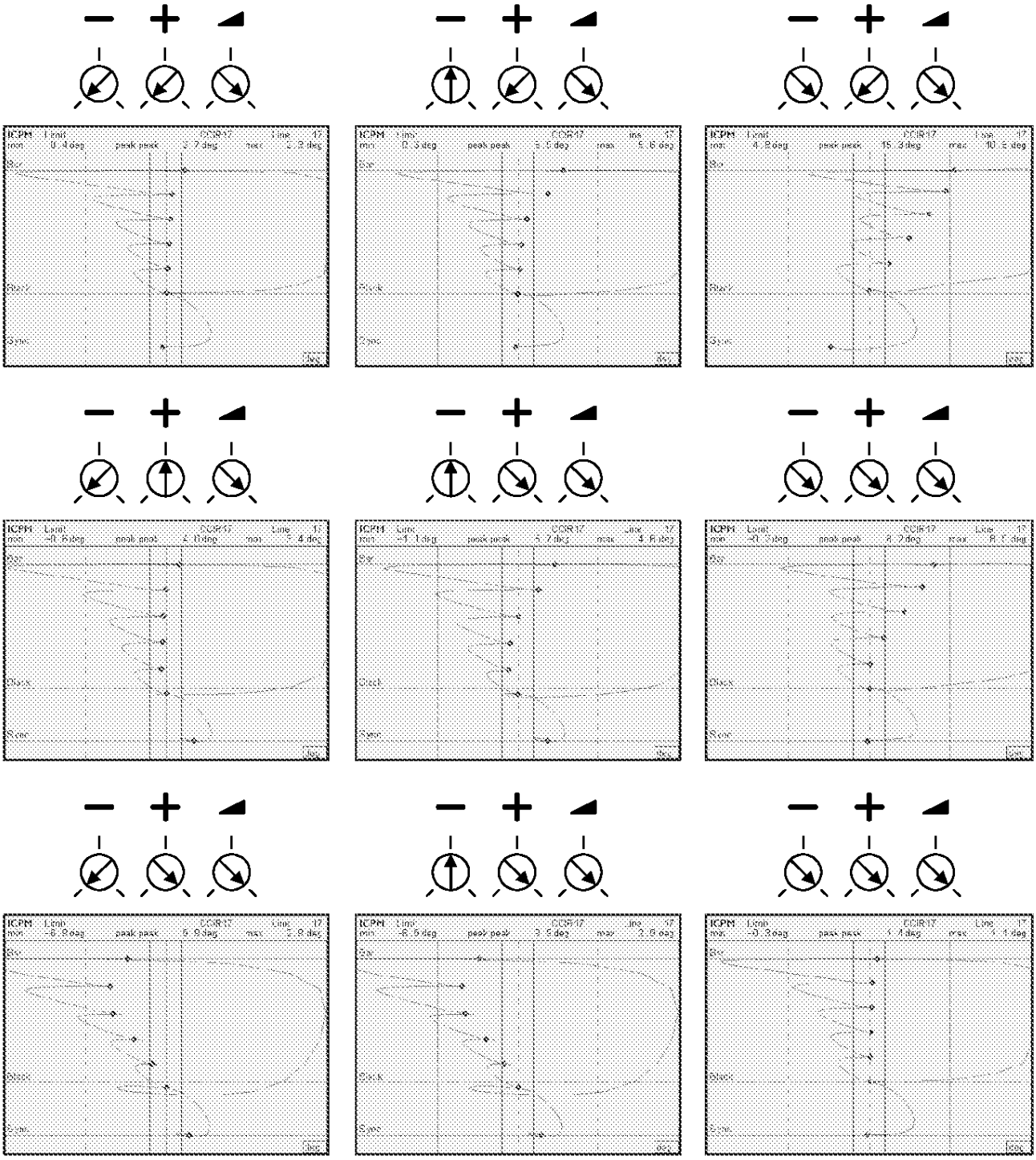
the compensation has to be found, then the figure reproducing the measure **in a 'specular' way** is to be considered.
In the catalogue there are also the positions of the trimmers and the jumpers to obtain all proposed configurations, of course intermediate solutions are possible and the intensity of all solutions may be scaled by means of the level trimmer which is considered to be at the maximum intervention in the catalogue.

DP pre-correction – a catalogue of the different kinds of pre-correction which can be introduced on the DP parameter is given below. Once the measure has been taken, the situation which better approximates the compensation has to be found, then the figure reproducing the measure **in a 'specular' way** is to be considered.
In the catalogue there are also the positions of the trimmers and the jumpers to obtain all proposed configurations, of course intermediate solutions are possible and the intensity of all solutions may be scaled by means of the level trimmer which is considered to be at the maximum intervention in the catalogue.

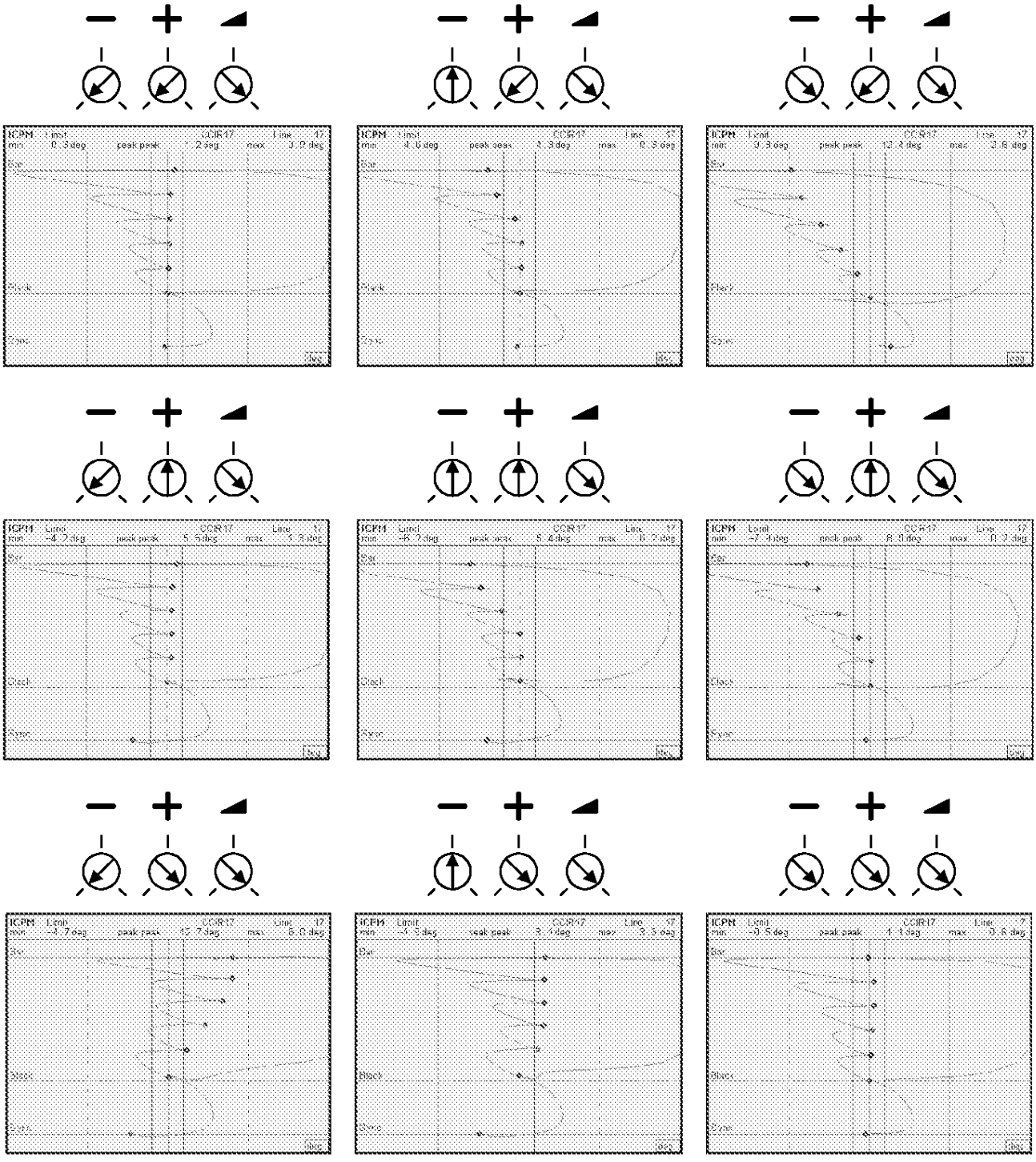
- ***I.C.P.M.*** Pre-correction catalogue with: JP7 → 1-2; JP8 → 1-2



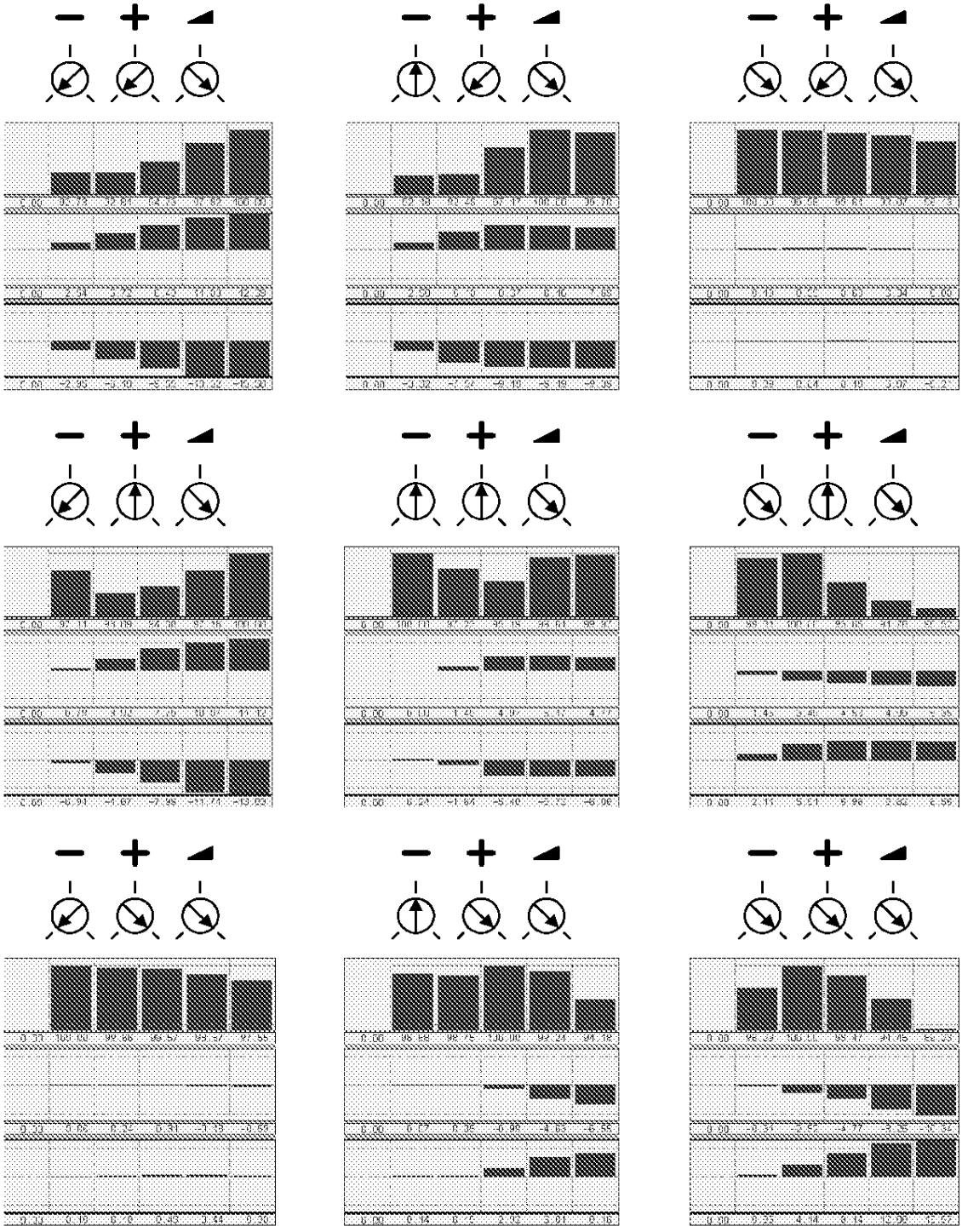
- ***I.C.P.M.*** Pre-correction catalogue with: JP7 → 2-3; JP8 → 1-2



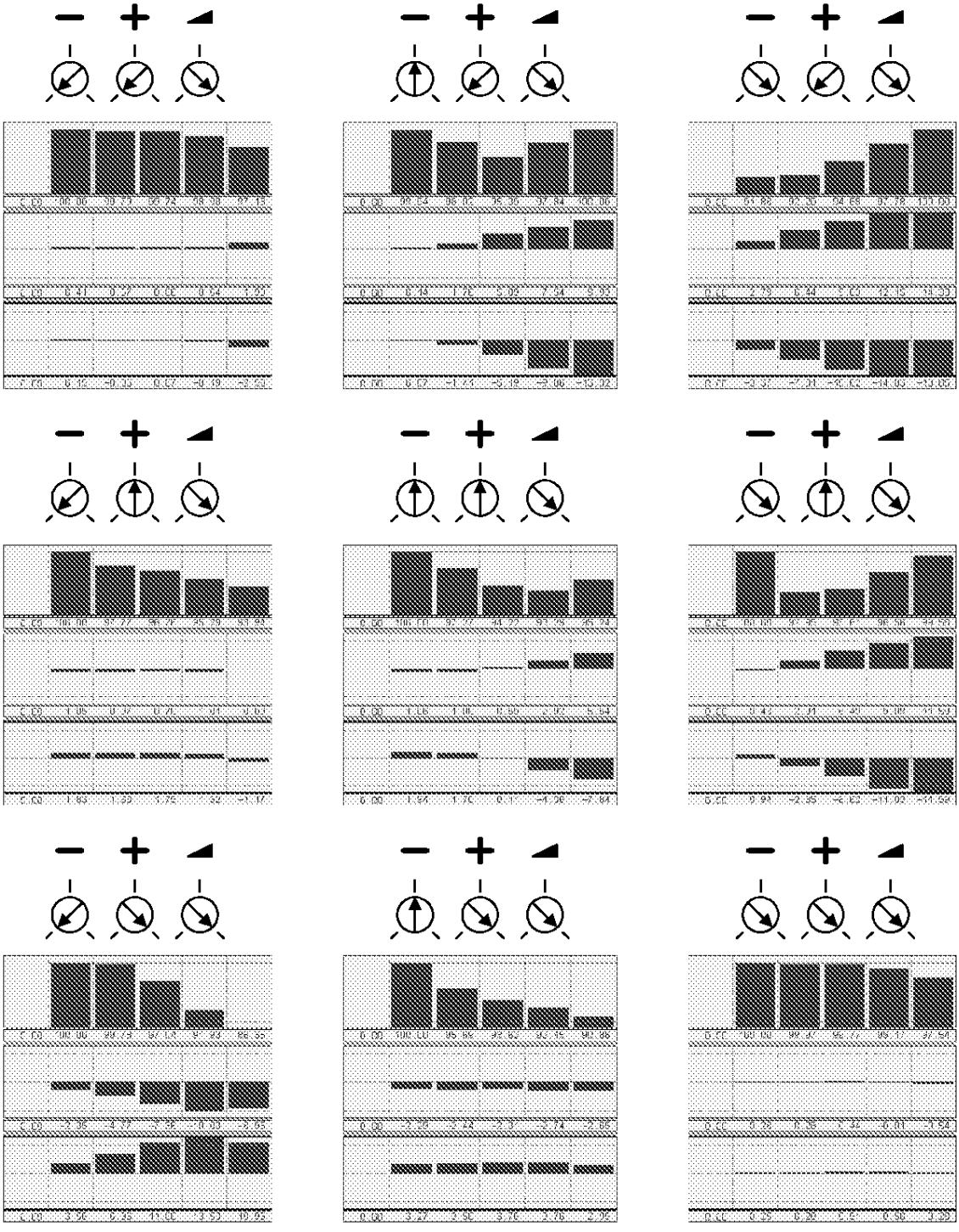
- ***I.C.P.M.*** Pre-correction catalogue with: JP7 → 1-2; JP8 → 2-3



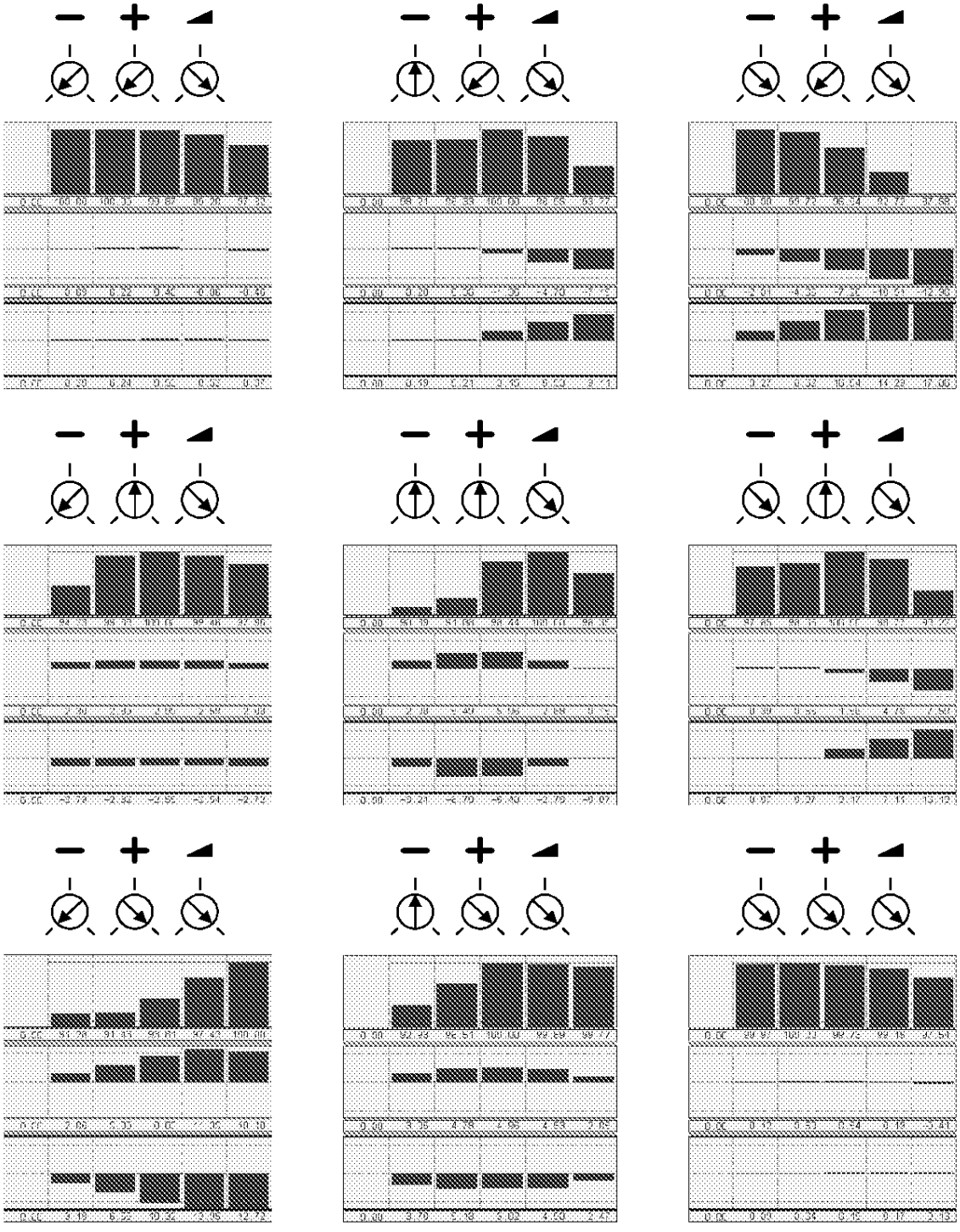
- ***D.P.*** Pre-correction catalogue with: JP6 → 1-2; JP9 → 1-2



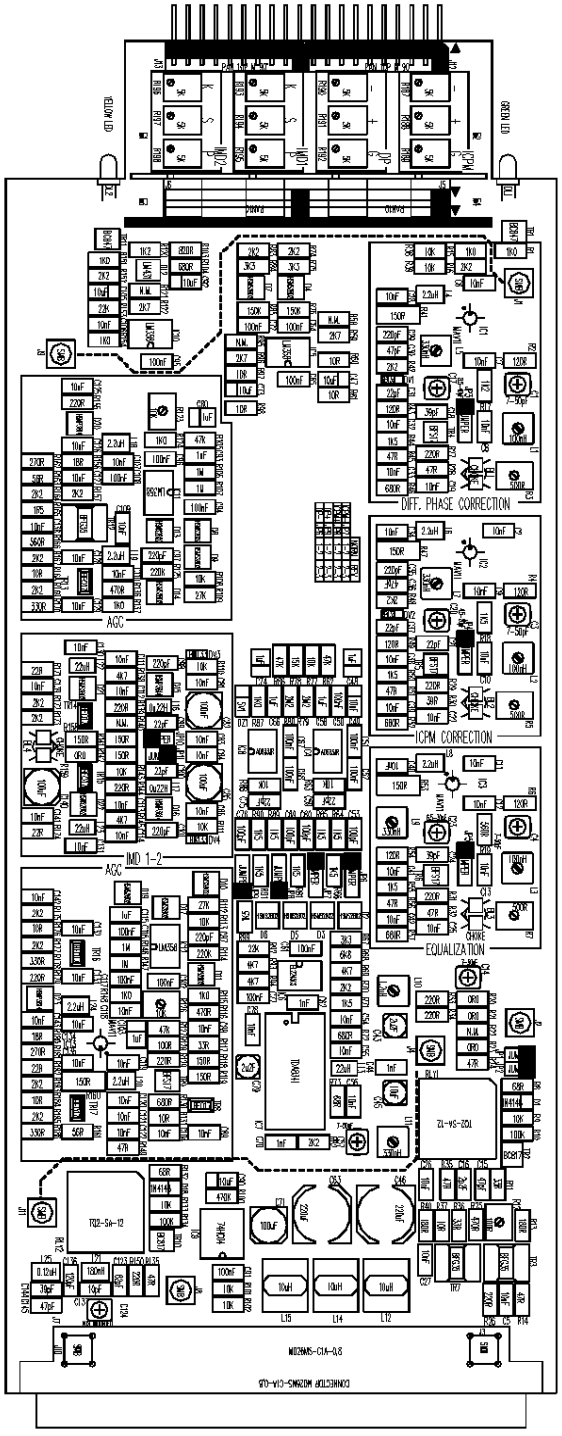
- ***D.P.*** Pre-correction catalogue with: JP6 → 2-3; JP9 → 1-2

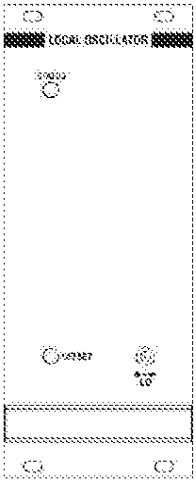


- ***D.P.*** Pre-correction catalogue with: JP6 → 1-2; JP9 → 2-3



Component layout SCH0209AR1



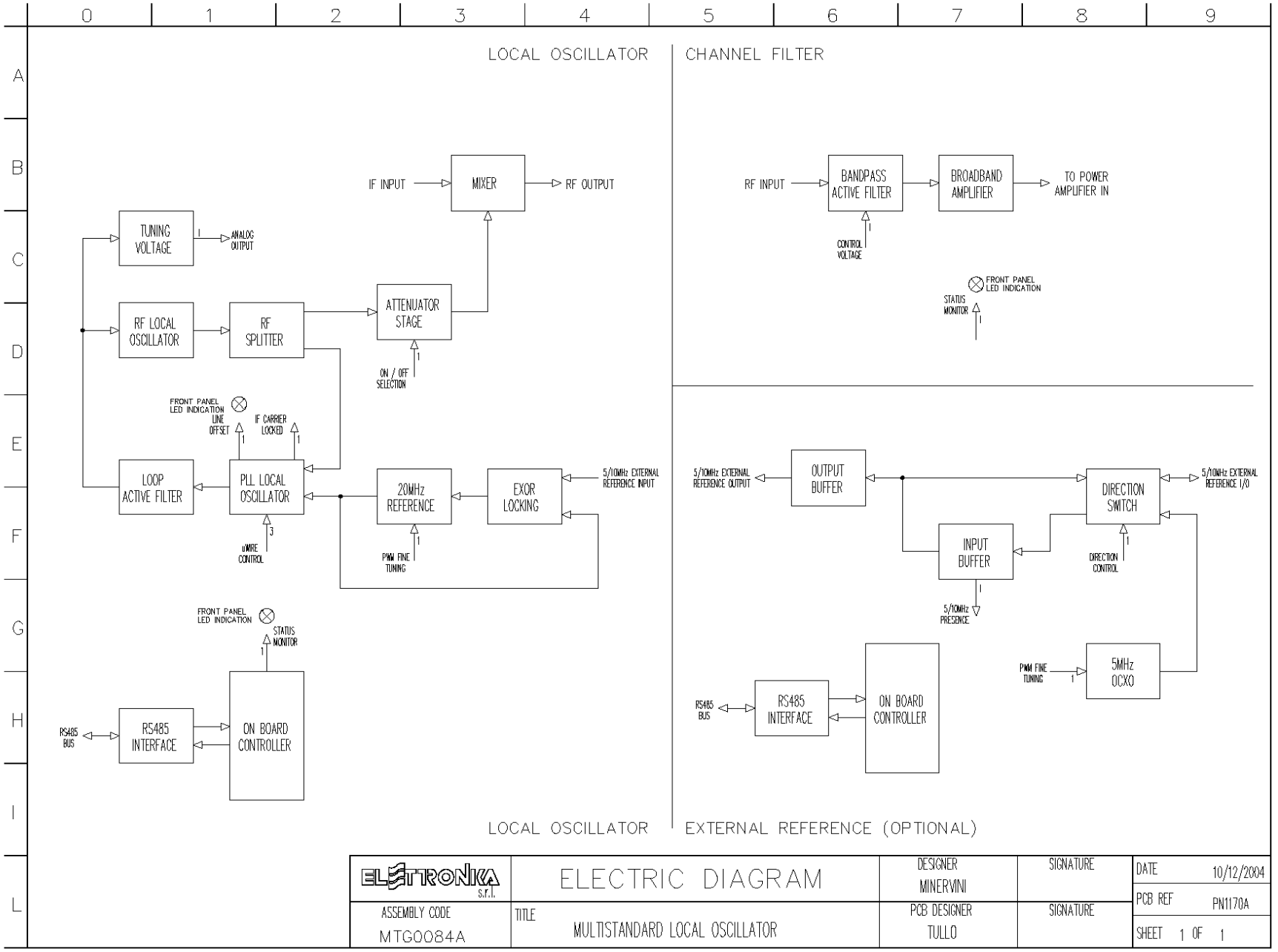


DESCRIPTION

The synthesis system of the local oscillator for the channel conversion is based on a control technique which allows to obtain the programming of the standard, the channel (split into the three bands I, III, IV/V) and the line offset (as multiple of the line frequency of the video signal) via software, with no change to be made.
The module includes an internal VCTCXO reference which can be locked to a more precise 5/10MHz reference (trough the bus) needed if the field offset is used.

TECHNICAL CHARACTERISTICS

Nominal level	+13dBm ±1dB
FM S/N ccir unweight.	>65dB
FM S/N ccir wght.	>60dB
Analog measures	VCO control voltage
Carrier frequency synthesis	A PLL
Offset	Line offset, step ±1/12 line frequency
O.L. carrier characteristics	On/Off selection and fine adjust
Frequency reference	Internal TCXO externally lockable
External interface	Microprocessor with RS485 protocol
Firmware	Re-configurable via RS485



ELETTRONIKA s.r.l.	ELECTRIC DIAGRAM	DESIGNER MINERVINI	SIGNATURE	DATE 10/12/2004
ASSEMBLY CODE MTG0084A	TITLE MULTISTANDARD LOCAL OSCILLATOR	PCB DESIGNER TULLO	SIGNATURE	PCB REF PN1170A
				SHEET 1 OF 1

The module contains the following blocks:

1. **Local oscillator** – generated the carrier to be synthesised, it is split into three windows (I-II / III / IV-V band) to ensure the coverage of all of the TV channels to be implemented for all standards.
2. **Radio-frequency splitter** – splits the signal coming from the local oscillator by means of splitters and amplifiers, with 10dB attenuation and gain respectively, to ensure the complete isolation of the LO from the other stages and to minimise the 'frequency pulling' phenomenon.
3. **PLL stage** – synthesises the desired channel by locking the LO to a 20MHz frequency reference by means of a PLL which can be configured via uWire and provides the locking and line-offset indication (LED on frontal panel); the choice is made via software.
4. **Active ring filter** – stabilises the system in PLL retro-action and e has to be modified if the operating band of the module changes (see table attached to the electrical diagram).
5. **Conditioning stage of the correction voltage** – conditions the correction voltage of the PLL ring providing a conditioned analog voltage for the A/D conversion; the voltage is processed by the microcontroller of the display board (see MTG0079) to be displayed as VU-METER.
6. **Mixer** – in the UPCONVERTER version of the module, converts to channel the intermediate frequency coming from the pre-corrector (see MTG0073) using a LEVEL13 mixer (in case the module is only used as LO, see REPEATER configuration, this stage is not present and the synthesised carrier goes directly to the output of the module).
7. **20MHz reference** – the frequency reference to the PLL synthesis of the carrier is generated by an internal TCXO which fine control of the frequency is internally generated via PWM by the microcontroller or, alternately, can be locked to a more precise 5/10MHz external reference (see MTG0076).
8. **Controller** – all of the described operations are managed by a microcontroller communicating to the user interface board (see MTG0079) by RS485 protocol; the local controller stores the status of the module and a reprogramming of the firmware (possible via RS485 from the display board) does not alter its contents.

CALIBRATION PROCEDURE

- List of instrument

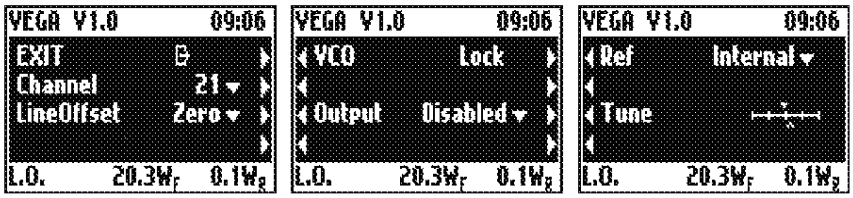
MEASURE	INSTRUMENT
Lock of the carriers and reference	*- Spectrum analyser* *- Oscilloscope* *- Tester*

- Description of the adjustment points

COMPONENT	DESCRIPTION
C1, C2, C3	Tuning of the local oscillator (SCH0292 - 0309 - 0310)
J3	LO input
J5, J8	RF link (absent in case of LO configuration)
J4	LO monitor (panel)
JP1	Unused
J2	Testpoint for the debug of the PLL

The calibration procedure of the module requires a complete structure of display board (see MTG0079) and extension module (see MTG0095) in order to perform the software selection which will be referred to later and power the module itself..

- Menu of the Multistandard UHF Local Oscillator Module



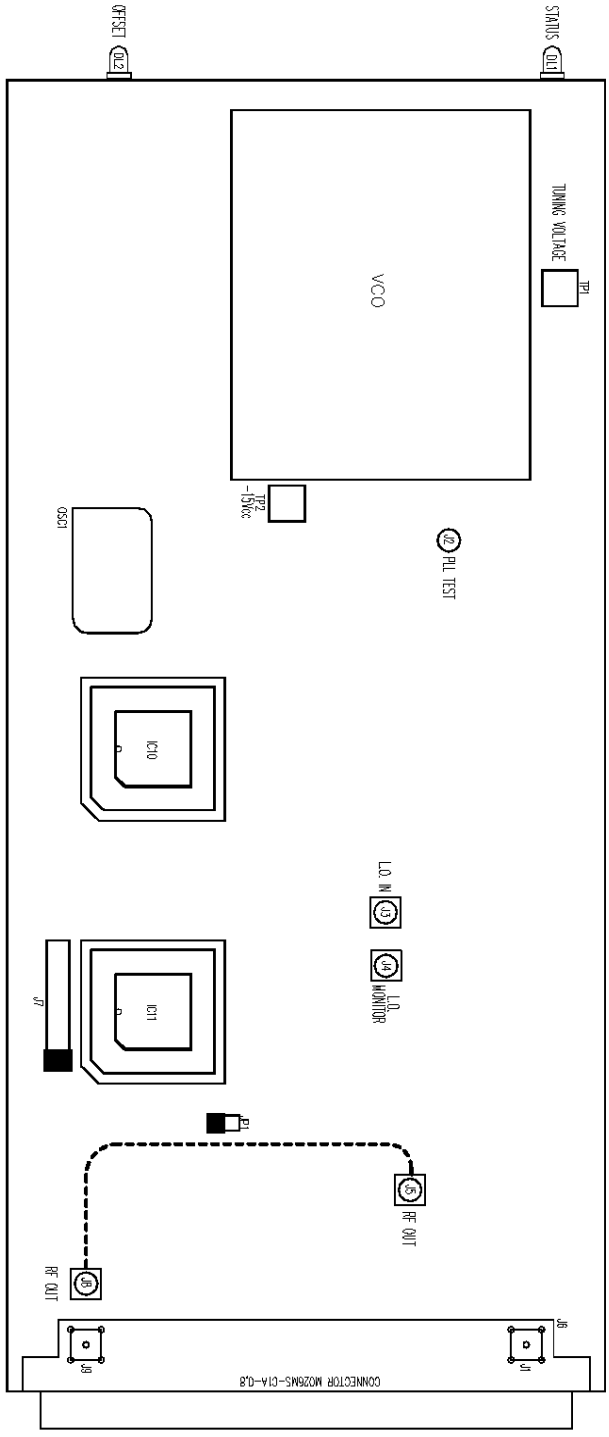
Verification of the local oscillator section – connect a spectrum analyser to the monitor of the **J4** module and check the sections therein:

- ❑ Configure the module with ***Output*** *Enabled*, ***LineOffset*** *Zero*, ***Ref*** *Internal* and ***Channel*** on the desired channel, and calibrate **C1(C2** and **C3)** to lock the carrier to the LO frequency of the standard and channel set (to change the standard refer to the standard changing procedure) and obtain a locking voltage between *2V* and *3V* on **TP1**, checking that ***VCO*** is on *Lock* in the display menu.

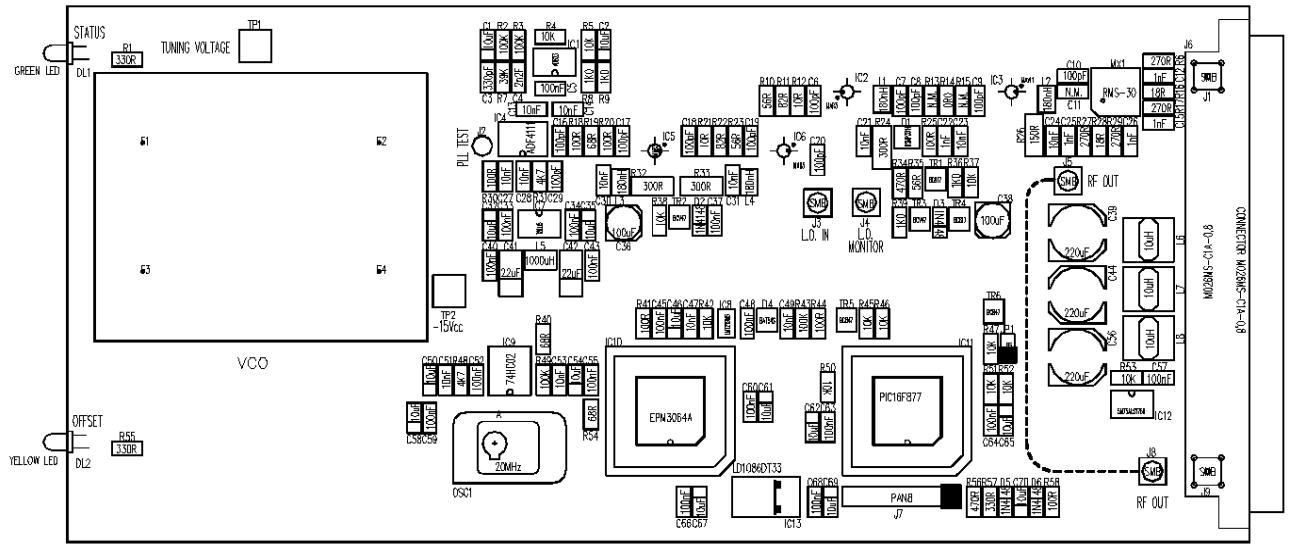
Verification of the external reference section – connect a spectrum analyser to the monitor of the **J4** module and check the sections therein:

- ❑ Configure the module with ***Ref****Internal* and check that it is possible to find adjust the synthesised frequency by acting on Tune.

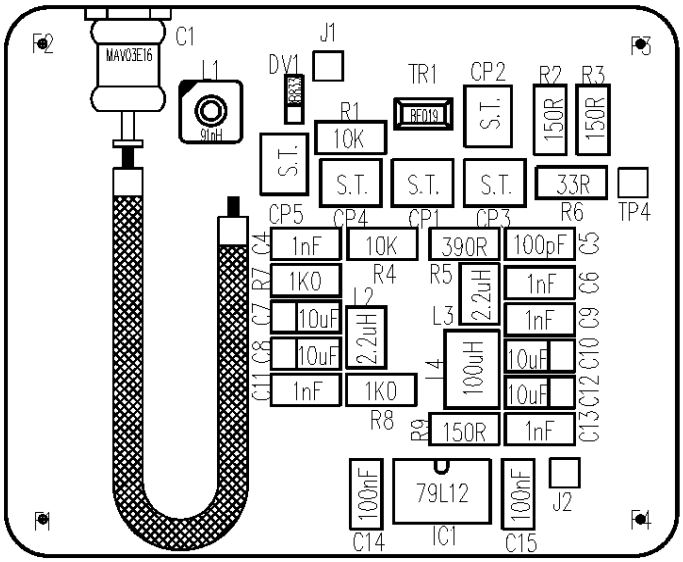
Component layout for adjustment points

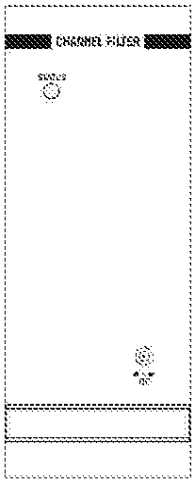


Component layout SCH0293AR0



Component layout SCH0292AR0





DESCRIPTION

The module filters the signal coming from the conversion mixer removing the local oscillator and the upper side-band and contains the voltage-controlled gain stage composed by a pin-diode attenuation cell followed by a wide-band amplification stage used as driver of the final stage.

TECHNICAL CHARACTERISTICS

Input/output impedance	50Ω R.O.S.>20dB
Filter type	Active 5-cell band-pass
RF-attenuation type	4 PIN-diodes cell
Output amplifier	Wide band
Overall gain	25dB (max.)

The module contains the following blocks:

1. **Active band-pass filter** – filters the lower side-band after conversion, it is split into three windows (I-II / III / IV-V band) to ensure the coverage of all of the TV channels to be implemented for all standards, and contains the PIN-diode attenuation cell for the gain control.

2. **Wide-band amplifier** – amplifies the filtered channel in order to obtain the correct driving level for the RF final stages (see MTF0088-0087-0089).

CALIBRATION PROCEDURE

- List of instruments

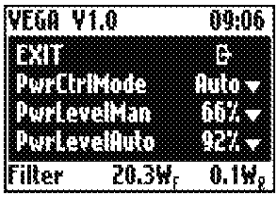
MEASURE	INSTRUMENT
Calibration of the channel filter	*- Network analyser* *- Spectrum analyser with tracking*

- Description of the adjustment points

COMPONENT	DESCRIPTION
C1-C8, C18-19	Channel filter calibration for bands III and IV-V
C17, C20-24, C26-27, C31-32	Channel filter calibration for band I-II
L1-6	Channel filter calibration for band I-II
J6	RF monitor (panel)
JP1, R29	Local gain control of the filter
J2	Channel filter input
J4	Channel filter output

The calibration procedure of the module requires a complete structure of display board (see MTG0079) and extension module (see MTG0095) in order to perform the software selection which will be referred to later and power the module itself.

- Menu of the Multistandard UHF Channel Filter Module

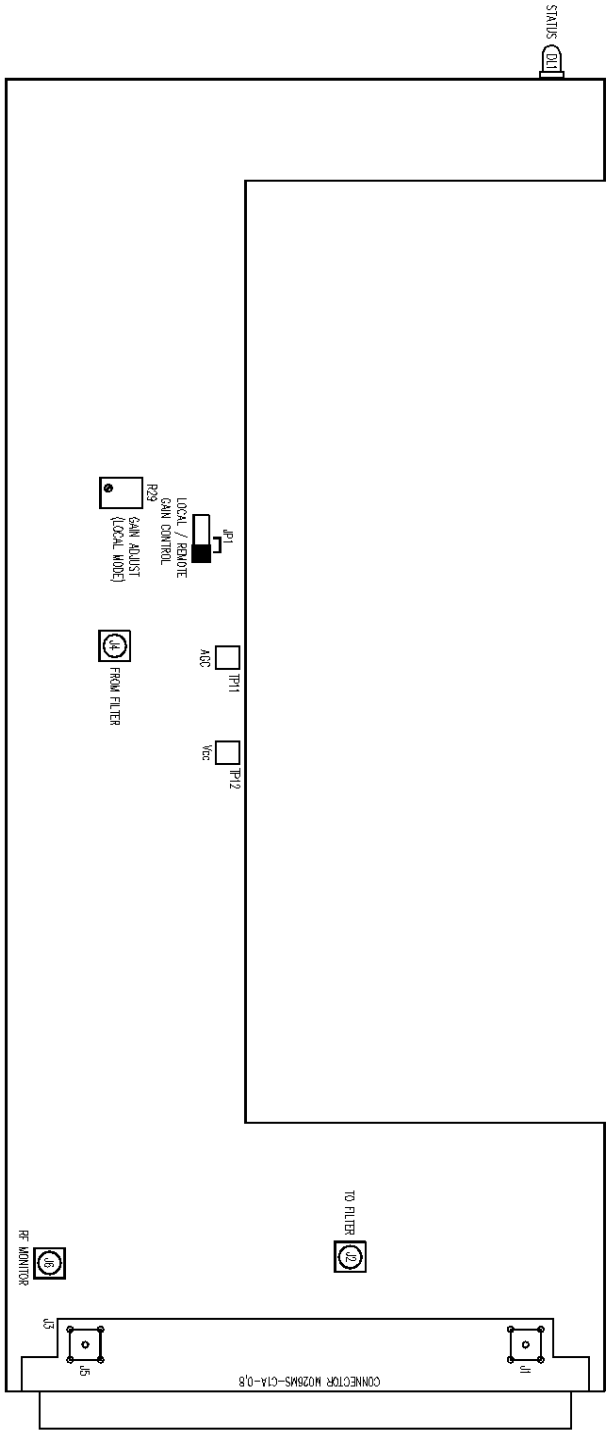


Verification of the channel filter – connect a network analyser to the channel filter and calibrate its components to obtain the desired frequency response:

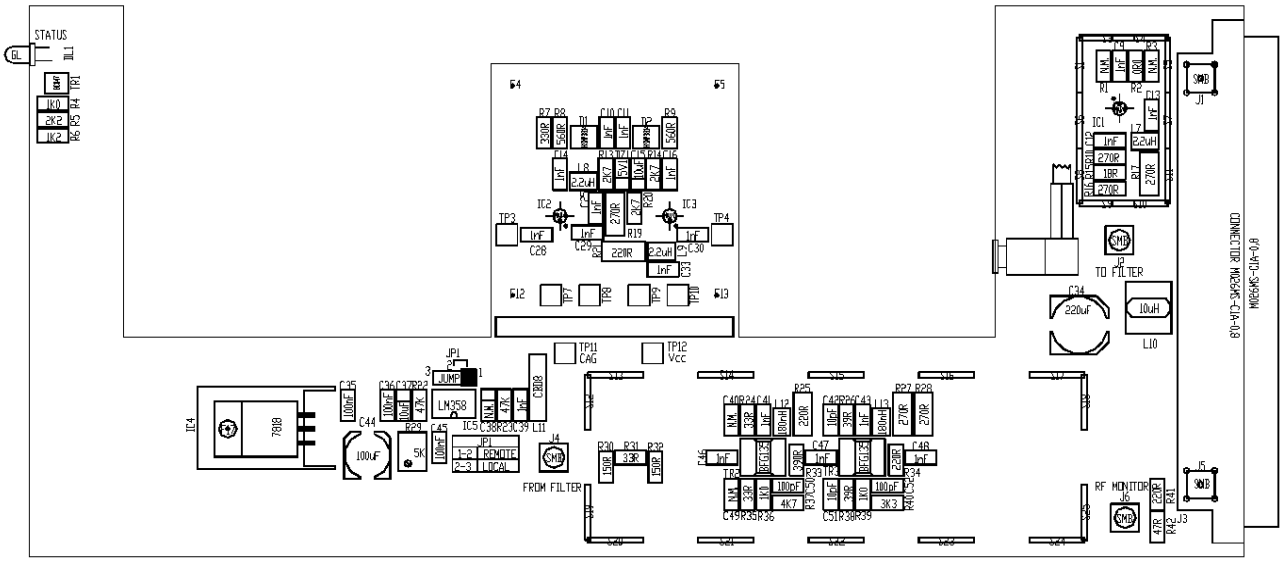
- Configure the module with ***PwrCtrlMode*** *Man* and verify that it is possible to change the gain of the filter by acting on ***PwrLevelMan***, setting **JP1** *Remote*.

Verification of the wide-band amplifier section – connect a spectrum analyser with tracking between **J4** and **J5** check that the frequency response of the amplifier is flat within *1dB* from *50MHz* to *900MHz*.

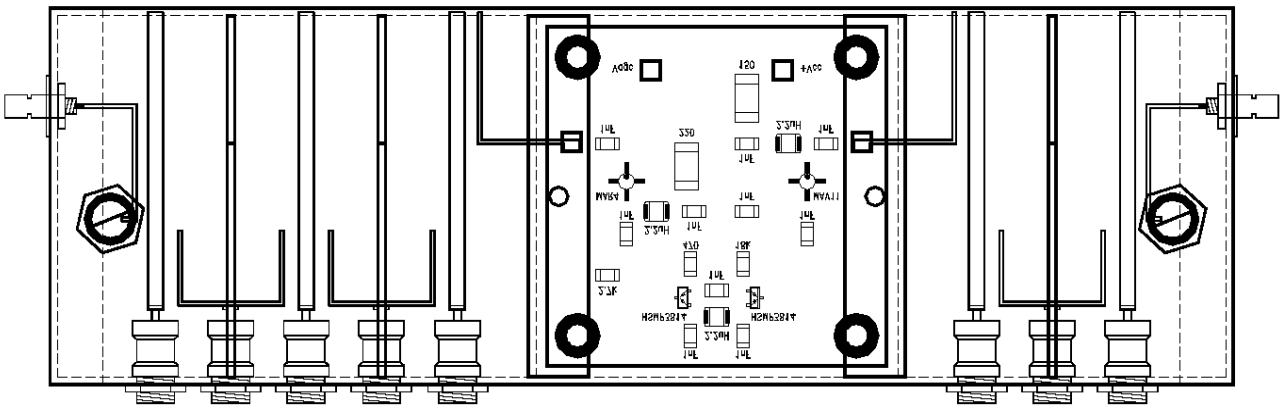
Component layout for adjustment points



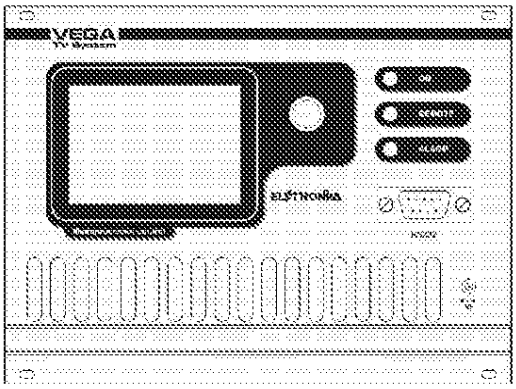
Component layout SCH0222AR2



Component layout UHF Channel Filter



SCH0135AR1 DESCRIPTION



The Controller module, located on the right side of the VEGA TV modulator, is the user interface of the whole modulator. It gathers the data from all the sections of the modulator, processes them by means of a 16bit flash micro-controller by Fujitsu and makes them available to the user both through the local interface, composed by a display and a knob, and the remote interface made up by the serial port (either the RS232 on the front or the RS485 on the back, as selected) or the interface of the telemeasuring connector.
The acquisition and setting of all the concerned parameters is made in two different ways. Analog measures reach the board from the individual modules as voltages, are conditioned on the board and then converted by an internal A/D converter in the micro.
The remaining parameters are gathered through a 2-wire RS485 interface, which runs on the bus. The display board acts as master on this 485 bus. Besides it is provided with an RTC and a non-volatile memory on an internal I2C bus.

- Dip-Switch

The display board is provided with 4 dip-switches. The dip-switches 3 and 4 are used to program the flash memory of the flash micro-controller by Fujitsu, in detail:

DIP3: On DIP4: Off Boot Programming
DIP3: Off DIP4: On Run or Firmware Programming

The "Boot Programming" configuration is only for BIOS programming purposes.
Once the BIOS has been programmed, the firmware has to be programmed at least once in order to use the board. The firmware programming and the normal operation of the board are obtained with the same position of the dip switches.
For more detail on Firmware upgrade please refer to the "Firmware Upgrade" section.

DIP2: On Factory setting
DIP2 is set to ON only during the factory setup of the exciter. This allow to store in the memory all of the settings made as 'factory defaults'.

Once the test is completed, and while the modulator is used normally, the DIP2 must be kept OFF.

- LEDs

The board is provided with three LEDs.

- On (green): it is lit when the exciter is switched on by local or remote control.

- Remote (yellow): it is lit when the exciter has been set to accept remote commands. To have it accept local commands again, the local/remote selection menu can be used.

- Alarm (red): shows that an alarm is present.
In case of alarm the red LED lights up and the icon of a bell appears in the upper bar of the display. If the alarm disappears, the red LED is turned off and the bell starts blinking, in order to show that an anomaly occurred. To know the details of the anomaly and when it occurred, the history menu can be used. Once this menu is accessed, the blinking bell icon disappears.
While an alarm is present the exciter switch off the output power. When the alarm disappear, the power is switched on again. After 5 times the exciter switch off the output power, the exciter goes in LockOut state: the power remains off till the user reset the LockOut. If the fails are far more that 1 hour than the LockOut counter is automatically cleaned.

TECHNICAL CHARACTERISTICS

Flash ROM	256kByte
RAM	6kByte
EEPROM	64kBit
Serial interfaces	2xRS485 or 1xRS485 + 1xRS232
Graphic display	128x64pixel blue with white LED back light
Encoder	Mechanical with push button
Clock and Calendar	Lithium battery backup
Telemeasures	Output: FWD, REF, Alarm
	Input: Remote OFF

FIRMWARE UPGRADE

Inside the VEGA exciter there are 5 micro-controllers. One of these is the one of the display board (16bit Fujitsu with 256K Flash) while 4 are in the audio, video, local oscillator and external reference boards respectively (8bit Microchip with 8K Flash).
It is possible to upgrade all of the micro-controllers of the exciter, but the procedures differ from the display one and the remaining four.
All upgrades are made by means of the RS232 connector on the front panel of the exciter.
All of the firmware inside the exciter are made up by two parts: the BIOS and the firmware proper. The former only programs the built-in Flash memory, while all of the operations of the micro are determined by the latter.

- ***Upgrade of the BIOS of the display board:***

While the exciter is off, set the dip-switched of the board on these positions DIP3:ON DIP4:OFF. Run the Fujitsu Flash MCU programmer application, select the BIOS file to be used, select download and follow the instructions given by the application.

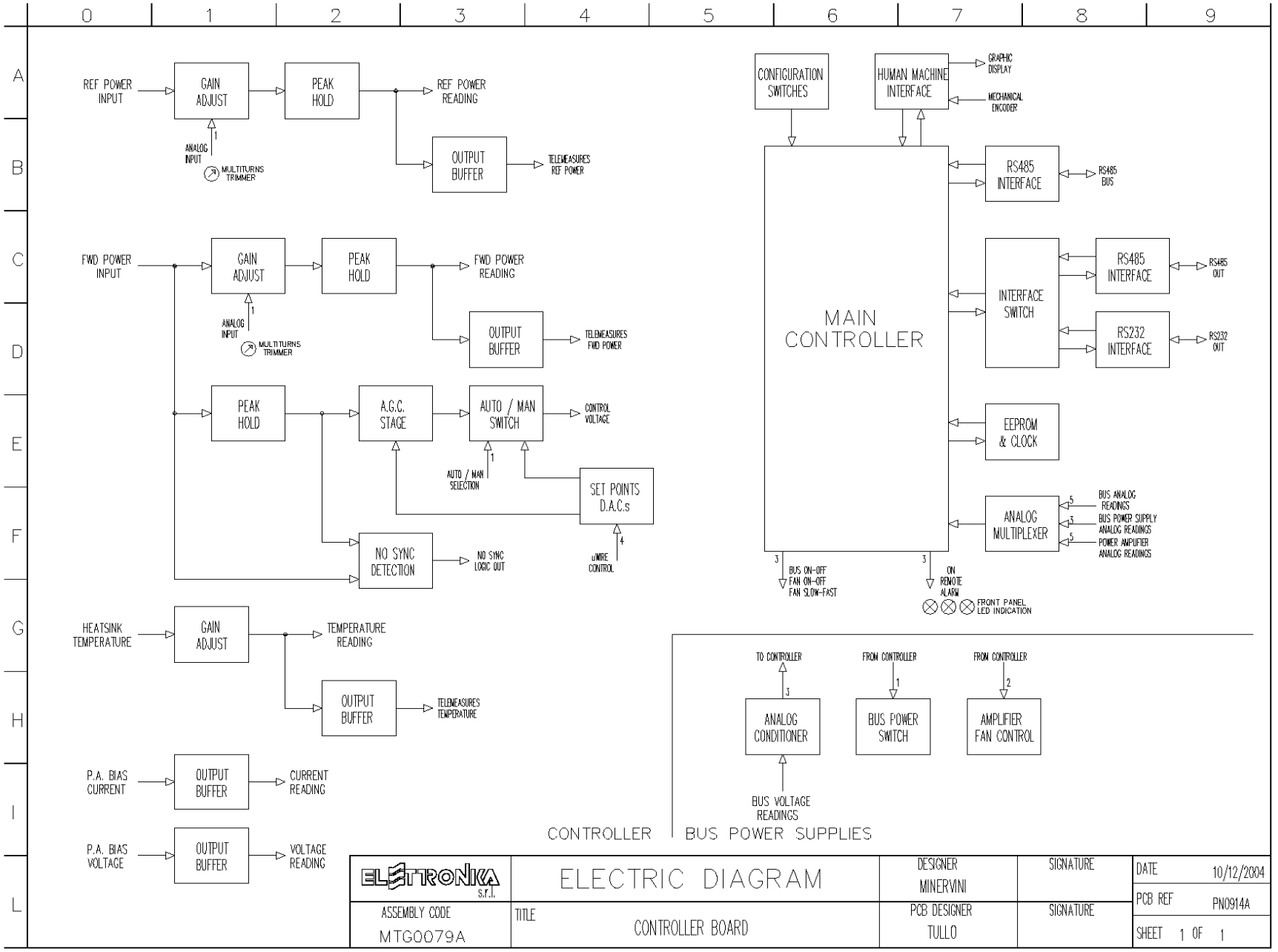
- ***Upgrade of the FIRMWARE of the display board:***

A display board provided with the BIOS is needed.
While the exciter is off, set the dip-switched of the board on these positions DIP3:OFF DIP4:ON. Run the Vega Flash Application, select the upgrade of the display board and the file to be used, select download and switch the exciter on. The upgrade will start automatically.

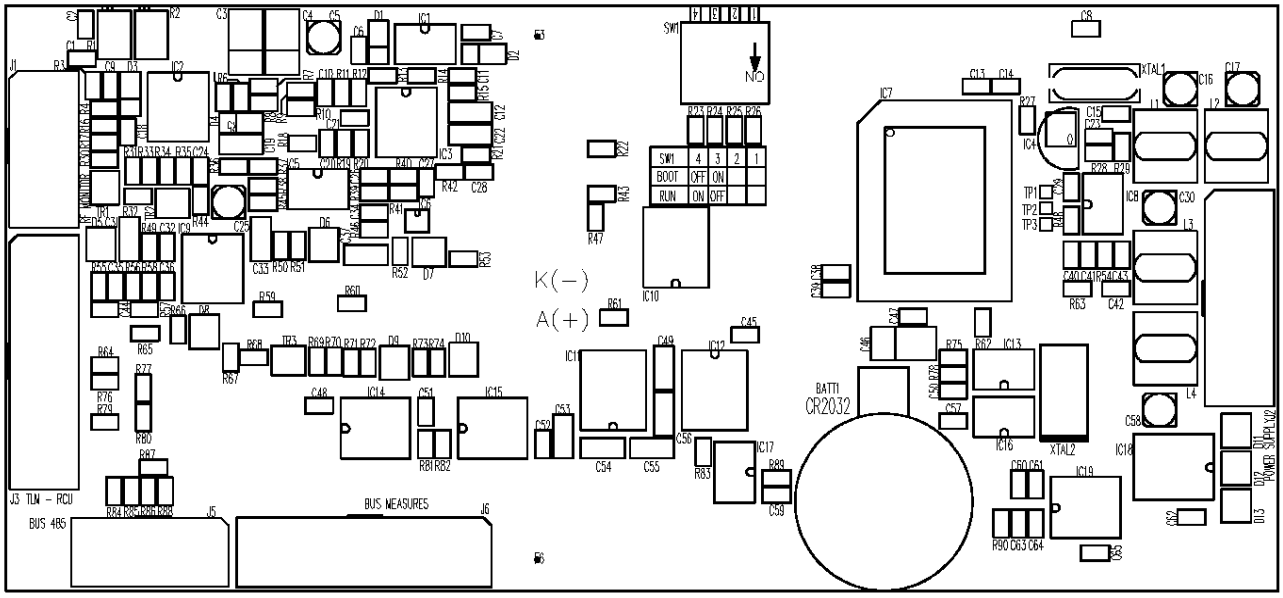
- ***Upgrade of the boards on the BUS:***

A working display board is needed in order to upgrade the boards on the BUS, because the programming of the modules is made trough the display board.

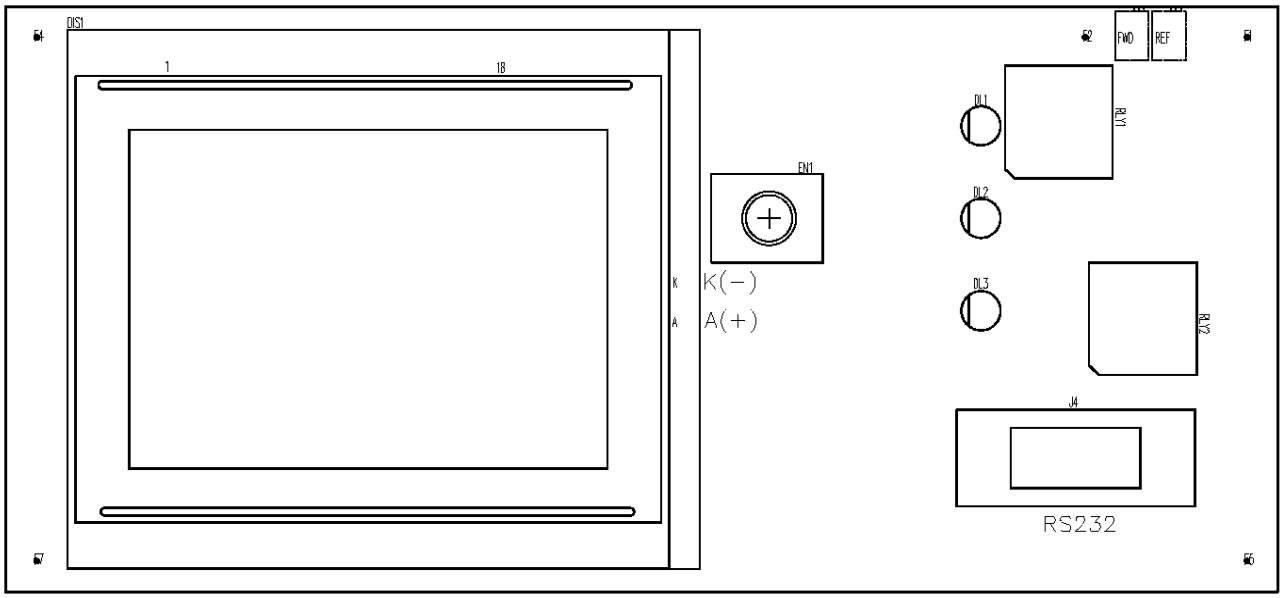
Warning: while it is possible to program both the BIOS and the firmware of the display board, it is only possible to change the firmware, and not the BIOS, of the boards on the bus. Since the BIOS is in the same micro as the firmware, this means that it is not possible to program the micro of a board on the bus on a virgin micro, which can be done, instead, on the display.
To proceed with the upgrade, while the exciter is on and remote, run the Vega Flash Application, select the board to be upgraded and the file to be sent, then select download. The upgrade will start automatically.


REF POWER INPUT
GAIN ADJUST
PEAK HOLD
REF POWER READING
ANALOG INPUT
MULTITURNS TRIMMER
OUTPUT BUFFER
TELEMEASURES REF POWER
FWD POWER INPUT
GAIN ADJUST
PEAK HOLD
FWD POWER READING
ANALOG INPUT
MULTITURNS TRIMMER
OUTPUT BUFFER
TELEMEASURES FWD POWER
PEAK HOLD
A.G.C. STAGE
AUTO / MAN SWITCH
CONTROL VOLTAGE
AUTO / MAN SELECTION
SET POINTS D.A.C.s
uWIRE CONTROL
NO SYNC DETECTION
NO SYNC LOGIC OUT
HEATSINK TEMPERATURE
GAIN ADJUST
TEMPERATURE READING
OUTPUT BUFFER
TELEMEASURES TEMPERATURE
P.A. BIAS CURRENT
OUTPUT BUFFER
CURRENT READING
P.A. BIAS VOLTAGE
OUTPUT BUFFER
VOLTAGE READING
CONFIGURATION SWITCHES
HUMAN MACHINE INTERFACE
GRAPHIC DISPLAY
MECHANICAL ENCODER
MAIN CONTROLLER
RS485 INTERFACE
RS485 BUS
INTERFACE SWITCH
RS485 INTERFACE
RS485 OUT
RS232 INTERFACE
RS232 OUT
EEPROM & CLOCK
ANALOG MULTIPLEXER
BUS ANALOG READINGS
BUS POWER SUPPLY ANALOG READINGS
POWER AMPLIFIER ANALOG READINGS
BUS ON-OFF
FAN ON-OFF
FAN SLOW-FAST
ON REMOTE ALARM
FRONT PANEL LED INDICATION
TO CONTROLLER
FROM CONTROLLER
FROM CONTROLLER
ANALOG CONDITIONER
BUS POWER SWITCH
AMPLIFIER FAN CONTROL
BUS VOLTAGE READINGS
CONTROLLER
BUS POWER SUPPLIES
ELETTRONIKA S.r.l.
ELECTRIC DIAGRAM
DESIGNER
MINERVINI
SIGNATURE
DATE 10/12/2004
ASSEMBLY CODE
MTG0079A
TITLE
CONTROLLER BOARD
PCB DESIGNER
TULLO
SIGNATURE
PCB REF PN0914A
SHEET 1 OF 1

Component layout SCH0135AR1 - Bot layer



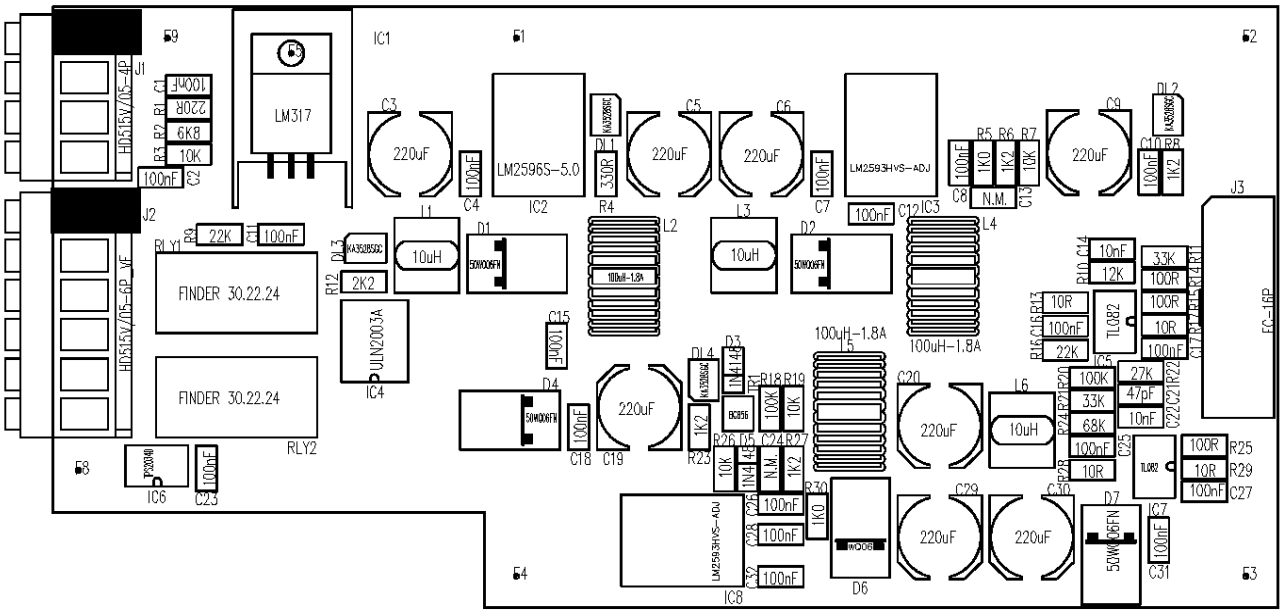
Component layout SCH0135AR1 - Top layer



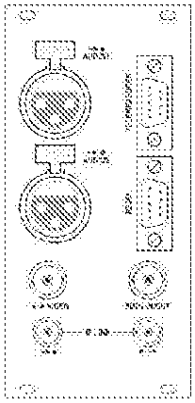
SCH0231AR1 DESCRIPTION

The power supply accepts a nominal continuous input voltage of 28V and supplies three continuous current output with voltages of +5V, +15V and -15V. It also provides a voltage of +28V to the system bus. The power supply voltages towards the system bus are switched by means of relays controlled by the micro-processor of the control board.
There are switching regulators for the +5V, +15V and -15V voltages.
The power supply board provides the operating voltages to the control board trough multi-wire flat cable. In this there are also analog voltages to monitor the power supply status. The monitoring of the +5V, +15V and -15V voltages are conditioned to about 4V nominal.
The board provides the power supply to the system fan. Its on/off status and its speed can be set by the micro-processor of the control board.
The connections to the system bus and power supply board are made using a fast-lock connector.

Component layout SCH0231AR1



DESCRIPTION

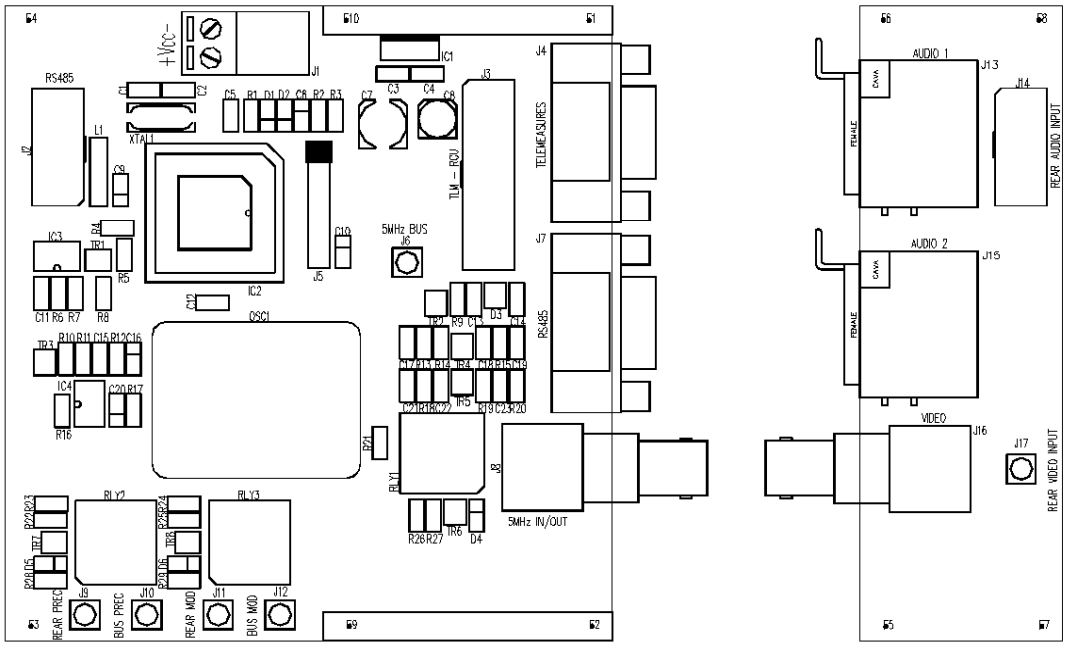


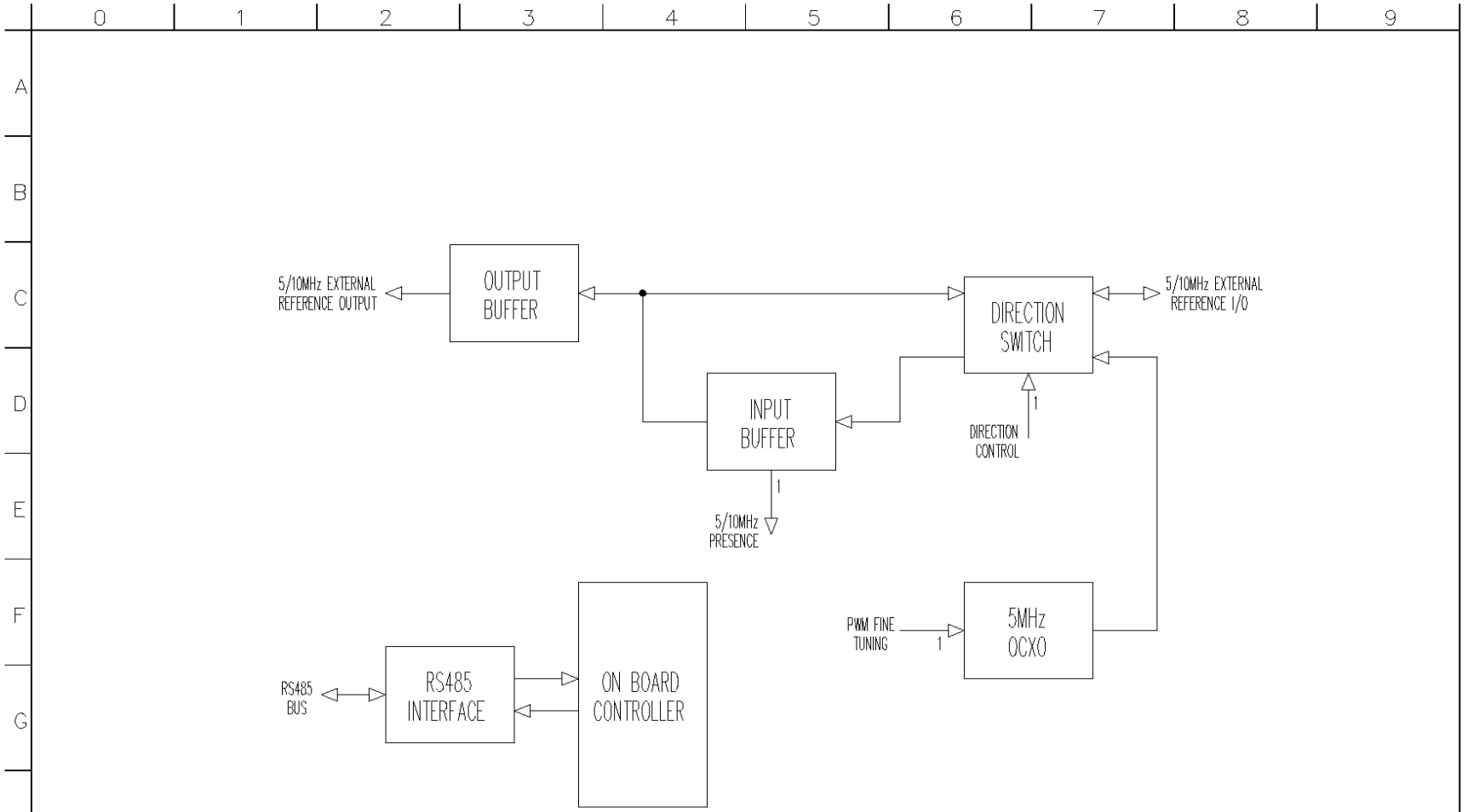
The board contains the 5/10MHz external reference and a series of functions on the back of the apparatus: the rear audio and video inputs, the telemeasuring connectors and the RS485, the external reference input (or output) and the IF connection before the linearity pre-corrector, in order to allow the insertion in the chain of different modulation systems such as NICAM.

TECHNICAL CHARACTERISTICS

Frequency reference	5-10MHz
Detector presence	0dBm threshold
Connector	BNC input-output selectable (sw)
O.C.X.O. Characteristics *(optional)*	0.05ppm long term stability
O.C.X.O. Tuning frequency	±5ppm fine tunability (sw)
O.C.X.O. Warm up consumption	4.5W 10min @25°C
IF Link	OPEN-CLOSED Selection switch (sw)
A-V Rear connections	Available on exciter arrangement
Telemasures	DB9
RS485-RS232	DB9 Selectable (sw)

Component layout SCH0266AR1





ELETTRONIKA s.r.l.	ELECTRIC DIAGRAM	DESIGNER MINERVINI	SIGNATURE	DATE 09/11/2004
ASSEMBLY CODE MTG0076A	TITLE EXTERNAL REFEREMENT MODULE	PCB DESIGNER TULLO	SIGNATURE	PCB REF PN1112AR2
				SHEET 1 OF 1

The module contains the following blocks:

1. **Input and output buffers** – de-couple the internal circuitry from the I/O conenctors and detect the presence of the reference signal.
2. **Direction switch** – allows the configuration of the BNC as either input or output for the 5/10MHz reference signal.
3. **5MHz O.C.X.O.**– 5MHz internal reference system *(optional)*, which frequency can be fine-adjusted via software.
4. **Controller** – all of the described operations are managed by a microcontroller communicating to the user interface board (see MTG0079) by RS485 protocol; the local controller stores the status of the module and a reprogramming of the firmware (possible via RS485 from the display board) does not after its contents.

EXTERNAL PIN OUT CONNECTORS

Telemeasures (DB9)

PIN N°	SIGNAL TYPE	IN / OUT	FUNCTION
1	Analog	Output	FWD Power
2	Analog	Output	REF Power
3	Analog	Output	Temperature
4	Analog	Input	FWD Power
5	GND	-	-
6	Digital	Output	Free contact with pin7 - Alarm
7	Digital	Output	Free contact with pin6 - Alarm
8	Digital	Input	GND= Off - OPEN= On
9	Digital	Input	N.U.

RS485 (DB9)

PIN N°	FUNCTION
1	N.C.
2	RX-
3	RX+
4	+5V
5	GND
6	+5V
7	TX-
8	TX+
9	N.C.

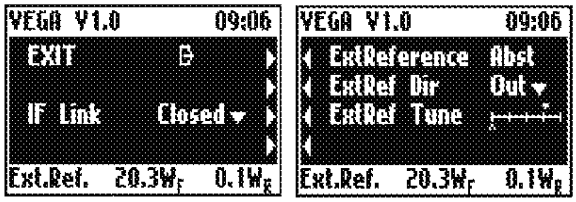
CALIBRATION PROCEDURE

- *List of instrument*

MEASURE	INSTRUMENT
Frequency referement control	- *Spectrum analyser*

The calibration procedure of the module requires a complete structure of display board (see MTG0079) in order to perform the software selection which will be referred to later and power the module itself..

- Menu of the External Referement Module



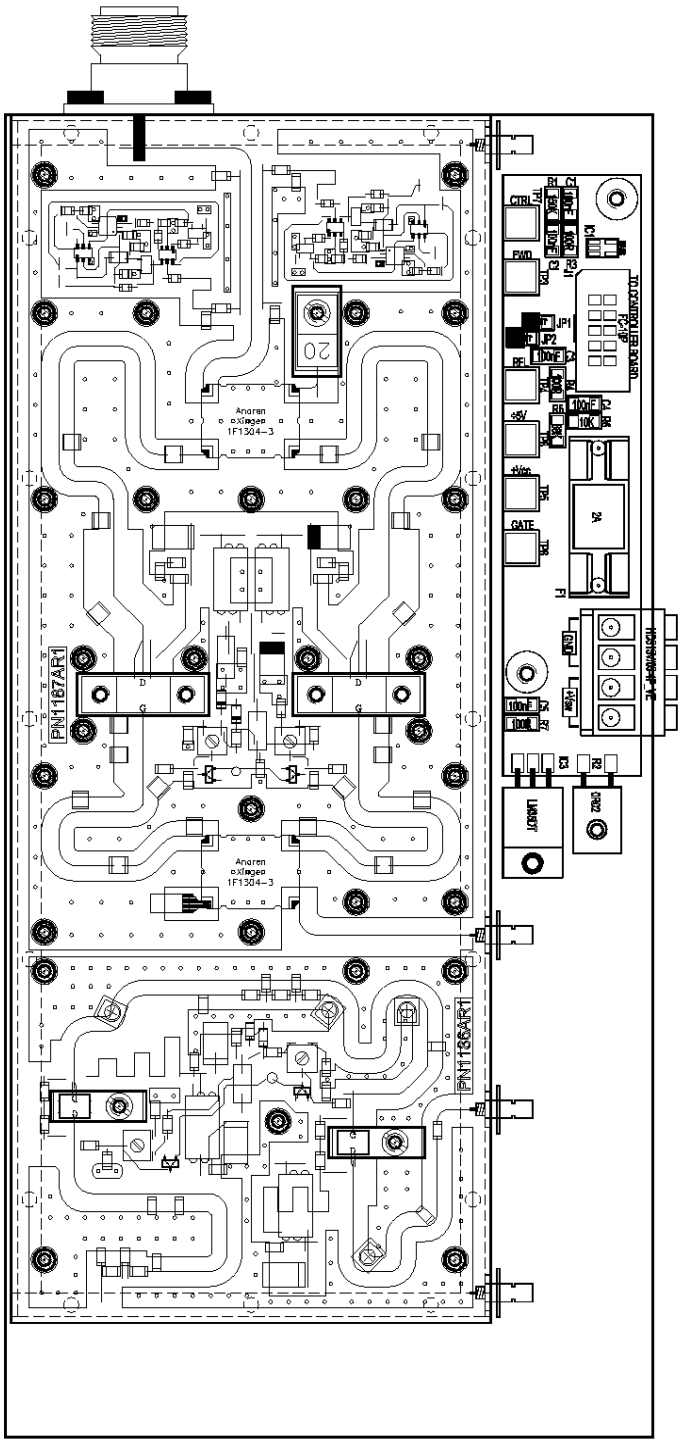
Verification of the external reference section – connect a spectrum analyser to the BNC labelled *EXT REF IN/OUT* and check the sections therein:

- ❑ Configure the module with ***ExtREF Dir Out*** and check the presence of the 5MHz carrier with ***ExtReference*** set to Pres in the display menu.
- ❑ Check that the 5MHz frequency is fine-adjusted by acting on ***ExtRef Tune***.

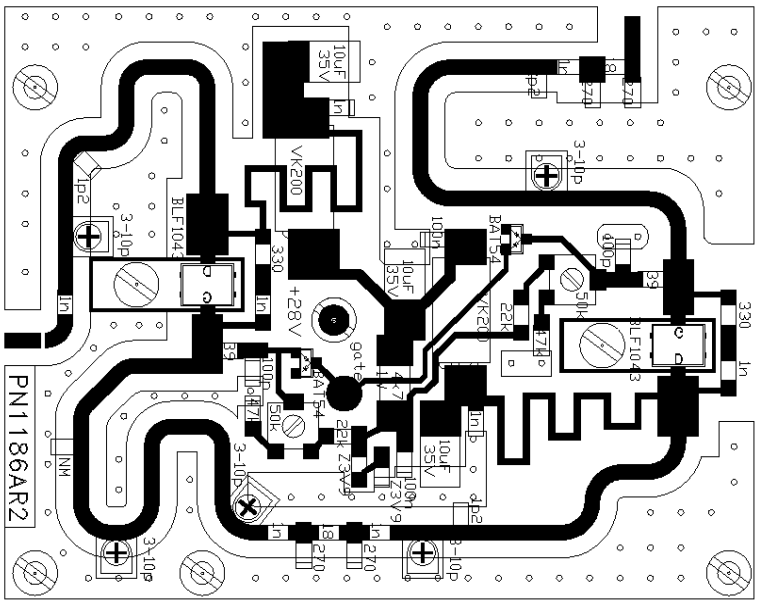
Verification of the IF Link section:

- ❑ Configure the module with ***IF Link*** open and closed checking the switching of the relays.

Component layout MTF0088AR1

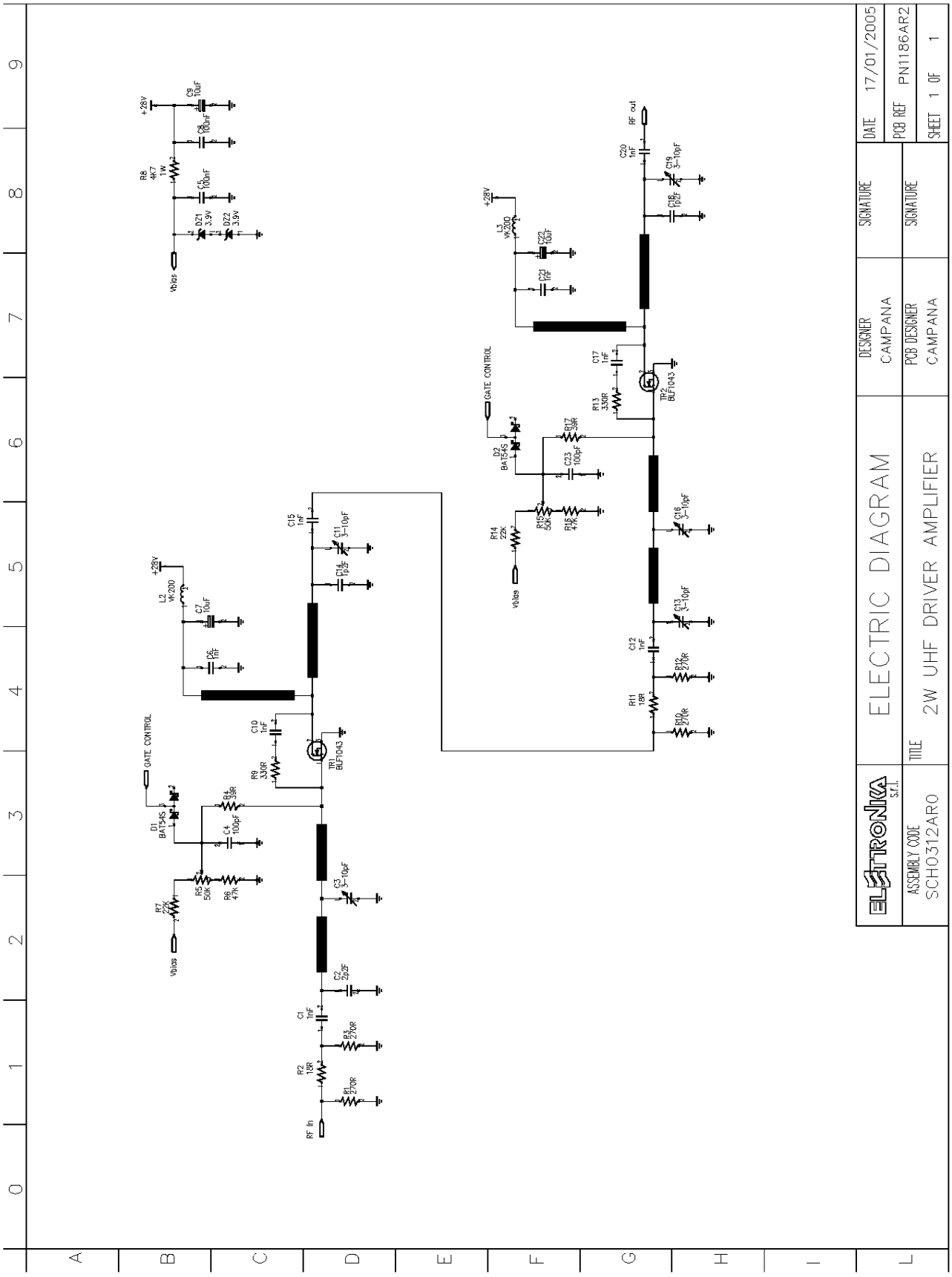


Component layout SCH0312AR0

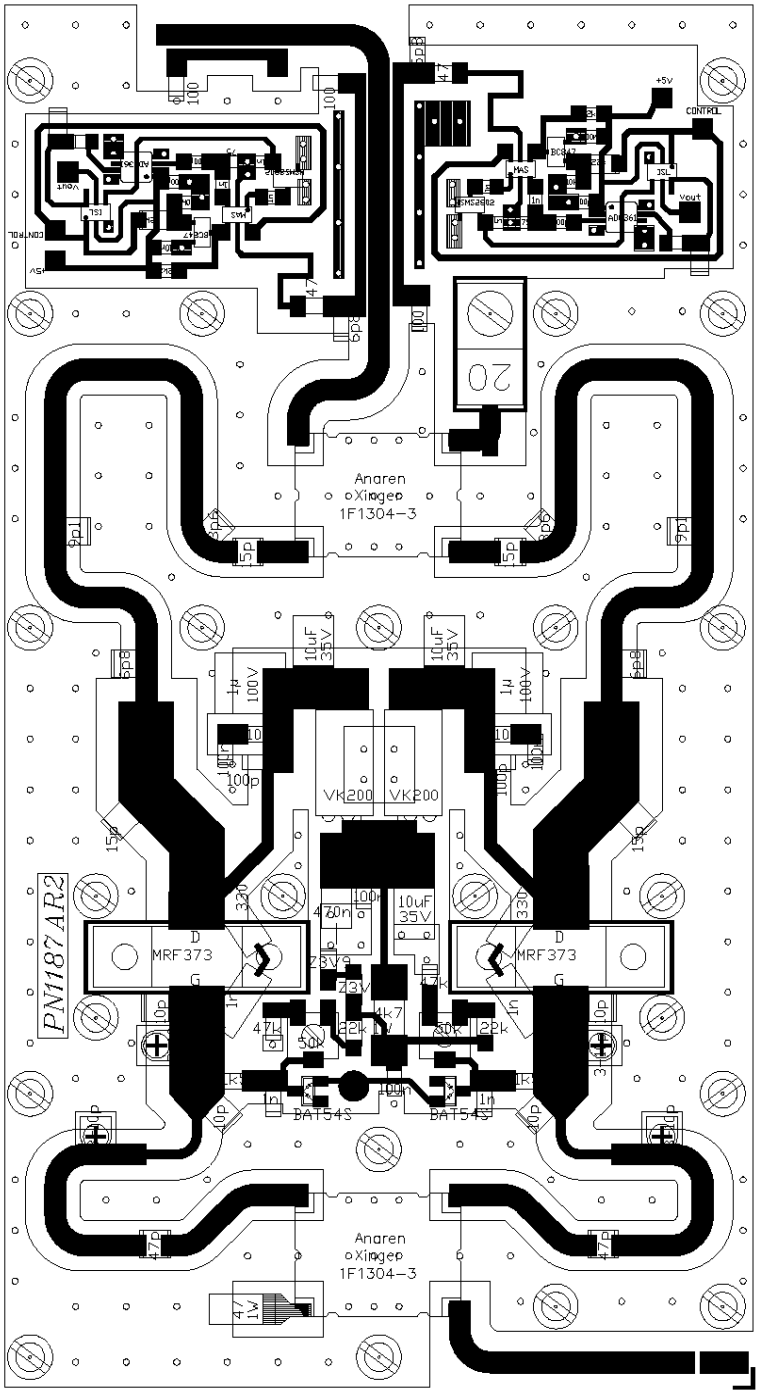


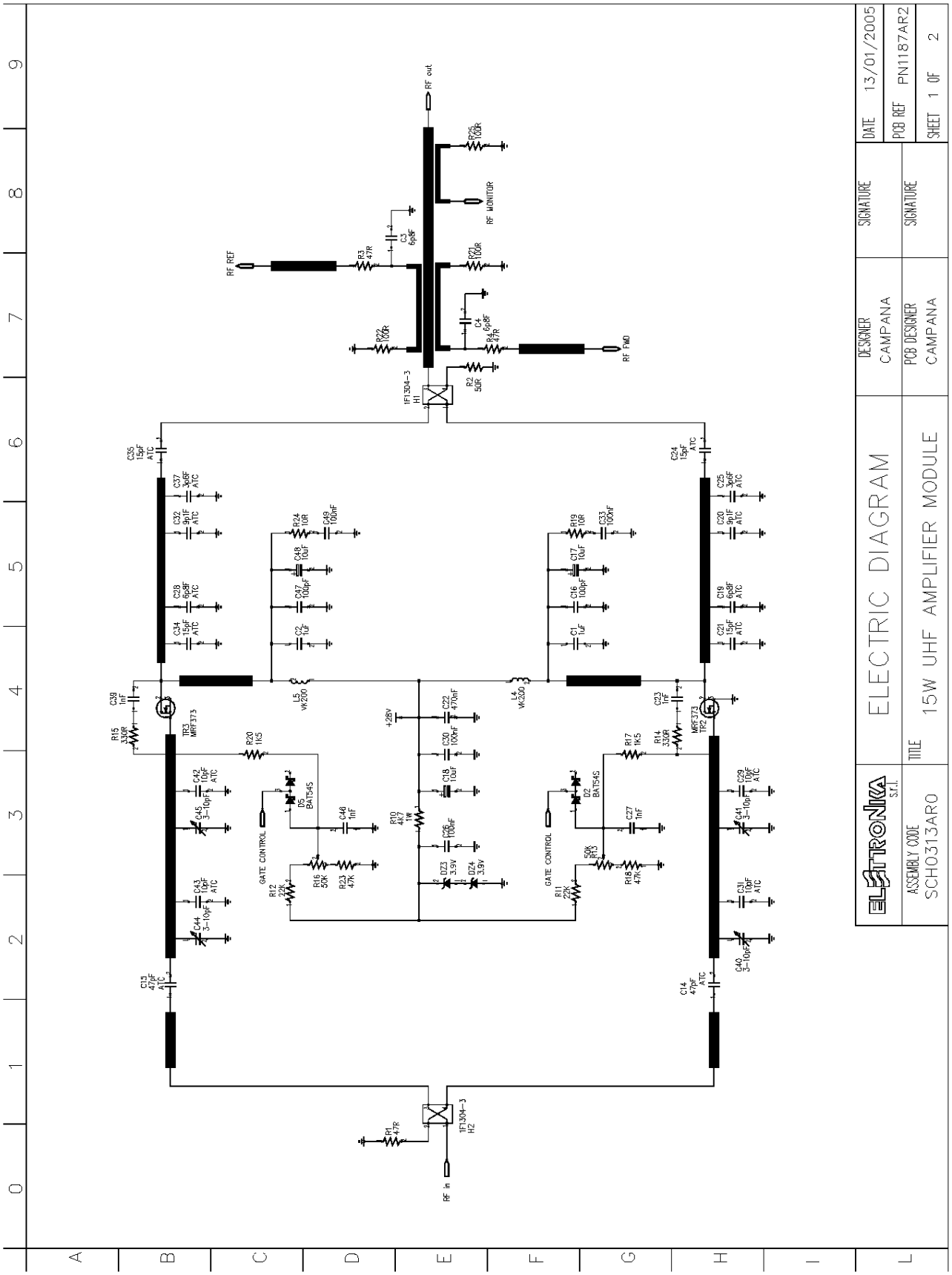
COMPONENT LIST *SCH0312AR0*

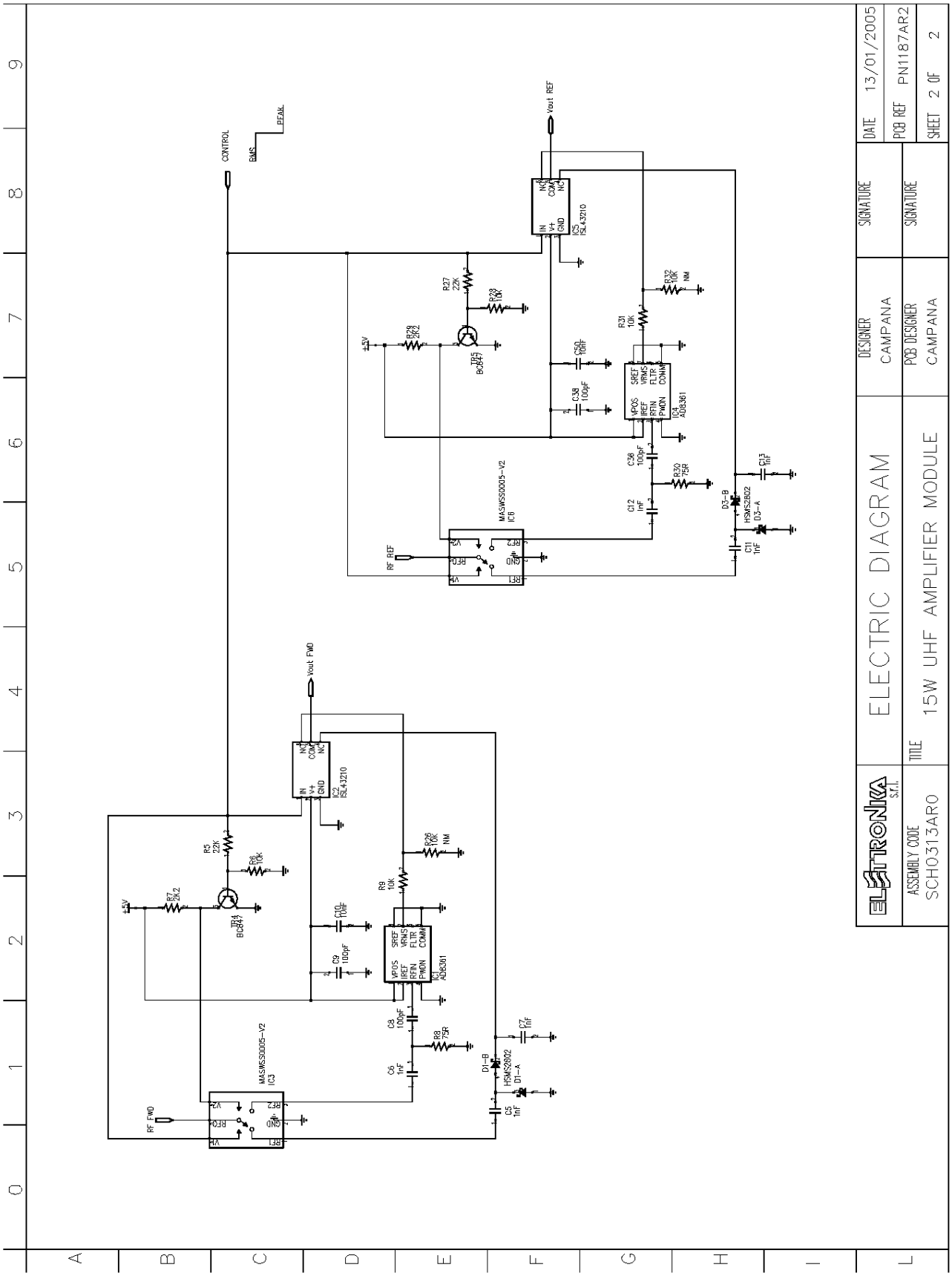
Part Name/Number	Description	Qty.	Comps.
CC 100nF-S 01065C	01065C Y5V 1206 COND	2	C5, C8
CC 100pF-S 01092	01092 SMD 1206 COND	2	C4, C23
CC 1nF-S 01096	01096 SMD 1206 COND	8	C1, C6, C10, C12, C15, C17, C20, C21
CC 1p2F-S 01081	01081 SMD 1206 COND	2	C14, C18
CC 2p2F-S 01081B	01081B SMD 1206 COND	1	C2
CE 10uF35V-S 01628A	01628A TANTALIUM ELETTR SMD CO	3	C7, C9, C22
CV 3-10pF-S 01475	01475 VARIABLE COND	5	C3, C11, C13, C16, C19
D BAT54S	03199 SMD SCHOTTKY DIODE A-K T	2	D1-2
DZ 3V9 03107	03107 ZENER DIODE	2	DZ1-2
IND VK200 05013	05013 INDUCTOR	2	L2-3
R 18R-S 00020A	00020A RES 1/4W 5% SMD 1206	2	R2, R11
R 22K-S 00057A	00057A RES 1/4W 5% SMD 1206	2	R7, R14
R 270R-S 00034A	00034A RES 1/4W5% SMD 1206	4	R1, R3, R10, R12
R 330R-S 00035B	00035B RES 1/4W 5% SMD 1206	2	R9, R13
R 39R-S 00024A	00024A RES 1/4W 5% SMD 1206	2	R4, R17
R 47K-S 00061A	00061A RES 1/4W 5% SMD 1206	2	R6, R16
R 4K7-1W-S	00401 RES 1W 5% SMD 2512	1	R8
RV 50K-S-H/S 00797	00797 SMD VARIABLE RESISTOR	2	R5, R15
TR BUZ30A	03020 MOSFET-N TRANSISTOR	2	TR1-2


ELECTRIC DIAGRAM
2W UHF DRIVER AMPLIFIER
ELETRONIKA S.r.l.
ASSEMBLY CODE SCH0312AR0
TITLE
DESIGNER CAMPANA
PCB DESIGNER CAMPANA
SIGNATURE
SIGNATURE
DATE 17/01/2005
PCB REF PN1186AR2
SHEET 1 OF 1
RF In
RF out
GATE CONTROL
+28V
Vbias
TR1 BLF1043
TP2 BLF1043
D1 BAT54S
D2 BAT54S
L2 VK200
L3 VK200
D21 3.9V
D22 3.9V

Component layout SCH0313AR0

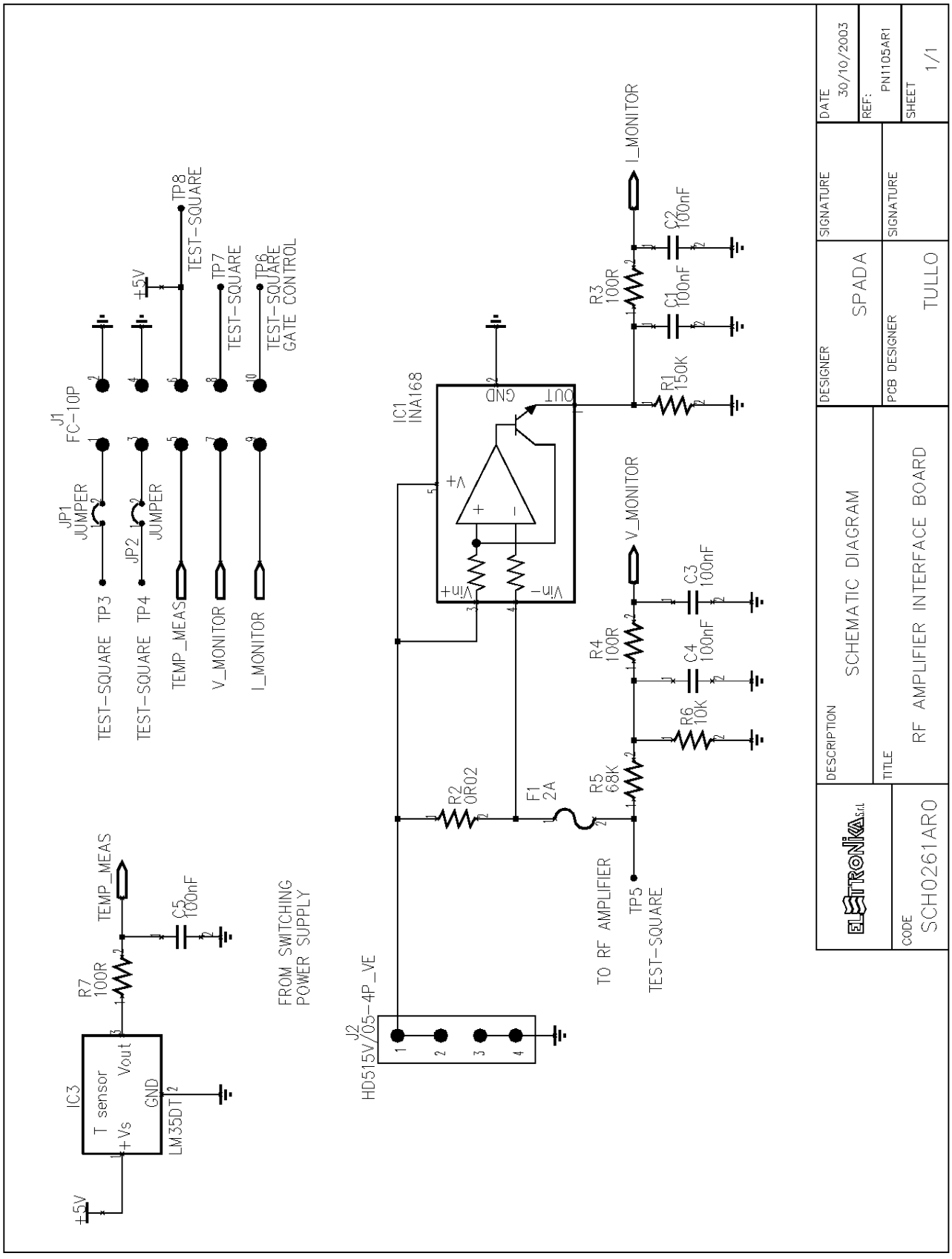



ELETTRONIKA S.r.l.
ELECTRIC DIAGRAM
15W UHF AMPLIFIER MODULE
ASSEMBLY CODE SCH0313ARO
TITLE
DESIGNER CAMPANA
PCB DESIGNER CAMPANA
SIGNATURE
SIGNATURE
DATE 13/01/2005
PCB REF PN1187AR2
SHEET 1 OF 2
RF REF
RF out
RF MONITOR
RF FWD
RF in
GATE CONTROL
GATE CONTROL
+28V
MRF373
MRF373
BAT54S
BAT54S
3.9V
3.9V
IFT304-3
IFT304-3

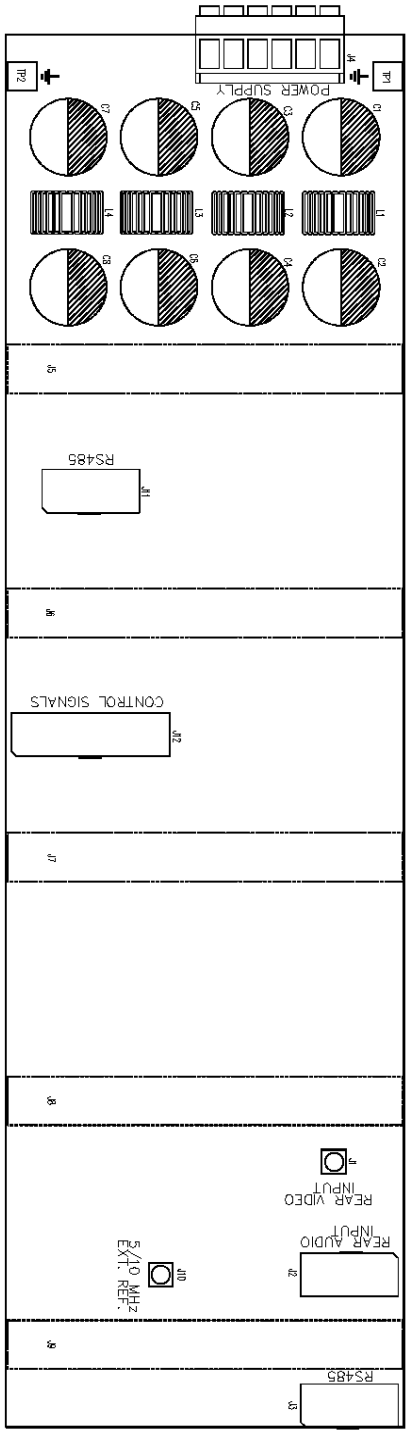

ELETRONIKA S.r.l.
ELECTRIC DIAGRAM
15W UHF AMPLIFIER MODULE
ASSEMBLY CODE SCH0313ARO
TITLE
DESIGNER CAMPANA
PCB DESIGNER CAMPANA
SIGNATURE
SIGNATURE
DATE 13/01/2005
PCB REF PN1187AR2
SHEET 2 OF 2
CONTROL
BIAS
EEAK
Vout REF
Vout FWD
RF FWD
RF REF
IC1 AD8361
IC2 ISL43210
IC3 MASWSS0005-V2
IC4 AD8361
IC5 ISL43210
IC6 MASWSS0005-V2
D1-A HSMS2802
D1-B HSMS2802
D3-A HSMS2802
D3-B HSMS2802
TR1 BC847
TR2 BC847
TR3 BC847
TR4 BC847
+5V
R5 22K
R6 10K
R7 5K2
R8 75R
R9 10K
R10 10K NM
R11 10K
R12 10K NM
R27 22K
R28 10K
R29 5K2
R30 75R
R31 10K
R32 10K NM
C5 1nF
C6 1nF
C7 1nF
C8 100pF
C9 100pF
C10 10nF
C11 1nF
C12 1nF
C13 1nF
C37 10nF
C38 100pF
C39 100pF

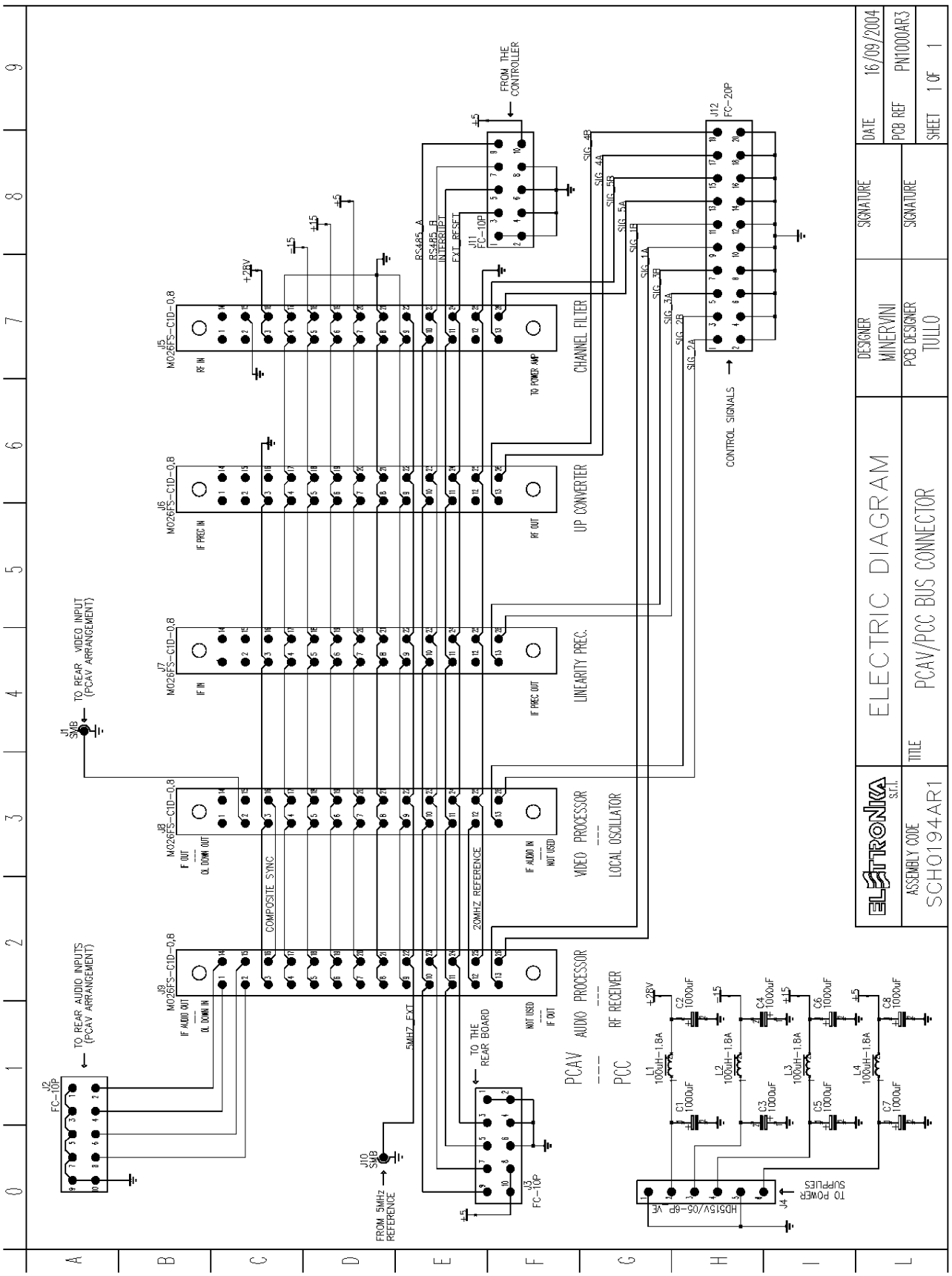
COMPONENT LIST *SCH0313AR0*

Part Name/Number	Description	Qty.	Comps.
CC 100nF-S 01065C	01065C Y5V 1206 COND	1	C26
CC 100nFAVX 01065A	01065A CERAMIC COND	3	C30, C33, C49
CC 100pF-S 01092	01092 SMD 1206 COND	2	C16, C47
CC 100pF-S 01092C	01092C SMD 0805 COND	4	C8-9, C36, C38
CC 10nF-S 01053A	01053A SMD 0805 COND	2	C10, C50
CC 10pF-S 01086	01086 SMD 1206 COND	4	C29, C31, C42-43
CC 1nF 01041	01041 CERAMIC COND	2	C23, C39
CC 1nF-S 01096	01096 SMD 1206 COND	2	C27, C46
CC 1nF-S 01096A	01096A SMD 0805 COND	6	C5-7, C11-13
CC 1uF 01077	01077 CERAMIC COND	2	C1-2
CC 470nF 100V-S	01073A POLIESTER COND SMD MOUN	1	C22
CC 47pF-S 01100	01100 SMD 1206 COND	2	C14-15
CC 56pF-S 01091	01091 SMD 1206 COND	4	C20, C25, C32, C37
CC 6p8F-S 01084	01084 SMD 1206 COND	8	C3-4, C19, C21, C24, C28, C34-35
CE 10uF35V-S 01628A	01628A TANTALIUM ELETTR SMD CO	3	C17-18, C48
CV 3-10pF-S 01475	01475 VARIABLE COND	4	C40-41, C44-45
D BAT54S	03199 SMD SCHOTTKY DIODE A-K T	2	D2, D5
D HSMS2802 03207	03207 SMD DIODE	2	D1, D3
DZ 3V9 03107	03107 ZENER DIODE	2	DZ3-4
H ANAREN 1F1304-3	05368 HIBRID COUPLER ANAREM	2	H1-2
IC AD8361 04899	04899 SMD INTEG CIRCUIT	2	IC1, IC4
IC ISL43210-S	04567 SMD INTEG CIRCUIT	2	IC2, IC5
IC MASWSS0005-V2-S	04568 SMD INTEG CIRCUIT	2	IC3, IC6
IND VK200 05013	05013 INDUCTOR	2	L4-5
R 100R-S 00029A	00029A RES 1/4W 5% SMD 1206	3	R21-22, R25
R 10K-S 00053C	00053C RES 1/4W 5% SMD 0805	6	R6, R9, R26, R28, R31-32
R 10R-S 00017A	00017A RES 1/4W 5% SMD 1206	2	R19, R24
R 1K5-S 00043A	00043A RES 1/4W 5% SMD 1206	2	R17, R20
R 22K-S 00057A	00057A RES 1/4W 5% SMD 1206	4	R5, R11-12, R27
R 2K2-S 00045C	00045C RES 1/4W 5% SMD 0805	2	R7, R29
R 330R 0035	0035 RES 1/4W 5%	2	R14-15
R 47K-S 00061A	00061A RES 1/4W 5% SMD 1206	2	R18, R23
R 47R-1W-S	00384 RES 1W 5% SMD 2512	1	R1
R 47R-S 00025A	00025A RES 1/4W 5% SMD 1206	2	R3-4
R 4K7-1W-S	00401 RES 1W 5% SMD 2512	1	R10
R 50R 60W TERM	00432 50 OHM 60W RF TERM	1	R2
R 75R-S 00221C	00221C RES 1/4W 5% SMD 0805	2	R8, R30
RV 50K-S-H/S 00797	00797 SMD VARIABLE RESISTOR	2	R13, R16
TR BC847 03456	03456 NPN SMD TRANSISTOR	2	TR4-5
TR BUZ30A	03020 MOSFET-N TRANSISTOR	2	TR2-3


J1
FC-10P
JP1
JUMPER
JP2
JUMPER
TEST-SQUARE TP3
TEST-SQUARE TP4
TEMP_MEAS
V_MONITOR
I_MONITOR
+5V
TP8
TEST-SQUARE
TP7
TEST-SQUARE
TP6
TEST-SQUARE
GATE CONTROL
IC3
T sensor
+Vs
Vout
GND
LM35DT
R7
100R
C5
100nF
TEMP_MEAS
FROM SWITCHING
POWER SUPPLY
J2
HD515V/05-4P_VE
IC1
INA168
GND
OUT
V+
Vin+
Vin-
R2
0R02
F1
2A
R5
68K
R4
100R
C4
100nF
R6
10K
C3
100nF
V_MONITOR
TP5
TEST-SQUARE
TO RF AMPLIFIER
R3
100R
C2
100nF
C1
100nF
R1
150K
I_MONITOR
DESCRIPTION
SCHEMATIC DIAGRAM
TITLE
RF AMPLIFIER INTERFACE BOARD
CODE
SCH0261AR0
DESIGNER
SPADA
PCB DESIGNER
TULLO
SIGNATURE
SIGNATURE
DATE
30/10/2003
REF:
PN1105AR1
SHEET
1/1

Component layout SCH0194AR1



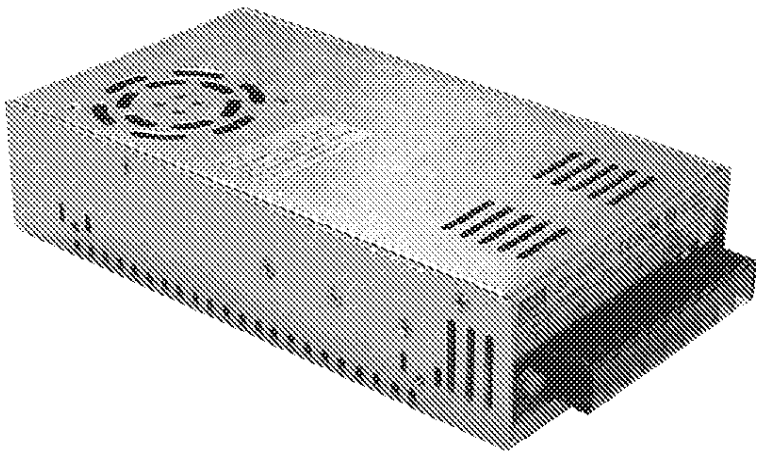

ELETRONIKA S.r.l.
ELECTRIC DIAGRAM
PCAV/PCC BUS CONNECTOR
ASSEMBLY CODE SCH0194AR1
DESIGNER MINERVINI
PCB DESIGNER TULLO
DATE 16/09/2004
PCB REF PN10004AR3
SHEET 1 OF 1
PCAV AUDIO PROCESSOR
PCC RF RECEIVER
VIDEO PROCESSOR
LOCAL OSCILLATOR
LINEARITY PREC.
UP CONVERTER
CHANNEL FILTER
TO REAR AUDIO INPUTS (PCAV ARRANGEMENT)
TO REAR VIDEO INPUT (PCAV ARRANGEMENT)
FROM THE CONTROLLER
CONTROL SIGNALS
TO THE REAR BOARD
FROM 5MHz REFERENCE
TO POWER SUPPLIES
COMPOSITE SYNC
20MHZ REFERENCE
5MHZ_EXT
RS485_A
RS485_B
INTERRUPT
EXT_RESET
+28V
+15
+5

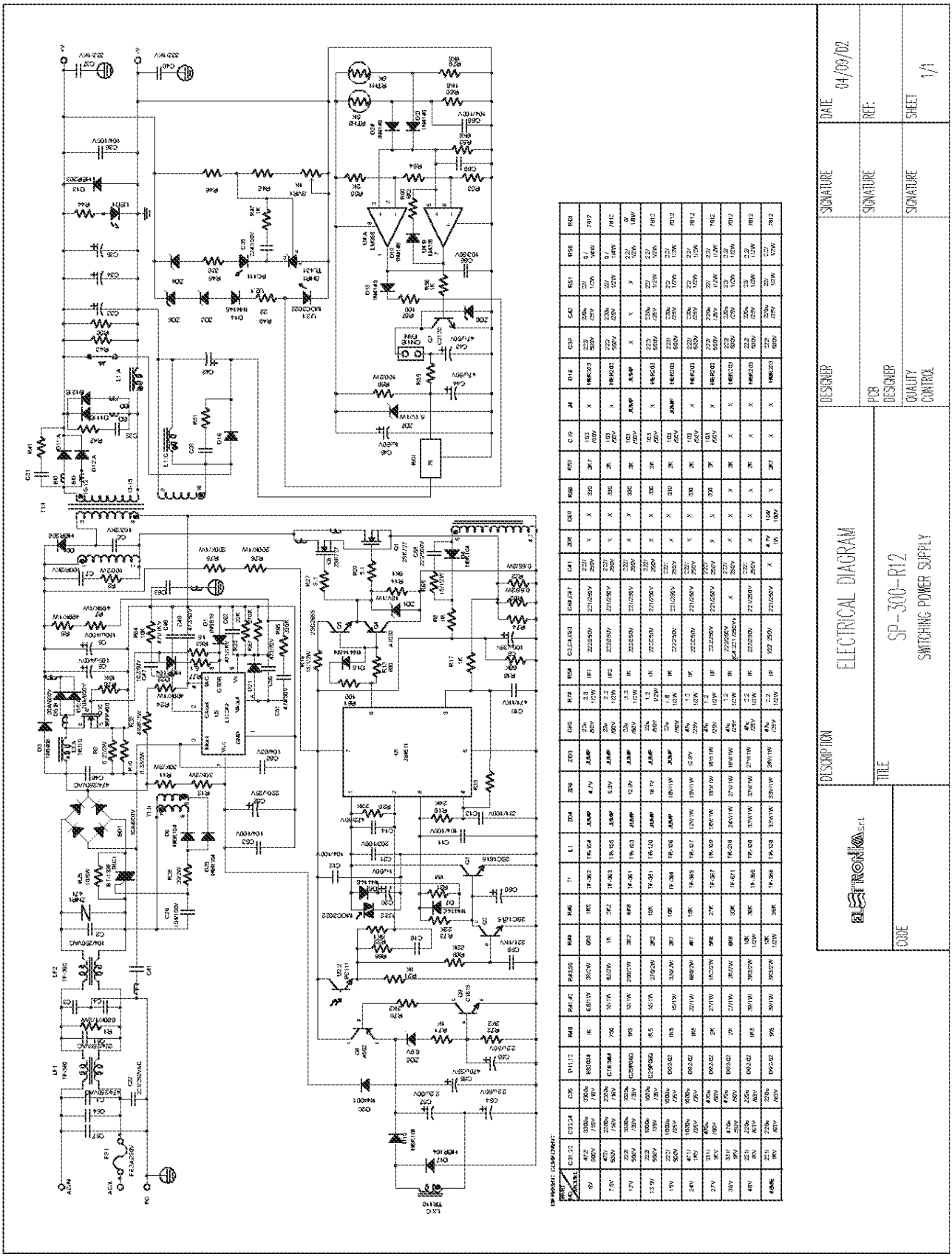
COMPONENT LIST *SCH0194AR1*

Part Name/Number	Description	Qty.	Comps.
CC 100nF-S 01065C	01065C Y5V 1206 COND	19	C1-2, C4, C7-8, C10-12, C15-18, C23, C25-28, C31-32
CC 10nF-S 01053B	01053B SMD 1206 COND	2	C14, C22
CC 1206 N. M.	N. M. SMD 1206 COND	2	C13, C24
CC 47pF-S 01100	01100 SMD 1206 COND	1	C21
CE 220uF50V LOW ESR	01799A ELETTR SMD COND LOW ESR	8	C3, C5-6, C9, C19-20, C29-30
D 1N4148-S 03002	03002 SMD DIODE	2	D3, D5
D 50WQ06FN	03019A SMD DIODE SCHOTTKY 5,5A	5	D1-2, D4, D6-7
DL KA-3528SGC 03057	03057 GREEN SMD LED DIODE	4	DL1-4
IC LM2593HVS-ADJ	04089 SMD INTEG CIRCUIT	2	IC3, IC8
IC LM2596S-5.0	04580 SMD INTEG CIRCUIT	1	IC2
IC LM317 04340	04340 INTEG CIRCUIT	1	IC1
IC TL082-S 04796A	04796A SMD INTEG CIRCUIT	2	IC5, IC7
IC TPS2034D-S	04088 SMD INTEG CIRCUIT	1	IC6
IC ULN2003A 4870	04870 SMD INTEG CIRCUIT	1	IC4
IND MS85 10uH-S	04948 INDUCTOR 2,7A	3	L1, L3, L6
IND T100uH-1.8A 4958	04958 TOROIDAL-STORAGE CHOKES	3	L2, L4-5
J CON HD515V/05-4PVE	02881 + 02882 PANDUIT PCB CONN	1	J1
J CON HD515V/05-6PVE	02883 + 02884 PANDUIT PCB CONN	1	J2
J FC-16P 02701-02700	02701+02700 PCB CONNECTOR POL	1	J3
R 100K-1%-S 00065B	00065B RES 1/4W 1% SMD 1206	2	R18, R20
R 100R-1%-S 00029D	00029D RES 1/4W 1% SMD 1206	3	R14-15, R25
R 10K-1%-S 00053B	00053B RES 1/4W 1% SMD 1206	4	R3, R7, R19, R26
R 10R-1%-S 00017D	00017D RES 1/4W 1% SMD 1206	4	R13, R17, R28-29
R 12K-1%-S 00054B	00054B RES 1/4W 1% SMD 1206	1	R10
R 1K0-1%-S 00041B	00041B RES 1/4W 1% SMD 1206	2	R5, R30
R 1K2-1%-S 00042A	00042A RES 1/4W 1% SMD 1206	4	R6, R8, R23, R27
R 220R-1%-S 00033C	00033C RES 1/4W 1% SMD 1206	1	R1
R 22K-1%-S 00057B	00057B RES 1/4W 1% SMD 1206	2	R9, R16
R 27K-1%-S 00058B	00058B RES 1/4W 1% SMD 1206	1	R22
R 2K2-1%-S 00045B	00045B RES 1/4W 1% SMD 1206	1	R12
R 330R-1%-S 00035A	00035A RES 1/4W 1% SMD 1206	1	R4
R 33K-1%-S 00059B	00059B RES 1/4W 1% SMD 1206	2	R11, R21
R 68K-1%-S 00063B	00063B RES 1/4W 1% SMD 1206	1	R24
R 6K8-1%-S 00051B	00051B RES 1/4W 1% SMD 1206	1	R2
RL 30.22.24 07569	07569 RELE	2	RLY1-2
TR BC856 03455	03455 PNP SMD TRANSISTOR	1	TR1

SPECIFICATION

MODEL	SP-300-27
Input voltage	88~264VAC universal input
Input current/frequency	4A/115V, 2A/230V; 47-63Hz
Inrush current	15A/115V, 30A/230V
Output voltage	27V, 11A (+/-10% ADJ.)
Overload protection	105%~135% output pulsing mode
Setup, rise, hol up time	115%~145% of output
Withstand voltage	I/P-o/P:3KV, I/P-FG: 1.5KV, 1min.
Working temp	0-40°C@100%, -10°C@80%, 50°C@50%
Safety standards	UL 1012, TUV EN60950
EMC standards	(EN55022), IEC1000-4-2~6, 8, 11, IEC1000-3-2
Connection	9P/9.5mm pitch terminal block
Weight	1.2kgs
Packing	12PCS/1CUFT
Dimensions	230x115x50mm




ELECTRONIKA s.r.l.
DESCRIPTION
TITLE
CODE
ELECTRICAL DIAGRAM
SP-300-R12
SWITCHING POWER SUPPLY
DESIGNER
PCB DESIGNER
QUALITY CONTROL
SIGNATURE
DATE 04/09/02
REF:
SHEET 1/1

COMPONENT LIST *SP-300-027*

SPECIFICATIONS	QUANTITY	POSITION
BOM FOR SP-300-27 ON CASE	1	
CASE 912A-T	1	
CASE 912B-D	1	
1206TS1;L:15cm+TUBE/TYPE:B;	1	
HS HS010-R1 S-320	2	HS4, HS5
HS HS010A SP-300	1	HS3
HS YS018W-018A-R1 7106AW-018A	1	HS3
MHS001 30mm	2	HS4, HS5
28x48 3.2	1	D11
TO220-A 11.4x21.5x5.8	1	D5
TO3P-A 17.5x28.5x5.9	3	Q1, Q10, Q6
MYLAR FILM 912-R4	1	CASE
BOX 912 244x125x66mm	1	1
SCREW F 3x4 ISO NI	2	HS3
SCREW F 3x6 ISO NI	4	HS4, HS5
SCREW F 3x15 ISO NI	3	HS3, HS4, HS5
SCREW P 3x6 ISO NI	6	PCB, RTH2
SCREW F 5.0x12 TP1 NI	2	FAN
SCREW F 3x6 TP2 NI	6	CASE
LABEL UL SP-300-27-R4	1	CASE
LABEL INDCON UL E010-R2 FAN CONT.	1	
CARTON 912 0.98CUFT	1	12
327x18mm	1	1 TB1
BOM FOR SP-300-27 ON PCB	1	
R/C 1/4W 1Ω 5% HP=10 T-52mm	1	R8
R/C 1/4W 5.1Ω 5% HP=10 T-52mm	3	R27, R29, R77
R/C 1/4W 15Ω 5% HP=10 T-52mm	1	R63
R/C 1/4W 22Ω 5% HP=10 T-52mm	1	R49
R/C 1/4W 100Ω 5% HP=10 T-52mm	2	R57, R61
R/C 1/4W 330Ω 5% HP=10 T-52mm	2	R45, R66
R/C 1/4W 680Ω 5% HP=10 T-52mm	1	R13
R/C 1/4W 1kΩ 5% HP=10 T-52mm	5	R17, R21, R47, R54, R56
R/C 1/4W 1kΩ 5% HP=10 T-52mm	1	R71
R/C 1/4W 1.8kΩ 5% HP=10 T-52mm	2	R79, R80
R/C 1/4W 2kΩ 5% HP=10 T-52mm	3	R48, R53, R55
R/C 1/4W 2.2kΩ 5% HP=10 T-52mm	2	R70, R72
R/C 1/4W 5.1kΩ 5% HP=10 T-52mm	2	R14, R22
R/C 1/4W 5.6kΩ 5% HP=10 T-52mm	1	R44
R/C 1/4W 6.2kΩ 5% HP=10 T-52mm	1	R60
R/C 1/4W 6.8kΩ 5% HP=10 T-52mm	1	R52
R/C 1/4W 10kΩ 5% HP=10 T-52mm	1	R64
R/C 1/4W 15kΩ 5% HP=10 T-52mm	1	R78

SPECIFICATIONS	QUANTITY	POSITION
R/C 1/4W 22kΩ 5% HP=10 T-52mm	2	R23, R73
R/C 1/4W 27kΩ 5% HP=10 T-52mm	1	R46
R/C 1/4W 68kΩ 5% HP=10 T-52mm	1	R18
R/C 1/4W 82kΩ 5% HP=10 T-52mm	1	R69
R/C 1/4W 270kΩ 5% HP=10 T-52mm	1	R67
R/C 1/4W 330kΩ 5% HP=10 T-52mm	1	R65
R/C 1/4W 1MΩ 5% HP=10 T-52mm	1	R31
R/C 1/2W 1.2Ω 5% T-52mm	1	R74
R/C 1/2W 2.2Ω 5% T-52mm	1	R58
R/C 1/2W 15Ω 5% T-52mm	2	R16, R68
R/C 1/2W 22Ω 5% T-52mm	1	R51
R/C 1/2W 680kΩ 5% T-52mm	1	R1
R/C 1W 27Ω 5%	2	R41, R42
R/C 1W 200kΩ 5% CFR-1WS	2	R75, R76
R/MO 2W 39Ω 5%	1	R28
R/MO 2W 100Ω 5%	2	R2, R59
R/MO 2W 1.2kΩ 5% KINK	2	R43, R50
R/MO 2W 30kΩ 5%	2	R11, R12
R/M 1/4W 22kΩ 1% T-52mm	1	R26
R/M 1/4W 24kΩ 1% T-52mm	1	R19
R/M 1W 499kΩ 1% MFR-1WS	4	R20, R24, R6, R7
R/NW 2W 0.22Ω 5%	1	R9
R/NW 2W 0.33Ω 5%	1	R10
R/NW 5W 0.68Ω 5%	2	R32, R62
R/FS 5W 10Ω 10% T=130°C	1	R25
MVR 0.3W 1kΩ 10% VP=5x2.5	1	SVR1
NTC TTC-502K P=5	1	RTH1
NTC 5kΩ 10% TSC-502	1	RTH2
MOV 0.6W 470V TNR15G471K	1	ZNR1
JUMP 1 P=10	2	J1, J2
JUMP 1 P=12.5	1	J5
JUMP 1 P=20	1	J3
C/Y2 221/250VAC 20% P=7.5 AC	1	C22
C/Y2 222/250VAC 20% P=7.5 AC	2	C41, C63
C/Y2 472/250VAC 20% P=7.5 AC	2	C3, C4
C/X2 104/250VAC 20% P=15 KNB153X	1	C2
C/X2 224/250VAC 20% P=22 KNB153X	1	C61
C/X2 474/250VAC 20% P=22 KNB153X	2	C1, C46
C/M 104/63V 10% P=5	5	C11, C12, C36, C53, C68
C/M 104/100V 10% P=5	2	C26, C65
C/M 224/63V 10% P=5	1	C38
C/M 474/50V 10% P=5	1	C51
C/C 221/1KV 10% P=5 Y5P	1	C59
C/C 331/100V 10% P=5 Y5P	1	C13

SPECIFICATIONS	QUANTITY	POSITION
C/C 331/1KV 10% P=5 Y5P	2	C31, C32
C/C 471/1KV 10% P=5 Y5P	3	C10, C48, C62
C/C 222/500V 20% P=5 Z5U	2	C39, C58
C/ML 102/100V 5% P=3	1	C47
C/ML 472/100V 5% P=3	2	C14, C49
C/ML 103/100V 5% P=3	2	C19, C66
C/ML 203/100V 5% P=5	1	C21
C/ML 473/100V 5% P=5	1	C50
C/C 101/2KV EPOXY 10% P=5 Y5P	1	C7
C/C 103/2KV EPOXY 80, -20% P=10 Y5V	1	C8
C/C 333/1KV EPOXY 20% P=10 Z5V	2	C37, C40
C/E 150u/400V 85°C 22x30 HP3	2	C5, C6
C/E 1u/50V 105°C 5x11 KM	2	C20, C45
C/E 2.2u/50V 105°C 5x11 KM	3	C54, C55, C57
C/E 47u/25V 105°C 5x11 KM	1	C60
C/E 47u/50V 105°C 6.3x11 KM	2	C43, C44
C/E 100u/35V 105°C 8x11.5 KM	1	C9
C/E 220u/25V 105°C 8x11.5 KM	2	C42, C52
C/E 470u/25V LL5K 10x16 YXG	1	C56
C/E 470u/50V LL5K 12.5x25 YXG	3	C33, C34, C35
BD 10A/600V GLASS D10XB60	1	BD1
RD 1A/50V 1N4001 T-52mm	1	D20
RD 3A/600V 1N5406 DO-201	1	D3
SFRD ESAD92-02 20A/200V TO3P	2	D11, D12
SFRD HER104 1A/300V T-52mm	5	D10, D17, D22, D25, D4
SFRD HER104 1A/300V T-52mm	1	D6
SFRD HER203 2A/200V T-52mm	2	D13, D16
SFRD HER208 2A/1KV T-52mm	1	D9
SFRD RHRP1560 15A/600V TO220	1	D5
SBD 1N5819 1A/40V T-52mm	1	D1
HIGH-SPEED DIODE 1N4148 T-52mm	5	D14, D15, D18, D19, D23
HIGH-SPEED DIODE 1N4148 T-52mm	3	D24, D7, D8
ZD 1/2W 8.9V 2% 9B3 T-52mm	1	ZD5
ZD 1W 5.1V 2% 1N4733 T-52mm	1	ZD7
ZD 1W 18V 2% 1N4746 T-52mm	4	ZD1, ZD3, ZD4, ZD6
LED GREEN 204GD-A	1	LED1
BJT 2SA1020 -2A/50V TO92M	1	Q4
BJT 2SA562Y -0.5A/-30V TO92	1	Q8
BJT 2SC1815GR 0.1A/40V TO92	3	Q2, Q3, Q9
BJT 2SC2120 0.8A/30V TO92	1	Q7
BJT 2SC2655 2A/50V TO92M	1	Q5
FET 2SK2652 6A/900V TO3P	2	Q1, Q6

SPECIFICATIONS	QUANTITY	POSITION
FET IRFP460 20A/500V TO3P	1	Q10
TRIAC BTA16-600B 16A TO220	1	TRC1
SHR 431 2.5V 2% MM1431AT	1	SHR1
RG MC7812CT 1.0A/12V TO220	1	RG1
PHOTO CNX82A PC111	1	U2
PHOTO-TRIAC MOC3022	1	U3
PWM TL3845P TI	1	U1
OP LM358 LA6358N	1	U4
CONTROL LT1249CN8	1	U5
TR109-R4 Ku130125 SP300-27	1	L1
TR110-R8 Ku130125	1	L3
LF TF360-RA ET-28 6mH	2	LF1, LF2
MT TF367-R2 ETD-39 SP-300-27	1	T1
BEAD CORE BD-001A-M4S RH 3.5x3x1.5	5	C37, C3F. C3S, C40S, C41F
BEAD CORE BD-001A-M4S RH 3.5x3x1.5	5	C41S, C4F, C4S, C63F, C63S
BEAD CORE BD-002A-M4S RH 3.5x6x1.5	5	D11A, D11A, D12A, D12A, D5A
BEAD CORE BD-002A-M4S RH 3.5x6x1.5	2	Q1D, Q6D
FUSE F6.3 L 250 5x20 G- U GFE	1	FS1
FUSE CLIP 5x20	2	FS1
TB DT-4C-B14W (1173) -09	1	TB1
WAFER 8822-02 P=2.5	1	CN1
WIRE 07#18 70mm 52Tx2	1	A-A
HS YS021W-3 72020-3 h=25m/m	1	HS2
HS YS026W-030-R1 72021W-030	1	HS1
CORE MS-130125 HKH-130	2	L1, L3
PCB SP-300-R11 FR-4 2OZ DS	1	PCB
SCREW P 3x6 ISO NI	1	TRC1
SCREW P 3x8 ISO NI	1	BD1
SCREW T 3x6 TP2 B H	1	RG1
1.0 1M (7mm)	7/1000	D5
2.0 1M (9mm)	45/1000	Q1, Q1, Q10, Q10, Q6
2.0 1M (9mm)	9/1000	Q6