

SLA30000 Series

High Speed Gate Array



- Super high-speed, and high density gate array
- Dual power supply operation
- Raw gates from 18K to 216K gates (Sea of gates)

DESCRIPTION

The SLA30000 Series is an SOG-type CMOS gate array featuring the very high-speed operations, high density, and high output drive capability. This series has a full lineup of gate arrays to cover 18,544 to 216,216 gates for the large-scale, and high-speed systems. They can drive with both +5V and +3V supply voltages.

This series also has a built-in level shifter to provide dual-power interfacing in various low-voltage applications. The I/O cells supporting the PCI Revision 2.0 are available for PCs and peripheral equipments. Also, the micro-ampere order, low-noise output cells are available for portable equipments and instruments of various applications.

FEATURES

- Super-high density (adopting 0.6 μ m silicon gate CMOS with 2 and 3-metal layers)
- High-speed operation (operation delay of internal gate = 0.25ns at 5.0V, 2-input power NAND standard)
- Selectable supply voltage: 5.0V, 3.3V, 3.0V and built-in dual-power supplies level shift circuit
- Output drivability (IOL = 100 μ , 1, 4, 8, 12 mA when PCI = 5.0V, IOL = 50 μ , 500 μ , 4, 6, 12 mA when PCI = 3.3V)
- On-chip RAM available
- I/O cells supporting the PCI Revision 2.0 and low noise output cells available

PRODUCT LINEUP

Features	Master	2-layer Metal	SLA3018	SLA3030	SLA3042	SLA3055	SLA3075	SLA3109	SLA3125	SLA3216
		3-layer Metal	SLA301T	SLA303T	SLA304T	SLA305T	SLA307T	SLA310T	SLA312T	SLA321T
Total BCs (Raw Gates)	Dual Power Supply		18,544	30,846	42,262	55,341	75,450	109,080	125,836	216,216
	Single Power Supply		23,572	37,232	49,680	63,784	85,251	120,802	138,400	232,582
Usable BCs 2-layer Metal (Dual Power Supply)	2-layer Metal		9,272	15,423	19,863	26,010	33,952	49,086	54,109	86,486
	3-layer Metal		16,318	26,219	35,077	44,272	58,851	81,810	94,377	151,351
Usable BCs 2-layer Metal (Single Power Supply)	2-layer Meta		11,786	18,616	23,349	29,978	38,362	54,360	59,512	93,032
	3-layer Metal		20,743	31,647	41,234	51,027	66,495	90,601	103,800	162,807
Number of PADs			128	160	184	208	240	256	304	376
Propagation Delay	Internal Gates	tpd = 0.25ns (standard at 5.0V), tpd = 0.33ns (standard at 3.3V)								
	Input Buffers	tpd = 0.48ns (standard at 5.0V), tpd = 0.63ns (standard at 3.3V)								
	Output Buffers	tpd = 2.08ns (standard at 5.0V), tpd = 2.86ns (standard at 3.3V) CL = 50pF								
I/O Level		CMOS, TTL, PCI								
Input Mode		TTL, CMOS, Pull-up/Pull-down, schmitt, 3.0/3.3/5.0V Level interface (Level shifter)								
Output Mode		Normal, open drain, 3-state, Bi-directional, 3.0/3.3/5.0V Level interface (Level shifter)								

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Item	Symbol	Rating	Unit
Power voltage	V _{DD}	-0.3 ~ 6.0	V
Input voltage	V _I	-0.3 to V _{DD} +0.5	V
Output voltage	V _O	-0.3 to V _{DD} +0.5	V
Output current/pin	I _{OUT}	±25(±50 ^{*1})	mA
Storage temperature	T _{stg}	-65 ~150	°C

*1: For cell of 24mA output current

■ RECOMMENDED OPERATING CONDITIONS

● Single power supply

Item	Symbol	Min.	Typ.	Max.	Unit
Power voltage	V _{DD}	2.70	3.00	3.30	V
		3.00	3.30	3.60	
		4.75	5.00	5.25	
		4.50	5.00	5.50	
Input voltage	V _I	V _{SS}	-	V _{DD}	V
Operating temperature	T _{opr}	0	25	70	°C
		-40	25	85	°C
Normal input during input rise time	t _{ri}	-	-	50	ns
Normal input during input fall time	t _{fi}	-	-	50	ns
Schmitt input during input rise time	t _{ri}	-	-	5	ms
Schmitt input during input fall time	t _{fi}	-	-	5	ms

● Dual power supply

Item	Symbol	Min.	Typ.	Max.	Unit
Power voltage (High voltage)	HV _{DD}	4.75	5.00	5.25	V
	HV _{DD}	4.50	5.00	5.50	V
Power voltage (Low voltage)	LV _{DD}	2.70	3.00	3.30	V
	LV _{DD}	3.00	3.30	3.60	V
Input voltage	HV _I	V _{SS}	-	HV _{DD}	V
	LV _I	V _{SS}	-	LV _{DD}	V
Operating temperature	T _{opr}	0	25	70	°C
		-40	25	85	°C
Normal input during input rise time	t _{ri}	-	-	50	ns
Normal input during input fall time	t _{fi}	-	-	50	ns
Schmitt input during input rise time	t _{ri}	-	-	5	ms
Schmitt input during input fall time	t _{fi}	-	-	5	ms

■ ELECTRICAL CHARACTERISTICS (VDD=5V)

(VDD = 5V, VSS = 0V, Ta = -40 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Stand-by current *	I _{DDs}	Stop position	-	-	400	μA	
Input leakage current	I _{LI}	-	-1	-	1	μA	
Off-state leakage current	I _{OZ}	-	-1	-	1	μA	
High level output voltage	V _{OH}	I _{OH} = -0.1mA (Type S), -1mA (Type M), -4mA (Type 1), -8mA (Type 2), -12mA (Type 3, 4) V _{DD} = Min.	V _{DD} -4	-	-	V	
Low level output voltage	V _{OL}	I _{OL} = 0.1mA (Type S), 1mA (Type M), 4mA (Type 1), 8mA (Type 2), 12mA (Type 3), 24mA (Type 4) V _{DD} = Min.	-	-	0.4	V	
High level input voltage	V _{IH1}	CMOS level, V _{DD} = Max.	3.5	-	-	V	
Low level input voltage	V _{IL1}	CMOS level, V _{DD} = Min.	-	-	1.0	V	
High level input voltage	V _{T1+}	CMOS Schmitt, V _{DD} = 5.0V	-	-	4.0	V	
Low level input voltage	V _{T1-}	CMOS Schmitt, V _{DD} = 5.0V	0.8	-	-	V	
Hysteresis voltage	V _{H1}	CMOS Schmitt, V _{DD} = 5.0V	0.3	-	-	V	
High level input voltage	V _{IH2}	TTL level, V _{DD} = Max.	2.0	-	-	V	
Low level input voltage	V _{IL2}	TTL level, V _{DD} = Min.	-	-	0.8	V	
High level input voltage	V _{T2+}	TTL Schmitt, V _{DD} = 5.0V	-	-	2.4	V	
Low level input voltage	V _{T2-}	TTL Schmitt, V _{DD} = 5.0V	0.6	-	-	V	
Hysteresis voltage	V _{H2}	TTL Schmitt, V _{DD} = 5.0V	0.1	-	-	V	
High level input voltage	V _{IH3}	PCI level, V _{DD} = Max.	2.0	-	-	V	
Low level input voltage	V _{IL3}	PCI level, V _{DD} = Min.	-	-	0.8	V	
High level output current	I _{OH3}	Available for PCI , V _{OH} = 1.4V, V _{DD} = Min., V _{OH} = 3.1V, V _{DD} = Max.	-44 -	- -	- -142	 mA	
Low level output current	I _{OL3}	Available for PCI , V _{OL} = 2.2V, V _{DD} = Min., V _{OL} = 0.71V, V _{DD} = Max.	95 -	- -	- 206	 mA	
Pull-up resistor	R _{PU}	V _I = 0V	Type 1 Type 2	25 50	50 100	100 200	KΩ
Pull-down resistor	R _{PD}	V _I = V _{DD}	Type 1 Type 2	25 50	50 100	100 200	
High level hold current	I _{BHH1}	Available for bus holding, V _{IN} = 3.5V (CMOS system) V _{DD} = Max.	-	-	-90	μA	
Low level hold current	I _{BHL1}	Available for bus holding, V _{IN} = 1.0V (CMOS system) V _{DD} = Max.	-	-	60	μA	
High level hold current	I _{BHH2}	Available for bus holding, V _{IN} = 2.0V (TTL system) V _{DD} = Max.	-	-	-110	μA	
Low level hold current	I _{BHL2}	Available for bus holding, V _{IN} = 0.8V (TTL system) V _{DD} = Max.	-	-	50	μA	
High level inversion current	I _{BHHO}	Available for bus holding, V _{DD} = Min.	-900	-	-	mA	
Low level inversion current	I _{BHLO}	Available for bus holding, V _{DD} = Min.	530	-	-	mA	
Input pin capacitance	C _I	f = 1MHz, V _{DD} = 0V	-	-	12	pF	
Output pin capacitance	C _O	f = 1MHz, V _{DD} = 0V	-	-	12	pF	
I/O pin capacitance	C _{IO}	f = 1MHz, V _{DD} = 0V	-	-	12	pF	

* Stand by current is a representative value of 6resy series

■ ELECTRICAL CHARACTERISTICS (V_{DD}=3V)

(V_{DD} = 3V±0.3V, V_{SS} = 0V, Ta = -40 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Stand-by current*	I _{DDs}	Stop position	-	-	260	μA	
Input leakage current	I _{LI}	-	-1	-	1	μA	
Off-state leakage current	I _{oZ}	-	-1	-	1	μA	
High level output voltage	V _{OH}	I _{OH} = -0.05mA (Type S), -0.5mA (Type M), -1.8mA (Type 1), -3.5mA (Type 2), -5mA (Type 3, 4) V _{DD} = Min.	V _{DD} -0.3	-	-	V	
Low level output voltage	V _{OL}	I _{OL} = 0.05mA (Type S), 0.5mA (Type M), 1.8mA (Type 1), 3.5mA (Type 2), 5mA (Type 3), 10mA (Type 4) V _{DD} = Min.	-	-	0.3	V	
High level input voltage	V _{IH1}	CMOS level, V _{DD} = Max.	2.0	-	-	V	
Low level input voltage	V _{IL1}	CMOS level, V _{DD} = Min.	-	-	0.8	V	
High level input voltage	V _{T1+}	CMOS Schmitt, V _{DD} = 3.0V	-	-	2.3	V	
Low level input voltage	V _{T1-}	CMOS Schmitt, V _{DD} = 3.0V	0.5	-	-	V	
Hysteresis voltage	V _{H1}	CMOS Schmitt, V _{DD} = 3.0V	0.1	-	-	V	
High level input voltage	V _{IH3}	PCI level, V _{DD} = Max.	1.58	-	-	V	
Low level input voltage	V _{IL3}	PCI level, V _{DD} = Min.	-	-	0.88	V	
High level output current	I _{OH3}	Available for PCI, V _{OH} = 0.81V, V _{DD} = Min., V _{OH} = 2.31V, V _{DD} = Max.	-33 -	-	- -105	mA mA	
Low level output current	I _{OL3}	Available for PCI, V _{OL} = 1.62V, V _{DD} = Min., V _{OL} = 0.60V, V _{DD} = Max.	44 -	-	- 125	mA mA	
Pull-up resistor	R _{PU}	V _I = 0V	Type 1	50	100	200	KΩ
			Type 2	100	200	400	
Pull-down resistor	R _{PD}	V _O = V _{DD}	Type 1	50	100	200	KΩ
			Type 2	100	200	400	
High level hold current	I _{BHH}	Available for bus holding, V _{IN} = 2.0V V _{DD} = Max.	-	-	-32	μA	
Low level hold current	I _{BHL}	Available for bus holding, V _{IN} = 0.8V V _{DD} = Max.	-	-	27	μA	
High level inversion current	I _{BHHO}	Available for bus holding, V _{DD} = Min.	-290	-	-	mA	
Low level inversion current	I _{BHLO}	Available for bus holding, V _{DD} = Min.	170	-	-	mA	
Input pin capacitance	C _I	f = 1MHz, V _{DD} = 0V	-	-	12	pF	
Output pin capacitance	C _O	f = 1MHz, V _{DD} = 0V	-	-	12	pF	
I/O pin capacitance	C _{IO}	f = 1MHz, V _{DD} = 0V	-	-	12	pF	

* Stand by current is a representative value of eresy series

■ ELECTRICAL CHARACTERISTICS (VDD=3.3V)

(VDD = 3.3V±0.3V, VSS = 0V, Ta = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Stand-by current*	I _{DDs}	Stop position	-	-	290	μA	
Input leakage current	I _{LI}	-	-1	-	1	μA	
Off-state leakage current	I _{OZ}	-	-1	-	1	μA	
High level output voltage	V _{OH}	I _{OH} = -0.05mA (Type S), -0.5mA (Type M), -2mA (Type 1), -4mA (Type 2), -6mA (Type 3, 4) V _{DD} = Min.	V _{DD} -0.3	-	-	V	
Low level output voltage	V _{OL}	I _{OL} = 0.05mA (Type S), 0.5mA (Type M), 2mA (Type 1), 4mA (Type 2), 6mA (Type 3), 12mA (Type 4) V _{DD} = Min.	-	-	0.3	V	
High level input voltage	V _{IH1}	CMOS level, V _{DD} = Max.	2.2	-	-	V	
Low level input voltage	V _{IL1}	CMOS level, V _{DD} = Min.	-	-	0.8	V	
High level input voltage	V _{T1+}	CMOS Schmitt, V _{DD} = 3.3V	-	-	2.4	V	
Low level input voltage	V _{T1-}	CMOS Schmitt, V _{DD} = 3.3V	0.6	-	-	V	
Hysteresis voltage	V _{H1}	CMOS Schmitt, V _{DD} = 3.3V	0.1	-	-	V	
High level input voltage	V _{IH3}	PCI level, V _{DD} = Max.	1.71	-	-	V	
Low level input voltage	V _{IL3}	PCI level, V _{DD} = Min.	-	-	0.98	V	
High level output current	I _{OH3}	Available for PCI, V _{OH} = 0.90V, V _{DD} = Min., V _{OH} = 2.52V, V _{DD} = Max.	-36 -	- -	- -115	mA mA	
Low level input current	I _{OL3}	Available for PCI, V _{OL} = 1.8V, V _{DD} = Min., V _{OL} = 0.65V, V _{DD} = Max.	48 -	- -	- 137	mA mA	
Pull-up resistor	R _{PU}	V _I = 0V	Type 1	45	90	180	KΩ
			Type 2	90	180	360	
Pull-down resistor	R _{PD}	V _I = V _{DD}	Type 1	45	90	180	KΩ
			Type 2	100	200	360	
High level hold current	I _{BHH}	Available for bus holding, V _{IN} = 2.0V V _{DD} = Max.	-	-	-40	μA	
Low level hold current	I _{BHL}	Available for bus holding, V _{IN} = 0.8V V _{DD} = Max.	-	-	30	μA	
High level inversion current	I _{BHHO}	Available for bus holding, V _{DD} = Min.	-350	-	-	μA	
Low level inversion current	I _{BHLO}	Available for bus holding, V _{DD} = Min.	210	-	-	μA	
Input pin capacitance	C _I	f = 1MHz, V _{DD} = 0V	-	-	12	pF	
Output pin capacitance	C _O	f = 1MHz, V _{DD} = 0V	-	-	12	pF	
I/O pin capacitance	C _{IO}	f = 1MHz, V _{DD} = 0V	-	-	12	pF	

* Stand by current is a representative value of eryl series

■ ELECTRICAL CHARACTERISTICS (Stand-by Current)

● Single power supply (Ta= -40 to 85°C)

Master	5V±10% I _{DDs} Max.	3.3V±0.3V I _{DDs} Max.	3.0V±0.3V I _{DDs} Max.	Unit
SLA3018/301T	300	220	200	μA
SLA3030/303T				
SLA3042/304T				
SLA3055/305T	400	290	260	μA
SLA3075/307T				
SLA3109/310T				
SLA3125/312T	600	430	400	μA
SLA3216/321T				

● Dual power supply (Ta= -40 to 85°C)

Master	5V±10% H _I DDs Max.	3.3V±0.3V L _I DDs Max.	5V±10% H _I DDs Max.	3.0V±0.3V L _I DDs Max.	Unit
SLA3018/301T	80	220	80	200	μA
SLA3030/303T					
SLA3042/304T					
SLA3055/305T	100	290	100	260	μA
SLA3075/307T					
SLA3109/310T					
SLA3125/312T	160	430	160	400	μA
SLA3216/321T					

H_IDDs: Stand-by current between HV_{DD} and V_{SS}.

L_IDDs: Stand-by current between LV_{DD} and V_{SS}.

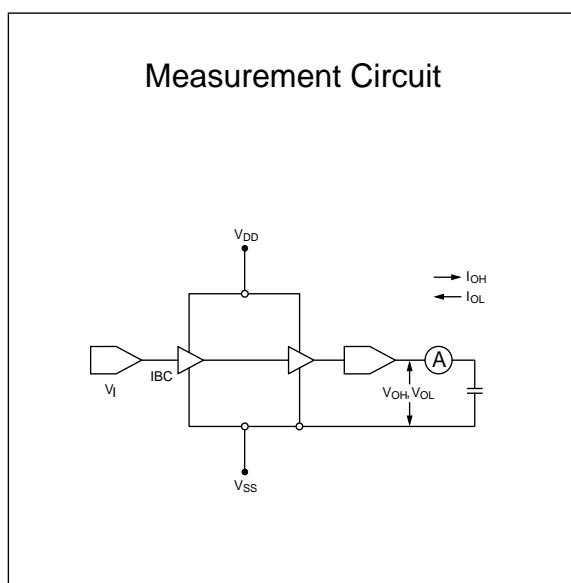
- In case of dual power supply, total stand-by current is the sum of H_IDDs and L_IDDs.

■ CHARACTERISTICS CURVES (V_{DD}=5V)

● Output Current Characteristics (5.0V±10%)

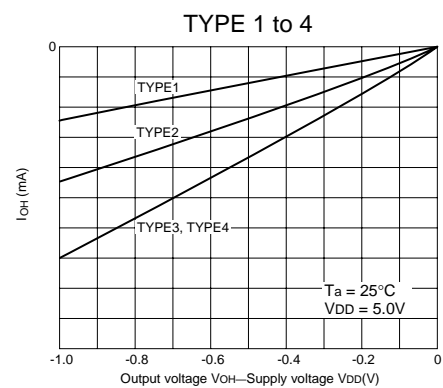
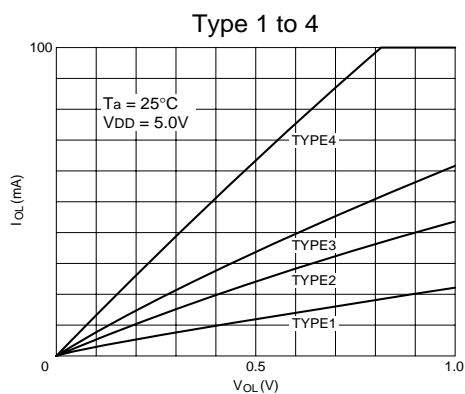
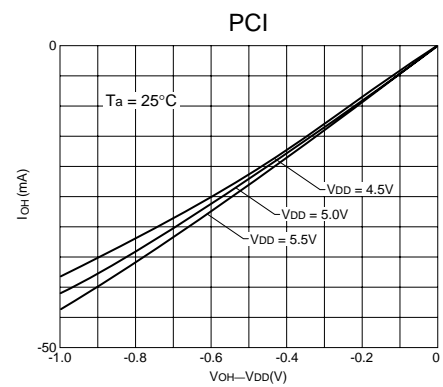
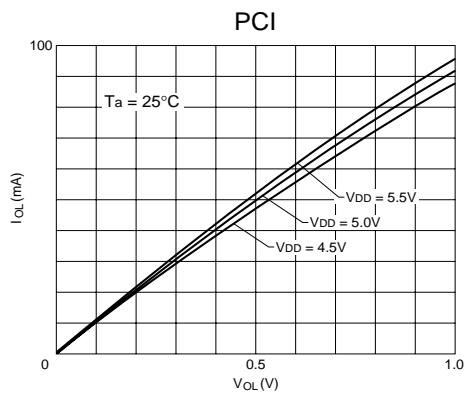
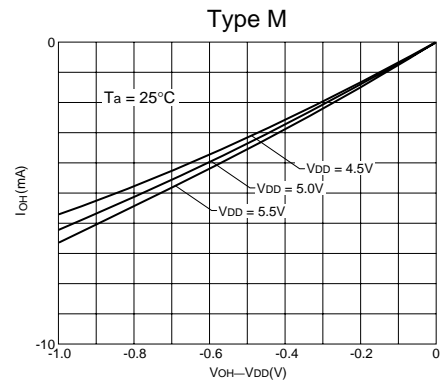
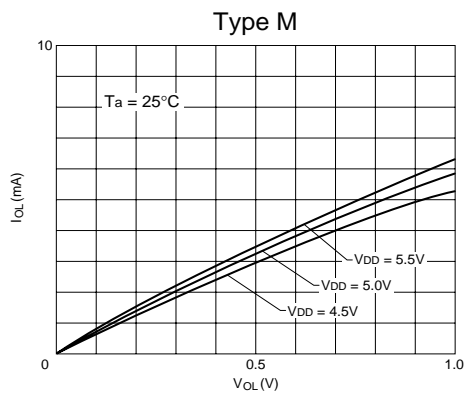
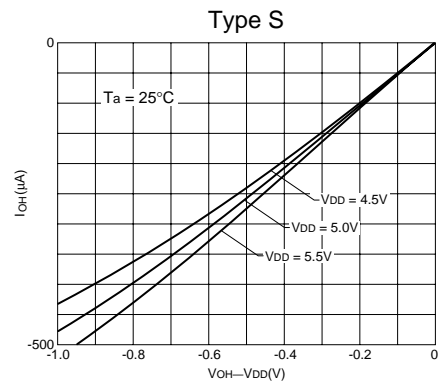
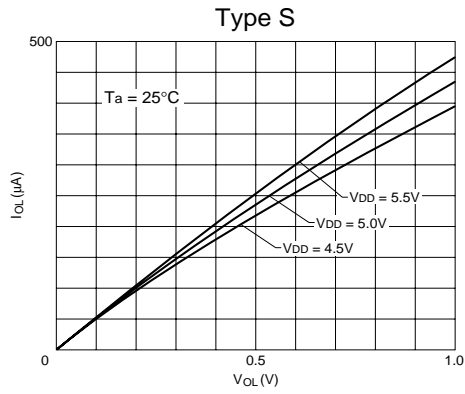
Type number	Output Current	
	I _{OH} (mA)	I _{OL} (mA)
TypeS	-0.1	0.1
TypeM	-1	1
Type1	-4	4
Type2	-8	8
Type3	-12	12
Type4	-12	24
PCI	Conforms to PCI standard.	

Letters S, M and 1 to 4 of "Type*" represent the numbers used for the output cell name (in format of "XX□X").



Low level output current

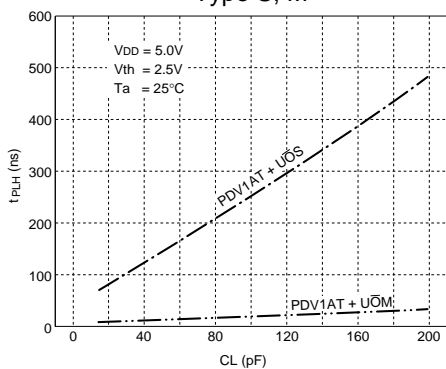
High level output current



● t_{pd}, t_r, t_{f-CL}

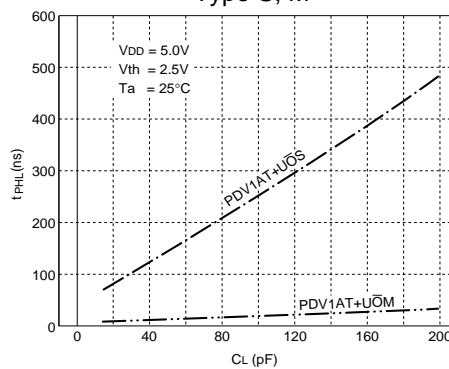
t_{PLH} vs. CL

Type S, M

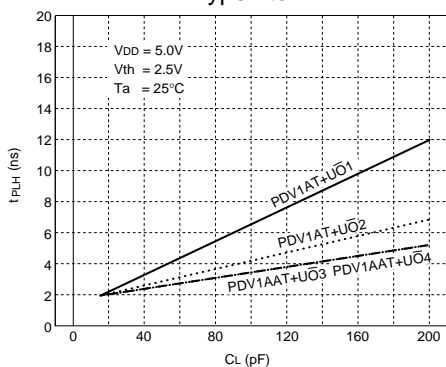


t_{PHL} vs. CL

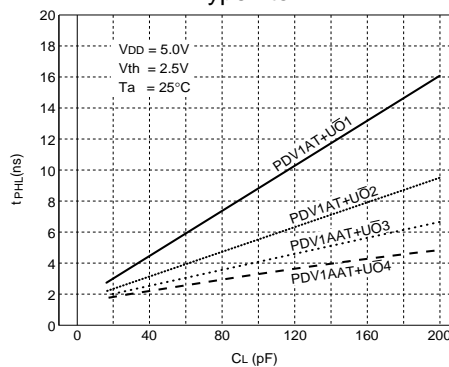
Type S, M



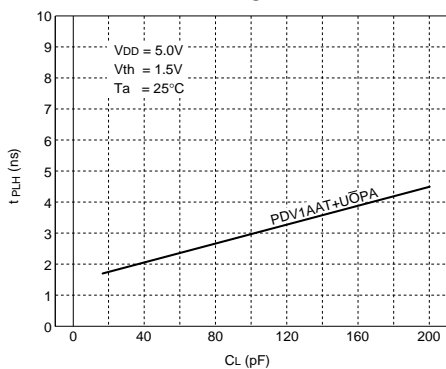
Type1 to 4



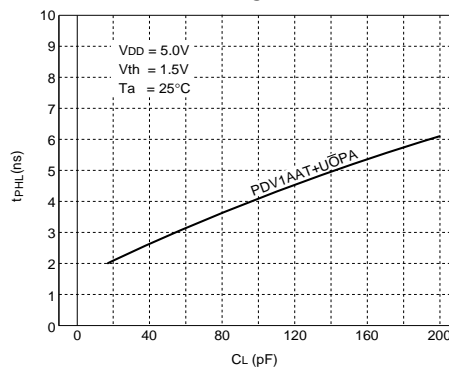
Type1 to 4



PCI



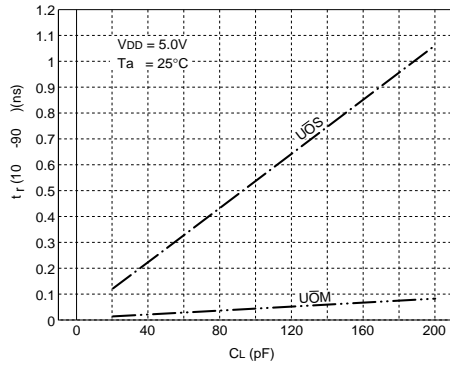
PCI



● tpd, tr, tf-CL

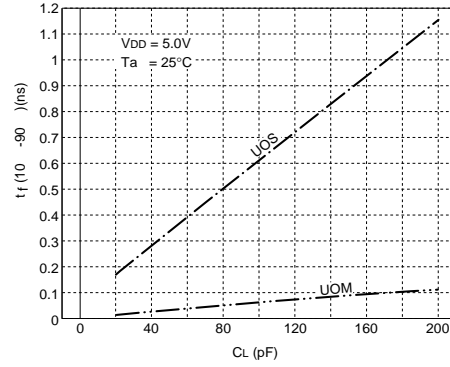
tr vs. CL

Type S, M

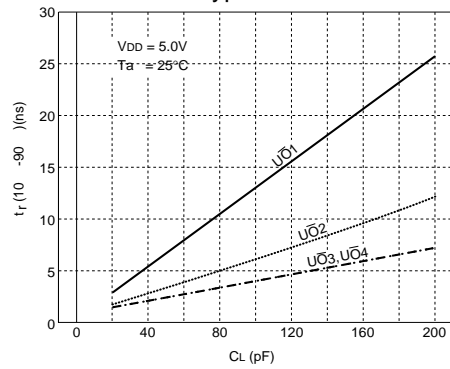


tf vs. CL

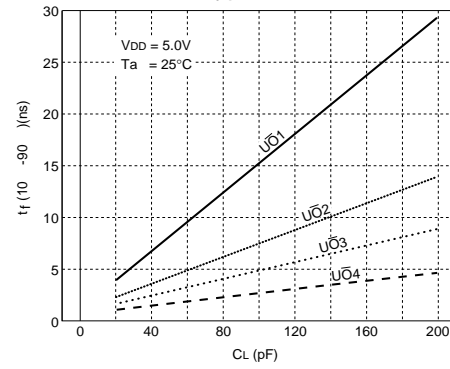
Type S, M



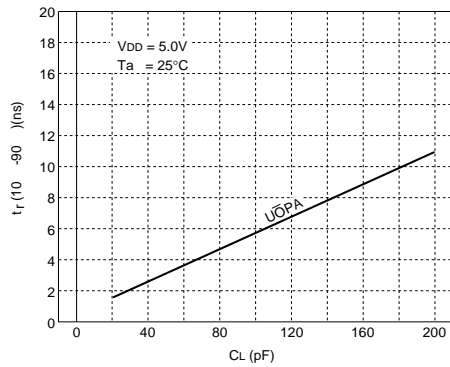
Type1 to 4



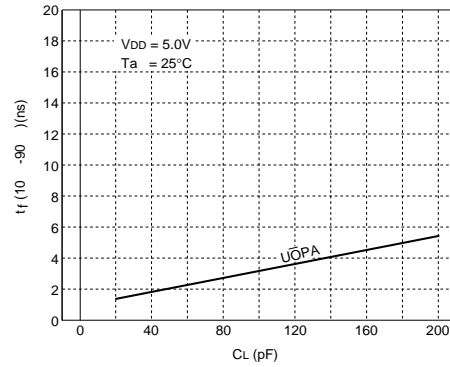
Type1 to 4



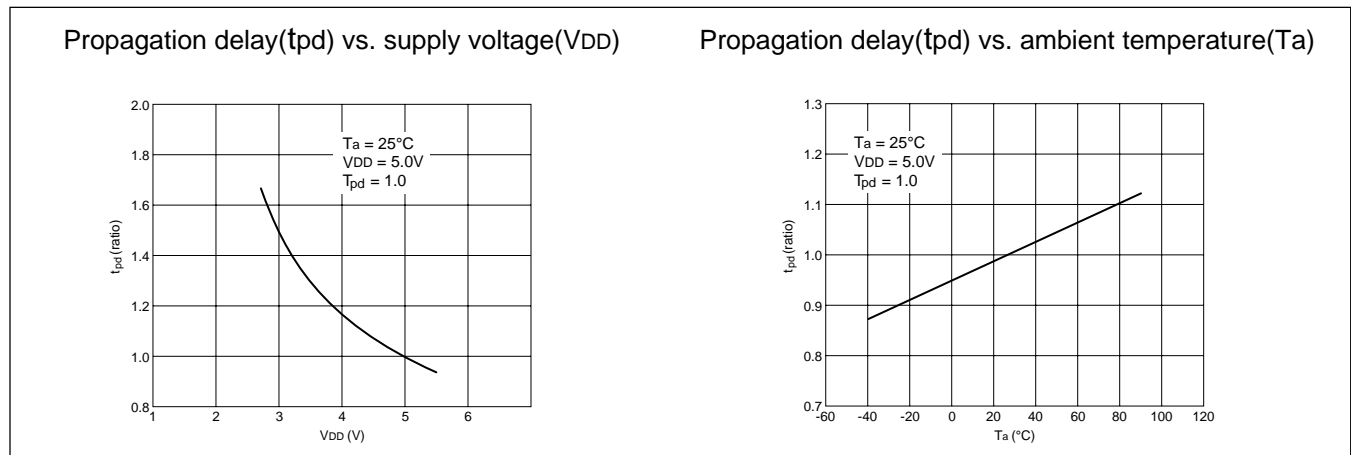
PCI



PCI



● Delay Time



■ CHARACTERISTICS CURVES ($V_{DD}=3.3V$)

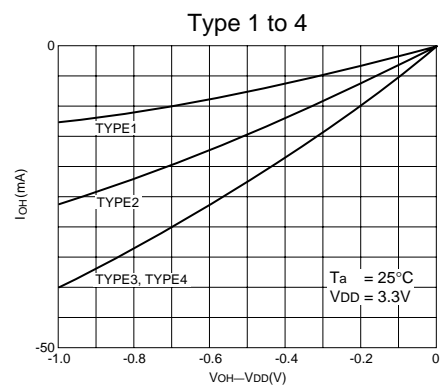
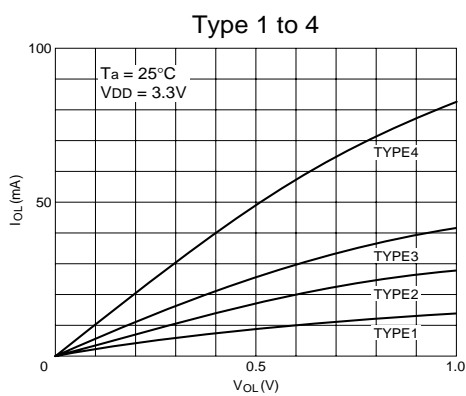
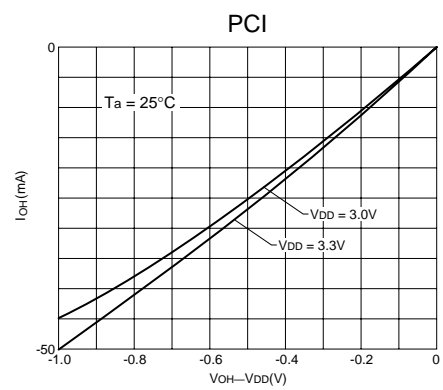
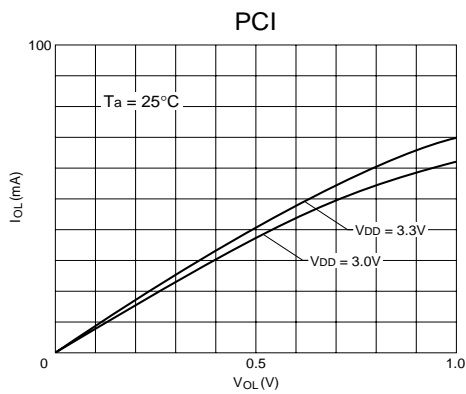
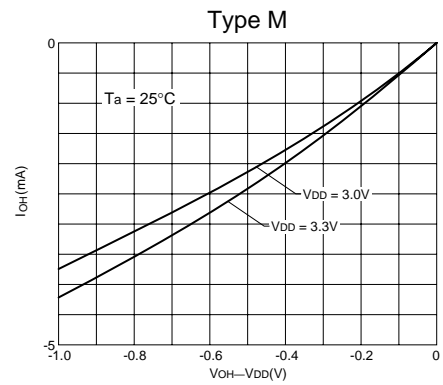
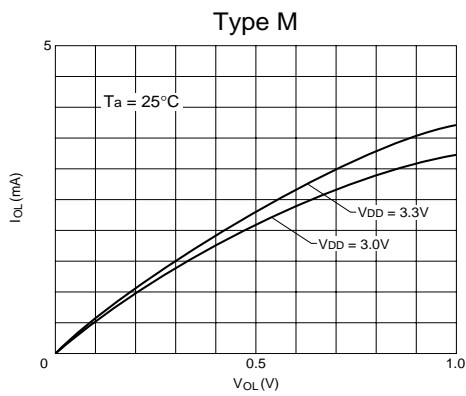
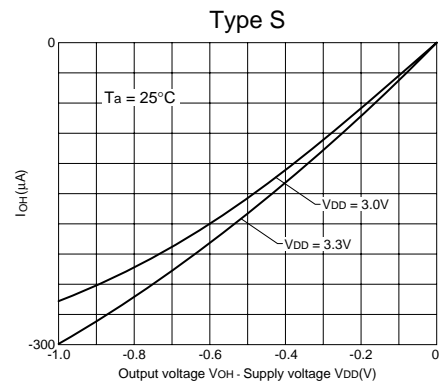
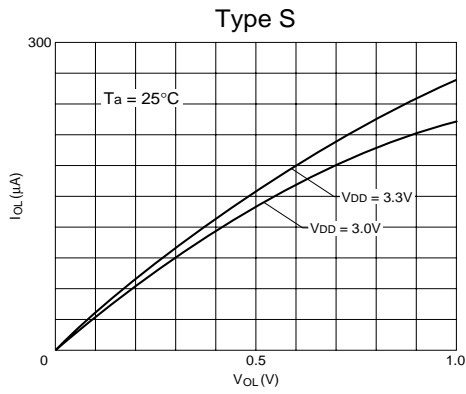
● Output Current ($3.3V \pm 0.3V$)

Type number	Output Current	
	I_{OH} (mA)	I_{OL} (mA)
TypeS	-0.05	0.05
TypeM	-0.5	0.5
Type1	-2	2
Type2	-4	4
Type3	-6	6
Type4	-6	12
PCI	Conforms to PCI standard.	

Letters S, M and 1 to 4 of "Type*" represent the numbers used for the output cell name (in format of "XX□X").

Low level output current

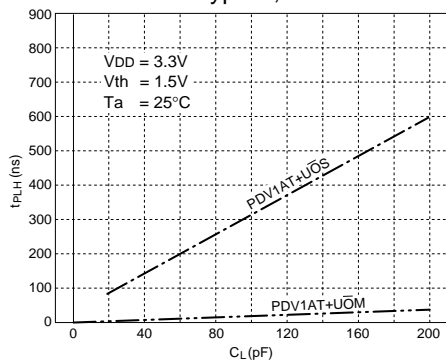
High level output current



● tpd, tr, tf-CL

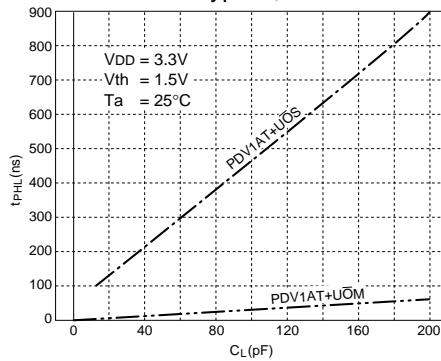
tpLH vs. CL

Type S, M

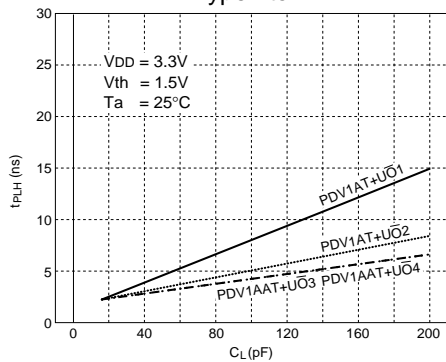


tpHL vs. CL

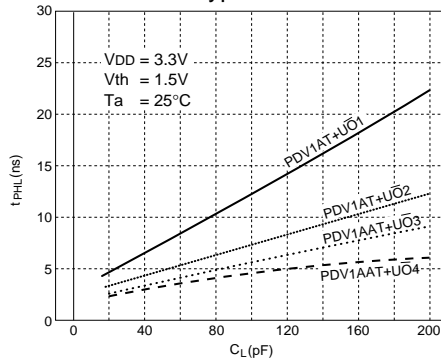
Type S, M



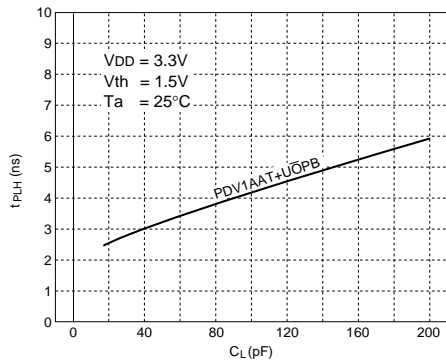
Type1 to 4



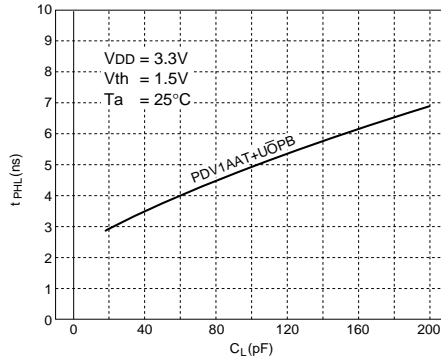
Type1 to 4



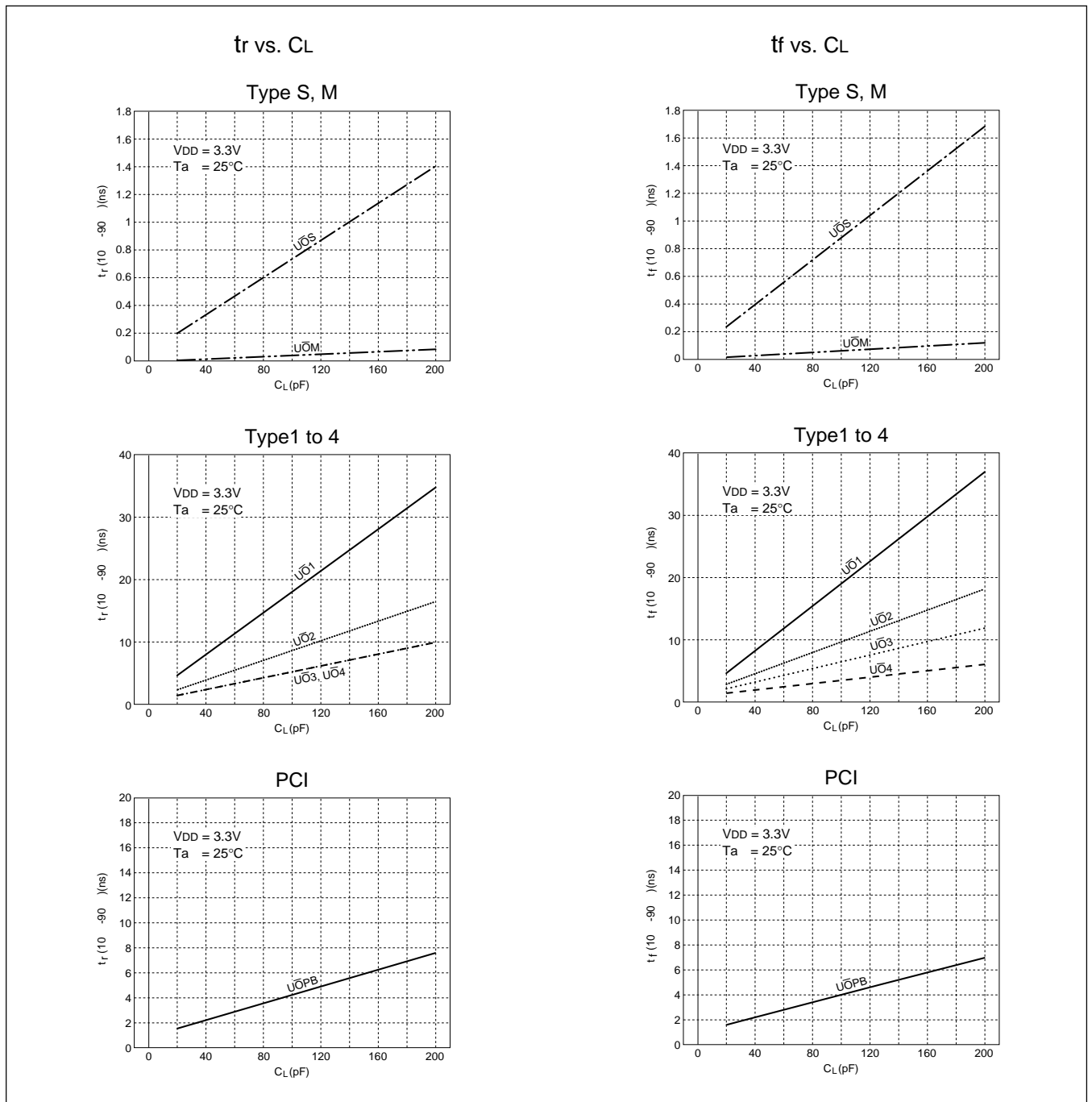
PCI



PCI



● tpd, tr, tf-CL



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