Fibocom

Perfect Wireless Experience
完美无线体验

L850-GL Hardware User Manual

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Version Record

Version	Update date	Remark
V1.0.0	2016-12-08	Draft
V1.0.1	2016-12-16	Modify the PCIe Interface Application; Update the Pin Definition: change pin65 to NC
V1.0.2	2017-02-09	Modify the description Update the content of PCIe Add the power Consumption of 3CA
V1.0.3	2017-07-26	1. Update timing of power on/off and reset 2. Update PCIe, add USB support 3. Update power consumption, TX power, RX sensitivity and other data
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V1.0.6	2018-2-26	1. Modify COEX pin define 2. Del L850-GL-02 product model

Applicability Table

No.	Product model	Description
1	L850-GL-00	NA
2	L850-GL-01	NA
3	L850-GL-03	NA
4	L850-GL-05	NA
5	L850-GL-10	NA

Contents

1 Foreword

1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of L850-GL (hereinafter referred to as L850). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of L850 modules and develop products.

1.2 Reference Standard

The design of the product complies with the following standards:

- 3GPP TS 34.121-1 V8.11.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD);Part 1: Conformance specification
- 3GPP TS 34.122 V11.13.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V11.4.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI Express M.2 Specification Rev1.1

1.3 Related Documents

- RF Antenna Application Design Specification
- L8-Family System Driver Integration and Application Guidance
- L8-Family AT Commands Manual

2 Overview

2.1 Introduction

L850 is a highly integrated 4G WWAN module which uses M.2 form factor interface. It supports LTE FDD/LTE TDD/WCDMA systems and can be applied to most cellular networks of mobile carrier in the world.

2.2 Specification

Specification		
Operating Band	LTE FDD: Band 1, 2, 3, 4, 5, 7, 8, 11, 12, 13, 17, 18, 19, 20, 21, 26, 28, 29, 30, 66	
	LTE TDD: Band 38, 39, 40, 41	
	WCDMA/HSPA+: Band 1, 2, 4, 5, 8	
	GNSS/Beidou: support	
Data Transmission	LTE FDD	450Mbps DL/50Mbps UL(Cat 9)
	LTE TDD	347Mbps DL/30Mbps UL(Cat 9) When LTE TDD achieves maximum DL rate, its UL rate can reach 10Mbps only
	UMTS/HSPA+	UMTS: 384 kbps DL/384 kbps UL
		DC-HSPA+: 42Mbps DL(Cat 24)/5.76Mbps UL(Cat6)
Power Supply	DC 3.135V～4.4V, Typical 3.3V	
Temperature	Normal operating temperature: -10°C ～+55°C	
	Extended operating temperature: -20°C ～+65°C	
	Storage temperature: -40°C ～+85°C	
Physical characteristics	Interface: M.2 Key-B	
	Dimension：30 x 42 x 2.3mm	
	Weight: About 5.8 g	
Interface		
Antenna Connector	WWAN Main Antenna x 1	
	WWAN Diversity Antenna x 1	
Function Interface	USIM 3V/1.8V	

Specification	
	PCIe 1.0 X1
	USB 2.0
	USB 3.0(Base on Linux)
	W_Disable#
	Body Sar
	LED
	Clock
	Tunable antenna
	I2S(Reserved)
	I2C(Reserved)

Software	
Protocol Stack	IPV4/IPV6
AT commands	3GPP TS 27.007 and 27.005
Firmware update	PCIe
Other feature	Multiple carrier
	Windows MBIM support
	Windows update
	AGNSS

Note:

When temperature goes beyond normal operating temperature range of -10°C~+55°C, RF performance of module may be slightly off 3GPP specifications. For normal operating temperature, LTE FDD Band 4 and 13 can support temperature ranging from -20℃ to +60℃.

2.3 Warning

2.3.1 FCC Statement

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
-

FCC Caution:

➢ Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

➢ This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

➢

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the maximum antenna gain allowed for use with this device is 5 dBi.
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "**Contains FCC ID: ZMOL850GLD-D1**". The grantee's FCC ID can be used

only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

2.3.2 IC Statement

Industry Canada statement

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

1) this device may not cause interference, and

2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1) l'appareil ne doit pas produire de brouillage, et

2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

This device complies with RSS-310 of Industry Canada. Operation is subject to the condition that this device does not cause harmful interference.

Cet appareil est conforme à la norme RSS-310 d'Industrie Canada. L'opération est soumise à la condition que cet appareil ne provoque aucune interférence nuisible.

This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter, except tested built-in radios.

Cet appareil et son antenne ne doivent pas être situés ou fonctionner en conjonction avec une autre antenne ou un autre émetteur, exception faites des radios intégrées qui ont été testées.

The County Code Selection feature is disabled for products marketed in the US/ Canada.

La fonction de sélection de l'indicatif du pays est désactivée pour les produits commercialisés aux États-Unis et au Canada.

Radiation Exposure Statement:

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

IC : 21374-L850GLD

2.3.3 CE Statement

▸ EU Regulatory Conformance

Hereby, We, Fibocom Wireless Inc. declares that the radio equipment type L850-GL is in compliance with the Directive 2014/53/EU.

In all cases assessment of the final product must be mass against the Essential requirements of the Directive 2014/53/EU Articles 3.1(a) and (b), safety and EMC respectively, as well as any relevant Article3.2 requirements.

The maximum antenna gain for is 5 dBi and the antenna separation distance is 20cm.

► Declaration of Conformity(should include manufacturer contact info.)

Please added certification standard in your user manual which depended on the test standards your device performed., If the DoC should be a simplified version, please take below as reference, The full text of the EU declaration of conformity is available at the following internet address: http//www.

2.4 CA combinations

CA Combinations		
2CA	Inter-band	1+3, 5, 8, 11, 18, 19, 20, 21, 26
		2+4, 5, 12, 13, 17, 29, 30, 66
		3+5, 7, 8, 19, 20, 28
		4+5, 12, 13, 17, 29, 30
		5+7, 30, 66
		7+20, 28
		8+11
		12+30
		13+66
		29+30
	Intra-band(non-contiguous)	2, 3, 4, 7, 41
	Intra-band(contiguous)	2, 3, 7, 40, 41
3CA	Inter-band	1+3+7, 1+3+8，1+3+19, 1+3+20, 1+3+28, 1+7+20, 1+7+28, 1+8+11, 1+19+21
		2+4+5, 2+4+13, 2+5+30, 2+12+30, 2+29+30, 2+5+66, 2+13+66
		3+7+20, 3+7+28
		4+5+30, 4+12+30, 4+29+30
	2 intra-band(non-contiguous) plus inter-band	2+2+5, 2+2+13
		4+4+5, 4+4+13
	2 intra-band(contiguous) plus inter-band	2+2+29
		3+3+1, 3+3+5, 3+3+7, 3+3+20, 3+3+28
		2+66+66, 5+66+66, 13+66+66
		7+7+3, 7+7+28
	Intra-band(non-contiguous)	41, 66
	Intra-band(contiguous)	40, 41, 66

2.5 Application Framework

The peripheral applications for L850 module are shown in Figure 2-1:
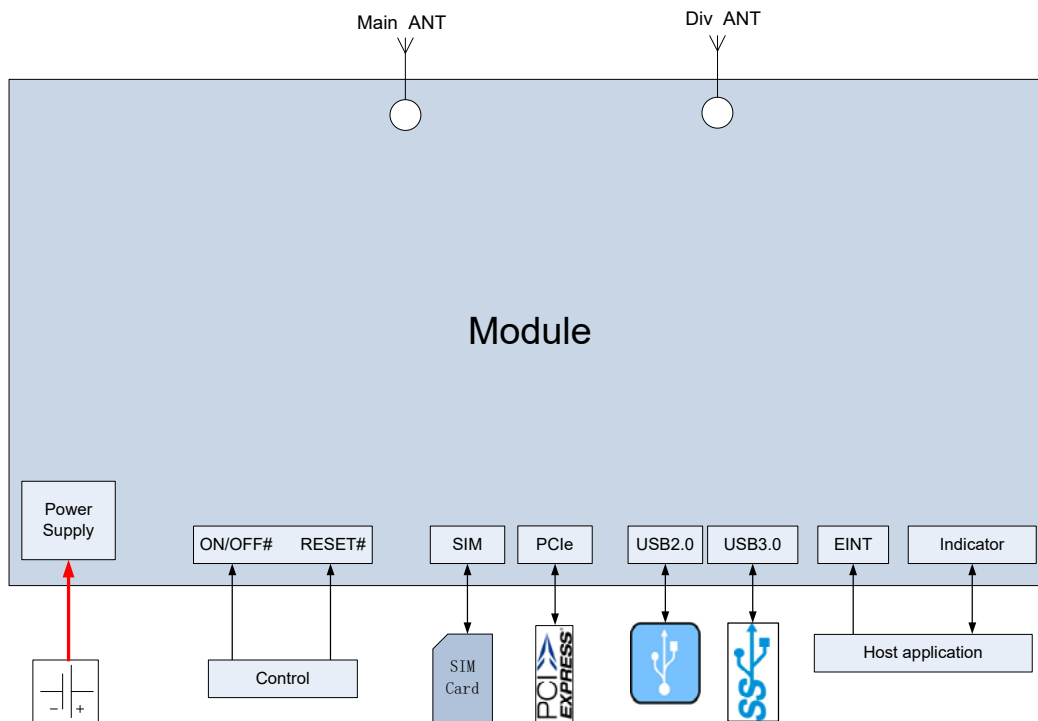
Figure2-1 Application Framework

2.6 Hardware Block Diagram

The hardware block diagram in Figure 2-2 shows the main hardware functions of L850 module, including base band and RF functions.

Baseband contains the followings:

- GSM/UMTS/LTE FDD controller/Power supply
- NAND/internal LPDDR2 RAM
- Application interface

RF contains the followings:

- RF Transceiver
- RF Power/PA
- RF Front end
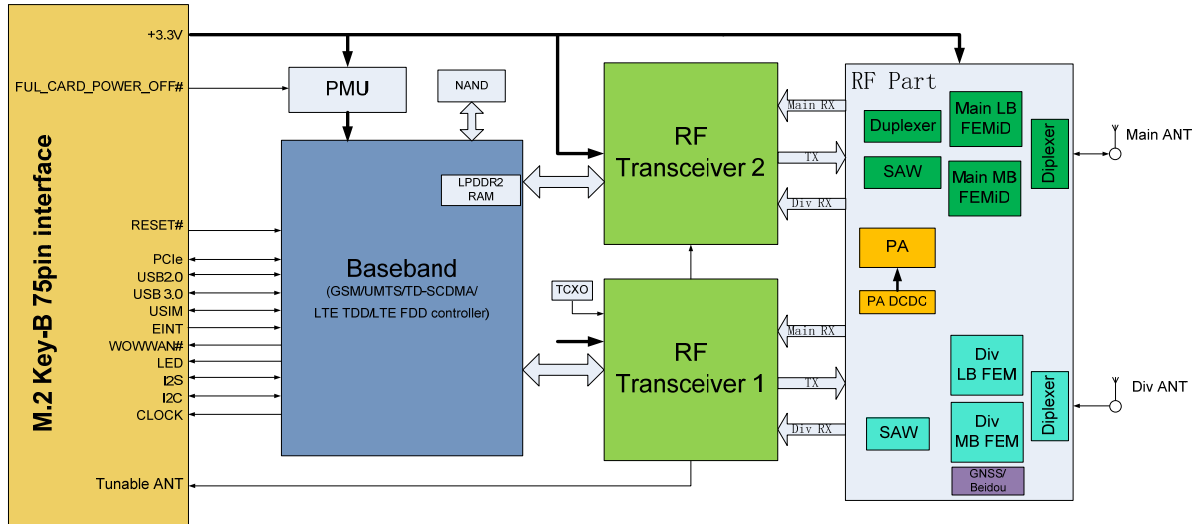- RF Filter
- Antenna Connector

Figure 2-2 Hardware Block Diagram

![Fibocom logo]

3 Application Interface

3.1 M.2 Interface

The L850 module applies standard M.2 Key-B interface, with a total of 75 pins.

3.1.1 Pin Map

74	+3.3V		CONFIG_2	75
72	+3.3V		GND	73
70	+3.3V		GND	71
68	NC		CONFIG_1	69
66	SIM_DETECT(1.8V)		RESET#(1.8V)	67
64	COEX_TXD(1.8V)		NC	65
62	COEX_RXD(1.8V)		ANTCTL2(1.8V)	63
60	COEX3(1.8V)		ANTCTL1(1.8V)	61
58	RFE_RFFE2_SDATA(3.3/1.8V)		ANTCTL0(1.8V)	59
56	RFE_RFFE2_SCLK(3.3/1.8V)		GND	57
54	PEWAKE# (3.3V)		REFCLKP	55
52	CLKREQ# (3.3V)		REFCLKN	53
50	PERST# (3.3V)		GND	51
48	TX_BLANKING(1.8V)		PERp0	49
46	SYSCLK(1.8V)		PERn0	47
44	GNSS_IRQ(1.8V)		GND	45
42	GNSS_SDA(1.8V)		PETp0	43
40	GNSS_SCL(1.8V)		PETn0	41
38	NC		GND	39
36	UIM_PWR		USB3.0_RX+	37
34	UIM_DATA		USB3.0_RX-	35
32	UIM_CLK		GND	33
30	UIM_RESET		USB3.0_TX+	31
28	I2S_WA(1.8V)		USB3.0_TX-	29
26	W_DISABLE2#(3.3/1.8V)		GND	27
24	I2S_TX(1.8V)		DPR(3.3/1.8V)	25
22	I2S_RX(1.8V)		WOWWAN#(1.8V)	23
20	I2S_CLK(1.8V)		CONFIG_0	21
	Notch		Notch	
	Notch		Notch	
	Notch		Notch	
	Notch		Notch	
	Notch		GND	11
10	LED1#(3.3V OD)		USB D-	9
8	W_DISABLE1#(3.3/1.8V)		USB D+	7
6	FULL_CARD_POWER_OFF#(3.3/1.8V)		GND	5
4	+3.3V		GND	3
2	+3.3V		CONFIG_3	1

Figure 3-1 Pin Map

⚠ **Note:**

Pin "Notch" represents the gap of the gold fingers.

3.1.2 Pin Definition

The pin definition is as follows:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
1	CONFIG_3	O	NC	NC, L850 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	
2	+3.3V	PI		Power input	Power Supply
3	GND			GND	Power Supply
4	+3.3V	PI		Power input	Power Supply
5	GND			GND	Power Supply
6	FULL_CARD_ POWER_OFF#	I	PU	Power enable, Module power on input, internal pull up	CMOS 3.3/1.8V
7	USB D+	I/O		USB Data Plus	0.3---3V
8	W_DISABLE1#	I	PD	WWAN Disable, active low	CMOS 3.3/1.8V
9	USB D-	I/O		USB Data Minus	0.3---3V
10	LED1#	O	T	System status LED, Output open drain, CMOS 3.3V	CMOS 3.3V
11	GND			GND	Power Supply
12	Notch			Notch	
13	Notch			Notch	
14	Notch			Notch	
15	Notch			Notch	
16	Notch			Notch	
17	Notch			Notch	
18	Notch			Notch	
19	Notch			Notch	
20	I2S_CLK	O	PD	I2S Serial clock, Reserved	CMOS 1.8V
21	CONFIG_0		GND	GND, L850 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
22	I2S_RX	I	PD	I2S Serial receive data, Reserved	CMOS 1.8V
23	WOWWAN#	O	PD	Wake up host, Reserved	CMOS 1.8V
24	I2S_TX	O	PD	I2S Serial transmit data, Reserved	CMOS 1.8V
25	DPR	I	PU	Body SAR Detect, active low	CMOS 3.3/1.8V
26	W_DISABLE2#	I	PU	GNSS disable, active low, Reserved	CMOS 3.3/1.8V
27	GND			GND	Power Supply
28	I2S_WA	O	PD	I2S Word alignment/select, Reserved	CMOS 1.8V
29	USB3.0_TX-	O		USB3.0 Transmit data minus	
30	UIM_RESET	O	L	SIM reset signal	1.8V/3V
31	USB3.0_TX+	O		USB3.0 Transmit data plus	
32	UIM_CLK	O	L	SIM clock Signal	1.8V/3V
33	GND			GND	电源
34	UIM_DATA	I/O	L	SIM data input/output	1.8V/3V
35	USB3.0_RX-	I		USB3.0 receive data minus	
36	UIM_PWR	O		SIM power supply, 3V/1.8V	1.8V/3V
37	USB3.0_RX+	I		USB3.0 receive data plus	
38	NC			NC	
39	GND			GND	Power Supply
40	GNSS_SCL	O	PU	I2C Serial clock, Reserved	CMOS 1.8V
41	PETn0	O		PCIe TX Differential signals Negative	
42	GNSS_SDA	I/O	PU	I2C Serial data input/output, Reserved	CMOS 1.8V
43	PETp0	O		PCIe TX Differential signals Positive	
44	GNSS_IRQ	I	PD	GNSS Interrupt Request, Reserved	CMOS 1.8V
45	GND			GND	Power Supply

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
46	SYSCLK	O	PD	26M clock output	1.8V
47	PERn0	I		PCIe RX Differential signals Negative	
48	TX_BLANKING	O	PD	PA Blanking Timer, Reserved	CMOS 1.8V
49	PERp0	I		PCIe RX Differential signals Positive	
50	PERST#	I	T	Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	CMOS 3.3V
51	GND			GND	Power Supply
52	CLKREQ#	O	T	Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, internal pull up(10KΩ)	CMOS 3.3V
53	REFCLKN	I		PCIe Reference Clock signal Negative	
54	PEWAKE#	O	L	Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up on platform	CMOS 3.3V
55	REFCLKP	I		PCIe Reference Clock signal Positive	
56	RFE_RFFE2_ SCLK	O		MIPI Interface Tunable ANT, RFFE2 clock, Open Drain output	CMOS 3.3/1.8V
57	GND			GND	Power Supply
58	RFE_RFFE2_ SDATA	O		MIPI Interface Tunable ANT, RFFE2 data, Open Drain output	CMOS 3.3/1.8V
59	ANTCTL0	O		Tunable ANT CTRL0	CMOS 1.8V
60	COEX3	I/O	PD	Wireless Coexistence between WWAN and WiFi/BT modules, based on BT-SIG	CMOS 1.8V

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
				coexistence protocol. COEX_EXT_FTA, Reserved	
61	ANTCTL1	O	-	Tunable ANT CTRL1	CMOS 1.8V
62	COEX_RXD	I	T	Wireless Coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART receive signal(WWAN module side), Reserved	CMOS 1.8V
63	ANTCTL2	O	-	Tunable ANT CTRL2	CMOS 1.8V
64	COEX_TXD	O	T	Wireless Coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART transmit signal(WWAN module side), Reserved	CMOS 1.8V
65	NC			NC	
66	SIM_DETECT	I	PD	SIM Detect, internal pull up(390KΩ), active high	CMOS 1.8V
67	RESET#	I		WWAN reset input, internal pull up(10KΩ), active low	CMOS 1.8V
68	NC			NC	
69	CONFIG_1	O	GND	GND, L850 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	
70	+3.3V	PI		Power input	Power Supply
71	GND			GND	Power Supply
72	+3.3V	PI		Power input	Power Supply
73	GND			GND	Power Supply
74	+3.3V	PI		Power input	Power Supply
75	CONFIG_2	O	GND	GND, L850 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	

Reset Value: The initial status after module reset, not the status when working.

H: High Voltage Level

L: Low Voltage Level

PD: Pull-Down

PU: Pull-Up

T: Tristate

OD: Open Drain

PP: Push-Pull

PI: Power Input

PO: Power Output

⚠️ **Note:**

The unused pins can be left floating.

3.2 Power Supply

The power interface of L850 module as shown in the following table:

Pin	Pin Name	I/O	Pin Description	DC Parameter（V）		
				Minimum Value	Typical Value	Maximum Value
2, 4, 70, 72, 74	+3.3V	PI	Power supply input	3.135	3.3	4.4
36	UIM_PWR	PO	USIM power supply	-	1.8V/3V	-

L850 module uses PCIe interface, according to the PCIe specification, the PCIe Vmain should be used as the +3.3V power source, not the Vaux. The Vaux is the PCIe backup power source and it is not sufficient as the power supply. In addition, the DC/DC power supply other than PCIe ports should not be used as the external power cannot control the module status through the PCIe protocol.

3.2.1 Power Supply

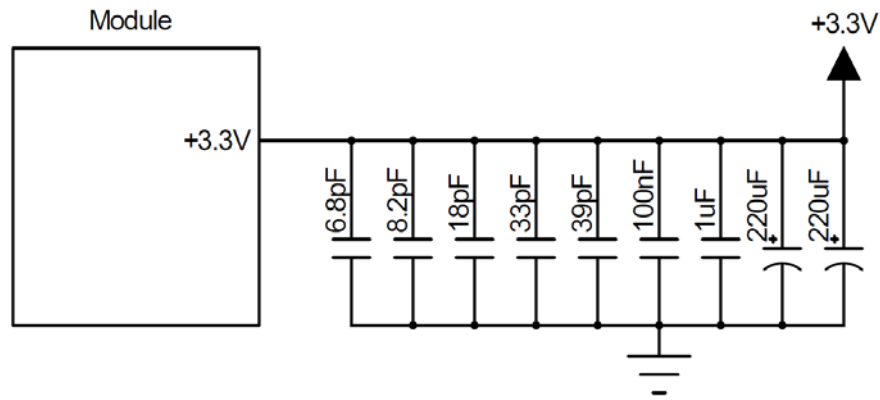The L850 module should be powered through the +3.3V pins, and the power supply design is shown in Figure 3-2:

Figure 3-2 Power Supply Design

The filter capacitor design for power supply as shown in the following table:

Recommended capacitance	Application	Description
220uF x 2	Voltage-stabilizing capacitors	Reduce power fluctuations of the module in operation, requiring capacitors with low ESR. ● LDO or DC/DC power supply requires the capacitor of no less than 440uF ● The capacitor for battery power supply can be reduced to 100~200uF
1uF, 100nF	Digital signal noise	Filter out the interference generated from the clock and digital signals
39pF, 33pF	700/800, 850/900 MHz frequency band	Filter out low frequency band RF interference
18pF, 8.2pF, 6.8pF	1500/1700/1800/1900, 2100/2300, 2500/2600MHzfrequency band	Filter out medium/high frequency band RF interference

The stable power supply can ensure the normal operation of L850 module; and the ripple of the power supply should be less than 300mV in design. When the module operates with the maximum emission power, the maximum operating current can reach 1000mA, so the power source should be not lower than 3.135V, or the module may shut down or reboot. The power supply limits are shown in Figure 3-3:
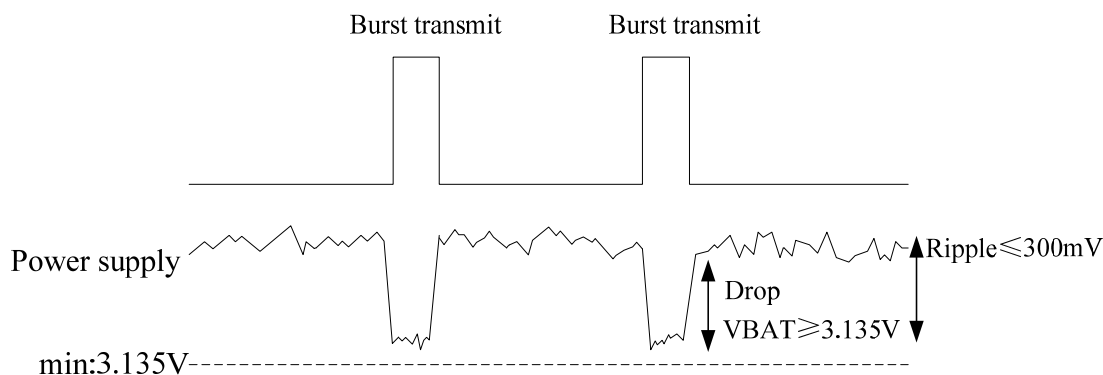

Figure 3-3 Power Supply Limit

3.2.2 Logic level

The L850module 1.8V logic level definition as shown in the following table:

Parameters	Minimum	Typical	Maximum	Unit
1.8V logic level	1.71	1.8	1.89	V
V_{IH}	1.3	1.8	1.89	V
V_{IL}	-0.3	0	0.3	V

The L850module 3.3V logic level definition as shown in the following table:

Parameters	Minimum	Typical	Maximum	Unit
3.3V logic level	3.135	3.3	3.465	V
V_{IH}	2.3	3.3	3.465	V
V_{IL}	-0.3	0	0.3	V

3.2.3 Power Consumption

In the condition of 3.3V power supply, the L850 power consumption as shown in the following table:

Parameter	Mode	Condition	Average Current(mA)
I_{off}	Power off	Power supply, module power off	0.08
I_{Sleep}	WCDMA	DRX=6	3.3
		DRX=8	2.6
		DRX=9	2.4
	LTE FDD	Paging cycle #64 frames (0.64 sec DRx cycle)	3.8
	LTE TDD	Paging cycle #64 frames (0.64 sec DRx cycle)	4.2
	Radio Off	AT+CFUN=4, Flight mode	2.0
$I_{WCDMA-RMS}$	WCDMA	WCDMA Data call Band 1 @+23.5dBm	580
		WCDMA Data call Band 2 @+23.5dBm	700
		WCDMA Data call Band 4 @+23.5dBm	530
		WCDMA Data call Band 5 @+23.5dBm	480
		WCDMA Data call Band 8 @+23.5dBm	560
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data call Band 1 @+23dBm	700
		LTE FDD Data call Band 2 @+23dBm	760
		LTE FDD Data call Band 3 @+23dBm	790

Parameter	Mode	Condition	Average Current(mA)
		LTE FDD Data call Band 4 @+23dBm	770
		LTE FDD Data call Band 5 @+23dBm	600
		LTE FDD Data call Band 7 @+23dBm	860
		LTE FDD Data call Band 8 @+23dBm	580
		LTE FDD Data call Band 11 @+23dBm	850
		LTE FDD Data call Band 12 @+23dBm	650
		LTE FDD Data call Band 13 @+23dBm	660
		LTE FDD Data call Band 17 @+23dBm	670
		LTE FDD Data call Band 18 @+23dBm	620
		LTE FDD Data call Band 19 @+23dBm	580
		LTE FDD Data call Band 20 @+23dBm	650
		LTE FDD Data call Band 21 @+23dBm	850
		LTE FDD Data call Band 26 @+23dBm	580
		LTE FDD Data call Band 28 @+23dBm	600
		LTE FDD Data call Band 30 @+22dBm	820
		LTE FDD Data call Band 66 @+23dBm	780
	LTE TDD	LTE TDD Data call Band 38 @+23dBm	450
		LTE TDD Data call Band 39 @+23dBm	350
		LTE TDD Data call Band 40 @+23dBm	380
		LTE TDD Data call Band 41 @+23dBm	460

In 3CA mode, the L850 power consumption as shown in the following table: ：

3CA Combination	Condition (LTE FDD 3CA, Full RB)	Average Current(mA)
1+3+7, 1+3+8, 1+3+19, 1+3+20, 1+3+28, 1+7+20, 1+7+28, 1+8+11, 1+19+21 2+4+5, 2+4+13, 2+5+30, 2+12+30, 2+29+30	Band 1 @+22dBm	920
	Band 2 @+22dBm	900
	Band 3 @+22dBm	1170

3CA Combination	Condition (LTE FDD 3CA, Full RB)	Average Current(mA)
3+7+20, 3+7+28	Band 4 @+22dBm	930
4+5+30, 4+12+30, 4+29+30	Band 5 @+22dBm	710
5+66+2, 13+66+2	Band 7 @+22dBm	950
2+2+5, 2+2+13	Band 8 @+22dBm	650
3+3+7, 3+7+7, 3+3+20	Band 11 @+22dBm	1000
4+4+5, 4+4+13	Band 12 @+22dBm	790
5+66+66, 13+66+66, 66+66+2, 66+66+66	Band 13 @+22dBm	700
7+7+28, 3+3+28, 3+3+5, 1+3+3	Band 19 @+22dBm	690
	Band 20 @+22dBm	730
	Band 21 @+22dBm	890
	Band 28 @+22dBm	670
	Band 30 @+21dBm	910
	Band 66 @+22dBm	820

![Note icon] **Note：**

The data above is an average value obtained by testing some samples.

3.3 Control Signal

The L850 module provides two control signals for power on/off and reset operations, the pin defined as shown in the following table:

Pin	Pin Name	I/O	Reset Value	Functions	Type
6	FULL_CARD_POWER_OFF#	I	PU	Module power on/off input, internal pull up Power on: High/Floating Power off: Low	3.3/1.8V
67	RESET#	I	-	WWAN reset input, internal pull up(10KΩ), active low	1.8V
50	PERST#	I	T	Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole	CMOS 3.3V

Pin	Pin Name	I/O	Reset Value	Functions	Type
				module, not only PCIe interface. Active low, internal pull up(10KΩ)	

⚠️ **Note：**

RESET# and PERST# need to be controlled by independent GPIO, and not shared with other devices on the host.

3.3.1 Module Start-Up

3.3.1.1 Start-up Circuit

The FULL_CARD_POWER_OFF# pin needs an external 3.3V or 1.8V pull up for booting up. The VDD_1V8 should be provided from the external circuit. AP (Application Processor) controls the module start-up，and the circuit design is shown in Figure3-4:
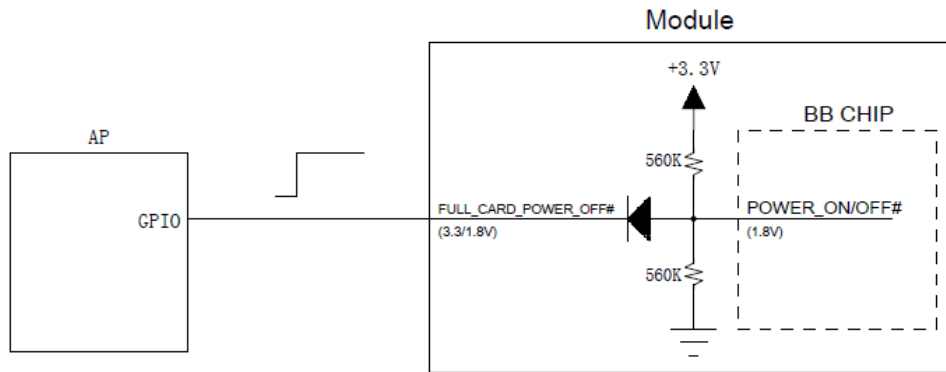
Figure 3-4 Circuit for Module Start-up Controlled by AP

3.3.1.2 Start-up Timing Sequence

When power supply is ready, the PMU of module will power on and start initialization process by pulling high FULL_CARD_POWER_OFF# signal. After about 10s, module will complete initialization process. The start-up timing is shown in Figure 3-5:
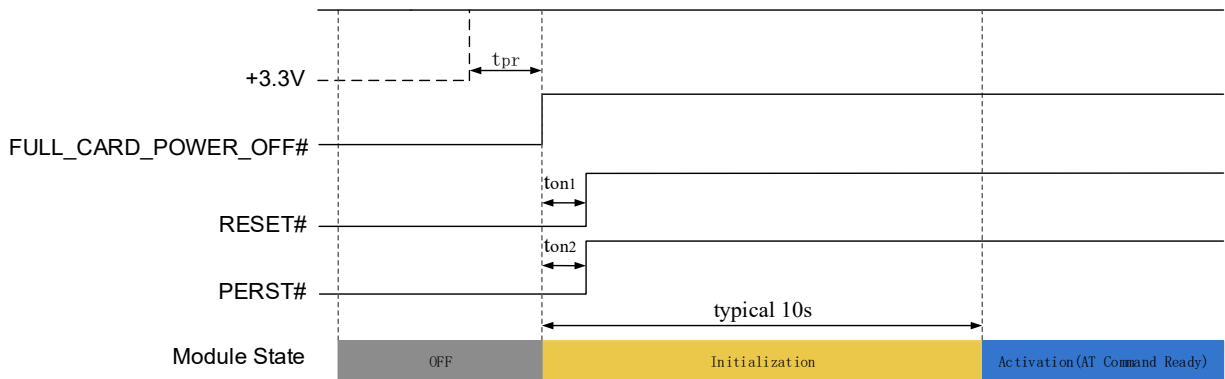

Figure 3-5 Timing Control for Start-up

Index	Minimum	Typical	Notes
t_{pr}	-	-	+3.3V power supply rises time. If power supply always ready, there is no t_{pr}
t_{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t_{on2}	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#

3.3.2 Module Shutdown

The module can be shut down by the following controls:

Shutdown Control	Action	Condition
Software	Sending AT+CFUN=0 command	Normal shutdown(recommend)
Hardware	Pull down FULL_CARD_POWER_OFF# pin	Only used when a hardware exception occurs and the software control cannot be used.

The module can be shut down by sending AT+CFUN=0 command. When the module receives the software shutdown command, the module will start the finalization process (the reverse process of initialization), and it will be completed after t_{sd} time(t_{sd} is the time which AP receive OK of "AT+CFUN=0", if there is no response, the max t_{sd} is 5s). In the finalization process, the module will save the network, SIM card and some other parameters from memory, then clear the memory and shut down PMU. The software control timing is shown in Figure 3-6:
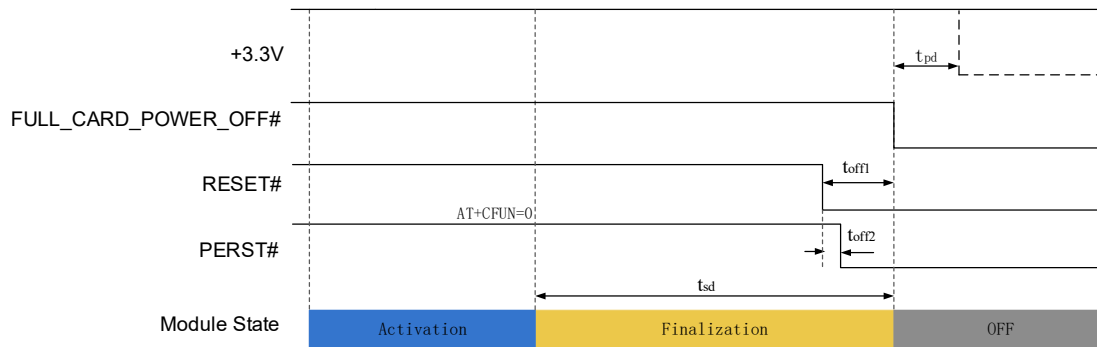

Figure 3-6 Software control power off timing

Index	Minimum	Typical	Maxim	Notes
t_{pd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t_{pd}
t_{off1}	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_OFF#
t_{off2}	0ms	30ms	t_{off1}	PERST# should asserted after RESET#

3.3.3 Module Reset

The L850 module can reset to its initial status by pulling down the RESET# signal for more than 10ms (30msis recommended), and module will restart after RESET# signal is released. When customer executes RESET# function, the PMU remains its power inside the module. The recommended circuit design is shown in the Figure 3-7:
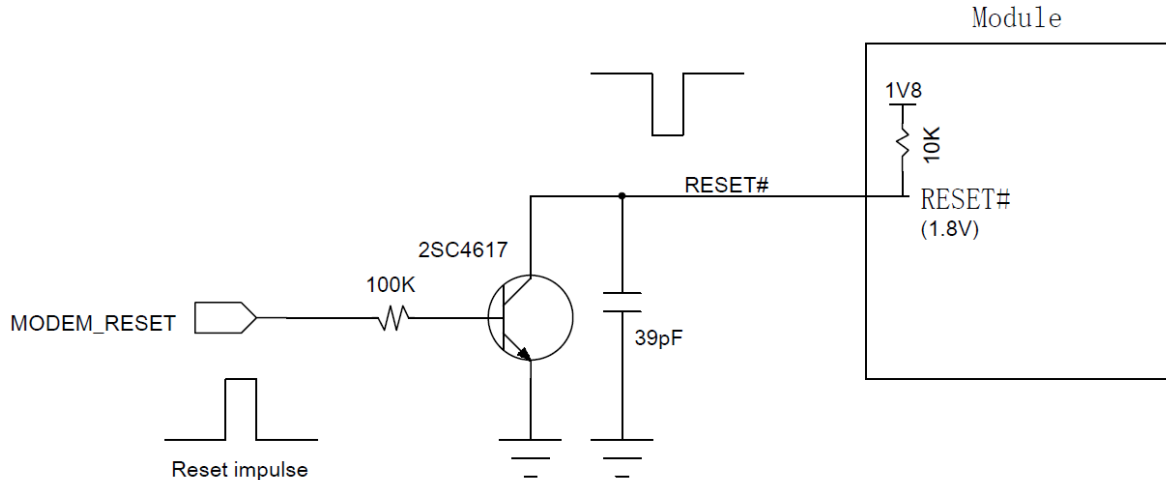

Figure 3-7 Recommended Design for Reset Circuit

There are two reset control timings as below:

- Host may keep FULL_CARD_POWER_OFF# high when system restarting, module reset timing is shown in the Figure 3-8;

- Host may assert FULL_CARD_POWER_OFF# high when system restarting, module reset timing is shown in the Figure 3-9;
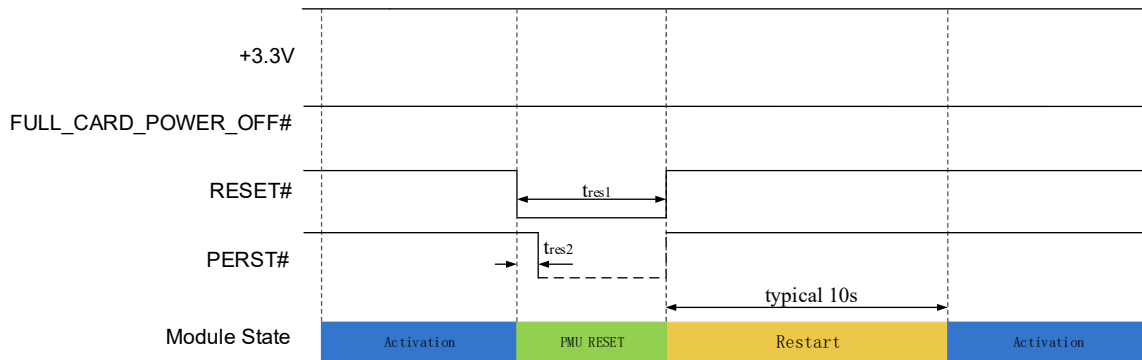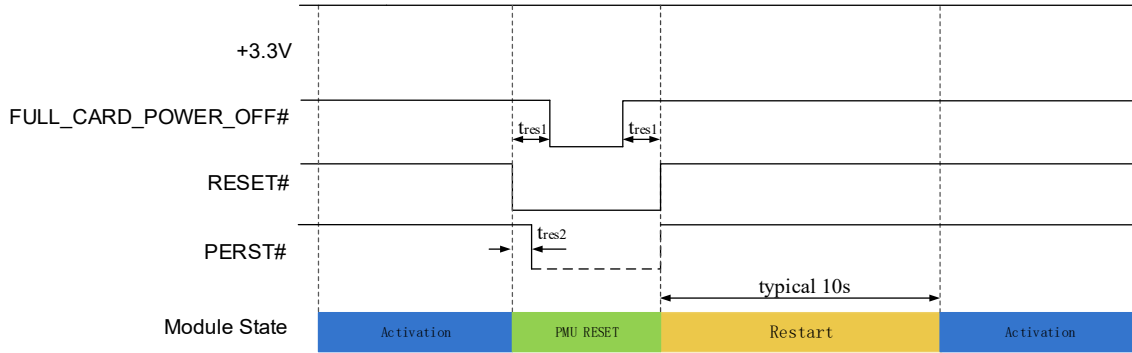

Figure 3-8 Reset control timing1st

Figure 3-9 Reset control timing2nd

Index	Minimum	Typical	Notes
t$_{res1}$	10ms	30ms	RESET# should asserted time
t$_{res2}$	0ms	30ms	PERST# should asserted after RESET#. PERST# is not required for modem restart, thus this pin can be remains high during restart

Note:

RESET# is a sensitive signal, it's recommended to add a filter capacitor close to the module. In case of PCB layout, the RESET# signal lines should keep away from the RF interference and protected by GND. Also, the RESET# signal lines shall neither near the PCB edge nor route on the surface planes to avoid module from reset caused by ESD problems.

3.3.4 PCIe Reset

Module supports PCIe goes in to D3cold L2 state in Win10 system. The D0->D3cold L2@S0/S0ix/S3 ->D0 timing is shown in figure 3-10:
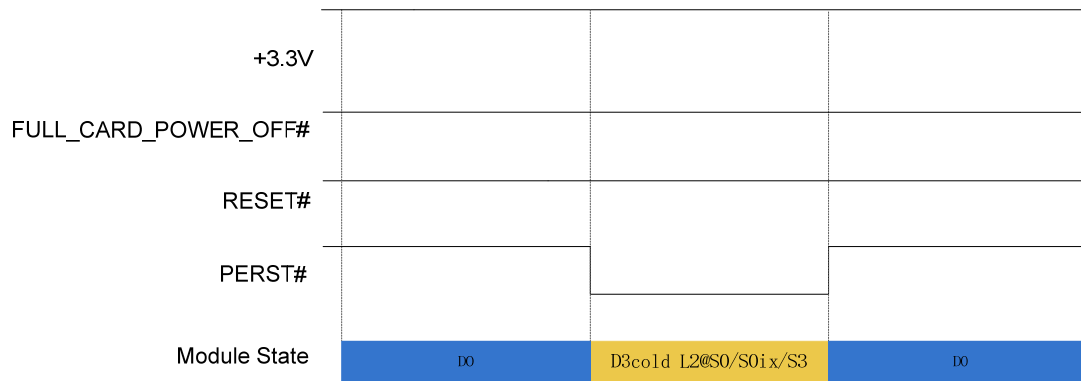

Figure 3-10 PCIe reset timing

3.4 PCIe & USB

L850 module supports PCIe and USB interface for data request. PCIe & USB interface functions are as below table:

Interface	System	Priority	Description
PCIe	Win10	High	Priority: PCIe>USB. If PCIe and USB ports connected both with PC, module will initial PCIe first, then disable USB port
USB	Android/Linux	Low	It must disconnect PCIe port, only keep USB connecting. If keep PCIe and USB connecting both, it needs disable PCIe by BIOS/UEFI of PC

3.4.1PCIe Interface

L850 module supports PCIe 1.0 interface and one data transmission channel.

After L850 module is inserted into PC, PCIe interface can, work with the drive program, map an MBIM port and a GNSS port in Win10 system. While MBIM interface is used for initiating data service in Win10 system and GNSS interface for receiving GNSS data.

3.4.1.1 PCIe Interface Definition

Pin#	Pin Name	I/O	Reset Value	Description	Type
41	PETn0	O	-	PCIe TX Differential signals Negative	-
43	PETP0	O	-	PCIe TX Differential signals Positive	-
47	PERn0	I	-	PCIe RX Differential signals NegativeBit0	-
49	PERP0	I	-	PCIe RX Differential signals Positive	-
53	REFCLKN	I	-	PCIe Reference Clock signal Negative	-
55	REFCLKP	I	-	PCIe Reference Clock signal Positive	-
50	PERST#	I	T	Asserted to reset module PCIe interface default. If module went into coredump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	CMOS 3.3V

Pin#	Pin Name	I/O	Reset Value	Description	Type
52	CLKREQ#	O	T	Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, internal pull up(10KΩ)	CMOS 3.3V
54	PEWAKE#	O	L	Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up on platform	CMOS 3.3V

3.4.1.2 PCIe Interface Application

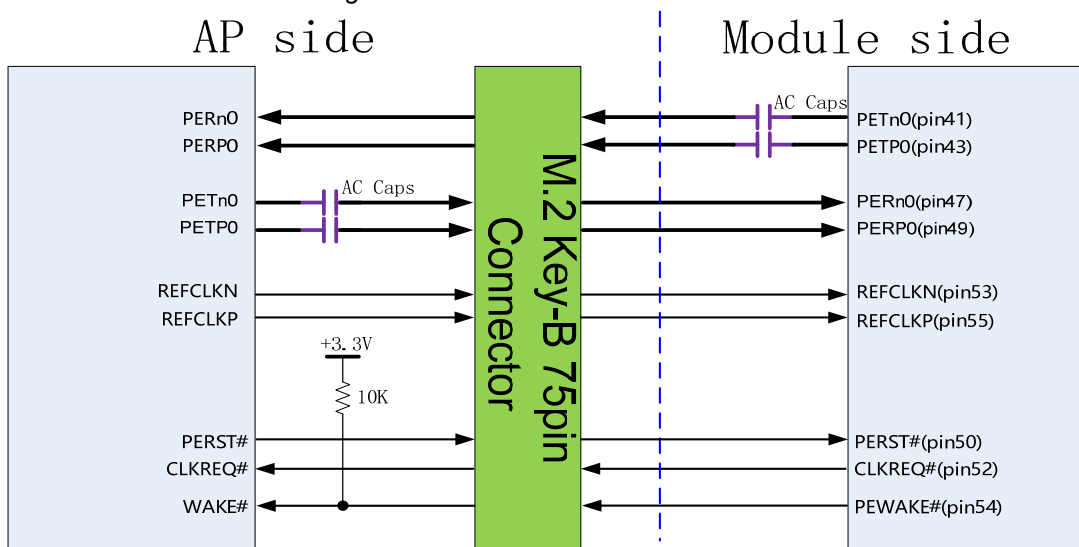The reference circuit is shown in Figure 3-11:

Figure 3-11 Reference Circuit for PCIe Interface

L850 module supports one PCIe 1.0 interface, including three difference pairs: transmit pair TXP/N, receiving pair RXP/N and clock pair CLKP/N.

PCIe can achieve the maximum transmission rate of 2.5 GT/s, and must strictly follow the rules below in PCB Layout:

- The differential signal pair lines shall be parallel and equal in length;
- The differential signal pair lines shall be short if possible and be controlled within 15 inch(380 mm) for AP end;
- The impedance of differential signal pair lines is recommended to be 100 ohm, and can be controlled to 80～120 ohm in accordance with PCIe protocol;

- It shall avoid the discontinuous reference ground, such as segment and space;

- When the differential signal lines go through different layers, the via hole of grounding signal should be in close to that of signal, and generally, each pair of signals require 1-3 grounding signal via holes and the lines shall never cross the segment of plane;

- Try to avoid bended lines and avoid introducing common-mode noise in the system, which will influence the signal integrity and EMI of difference pair. As shown in Figure 3-12, the bending angle of all lines should be equal or greater than 135°, the spacing between difference pair lines should be larger than 20mil, and the line caused by bending should be greater than 1.5 times line width at least. When a serpentine line is used for length match with another line, the bended length of each segment shall be at least 3 times the line width (≥3W). The largest spacing between the bended part of the serpentine line and another one of the differential lines must be less than 2 times the spacing of normal differential lines (S1<2S);
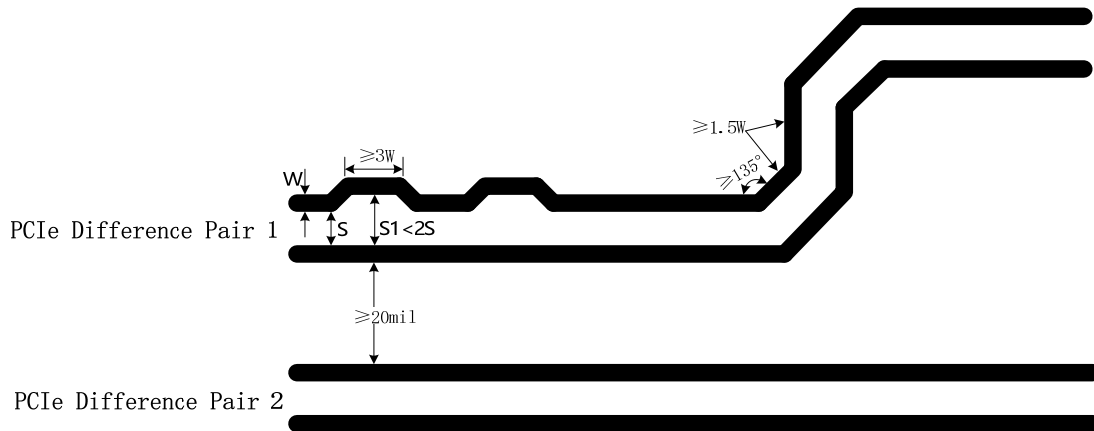

Figure 3-12 Requirement of PCIe Line

- The difference in length of two data lines in difference pair should be within 5mil, and the length match is required for all parts. When the length match is conducted for the differential lines, the designed position of correct match should be close to that of incorrect match, as shown in Figure 3-13. However, there is no specific requirements for the length match of transmit pair and receiving pair, that is, the length match is only required in the internal differential lines rather than between different difference pairs. The length match should be close to the signal pin and pass the small-angle bending design.
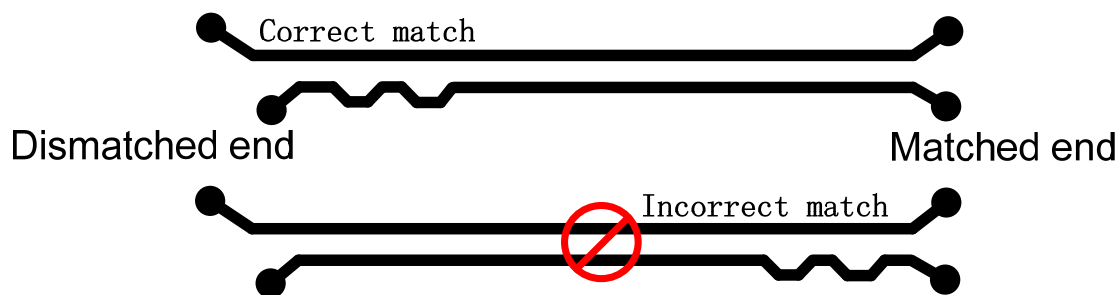
Figure 3-13 Length Match Design of PCIe Difference Pair

3.4.2USB Interface

The L850 module supports USB2.0 which is compatible with USB High-Speed (480 Mbit/s) and USB Full-Speed (12 Mbit/s).It supports USB3.0 using for LTE cat9 high speed data throughput at the same time. For the USB timing and electrical specification of L850 module, please refer to Universal Serial Bus Specification 2.0" and "Universal Serial Bus Specification 3.0".

When module inserted PC, USB can enumerate three ACM and three NCM ports in Android/Linux system, the ports can be configured in practical application.

3.4.2.1 USB Interface Definition

Pin#	Pin Name	I/O	Description	Type
7	USB_D+	I/O	USB Data Plus	0.3---3V, USB2.0
9	USB_D-	I/O	USB Data Minus	0.3---3V, USB2.0
29	USB3.0_TX-	O	USB3.0 Transmit data minus	-
31	USB3.0_TX+	O	USB3.0 Transmit data plus	-
35	USB3.0_RX-	I	USB3.0 receive data minus	-
37	USB3.0_RX+	I	USB3.0 receive data plus	-

3.4.2.2 USB2.0 Interface Application
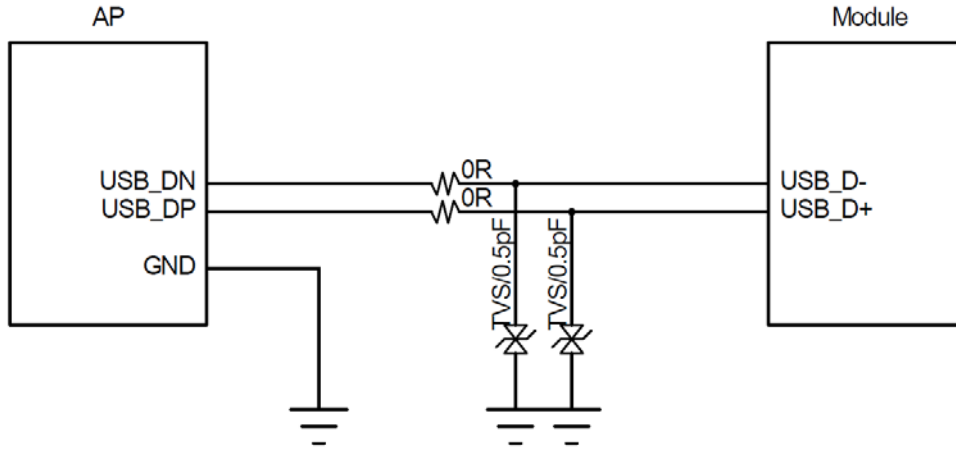
The reference circuit is shown in Figure 3-14:

Figure 3-14 Reference Circuit for USB 2.0 Interface

Since the module supports USB 2.0 High-Speed, it is required to use TVS diodes with equivalent capacitance of 1pF or smaller ones on the USB_D-/D+ differential signal lines, it is recommended to use 0.5pF TVS diodes.

USB_D- and USB_D+ are high speed differential signal lines with the maximum transfer rate of480 Mbit/s, so the following rules shall be followed carefully in the case of PCB layout:

- USB_D- and USB_D+ signal lines should have the differential impedance of 90 ohms.
- USB_D- and USB_D+ signal lines should be parallel and have the equal length, the right angle routing should be avoided.
- USB_D- and USB_D+ signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

3.4.2.3 USB3.0 Interface Application

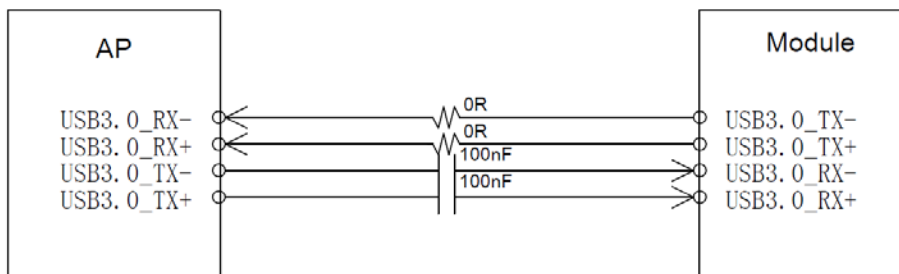The reference circuit is shown in Figure 3-15:

Figure 3-15 Reference Circuit for USB 3.0 Interface

USB 3.0 signals are super speed differential signal lines with the maximum transfer rate of5Gbps.So the following rules shall be followed carefully in the case of PCB layout:

- USB3.0_TX-/USB3.0_TX+ and USB3.0_RX-/ USB3.0_RX+ are two pairs differential signal lines, the differential impedance should be controlled as100 ohms.
- The two pairs differential signal lines should be parallel and have the equal length, the right

angle routing should be avoided.

- The two pairs differential signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

3.5 USIM Interface

The L850 module has a built-in USIM card interface, which supports 1.8V and 3V SIM cards.

3.5.1 USIM Pins

The USIM pins description as shown in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Type
36	UIM_PWR	PO	_	USIM power supply	1.8V/3V
30	UIM_RESET	O	L	USIM reset	1.8V/3V
32	UIM_CLK	O	L	USIM clock	1.8V/3V
34	UIM_DATA	I/O	L	USIM data, internal pull up(4.7KΩ)	1.8V/3V
66	SIM_DETECT	I	PD	USIM card detect, internal 390K pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached.	1.8V

3.5.2 USIM Interface Circuit

3.5.2.1 N.C. SIM Card Slot

The reference circuit design for N.C. (Normally Closed) SIM card slot is shown in Figure 3-16:
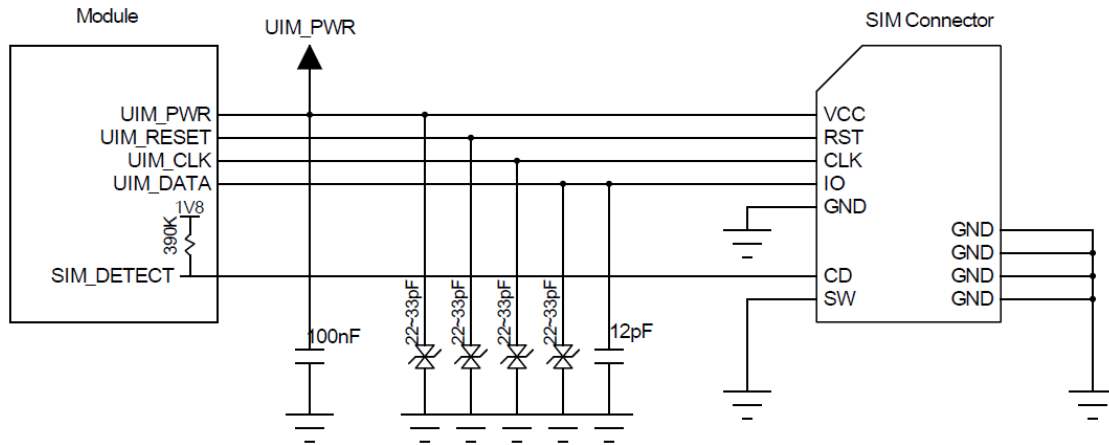
Figure 3-16Reference Circuit for N.C. SIM Card Slot

The principles of the N.C.SIM card slot are described as follows:

- When the SIM card is detached, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin low.
- When the SIM card is inserted, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin high.

3.5.2.2 N.O. SIM Card Slot

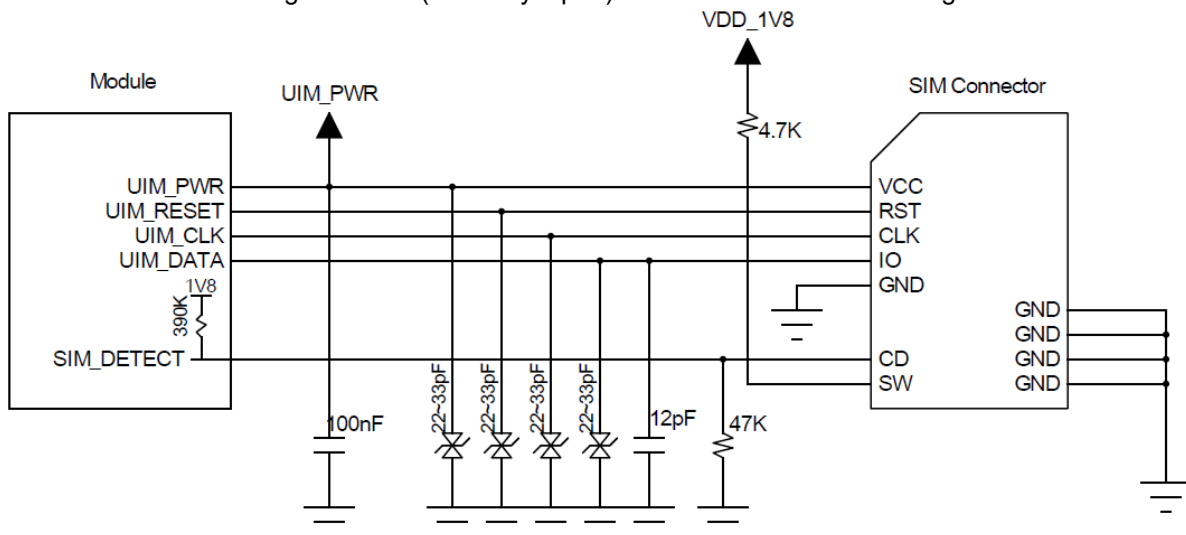The reference circuit design for N.O. (Normally Open) SIM card slot is shown in Figure 3-17:

Figure 3-17 Reference Circuit for N.O. SIM Card Slot

The principles of the N.O.SIM card slot are described as follows:

- When the SIM card is detached, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin low.
- When the SIM card is inserted, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin high.

3.5.3 USIM Hot-Plugging

The L850 module supports the SIM card hot-plugging function, which determines whether the SIM card is inserted or detached by detecting the SIM_DETECT pin state of the SIM card slot.

The SIM card hot-plugging function can be configured by "AT+MSMPD" command, and the description for AT command as shown in the following table:

AT Command	Hot-plugging Detection	Function Description
AT+MSMPD=1	Enable	Default value, the SIM card hot-plugging detection function is enabled. The module can detect whether the SIM card is inserted or not through the SIM_DETECT pin state.
AT+MSMPD=0	Disable	The SIM card hot-plugging detect function is disabled. The module reads the SIM card when starting up, and the SIM_DETECT status will not be detected.

After the SIM card hot-plugging detection function is enabled, the module detects that the SIM card is inserted when the SIM_DETECT pin is high, then executes the initialization program and finish the network registration after reading the SIM card information. When the SIM_DETECT pin is low, the module determines that the SIM card is detached and does not read the SIM card.

> **Note:**
>
> By default, SIM_DETECT is active-high, which can be switched to active-low by the AT command. Please refer to the AT Commands Manual for the AT command.

3.5.4 USIM Design

The SIM card circuit design shall meet the EMC standards and ESD requirements with the improved capability to resist interference, to ensure that the SIM card can work stably. The following guidelines should be noted in case of design:

- The SIM card slot placement should near the module as close as possible, and away from the RF antenna, DC/DC power supply, clock signal lines, and other strong interference sources.
- The SIM card slot with a metal shielding housing can improve the anti-interference ability.
- The trace length between the SIM card slot and the module should not exceed 100mm, or it could reduce the signal quality.
- The UIM_CLK and UIM_DATA signal lines should be isolated by GND to avoid crosstalk

interference. If it is difficult for the layout, the whole SIM signal lines should be wrapped with GND as a group at least.

- The filter capacitors and ESD devices for SIM card signals should be placed near to the SIM card slot, and the ESD devices with 22~33pF capacitance should be used.

3.6 Status Indicator

The L850 module provides three signals to indicate the operating status of the module, and the status indicator pins as shown in the following table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
10	LED1#	O	PD	System status LED, drain output.	CMOS 3.3V
23	WOWWAN#	O	PU	Module wakes up Host (AP)，Reserved	CMOS 1.8V
48	TX_BLANKING	O	PD	PA Blanking output, external GPS control signal，Reserved	CMOS 1.8V

3.6.1 LED#1 Signal

The LED#1 signal is used to indicate the operating status of the module, and the detailed description as shown in the following table:

Module Status	LED1# Signal
RF function ON	Low level (LED On)
RF function OFF	High level (LED Off)

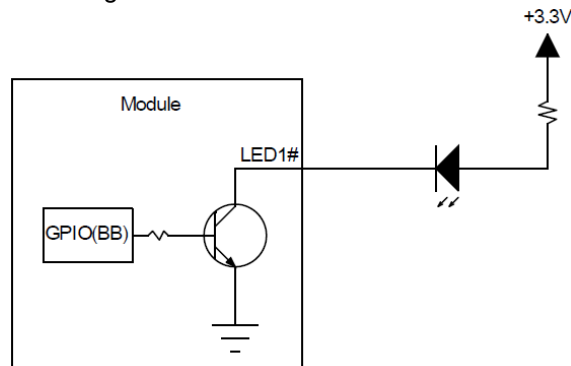The LED driving circuit is shown in figure 3-18:

Figure 3-18 LED Driving Circuit

⚠ **Note:**

The resistance of LED current-limiting resistor is selected according to the driving voltage and the driving current.

3.7 Interrupt Control

The L850 module provides four interrupt signals, and the pin definition is as follows:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
8	W_DISABLE1#	I	PD	Enable/Disable RF network	CMOS 3.3V
25	DPR	I	PU	Body SAR detection	CMOS 1.8V
26	W_DISABLE2#	I	PU	GNSS Disable signal, Reserved	CMOS 1.8V
44	GNSS_IRQ	I	PD	GNSS Interrupt Request, Reserved	CMOS 1.8V

3.7.1 W_DISABLE1#

The module provides a hardware pin to enable/disable WWAN RF function, and the function can also be controlled by the AT command. The module enters the Flight mode after the RF function is disabled. The definition of W_DISABLE1# signal is as follows:

W_DISABLE1# signal	Function
High/Floating	WWAN function is enabled, the module exits the Flight mode.
Low	WWAN function is disabled, the module enters Flight mode.

⚠️ **Note：**

The function of W_DISABLE1# can be customized, please refer to the software porting guide.

3.7.2 BODYSAR

The L850 module supports Body SAR function by detecting the DPR pin. The voltage level of DPR is high by default, and when the SAR sensor detects the closing human body, the DPR signal will be pulled down. As the result, the module then lowers down its emission power to its default threshold value, thus reducing the RF radiation on the human body. The threshold of emission power can be set by the AT Commands. The definition of DPR signal as shown in the following table:

DPR signal	Function
High/Floating	The module keeps the default emission power
Low	Lower the maximum emission power to the threshold value of the module.

3.8 Clock Interface

The L850 module supports a clock interface, it can output 26MHz clock.

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
46	SYSCLK	O		26M clock output, default disabled can be used for external GPS, etc	1.8V

3.9 ANT Tunable Interface

The module supports ANT Tunable interfaces with two different control modes, i.e. MIPI interface and 3bit GPO interface. Through cooperating with external antenna adapter switch via ANT Tunable, it can flexibly configure the bands of LTE antenna to improve the antenna's working efficiency and save space for the antenna.

Pin	Pin Name	I/O	Pin Description	Type
56	RFE_RFFE2_SCLK	O	Tunable ANT control, MIPI Interface, RFFE2 clock, Open Drain output	CMOS 3.3/1.8V
58	RFE_RFFE2_SDATA	O	Tunable ANT control, MIPI Interface, RFFE2 data, Open Drain output	CMOS 3.3/1.8V
59	ANTCTL0	O	Tunable ANT control, GPO interface, Bit0	CMOS 1.8V
61	ANTCTL1	O	Tunable ANT control, GPO interface, bit1	CMOS 1.8V
63	ANTCTL2	O	Tunable ANT control, GPO interface, Bit2	CMOS 1.8V

3.10   Configuration Interface

The L850 module provides four config pins for the configuration as the WWAN-PCIe, USB3.0 type M.2 module:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
1	CONFIG_3	O	-	NC	
21	CONFIG_0	O	L	Internally connected to GND	

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
69	CONFIG_1	O	L	Internally connected to GND	
75	CONFIG_2	O	L	Internally connected to GND	

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN–USB3.1, PCIe Gen1	0

Please refer to PCI Express M.2 Specification Rev1.1" for more details.

3.11   Other Interfaces

The module does not support other interfaces yet.

4 Radio Frequency

4.1 RF Interface

4.1.1 RF Interface Functionality

The L850 module supports two RF connectors used for external antenna connection. As the Figure 4-1 shows, "M" is for Main antenna, used to receive and transmit RF signals; "D/G" is for Diversity antenna, used to receive the diversity RF signals.
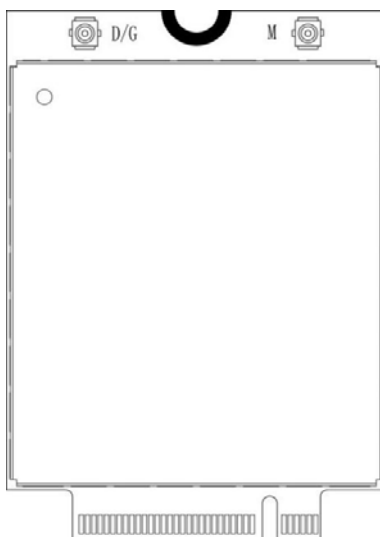

Figure 4-1 RF connectors

4.1.2 RF Connector Characteristic

Rated Condition		Environment Condition	
Frequency Range	DC to 6GHz	Temperature Range	
Characteristic Impedance	50Ω	–40°C to +85°C	

4.1.3 RF Connector Dimension

The L850 module adopts standard M.2 module RF connectors, the model name is 818004607 from ECT company, and the connector size is 2*2*0.6m. The connector dimension is shown as following picture:
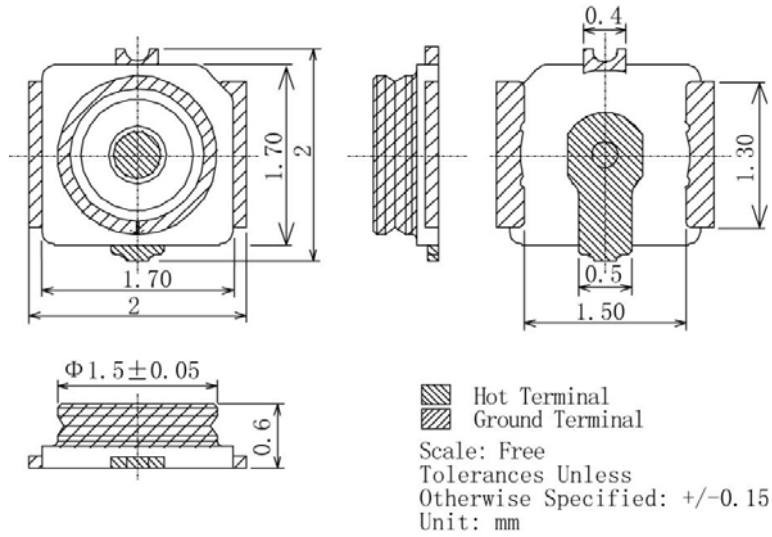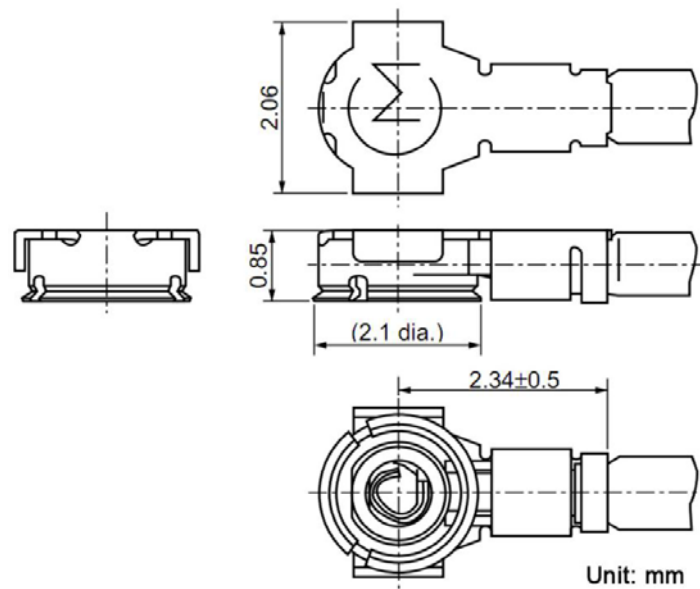
Figure 4-2 RF connector dimensions

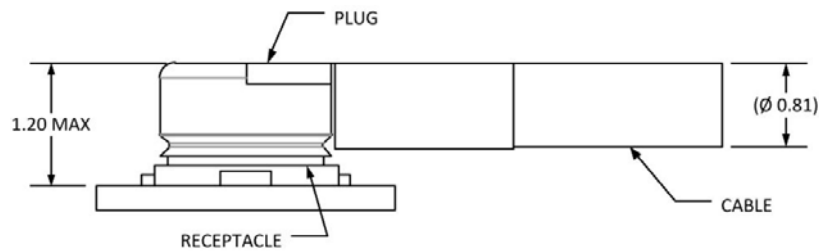Figure 4-3 0.81mm coaxial antenna dimensions

Figure 4-4 Schematic diagram of 0.81mm coaxial antenna connected to the RF connector

4.2 Operating Band

The L850 module operating bands of the antennas are as follows:

Operating Band	Description	Mode	Tx (MHz)	Rx (MHz)
Band 1	2100MHz	LTE FDD/WCDMA	1920 - 1980	2110 - 2170
Band 2	1900MHz	LTE FDD/WCDMA	1850 - 1910	1930 - 1990
Band 3	1800MHz	LTE FDD	1710 - 1785	1805 - 1880
Band 4	1700MHz	LTE FDD/WCDMA	1710 - 1755	2110 - 2155
Band 5	850MHz	LTE FDD/WCDMA	824 - 849	869 - 894
Band 7	2600Mhz	LTE FDD	2500 - 2570	2620 - 2690
Band 8	900MHz	LTE FDD/WCDMA	880 - 915	925 - 960
Band 11	1500MHz	LTE FDD	1427.9 - 1447.9	1475.9 - 1495.9
Band 12	700MHz	LTE FDD	699 - 716	729 - 746
Band 13	700MHz	LTE FDD	777 - 787	746 - 756
Band 17	700MHz	LTE FDD	704 - 716	734 - 746
Band 18	800MHz	LTE FDD	815 - 830	860 - 875
Band 19	800MHz	LTE FDD	830 - 845	875 - 890
Band 20	800MHz	LTE FDD	832 - 862	791 - 821
Band 21	1500MHz	LTE FDD	1447.9 - 1462.9	1495.9 - 1510.9
Band 26	850MHz	LTE FDD	814 - 849	859 - 894
Band 28	700MHz	LTE FDD	703 - 748	758 - 803
Band 29	700MHz	LTE FDD	N/A	716 - 728
Band 30	2300MHz	LTE FDD	2305 - 2315	2350 - 2360
Band 66	1700MHz	LTE FDD	1710 - 1780	2110 - 2200
Band 38	2600MHz	LTE TDD	2570 - 2620	
Band 39	1900MHZ	LTE TDD	1880 - 1920	
Band 40	2300MHz	LTE TDD	2300 - 2400	
Band 41	2500MHZ	LTE TDD	2496 - 2690	
GPS L1	-	-	/	1575.42±1.023
GLONASS L1	-	-	/	1602.5625±4

Operating Band	Description	Mode	Tx (MHz)	Rx (MHz)
BeiDou	-	-	/	1561.098±2.046

4.3 Transmitting Power

The transmitting power for each band of the L850 module as shown in the following table:

Mode	Band	3GPP Requirement(dBm)	Tx Power(dBm)	Note
WCDMA	Band 1	24+1.7/-3.7	23.5±1	-
	Band 2	24+1.7/-3.7	23.5±1	-
	Band 4	24+1.7/-3.7	23.5±1	-
	Band 5	24+1.7/-3.7	23.5±1	-
	Band 8	24+1.7/-3.7	23.5±1	-
LTE FDD	Band 1	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 2	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 3	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 4	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 5	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 7	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 8	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 11	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 12	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 13	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 17	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 18	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 19	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 20	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 21	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 26	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 28	23+2.7/-3.2	23±1	10MHz Bandwidth, 1 RB
	Band 30	23±2.7	22±1	10MHz Bandwidth, 1 RB

Mode	Band	3GPP Requirement(dBm)	Tx Power(dBm)	Note
	Band 66	23±2.7	23±1	10MHz Bandwidth, 1 RB
LTE TDD	Band 38	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 39	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 40	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 41	23±2.7	23±1	10MHz Bandwidth, 1 RB

4.4 Receiver Sensitivity

The receiver sensitivity for each band of the L850 module as shown in the following table:

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity(dBm) Typical	Note
WCDMA	Band 1	-106.7	-110	BER<0.1%
	Band 2	-104.7	-110	BER<0.1%
	Band 4	-106.7	-110	BER<0.1%
	Band 5	-104.7	-111	BER<0.1%
	Band 8	-103.7	-110	BER<0.1%
LTE FDD	Band 1	-96.3	-101.5	10MHz Bandwidth
	Band 2	-94.3	-101.5	10MHz Bandwidth
	Band 3	-93.3	-102	10MHz Bandwidth
	Band 4	-96.3	-102	10MHz Bandwidth
	Band 5	-94.3	-103	10MHz Bandwidth
	Band 7	-94.3	-101	10MHz Bandwidth
	Band 8	-93.3	-102.5	10MHz Bandwidth
	Band 11	-96.3	-99	10MHz Bandwidth
	Band 12	-93.3	-102.5	10MHz Bandwidth
	Band 13	-93.3	-102.5	10MHz Bandwidth
	Band 17	-93.3	-102.5	10MHz Bandwidth
	Band 18	-96.3	-103	10MHz Bandwidth
	Band 19	-96.3	-103	10MHz Bandwidth

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity(dBm) Typical	Note
	Band 20	-93.3	-102.5	10MHz Bandwidth
	Band 21	-96.3	-99	10MHz Bandwidth
	Band 26	-93.8	-103	10MHz Bandwidth
	Band 28	-94.8	-103	10MHz Bandwidth
	Band 29	-93.3	-101	10MHz Bandwidth
	Band 30	-95.3	-99.5	10MHz Bandwidth
	Band 66	-95.8	-101.5	10MHz Bandwidth
LTE TDD	Band 38	-96.3	-101	10MHz Bandwidth
	Band 39	-96.3	-101.5	10MHz Bandwidth
	Band 40	-96.3	-100.5	10MHz Bandwidth
	Band 41	-94.3	-100	10MHz Bandwidth

Note:

The above values are measured for the dual antennas situation (Main+Diversity). For single main antenna (without Diversity), the sensitivity will drop around 3dBm for each band of LTE.

4.5 GNSS

L850 module supports GNSS/BeiDou and AGNSS functions, and adopts RF Diversity and GNSS/Beidou integrated antenna.

Description		Condition	Test Result
Power		GPS fixing	120mA / -130dbm
		GPS tracking	120mA / -130dbm
		GLONASS fixing	120mA / -130dbm
		GLONASS tracking	125mA / -130dbm
		BeiDou fixing	120mA / -130dbm
		BeiDou tracking	120mA / -130dbm
		GPS Sleep	0.7mA
		GLONASS Sleep	0.8mA
		BeiDou Sleep	0.7mA
TTFF	GPS	Cold start	37s / -130dBm

Description		Condition	Test Result
		Warm start	34s / -130dBm
		Hot Start	2s / -130dBm
	GLONASS	Cold start	31s / -130dBm
		Warm start	22s / -130dBm
		Hot Start	3s / -130dBm
	BeiDou	Cold start	148s / -130dBm
		Warm start	148s / -130dBm
		Hot Start	3s / -130dBm
	AGNSS	Cold start	TBD
Sensitivity	GPS	Tracking	-160dBm
		Acquisition	-149dBm
	GLONASS	Tracking	-160dBm
		Acquisition	-146dBm
	BeiDou	Tracking	-160dBm
		Acquisition	-141dBm

⚠ **Note:**

Please note that GPS current is tested with RF disabled.

4.6 Antenna Design

The L850module provides main and diversity antenna interfaces, and the antenna design requirements as shown in the following table:

L850 module Main antenna requirements	
Frequency range	The most proper antenna to adapt the frequencies should be used.
Bandwidth(WCDMA)	WCDMA band 1(2100) : 250 MHz WCDMA band 2(1900) : 140 MHz WCDMA band 4(1700) : 445 MHz WCDMA band 5(850) : 70 MHz WCDMA band 8(900) : 80 MHz
Bandwidth(LTE)	LTE band 1(2100): 250 MHz

L850 module Main antenna requirements	
	LTE band 2(1900): 140 MHz
	LTE Band 3(1800): 170 MHz
	LTE band 4(1700): 445 MHz
	LTE band 5(850): 70 MHz
	LTE band 7(2600): 190 MHz
	LTE Band 8(900): 80 MHz
	LTE Band 11(1500): 68 MHz
	LTE Band 12(700): 47 MHz
	LTE Band 13(700): 41 MHz
	LTE Band 17(700): 42 MHz
	LTE Band 18(800): 80 MHz
	LTE Band 19(800): 80 MHz
	LTE band 20(800): 71 MHz
	LTE band 21(1500): 63 MHz
	LTE band 26(850): 80 MHz
	LTE band 28(700): 100 MHz
	LTE band 29(700): 12 MHz
	LTE band 30(2300): 55 MHz
	LTE band 66(1700): 490 MHz
	LTE band 38(2600): 50 MHz
	LTE Band 39(1900): 40 MHz
	LTE band 40(2300): 100 MHz
	LTE band 41(2500): 194 MHz
Bandwidth(GNSS/BeiDou)	GPS: 2 MHz GLONASS: 8 MHz BeiDou: 4 MHz
Impedance	50Ohm
Input power	> 26dBm average power WCDMA & LTE
Recommended standing-wave ratio (SWR)	≤ 2: 1

5 Structure Specification

5.1 Product Appearance

The product appearance for L850 module is shown in Figure5-1:
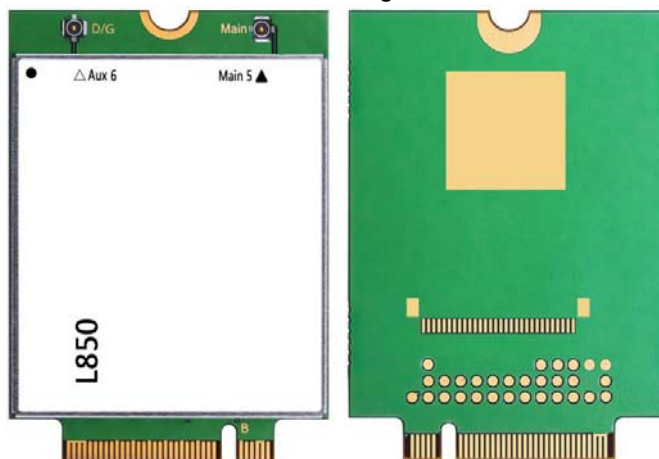
Figure 5-1 Module Appearance

5.2 Dimension of Structure

The structural dimension of the L850 module is shown in Figure 5-2:
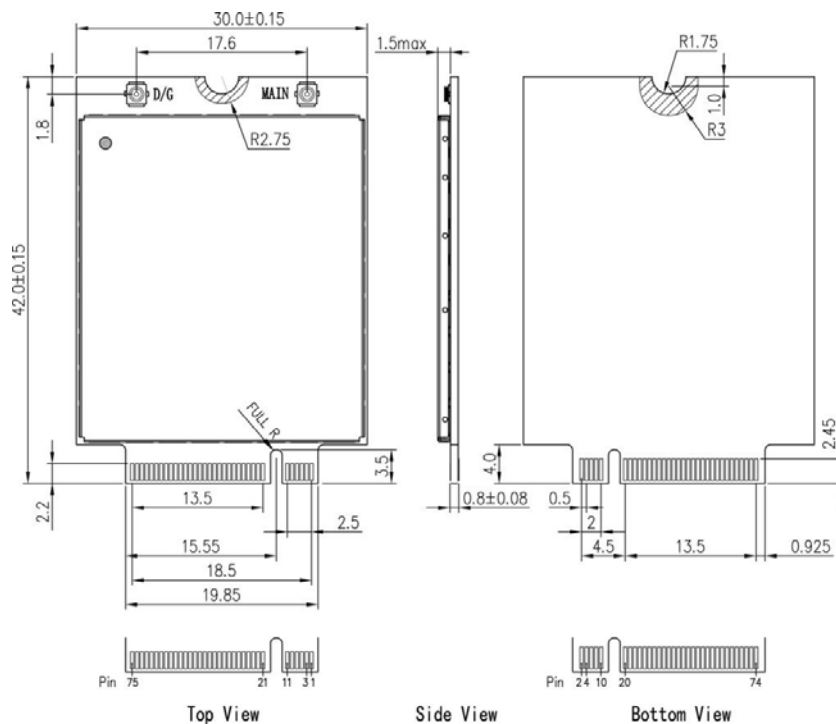
Figure 5-2 Dimension of Structure

5.3 M.2 Interface Model

The L850 M.2 module adopts 75-pin gold finger as external interface, where 67 pins are signal pins and 8 pins are notch pins as shown in Figure 3-1. For module dimension, please refer to 5.2 Dimension of Structure. Based on the M.2 interface definition, L850 module adopts Type 3042-S3-B interface (30x42mm, the component maximum height on t top layer is 1.5mm, PCB thickness is 0.8mm, and KEY ID is B).

5.4 M.2 Connector

The L850 module connects to AP via M.2 connector, it is recommended to use M.2 connector from LOTES company with the model APCI0026-P001A as shown in Figure 5-3. The package of connector, please refer to the specification.
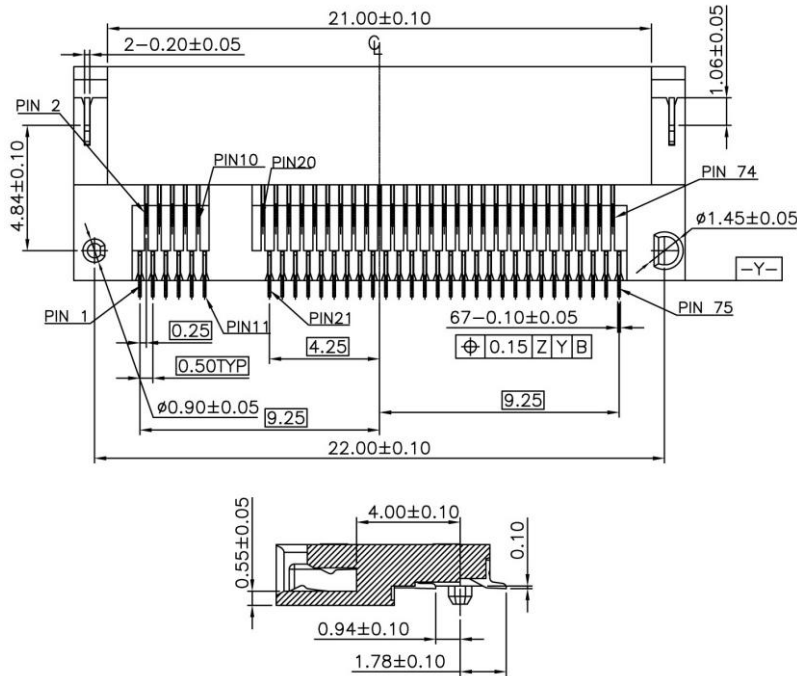
\# Figure 5-3 M.2 Dimension of Structure

5.5 Storage

5.5.1 Storage Life

Storage Conditions (recommended): Temperature is 23 ± 5 □, relative humidity is less than RH 60%.

Storage period: Under the recommended storage conditions, the storage life is 12 months.

5.6 Packing

The L850 module uses the tray sealed packing, combined with the outer packing method using the hard cartoon box, so that the storage, transportation and the usage of modules can be protected to the greatest extent.

⚠ **Note：**

The module is a precision electronic product, and may suffer permanent damage if no correct electrostatic protection measures are taken.

5.6.1 Tray Package

The L850 module uses tray package, 20 pcs are packed in each tray, with 5 trays in each box and 6 boxes

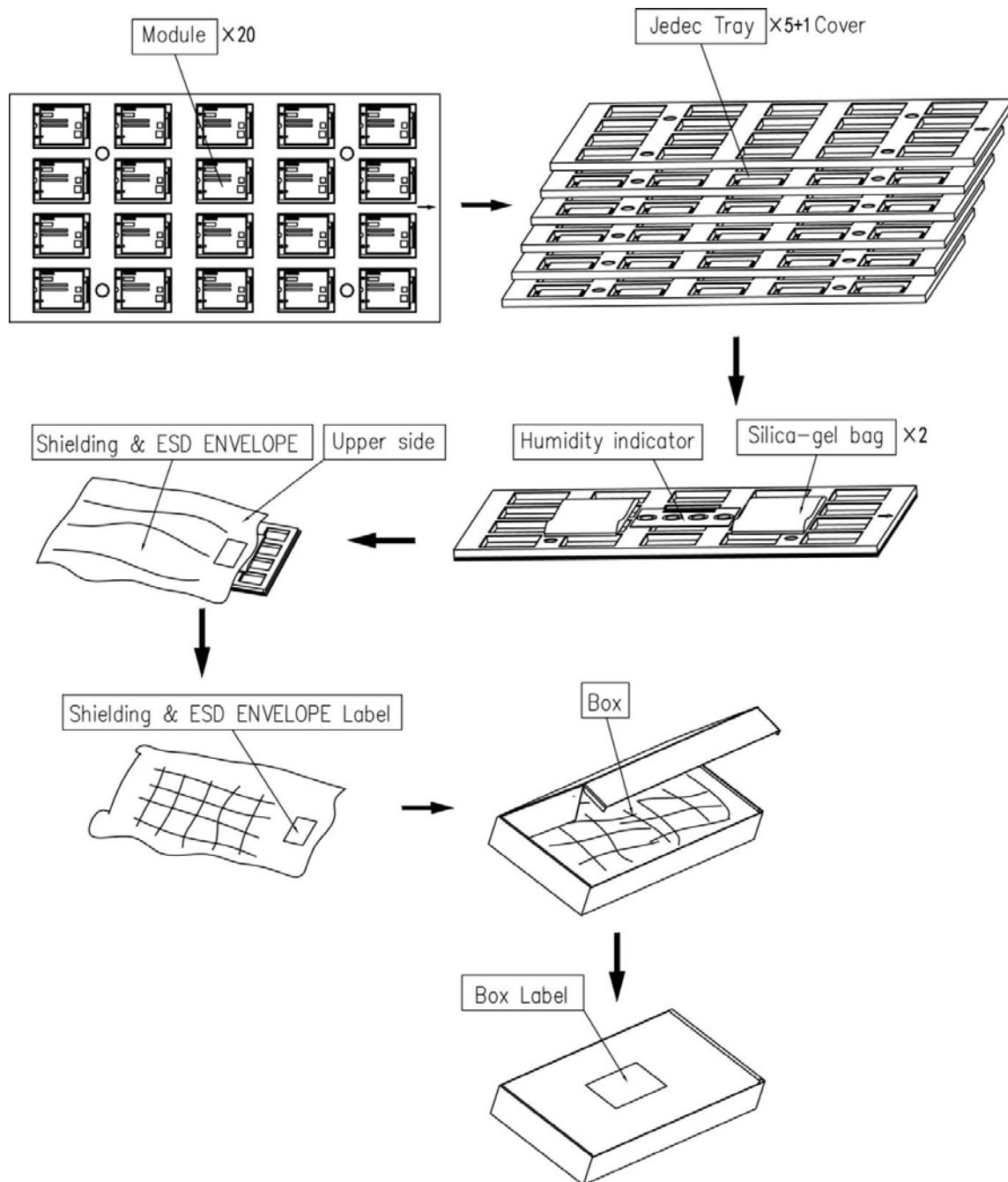in each case. Tray packaging process is shown in Figure 5-4:

Figure 5-4 Tray Packaging Process

5.6.2 Tray size
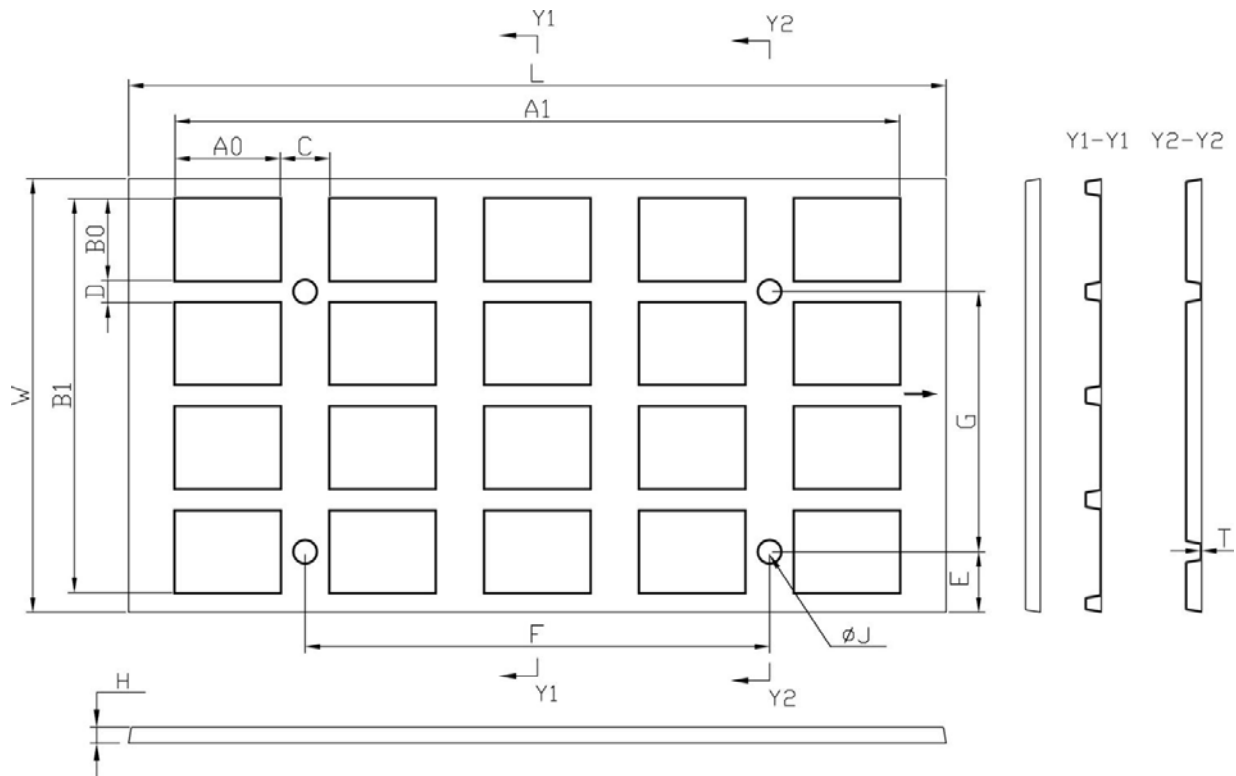
The pallet size is 330*175*6.0mm, as shown in Figure 5-5:

Figure 5-5Tray Size (Unit: mm)

ITEM	DIM(Unit: mm)
L	330.0±0.5
W	175.0±0.5
H	6.0±0.3
T	0.5±0.1
A0	43±0.3
B0	33.0±0.3
A1	294.0±0.3
B1	159.0±0.3
C	20.0±0.5
D	9.0±0.5
E	24.5±0.5
F	187.5±0.2
G	105.0±0.2
J	9.0±0.2