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Flaircomm Microelectronics, Inc.

FLC-BTM020

Datasheet

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Release Record

Version	Release Date	Comments
V0.1	April 18, 2018	Release
V0.2	May 24, 2018	Add reference circuit and RF Layout and placement
V0.3	Jan 15,2019	Add a new type---BTM020IQ2D Remove type-- BTM020IQ2A
	5.21.2019	1. 修改休眠时的功耗 2. ADD Cautions &Warnings

CONTENTS

TABLES AND FIGURES

1. Introduction

FLC-BTM020 is a Bluetooth low energy (BLE) module supporting BT5.0 (BLE only). This module makes it easy for customers to add Bluetooth low energy to their products. Customers can easily establish wireless connections with the module. It supports Bluetooth low energy (Bluetooth 5), ANT and 2.4GHz proprietary protocol stacks. It also has a NFC-A tag(Temporarily unavailable) interface for OOB pairing.

1.1 Naming Declaration

New Naming	Old Naming	Description
FLC-BTM020IQ2B	No	Module without antenna
FLC-BTM020IQ2D	No	Module with microstrip antenna

Table 1: Naming Declaration

1.2 Block Diagram

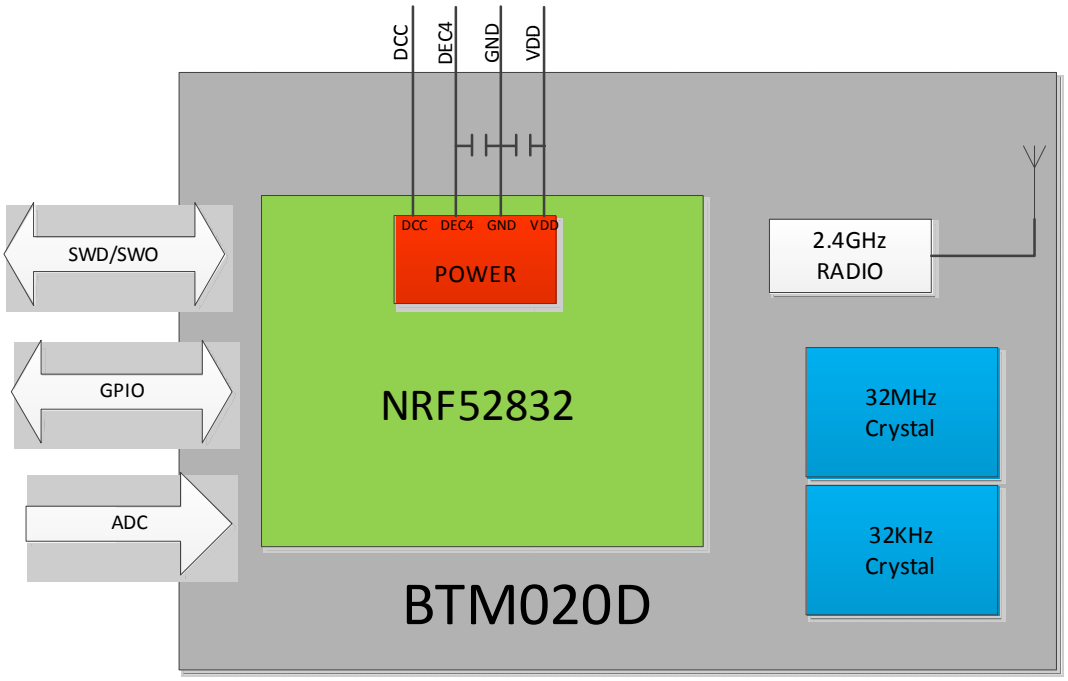


Figure 1: BTM020A Block Diagram

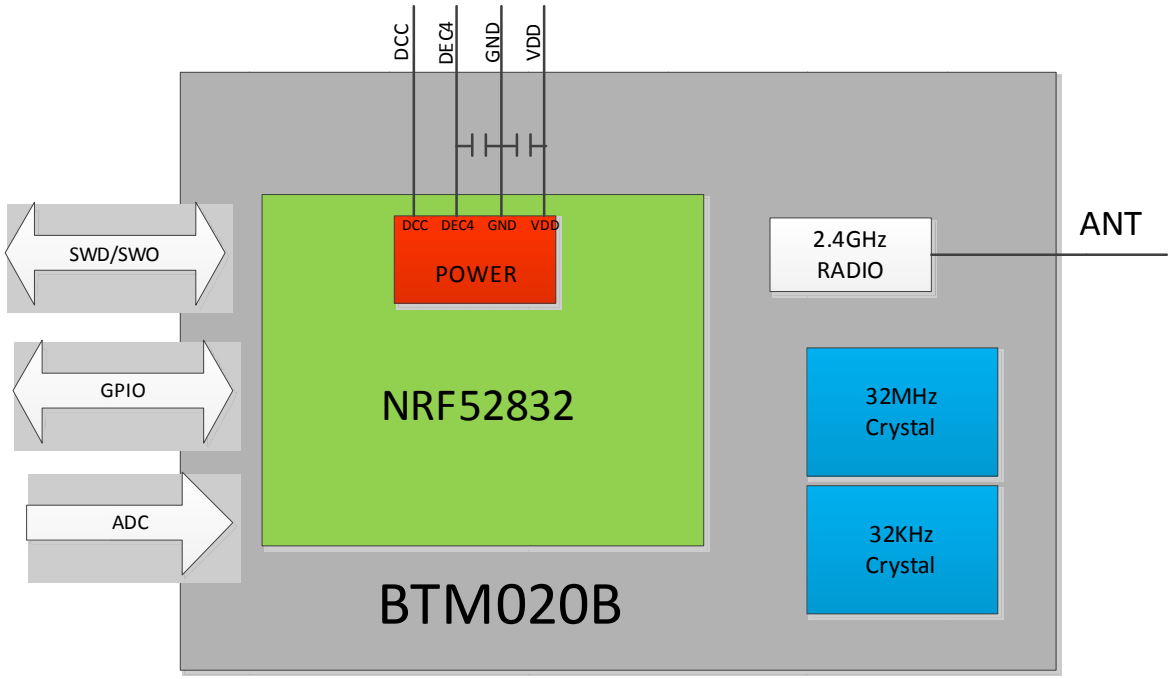


Figure 2: BTM020B Block Diagram

1.3 Features

- BT5.0(BLE only)，up to 2Mbps
- -96dbm sensitivity, TX power -20~ 4dBm in 4dB steps
- Include ATT, GATT, SMP, L2CAP, GAP
- AES HW encryption with Easy DMA
- ANT,2.4GHz,NFC-A tag(Temporarily unavailable)
- Cortex M4F MCU with 64KB RAM ,512KB FLASH
- 20-channel Programmable peripheral interconnect (PPI)
- 12 bits ADC
- UART,SPI,I2C,QDEC, PDM
- SWD Debug interface
- BQB ,CE,FCC
- Size:

  12.7mm x 9.5mm (BTM020IQ2B)

18.5mm x 9.5mm (BTM020IQ2D)

- Operating temperature: -40℃ to +85℃

1.4 Applications

Smart home: heating control and lighting control

Health sensors: blood pressure, thermometer and glucose meters

Sports and fitness sensors: heart rate, runner speed and cadence, cycle speed and cadence

HID Devices: keyboards, mice, touchpads, remote controls.

Beacons.

2. General Specification

Bluetooth Specification	
Standard	Bluetooth 5.0（BLE only)
Protocols Supported	ATT, GATT, SMP, L2CAP, GAP.etc
Frequency Band	2.402GHz ~ 2.480GHz
Antenna	None(BTM020IQ2B)
	Microstrip antenna(BTM020IQ2D)
High System Clock	32MHz
Low System Clock	32.768kHz
Interface [a]	UART,PIO, SPI,AIO,I2S,PDM,ADC
Sensitivity	-96dBm
RF TX Power	-20~ 4dBm
Power	
Power Supply Voltage	1.7 ~ 3.6V DC
Deep Sleep Current	0.3uA in system off mode
Operating Environment	
Temperature	-40 ~85° C
Certifications	BQB/FCC/CE
Dimension	
BTM020IQ2B	9.5mm x 12.7mm
BTM020IQ2D	9.5mm x 18.5 mm
Weight	
BTM020IQ2B	TBD

BTM020IQ2D	TBD

Table 2: General Specification

a: interface definition is base on the software

3. Pin Configuration

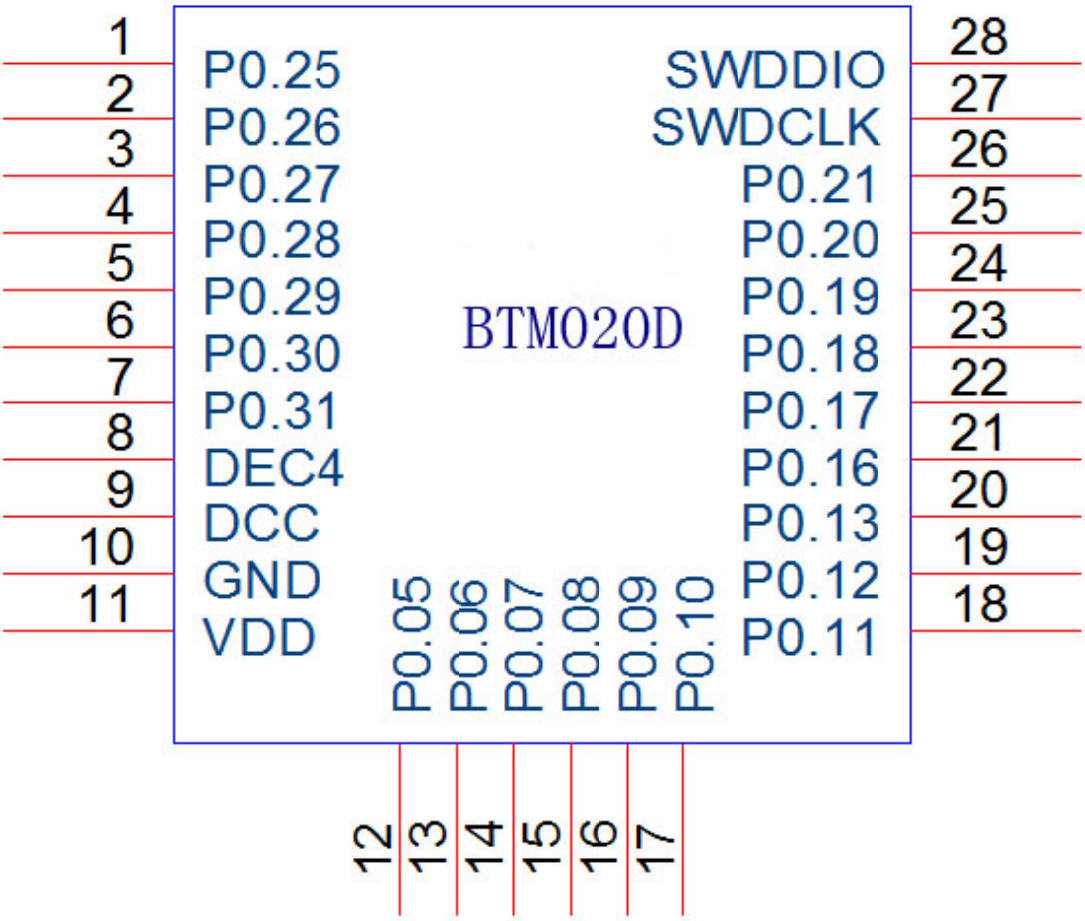


Figure 1: Pin Configuration of BTM020IQ2D

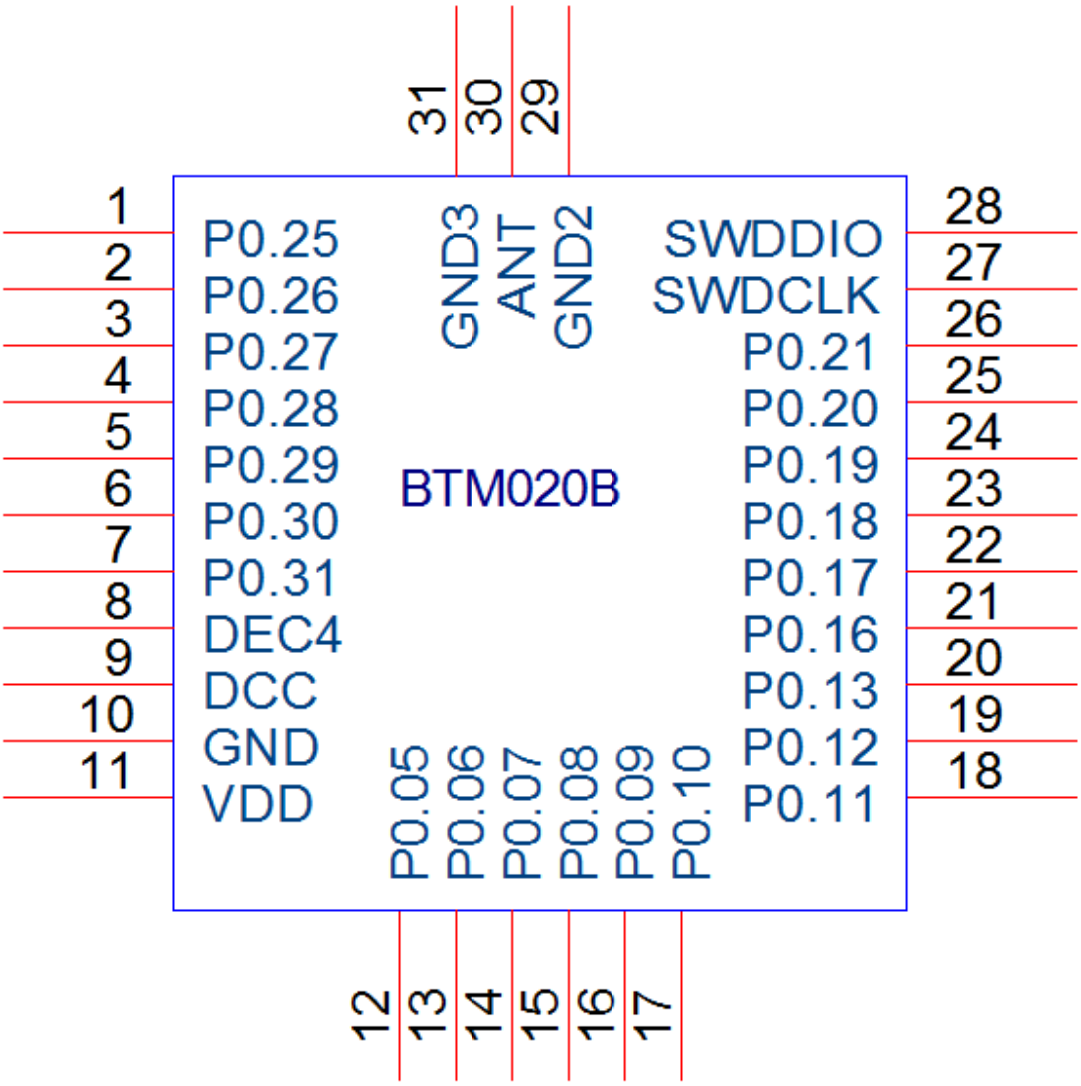


Figure 2: Pin Configuration of BTM020IQ2B

4. Pin Definition

4.1 BTM020IQ2D Pin Definition:

5. BTM020D Pin Description

PIN	Symbol	PIN Type	Description
1	P0.25	Digital I/O	* General purpose I/O
2	P0.26	Digital I/O	General purpose I/O
3	P0.27	Digital I/O	General purpose I/O
4	P0.28/ANI4	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
5	P0.29/ANI5	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
6	P0.30/ANI6	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
7	P0.31/ANI7	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
8	DEC	Power	1.3 V regulator supply decoupling Input from DC/DC regulator Output from 1.3 V LDO
9	DCC	Power	DC/DC regulator output
10	GND	Power	Ground
11	VDD	Power	Power supply
12	P0.05	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
13	P0.06	Digital I/O	General purpose I/O
14	P0.07	Digital I/O	General purpose I/O
15	P0.08	Digital I/O	General purpose I/O
16	P0.09 NFC1	Digital I/O NFC input	General purpose I/O NFC antenna connection
17	P0.10 NFC2	Digital I/O NFC input	General purpose I/O NFC antenna connection
18	P0.11	Digital I/O	General purpose I/O
19	P0.12	Digital I/O	General purpose I/O
20	P0.13	Digital I/O	General purpose I/O

21	P0.16	Digital I/O	General purpose I/O
22	P0.17	Digital I/O	General purpose I/O
23	P0.18/SWO	Digital I/O	General purpose I/O Single wire output
24	P0.19	Digital I/O	General purpose I/O
25	P0.20	Digital I/O	General purpose I/O
26	P0.21/NRESET	Digital I/O	General purpose I/O Configurable as pin reset
27	SWDCLK	Digital Input	Serial wire debug clock input for debug and programming
28	SWDDIO	Digital I/O	Serial wire debug I/O for debug and programming

Table 3: BTM020D Pin Definition

* Note: All general purpose I/O pins can be configured as special function peripherals except ADC and NFC.

5.1 BTM020B Pin Definition:

BTM020B Pin Description			
PIN	**Symbol**	**PIN Type**	**Description**
1	P0.25	Digital I/O	General purpose I/O
2	P0.26	Digital I/O	General purpose I/O
3	P0.27	Digital I/O	General purpose I/O
4	P0.28/ANI4	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
5	P0.29/ANI5	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
6	P0.30/ANI6	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
7	P0.31/ANI7	Digital I/O	General purpose I/O

		Analog input	SAADC/COMP/LPCOMP input
8	DEC	Power	1.3 V regulator supply decoupling Input from DC/DC regulator Output from 1.3 V LDO
9	DCC	Power	DC/DC regulator output
10	GND	Power	Ground
11	VDD	Power	Power supply
12	P0.05	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
13	P0.06	Digital I/O	General purpose I/O
14	P0.07	Digital I/O	General purpose I/O
15	P0.08	Digital I/O	General purpose I/O
16	P0.09 NFC1	Digital I/O NFC input	General purpose I/O NFC antenna connection
17	P0.10 NFC2	Digital I/O NFC input	General purpose I/O NFC antenna connection
18	P0.11	Digital I/O	General purpose I/O
19	P0.12	Digital I/O	General purpose I/O
20	P0.13	Digital I/O	General purpose I/O
21	P0.16	Digital I/O	General purpose I/O
22	P0.17	Digital I/O	General purpose I/O
23	P0.18/SWO	Digital I/O	General purpose I/O Single wire output
24	P0.19	Digital I/O	General purpose I/O
25	P0.20	Digital I/O	General purpose I/O
26	P0.21/NRESET	Digital I/O	General purpose I/O Configurable as pin reset
27	SWDCLK	Digital Input	Serial wire debug clock input for debug and programming
28	SWDDIO	Digital I/O	Serial wire debug I/O for debug and programming
29	GND	Power	Ground

30	ANT	RF	Single-ended radio antenna connection
31	GND	Power	Ground

Table 4: BTM020B Pin Definition

* Note: All General purpose I/O pins can be configured as special function peripherals except ADC and NFC**.**

5.2 GPIO Recommended Usage for BTM020B/D

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the Radio power supply and antenna pins.

PIN	GPIO	Recommended Usage
1	P0.25	Low drive, low frequency I/O only.
2	P0.26	
3	P0.27	
4	P0.28	
5	P0.29	
6	P0.30	
7	P0.31	

Table 5: GPIO Recommended Usage

6. Recommended Operating Conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Min	Nom	Max	Unit
VDD	Supply voltage independent of DCDC enable	1.7	3	3.6	V
t(R_VDD)	Supply rise time(0V to 1.7V)			60	ms
TA	Operating temperature	-40	25	85	℃

Table 6: Recommended Operating Conditions

7. Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

	Min.	Max.	Unit
Supply voltages			
VDD	-0.3	3.9	V
VSS		0	V
I/O pin voltage			
V(I/O), VDD ageabil	-0.3	VDD+0.3V	V
V(I/O), VDD >3.6 V	-0.3	3.9	V
NFC antenna pin current			
INFC1/2		80	mA
Radio			
RF input level		10	dBm
Environmental QFN48, 6tof the devic			
Storage temperature	-40	125	° 2
MSL (moisture sensitivity level)		3	
ESD HBM (human body model)		4	KV
ESD CDM (charged device model)		1000	V

Table 7: Absolute Maximum Ratings

8. Power Supply

This device has the following power supply features:

• On-chip LDO and DC/DC regulators

• Global System ON/OFF modes

• Individual RAM section power control for all system modes

• Analog or digital pin wakeup from System OFF

• Supervisor HW to manage power on reset, brownout, and power fail

• Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency

• Automatic switching between LDO and DC/DC regulator based on load to maximize efficiency.

8.1 Regulators

The following internal power regulator alternatives are supported:

• Internal LDO regulator

• Internal DC/DC regulator

The LDO is the default regulator. The DC/DC regulator can be used as an alternative to the LDO regulator and is enabled through the DCDCEN register. Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external inductance to be connected, as shown in below Figure:

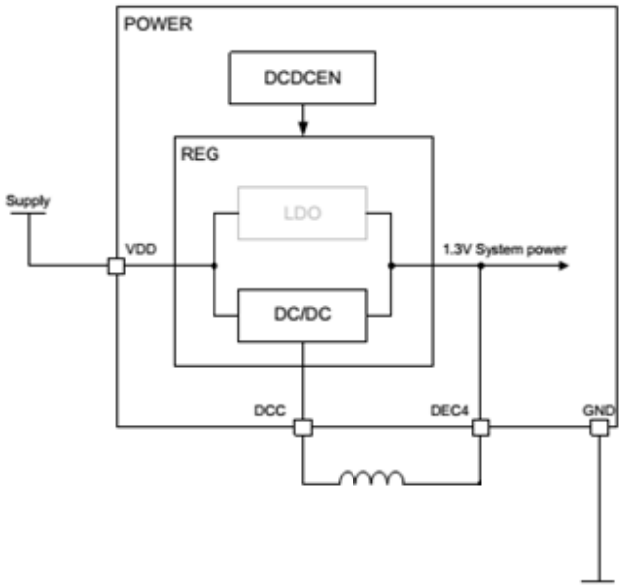


Figure 3: DC-DC Regulator Set Up

8.2 Power Supply Supervisor

The power supply supervisor initializes the system at power-on and provides an early warning of impending power failure.

In addition, the power supply supervisor puts the system in a reset state if the supply voltage is too low for safe operation (brownout).

8.3 System OFF Mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode, the device can be woken up through one of the following signals:

1. The DETECT signal, optionally generated by the GPIO peripheral
2. The ANADETECT signal, optionally generated by the LPCOMP module
3. The SENSE signal, optionally generated by the NFC module to "wake-on-field"
4. A reset

8.4 System ON Mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.

8.5 Power Supply Supervisor

The power supply supervisor initializes the system at power-on and provides an early warning of impending power failure. In addition, the power supply supervisor puts the system in a reset state if the supply voltage is too low for safe operation (brownout). The power supply supervisor is illustrated in Figure 6.

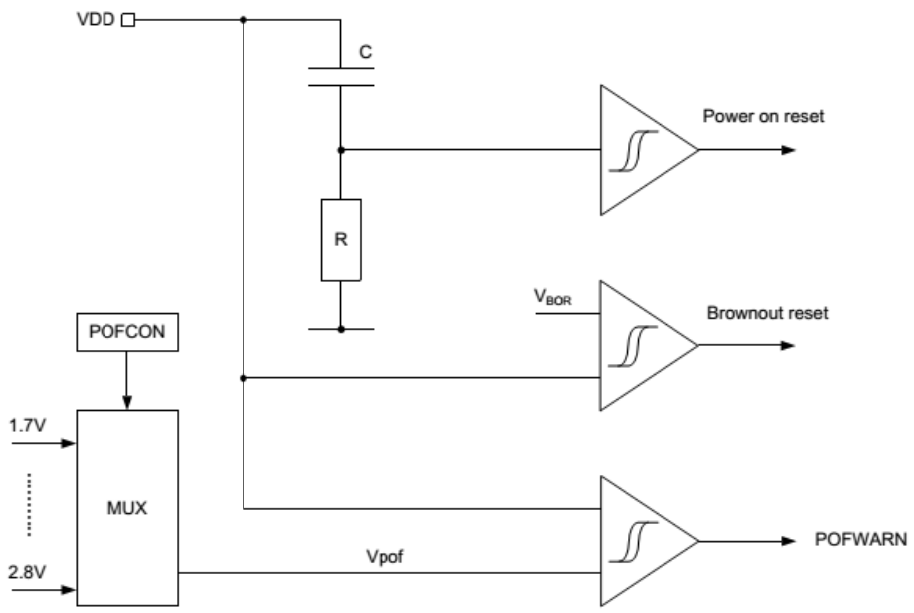


Figure 4: Power Supply Supervisor

8.6 Current Consumption Scenarios

Each scenario specifies a set of active operations and conditions applying to the given scenario. Current consumption scenarios, common condition shows the conditions used for a scenario unless otherwise is stated in the scenario description.

Condition	Value
VDD	3V
Temperature	25℃
CPU	WFI/WFE sleep
Peripherals	All idle
Clock	Not running
Regulator	DCDC

Table 8: Current Consumption Scenarios, Common Conditions

8.7 Electrical Specification

Symbol	Description	Min	Typ	Max	Unit
I(RADIO_TX0)	0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		7.1		mA
I(RADIO_TX1)	-40dBm Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		4.1		mA
I(RADIO_RX0)	Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFX		6.5		mA
I(S0)	CPU running CoreMark from Flash, Radio 0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO, Cache enabled		9.2		mA
I(S1)	CPU running CoreMark from Flash, Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO, Cache enabled		9.2		mA

Table 9: Current Consumption: Radio

Symbol	Description	Min	Typ	Max	Unit
ION_RAMOFF_EVENT	System ON, No RAM retention, Wake on any event		1.2		uA
ION_RAMON_EVENT	System ON, Full RAM retention, Wake on any event		1.5		uA
ION_RAMOFF_RTC	System ON, No RAM retention, Wake on RTC		1.9		uA
ION_RAMOFF_RESET	System OFF, No RAM retention, Wake on reset		0.3		uA
ION_RAMOFF_GPIO	System OFF, No RAM retention, Wake on GPIO		0.3		uA
ION_RAMOFF_LPCOMP	System OFF, No RAM retention, Wake on LPCOMP		1.9		uA
ION_RAMOFF_NF	System OFF, No RAM retention, Wake on NFC field		0.7		uA
ION_RAMOFF_RESET	System OFF, Full 64 kB RAM retention, Wake on reset		0.7		uA

Table 10: Current Consumption: Ultra-Low Power

9. Reset

There are multiple sources that may trigger a reset.

9.1 Power-On Reset

The power-on reset generator initializes the system at power-on. The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started. A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

9.2 Pin Reset

A pin reset is generated when the physical reset pin on the device is asserted.

Note: Pin reset is not available on all pins.

9.3 Wakeup From System OFF Mode Reset

The device is reset when it wakes up from System OFF mode.

The DAP is not reset following a wake up from System OFF mode if the device is in debug interface mode.

9.4 Soft Reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM®core is set.

9.5 Watchdog Reset

A Watchdog reset is generated when the watchdog times out.

9.6 Brown-Out Reset

The brown-out reset generator puts the system in reset state if the supply voltage drops below the brownout reset (BOR) threshold.

10. Reference Circuitry

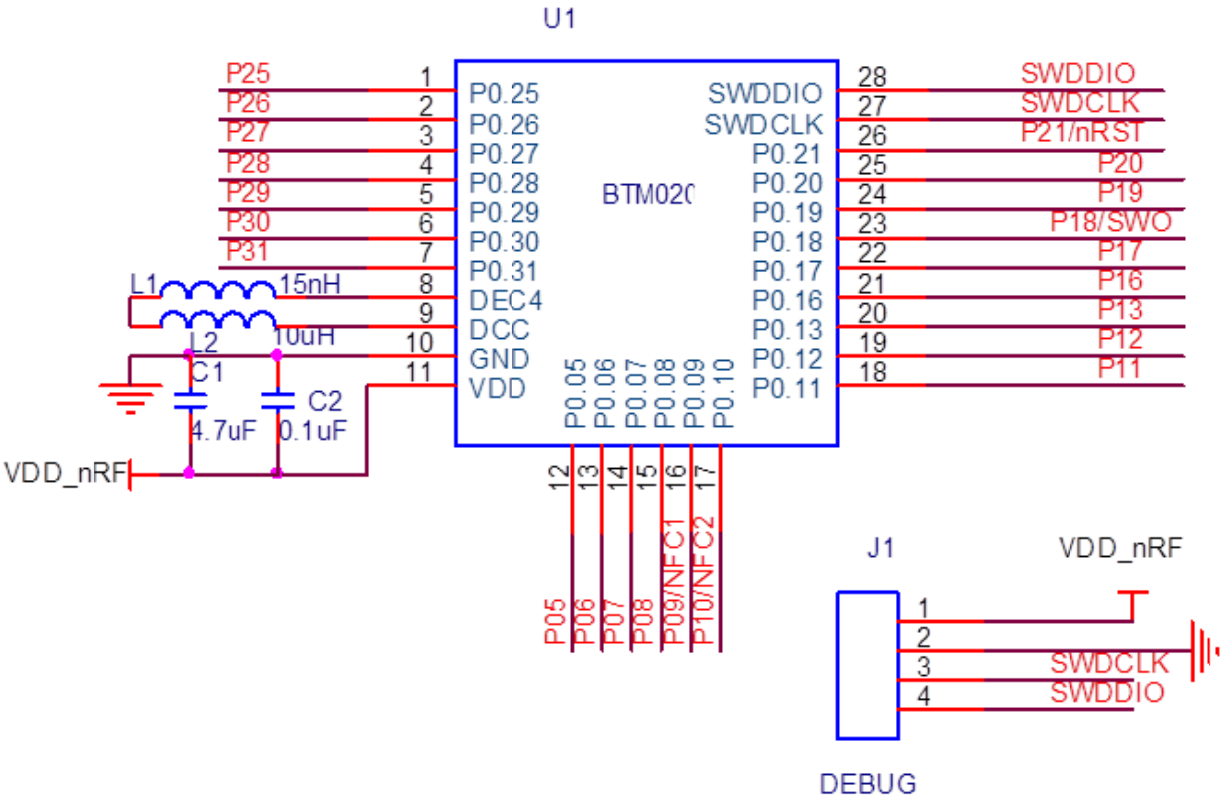


Figure 5: BTM020D With DC-DC Regulator Setup

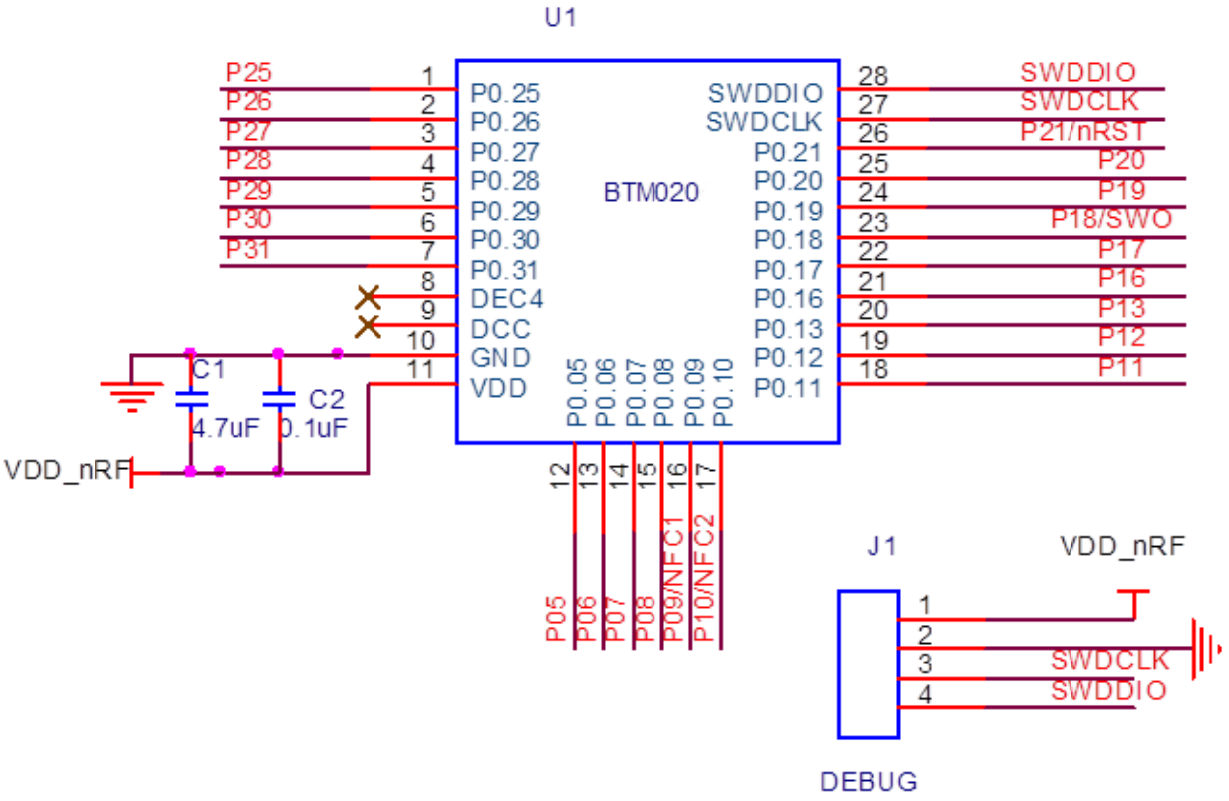


Figure 6: BTM020D With Internal LDO Setup

11. RF Layout And Placement

Special attention must be paid to the placement and design of the carrier board. Proper design and layout of the module will help provide the performance and range expected of the module.

The area of the board directly underneath the antenna should be clear of copper on all layers. Keep metal away from the antenna as these will affect the radiation pattern and other performance. The best performance is obtained by having the antenna overhang the carrier board so that it is in air. If this is no possible, a cutout is the best alternative.

11.1 Module Placement Recommendations

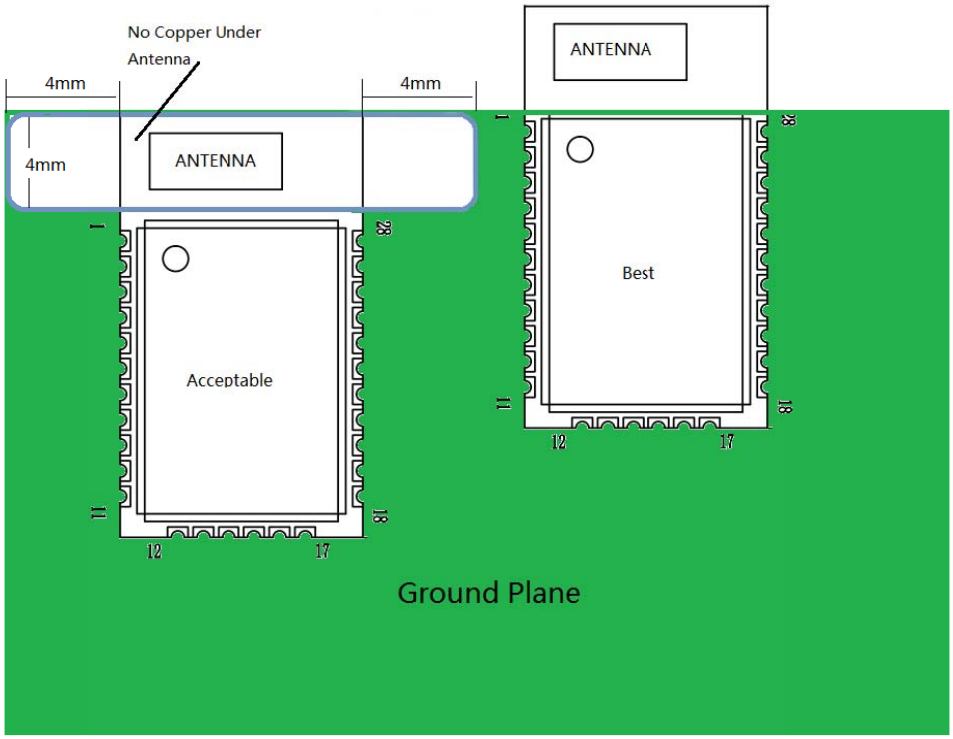
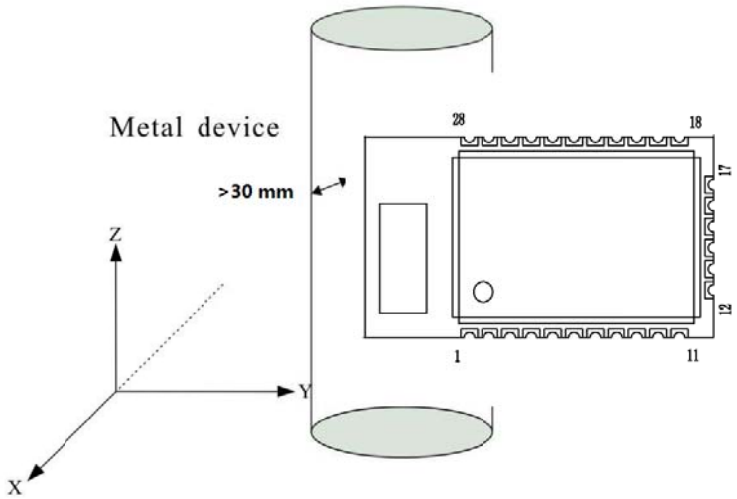


Figure 7: Module Mounting Options

11.2 Effect of Metals Nearby

Another significant source of issues for RF is the presence of metal near the antenna. Metal also produces an effect on the electric field and change the radiation pattern or create nulls where no signal is received. Any nearby metal may affect the antenna significantly and reduce the range. It's therefore critical to keep any metal way at least 30mm from the module. Your design should place any metal as far away as possible.



Leave 30mm Clearance Space from the Module Built-in Antenna

Figure 8: Keep Any Metal Away At Least 30mm From The Module

12. Mechanical Specifications

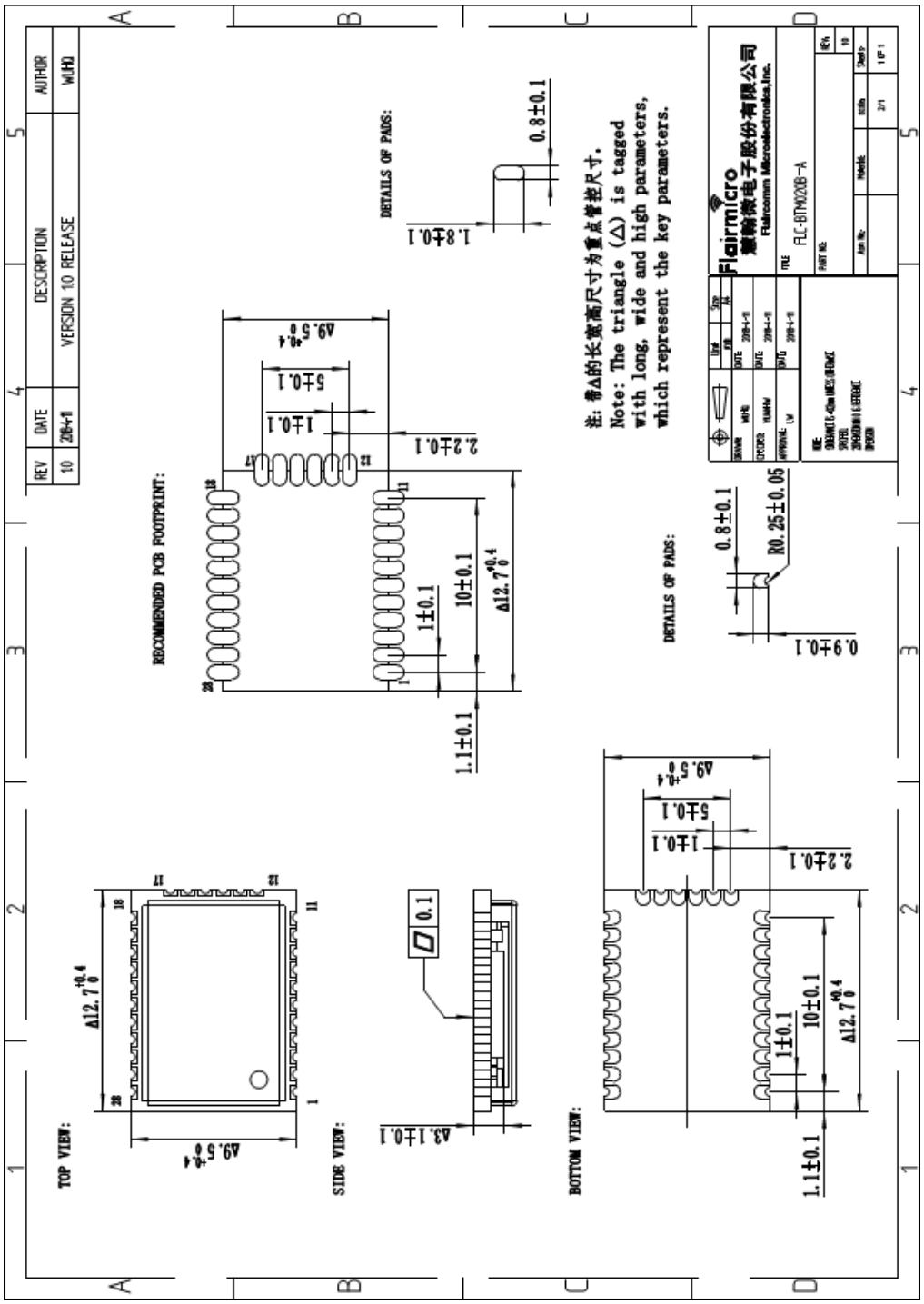


Figure **12**: Mechanical Characteristics (BTM020B)

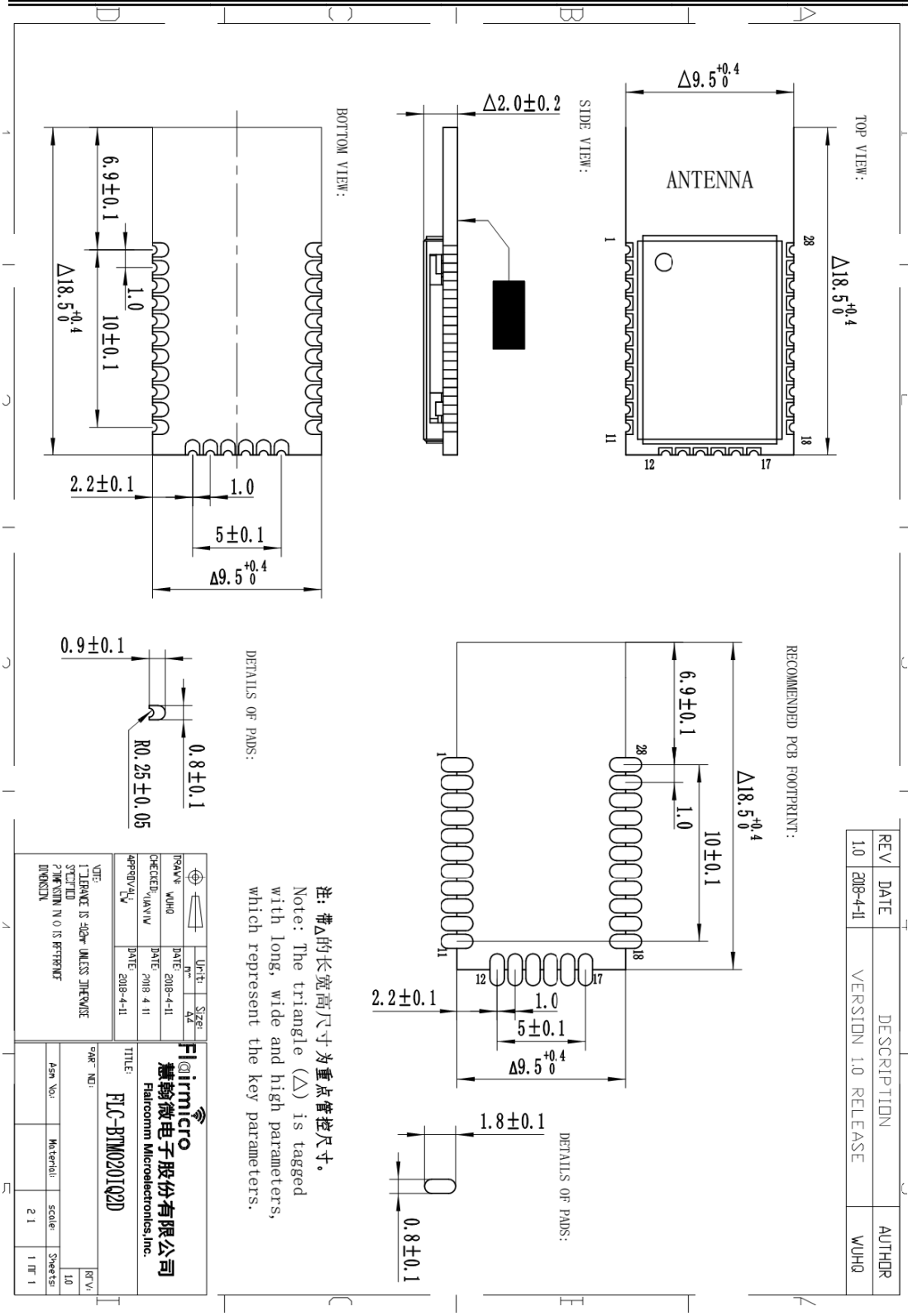


Figure 13: Mechanical Characteristics (BTM020D)

Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

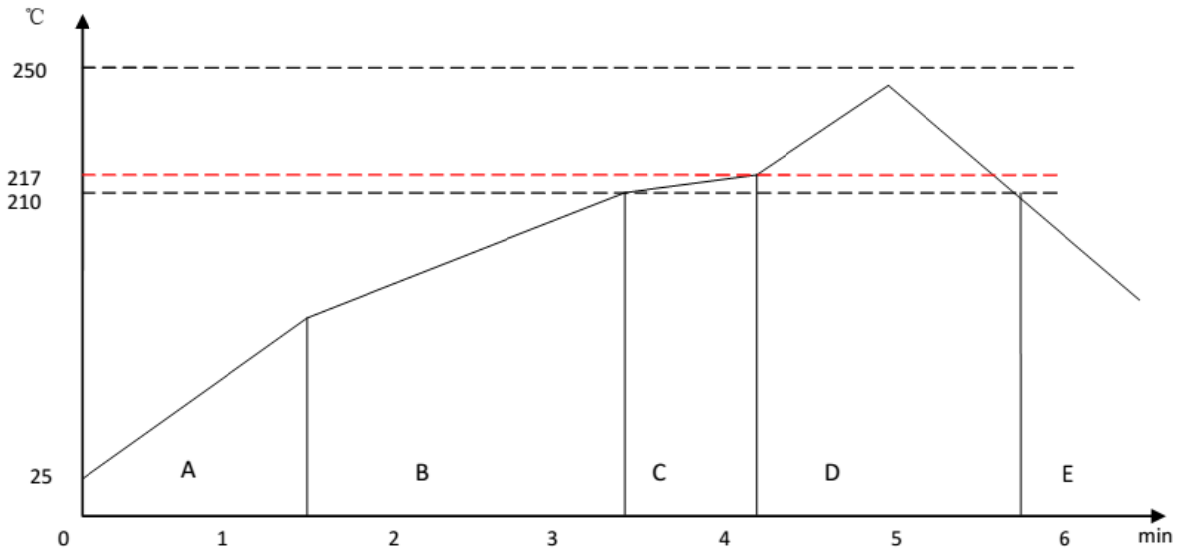


Figure 14: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, typically 0.5 – 2 ℃/s. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 ℃. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re -oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. The temperature is recommended to be 150℃to 210℃ for 60 to 120 second for this zone.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217℃ for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.

The recommended peak temperature (Tp) is 230 ~ 250℃. The soldering time should be 30 to 90 second when the temperature is above 217℃.

Cooling Zone (E) —The cooling ate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical cooling rate should be 4 ℃.

13. Ordering Information

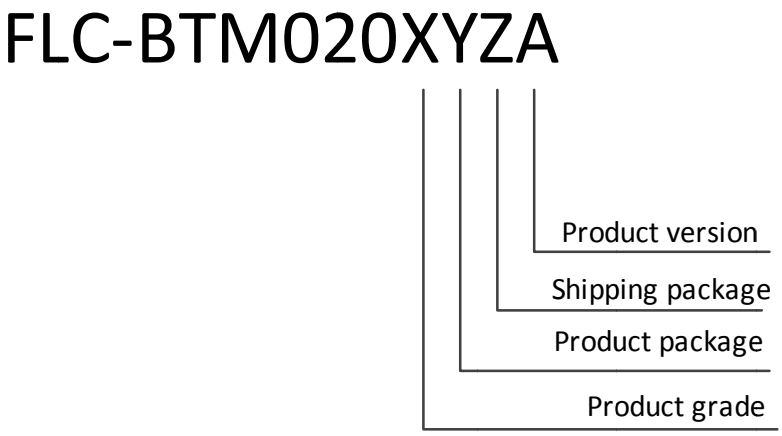


Figure 15: Ordering Information

13.1 Product Revision

Product Revision	Description	Availability
A	BTM020IQ2A with chip antenna	NO
B	BTM020IQ2B without antenna	YES
D	BTM020IQ2D with microstrip antenna	YES

Table 11: Product Revision

13.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Foam Tray	TBD	TBD
1	Plastic Tray	TBD	TBD
2	Tape	TBD	TBD

Table 12: Shipping Package

13.3 Product Package

Product Package	Description	Availability
Q	QFN	YES
L	LGA	NO
B	BGA	NO
C	Connector	NO

Table 13: Product Package

13.4 Product Grade

Product Grade	Description	Availability
C	Consumer	No
I	Industrial	Yes
V	Automobile After-Market	No
A	Automobile Before-Market	No

Table 14: Product Grade

14. Cautions &Warnings

14.1 FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference.

(2) this device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

14.2 Host labeling requirement

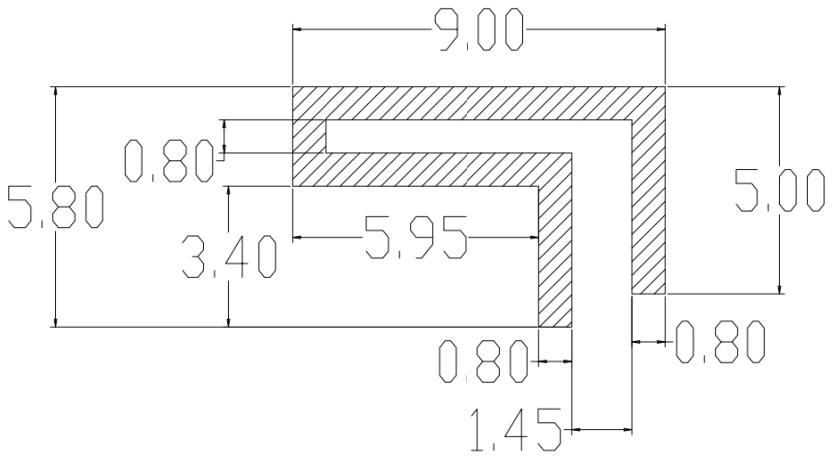
(A) Host labeling requirement: Contains FCC ID: P4I-BTM020

The module “FLC-BTM020IQ2B” has no antenna structure itself, only the host with qualified trace antenna design is applicable. CIIPC or new filing may be required for host device.”

(B) If the modular transmitter uses an electronic display of the FCC identification number, the information must be readily accessible and visible on the modular transmitter or on the device in which it is installed. If the module is installed inside another device, then the outside of the device into which the module is installed must display a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains FCC certified transmitter module(s).”

14.3 Trace antenna design

This antenna is a microstrip antenna which can be used with all 2.4GHz transceivers and transmitters.



The trace from the antenna port of the module to an external antenna should be 50Ω.

Gain Efficiency

f(MHz)	Eff	Ave Gain
2400	65%	-1.8
2410	65%	-1.9
2420	64%	-1.9
2430	65%	-1.9
2440	63%	-2.0
2450	62%	-2.1
2460	60%	-2.2
2470	61%	-2.2
2480	62%	-2.1
2490	63%	-2.0
2500	64%	-2.0
AVE	63%	-2.0

Warning

Please note that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.