Revision history

0	12/20/2014	Initial version

1. Overview

In translation

2. Features

Operating voltage : 3.3V
Operating temperature : 0 - 85 °C
CPU Cortex-M4 @ 120MHz
- Flash 512KB
- Memory 128KB

Wi-Fi system
- IEEE 802.11b/g/n
- Single stream 1x1
- Single-band 2.4GHz
- Green Tx power saving mode
- Low power listen mode
- Data rates up to 150Mbps
- Data rates up to 1-52Mbps for 802.11 b/g, data rates up to 150Mbps for 802.11n (MCS0-7).
- Networking protocol support : IPv4/IPv6, TCP/UDP, ARP/NDP, DHCPv4, ICMPv6
- Full security support : WPS, WPA, WPA2, WAPI, WEP, TKIP
- Each Tx power calibrated

Software and stack
- Real Time OS : MQX
- Architecture of internet software : Alljoyn
- iOS homekit frame and MFi supported
- Bootloader encrypted with RSA2048/SHA-256
- Update firmware via WiFi or UART
- Drivers of interfaces of MCU

Suitable integrated development environment
- IAR EWARM V7.10 or above
- GCC ARM V4.8.4 or above

3. Hardware Specification

3.1 System block diagram

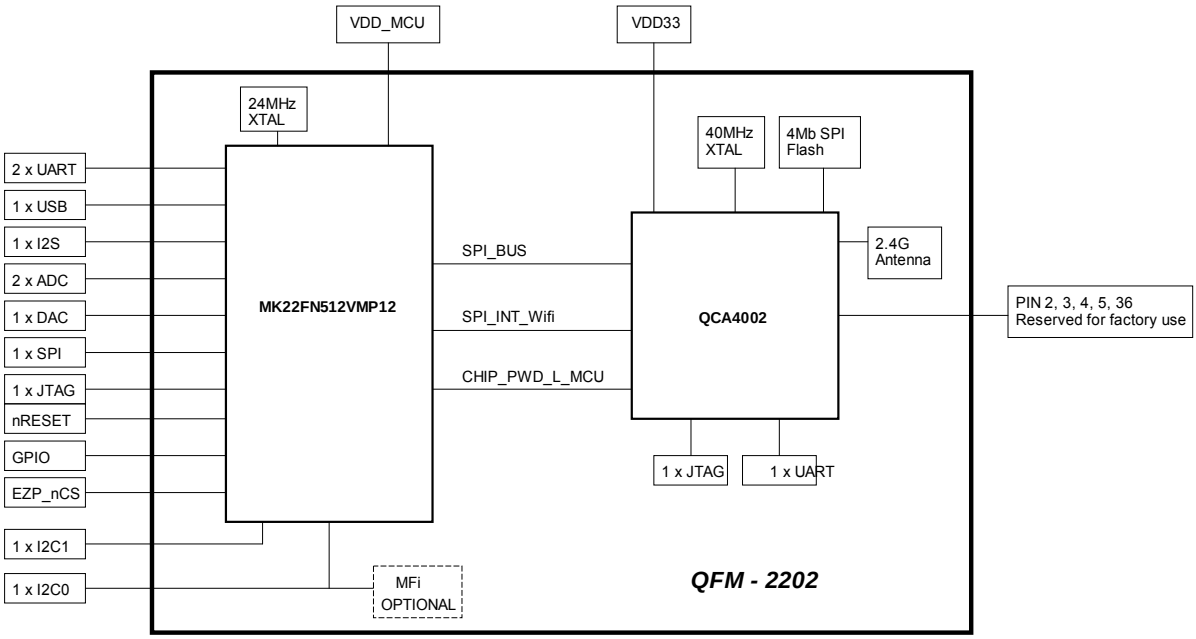

Figure-1 QFM-2202 system block diagram

3.2 Module signal description

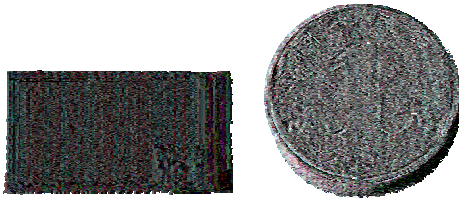

Figure-2 QFM-2202 top view

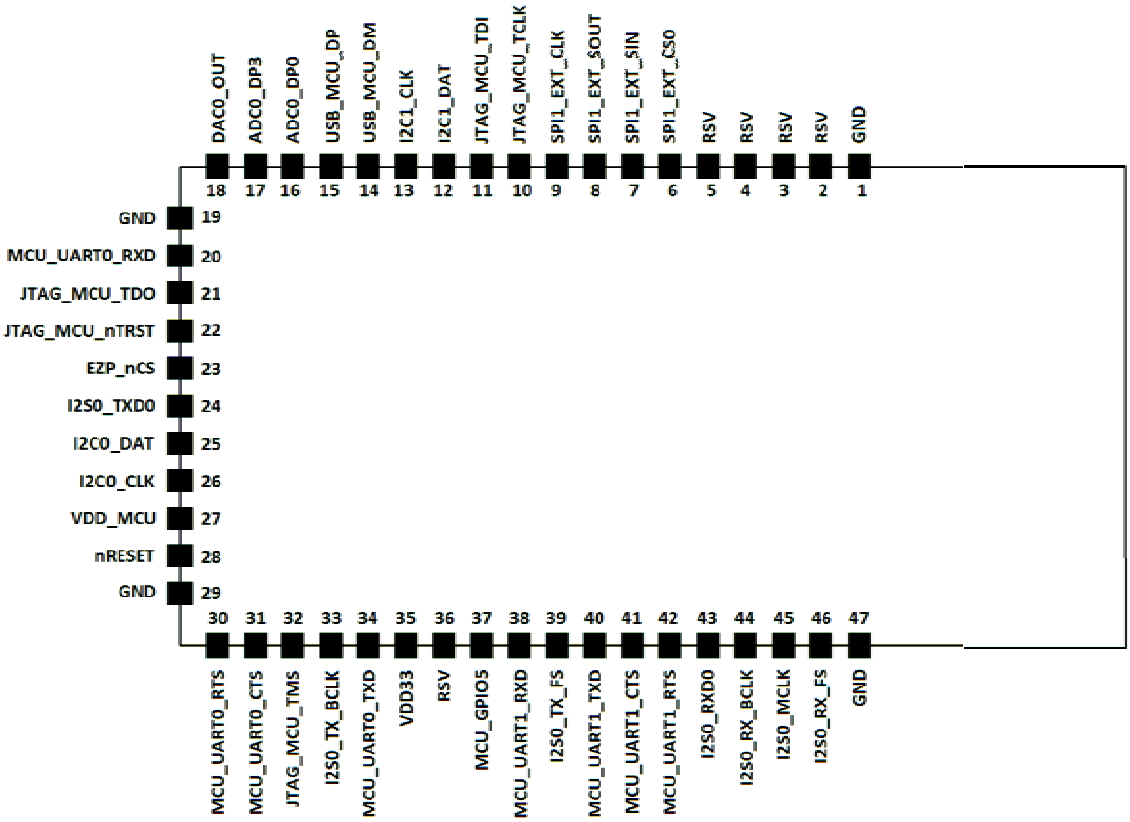

Figure-3 QFM-2202 pinout top view

Table-1 QFM-2202 pin assignment and description

Signal name	Pin	Type	Description
GND	1, 19, 29, 47	Power	Ground
VDD_MCU	27	Power	3.3V power supply for K22
VDD33	35	Power	3.3V power supply for QCA4002
RSV	2, 3, 4, 5, 36	N/A	Reserved for factory use, NC
USB_MCU_DM	14		USB FS/LS OTG controller with onchip transceiver.
USB_MCU_DP	15		
ADC0_DP0	16	AI	16-bit SAR ADCs converting at 1.2 MS/s in 12bit mode.
ADC0_DP3	17	AI	
DAC0_OUT	18	AO	12-bit DAC.
nRESET	28	DI	K22 POR reset, active LOW.
EZP_nCS [1]	23	DI [2]	EzPort Chip Select
SPI1_EXT_CS0	6	DIO [2]	Peripheral Chip Select
SPI1_EXT_SIN	7	DI [2]	Serial Data In
SPI1_EXT_SOUT	8	DO [2]	Serial Data Out
SPI1_EXT_CLK	9	DIO [2]	Serial Clock
JTAG_MCU_TCLK	10	DI [2]	JTAG Test Clock / Serial Wire Clock
JTAG_MCU_TDI	11	DI [2]	JTAG Test Data Input
JTAG_MCU_TDO	21	DO [2]	JTAG Test Data Output
JTAG_MCU_nTRST	22	DI [2]	JTAG Reset
JTAG_MCU_TMS	32	DIO [2]	JTAG Test Mode Selection / Serial Wire Data
I2C1_DAT	12	DIO [2]	Bidirectional serial data line of the I2C system
I2C1_CLK	13	DIO [2]	Bidirectional serial clock line of the I2C system
I2C0_DAT	25	DIO [2]	Bidirectional serial data line of the I2C system
I2C0_CLK	26	DIO [2]	Bidirectional serial clock line of the I2C system
MCU_UART0_RXD	20	DI [2]	Receive data
MCU_UART0_RTS	30	DO [2]	Request to send
MCU_UART0_CTS	31	DI [2]	Clear to send
MCU_UART0_TXD	34	DO [2]	Transmit data
MCU_UART1_RXD	38	DI [2]	Receive data
MCU_UART1_TXD	40	DO [2]	Transmit data
MCU_UART1_CTS	41	DI [2]	Clear to send
MCU_UART1_RTS	42	DO [2]	Request to send
I2S0_TXD0	24	DO [2]	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word.
I2S0_TX_BCLK	33	DIO [2]	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.
I2S0_TX_FS	39	DIO [2]	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.
I2S0_RXD0	43	DI [2]	Receive Data. The receive data is sampled synchronously by the bit clock.
I2S0_RX_BCLK	44	DIO [2]	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.
I2S0_MCLK	45	DIO [2]	Audio Master Clock. The master clock is an input when externally generated and an output when

			internally generated.
I2S0_RX_FS	46	DIO [2]	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.
MCU_GPIO5	37	DIO [2]	

[1] Minimum 2 bus clock cycles of EZP_nCS=0 after reset will force K22 enter into EZP mode.

[2] All IOs are with multiplexed functions. See table-2 for details.

3.3 Module GPIO pin functions

Table-2 QFM-2202 GPIO pin functions

Signal	Pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
EZP_nCS	23	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
SPI1_EXT_CS0	6	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN	SPI1_PCS0	
SPI1_EXT_SIN	7	DISABLED		PTD7		UART0_TX	FTM0_CH7		FTM0_FLT1	SPI1_SIN	
SPI1_EXT_SOUT	8	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
SPI1_EXT_CLK	9	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b	SPI1_SCK	
JTAG_MCU_TCLK	10	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
JTAG_MCU_TDI	11	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
JTAG_MCU_TDO	21	JTAG_TDO/ TRACE_SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
JTAG_MCU_nTRST	22	DISABLED		PTA5	USB_CLKIN	FTM0_CH2			I2S0_TX_BCLK	JTAG_TRST_b	
JTAG_MCU_TMS	32	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
I2C1_DAT	12	ADC1_SE4a	ADC1_SE4a	PTE0/ CLKOUT32K	SPI1_PCS1	UART1_TX			I2C1_SDA	RTC_CLKOUT	
I2C1_CLK	13	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			I2C1_SCL	SPI1_SIN	
I2C0_DAT	25	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
I2C0_CLK	26	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA		
MCU_UART0_RXD	20	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0	FB_AD17	EWM_IN		
MCU_UART0_RTS	30	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
MCU_UART0_CTS	31	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b			FTM0_FLT0		
MCU_UART0_TXD	34	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1	FB_AD16	EWM_OUT_b		
MCU_UART1_RXD	38	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK	LPUART0_RX	
MCU_UART1_TXD	40	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT	LPUART0_TX	
MCU_UART1_CTS	41	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12	I2S0_TX_FS	LPUART0_CTS_b	
MCU_UART1_RTS	42	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13	I2S0_TXD0	LPUART0_RTS_b	
I2S0_TXD0	24	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_PHA	
I2S0_BCLK	33	DISABLED		PTB18		FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_PHA		
I2S0_TX_FS	39	DISABLED		PTB19		FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
I2S0_RXD0	43	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT	FTM0_CH2	
I2S0_RX_BCLK	44	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	FB_AD9	I2S0_MCLK		
I2S0_MCLK	45	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7			
I2S0_RX_FS	46	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS	FB_AD8			
MCU_GPIO5	37	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG	USB_SOF_OUT	FB_AD14			

3.4 Electrical characteristics

3.4.1 Absolute maximum ratings

Table-3 QFM-2202 absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{DD_MCU}	MCU Supply Voltage	-0.3	3.8	V
V_{DD33}	QCA4002 Supply Voltage	-0.3	4.0	V
V_{DIO}	Digital Input Voltage	-0.3	V_{DD_MCU} + 0.3	V
V_{AIO}	Analog [1]	-0.3	V_{DD_MCU} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{USB_DP}	USB_DP Input Voltage	-0.3	3.63	V
V_{USB_DM}	USB_DM Input Voltage	-0.3	3.63	V

[1] Analog pins are defined as pins that do not have an associated general purpose I/O port function.

3.4.2 Recommended operating conditions

Table-4 QFM-2202 recommended operating conditions

Symbol	Description	Min.	Max.	Unit
V_{DD_MCU}	MCU Supply Voltage	2.7	3.6	V

V_{DD33}	QCA4002 Supply Voltage	3.14	3.46	V
T_{STG}	Storage temperature	- 40	135	°C
T_A	Operating Temperature	0	85	°C

3.4.3 DC electrical characteristics

Table-5 QFM-2202 DC electrical characteristics

Symbol	Description	Min.	Max.	Unit
V_{IH}	Input High Voltage	0.7 x V_{DD_MCU}	—	V
V_{IL}	Input Low Voltage	—	0.35 x V_{DD_MCU}	V
V_{OH}	Output high voltage			
	Normal drive pad (I_{OH} = -5mA)	V_{DD_MCU} - 0.5	—	V
	High drive pad (I_{OH} = -20mA)	V_{DD_MCU} - 0.5	—	
V_{OL}	Output low voltage			
	Normal drive pad (I_{OH} = 5mA)	—	0.5	V
	High drive pad (I_{OH} = 20mA)	—	0.5	
I_{OHT}	Output high current total for all ports	—	100	mA
I_{OLT}	Output low current total for all ports	—	100	mA
I_{IN}	Input leakage current (per pin) for full temperature range			
	All pins other than high drive port pins	—	0.5	uA
	High drive port pins	—	0.5	
I_{IN}	Input leakage current (total all pins) for full temperature range	—	1.0	uA
R_{PU}	Internal pullup resistors	20	50	kΩ
R_{PD}	Internal pulldown resistors	20	50	kΩ
V_{HYS}	Input Hysteresis	0.06 x V_{DD_MCU}	—	V
I_{ICIO}	Analog and I/O pin DC injection current - single pin			
	V_{IN} < V_{SS} - 0.3V (Negative current injection)	-3	—	mA
	V_{IN} > V_{DD_MCU} + 0.3V (Positive current injection)	—	+3	
I_{ICcont} [1]	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins			mA
	Negative current injection	-25	—	
	Positive current injection	—	+25	
V_{ODPU}	Open drain pullup voltage level	V_{DD_MCU}	V_{DD_MCU}	V
V_{RAM}	V_{DD_mcu} voltage required to retain RAM	1.2	—	V
V_{POR} [2]	Falling V_{DD_mcu} POR detect voltage	0.8	1.5	V

[1] All analog and I/O pins are internally clamped to V_{SS} and V_{DD_mcu} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{INVIO\_MAX})/|I_{ICIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

[2] Typical value is 1.1V.

3.5 Power up sequence

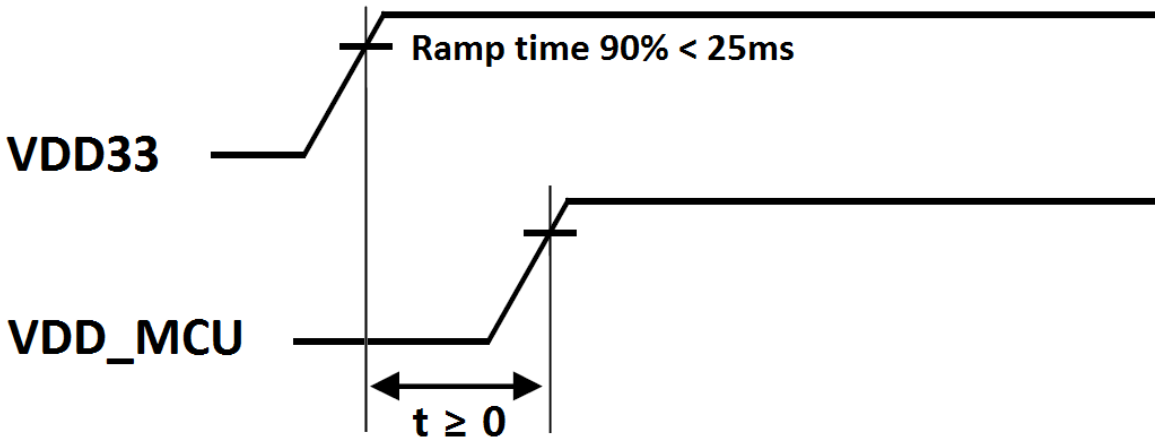

Figure-4 QFM-2202 power up sequence

3.6 Power consumption

3.6.1 Operating power consumption

Table-6 QFM-2202 operating power consumption

Mode	Standard	Rate	Typ	Unit
Tx	11b	1	247.6	mA
		11	241.2	
	11g	6	246.1	
		54	210.6	
	11n HT20	MCS0	263.0	
		MCS7	217.3	
	11n HT40	MCS0	221.5	
		MCS7	195.5	
Rx	All rates		66.7	mA

3.6.2 Standby power consumption

Table-7 QFM-2202 standby power consumption

Mode	State	Typical current consumption for SPI/UART at 3.3V				
Standby	CHIP_PWD	5uA				
	HOST_OFF	50uA				
	SLEEP	130uA				
Power Save Mode (2.4G) (Low Power Listen disabled) [1]	DTIM period	Current Cons. (uA)	T1 (ms)	T2 (ms)	Tbeacon (ms)	T3 (ms)
	DTIM 1	1090	2.01	0.36	0.99	0.39
	DTIM 3	473	1.99	0.32	1.06	0.41
	DTIM 5	335	1.99	0.30	1.01	0.41
	DTIM 10	258	1.97	0.43	0.97	0.47

[1] Numbers are for switch mode.

3.7 RF characteristics RF

3.7.1 Wireless LAN radio configuration and general specifications

Table-8 Wireless LAN radio configuration and general specifications

Item	Specification		Unit
Country/Domain Code [1]	Reserved		—
Center Frequency	11b	2.412-2.472	GHz
	11g	2.412-2.472	GHz
	11n HT20	2.412-2.472	GHz
	11n HT40	2.422-2.452	GHz
Rate	11b	1, 2, 5.5, 11	Mbps
	11g	6, 9, 12, 18, 24, 36, 48, 54	Mbps
	11n 1stream	MCS0, 1, 2, 3, 4, 5, 6, 7	Mbps
Modulation type	11b	DSSS (CCK, DQPSK, DBPSK)	—
	11g/n	OFDM (64QAM, 16QAM, QPSK, BPSK)	—

[1] This code will be written during calibration.

3.7.2 radio Tx characteristics

Table-9 radio Tx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Tx output frequency range	—	2.412	—	2.484	GHz
P_{out}	Output power [1]					
	11b	1 Mbps	—	19	—	dBm
		11 Mbps	—	19	—	dBm
	11g	6 Mbps	—	19	—	dBm
		54 Mbps	—	18	—	dBm
	11n HT20	MCS0	—	20	—	dBm
		MCS7	—	17	—	dBm
	11n HT40	MCS0	—	17	—	dBm
		MCS7	—	14	—	dBm

[1] Performance calculated at the balun. Loss from balun to antenna connector in the test board is 1.2 dB (2.4GHz).

3.7.3 radio Rx characteristics

Table-10 radio Rx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Rx input frequency range	—	2.412	—	2.484	GHz
S_{rf}	Sensitivity [1]					
	CCK	1 Mbps				
		2 Mbps				
		5.5 Mbps				
		11 Mbps				
	OFDM	6 Mbps				
		9 Mbps				
		12 Mbps				
		18 Mbps				
		24 Mbps				
		36 Mbps				
		48 Mbps				
		54 Mbps				
	HT20	MCS0				
		MCS1				

		MCS2				
		MCS3				
		MCS4				
		MCS5				
		MCS6				
		MCS7				
	HT40	MCS0				
		MCS1				
		MCS2				
		MCS3				
		MCS4				
		MCS5				
		MCS6				
		MCS7				

[1] Performance measured at the balun. Loss from balun to antenna connector in the test board is 1.2 dB (2.4GHz).

4. Layout guide

1）The antenna area should be towards outside of base board. The distance from pin1 or pin47 to edge of board should be smaller than 2mm.

2）Red rectangle is the clearance area: on the base board, top and internal layers of the red rectangle should have no shapes or clines; the bottom layer of the red rectangle should have a whole ground shape.

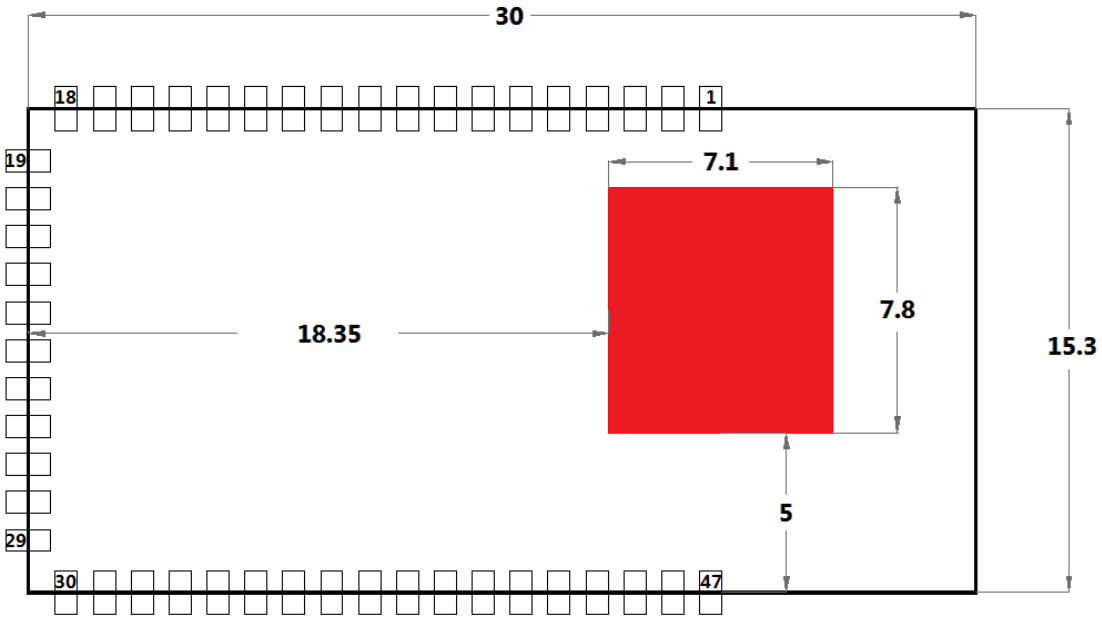

Figure-5 QFM-2202 clearance area for base board

5. Mechanical interface specification

5.1 QFM-2202 module dimensions

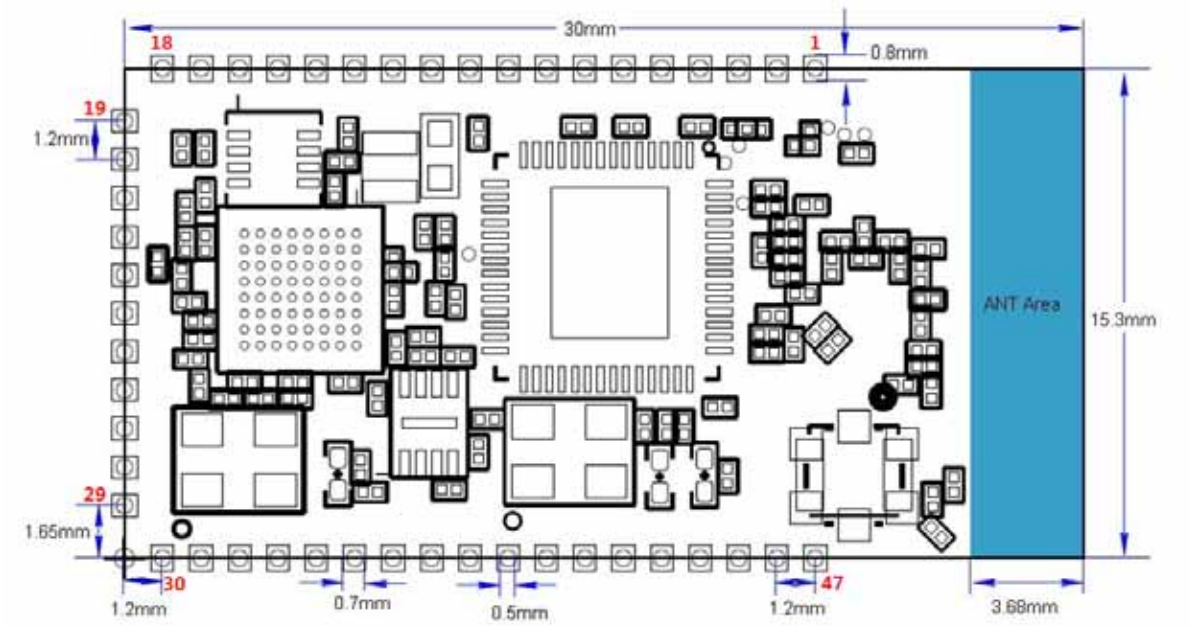

Figure-6 QFM-2202 module dimensions top view

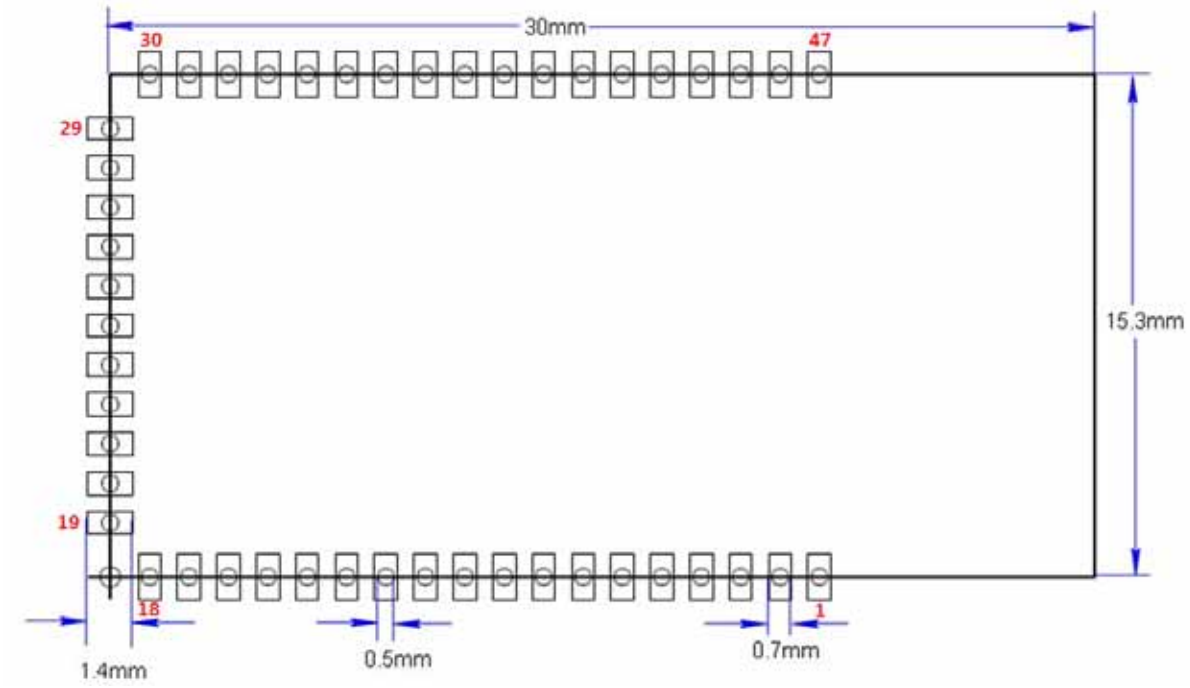

Figure-7 QFM-2202 module dimensions bottom view

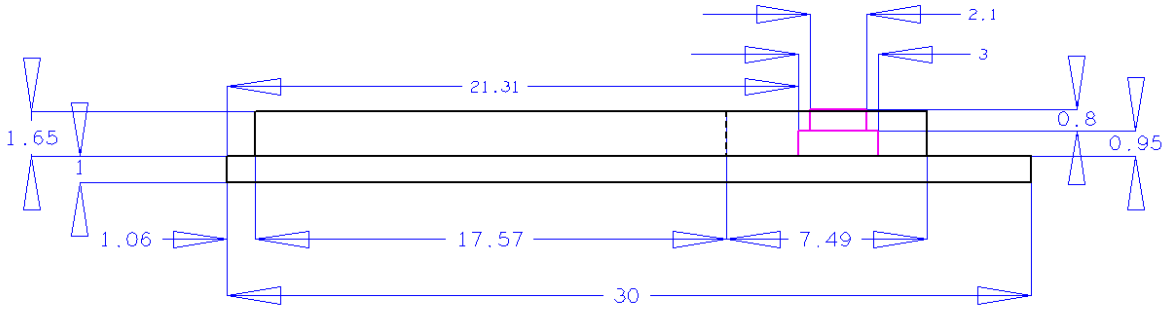

Figure-8 QFM-2202 module dimensions side view (unit: mm)

6. Ordering Information

Part number	Temperature	Package	MFi & HomeKit
QFM-2202	0 to 85 °C		Not Available
QFM-2202-A	0 to 85 °C		Available

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digi tal device, pursuant to part 15 of the FCC rules. These limits are designed to provide r easonable protection against harmful interference in a residential installation. This equ ipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio co mmunications. However, there is no guarantee that interference will not occur in a par ticular installation. If this equipment does cause harmful interference to radio or televi sion reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measu res: -Reorient or relocate the receiving antenna. -
Increase the separation between the equipment and receiver. -
Connect the equipment into an outlet on a circuit different from that to which the recei ver is connected. -Consult the dealer or an experienced radio/TV technician for help.

You are cautioned that changes or modifications not expressly approved by the party r esponsible for compliance could void your authority to operate the equipment.

FCC RF Radiation Exposure Statement: 1. This Transmitter must not be co-
located or operating in conjunction with any other antenna or transmitter. 2.
This equipment complies with FCC RF radiation exposure limits set forth for an unco ntrolled environment. This equipment should be installed and operated with a minimu m distance of 20 centimeters between the radiator and your body.

Information to OEM integrator
The OEM integrator has to be aware not to provide information to the end user regard ing how to install or remove this RF module in the user manual of the end product. Th e user manual which is provided by OEM integrators for end users must include the fo llowing information in a prominent location.
1. To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co- located or operating in conjunction with any other antenna or transmitter, except in accordance with FCC multi-transmitter product

transmitter product procedures.

2. Only those antennas with same type and lesser gain filed under this FCC ID number c an be used with this device.

3. The regulatory label on the final system must include the statement: “Contains FCC I D: RUN-QFM2202“.

4. The final system integrator must ensure there is no instruction provided in the user manual or customer documentation indicating how to install or remove the transmitter module except such device has implemented two-ways authentication between module and the host system.