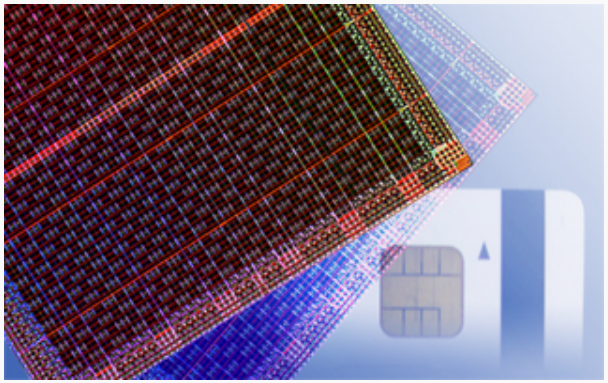
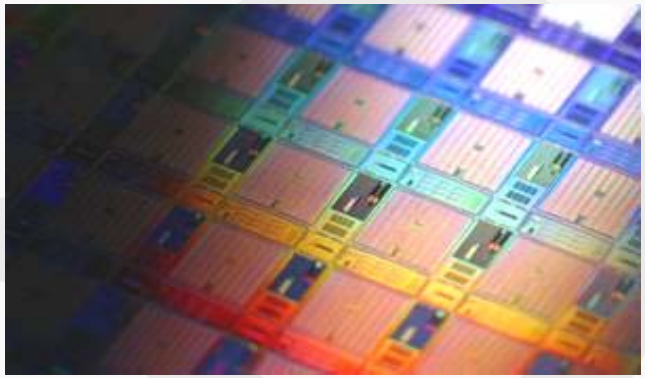
FUJITSU THE POSSIBILITIES ARE INFINITE





65nm CMOS Process Technology

Paul Kim
Senior Manager, Foundry Services
Fujitsu Microelectronics America, Inc.

New 300mm Fabs – Mie, Japan

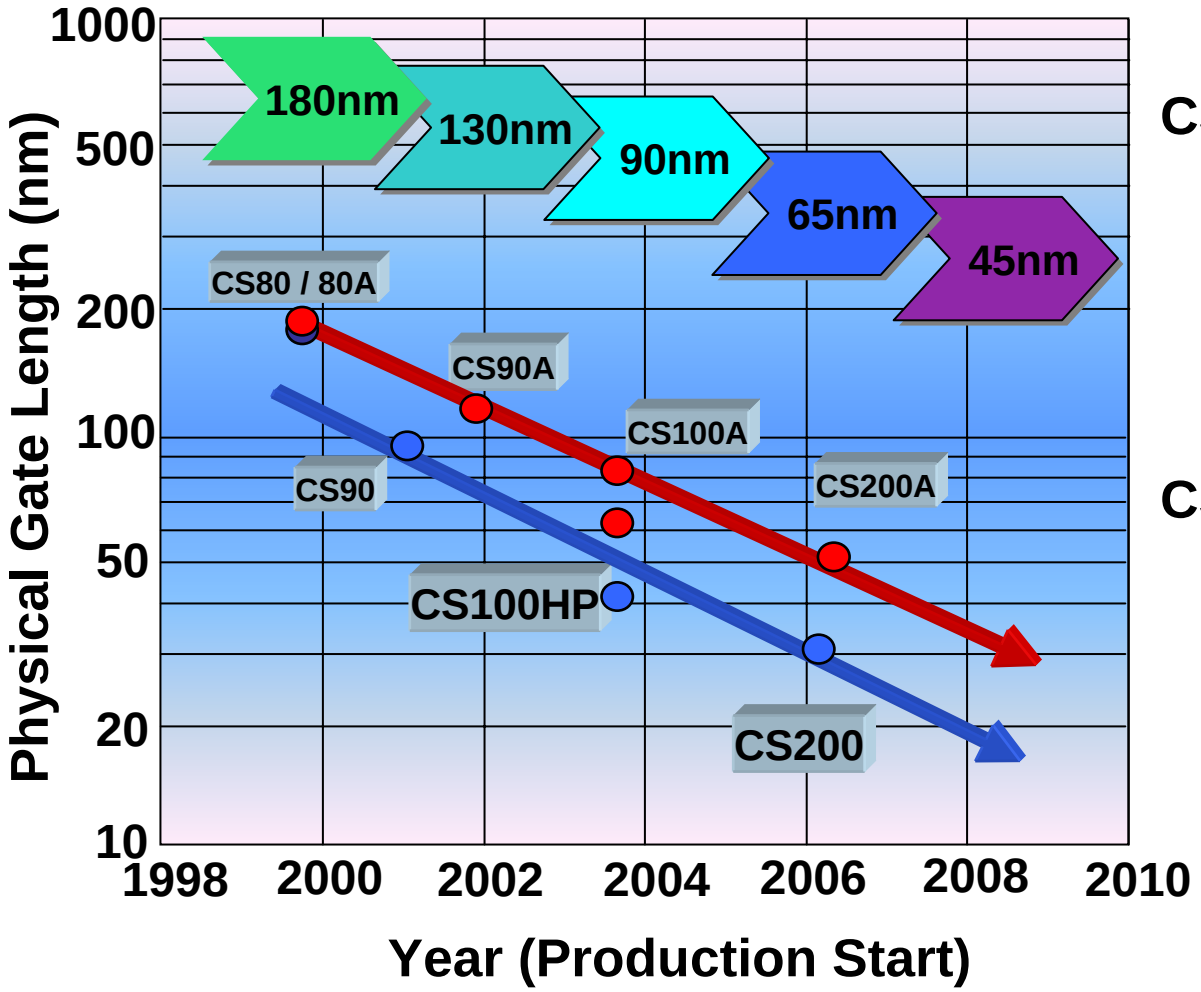
300mm Fab No.2

- Process
  - 65nm/90nm CMOS Logic
- Structural Features
  - Seismic-vibration control construction
  - Clean room area: 24,000 sq. meters
- Production Capacity
  - 10,000 wafers per month (FY07 projection)
  - Maximum capacity of 25,000 wafers per month
- Planned Start of Operation
  - April 2007

300mm Fab No.1

- Process
  - 90nm/65nm CMOS Logic
- Structural Features
  - Seismic-control construction
  - Clean room area: 12,000 sq. meters
- Production Capacity
  - 15,000 wafers per month (FY06)
- Start of Operation
  - April 2005

CMOS Technology Roadmap



CS100/CS100A (90nm)

- L actual=40-80nm
- SiOC (k:2.9) low-k
- Dual Damascene Cu

CS200/CS200A (65nm)

- L actual=30-50nm
- NCS (Nano-Clustering Silica)

Proven Track Record of 90nm Complex Designs and Products

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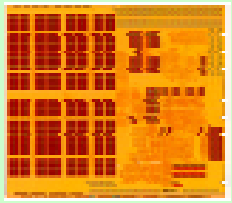
Processors for PRIMEPOWER

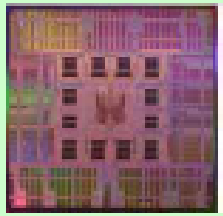
Achieves world-leading performance and reliability

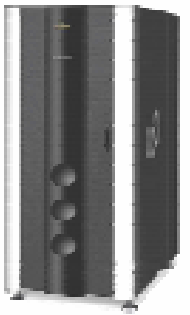


Chipset for PRIMEQUEST

Achieves mainframe-class reliability and scalability

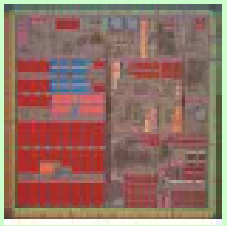
Helped reduce development time





Baseband chip for FOMA 3G mobile phones

LSI power consumption reduced 50%
(compared to existing tech)



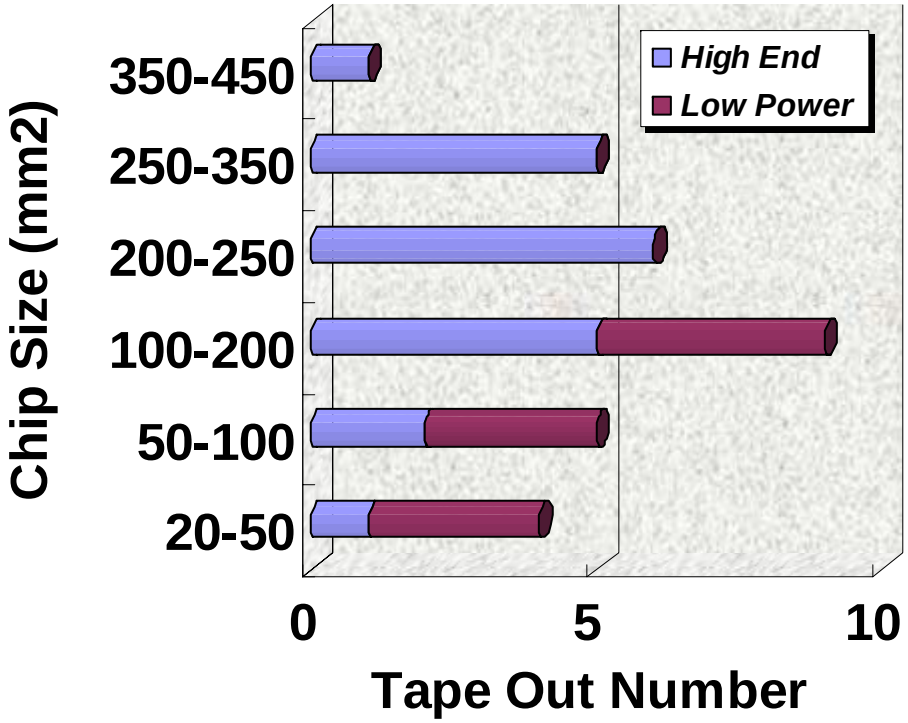
Proven Track Record of 90nm Complex Designs and Products – continued

High-performance Products

- PC CPU (Transmeta)
- Large-scale FPGA (Lattice)
- Others

Low-power Products

- Multimedia processor
- Digital AV products
- Others



65nm, CS200 / 200A Features

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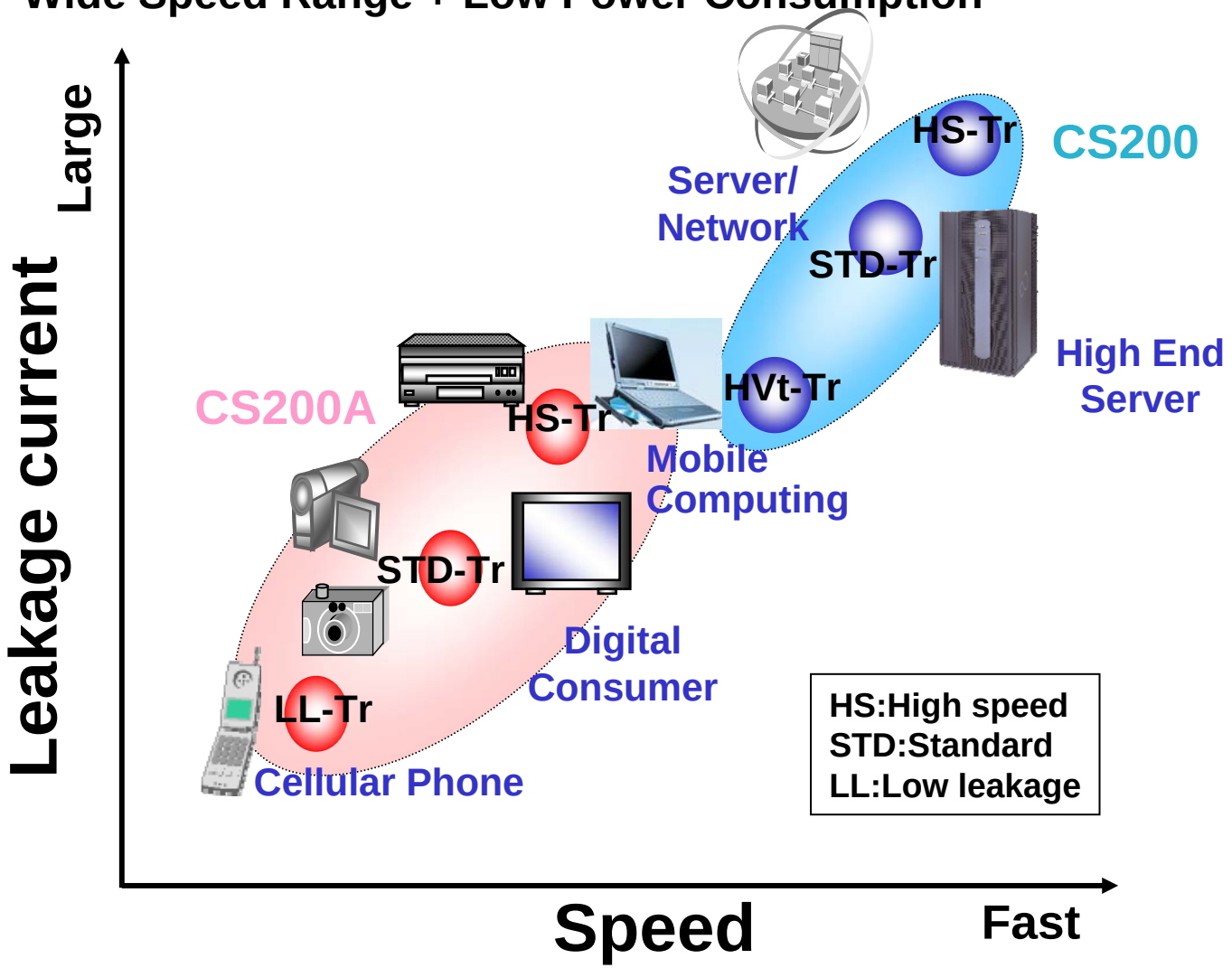
Features

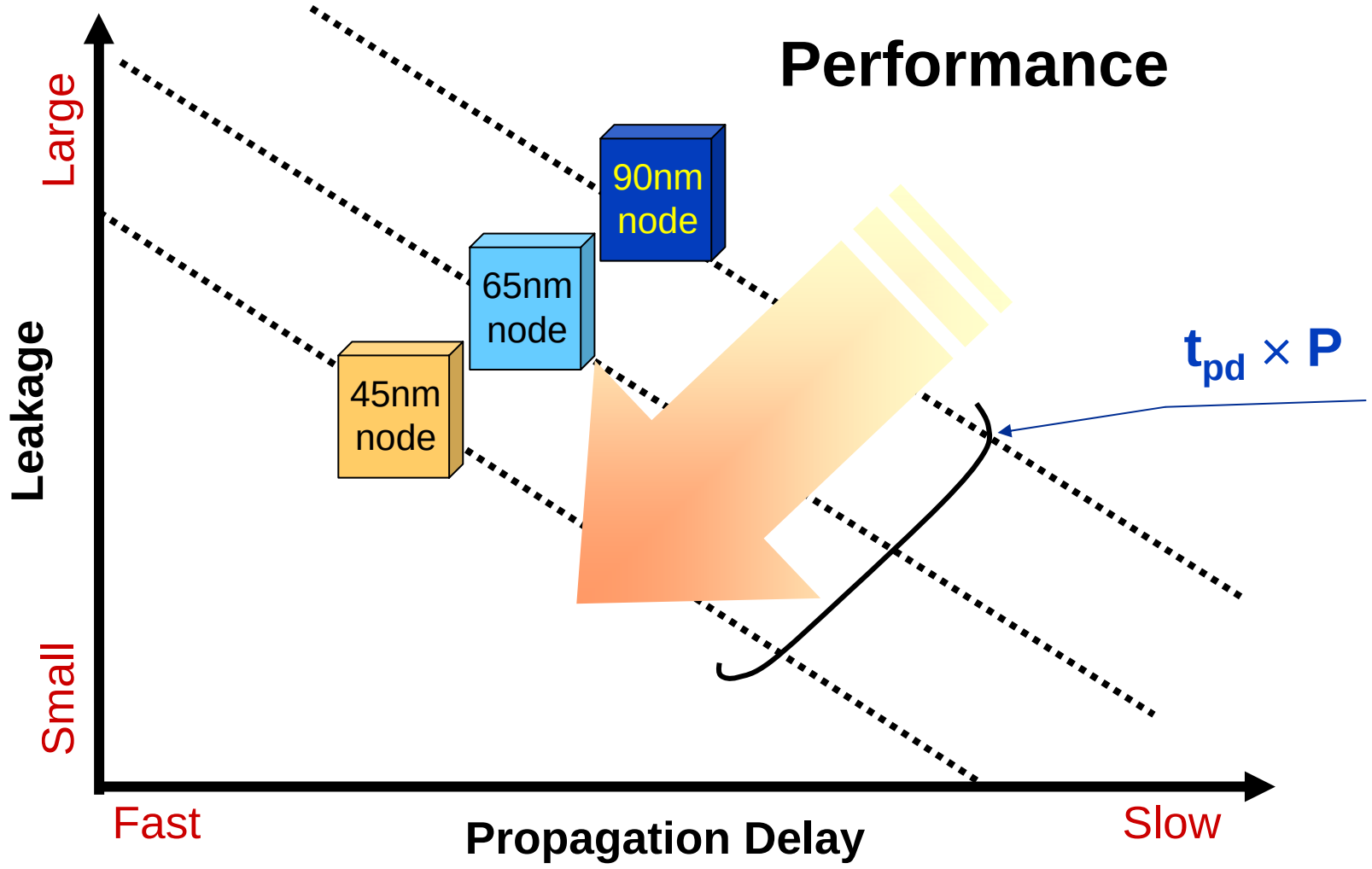
- **Ultra-high-speed performance (CS200)**
  - L_G = 30nm, on-current enhance
- **Compared to 90nm technology, CS200 offers:**
  - 1.3 times faster speed
  - 0.6 times lower power
  - 2 times higher density
- **3 variations of V_{th} on a chip (CS200A)**
- **(1.8V & 2.5V) or (1.8V & 3.3V) I/O combination available**
- **11-layer copper interconnects with robust, very low K ILD**

CS200 / 200A Transistor Variations

CS200: Ultra High Speed
CS200A: Wide Speed Range + Low Power Consumption



Leading-edge Transistors



Ultra-Thin Gate Insulator / Mobility Improvement

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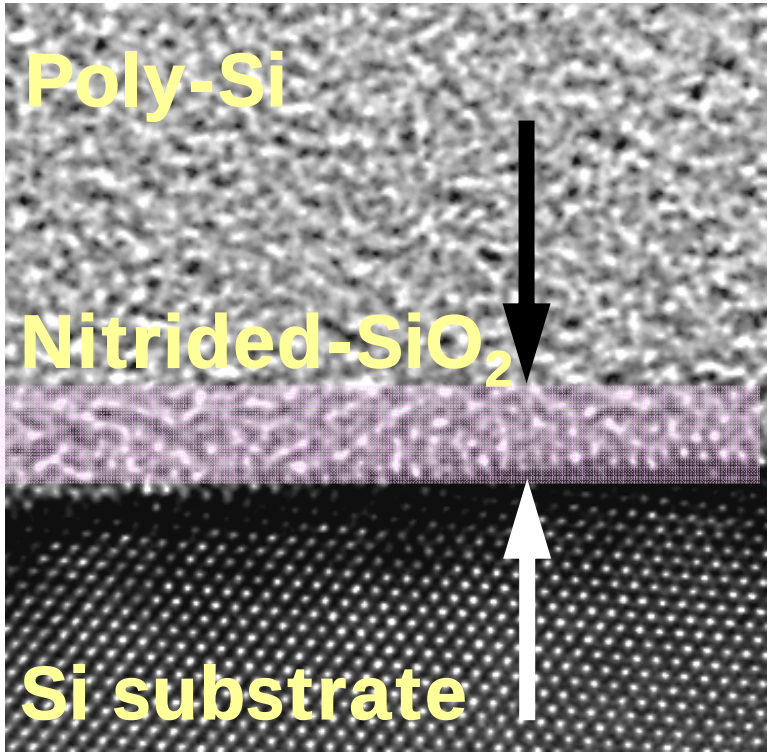
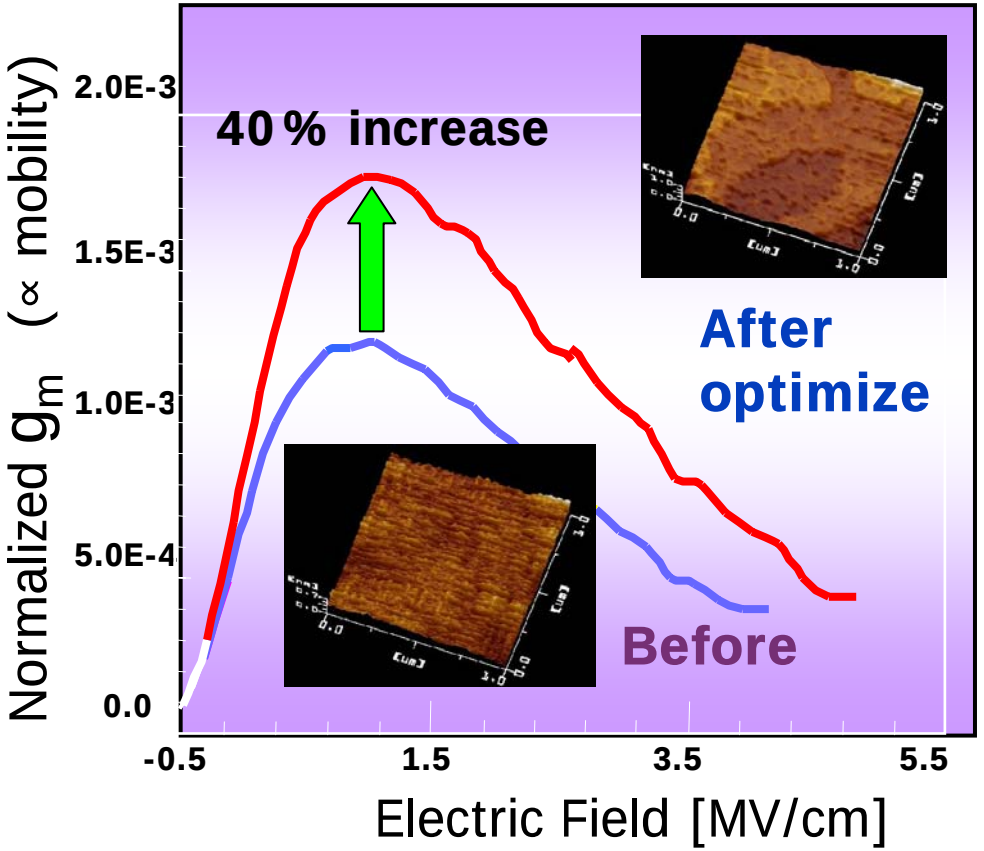
1nm-thick Gate Oxide



Surface Cleaning



Speed Performance Improvements

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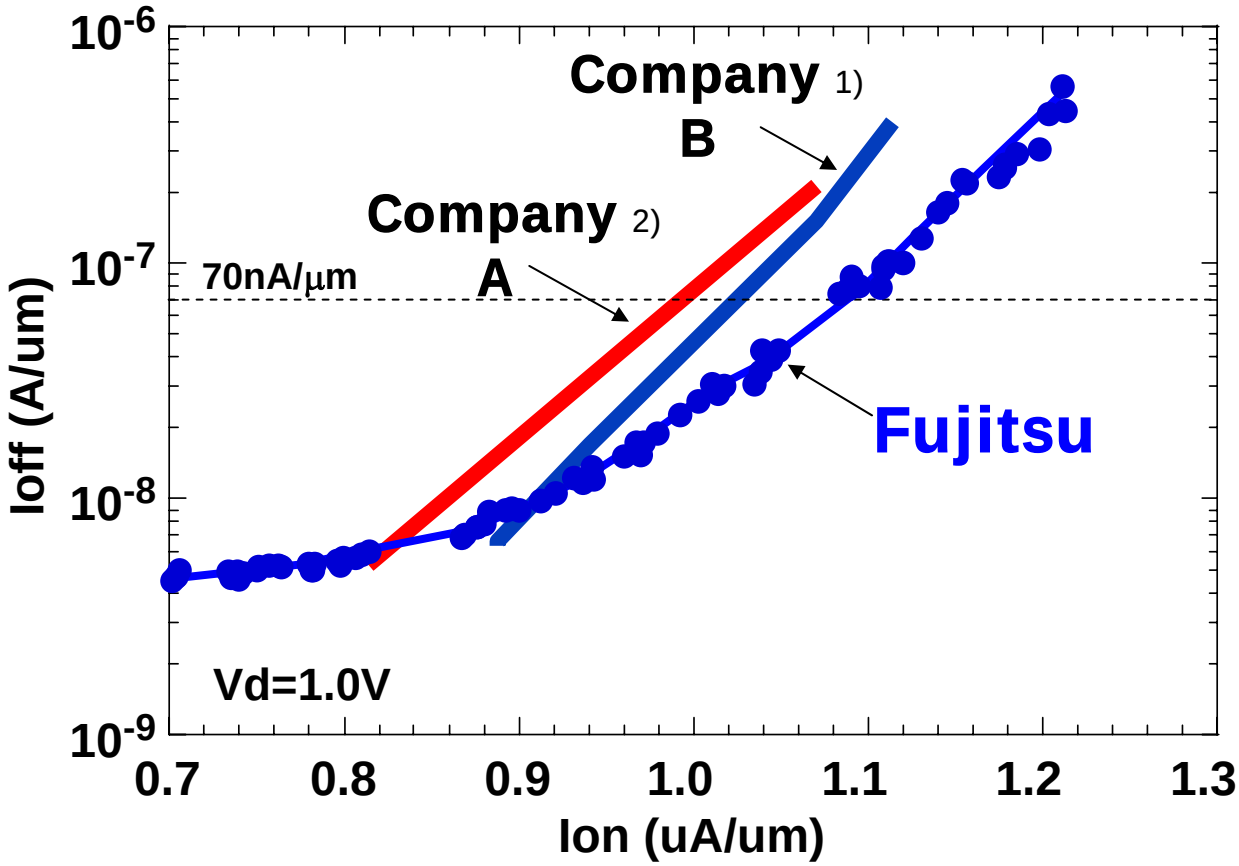
	65nm CS200 (ps/gate)	90nm CS100 (ps/gate)	Delay Improvement
Inverter	5.7	7.0	19%
2-input NAND	8.7	11.4	24%
2-input NAND + 200 grid interconnect load	23.1	30.8	25%

High-Performance Competitive Transistors

FUJITSU

Ion vs Ioff Characteristics of nMOSFETs



Ref.
1, 2) 2004 Symposium on VLSI Technology

Advanced Cu and Low-k

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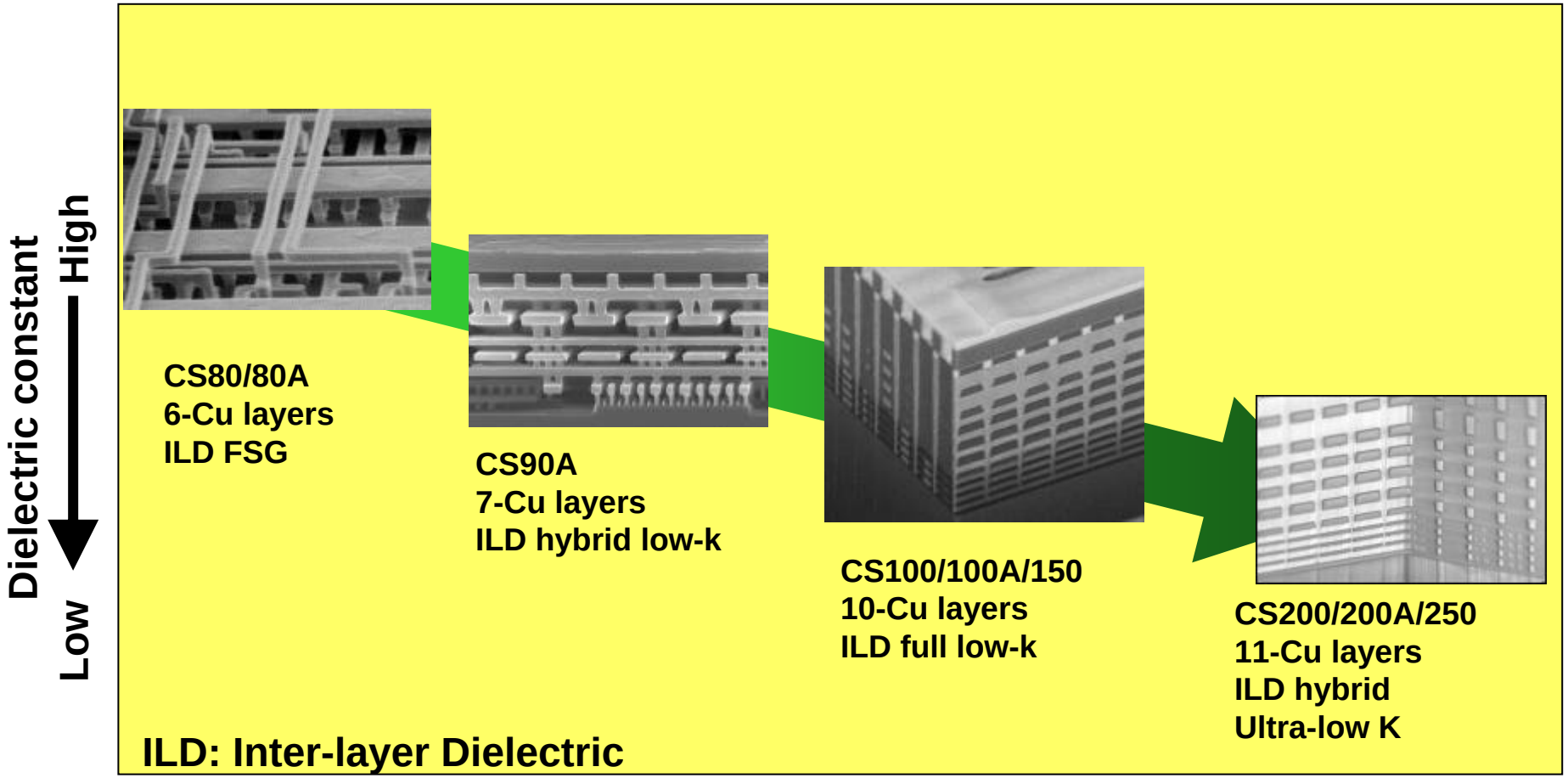
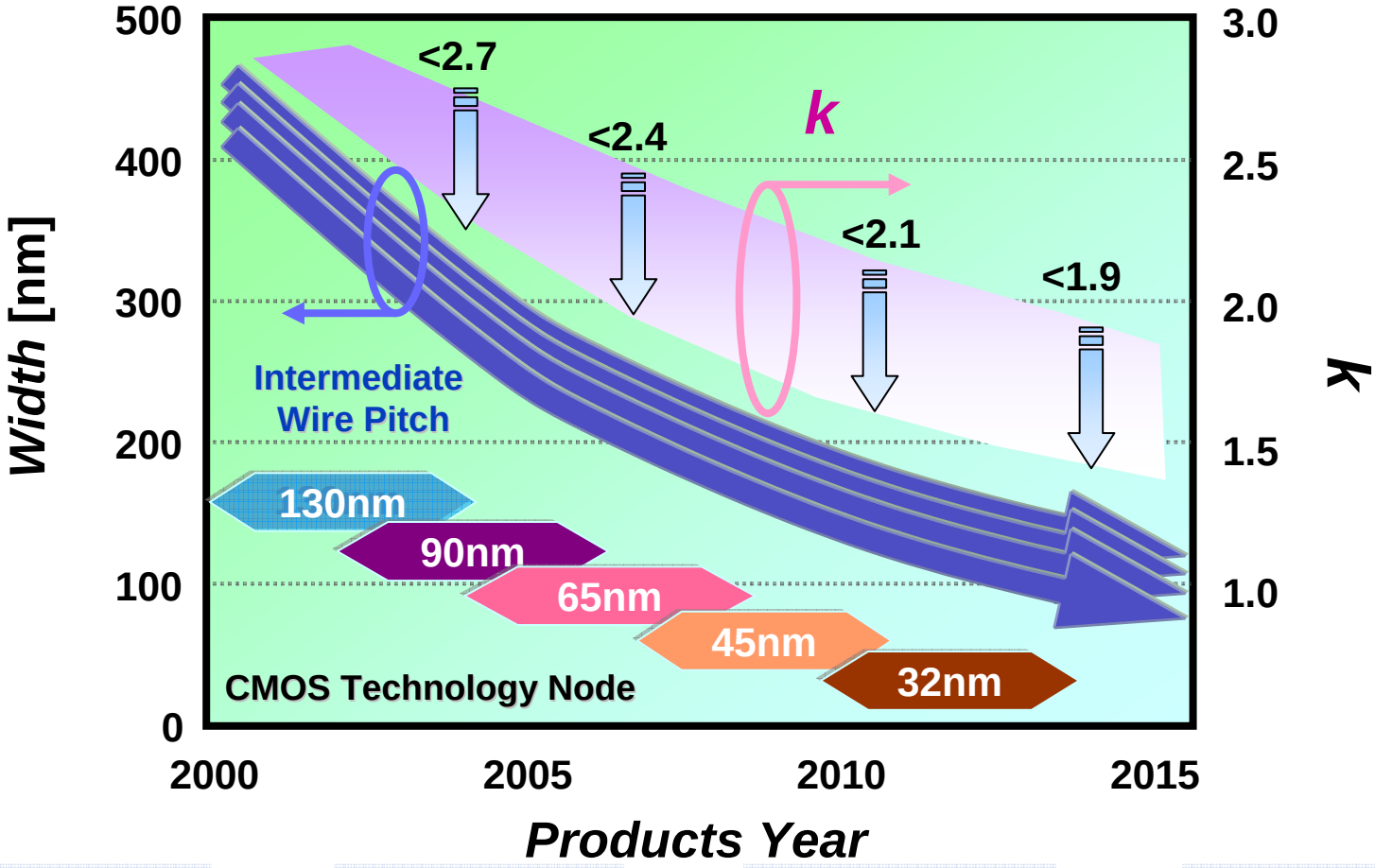
Four Generations of Experience



Fujitsu's Low-k Leads ITRS

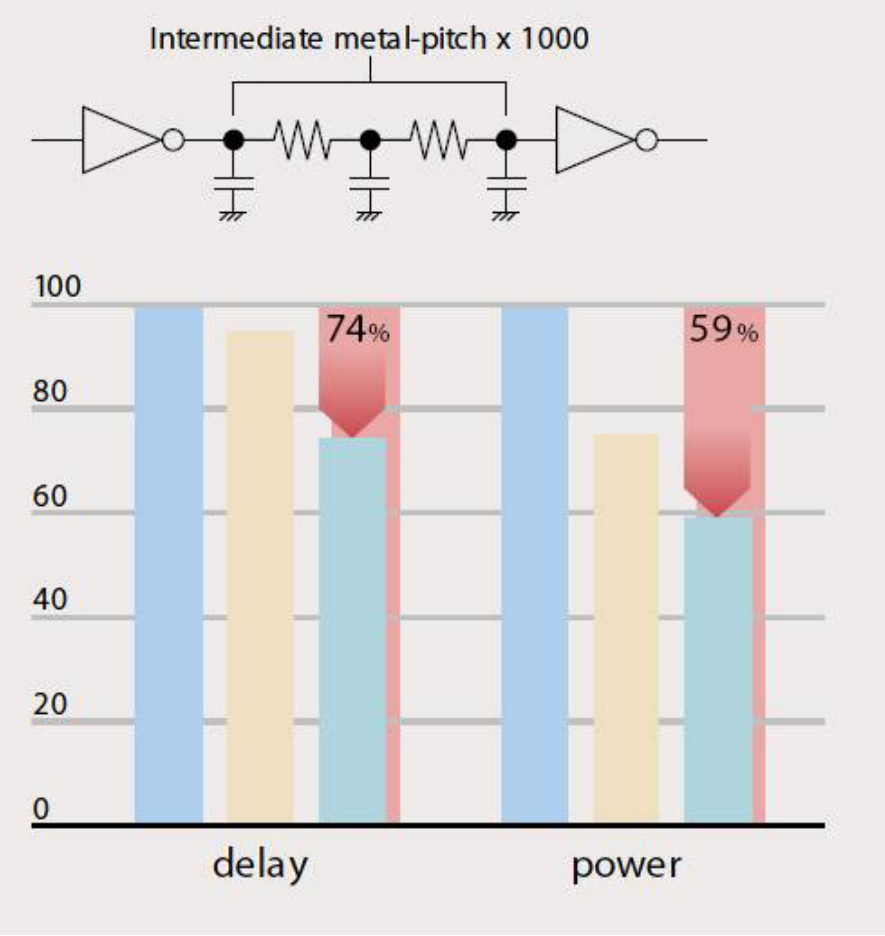


CS90	CS100	CS200	CS300
SiLK™/SiO 2	Full- SiOC	NCS/ SiOC	Full - NCS
K=2.7/4.1	K=2.9/2.9	K=2.25/2.9	K=2.25/2.25

Low-k Advantages of 65nm

FUJITSU

Ultra low-k impacts on speed and power dissipation



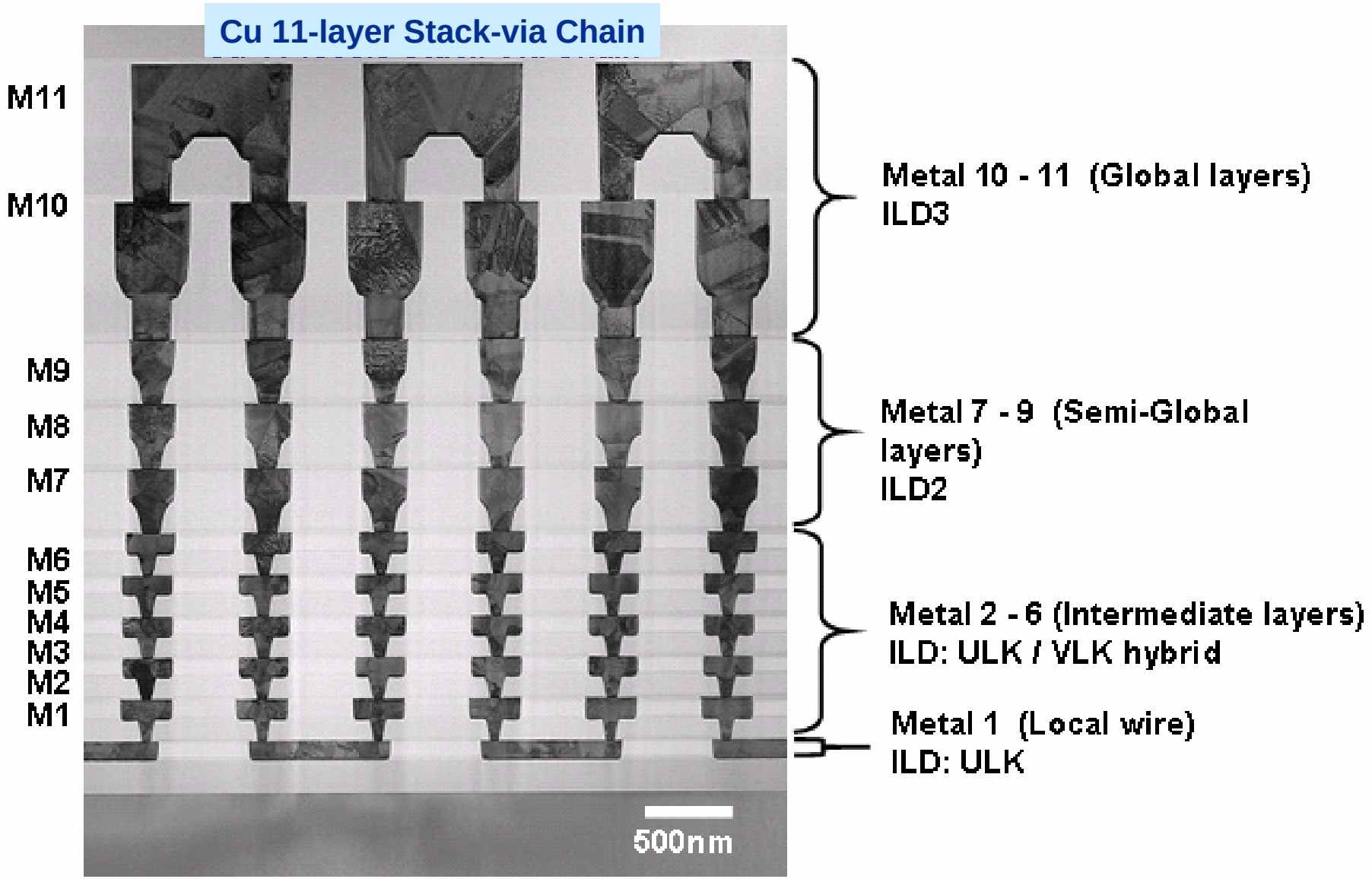
CS100A (90nm)
with SiOC/SiOC
Rsh: 90mΩ/sq., C: 56fF/1000 grid

CS200A (65nm)
with SiOC/SiOC
Rsh: 150mΩ/sq., C: 52fF/1000 grid

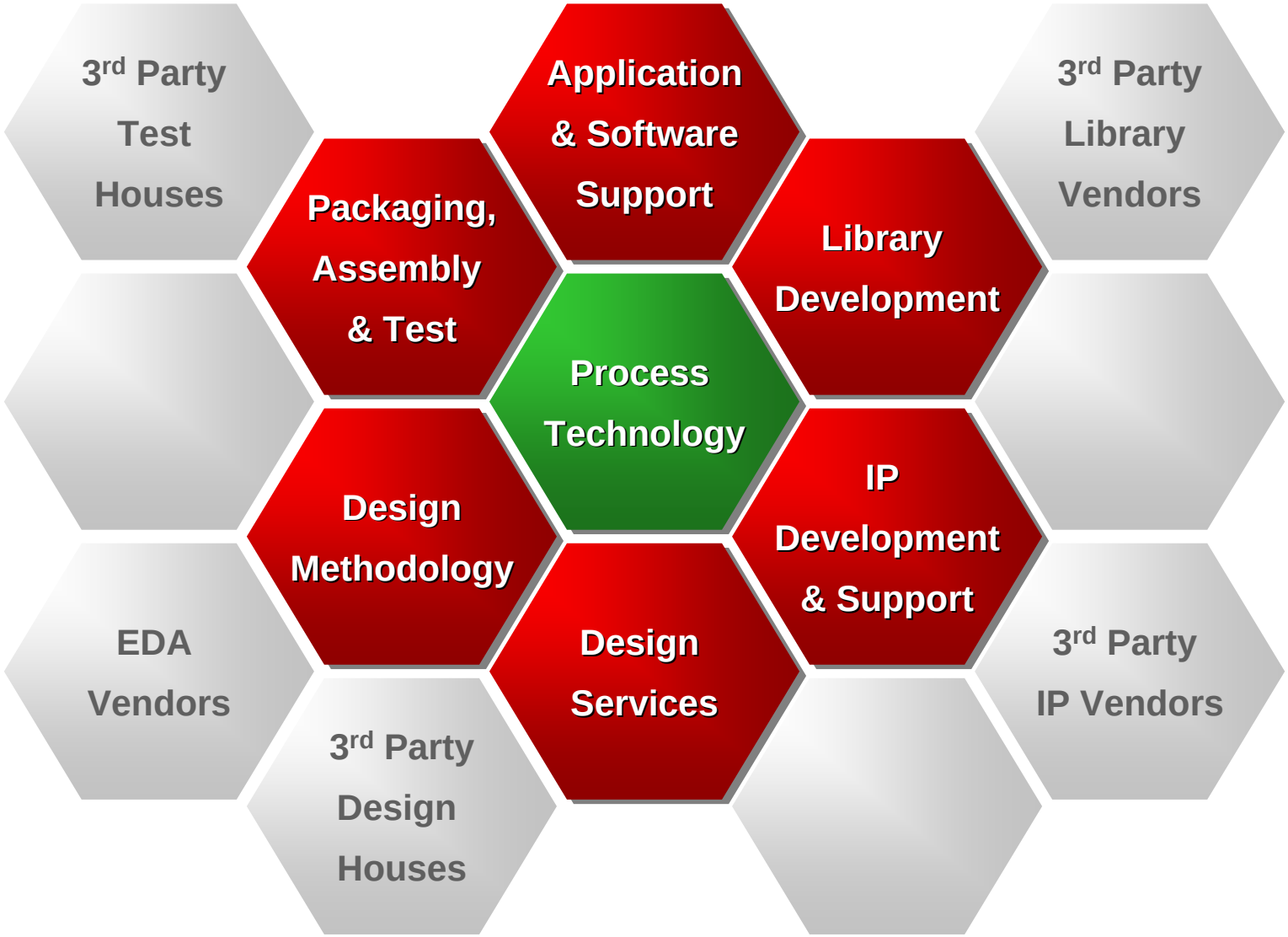
CS200A (65nm)
with NCS/SiOC
Rsh: 150mΩ/sq., C: 40fF/1000 grid

11-Layer Copper Interconnects

FUJITSU

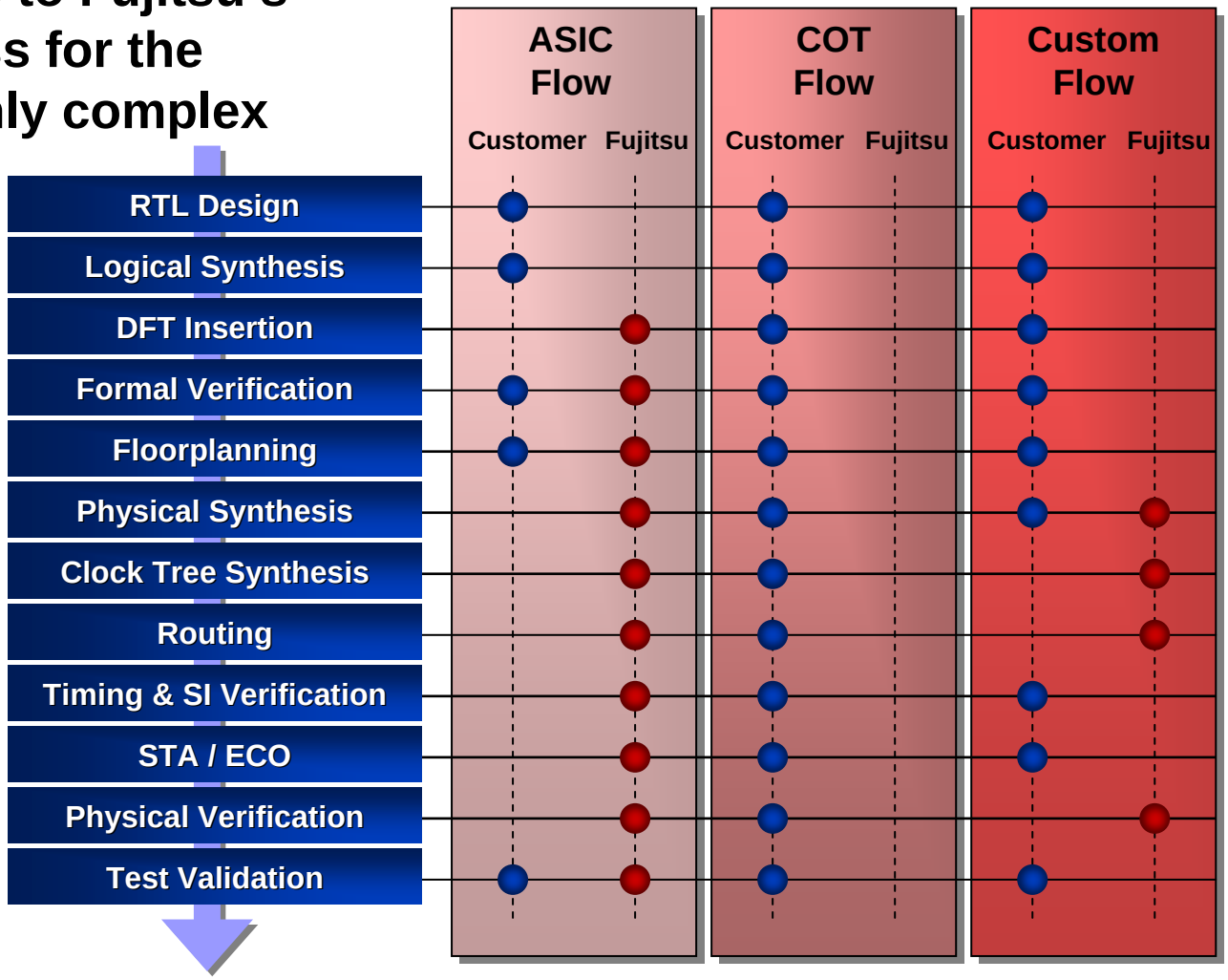


The Fujitsu Ecosystem



Fujitsu Technology Access

Flexible collaboration models provide easy access to Fujitsu's leading-edge process for the development of highly complex silicon products



Design Flow & Methodology

- Reference design flow - Fujitsu's leading-edge design methodology focuses on timing, signal and power integrity closure
- Support for both Cadence SOCEncounter™ and Synopsys Galaxy™ platforms
- In-house CAD software development augments leading third-party EDA solutions
- Ensures silicon correlation and a fast path to silicon success by combining Fujitsu's strengths in process, CAD tool and methodology development with design experience and expertise
- Production proven flows used on 100+ multi-million-gate designs at 180, 130 and 90nm
- Constantly updated and improved to address all issues at each process node

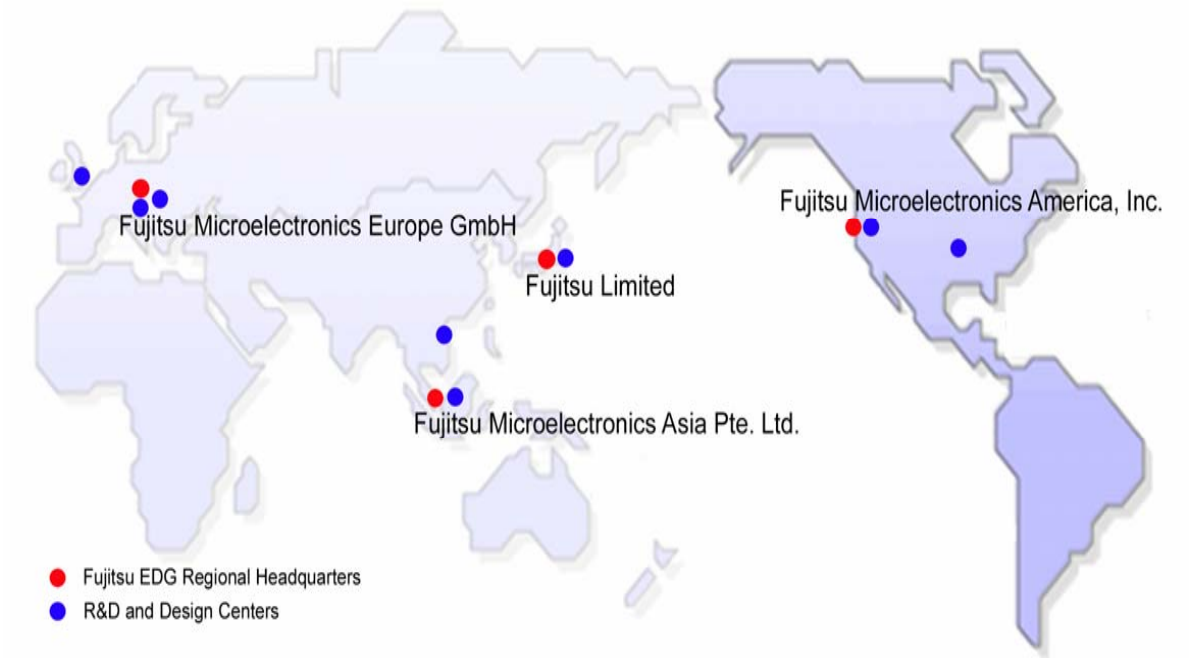
Fujitsu Design Services

- Library and tool support
- Methodology development and support
- High-speed I/O design and expertise
- Vertical expertise and IP cores
- RTL design
- Synthesis and physical synthesis
- Design partitioning and floorplanning
- Static timing analysis
- Test insertion and ATPG generation
- Place and route
- Timing and SI closure
- Formal verification
- Physical verification
- Test and product engineering

Fujitsu Worldwide Design Centers

Global Presence

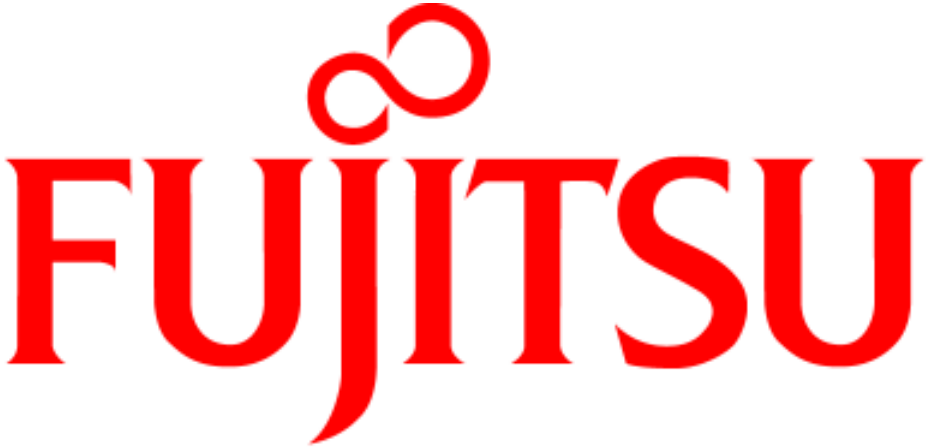
- Local design centers around the world provide design services for all phases of the development process



- Skilled engineering teams experienced in development of large complex designs at 130nm and below
- 100+ multi-million gate designs taped out

Summary

- **Fujitsu Objective**
  - Helping customers accelerate their innovation, differentiate their products and enhance their competitive advantage, therefore helping them succeed
- **Leading-edge technologies**
  - Strength in process technologies
    - 90nm, 65nm and beyond
  - Partnerships and customer collaborations
    - Flexible customer engagements and close collaborations
    - Early customer engagements
    - Tailored support and services to meet customer needs
  - System-level LSI solutions
    - ASIC and ASSP/SoC, including10GbE switch chip and WiMAX SoC
  - Full design and development environments and support



THE POSSIBILITIES ARE INFINITE