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IC Package



Providing New Technologies for the Near Future

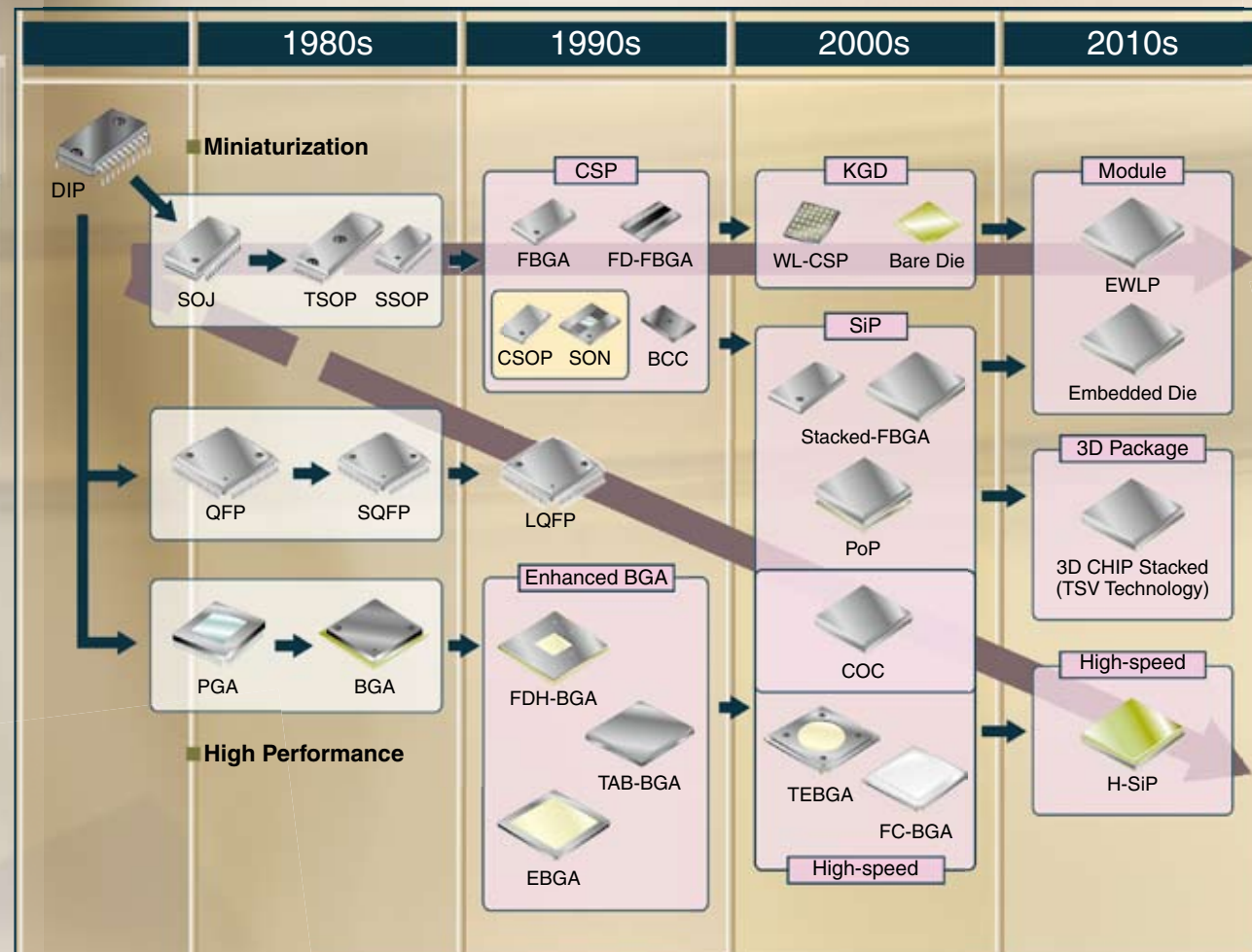
Trends in Package Development

Electronic products have been in growing demand, such as personal computers, mobile phones and PDAs, and its technology innovation has constantly come along. The IC technology is supporting customers to meet market demands today and in the future.

Packaging solutions enable to reduce size and space requirements as a key technology. The packages such as CSP (Chip Size Package or Chip Scale Package) and BGA (Ball Grid Array) have supported high-density wiring technology and widely used in the market.

Miniaturization forced the use of new approaches in die packaging in order to achieve the smallest possible solutions. Leading the van of CSP, Fujitsu Semiconductor has launched the mass-production packages of SON which was impressed as the world's smallest level.

Fujitsu Semiconductor has a mass-production lineup of super compact packages such as FBGA (Fine Pitch BGA) and WL-CSP (Wafer Level CSP) and beyond. The high pin count packages, PBGA (Plastic BGA) and TEBGA (Thermal Enhanced BGA) have been mass-produced in order to fulfill the size and weight limitations, for example portable equipment.

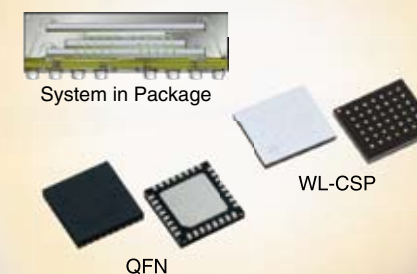


Package Solutions

Fujitsu Semiconductor offers a wide range of packages to optimize applications in a way most suited for customers' requirements.

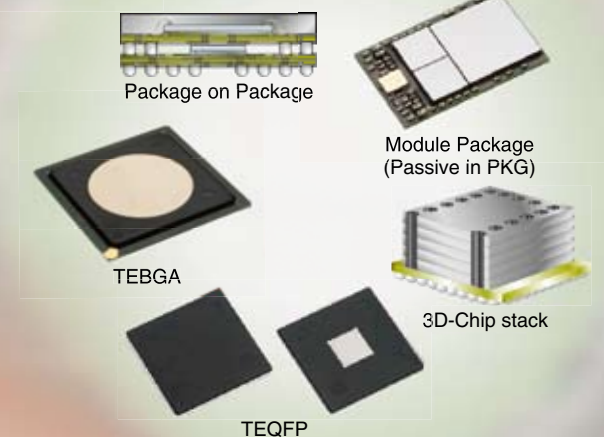
Mobile

- Super compact, light, thin -

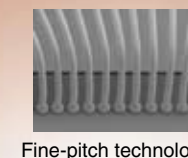


Digital AV

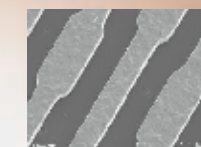
- High density, high function, high performance -



Ultra thin technology



Fine-pitch technology



Fine wiring

Key technologies

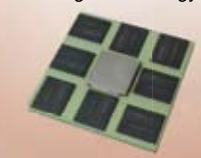
Cutting-edge technologies
Lower cost by integrated design
Environmental considerations

Key technologies

Bump technology



Design technology



CoC technology



High-end

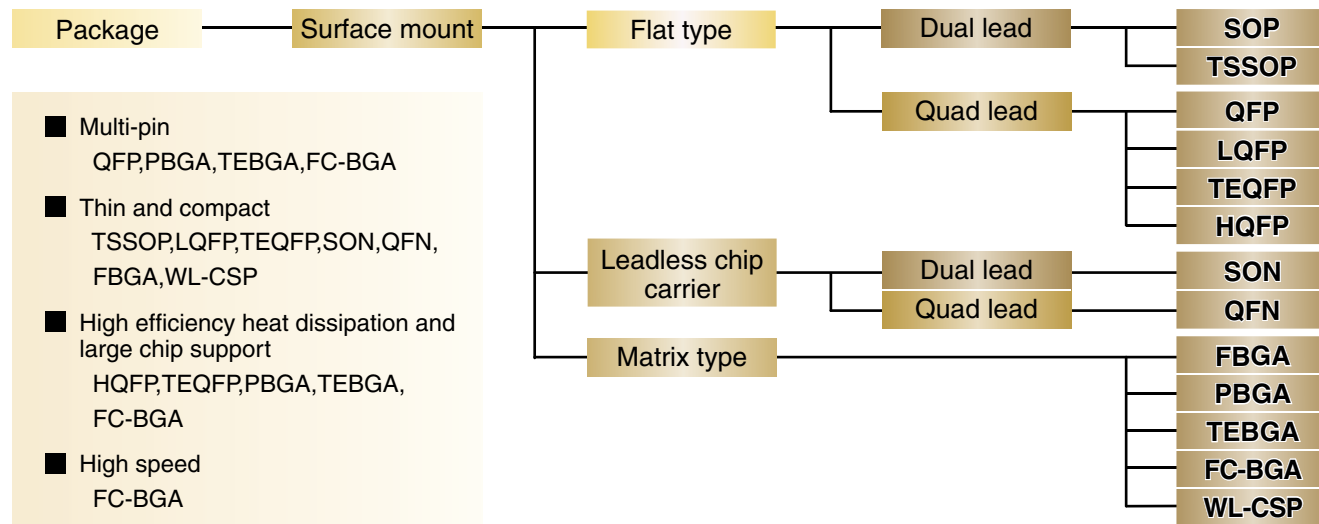
- Ultra high speed, high efficiency heat dissipation -



Automotive

- High reliability, high heat resistance -

Package Line-up



SOP (Small Outline L-Leaded Package) TSSOP (Thin Shrink Small Outline Package)

Features

- Superior cost performance with a mature technology.
- High reliability in mounting the package on printed circuit boards.
- Thin and compact.

SOP and TSSOP Package external view

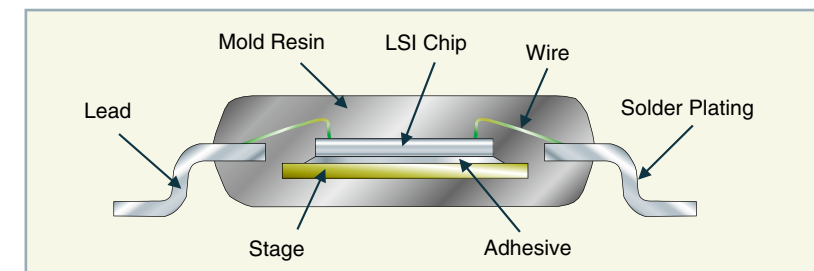


SOP



TSSOP

SOP and TSSOP Package cross section



SOP and TSSOP Package line-up

Package type	Package size (mm)		Mounting height (mm)	Pin count		
	X	Y		Pin pitch 1.27mm	Pin pitch 0.65mm	Pin pitch 0.50mm
SOP	5.3	5.24	2.10 Max.	8	—	—
	7.5	12.7	2.65 Max.	20	—	—
TSSOP	4.4	3.1	1.20 Max.	—	8	—
	4.4	4.96		—	14/16	—
	4.4	6.5		—	20	24
	4.4	7.8		—	24	30
	4.4	9.7		—	28	—

Please contact us for information on other packages.

Package Overview

	Package type	Package structure	Pin count	I/O frequency (GHz)	Heat resistance θ_{ja} (°C/W) (0m/s)	Application
High-end	FC-CBGA		450~2116	~5	7~	Routers, Servers, Workstations, Backbone transmission devices
	FC-PBGA (AISIC-LID)		450~2116	~2.5	7~	
	FC-PBGA (Cu-LID)		450~1156	~2.5	9~	Routers, Personal computers, Graphics, Digital TVs, Set top boxes, Printers
	TEBGA		256~1156	~1.6	13~	
Consumer appliances	PBGA		256~1156	~1.6	15~	Personal computers, Mobile phones, Digital video cameras, Digital still cameras, PDAs
	FBGA		66~906	~1	17~60	
	SON QFN		6~68	~1.5	20~40	Mobile phones, Digital video cameras, Digital still cameras, PDAs
	WL-CSP		42~309	~2.5	25~60	
	QFP LQFP		48~304	~2.5	15~100	Personal computers, Digital TV, Set top boxes, Printers
	TEQFP		48~256	~2.5	15~35	

QFP

LQFP

TEQFP

HQFP

(Quad Flat Package)

(Low Profile Quad Flat Package)

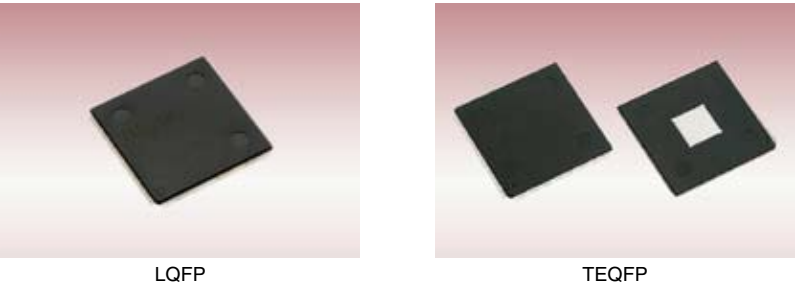
(Thermally Enhanced QFP)

(QFP with Heat Sink)

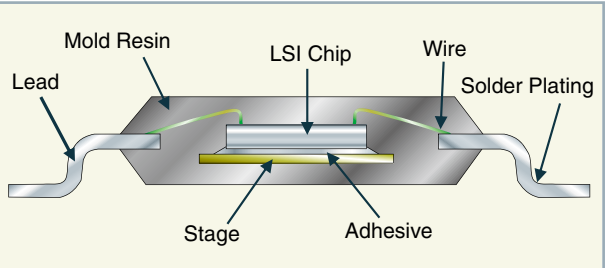
- Features

 - Equipped with outer leads at the four corners of the package.
 - Superior cost performance with a mature technology.
 - High reliability in mounting the package on printed circuit boards.
 - TEQFP and HQFP can be mounted with a chip with high heat emission because of their high efficiency in heat dissipation.

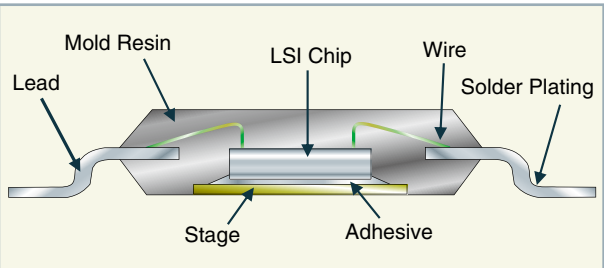
QFP Package external view



QFP and LQFP Package cross section



TEQFP Package cross section



QFP Packages line-up

Package type	Package size (mm)		Mounting height (mm)	Pin count		
	X	Y		Pin pitch 0.65mm	Pin pitch 0.50mm	Pin pitch 0.40mm
QFP	14.0	20.0	3.35 Max.	100	—	—
	28.0	28.0	3.95 Max.	—	208	—
	32.0	32.0	4.03 Max.	—	240	—
LQFP TEQFP	7.0	7.0	1.70 Max.	—	48	64
	10.0	10.0		52	64	—
	12.0	12.0		64	80	—
	14.0	14.0		—	100	—
	16.0	16.0		—	120	144
	20.0	20.0		—	144	—
	24.0	24.0		—	176	216
HQFP	28.0	28.0	—	—	208	256
	28.0	28.0	3.95 Max.	—	208	—
	32.0	32.0	4.03 Max.	—	—	256
	40.0	40.0	4.10 Max.	—	240	296
				—	304	—

Please contact us for information on other packages.

SON

QFN

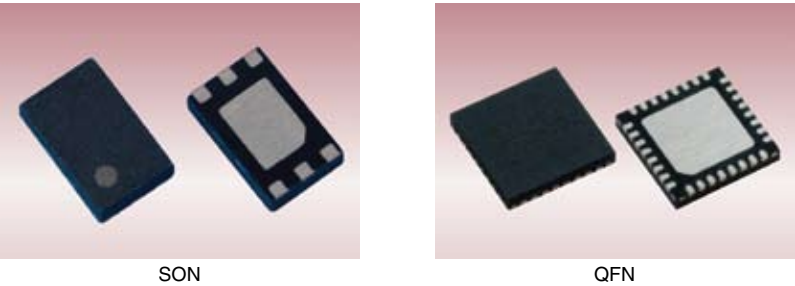
(Small Outline Non-leaded Package)

(Quad Flat Non-Leaded Package)

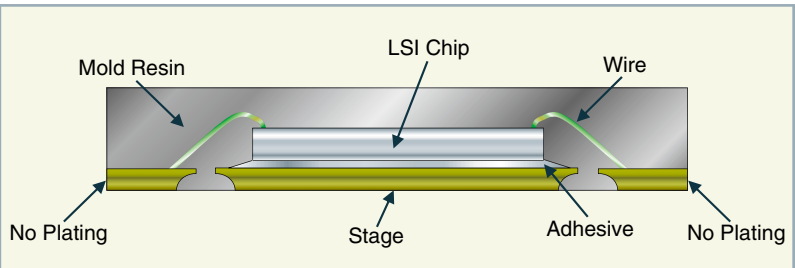
- Features

 - Thin and compact.
 - Better cost performance compared to BGA.

Package external view



Package cross section



SON Package line-up

Package size (mm)		Mounting height (mm)	Pin count		
X	Y		Pin pitch 0.65mm	Pin pitch 0.50mm	Pin pitch 0.40mm
1.80	2.85	0.80 Max.	6	—	—
2.0	2.0		—	8	—
3.0	3.0		—	10	—

QFN Package line-up

Package size (mm)		Mounting height (mm)	Pin count		
X	Y		Pin pitch 0.65mm	Pin pitch 0.50mm	Pin pitch 0.40mm
2.5	3.5	0.80 Max.	—	—	24
3.0	3.0		—	16	20
4.0	4.0		16	16/20/24	28
5.0	5.0		—	28/32	40
6.0	6.0		—	40	48
7.0	7.0		—	48	56
8.0	8.0		—	—	68
9.0	9.0		—	64	—

Please contact us for information on other packages.

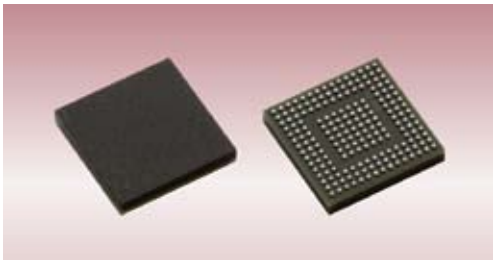
FBGA (Fine pitch Ball Grid Array)

Features

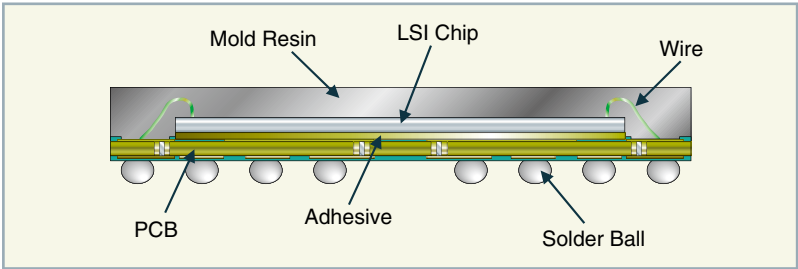
Low profile and multi-pin support, suitable for portable devices such as mobile phones and DSCs.

- Fine pitch (pin pitch from 0.4mm) and thin.
- Superior electrical characteristics and reliability.
- Plentiful line-up and customization support.

FBGA Package external view



FBGA Package cross section



FBGA Package line-up

Pin pitch : 0.50mm (Less than 500pin)

Package code	Pin count		Package size (mm)		Pin arrangement
	Total	number of TBs* included	X	Y	
BGA-66P-M01	66	9	5.0	5.0	2 rows
BGA-82P-M01	82	9	6.0	6.0	2 rows
BGA-96P-M04	96	0	6.0	6.0	3 rows
BGA-100P-M03	100	0	7.0	7.0	2 + (1) + 1 rows
BGA-112P-M05	112	0	7.0	7.0	3 rows (With nonexistent pins)
BGA-130P-M02	130	9	7.0	7.0	3 rows
BGA-144P-M09	144	0	7.0	7.0	4 rows
BGA-168P-M03	168	25	9.0	9.0	3 rows (With nonexistent pins)
BGA-208P-M01	208	0	9.0	9.0	4 rows
BGA-232P-M01	232	0	12.0	12.0	2 + (1) + 2 rows
BGA-240P-M02	289	49	10.0	10.0	4 rows
BGA-240P-M03	240	0	10.0	10.0	4 rows
BGA-289P-M01	289	25	10.0	10.0	3 + (1) + 2 rows
BGA-304P-M05	304	0	13.0	13.0	2 + (1) + 2 rows
BGA-304P-M07	304	0	12.0	12.0	4 rows
BGA-337P-M02	428	81	13.0	13.0	4 rows
BGA-345P-Mxx	345	25	12.0	12.0	2 + (1) + 2 + (1) + 1 rows
BGA-385P-M01	434	49	13.0	13.0	3 + (1) + 2 rows
BGA-385P-M02	385	81	13.0	13.0	2 + (2) + 2 rows
BGA-385P-M03	385	81	12.0	12.0	4 rows
BGA-400P-M04	481	81	15.0	15.0	4 rows

*TB : Thermal Ball

FBGA Package line-up

Pin pitch : 0.50mm (500pin or more)

Package code	Pin count		Package size (mm)		Pin arrangement
	Total	number of TBs* included	X	Y	
BGA-506P-Mxx	506	81	14.0	14.0	3 + (1) + 2 rows
BGA-562P-M03	562	81	14.0	14.0	3 + (1) + 3 rows
BGA-586P-Mxx	586	121	15.0	15.0	3 + (1) + 2 rows
BGA-586P-M04	586	49	15.0	15.0	4 + (1) + 2 rows
BGA-610P-M01	610	121	16.0	16.0	3 + (2) + 2 rows
BGA-650P-M03	650	169	15.0	15.0	5 rows
BGA-753P-Mxx	753	169	18.0	18.0	3 + (1) + 2 rows
BGA-770P-M01	770	121	16.0	16.0	4 + (1) + 3 rows
BGA-842P-Mxx	842	169	18.0	18.0	3 + (1) + 2 rows
BGA-906P-Mxx	906	169	18.0	18.0	3 + (1) + 2 + (1) + 2 rows

*TB : Thermal Ball

Pin pitch : 0.65mm

Package code	Pin count		Package size (mm)		Pin arrangement
	Total	number of TBs* included	X	Y	
BGA-176P-M05	176	0	11.0	11.0	4 rows
BGA-204P-M01	204	0	11.0	11.0	3 + (1) + 2 rows
BGA-240P-M07	240	0	13.0	13.0	4 rows
BGA-252P-M01	252	0	13.0	13.0	5 rows (With nonexistent pins)
BGA-280P-M03	280	0	13.0	13.0	5 rows
BGA-360P-M05	441	81	16.0	16.0	5 rows
BGA-385P-M04	385	25	16.0	16.0	5 rows

*TB : Thermal Ball

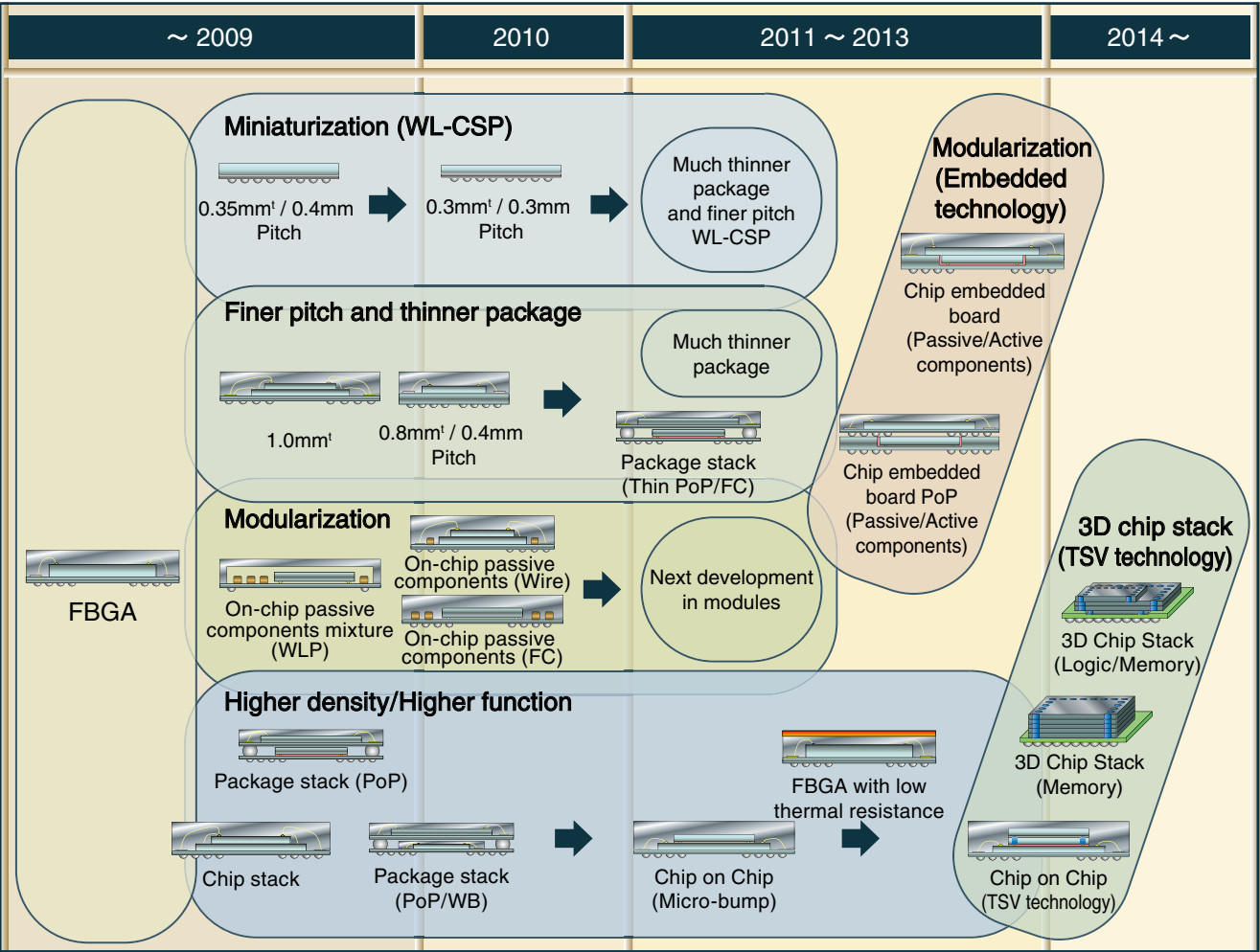
Pin pitch : 0.80mm

Package code	Pin count		Package size (mm)		Pin arrangement
	Total	number of TBs* included	X	Y	
BGA-112P-M04	112	0	10.0	10.0	4 rows
BGA-144P-M06	144	0	12.0	12.0	4 rows
BGA-144P-M07	144	0	12.0	12.0	4 rows (With nonexistent pins)
BGA-176P-M04	176	0	12.0	12.0	5 rows (With nonexistent pins)
BGA-188P-M01	188	0	15.0	15.0	4 rows (With nonexistent pins)
BGA-192P-M06	192	—	12.0	12.0	Full Matrix (With nonexistent pins)
BGA-224P-M06	224	0	16.0	16.0	4 rows
BGA-224P-M08	260	36	16.0	16.0	4 rows
BGA-224P-M09	288	64	16.0	16.0	4 rows
BGA-240P-M06	240	0	15.0	15.0	5 rows
BGA-256P-M17	256	49	18.0	18.0	2 + (1) + 2 rows
BGA-272P-M06	321	49	18.0	18.0	4 rows
BGA-272P-M08	272	0	18.0	18.0	4 rows
BGA-320P-M05	369	49	18.0	18.0	5 rows
BGA-441P-M01	441	—	18.0	18.0	Full Matrix

Please contact us for information on other pin arrangements.

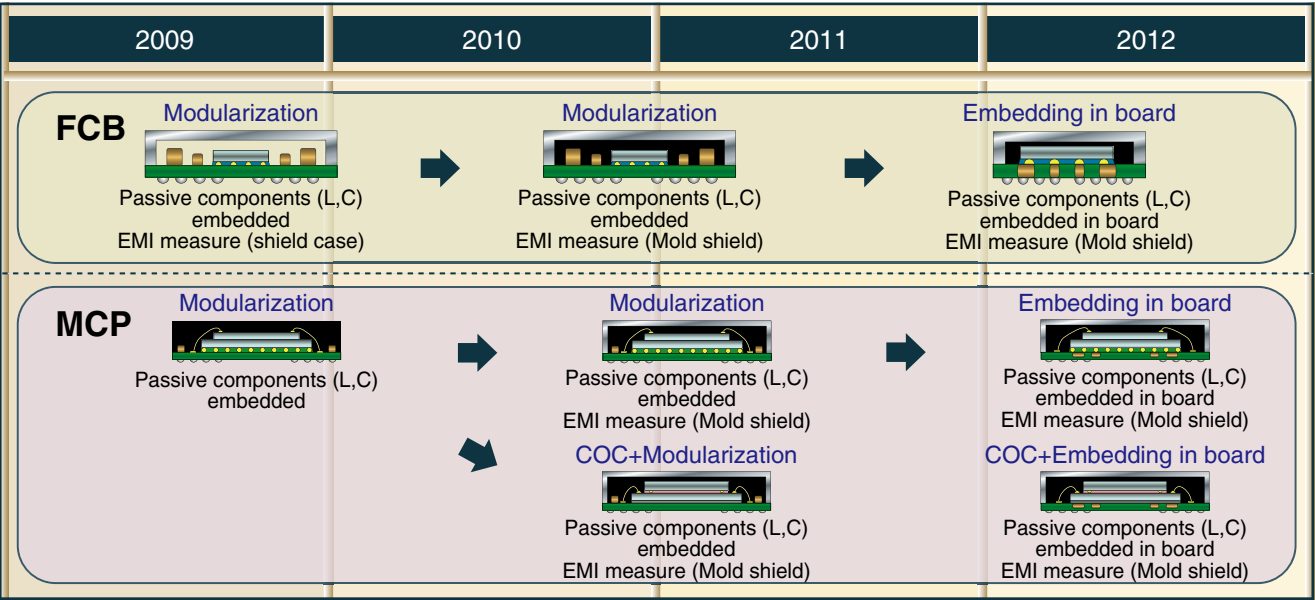
*TB : Thermal Ball

CSP Road map



Fujitsu Semiconductor will provide the most suitable SiP to the customer's requirements with our extensive implementation technologies. Please contact us for any requests.

Module package road map



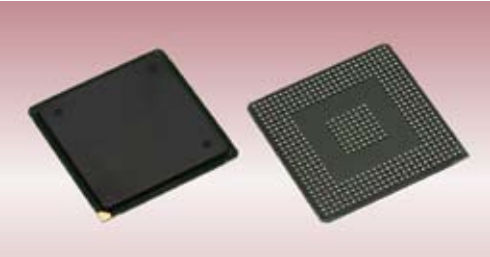
PBGA

(Plastic Ball Grid Array)

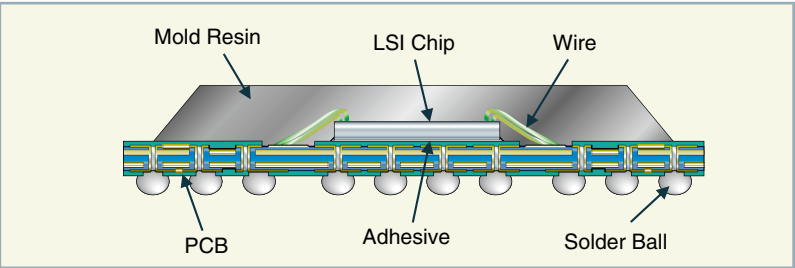
Features

- Sealed with plastic resin to achieve high cost performance.
- Superior support for multi-pin.
- Package sizes at 27mmSQ, 31mmSQ, and 35mmSQ are available.

PBGA Package external view



PBGA Package cross section



PBGA Package line-up

Package code	Pin count		Package size (mm)		Pin arrangement	Pin pitch (mm)
	Total	number of TBs* included	X	Y		
BGA-256P-M24	256	—	17.0	17.0	Full Matrix	1.00
BGA-256P-M27	256	0	27.0	27.0	4 rows	1.27
BGA-320P-M06	320	64	27.0	27.0	4 rows	1.27
BGA-321P-M02	321	—	19.0	19.0	Full Matrix (With nonexistent pins)	1.00
BGA-353P-M02	353	49	31.0	31.0	4 rows	1.27
BGA-416P-M05	416	64	27.0	27.0	4 rows	1.00
BGA-416P-M09	416	64	35.0	35.0	4 rows	1.27
BGA-480P-M14	480	64	27.0	27.0	5 rows	1.00
BGA-484P-M07	484	64	27.0	27.0	5 rows	1.00
BGA-484P-M11	484	64	35.0	35.0	5 rows	1.27
BGA-493P-M01	493	64	27.0	27.0	3 + (2) + 3 rows (With nonexistent pins)	1.00
BGA-496P-M02	496	144	27.0	27.0	4 rows	1.00
BGA-544P-M04	544	64	27.0	27.0	6 rows	1.00
BGA-564P-M01	564	64	31.0	31.0	5 rows	1.00
BGA-676P-M06	676	—	27.0	27.0	Full Matrix	1.00
BGA-676P-M14	676	100	35.0	35.0	5 rows	1.00
BGA-868P-M03	868	196	35.0	35.0	6 rows	1.00
BGA-900P-M14	900	—	31.0	31.0	Full Matrix	1.00

Please contact us for information on other pin arrangements.

*TB : Thermal Ball

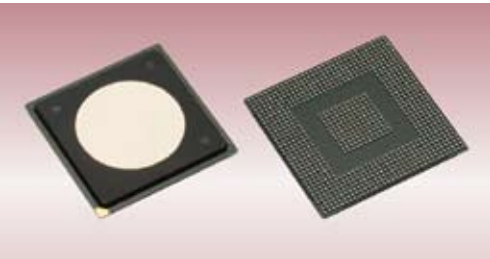
TEBGA

(Thermally Enhanced Ball Grid Array)

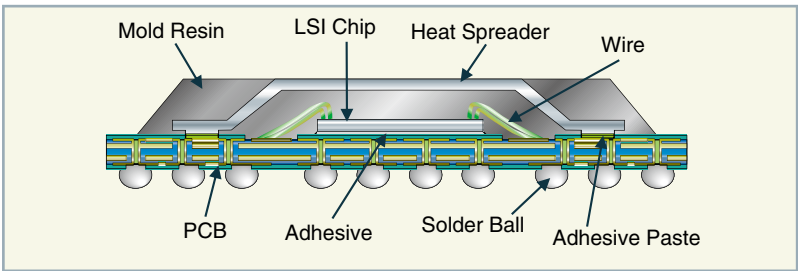
Features

- Superior thermal characteristics.
- Superior support for multi-pin.
- Package sizes at 27mmSQ and 35mmSQ are available.

TEBGA Package external view



TEBGA Package cross section



TEBGA Package line-up

Package code	Pin count		Package size (mm)		Pin arrangement	Pin pitch (mm)
	Total	number of TBs* included	X	Y		
BGA-320P-Mxx	320	64	27.0	27.0	4 rows	1.27
BGA-416P-Mxx	416	64	27.0	27.0	4 rows	1.00
BGA-416P-M06	416	64	35.0	35.0	4 rows	1.27
BGA-480P-Mxx	480	64	27.0	27.0	5 rows	1.00
BGA-484P-M09	484	64	27.0	27.0	5 rows	1.00
BGA-484P-M08	484	64	35.0	35.0	5 rows	1.27
BGA-520P-Mxx	520	100	35.0	35.0	5 rows	1.27
BGA-543P-M01	543	64	27.0	27.0	6 rows	1.00
BGA-544P-M02	544	64	27.0	27.0	6 rows	1.00
BGA-676P-M10	676	—	27.0	27.0	Full Matrix	1.00
BGA-676P-M12	676	100	35.0	35.0	5 rows	1.00
BGA-770P-Mxx	772	100	35.0	35.0	6 rows	1.00
BGA-808P-M01	808	144	35.0	35.0	5+2 rows (With nonexistent pins)	1.00
BGA-868P-M01	868	196	35.0	35.0	6 rows	1.00
BGA-900P-M08	900	144	35.0	35.0	7 rows	1.00
BGA-1156P-M11	1156	—	35.0	35.0	Full Matrix	1.00

Please contact us for information on other pin arrangements.

*TB : Thermal Ball

FC-BGA

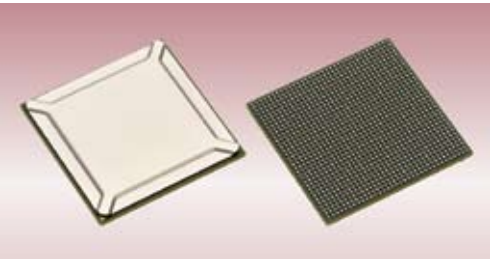
(Flip Chip Ball Grid Array)

Features

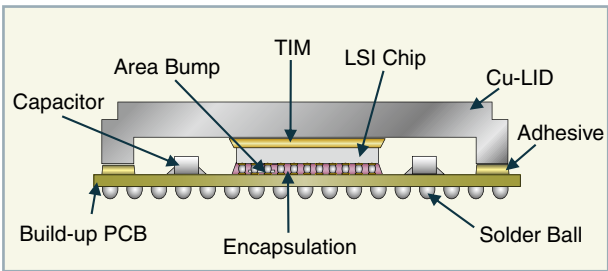
Superior electrical and thermal performance thanks to the flip chip bonding technology.
Wide support from consumer to high-end applications including servers.

- Support for ultra multi-pin by arranging the chip electrode over an area.
- Good dissipation of heat produced from the high electric consumption chip by deployment of a heat spreader.
- Capable of reduction of waveform distortion and high speed transmission (GHz level) for high frequencies.
- Fully customizable according to the customer's requirements.

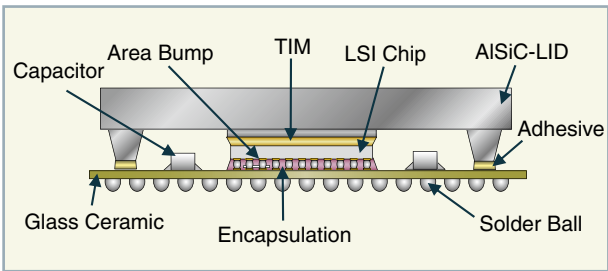
FC-BGA Package external view



FC-PBGA Package cross section



FC-CBGA Package cross section



FC-BGA Package line-up

FC-PBGA

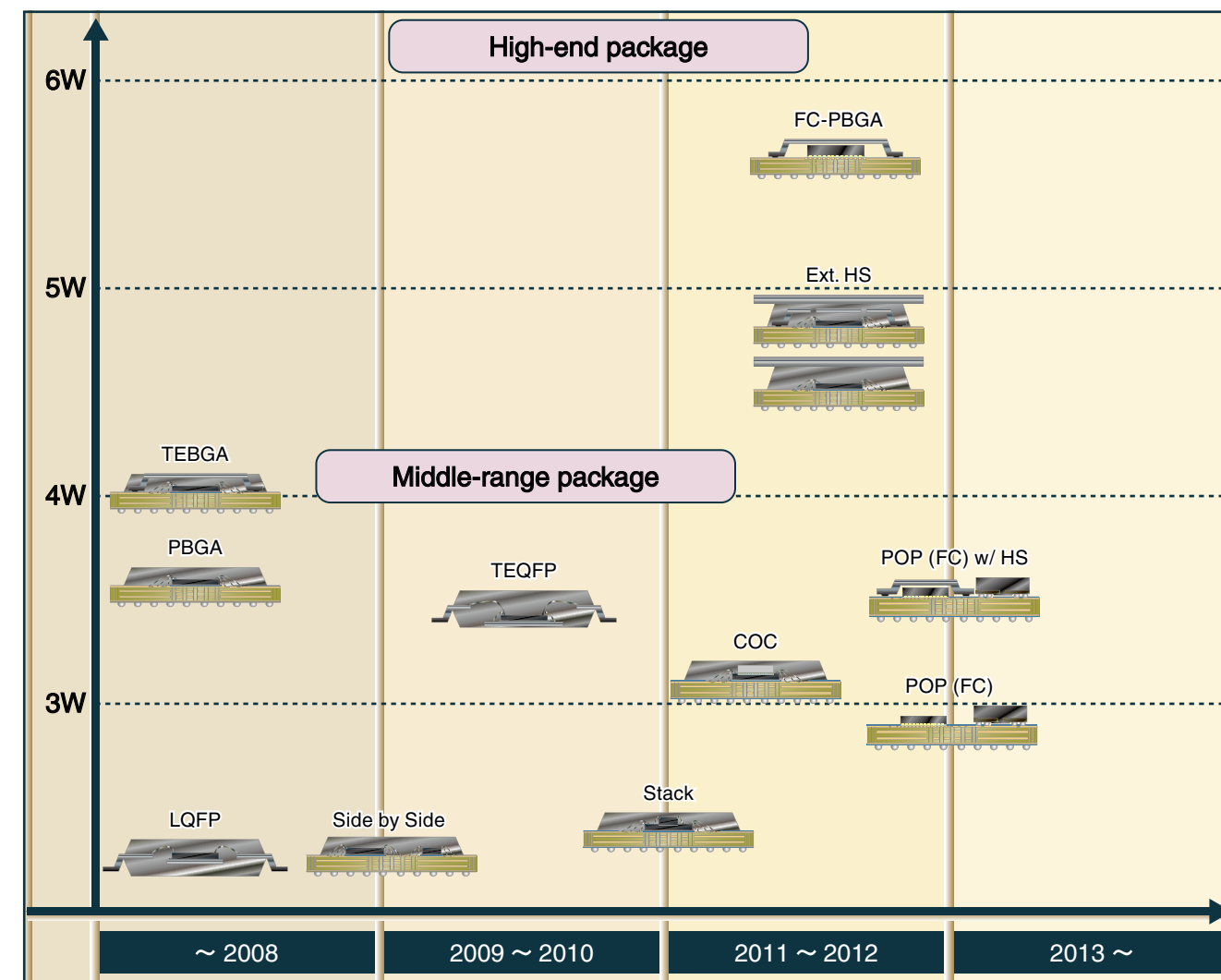
Pin count	Package size (mm)		Pin arrangement	Ball matrix	Pin pitch (mm)
	X	Y			
BGA484	23.0	23.0	Full Matrix	22 × 22	1.00
BGA592	21.0	21.0	Full Matrix (With nonexistent pins)	25 × 25	0.80
BGA625	17.0	17.0	Full Matrix	25 × 25	0.65
BGA625	27.0	27.0	Full Matrix	25 × 25	1.00
BGA729	29.0	29.0	Full Matrix	27 × 27	1.00
BGA900	31.0	31.0	Full Matrix	30 × 30	1.00
BGA1020	33.0	33.0	Full Matrix	32 × 32	1.00
BGA1156	35.0	35.0	Full Matrix	34 × 34	1.00
BGA1206	37.5	37.5	Full Matrix (With nonexistent pins)	36 × 36	1.00
BGA1396	37.5	37.5	Full Matrix	37 × 37	1.00
BGA1681	42.5	42.5	Full Matrix	41 × 41	1.00

FC-CBGA

Pin count	Package size (mm)		Pin arrangement	Ball matrix	Pin pitch (mm)
	X	Y			
BGA625	27.0	27.0	Full Matrix	25 × 25	1.00
BGA625	33.0	33.0	Full Matrix	25 × 25	1.27
BGA729	35.0	35.0	Full Matrix	27 × 27	1.27
BGA900	31.0	31.0	Full Matrix	30 × 30	1.00
BGA900	40.0	40.0	Full Matrix	30 × 30	1.27
BGA1089	42.5	42.5	Full Matrix	33 × 33	1.27
BGA1156	35.0	35.0	Full Matrix	34 × 34	1.00
BGA1225	45.0	45.0	Full Matrix	35 × 35	1.27
BGA1369	37.5	37.5	Full Matrix	37 × 37	1.00
BGA1681	42.5	42.5	Full Matrix	41 × 41	1.00
BGA2116	47.5	47.5	Full Matrix	46 × 46	1.00

Please contact us for information on other pin arrangements.

Middle to High-end package road map



Fujitsu Semiconductor will provide the most suitable SiP to the customer's requirements with our extensive implementation technologies. Please contact us for any requests.

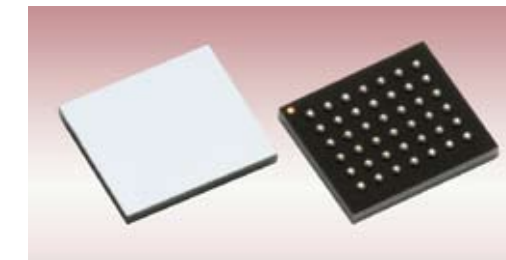
WL-CSP (Wafer Level CSP)

Features

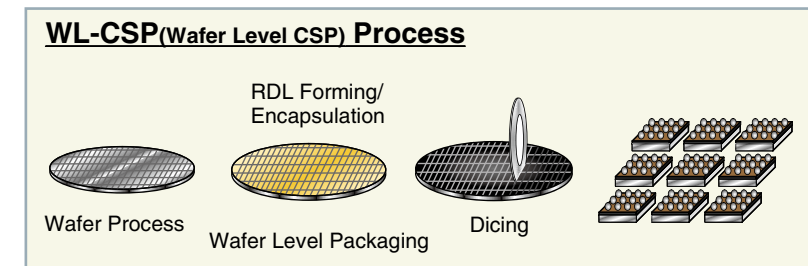
Ultra compact, ultra thin, multi-pin, and superior humidity and reflow resistance by wafer consistent assembly.
Also called as "Super CSP."

- Ultra compact, ultra thin, and light weight suitable for mobile devices and digital electric household appliances.
- JEDEC Moisture Sensitivity Level 1 clear.
- Support for pin pitch at less than or equal to 0.5mm contributing towards multi-pin.
- High speed transmission by reducing the wire length.
- Compliant with JEITA standards and fully customizable according to customer needs.

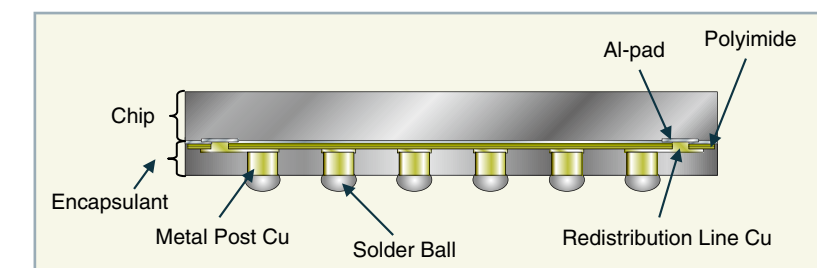
WL-CSP External view



WL-CSP Processes



WL-CSP Package cross section



Mass-production actual performance

WL-CSP	WLP112	WLP309	WLP15	WLP42	WLP70-02	WLP143
Wafer Size	200 mm	200 mm	200 mm	300 mm	300 mm	300 mm
Package Size	6.46 × 6.46 mm	7.56 × 7.56 mm	1.77 × 1.77 mm	3.30 × 2.95 mm	3.408 × 4.486 mm	7.81 × 6.10 mm
Package Height	0.6 mm Max	0.8 mm Max	0.64 mm Max	0.50 mm Max	0.35 mm Max	0.55 mm Max
Chip Thickness	390μm TYP	520μm TYP	390μm TYP	300μm TYP	220μm TYP	350μm TYP
Encapsulant Thickness	50μm TYP	50μm TYP	50μm TYP	50μm TYP	50μm TYP	50μm TYP
Ball Pitch	0.5 mm	0.4 mm	0.4 mm	0.4 mm	0.4 mm	0.5 mm
Ball Height	110μm TYP	150μm TYP	150μm TYP	100μm TYP	100μm TYP	100μm TYP

Technology road map

		2010	2011	2012
WL-CSP Structure	Height (Min)	0.25 mm	←	←
	Ball/Land pitch (Min)	0.3 mm	←	0.25 mm
	Ball/Land dia. (Min)	0.15 mm	←	0.13 mm
RDL Technology	Line/Space	20μm / 15μm	←	15μm / 15μm
	Via/Land Pitch (Inline)	50μm	←	40 μm
Others	Wafer size	6 / 8 / 12 inch	←	←
	Scribe Width (Min)	90μm	←	←
	6/8in	90μm (≤ 0.35-t)	←	←
	12in	100μm (> 0.35-t)	←	←
	Solder	Pb Free	←	←
	Mold resin	Halogen free	←	←

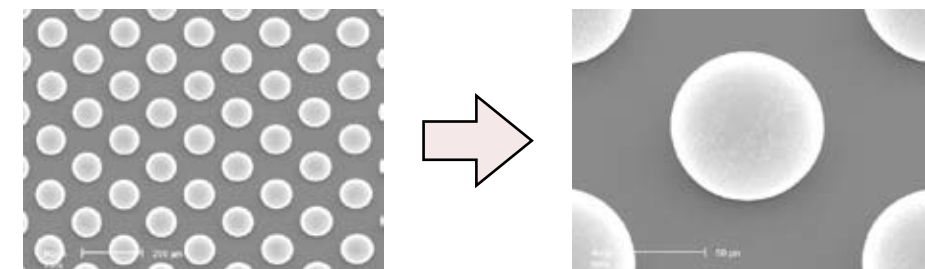
Bump on Pad

Features

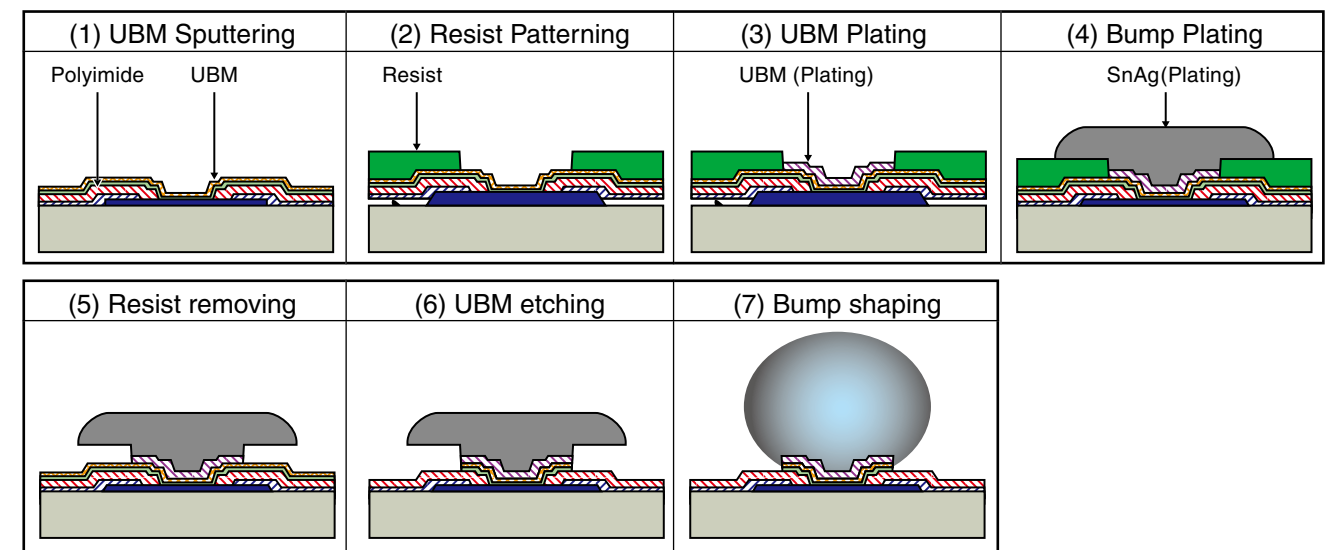
Wafer process and bumping in consolidated assembly.

- Technology supporting wide range of products from low-end applications such as mobile devices and digital electric household appliances to high-end applications such as servers.
- Promote multi-pin with min. 50μm AL pad pitch.
- Able to form wiring layer under a bump on demand.

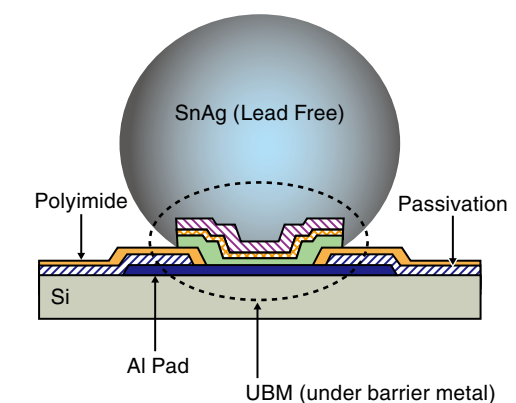
Bump External view



Manufacturing process

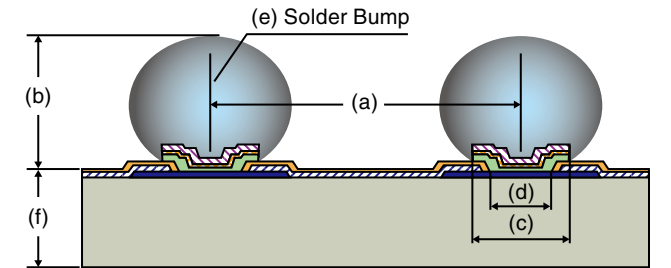


Bump Cross section



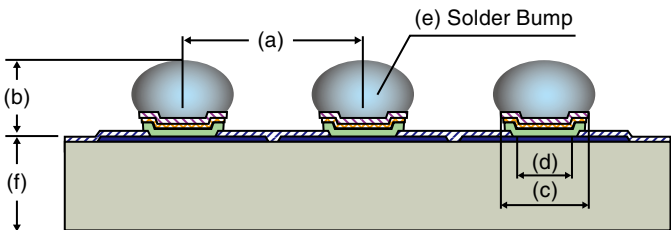
■ Typical specification

(a)	Bump pitch	176μm
(b)	Bump height	85μm
(c)	UBM size	80μm (typical)
(d)	Passivation opening size	50μm (typical)
(e)	Bump material	SnAg (or PbSn)
(f)	Chip thickness (the thinnest case)	200μm



■ Micro bump chip specification (example)

(a)	Bump pitch	50μm
(b)	Bump height	18μm
(c)	UBM size	32μm (typical)
(d)	Passivation opening size	17μm (typical)
(e)	Bump material	SnAg
(f)	Chip thickness (the thinnest case)	150μm



■ Mass-production actual performance

Wafer bumping	A	B	C
Purpose	High-end video	1seg tuner	Image processing
Wafer size	300 mm	300 mm	300 mm
Chip size	9.52 × 14.44 mm	2.90 × 2.90 mm	5.10 × 4.50 mm
UBM size	0.080 mm	0.080 mm	0.200 mm
Bump height	0.085 mm	0.085 mm	0.100 mm
Bump pitch	0.176 mm	0.250 mm	0.400 mm
Chip thickness	0.550 mm	0.185 mm	0.450 mm
Bump material	SnAg	SnAg	SnAg

■ Technology road map

	~ 2009	~ 2010	~ 2011	2012 ~
Standard bump	Pitch 150μm (Min) UBM 85μm (Max) Height 80μm (Max)		Pitch 130μm UBM 85μm Height 80μm	Pitch 100μm UBM 70μm Height 70μm
Micro bump	Pitch 50μm (Min) UBM 30μm (Min) Height 18μm (Max)		Pitch 40/30μm UBM 20μm Height 18μm	
Bump package		UBM 200μm (Max) Height 100μm (Max)		
Re-distribution layer bump	L&S 20/20μm (Min) UBM 200μm (Max) Height 100μm (Max)	L&S 15/20μm UBM 200μm Height 100μm		L&S 10/15μm UBM 200μm Height 100μm

■ Main package (Full scale: Size comparison)

[Notation example]
625 : Pin count
(17 × 17) : Package size (unit:mm)

