SERVICE MANUAL

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Version 0.0

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1. SPECIFICATION

1.1 General specification
- 1.1.1 Duplexer spacing : 80 MHz
- 1.1.2 Number of FA : 1150 channel
- 1.1.3 Power supply : 3.3 ± 10%
- 1.1.4 Power consumption :
  - 1) Talk : 450mA (+10dBm)
  - 2) Standby : 40mA for sleep mode, 200mA for idle mode
- 1.1.5 Operating temperature : -20C ~ 55C
- 1.1.6 Frequency stability : ± 150Hz
- 1.1.7 Antenna : Extendable Antenna
- 1.1.8 Size : 85.6 x 54.0 x 5.0 mm (3.37 x 2.13 x 0.197 in)
- 1.1.9 Weight : 34g

1.2 Receiver specifications
- 1.2.1 Frequency range : 1931.25 ~ 1988.75 MHz
- 1.2.2 Local oscillator frequency range : 1720 ~ 1780MHz
- 1.2.3 Intermediate frequency 210.38 MHz
- 1.2.4 Sensitivity : Better than -104 dBm

1.3 Transmitter Specifications
- 1.3.1 Frequency range 1851.25 ~ 1908.75 MHz
- 1.3.2 Emissions Designator: 1M25F7D
- 1.3.3 Local oscillator frequency range : 1720 ~ 1780 MHz
- 1.3.4 IF frequency : 130.38 MHz

1.3.5 Output power : 300 mW

2. OPERATING INSTRUCTION

Before the card can be used to access the internet or sending/receiving e-mails etc., installation of software for the 1900-1X-CDMA card needs to be performed as per the instructions that accompany the installation diskette/CD. When the card is installed and configured properly, it will be automatically recognized when inserted in the type II slot in a Laptop computer. The data can be accessed by clicking On the self explanatory icons in the 1900-1X-CDMA driver software.

3. CIRCUIT INSTRUCTION

1900-1X-CDMA is designed based on the CDMA standard, EIA/TIA and consisted of RF and logic assembly part.

3.1 RF part

RF part consists of power supply, frequency synthesizer, TX and RX sections.

3.1.1 Power supply

Power for RF section is supplied from laptop battery. Following voltages are generated by the on-board power management IC: ;

- 3.0V → RX IF part
- 3.0V → TX RF part
- 3.0V → PLL
- 3.0V → TCXO
- 3.0V → IFT, IFR, Baseband circuitry
- 3.0V → PA_REF
- 2.8V → PCMCIA interface circuitry

3.1.2 Frequency synthesizer

Frequency synthesizer uses VC_TCXO (19.68 MHz) as a reference frequency. Then 19.68MHz of VC_TCXO is divided by the reference divider to 10KHz comparison frequency. The internal RF VCO generates the LO frequencies for both TX/RX bands and receive IF. The DC control voltage for TCXO is generated by low pass filtering a PDM waveform provided by MSM-5500 baseband IC. The synthesizer employs a digital phase locked loop (PLL) technique. Combined with a high quality reference OSC, it provides a very stable local oscillator (LO) in the range of 1720 ~ 1780 MHz and 420.76 MHz for receive IF local oscillator.

3.1.2.2 Rx IF synthesizer (420.76 MHz)

Rx IF synthesizer oscillates at 420.76 MHz that is the double of Rx IF frequency. The IF frequency 210.38 MHz is generated inside the IFR chip by dividing this frequency by 2.

3.1.2.3 Tx IF synthesizer (260.76MHz)

TX PLL consists of PLL synthesizer, IFT3000, Loop filter and the VC_TCXO. It oscillates at 260.76MHz that is double the the TX IF frequency. The 130.38MHz TX IF frequency is generated by dividing this by 2 inside the IFT

3.1.3 Rx part

Rx parts consist of Agilent FBAR duplexer, Receiver front end chip (LNA, down converter), IF SAW and IFR3000 and the role of each part is as follows;

3.1.3.1 Duplxer

Agilent FBAR Duplexer consists of TX and RX filters TX filter consists of BPF (Band Pass Filter) and rejects any TX spurs or noise falling into the RX band. The RX port has a BPF that prevents TX interference into the RX band.

3.1.3.2 RF F/E MD59-0049 LNA/DOWNCONVERTER

MD-59-0049 front end chip consists of an LNA, RF amplifier, Mixer, IF amplifier, and LO Buffer. This IC has good linearity, wide dynamic range, and low power consumption.

The down converter generates RF_IF of 210.38 using the PLLMHz which is fed in to the IF-Baseband chip (IFR-3000).

3.1.3.3 IFR3000

IFR3000 is located between MSM-5000 digital processor and RF subsystem. It controls the RX power level with an internal AGC (Automatic Gain Control) amplifier, depending on the IF signal strength. It has 90dB of dynamic range. The full dynamic range is from +45dB to –45 dB at gain control voltage of 2.8 to 0.1 volts respectively. The IF mixer down-converts RX-IF signal (210.38 MHz) to quadrature analog basedband.

IFR-3000 CDMA receive signal path includes;

IF to Baseband Down Conversion
Separate Filters and ADCs
Conversion of analog base-band to digital format

CDMA sampling clock synthesizer
Local Oscillator for I-Q Mixer
I.Q offset Control Loop
Three-line Serial Bus Interface (SBI) for initializing and control of the IFR3000 from MSM5000

3.1.3.4 RX-IF SAW

RX-IF SAW is used to reject any undesirable out of band signal.

Rx Mode Operation

210.38 MHz of RX center frequency includes CDMA spread spectrum modulation signal that ±630KHz wide. Rx center frequency is converted to the I&Q baseband signal through a mixer that is part of IFR3000. The receive signal is passed on to MSM5000 after low pass filtering. . . This signal is digitized by 4 bit flash ADC.

3.1.4 TX Part

TX part consists of IFT3000, Up Converter, Power Amplifier Pre – Driver, Power Amplifier IC, and Duplexer and the role of each part is as follows ;

3.1.4.1 IFT3000 (Baseband-IF Converter)

IFT3000 consists of AGC amplifier and Baseband Analog Processor and TX IF PLL.
IFT3000 converts digital I and Q baseband components into analog I and Q components, and converts up to the IF frequency and puts out an amplitude controlled
Tx IF signal. Base-band analog processor has PLL in it and has general purpose ADC circuit to read the battery
strength and temperature.
AGC is designed to control the gain according to the strength of signal that is generated from Tx IF synthesizer within 84dB of maximmum dynamic
range. The gain of the AGC amplifier is +0.8dB when gain control voltage is 2.7V and is –82.3dB when gain control voltage is 0.3V but actually uses 80dB
(0.7V ~ 2.5V) of gain range.
Single mode operation for CDMA transmit signal path includes ;
Conversion of digital I-Q Data to Analog Base Band Signals
Base Band to IF Up Conversion
Local Oscillator for I-Q Mixer
Mode Control Logic for Rx/Tx
General Purpose ADC for System Monitoring
Three-line Serial Bus Interface (SBI) for control of the IFT3000 via the MSM3000

Tx Operation Mode

8Bits I,Q Data that is from MSM3000 is input to I,Q D/A Converter. I data from rising edge of Tx clock is saved at I DAC and Q data from fallingedge is saved at Q DAC. The frequency spectrum of CDMA DAC has noise that is generated at Tx clock is
filtered by the anti -aliasing LPF (630KHz).. These analog, I,Q signals is synthesized
differentially with 130.38MHz IF that is generated at synthesizer of Tx center frequency and transferred to Tx AGC part.

3.1.4.2 TX Up converter and Power Amplifier Pre-Driver:

The final TX frequency of 1850-1910MHz is generated by the TX upconverter and driver amplifier chip using the IF of 130.38MHz and 1720-1780MHz LO generated by the PLL. The PA driver amplifies this signal so that PA sees a sufficient signal level at its input.

3.1.4.3 Power Amplifier

The power amplifier amplifies the TX power to required transmit levels with sufficient linearity to keep the spurious emissions within limits. The voltage for the PA is supplied directly from the main supply. It can be turned off by taking the PA_ON input low.

3.2 Logic part

Logic part consists of power supply, digital part, PCMCIA interface part.

3.2.1 Power Supply

Power is supplied to the power management IC directly from the Laptop supply. The power management IC generates different voltages as required by other sections of the card.

3.2.2 Digital Circuits

Digital part consists of MSM5000, Memory (Flash, SRAM) and EEPROM. MSM5000 is the ASIC chip designed for base-band digital signal processing
and the standard clock that is needed for operation is ; CHIPx8 (9.8304MHz) provided from RF part and 2 resonators (27MHz & 32.768KHz. The role of each clock is as follows;

- CHIPx8 : The clock that is developed in the IFR3000 by dividing the 19.68MHz TCXO frequency by a
512/1025 divider.

- TCXO : The clock source for various blocks of the MSM3500.- 27MHz : The clock is needed for operation of u -processor that is in MSM53000
- 32.768KHz : This clock extends the battery life by operating the during sleep mode to save the power.

MSM500 has following features:
- Low operating voltage (2.7 ~ 3.6V)
- Interfaces with IFT3000 and IFR3000 of RF part directly
- Includes EVRC vocoder internally and can have external vocoder optionally
- Includes internal echo cancellation
- Including internal voice operated switch
- Microprocessor of ARM7TDMI is operated as sub-system

Memory consists of 8Mbit Flash, 2Mbit SRAM and 128Kbit of EEPROM. The main programs of the data-card are stored in Flash ROM. ESN, NAM and other parameters and data related to call processing is stored in EEPROM.
SRAM has system parameters, data buffer and the stack values of each task.