# TRF7970A Multiprotocol Fully Integrated 13.56-MHz RFID and Near Field Communication (NFC) Transceiver IC

## 1 Device Overview

### 1.1 Features

- Supports Near Field Communication (NFC) Standards NFCIP-1 (ISO/IEC 18092) and NFCIP-2 (ISO/IEC 21481)
- Completely Integrated Protocol Handling for ISO15693, ISO18000-3, ISO14443A/B, and FeliCa™
- Integrated Encoders, Decoders, and Data Framing for NFC Initiator, Active and Passive Target Operation for All Three Bit Rates (106 kbps, 212 kbps, 424 kbps) and Card Emulation
- RF Field Detector With Programmable Wake-Up Levels for NFC Passive Transponder Emulation Operation
- RF Field Detector for NFC Physical Collision Avoidance.
- Integrated State Machine for ISO14443A Anticollision (Broken Bytes) Operation (Transponder Emulation or NFC Passive Target)
- Input Voltage Range: 2.7 VDC to 5.5 VDC
- Programmable Output Power: +20 dBm (100 mW), +23 dBm (200 mW)
- Programmable I/O Voltage Levels From 1.8 VDC to 5.5 VDC
- Programmable System Clock Frequency Output (RF, RF/2, RF/4) from 13.56-MHz or 27.12-MHz Crystal or Oscillator
- Integrated Voltage Regulator Output for Other System Components (MCU, Peripherals, Indicators), 20 mA (Max)
- Programmable Modulation Depth
- Dual Receiver Architecture With RSSI for Elimination of "Read Holes" and Adjacent Reader System or Ambient In-Band Noise Detection
- Programmable Power Modes for Ultra Low-Power System Design (Power Down <1 µA)
- Parallel or SPI Interface (With 127-Byte FIFO)
- Temperature Range: –40°C to 110°C
- 32-Pin QFN Package (5 mm x 5 mm)

### 1.2 Applications

- Mobile Devices (Tablets, Handsets)
- Secure Pairing ( *Bluetooth*®, Wi-Fi®, Other Paired Wireless Networks)
- Public Transport or Event Ticketing
- Passport or Payment (POS) Reader Systems
- Short-Range Wireless Communication Tasks (Firmware Updates)
- Product Identification or Authentication
- Medical Equipment or Consumables
- Access Control, Digital Door Locks
- Sharing of Electronic Business Cards

### 1.3 Description

The TRF7970A device is an integrated analog front end and data-framing device for a 13.56-MHz RFID and Near Field Communication (NFC) system. Built-in programming options make the device suitable for a wide range of applications for proximity and vicinity identification systems.

The device can perform in one of three modes: RFID and NFC reader, NFC peer, or in card emulation mode. Built-in user-configurable programming options make the device suitable for a wide range of applications. The TRF7970A device is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

Documentation, reference designs, EVM, and source code TI MSP430™ MCUs or ARM® MCUs are available.

**Device Information**

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| TRF7970ARHB | VQFN (32) | 5 mm x 5 mm |

## 1.4 Functional Block Diagram

Figure 1-1 shows the block diagram.

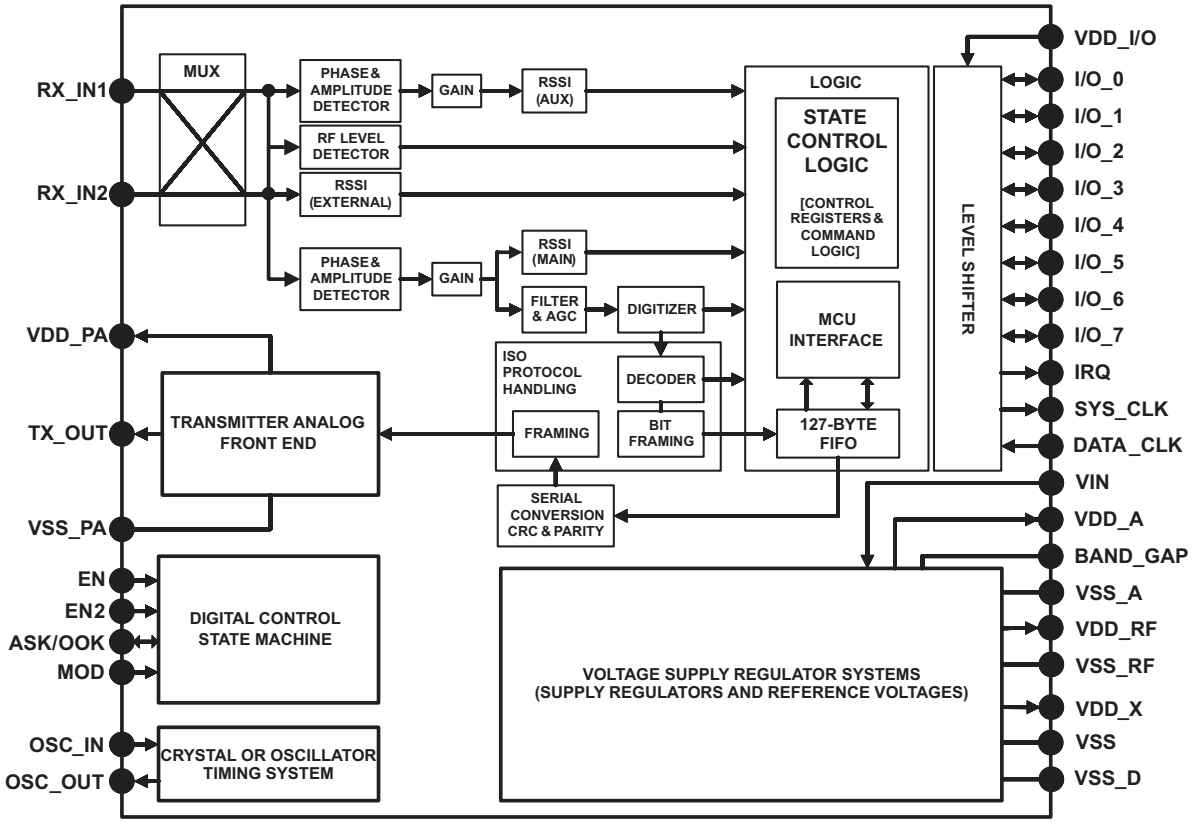


**Figure 1-1. Block Diagram**

# Table of Contents

## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision J (February 2014) to Revision K | Page |
|---|---|
| • Changed Figure 1-1 to show 127-byte FIFO | 2 |
| • Moved Section 3 | 5 |
| • Changed title of Section 4 | 6 |
| • Changed title of Section 5 | 9 |
| • Added ASK/OOK and MOD to $V_{IL}$ and $V_{IH}$ | 9 |
| • Moved Section 5.3 | 10 |
| • Changed $V_{DD\_A}$ TYP value from 3.5 V to 3.4 V | 10 |
| • Moved Section 5.4 | 11 |
| • Added $V_{(ESD)}$ MIN values, test specifications, and notes | 11 |
| • Changed title of Section 5.5 from Dissipation Ratings to Thermal Characteristics | 11 |
| • Moved Section 5.6 | 11 |
| • Changed title of Section 6 | 12 |
| • Moved previous Section 3, Device Overview, to Section 6.1 | 12 |
| • Changed from "By default, the AGC is frozen after..." to "By default, the AGC window comparator is set after..." | 21 |
| • Changed from "TX Pulse Length Control register (0x05)" to "TX Pulse Length Control register (0x06)" | 28 |
| • Changed from "18.8 s" to "18.8 µs" in the sentence that starts with "If the register contains all zeros..." | 28 |
| • Changed Table 6-18 to match Table 6-43 | 50 |
| • Changed command 0x18 to "Test internal RF" | 51 |
| • Changed command 0x19 to "Test external RF" | 51 |
| • Moved Section 6.14 | 55 |
| • Changed the sentence that starts "The AGC action is fast..." from "finishes after four subcarrier pulses" to "finishes within eight subcarrier pulses" | 64 |
| • Moved Section 7 | 75 |
| • Deleted previous Section 10, System Design, and moved contents to Section 7.3 through Section 7.5 | 77 |
| • Removed references to figure numbers in Figure 7-3 | 78 |

# 3 Device Characteristics

Table 3-1 shows the supported modes of operation for the TRF7970A device.

**Table 3-1. Supported Modes of Operation**

| P2P Initiator or Reader/Writer | | Card Emulation | | P2P Target | |
|---|---|---|---|---|---|
| Technology | Bit rate (kbps) | Technology | Bit rate (kbps) | Technology | Bit rate (kbps) |
| NFC-A/B (ISO14443A/B) | 106, 212, 424, 848(1) | NFC-A/B | 106 | NFC-A | 106 |
| NFC-F (JIS: X6319-4) | 212, 424 | N/A | N/A | NFC-F | 212, 424 |
| NFC-V (ISO15693) | 6.7, 26.7 | N/A | N/A | N/A | N/A |

(1) 848 kbps only applies to reader/writer mode.

# 4 Terminal Configuration and Functions

## 4.1 Pin Assignments

Figure 4-1 shows the pin assignments for the 32-pin RHB package.

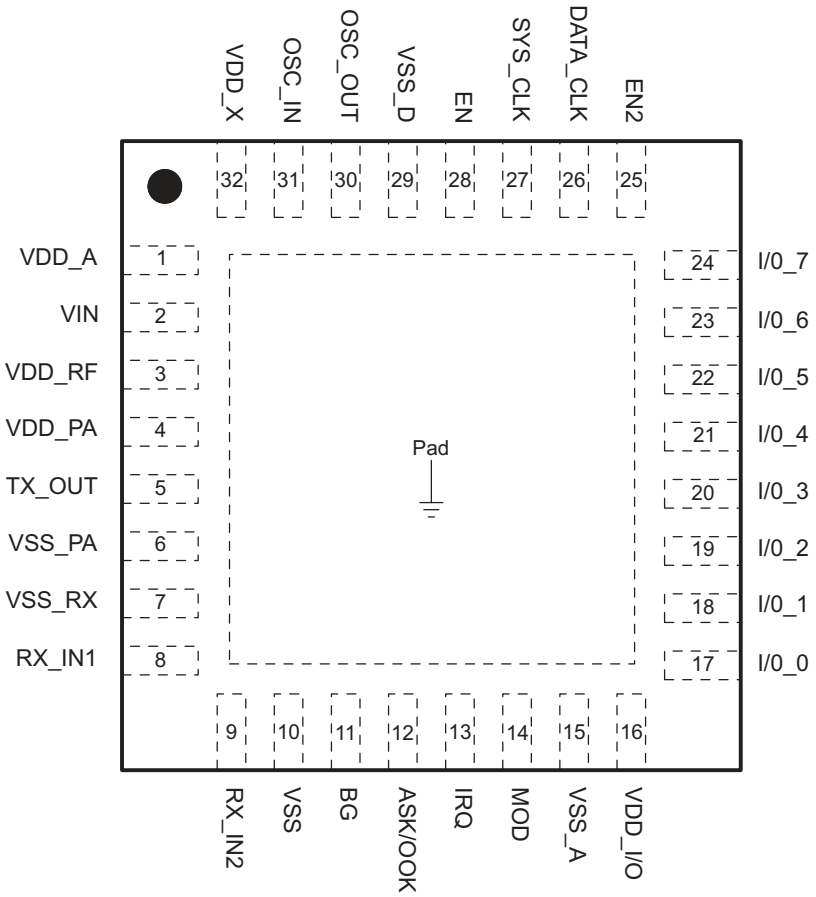


**Figure 4-1. 32-Pin RHB Package (Top View)**

## 4.2 Terminal Functions

Table 4-1 describes the signals.

**Table 4-1. Terminal Functions**

| TERMINAL | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $V_{DD\_A}$ | 1 | OUT | Internal regulated supply (2.7 V to 3.4 V) for analog circuitry |
| $V_{IN}$ | 2 | SUP | External supply input to chip (2.7 V to 5.5 V) |
| $V_{DD\_RF}$ | 3 | OUT | Internal regulated supply (2.7 V to 5 V), normally connected to $V_{DD\_PA}$ (pin 4) |
| $V_{DD\_PA}$ | 4 | INP | Supply for PA; normally connected externally to $V_{DD\_RF}$ (pin 3) |
| TX_OUT | 5 | OUT | RF output (selectable output power, 100 mW or 200 mW, with $V_{DD}$ = 5 V) |
| $V_{SS\_PA}$ | 6 | SUP | Negative supply for PA; normally connected to circuit ground |
| $V_{SS\_RX}$ | 7 | SUP | Negative supply for RX inputs; normally connected to circuit ground |
| RX_IN1 | 8 | INP | Main RX input |
| RX_IN2 | 9 | INP | Auxiliary RX input |
| $V_{SS}$ | 10 | SUP | Chip substrate ground |
| BAND_GAP | 11 | OUT | Bandgap voltage ($V_{BG}$ = 1.6 V); internal analog voltage reference |
| ASK/OOK | 12 | BID | Selection between ASK and OOK modulation (0 = ASK, 1 = OOK) for Direct Mode 0 or 1.<br>Can be configured as an output to provide the received analog signal output. |
| IRQ | 13 | OUT | Interrupt request |
| MOD | 14 | INP | External data modulation input for Direct Mode 0 or 1 |
| | | OUT | Subcarrier digital data output (see registers 0x1A and 0x1B) |
| $V_{SS\_A}$ | 15 | SUP | Negative supply for internal analog circuits; connected to GND |
| $V_{DD\_I/O}$ | 16 | INP | Supply for I/O communications (1.8 V to $V_{IN}$) level shifter. $V_{IN}$ should be never exceeded. |
| I/O_0 | 17 | BID | I/O pin for parallel communication |
| I/O_1 | 18 | BID | I/O pin for parallel communication |
| I/O_2 | 19 | BID | I/O pin for parallel communication<br>TX Enable (in Special Direct Mode) |
| I/O_3 | 20 | BID | I/O pin for parallel communication<br>TX Data (in Special Direct Mode) |
| I/O_4 | 21 | BID | I/O pin for parallel communication<br>Slave Select signal in SPI mode |
| I/O_5 | 22 | BID | I/O pin for parallel communication<br>Data clock output in Direct Mode 1 and Special Direct Mode |
| I/O_6 | 23 | BID | I/O pin for parallel communication<br>MISO for serial communication (SPI)<br>Serial bit data output in Direct Mode 1 or subcarrier signal in Direct Mode 0 |
| I/O_7 | 24 | BID | I/O pin for parallel communication.<br>MOSI for serial communication (SPI) |
| EN2 | 25 | INP | Selection of power down mode. If EN2 is connected to $V_{IN}$, then $V_{DD\_X}$ is active during power down mode 2 (for example, to supply the MCU). |
| DATA_CLK | 26 | INP | Data Clock input for MCU communication (parallel and serial) |
| SYS_CLK | 27 | OUT | If EN = 1 (EN2 = don't care) the system clock for MCU is configured. Depending on the crystal that is used, options are as follows (see register 0x09):<br>13.56-MHz crystal: Off, 3.39 MHz, 6.78 MHz, or 13.56 MHz<br>27.12-MHz crystal: Off, 6.78 MHz, 13.56 MHz, or 27.12 MHz<br>If EN = 0 and EN2 = 1, then system clock is set to 60 kHz |
| EN | 28 | INP | Chip enable input (If EN = 0, then chip is in sleep or power-down mode). |
| $V_{SS\_D}$ | 29 | SUP | Negative supply for internal digital circuits |

(1) SUP = Supply, INP = Input, BID = Bidirectional, OUT = Output

**Table 4-1. Terminal Functions (continued)**

| TERMINAL | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| OSC_OUT | 30 | OUT | Crystal or oscillator output |
| OSC_IN | 31 | INP | Crystal or oscillator input |
| | | OUT | Crystal oscillator output |
| $V_{DD\_X}$ | 32 | OUT | Internally regulated supply (2.7 V to 3.4 V) for digital circuit and external devices (for example, MCU) |
| Thermal Pad | PAD | SUP | Chip substrate ground |

# 5 Specifications

## 5.1 Absolute Maximum Ratings (1) (2)

over operating free-air temperature range (unless otherwise noted)

| | | | |
|---|---|---|---|
| $V_{IN}$ | Input voltage range | | -0.3 V to 6 V |
| $I_{IN}$ | Maximum current $V_{IN}$ | | 150 mA |
| $T_J$ | Maximum operating virtual junction temperature | Any condition | 140°C |
| | | Continuous operation, long-term reliability (3) | 125°C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to substrate ground terminal $V_{SS}$.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability or lifetime of the device.

## 5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating input voltage | | 2.7 | 5 | 5.5 | V |
| $T_A$ | Operating ambient temperature | | -40 | 25 | 110 | °C |
| $T_J$ | Operating virtual junction temperature | | -40 | 25 | 125 | °C |
| $V_{IL}$ | Input voltage - logic low | I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2, ASK/OOK, MOD | | | 0.2 x $V_{DD\_I/O}$ | V |
| $V_{IH}$ | Input voltage threshold, logic high | I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2, ASK/OOK, MOD | 0.8 x $V_{DD\_I/O}$ | | | V |

## 5.3 Electrical Characteristics

TYP operating conditions are $T_A$ = 25°C, VIN = 5 V, full-power mode (unless otherwise noted)
MIN and MAX operating conditions are over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{PD1}$ | Supply current in Power Down Mode 1 | All building blocks disabled, including supply-voltage regulators; measured after 500-ms settling time (EN = 0, EN2 = 0) | | 0.5 | 5 | µA |
| $I_{PD2}$ | Supply current in Power Down Mode 2 (Sleep Mode) | The SYS_CLK generator and $V_{DD\_X}$ remain active to support external circuitry; measured after 100-ms settling time (EN = 0, EN2 = 1) | | 120 | 200 | µA |
| $I_{STBY}$ | Supply current in stand-by mode | Oscillator running, supply-voltage regulators in low-consumption mode (EN = 1, EN2 = x) | | 1.9 | 3.5 | mA |
| $I_{ON1}$ | Supply current without antenna driver current | Oscillator, regulators, RX and AGC active, TX is off | | 10.5 | 14 | mA |
| $I_{ON2}$ | Supply current – TX (half power) | Oscillator, regulators, RX and AGC and TX active, $P_{OUT}$ = 100 mW | | 70 | 78 | mA |
| $I_{ON3}$ | Supply current – TX (full power) | Oscillator, regulators, RX and AGC and TX active, $P_{OUT}$ = 200 mW | | 130 | 150 | mA |
| $V_{POR}$ | Power-on reset voltage | Input voltage at $V_{IN}$ | 1.4 | 2 | 2.6 | V |
| $V_{BG}$ | Bandgap voltage (pin 11) | Internal analog reference voltage | 1.5 | 1.6 | 1.7 | V |
| $V_{DD\_A}$ | Regulated output voltage for analog circuitry (pin 1) | $V_{IN}$ = 5 V | 3.1 | 3.4 | 3.8 | V |
| $V_{DD\_X}$ | Regulated supply for external circuitry | Output voltage pin 32, $V_{IN}$ = 5 V | 3.1 | 3.4 | 3.8 | V |
| $I_{VDD\_Xmax}$ | Maximum output current of $V_{DD\_X}$ | Output current pin 32, $V_{IN}$ = 5 V | | | 20 | mA |
| $R_{RFOUT}$ | Antenna driver output resistance (1) | Half-power mode, $V_{IN}$ = 2.7 V to 5.5 V | | 8 | 12 | Ω |
| | | Full-power mode, $V_{IN}$ = 2.7 V to 5.5 V | | 4 | 6 | |
| $R_{RFIN}$ | RX_IN1 and RX_IN2 input resistance | | 4 | 10 | 20 | kΩ |
| $V_{RF\_INmax}$ | Maximum RF input voltage at RX_IN1 and RX_IN2 | $V_{RF\_INmax}$ should not exceed $V_{IN}$ | | 3.5 | | $V_{pp}$ |
| $V_{RF\_INmin}$ | Minimum RF input voltage at RX_IN1 and RX_IN2 (input sensitivity)(2) | $f_{SUBCARRIER}$= 424 kHz | | 1.4 | 2.5 | $mV_{pp}$ |
| | | $f_{SUBCARRIER}$ = 848 kHz | | 2.1 | 3 | |
| $f_{SYS\_CLK}$ | SYS_CLK frequency | In power mode 2, EN = 0, EN2 = 1 | 25 | 60 | 120 | kHz |
| $f_C$ | Carrier frequency | Defined by external crystal | | 13.56 | | MHz |
| $t_{CRYSTAL}$ | Crystal run-in time | Time until oscillator stable bit is set (register 0x0F)(3) | | 3 | | ms |
| $f_{D\_CLKmax}$ | Maximum DATA_CLK frequency(4) | Depends on capacitive load on the I/O lines, recommendation is 2 MHz(4) | 2 | 8 | 10 | MHz |
| $R_{OUT}$ | Output resistance I/O_0 to I/O_7 | | | 500 | 800 | Ω |
| $R_{SYS\_CLK}$ | Output resistance $R_{SYS\_CLK}$ | | | 200 | 400 | Ω |

(1) Antenna driver output resistance
(2) Measured with subcarrier signal at RX_IN1 or RX_IN2 and measured the digital output at MOD pin with register 0x1A bit 6 = 1.
(3) Depends on the crystal parameters and components
(4) Recommended DATA_CLK speed is 2 MHz. Higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load used).

## 5.4 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | | -55 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | -2 | 2 | kV |
| | | Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins(2) | -500 | 500 | V |
| | | Machine Model (MM) | -200 | 200 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance.

## 5.5 Thermal Characteristics

| PACKAGE | $\theta_{JC}$ | $\theta_{JA}$(1) | POWER RATING(2) | |
|---|---|---|---|---|
| | | | $T_A \le 25°C$ | $T_A \le 85°C$ |
| RHB (32 pin) | 31°C/W | 36.4°C/W | 2.7 W | 1.1 W |

(1) This data was taken using the JEDEC standard high-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

## 5.6 Switching Characteristics

TYP operating conditions are $T_A$ = 25°C, VIN = 5 V, full-power mode (unless otherwise noted)
MIN and MAX operating conditions are over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{LO/HI}$ | DATA_CLK time high or low, one half of DATA_CLK at 50% duty cycle | Depends on capacitive load on the I/O lines(1) | 250 | 62.5 | 50 | ns |
| $t_{STE,LEAD}$ | Slave select lead time, slave select low to clock | | | 200 | | ns |
| $t_{STE,LAG}$ | Slave select lag time, last clock to slave select high | | | 200 | | ns |
| $t_{STE,DIS}$ | Slave select disable time, slave select rising edge to next slave select falling edge | | 300 | | | ns |
| $t_{SU,SI}$ | MOSI input data setup time | | 15 | | | ns |
| $t_{HD,SI}$ | MOSI input data hold time | | 15 | | | ns |
| $t_{SU,SO}$ | MISO input data setup time | | 15 | | | ns |
| $t_{HD,SO}$ | MISO input data hold time | | 15 | | | ns |
| $t_{VALID,SO}$ | MISO output data valid time | DATA_CLK edge to MISO valid, $C_L \le 30$ pF | 30 | 50 | 75 | ns |

(1) Recommended DATA_CLK speed is 2 MHz. Higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load used).

## Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

**FCC Caution:**

- Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
- This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

**Radiation Exposure Statement:**

The product is a low power device and its output power is lower than FCC SAR exemption level. This module can be used with **Product name: T800**.

**This device is intended only for OEM integrators under the following conditions:**

1) The transmitter module may not be co-located with any other transmitter or antenna. The co-transmitting with other radio will need a separate evaluation.
2) Module approval valid only when this module is installed in the tested host "**Product name: T800**".

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed

**IMPORTANT NOTE:** In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

**End Product Labeling**

The final end product must be labeled in a visible area with the following: "**Contains FCC ID: QYLT800N**". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

**Manual Information to the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.