KME 900 Instruction Draft

1, Receiver Circuit

The FM dual-conversion super heterodyne receiver is designed for operation in the 935-941MHz frequency range.
The Receiver has intermediate frequencies (IF) of 82.2MHz and 455KHz.
Adjacent channel selectivity is obtained by using two band pass filters, a 82.2MHz crystal filter and a 455KHz ceramic filter.
The FM-detector is Quadrature discriminator.

1-1 Receiver Front-end

A RF signal from antenna is coupled though the low pass filters, antenna switch and band pass filter to the input of low noise amplifier TR201. The output of TR201 is coupled through band pass filter to input of 1'st Mixer TR203.
Front End selectivity is provided by these band pass filter.

1-2 1'st Mixer

The 1'st Mixer is a Transistor-Mixer (TR203), that converts a RF signal the 935-941MHz range to 82.2MHz 1'st IF frequency.
In the mixer stage, A RF signal from the Front-end RF filter is applied to the input of the Transistor-Mixer.

1-3 1'st IF

The 82.2MHz 1'st IF output signal is coupled from the output of T201 through IF amplifier TR204 and Crystal filter FL201 to IF-amplifier TR205.
The highly-selective crystal filters FL201-1 and FL 201-2 provide the first portion of the receiver IF selectivity. The out put of the filters is coupled through the impedance-matching net work T204, C246 and R224 to 1'st IF amplifier TR205.

1-4 2'nd Mixer, 2'nd IF filter,2'nd IF amplifier and FM detector

IC201 is an one-chip IC for FM communication system. It includes 2'nd Mixer, 2'nd IF amplifier and FM detector.
The 2'nd Mixer is a Balanced Mixer, that converts a 1'st IF signal 82.2MHz range to 455KHz 2'nd IF frequency. The 2'nd IF signal is applied to Ceramic Filter FL203, which provides the 455KHz selectivity. The output of the 2'nd IF filter is applied to 2'nd IF amplifier in IC201.
The 2'nd IF signal is then amplified, filtered and limited. Discriminator (DSC201) shifts the 2'nd IF signal by 90deg and applies it to the internal FM detector.
The FM detector compares the shifted IF signal to the internal IF signal to recover the audio modulation. The audio output of IC201 is applied to audio amplifier buffer IC205-2.
The audio output of IC205-2 is then applied to the SYSTEM CONTROL UNIT.

2, Transmitter Circuit

The Transmitter Circuit consists of one Class-A Amplifier TR101, Pre-Driver IC101, PA Module IC102, RF Amplifier TR102, Automatic Power Control Circuit (TR105- TR107), Antenna Switch (CD103, CD105-CD107 and CD109), Low Pass Filter (Micro Strip Line and C146-C153, C181 and C183).

2-1 Class-A Amplifier

The 896-902MHz and 935-941MHz RF input from Synthesizer output of TR316 is applied to the band pass filter FL301 through an attenuator pad R301-R303. RF input level is about +3dBm, that is amplified to +10dBm by TR101. This is controlled by TXENB+.

2-2 Pre-Driver

The output of TR101 is applied to the Pre-Driver IC101 through an attenuator pad R106-R108. The output of R107 is also amplified to about 600mW by IC101. This is controlled by TXENB+. The Pre-Driver consists of three stages RF amplifier. The first and second stages in IC101 are operated in Class-B. The third stage in IC101 is operated in Class-C.

2-3 PA Module

The output of IC101 is applied to the PA Module IC102 through an attenuator pad R110-R112. The output of R110 is amplified to about 13W. The PA Module consists of three stages RF amplifier. The first stage power supply voltage is controlled by power control circuit. The second and third stage power supply voltages are supplied by B_A+ via TR108. The first and second RF amplifiers are operated in Class-B. The third RF amplifier is operated in Class-C.

2-4 RF Amplifier

The input (about 13W) of the RF Amplifier is amplified to 25W.
Power Supply voltage for the RF Amplifier is connected with POWER SUPPLY BOARD through C1.

2-4 Automatic Power Control

The Automatic Power Control circuit samples the output power to the antenna to maintain a constant power level across the band. Also, a thermistor circuit (TR104 and RT101) senses the PA Module temperature to reduce the power level when the temperature is above +110°C. The Automatic Power Control circuit controls the supply voltage to the first stage in PA Module IC102. Directional coupler provides a sample of transmit power for diode CD102. Diode CD102 produce a positive DC voltage proportional to the transmit circuit output power level. When above VSWR 3, reflect coupler provides a sample of reflection power for diode CD101. Diode CD101 and CD102 produce voltages are summed, then that is compared to APCREF (D/A Voltage) from SYSTEM CONTROL UNIT by the amplifier TR105. The collector of TR105 is applied to DC amplifier TR106 and TR107, then the output voltage of TR107 controls to the first stage of PA Module.

2-5 Antenna Switch and Low Pass Filter

The Antenna Switch consists of CD103, CD105-CD107, CD109 and the Low Pass Filter consists of micro strip line and C146-C153,C181 and C183.
During transmit, TXENB+ line from SYSTEM CONTROL UNIT is high level. Transistor TR109 turns on supply +9VT to the Class-A Amplifier and Pre-Driver, Automatic Power Control circuit and PIN diode Antenna Switch CD103, CD105-CD107 and CD109. When transmitting, the Antenna Switch diode is low impedance.

3, Frequency Synthesizer Circuit

The Frequency Synthesizer circuit receives PLL data, and control information from the microcomputer and from this generates the Tx / Rx RF frequencies.
It also provides frequency lock status to SYSTEM CONTROL UNIT. It consist of the Reference Oscillator, PLL Frequency Synthesizer chip IC305, Loop filter, Rx VCO TR307, Tx VCO TR304, Feedback Buffer Amplifier, and Dual-Modulus Prescaler IC306. Rx VCO and Tx VCO are locked to the Reference Oscillator by a single direct-divide synthesis loop consisting of the Feedback Buffer, Prescaler, and PLL Frequency Synthesizer chip.
The Tx VCO operates over a frequency range of 448-451MHz and 467.5-470.5MHz.
The Rx VCO operates over a frequency range of 426.4-429.4MHz.

3-1 Reference Oscillator

The reference oscillator consists of a 1.5-PPM TCXO (Temperature Controlled Compensated Crystal Oscillator). The standard reference oscillator frequency is 12.8MHz.

The TCXO is enclosed in a RF shielded can. The TCXO is compensated by internal temperature compensated circuit for both low and high temperature. With no additional compensated the oscillator will provide 1.5 PPM stability from -30°C to +60°C.

3-2 PLL Frequency Synthesizer chip

PLL Frequency Synthesizer chip IC305 contains a programmable reference oscillator divider (R), phase detector, and programmable VCO dividers (+N, A).

A fixed integer number to obtain a 6.25KHz or 5KHz channel reference for the synthesizer divides the reference frequency 12.8MHz from the reference oscillator.

PC PROGRAMMER can change this divide value.

The internal phase detector compares the output of the reference divider with the output of internal +N,A counter. The +N, A count counter receives as its input the VCO frequency divided by the Prescaler and programmed by the microcomputer.

This results in an error voltage when the phase differ and a constant output voltage when phase-detector input compare in frequency and phase.

If a phase error is detected, an error voltage is developed and applied to the VCO DC offset and loop filter to reset the VCO frequency. The count of the +N, A counters is controlled by the frequency data received on the SCK-, SDT- and PLLENB- line from SYSTEM CONTROL UNIT.

When a different channel is selected or when changing to the transmit or receive mode an error voltage is generated and appears at the phase-detector output, APD(IC305-2pin), causing the Phase Locked Loop to acquire the new frequency.

3-3 Loop filter

The Loop filter consists of R352 through R349 and C379, C380 and C378.

This filter controls the bandwidth and stability of the synthesizer loop.

When a different channel changing or changing to the transmit or receive mode, FET switch is controlled by PLLFST- for PLL lock up first (aplox 9mSEC).

The output of the filter is applied to the varicaps in the transmit and receive VCO's to adjust and maintain the VCO frequency. The use of to VCO's allows rapid independent selection of transmit and receive frequencies across the frequency split.

3-4 Rx VCO

The Rx VCO consists of FET oscillator TR307, and followed by high-gain buffer TR305. TR305 prevents external loading and provides power gain.

The VCO is a colpitts oscillator with the various varactors, capacitors and coil the tank circuit.

The VCO is switched on and off DPTT- line. When DPTT- is high, the Rx VCO is turned on, transistor TR307 and TR305 is on. The output of the Rx VCO after 2 times(through R302) is typically 0dBm. The output is applied to the feedback buffer for the VCO frequency control and as the Receiver frequency to Rx 1'st Mixer through the Local oscillator buffer amplifier. The VCO voltage need only be set once at some frequency of the band and split, after which it operates over the entire split with no additional tuning.

3-5 Tx VCO

The Tx VCO is basically the same as the Rx VCO. The VCO consists of FET oscillator TR304 followed by high-gain buffer amplifier TR303. When DPTT- is low, the Tx VCO is turned on, transistor TR303 and TR304 is on. The output of the Tx VCO after 2 times(through R301) is typically 0dBm.

3-6 Common Doubler

The common doubler consists of TR317. The common doubler does the oscillation frequency of the reception/transmission VCO 2 times.

3-7 Feedback Buffer Amplifier

The output of Rx VCO and Tx VCO, from transistor TR305 and TR303 respectively, are supplied to Feedback Buffer Amplifier IC301 and TR308. That drives the Dual-Modulus Prescaler IC306.

3-8 Dual-Modulus Prescaler

The Dual-Modulus Prescaler completes the Phase Lock Loop(PLL) feedback path from the PLL Frequency synthesizer chip to the Loop Filter, to the VCO's and Feedback Buffers and then back to the PLL Frequency synthesizer chip through the Prescaler.

The Prescaler divides the VCO by 64 or 65 under control of MC(IC306-6pin) from the PLL Frequency synthesizer chip. The output of the Prescaler is applied to the PLL Frequency synthesizer chip where it is divided down 5KHz or 6.25KHz by and internal +N, A counter and compared in frequency and phase with the divided-down frequency for the Reference Oscillator. The result of this comparison is the error voltage used to maintain frequency lock. The +N, A counter is controlled by data received from the SYSTEM CONTROL UNIT. Depending on the operating frequency, the DC voltage at Test Point TP301 should be within 1.5 to 6.5 Vdc when the PLL is locked.

3-9 Lock Detect

The Lock Detect circuit consists of transistor TR310 and CD323.

If a large frequency error exists, the LD (IC305-14pin) positive lead from the PLL Frequency synthesizer chip will carry negative spikes to the SYSTEM CONTROL UNIT. When unlock ,PLLLOCK+ is low.

3-10 Loop Modulation Circuit

The Loop Modulation Circuit consists of IC303. Tx audio is integrated about fc= 0.15Hz for Loop Modulation. That signal is summed with the APD (IC305-2pin).