

Compact Flash CardMin.16MB ~ Max.512MB, ATA/IDE Interface Mode,Support 3 power save mode, 3.3V/5.0V OperatingPart No. CFCxxxSx

# **1.PRODUCT OVERVIEW**

## **GENERAL DESCRIPTION**

The CFCxxxSx series CompactFlash<sup>™</sup> card is a flash technology based with ATA interface flash memory card. It is constructed with flash disk controller chip and NAND-type (Samsung) flash memory device. The CompactFlash<sup>™</sup> card operates in both 3.3-Volt and 5.0-Volt power supplies. It comes in capacity of 16, 32, 64, 96, 128, 192, 256, 384 MB and up to 512 MB formatted for type-I card.

By optimizing flash memory management, the life of this card can be extended to its maximum level. Because the ECC function is included, the correctness of data transfer between the card and the mobile device can be guaranteed. The power down and sleep modes of the card can ensure longer life of the batteries in the mobile devices. It is a perfect choice of solid-state mass-storage cards for battery backup handheld devices such as Digital Camera, Audio Player, PDA, GPS, or the applications which require high environment tolerance with high performance sustained write speed.

# **FEATURES**

- ATA / True IDE compatible host interface
- ATA command set compatible
- Very high performance, very low power consumption
- Automatic error correction
- Support 3 power save mode : stop/idle/active
- Support for CIS implemented with 256 bytes of attribute memory
- Support for 8 or 16 bit host transfers
- 3.3V/5.0V operation voltage
- Host data transfer rate : 20MB/s
- Flash data transfer rate : 10MB/s
- Host Interface bus width : 8/16 bit Access
- Flash Interface bus width : 8 bit Access
- Capacity : Min. 16MB ~ Max. 512MB
- MTBF : 1,000,000 hours, minimum 30,000 insertions
- Operating vibration : 15G peak to peak maximum
- Operating shock : 1,000G maximum

## **PRODUCT SPECIFICATIONS**

**Capacities :** 

16, 32, 48, 64, 96, 128, 192, 256, 384 and up to 512 MB (formatted)

#### System Compatibility :

Please refer to the compatibility list of index.

#### **Performance :**

| Data Transfer Rates :  | up to 4.2 MB/s in ATA PIO mode 4 |
|------------------------|----------------------------------|
| To/from Flash memory : | up to 12.4 MB/s                  |
| To/from host :         | up to 20MB/s                     |
| Sustained write :      | up to 2.9MB/s in ATA PIO mode 4  |
| Sustained read :       | up to 5.62MB/s in ATA PIO mode 4 |

**Operating Voltage :**  $3.3V / 5.0V \pm 10\%$ 

#### **Power consumption :**

| Read mode  | 30 mA (typ), 40 mA (Max) |
|------------|--------------------------|
| Write mode | 30 mA (typ), 40 mA (Max) |
| Stop mode  | 30 µA (typ)              |

#### **Environment conditions :**

| Operating temperature | $0^{\circ}$ C to + $65^{\circ}$ C    |
|-----------------------|--------------------------------------|
| Storage temperature   | - $20^{\circ}$ C to + $70^{\circ}$ C |
| Relative humidity     | 95%(Max)                             |

#### **Dimension :**

| Weight    | Capacity dependent   |
|-----------|--|
| Length    | $36.4 \pm 0.15 \text{ mm} (1.433 \pm 0.006 \text{ in.})$           |
| Width     | $42.8 \pm 0.10 \text{ mm} (1.685 \pm 0.004 \text{ in.})$           |
| Thickness | $3.3 \text{ mm} \pm 0.10 \text{ mm} (0.130 \pm 0.004 \text{ in.})$ |

# HANBit ELECTRICAL SPECIFICATIONS

| Symbol           | Parameter           | Ratings        | Unit |
|------------------|---------------------|----------------|------|
| V <sub>DD</sub>  | Supply voltage      | - 0.3 to + 7.0 | V    |
| V <sub>IN</sub>  | Input voltage       | - 0.3 to + 7.0 | V    |
| I <sub>IN</sub>  | DC input current    | - 10           | mA   |
| T <sub>STG</sub> | Storage temperature | - 20 to + 85   | °C   |

#### **Table 1.1 Absolute Maximum Ratings**

#### **Table 1.2 Recommended Operating Conditions**

| Symbol          | Parameter          |      | Ratings      | Unit |
|-----------------|--------------------|------|--------------|------|
| V               | DC Symply yeltere  | 5V   | 4.75 to 5.25 | V    |
| V <sub>DD</sub> | DC Supply voltage  | 3.3V | 3.0 to 3.6   | V    |
| Ta              | Storage temperatur | re   | - 20 to +70  | °C   |

#### Table 1.3 DC Characteristics

# (Ta=0°C to 70°C, V<sub>DD</sub>=3.0 to 5.3V) Symbol Parameter

| Symbol          | Parameter                 | Min. | Тур. | Max. | Unit |
|-----------------|---------------------------|------|------|------|------|
| I <sub>DD</sub> | Operating Current         |      | 30   | 70   | mA   |
| I <sub>ds</sub> | Stop Current              |      | 50   | 150  | μΑ   |
| V <sub>DD</sub> | High Level Output Voltage | 2.4  |      |      | V    |
| V <sub>DD</sub> | Low Level Output Voltage  |      |      | 0.4  | V    |

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Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

#### Figure 1.1 Type I CompactFlash Storage Card Dimensions

# HANBit Electrical Interface

#### **Physical Description**

The host is connected to the CompactFlash Storage Card or CF+ Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

#### Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 4. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Section 4.3 defines the DC characteristics for all input and output type structures.

#### **Electrical Description**

The CompactFlash Storage Card functions in three basic modes:

- 1) PC Card ATA using I/O Mode
- 2) PC Card ATA using Memory Mode
- 3) True IDE Mode

Which is compatible with most disk drives. CompactFlash Storage Cards are required to support all three modes. The CF Cards normally function in the first and second modes, however they can optionally function in True IDE mode. The configuration of the CompactFlash Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the storage card or for True IDE Mode, pin 9 being grounded. The configuration of the CF Card will be controlled using configuration registers starting at the address defined in the configuration Tuple (CISTPL\_CONFIG) in the Attribute Memory space of the CF Card.

Signal description describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash Storage Card sources are outputs. The CompactFlash Storage Card logic levels conform to those specified in the PCMCIA Release 2.1 specification. Each signal has three possible operating modes:

- 1) PC Card Memory mode
- 2) PC Card I/O mode
- 3) True IDE

True IDE mode is required for CompactFlash Storage cards. All outputs from the card are totem pole except the data bus signals that are bi-directional tri-state.

# **2.PIN INFORMATION**

# HANBit PIN ASSIGNMENTS AND PIN TYPE

#### Table 2.1 Pin Assignment and Pin type

| PC Card Memory Mode |                  | PC Card I/O Mode |          |     |                  | True IDE Mode |          |     |                  |             |          |
|---------------------|------------------|------------------|----------|-----|------------------|---------------|----------|-----|------------------|-------------|----------|
| Pin                 | Signal           | Pin<br>Type      | Function | Pin | Signal           | Pin<br>Type   | Function | Pin | Signal           | Pin<br>Type | Function |
| 1                   | GND              | DC               | Ground   | 1   | GND              | DC            | Ground   | 1   | GND              | DC          | Ground   |
| 2                   | D03              | I/O              | I1Z, OZ3 | 2   | D03              | I/O           | I1Z, OZ3 | 2   | D03              | I/O         | I1Z, OZ3 |
| 3                   | D04              | I/O              | I1Z, OZ3 | 3   | D04              | I/O           | I1Z, OZ3 | 3   | D04              | I/O         | I1Z, OZ3 |
| 4                   | D05              | I/O              | I1Z, OZ3 | 4   | D05              | I/O           | I1Z, OZ3 | 4   | D05              | I/O         | I1Z, OZ3 |
| 5                   | D06              | I/O              | I1Z, OZ3 | 5   | D06              | I/O           | I1Z, OZ3 | 5   | D06              | I/O         | I1Z, OZ3 |
| 6                   | D07              | I/O              | I1Z, OZ3 | 6   | D07              | I/O           | I1Z, OZ3 | 6   | D07              | I/O         | I1Z, OZ3 |
| 7                   | -CE1             | Ι                | I3U      | 7   | -CE1             | Ι             | I3U      | 7   | -CS0             | Ι           | I3U      |
| 8                   | A10              | Ι                | I1Z      | 8   | A10              | Ι             | I1Z      | 8   | A10              | Ι           | I1Z      |
| 9                   | -OE              | Ι                | I3U      | 9   | -OE              | Ι             | I3U      | 9   | -ATA SEL         | Ι           | I3U      |
| 10                  | A09              | Ι                | I1Z      | 10  | A09              | Ι             | I1Z      | 10  | A09 <sup>2</sup> | Ι           | I1Z      |
| 11                  | A08              | Ι                | I1Z      | 11  | A08              | Ι             | I1Z      | 11  | $A08^2$          | Ι           | I1Z      |
| 12                  | A07              | Ι                | I1Z      | 12  | A07              | Ι             | I1Z      | 12  | A07 <sup>2</sup> | Ι           | I1Z      |
| 13                  | VCC              | DC               | Power    | 13  | VCC              | DC            | Power    | 13  | VCC              | DC          | Power    |
| 14                  | A06              | Ι                | I1Z      | 14  | A06              | Ι             | I1Z      | 14  | $A06^2$          | Ι           | I1Z      |
| 15                  | A05              | Ι                | I1Z      | 15  | A05              | Ι             | I1Z      | 15  | A05 <sup>2</sup> | Ι           | I1Z      |
| 16                  | A04              | Ι                | I1Z      | 16  | A04              | Ι             | I1Z      | 16  | $A04^2$          | Ι           | I1Z      |
| 17                  | A03              | Ι                | I1Z      | 17  | A03              | Ι             | I1Z      | 17  | A03 <sup>2</sup> | Ι           | IIZ      |
| 18                  | A02              | Ι                | I1Z      | 18  | A02              | Ι             | I1Z      | 18  | A02              | Ι           | IIZ      |
| 19                  | A01              | Ι                | I1Z      | 19  | A01              | Ι             | I1Z      | 19  | A01              | Ι           | IIZ      |
| 20                  | A00              | Ι                | I1Z      | 20  | A00              | Ι             | I1Z      | 20  | A00              | Ι           | I1Z      |
| 21                  | D00              | I/O              | I1Z, OZ3 | 21  | D00              | I/O           | I1Z, OZ3 | 21  | D00              | I/O         | I1Z, OZ3 |
| 22                  | D01              | I/O              | I1Z, OZ3 | 22  | D01              | I/O           | I1Z, OZ3 | 22  | D01              | I/O         | I1Z, OZ3 |
| 23                  | D02              | I/O              | I1Z, OZ3 | 23  | D02              | I/O           | I1Z, OZ3 | 23  | D02              | I/O         | I1Z, OZ3 |
| 24                  | WP               | 0                | OT3      | 24  | -IOIS16          | 0             | OT3      | 24  | -IOIS16          | 0           | OT3      |
| 25                  | -CD2             | 0                | Ground   | 25  | -CD2             | 0             | Ground   | 25  | -CD2             | 0           | Ground   |
| 26                  | -CD1             | 0                | Ground   | 26  | -CD1             | 0             | Ground   | 26  | -CD1             | 0           | Ground   |
| 27                  | D11 <sup>1</sup> | I/O              | I1Z, OZ3 | 27  | D11 <sup>1</sup> | I/O           | I1Z, OZ3 | 27  | $D11^1$          | I/O         | I1Z, OZ3 |
| 28                  | D12 <sup>1</sup> | I/O              | I1Z, OZ3 | 28  | D12 <sup>1</sup> | I/O           | I1Z, OZ3 | 28  | $D12^1$          | I/O         | I1Z, OZ3 |
| 29                  | D13 <sup>1</sup> | I/O              | I1Z, OZ3 | 29  | D13 <sup>1</sup> | I/O           | I1Z, OZ3 | 29  | D13 <sup>1</sup> | I/O         | I1Z, OZ3 |
| 30                  | D14 <sup>1</sup> | I/O              | I1Z, OZ3 | 30  | D14 <sup>1</sup> | I/O           | I1Z, OZ3 | 30  | $D14^1$          | I/O         | I1Z, OZ3 |
| 31                  | D15 <sup>1</sup> | I/O              | I1Z, OZ3 | 31  | D15 <sup>1</sup> | I/O           | I1Z, OZ3 | 31  | D15 <sup>1</sup> | I/O         | I1Z, OZ3 |
| 32                  | $-CE2^1$         | Ι                | I3U      | 32  | $-CE2^1$         | Ι             | I3U      | 32  | $-CS1^1$         | Ι           | I3U      |
| 33                  | -VS1             | 0                | Ground   | 33  | -VS1             | 0             | Ground   | 33  | -VS1             | 0           | Ground   |
| 34                  | -IORD            | Ι                | I3U      | 34  | -IORD            | Ι             | I3U      | 34  | -IORD            | Ι           | I3U      |
| 35                  | -IOWR            | Ι                | I3U      | 35  | -IOWR            | Ι             | I3U      | 35  | -IOWR            | Ι           | I3U      |
| 36                  | -WE              | Ι                | I3U      | 36  | -WE              | Ι             | I3U      | 36  | $-WE^3$          | Ι           | I3U      |

| PC Card Memory Mode |                  |             | PC Card I/O Mode |     |         |             | True IDE Mode |     |                   |             |          |
|---------------------|------------------|-------------|------------------|-----|---------|-------------|---------------|-----|-------------------|-------------|----------|
| Pin                 | Signal           | Pin<br>Type | Function         | Pin | Signal  | Pin<br>Type | Function      | Pin | Signal            | Pin<br>Type | Function |
| 37                  | RDY/BSY          | 0           | OT1              | 37  | IREQ    | 0           | OT1           | 37  | INTRQ             | 0           | OZ1      |
| 38                  | VCC              | DC          | Power            | 38  | VCC     | DC          | Power         | 38  | VCC               | DC          | Power    |
| 39                  | -CSEL            | Ι           | I2Z              | 39  | -CSEL   | Ι           | I2Z           | 39  | -CSEL             | Ι           | I2U      |
| 40                  | -VS2             | 0           | Open             | 40  | -VS2    | 0           | Open          | 40  | -VS2              | 0           | Open     |
| 41                  | RESET            | Ι           | I2Z              | 41  | RESET   | Ι           | I2Z           | 41  | -RESET            | Ι           | I2Z      |
| 42                  | -WAIT            | 0           | OT1              | 42  | -WAIT   | 0           | OT1           | 42  | IORDY             | 0           | ON1      |
| 43                  | -INPACK          | 0           | OT1              | 43  | -INPACK | 0           | OT1           | 43  | -INPACK           | 0           | OZ1      |
| 44                  | -REG             | Ι           | I3U              | 44  | -REG    | Ι           | I3U           | 44  | -REG <sup>3</sup> | Ι           | I3U      |
| 45                  | BVD2             | I/O         | I1U, OT1         | 45  | -SPKR   | I/O         | I1U, OT1      | 45  | -DASP             | I/O         | IIU, ON1 |
| 46                  | BVD1             | I/O         | I1U, OT1         | 46  | -STSCHG | I/O         | IIU, OT1      | 46  | -PDIAG            | I/O         | IIU, ON1 |
| 47                  | $D08^1$          | I/O         | I1Z, OZ3         | 47  | $D08^1$ | I/O         | I1Z, OZ3      | 47  | $D08^1$           | I/O         | I1Z, OZ3 |
| 48                  | D09 <sup>1</sup> | I/O         | I1Z, OZ3         | 48  | $D09^1$ | I/O         | I1Z, OZ3      | 48  | D09 <sup>1</sup>  | I/O         | I1Z, OZ3 |
| 49                  | $D10^1$          | I/O         | I1Z, OZ3         | 49  | $D10^1$ | I/O         | I1Z, OZ3      | 49  | $D10^1$           | I/O         | I1Z, OZ3 |
| 50                  | GND              | DC          | Ground           | 50  | GND     | DC          | Ground        | 50  | GND               | DC          | Ground   |

Note: 1. These signals are required only for 16bit access and not required when

installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.

- 2. Should be grounded by the host.
- 3. Should be tied to VCC by the host.
- 4. Optional required for PCMCIA Storage Cards.

## **Signal Descriptions**

#### Table 2.2 Signal Descriptions

| Signal Name                           | Dir.     | Pin       | Description  |
|---------------------------------------|----------|-----------|--|
| A10 - A0                              | Ι        | 8,10,11,1 | These address lines along with the -REG signal are used to select the  |
| (PC Card Memory Mode)                 |          | 2,14,15,1 | following: The I/O port address registers within the CompactFlash Storage  |
|                                       |          | 6,        | Card or CF+ Card, the memory mapped port address registers within the  |
|                                       |          | 17,18,    | CompactFlash Storage Card or CF+ Card, a byte in the card's information  |
| A10, A0                               |          | 19,20     | structure and its configuration control and status registers.  |
| AIV - AV<br>(PC Card I/O Mode)        |          |           | This signal is the same as the PC Card Memory Mode signal  |
|                                       |          | 10.10     | This signal is the same as the i C Cara meniory mode signal.   |
| A2 - A0                               | Ι        | 18,19,    | In True IDE Mode only A[2:0] are used to select the one of eight registers in                                    |
| (True IDE Mode)                       | Ĺ        | 20        | the Task File, the remaining address lines should be grounded by the host.                                       |
| BVD1                                  | I/O      | 46        | This signal is asserted high as BVD1 is not supported.   |
| (PC Card Memory Mode)                 |          |           |  |
|                                       |          |           |  |
| -STSCHG                               |          |           | This signal is asserted low to alert the host to changes in the RDY/-BSY and                                     |
| (PC Card I/O Mode)                    |          |           | Write Protect states, while the I/O interface is configured. Its use is  |
| Status Changed                        |          |           | controlled by the Card Config and Status Register.   |
|                                       |          |           | In the True IDE Mode, this is not four the first of the D  |
| -rua DE Mada)                         |          |           | In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol |
| (True IDE MOde)<br>BVD2               |          |           | iviasiei / Stave Hallusliake protocol.<br>This signal is assarted high as RVD2 is not supported.                 |
| (PC Card Memory Mode)                 | [/O      | 45        | i nis signal is assented night as D v D2 is not supported.   |
|                                       |          |           |  |
| -SPKR                                 |          |           | This line is the Binary Audio output from the card. If the Card does not   |
| (PC Card I/O Mode)                    |          |           | support the Binary Audio function, this line should be held negated.   |
| , , , , , , , , , , , , , , , , , , , |          |           |  |
| -DASP                                 |          |           | In the True IDE Mode, this input/output is the Disk Active/Slave Present   |
| (True IDE Mode)                       | <b> </b> | ļ         | signal in the Master/Slave handshake protocol.   |
| -CD1, -CD2                            | 0        | 26,25     | These Card Detect pins are connected to ground on the CompactFlash   |
| (PC Card Memory Mode)                 |          |           | Storage Card or CF+ Card. They are used by the host to determine that the  |
|                                       |          |           | CompactFlash Storage Card or CF+ Card is fully inserted into its socket.   |
|                                       |          |           | This signal is the same for all modes  |
| -CD1CD2                               |          |           | This signal is the same for all moues.   |
| (PC Card I/O Mode)                    |          |           |  |
|                                       |          |           | This signal is the same for all modes.   |
| -CD1, -CD2                            |          |           |  |
| (True IDE Mode)                       |          |           |  |
| -CE1, -CE2                            | Ι        | 7,32      | These input signals are used both to select the card and to indicate to the                                      |
| (PC Card Memory Mode)                 |          |           | card whether a byte or a word operation is being performedCE2 always   |
| Card Enable                           |          |           | accesses the odd byte of the word. –CE1 accesses the even byte or the Odd  |
|                                       |          |           | byte of the word depending on A0 and -CE2. A multiplexing scheme based   |
| CE1 CE2                               |          |           | on AU, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.  |
| -CEI, -CE2<br>(PC Card I/O Mode)      |          |           | This signal is the same as the DC Card Momery Mode signal  |
| Card Enable                           |          |           | This signal is the same as the i C Calu Memory Moue Signal.  |
| Sand Lindle                           |          |           | In the True IDE Mode CS0 is the chip select for the task file registers while                                    |
| -CS0, -CS1                            |          |           | CS2 is used to select the Alternate Status Register and the Device Control                                       |
| (True IDE Mode)                       |          |           | Register.  |
| Signal Name                           | Dir      | . Pin     | Description  |
| CSEL                                  | т        | 30        | This signal is not used for this mode.   |
| (PC Card Memory Mode)                 |          | 37        |  |
|                                       |          |           |  |
| CSEL                                  |          |           | This signal is not used for this mode.   |
| PC Card I/O Mode)                     |          |           |  |
| CSEI                                  |          |           | This internally pulled up signal is used to configure this device as a Master                                    |
| CATEL                                 |          |           | - I THIS INCLUARLY DURED UD SIGNAL IS USED TO CONTIGUE HUS DEVICE AS A MASTER                                    |

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| (True IDE Mode)                |      |        | or a Slave when configured in the True IDE Mode.                                 |
|--------------------------------|------|--------|--|
|                                |      |        | When this pin is grounded, this device is configured as a Master.                |
|                                |      |        | When the pin is open, this device is configured as a Slave.                      |
| D15 - D00                      | I/O  | 31,30, | These lines carry the Data, Commands and Status information between the          |
| (PC Card Memory Mode)          | 1/ 0 | 29,28, | host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is     |
|                                |      | 27,49, | the LSB of the Odd Byte of the Word.   |
|                                |      | 48,47, |  |
| D15 - D00                      |      | 6,5,4, | This signal is the same as the PC Card Memory Mode signal.                       |
| (PC Card I/O Mode)             |      | 3,2,   |  |
|                                |      | 23,22, |  |
| D15 - D00                      |      | 21     | In True IDE Mode, all Task File operations occur in byte mode on the low         |
| (True IDE Mode)                |      |        | order bus D00-D07 while all data transfers are 16 bit using D00-D15.             |
| GND                            |      | 1,50   | Ground.  |
| (PC Card Memory Mode)          |      |        |  |
| CND                            |      |        |  |
| GND<br>(DC Card L/O Mada)      |      |        | This signal is the same for all modes.   |
| (PC Card I/O Mode)             |      |        | This signal is the same for all modes  |
| (True IDE Mode)                |      |        | This signal is the same for all modes.   |
|                                | 0    | 10     | This signal is not used in this mode   |
| (PC Card Memory Mode)          | 0    | 43     | This signal is not used in this mode.  |
| (Te card Memory Mode)          |      |        |  |
| -INPACK                        |      |        | The Input Acknowledge signal is asserted by the CompactFlash Storage             |
| (PC Card I/O Mode)             |      |        | Card or CF+ Card when the card is selected and responding to an I/O read         |
| Input Acknowledge              |      |        | cycle at the address that is on the address bus. This signal is used by the      |
|                                |      |        | host to control the enable of any input data buffers between the                 |
|                                |      |        | CompactFlash Storage Card or CF+ Card and the CPU.                               |
|                                |      |        |  |
| -INPACK                        |      |        | In True IDE Mode this output signal is not used and should not be                |
| (True IDE Mode)                |      |        | connected at the host.   |
| -IORD                          | Ι    | 34     | This signal is not used in this mode.  |
| (PC Card Memory Mode)          |      |        |  |
|                                |      |        |  |
| -IORD                          |      |        | This is an I/O Read strobe generated by the host. This signal gates I/O data     |
| (PC Card I/O Mode)             |      |        | onto the bus from the CompactFlash Storage Card or CF+ Card when the card        |
|                                |      |        | is configured to use the I/O interface.  |
| IOND                           |      |        |  |
| -IOKD                          |      |        | Card I/O Mode  |
|                                |      |        | Card I/O Mode.   |
| -IOWR<br>(BC Card Mamory Mode) | Ι    | 35     | i nis signal is not used in this mode.   |
| (FC Card Memory Mode)          |      |        |  |
| JOWR                           |      |        | The I/O Write strobe pulse is used to clock I/O data on the Card Data bus        |
| (PC Card I/O Mode)             |      |        | into the CompactFlash Storage Card or CF+ Card controller registers when         |
| (i e cara i o mode)            |      |        | the CompactFlash Storage Card or CF+ Card is configured to use the I/O           |
|                                |      |        | interface. The clocking will occur on the negative to positive edge of the       |
|                                |      |        | signal (trailing edge).  |
|                                |      |        |  |
|                                |      |        | In True IDE Mode, this signal has the same function as in PC Card I/O Mode.      |
| -IOWR                          |      |        |  |
| (True IDE Mode)                |      |        |  |
| Signal Name                    | Dir. | Pin    | Description  |
| OF                             | _    | c.     | This is an Output Enable stroke generated by the host interface. It is used to   |
| (PC Card Memory Mode)          | I    | 9      | read data from the CompactElash Storage Card or $CE_{\perp}$ Card in Memory Mode |
|                                |      |        | and to read the CIS and configuration registers                                  |
|                                |      |        | and to read the C15 and configuration registers.                                 |
| -OE                            |      |        | In PC Card I/O Mode, this signal is used to read the CIS and configuration       |
| (PC Card I/O Mode)             |      |        | registers.   |

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| -ATA SEL<br>(True IDE Mode)                              |      |       | To enable True IDE Mode this input should be grounded by the host.   |
|--|------|-------|--|
| RDY/-BSY<br>(PC Card Memory Mode)                        | 0    | 37    | In Memory Mode this signal is set high when the CompactFlash Storage<br>Card or CF+ Card is ready to accept a new data transfer operation and held<br>low when the card is busy. The Host memory card socket must provide a<br>pull-up resistor.<br>At power up and at Reset, the RDY/-BSY signal is held low(busy) until the<br>CompactFlash Storage Card or CF+ Card has completed its power up or reset<br>function. No access of any type should be made to the CompactFlash<br>Storage Card or CF+ Card during this time. The RDY/-BSY signal is held high<br>(disabled from being busy) whenever the following condition is true: The<br>CompactFlash Storage Card or CF+ Card has been powered up with +RESET<br>continuously disconnected or asserted. |
| -IREQ<br>( PC Card I/O Mode)                             |      |       | I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.  |
| INTRQ<br>(True IDE Mode)                                 |      |       | In True IDE Mode signal is the active high Interrupt Request to the host.  |
| -REG<br>(PC Card Memory mode)<br>Attribute Memory Select | Ι    | 44    | This signal is used during Memory Cycles to distinguish between Common<br>Memory and Register (Attribute) Memory accesses. High for Common<br>Memory, Low for Attribute Memory.  |
| -REG<br>(PC Card I/O Mode)                               |      |       | The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.   |
| -REG<br>(True IDE Mode)                                  |      |       | In True IDE Mode this input signal is not used and should be connected to VCC by the host.   |
| RESET<br>(PC Card Memory Mode)                           | Ι    | 41    | When the pin is high, this signal Resets the CompactFlash Storage Card or CF+ Card. The CompactFlash Storage Card or CF+ Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.  |
| RESET<br>(PC Card I/O Mode)                              |      |       | This signal is the same as the PC Card Memory Mode signal.   |
| -RESET<br>(True IDE Mode)                                |      |       | In the True IDE Mode this input pin is the active low hardware reset from the host.  |
| VCC<br>(PC Card Memory Mode)                             |      | 13,38 | +5 V, +3.3 V power.  |
| VCC<br>(PC Card I/O Mode)                                |      |       | This signal is the same for all modes.   |
| VCC<br>(True IDE Mode)                                   |      |       | This signal is the same for all modes.   |
| Signal Name  | Dir. | Pin   | Description  |
| -VS1<br>-VS2<br>(PC Card Memory Mode)                    | 0    | 33,40 | Voltage Sense SignalsVS1 is grounded so that the CompactFlash Storage<br>Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by<br>PCMCIA for a secondary voltage.  |
| -VS1<br>-VS2   |      |       | This signal is the same for all modes.   |

|                       | I              |    |   |
|-----------------------|----------------|----|---|
| (PC Card I/O Mode)    |                |    |   |
| 1/01                  |                |    | This signal is the same for all modes   |
| -VSI                  |                |    | This signal is the same for all modes.  |
|                       |                |    |   |
| (True IDE Mode)       |                |    |   |
| -WAIT                 | 0              | 42 | The -WAIT signal is driven low by the CompactFlash Storage                        |
| (PC Card Memory Mode) |                |    | Card or CF+ Card to signal the host to delay completion of a                      |
|                       |                |    | memory or I/O cycle that is in progress.  |
| -WAIT                 |                |    |   |
| (PC Card I/O Mode)    |                |    | This signal is the same as the PC Card Memory Mode signal.                        |
|                       |                |    |   |
| IORDY                 |                |    | In True IDE Mode this output signal may be used as IORDY.                         |
| (True IDE Mode)       |                |    |   |
| -WE                   | Τ <sub>Ι</sub> | 36 | This is a signal driven by the host and used for strobing memory write data to    |
| (PC Card Memory Mode) | · ·            | 20 | the registers of the CompactFlash Storage Card or CF+ Card when the card is       |
|                       |                |    | configured in the memory interface mode. It is also used for writing the          |
|                       |                |    | configuration registers.  |
|                       |                |    |   |
| -WE                   |                |    | In PC Card I/O Mode, this signal is used for writing the configuration            |
| (PC Card I/O Mode)    |                |    | registers.  |
|                       |                |    |   |
| -WE                   |                |    | In True IDE Mode this input signal is not used and should be                      |
| (True IDE Mode)       |                |    | connected to VCC by the host.   |
| WP                    |                | 24 | Memory Mode - The CompactFlash Storage Card or CF+ Card does not have             |
| (PC Card Memory Mode) | 0              | 24 | a write protect switch. This signal is held low after the completion of the reset |
| Write Protect         |                |    | initialization sequence   |
| white Protect         |                |    | initialization sequence.  |
| -IOIS16               |                |    | 1/O Operation - When the CompactFlash Storage Card or CF+ Card is                 |
| (PC Card I/O Mode)    |                |    | configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port  |
| (Te cura i o mode)    |                |    | (-IOIS16) function A Low signal indicates that a 16 bit or odd byte only          |
|                       |                |    | operation can be performed at the addressed port                                  |
|                       |                |    | operation can be performed at the addressed port.                                 |
| -101816               |                |    | In True IDF Mode this output signal is asserted low when this                     |
| (True IDE Mode)       |                |    | device is expecting a word data transfer cycle                                    |
|                       |                |    | device is expecting a word data transfer eyele.                                   |