DATA RADIO MANUAL

HLD-100V2

SPECIFICATIONS

GENERAL

Equipment Type……Data radio

Band……VHF

Channel Spacings……..25kHz, 12.5kHz programmable

RF Output Power……...5/1 watt

Modulation Type……....F3D, D3E

Intermediate Frequency……...45.1MHz & 455KHz

Number of Channels……16

Frequency Source……..Synthesizer

Power Supply……...Power Supply (12 VDC Nominal Voltage)

Temperature Range

Storage……..from -40□ to + 80□

Operating……..from -30□ to + 60□

Current Consumption

Standby (Muted)……..< 65mA

Transmit 5 Watts RF Power……..< 2.0A

Transmit 1 Watts RF Power……..< 1.0A

Frequency Bands

		RX	TX
VHF	V2	148.000 – 174.000 MHz	148.000 – 174.000 MHz

TRANSMITTER

	Nom.	Max	Min
Carrier Power			
Hi	5W	< 6W	> 4.5W
Low	1W	< 1.5W	> 0.8W

Sustained Transmission……..Nominal conditions

Time :	5	10	30 Sec.
Power :	>90%	>85%	>80%

Frequency……< 0.5 kHz Nominal condition for VHF
±5.0 ppm Extreme condition for VHF

Frequency Deviation

25 kHz Channel Spacing……..Peak ±5.0, Min. ±3.8

12.5 kHz Channel Spacing……Peak ±2.5, Min. ±1.9

Audio Frequency Response……Within+1/-3dB of 6dB octave
@ 300 Hz to 2.55 kHz for 12.5 kHz C.S
@ 300 Hz to 3.0 kHz for 25 kHz C.S

Adjacent Channel Power

25 kHz……< 70 dBc @ Nominal Condition
< 65 dBc @ Extreme Condition

12.5 kHz……< 60 dBc @ Nominal Condition
< 55 dBc @ Extreme Condition

Conducted Spurious Emission……..< -57 dBc

Modulation Sensitivity……..100mV RMS @60% Peak Dev.

Hum & Noise :

25 kHz Channel Spacing……> 40 dB

12.5 kHz Channel Spacing……> 34 dB

Modulation Symmetry……..< 10% Peak Dev @ 1kHz input for nominal dev +20dB

Load Stability……No osc at ≥ 10:1 VSWR all phase angles and suitable antenna
No destroy at ≥ 20:1 all phase angle

Peak Deviation Range Adjustment @ kHz, Nom. Dev +20dB :

25 kHz Channel Spacing……..…..> Min. 3.5, Max. 6.0

12.5 kHz Channel Spacing……..……> Min. 1.5, Max. 4.0

RECEIVER

Sensitivity (12dB Sinad),…….. VHF<-118dBm @ Nom. Condition
VHF<-116dBm @ Extreme Condition

Amplitude Characteristic……...< ±3dB

Adjacent Channel Selectivity :

25 kHz Channel Spacing……..> 60dB @ Nom., > 55dB @ Extreme Condition

12.5 kHz Channel Spacing…….……> 50dB @ Nom., > 45dB @ Extreme Condition

Spurious Response Rejection……..70dB (100kHz-4 GHz)

Image Response……> 70

IF Response……> 70

Others……..…> 70

Intermodulation Response Rejection :

±25 kHz / 50 kHz……..65 dB

±50 kHz / 100 kHz……65 dB

Conducted Spurious Emission @ Nominal Conditions :

9 kHz – 1 GHz……...> -57 dBm

1 GHz – 4 GHz……..> -47 dBm

Rx Spurious Emissions (Radiated) @ Nominal Conditions

9 kHz – 1 GHz……> -57 dBm

1 GHz – 12.75 GHz…….……..> -47 dBm

AF Distortion……..5% @ Nom., < 10% @ Extreme condition

Rx Hum & Noise :

25.0 kHz CP……< 40 dB No PSOPH

12.5 kHz CP……< 35 dB with PSOPH

Receiver Response Time……< 16 mS

Squelch Opening Range……..RF level for 6 to 14 dB Sinad

Squelch Closing Range (Hysteresis):…… 0-6 dB Sinad @ Nominal Condition

Squelch Decay Time :

Rf Level at Threshold……..< 40mS

Rf Level at Threshold + 20dB……< 30mS

Squelch Decay Time…….5 mS Min., 20mS Max.

Antenna Socket Input Match……..> 10dB Return Loss

L.O.Frequency Temperature Stability……..1st <5 ppm, 2nd <15 ppm from -30□ to 60□

L.O.Frequency Aging Rate……..±2ppm/yeat

REFERENCY CRYSTAL

Frequency……14.4 MHz

Holder Type……..HC-18

Temperature Characteristic…….±5.0 ppm from -30□ to 60□

Aging Rate…….< 2 ppm /year in 1st year
< 1 ppm/ year thereafter

Lock time…….< 10mS

TX to RX…….< 20 (No Power Saving)

RX to TX…….< 20

INTRODUCTION

The HEADLINE HLD-100 Series of Rf Link Modules from HEADLINE utilizes the latest technology in its design and manufacturing.
Both the UHF and VHF models are PLL (Phase Lock Loop Synthesizer)/microprocessor controlled. And offer one to five Watts of power with 16 channel capability. Multiple functions Including 1200 to 9600 baud rates. AC and / or DC audio Coupling. GMSK and FSK modulation are standard in these Fully programmable wide bandwidth RF Link Module units.
The radio is programmed using a IBM^{R} Personal Computer, DOS^{R} based software, an interface module and a programming Cable. This allows the radio to be tailored to meet the Requirements of the individual user and the System(s) it is Operating within.

FEATURES

- Busy Channel Lockout
- 16 Channels
- TX Time-out
- Power Save
- 1/5 Watt Programmable Output
- 12.5 / 25 kHz Programmable Channel Spacing

Busy Channel Lockout

The Busy Channel Lockout feature, when enabled, disables the transmitter when the receiving channel is busy and the user attempts to transmit.

16 Channels

The HLD-100V2 Series radio can store up to 16 channels within the same band.

TX TIME-OUT

The TX Time-out feature, when enabled, limits the amount of Time that the user can continuously transmit. This time can be Set in increments of 10 seconds from 10 seconds to 990 second.

Power Save

The Power Save feature is used when an external battery is used as the power source. When Power Save is enabled, the receiver “ON” and “OFF” time can be programmed into the radio and allows the operator to set the length of time the receiver is asleep.

FCC and Industry Canada Warning Statement

According to the FCC and IC rules governing maximum permissible exposure to radio frequency radiation; all users must stay within a minimum of 0.5 meter of the device during operation and device shall be mounted in such a way that non-user persons will not inadvertently encroach that radius.

THEORY OF OPERATION
INTRODUCTION
DIGITAL CIRCUITS
RF CIRCUITS
RF CIRCUITS PLL SYNTHESIZER
RECEIVER

INTRODUCTION

The VHF radios are comprised of two PCB's(an RF PCB and digital PCB). These boards are connected with an 20pin female and male connector. The digital board is interfaced with external data equipment through the 9pin d-sub male connector, which controls the radio and data receiving and sending.

DIGITAL CIRCUITS

The Digital circuit contains the CPU, the channel select switch, and associated digital circuits.

TX-SIGNAL CIRCUIT

The TX data signal comes from Pin 2 of Con 2, and goes through IC1-C. The TX-signal is amplified by IC503-C,D.
The TX-signal is filtered by IC509-B,C which is a 4'th order low pass filter, the output of IC509-B is then fed to the RF board for TX modulation.

RX-SIGNAL CIRCUIT

The RX- data signal comes from the RF board. Which is connected with pin 20 of Con 1. The RX-signal is amplified by IC507 switched by IC1-A and adjusted by R12. The amplified signal goes to pin 10 of Con 2.

RSSI DETECTOR

From the RF board, the RSSI (Received Signal Strength
Indicator) signal flows to IC510-A through R129. The pulse is injected from pin 1 of IC510-A every I mS and C147 is discharged. It is then charged by R133. The RSSI signal is simultaneously input to pin 3 of IC510-A and those signals are compared. The compared signal is output from IC510-A. Pin 1 of IC510-A and the CPU detects the pulse width. The pulse width is varied by RSSI DC voltage, therefore, the carrier detection is controlled by the CPU.

EEPROM

RX / TX channel and RSSI detection level as well as other data from the programmer are stored in the EEPROM. The data stored is retained without power supplied. This is a non-volatile memory. The EEPROM may have information re-programmed or erased. IC502 is an EEPROM with 2048(8X256) capacity and data is written and read serially.

CHANNEL SELECTOR

One of 16 channels may be selected using the Dip Switch (SW2). SW2 encodes the channel number,

selected into 4-bit binary code. The binary code plus one equals the channel number. The binary code is decoded by the CPU enabling the appropriate RX or TX frequency and associated data to be selected from the EEPROM.

DC TO DC CONVERTER

The main DC power is injected to the DC to DC converter. The DC to DC converter regulates the various input power supply voltage and outputs a constant voltage of 7.2 Volts. It is a source for all of the RF and digital circuits.

The DC to DC converter is formed by IC801, Q801, Q802, L801,802 and R804,11. IC801 is a switch mode DC to DC Converter IC. Input DC various appears as a voltage various through R804,11. IC801 detects the voltage and controls the switching pulse. As the switching pulses, Q801 and Q802 switches the input DC of various supply voltages and generates the constant DC of supply voltage.

RF CIRCUITS

TRANSMITTER

The transmitter is comprised of :

1. Buffer
2. P.A..Module
3. Low Pass Filter
4. Antenna Switch
5. A.P.C.Circuits

BUFFER

VCO output level is -6dBm and amplified to +10dBm (VHF). The buffer consists of Q5,22 for isolation and gain.

P. A MODULE

The P.A.PART contains Q22,26,27. Three stage amplifier Q22 amplifies the TX signal from +10dBm to 100mW. Q26 is amplified to 0.5W. Q27 amplifies to 5W and then matched to 50 Ohms using the L. C. network, thereby reducing the harmonics by -30dB.

ANTENNA SWITCH

When transmitting, the diodes D21,22 and D23,24 are forward biased enabling the RF signal passage to the antenna. D6 is shorted to ground inhibiting the RF signal to front end. In receive the diodes D21,22 and D23,24 are revered biased passing the signal from the antenna through L1 and C173 to the front end without signal loss.

RF CIRCUITS PLL SYNTHESIZER

14.4MHz TCXO
The TCXO contains the 3-stage thermistor network compensation and crystal oscillator and modulation ports.
Compensation is ±5 PPM or less from -30c to +60c.

PLL IC DUAL MODULES PRESCALER

Input frequency of 14.4 MHz to IC6 MB15203SL pin 1 is

Divided to 6.25kHz or 5kHz or 2.5KHz by the reference counter, and then supplied to the comparator. RF signal input from VCO is divided to 1/64 at the prescaler in IC6, divided by A and N counter in IC6 to determine frequency steps, and then supplied to the comparator. PLL comparison frequency is 6.25/5/2.5kHz.
The A and N counter is programmed to obtain the desired frequency by serial data in the CPU. In the comparator, the phase difference between reference and VCO signal is compared. When the phase of the reference frequency is leading, Fv is the output, but when VCO frequency is leading, Fr is the output. When Fv=Fr, phase detector out is a very small pulse. 64/65 modulus prescaler is comprised in IC6:

LEVEL SHIFTER & CHARGE PUMP

The charge pump is used for changing output signals Fr,Fv at PLL IC from 0-5v to 0-7.2v necessary for controlling the VCO.

REFERENCE FREQUENCY LPF

The Loop Filter contains R56,57,58, C59,61,62. LPF settling time is 12mS with 1kHz frequency. This also reduces the residual side-band noise for the best signal-to-noise ratio.

VCO

The VCO consist of an RX VCO and a TX VCO. It is switched TX/RX by the power source. It is configured as a colpits oscillator and connected to the buffer as a cascade bias in order to save power. The varicap diode D301,303 are low-resistance elements and produce a change in frequency with a change in reverse bias voltage(2-7v). L308/L303 are resonant coils, which changes the control voltage by the tuning core. D302 modulation diode, modulates the audio signal. C317 compensates for the non-linearity of the VCO due to modulation diode, and maintains a constant modulation regardless of frequency.

RECEIVER

FRONT-END

The receive signal is routed backward through the low pass filter, then onward to Pin 1 of the Receiver Front End Module to a bandpass filter consisting of (C173 through C183, L106 through L107) is coupled to the base of Q19 which serves as an RF amplifier. Diode D103 serves as protection from static RF overload from nearby transmitters. The output of Q19 is then coupled to a second bandpass filter consisting of (C12 through C15 and L110 through L111). The output of Pin 6 is then coupled to the doubly balanced mixer D709. The receiver front end module is factory pre-tuned and requires no adjustment. Repair is effected by replacement of the entire module of the proper banded module. These are UHF 148MHz to 174MHz.

FIRST MIXER

D709, L720 and L723 are double balanced mixers which provide the 45.1MHz intermediate frequency output. The filtered frequency from the front end module is coupled to L720. The 45.1MHz 1F output is matched to the input of the 2-pole monolithic filter by L727,728, C24 and C25. The crystal filter provides a bandwidth of ±7.2kHz from the operating frequency providing a high degree of spurious and intermodulation protection.
Additionally, a 90MHz trap (XF1,2) is also placed at the filter output to provide additional attenuation of the second order IMD. The output of the filter is impedance matched by R161 to the base of the post of filter IF amplifier Q17.

SECOND OSCILLATOR MIXER LIMITER AND FM DETECTOR

The output of the post filter amplifier, Q17, is coupled via C98 to the input of IC3(TA31136FN). IC3 is a monolithic single conversion FM transceiver, containing a mixer, the second local oscillator, limiter and quadrature detector. Crystal XT1 44.645MHz is used to provide resultant 455kHz signal from the output of the second mixer. The mixer output is then routed to CF1(455F). These ceramic filters provide the adjacent channel selectivity of 25kHz bandwidth.

RSSI (RECEIVER SIGNAL STRENGTH INDICATOR)

The RSSI signal is output from IC3 on pin 12. As the receiver signals the output, DC voltage is varied as much as receiver signal strength.