technical reference guide

april 2003

Compaq D315 and hp d325 Personal Computers

This document provides information on the design, architecture, function, and capabilities of the Compaq D315 and the HP d325 Personal Computers. This information may be used by engineers, technicians, administrators, or anyone needing detailed information on the products covered.

Document Part Number 322898-002

This document is designed for printout in the 8 ½- x 11-inch format. The title block below may can be copied and/or cut out and placed into a slip or taped onto the binder.

TRG

Compaq D315 and hp d325 Personal Computers
featuring the AMD Athlon XP processor
and NVidia NForce chipsets

NOTICE

CAUTION: Text set off in this manner indicates that failure to follow directions could result in damage to equipment or loss of information.

NOTE: Text set off in this manner provides information that may be helpful or may require deserves special attention by the reader.

Technical Reference Guide
For the
Compaq D315 and hp d325 Personal Computers
Second Edition - April 2003
Document Part Number 322898-002

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INTRODUCTION

1.1 ABOUT THIS GUIDE

This guide provides technical information about Compaq D315 and the HP d325 personal computers, both which feature the AMD Athlon XP processor and an NVidia NForce series chipset. This document describes in detail the system's design and operation for programmers, engineers, technicians, and system administrators, as well as end-users wanting detailed information.

The chapters of this guide primarily describe the hardware and firmware elements and primarily deal with the system board and the power supply assembly. The appendices contain general data such as error codes and information about standard peripheral devices such as keyboards, graphics cards, and communications adapters.

This guide can be used either as an online document or in hardcopy form.

1.1.1 ONLINE VIEWING

Online viewing allows for quick navigating and convenient searching through the document. A color monitor will also allow the user to view the color shading used to highlight differential data. A softcopy of the latest edition of this guide is available for downloading in .pdf file format at the URL listed below:

http://www3.compaq.com/support/home/selectproduct.asp?destination+reflib&pid+-1

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1.1.2 HARDCOPY

A hardcopy of this guide may be obtained by printing from the .pdf file. The document is designed for printing in an 8 ½ x 11-inch format. Note that printing in black and white will lose color shading used in some illustrations and tables.

1.2 ADDITIONAL INFORMATION SOURCES

For more information on components mentioned in this guide refer to the indicated manufacturers' documentation, which may be available at the following online sources:

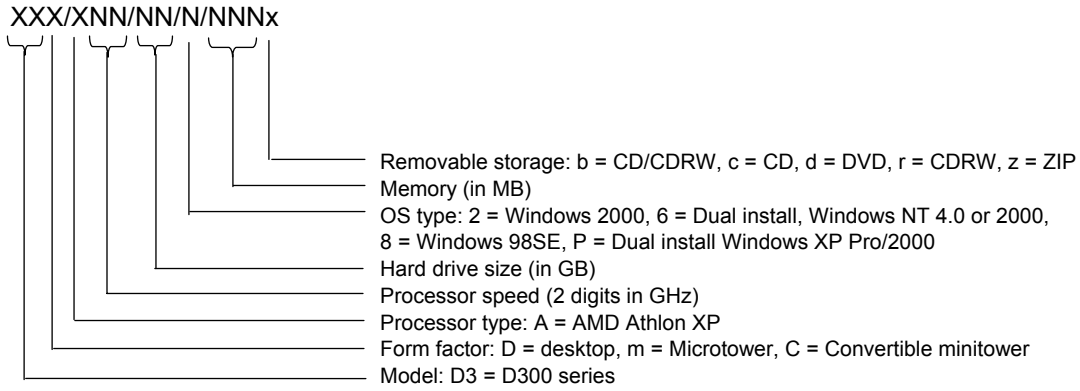
- Hewlett-Packard Company: http://www.hp.com
- Advanced Micro Devices, Inc: http://www.amd.com
- NVIDIA Corporation: http://www.nvidia.com
- Standard Microsystems Corporation: http://www.smsc.com
- Texas Instruments Inc.: http://www.ti.com
- USB user group: http://www.usb.org

1.3 MODEL NUMBERING CONVENTION

Two model numbering conventions (one for Compaq, one for HP) are used for the systems covered in this guide.

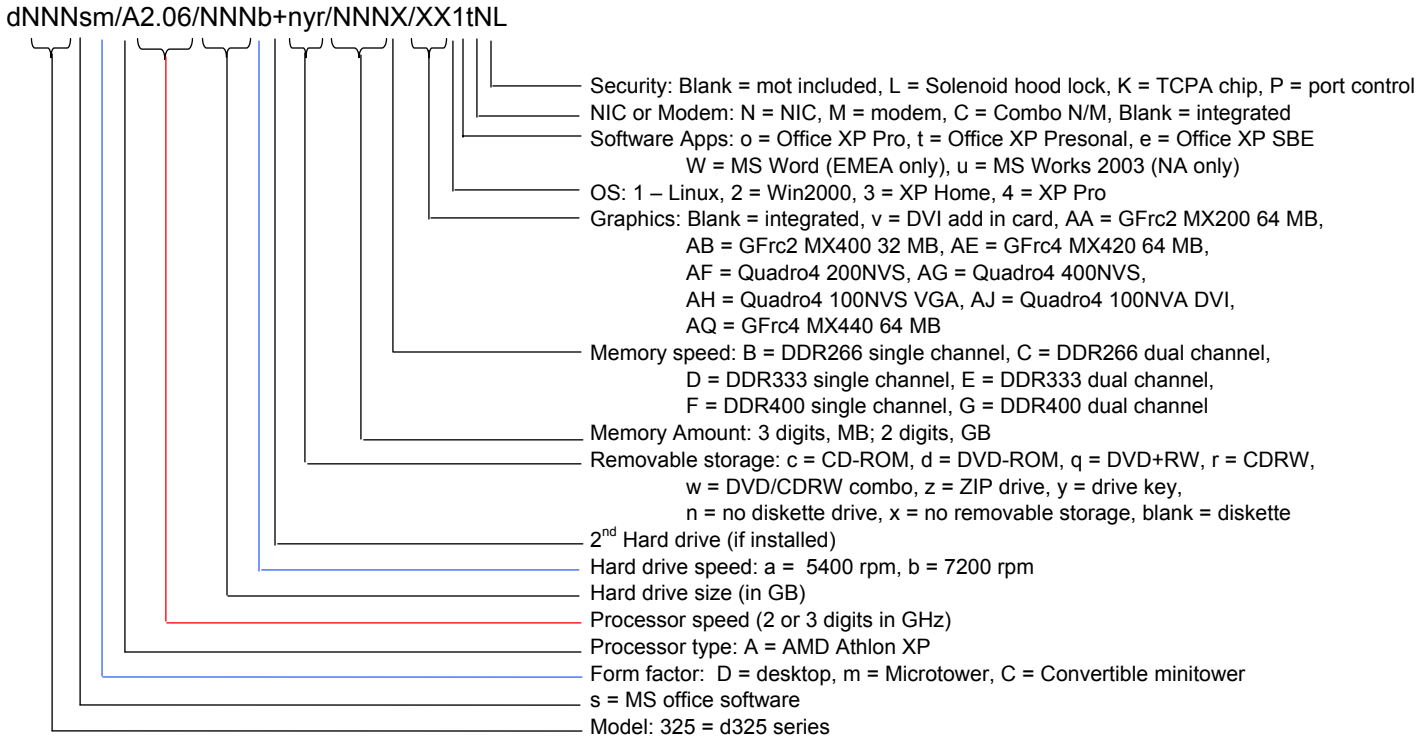
1.3.1 COMPAQ MODEL NUMBERING CONVENTION

The model numbering convention for Compaq systems is as follows:



1.3.2 hp MODEL NUMBERING CONVENTION

The model numbering convention for HP systems is as follows:



1.4 SERIAL NUMBER

The unit's serial number is located on a sticker placed on the exterior cabinet. The serial number may also be read with the Compaq Diagnostics or Compaq Insight Manager utilities.

1.5 NOTATIONAL CONVENTIONS

The notational guidelines used in this guide are described in the following subsections.

1.5.1 VALUES

Hexadecimal values are indicated by a numerical or alpha-numerical value followed by the letter "h." Binary values are indicated by a value of ones and zeros followed by the letter "b." Numerical values that have no succeeding letter can be assumed to be decimal unless otherwise stated.

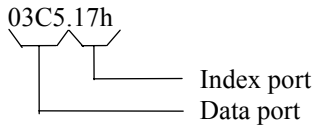
1.5.2 RANGES

Ranges or limits for a parameter are shown using the following methods:

Example A: Bits <7..4> = bits 7, 6, 5, and 4.
Example B: IRQ3-7, 9 = IRQ signals 3 through 7, and IRQ signal 9

1.5.3 REGISTER NOTATION AND USAGE

This guide uses standard Intel naming conventions in discussing the microprocessor's (CPU) internal registers. Registers that are accessed through programmable I/O using an indexing scheme are indicated using the following format:



In the example above, register 03C5.17h is accessed by writing the index port value 17h to the index address (03C4h), followed by a write to or a read from port 03C5h.

1.5.4 BIT NOTATION AND BYTE VALUES

Bit designations are labeled between brackets (i.e., "bit <0 >"). Binary values are shown with the most significant bit (MSb) on the far left, least significant bit (LSb) at the far right. Byte values in hexadecimal are also shown with the MSB on the left, LSB on the right.

1.6 COMMON ACRONYMS AND ABBREVIATIONS

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1.
Acronyms and Abbreviations

Acronym/Abbreviation	Description
A	ampere
AC	alternating current
ACPI	Advanced Configuration and Power Interface
A/D	analog-to-digital
ADC	Analog-to-digital converter
ADD	AGP digital display (card)
AGP	Accelerated graphics port
API	application programming interface
APIC	Advanced Programmable Interrupt Controller
APM	advanced power management
AOL	Alert-On-LAN™
ASIC	application-specific integrated circuit
AT	1) attention (modem commands) 2) 286-based PC architecture
ATA	AT attachment (IDE protocol)
ATAPI	AT attachment w/packet interface extensions
AVI	audio-video interleaved
AVGA	Advanced VGA
AWG	American Wire Gauge (specification)
BAT	Basic assurance test
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
BNC	Bayonet Neill-Concelman (connector type)
bps or b/s	bits per second
BSP	Bootstrap processor
BTO	Built to order
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory
CDS	compact disk system
CGA	color graphics adapter
Ch	Channel, chapter
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntlr	controller
Cntrl	control
codec	1. coder/decoder; 2. compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRIMM	Continuity (blank) RIMM
CRT	cathode ray tube
CSM	Compaq system management / Compaq server management

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
DAC	digital-to-analog converter
DC	direct current
DCH	DOS compatibility hole
DDC	Display Data Channel
DDR	Double data rate (memory)
DIMM	dual inline memory module
DIN	Deutche IndustriNorm (connector type)
DIP	dual inline package
DMA	direct memory access
DMI	Desktop management interface
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
DVI	Digital video interface
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically eraseable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE
ESCD	Extended System Configuration Data (format)
EV	Environmental Variable (data)
ExCA	Exchangeable Card Architecture
FIFO	first in / first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
FPS	Frames per second
ft	Foot/feet
GB	gigabyte
GMCH	Graphics/memory controller hub
GND	ground
GPIO	general purpose I/O
GPOC	general purpose open-collector
GPU	Graphics processing unit
GART	Graphics address re-mapping table
GUI	graphic user interface
h	hexadecimal
HW	hardware
hex	hexadecimal
Hz	Hertz (cycles-per-second)
ICH	I/O controller hub
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I/F	interface
IGP	Integrated graphics processor

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
in	inch
INT	interrupt
I/O	input/output
IPL	initial program loader
IrDA	Infrared Data Association
IRQ	interrupt request
ISA	industry standard architecture
Kb / KB	kilobits / kilobytes (x 1024 bits / x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kV	kilovolt
lb	pound
LAN	local area network
LCD	liquid crystal display
LED	light-emitting diode
LPC	Low pin count
LSI	large scale integration
LSb / LSB	least significant bit / least significant byte
LUN	logical unit (SCSI)
m	Meter
MCH	Memory controller hub
MCP	Media communication processor
MMX	multimedia extensions
MPEG	Motion Picture Experts Group
ms	millisecond
MSb / MSB	most significant bit / most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
n	variable parameter/value
NIC	network interface card/controller
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
NRZI	Non-return-to-zero inverted
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory
OS	operating system
PAL	1. programmable array logic 2. phase alternating line
PC	Personal computer
PCA	Printed circuit assembly
PCI	peripheral component interconnect
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
PFC	Power factor correction
PIN	personal identification number
PIO	Programmed I/O
PN	Part number
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RDRAM	(Direct) Rambus DRAM
RGB	red/green/blue (monitor input)
RH	Relative humidity
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	Read/Write
SCSI	small computer system interface
SDR	Singles data rate (memory)
SDRAM	Synchronous Dynamic RAM
SEC	Single Edge-Connector
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag
SGRAM	Synchronous Graphics RAM
SIMD	Single instruction multiple data
SIMM	single in-line memory module
SMART	Self Monitor Analysis Report Technology
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPD	serial presence detect
SPDIF	Sony/Philips Digital Interface (IEC-958 specification)
SPN	Spare part number
SPP	standard parallel port
SRAM	static RAM
SSE	Streaming SIMD extensions
STN	super twist pneumatic
SVGA	super VGA
SW	software

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
TAD	telephone answering device
TAFI	Temperature-sensing And Fan control Integrated circuit
TCP	tape carrier package
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTL	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
UDMA	Ultra DMA
URL	Uniform resource locator
us / μs	microsecond
USB	Universal Serial Bus
UTP	unshielded twisted pair
V	volt
VAC	Volts alternating current
VDC	Volts direct current
VESA	Video Electronic Standards Association
VGA	video graphics adapter
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WOL	Wake-On-LAN
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

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Chapter 2
SYSTEM OVERVIEW

2.1 INTRODUCTION

The Compaq D315 and HP d325 personal computers (Figure 2-1) deliver outstanding manageability, serviceability, and compatibility for enterprise environments. Based on the AMD Athlon XP processor and an NVidia NForce Chipset, these systems emphasize performance along with industry compatibility. These models feature an architecture incorporating the PCI bus. All models are easily upgradeable and expandable to keep pace with the needs of the office enterprise.

Figure 2-1. Compaq D315 and hp d325 Personal Computers

This chapter includes the following topics:

2.2 FEATURES AND OPTIONS

This section describes the standard features and available options.

2.2.1 STANDARD FEATURES

The following standard features are included on all models:

- AMD Athlon XP processor
- Three full-height, full-length PCI slots
- One AGP slot
- 3.5 inch, 1.44-MB diskette drive
- IDE controller w/UATA/100 mode support
- 5 drive bays (two internal 3.5", two internal 5.25", one 3.5" diskette drive)
- Hard drive fault prediction
- Communications interfaces including:
  - One serial interface
  - One parallel interface
  - One network interface
  - Six USB interfaces
- Plug 'n Play compatible (with ESCD support)
- Intelligent Manageability support
- Energy Star compliant
- Security features including:
  - Flash ROM Boot Block
  - Diskette drive disable, boot disable, write protect
  - Power-on password
  - Administrator password
  - Serial/parallel port disable
- PS/2 Compaq Easy-Access keyboard w/Windows support
- PS/2 Compaq Scroll Mouse
- 220-watt Power Supply
- Available with Windows XP Home, XP Professional, or Mandrake Linux 8.2

Table 2-1 lists the differences between the Compaq D315 and hp d325 models.

Table 2-1.
Feature Difference Matrix

Feature	Compaq D315	hp d325
DIMM type support (max)	PC2100 DDR	PC2700 DDR
Standard graphics controller	Integrated GeForce2 MX	Integrated GeForce 4 MX
AGP level of support	4X	8X
USB level of support	1.1	2.0
Multibay support?	No	Yes
Hood Sense/Hood Lock function?	No	Yes

2.2.2 OPTIONS

The following items are available as options for all models and may be included in the standard configuration of some models:

- System Memory:

  Model D315:
  PC2100 64-MB DDR DIMM (unbuffered, non-ECC)
  PC2100 128-MB DDR DIMM (unbuffered, non-ECC)
  PC2100 256-MB DDR DIMM (unbuffered, non-ECC)
  PC2100 512-MB DDR DIMM (unbuffered, non-ECC)

  Model D325:
  PC2700 64-MB DDR DIMM (unbuffered, non-ECC)
  PC2700 128-MB DDR DIMM (unbuffered, non-ECC)
  PC2700 256-MB DDR DIMM (unbuffered, non-ECC)
  PC2700 512-MB DDR DIMM (unbuffered, non-ECC)

- Hard drives/controllers:
  20-, 40-, 60, or 80-GB UATA/100 hard drive
  32-GB Wide Ultra3 SCSI hard drive

- Removeable media drives:
  16x/10x/40x CD-RW drive
  10x/40x Max DVD-ROM drive
  LS-120 Super Disk drive
  PCI DXR DVD Decoder kit

- Graphics Monitors:
  Compaq P700 17" CRT
  Compaq P900 19" CRT
  Compaq P1100 21" CRT
  Compaq TFT5010 15" Flat Panel
  Compaq TFT8020 18" Flat Panel

2.3 MECHANICAL DESIGN

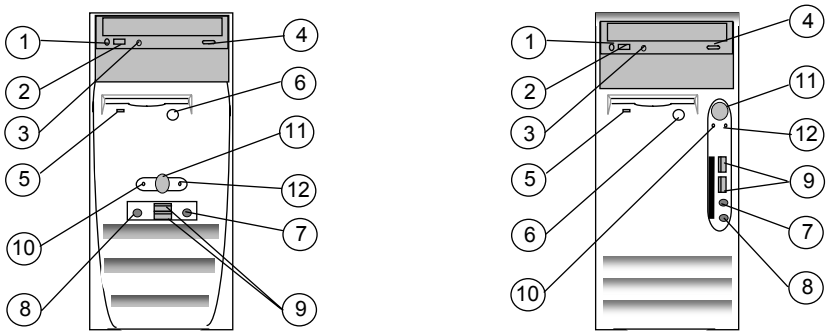
The following subsections describe the mechanical (physical) aspects of the Compaq D315 PC and the HP Business PC d325 models.

CAUTION: Voltages are present within the system unit whenever the unit is plugged into a live AC outlet, regardless of the system's "Power On" condition. **Always disconnect the power cable from the power outlet and/or from the system unit before handling the system unit in any way.**

NOTE: The following information is intended primarily for identification purposes only. **Before servicing these systems refer to the applicable *Service Reference Guide*.** Service personnel should review training materials also available on these products.

2.3.1 CABINET LAYOUTS

2.3.1.1 Front Views

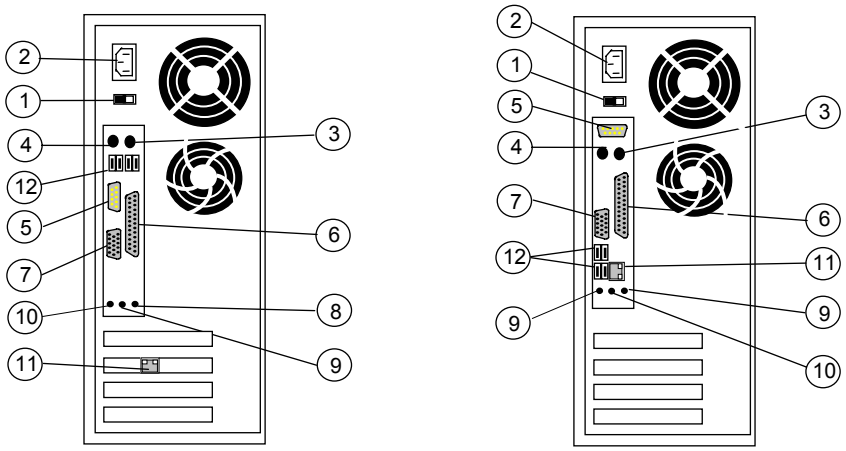


Item	Description
1	CD-ROM drive headphone jack
2	CD-ROM drive volume control
3	CD-ROM drive activity LED
4	CD-ROM drive open/close button
5	1.44-MB diskette drive activity LED
6	1.44-MB diskette drive eject button
7	Microphone In Jack
8	Headphone Out Jack
9	Universal Serial Bus Connectors (2)
10	Power LED
11	Power Button
12	Hard Drive Activity LED

Figure 2-2. Cabinet Layout, Front Views

2.3.1.2 Rear Views

Figure 2-4 shows the rear view of the Compaq D315 and HP d325 systems.



Item	Description	Item	Description
1	AC voltage switch	7	VGA monitor connector
2	AC power connector	8	Audio microphone in jack
3	Mouse connector	9	Audio line input jack
4	Keyboard connector	10	Audio line output jack
5	Serial connector	11	Network interface connector
6	Parallel connector	12	USB ports (4)

Figure 2-3. Cabinet Layout, Rear Views

2.3.2 CHASSIS LAYOUT

This section describes the internal layout of the chassis. For detailed information on servicing the chassis refer to the multimedia training and/or the *Service Reference Guide* for these systems. Figure 2-4 shows the layout for the Compaq D315 or hp d325 personal computers.

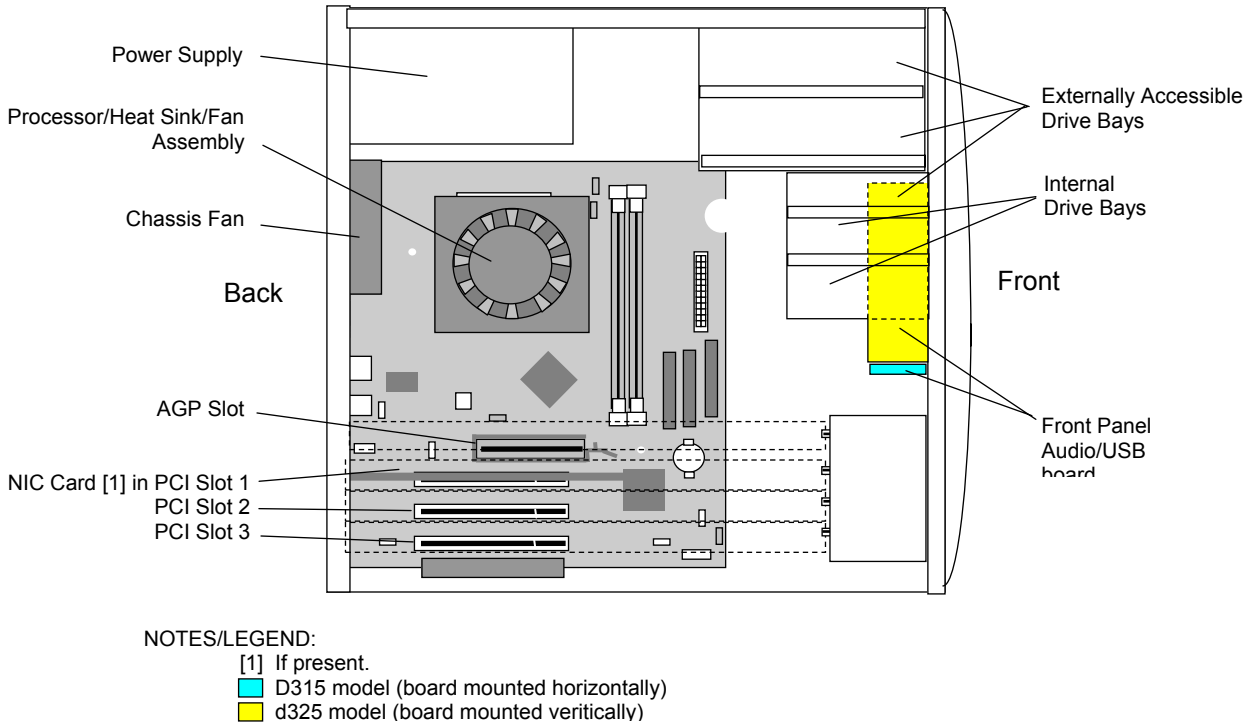
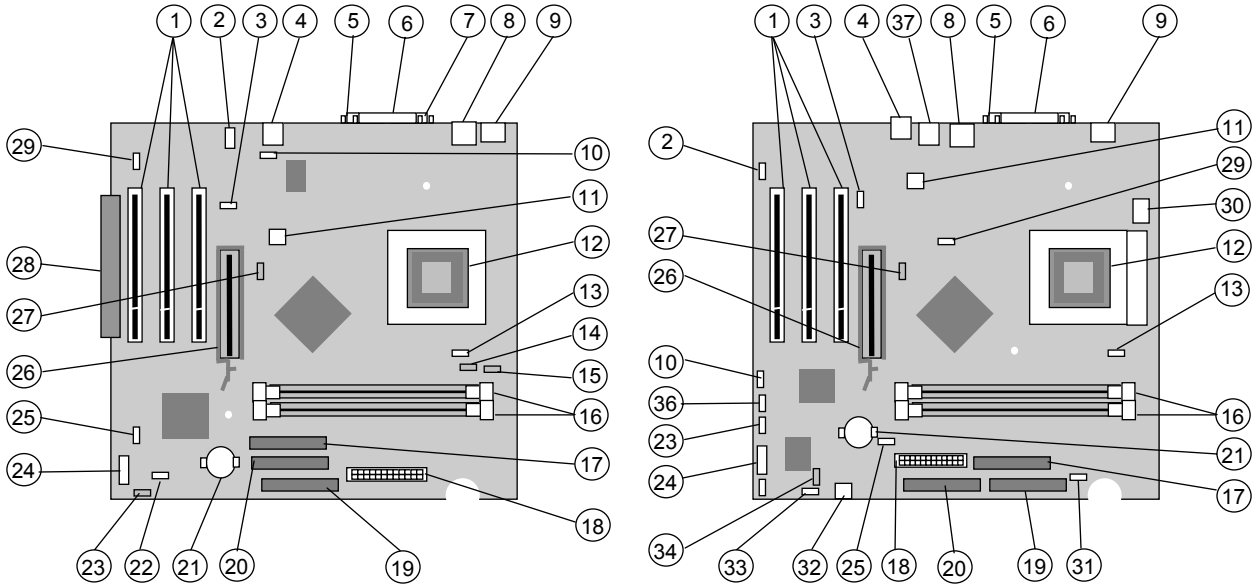


Figure 2-4. Chassis Layout, Left Side View

2.3.3 BOARD LAYOUTS

Figure 2-5 shows the system boards.



Item	Description	Item	Description
1	PCI slots	20	Primary ATA connector
2	Front panel audio connector	21	Battery
3	Chassis fan connector	22	CMOS clear jumper
4	Audio jacks: Mic in (top), line in, line out	23	Front panel USB connector
5	VGA connector	24	Front panel power switch / LED connector
6	Parallel port connector	25	Password clear jumper
7	Serial port connector	26	AGP slot
8	USB ports [2]	27	Safe mode jumper
9	Top: Mouse port; bottom: keyboard port	28	PCI bus expansion connector [1]
10	CD audio connector	29	Auxiliary audio connector
11	Processor power	30	Serial port (COM1) conenc/tor
12	Processor socket	31	MultiBay connector
13	Processor fan connector	32	Hood sense connector
14	Fan ground control	33	Hood lock connector
15	Fan power control	34	BIOS boot block connector
16	DIMM sockets	35	Fan CMD connector
17	Secondary ATA connector	36	Speaker audio connector
18	Power supply connector	37	NIC connector (top), USB ports (2) bottom
19	Diskette drive connector	--	--

NOTE8:

[1] Not used in this system.
[2] D315 board, 4 stack; d325 board, 2 stack

Figure 2-5. System Board Layouts

2.4 SYSTEM ARCHITECTURE

The Compaq D315 and HP d325 feature an architecture based on the AMD Athlon XP processor and an NVidia NForce chipset (Figure 2-6).

The AMD Athlon XP processor features an x86-class CPU that uses a highly-pipelined architecture to process a high volume of data per clock cycle to provide exceptional performance in handling audio, video, and image files. Operating at speeds up to 2.13 GHz, the Athlon XP processor is optimized for the Microsoft Windows XP operating system.

The D315 model uses a Nvidia NForce 220 chipset while the d325 model uses the NForce2 420 chipset. Both chipsets include the following functions and features:

- Athon XP processor support
- Integrated Graphics Processor (IGP) providing:
  - Integrated GeForce MX-class graphics controller
  - AGP interface support for graphics upgrade
  - SDRAM controller supporting two DDR DIMMs
- Media & Communication Processor (MCP) providing:
  - Two IDE controllers supporting up to four ATA100 storage devices
  - Six USB ports
  - AC link interface servicing the audio controller
  - PCI bus controller supporting up to three 32-bit 33-MHz PCI expansion devices
  - LPC bus interface serving the BIOS ROM and super I/O component

Table 2-1 lists the architectural differences between the D315 and d325 models:

Table 2-2.
Architectural Difference Matrix

Feature	Compaq D315	hp d325
Chipset type:	NForce 220	NForce2 420
North Bridge Component	IGP-64	IGP-128
South Bridge Component	MCP	MCP-2
FSB speed (max)	266 MHz	333 MHz
DIMM type support (max)	PC2100 DDR	PC2700 DDR
Standard graphics controller	Integrated GeForce2 MX	Integrated GeForce 4 MX
AGP level of support (max)	4X	8X
USB level of support (max)	1.1	2.0
Network Interface Controller	Separate PCI card	Integrated
Multibay support?	No	Yes
Hood Sense/Hood Lock function?	No	Yes

An STC LPC47B367 Super I/O Controller provides legacy PS/2 keyboard and mouse interfaces, serial and parallel interfaces, and diskette drive interface functions.

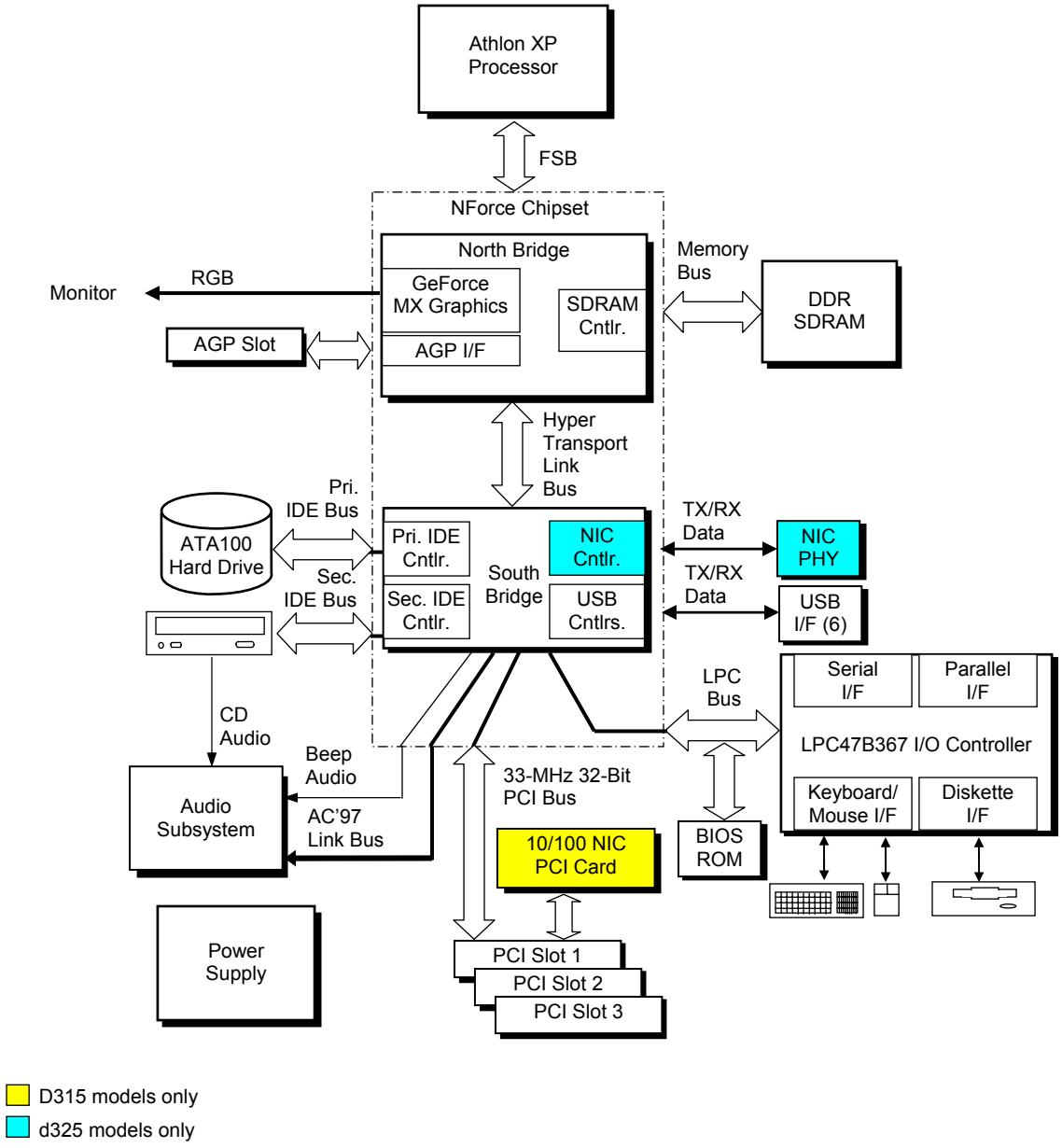


Figure 2-6. System Architecture, Block Diagram

2.4.1 AMD ATHLON XP PROCESSOR

The systems covered in this guide feature the AMD Athlon XP processor. This processor is compatible with software written for most x86-type microprocessors including the AMD Duron and Intel Pentium-type processors and includes the following features:

- QuantiSpeed™ architecture
- 128-KB L1 and 256-KB L2 full-speed caches
- 3DNow!™ professional technology (full SSE compatibility)
- 0.13 micron copper process technology

The Athlon XP processor uses a nine-stage, superscalar pipelined CPU core to process more instructions in a given clock cycle than other x86-type processors. Optimized for the Windows XP operating systems, the Athlon XP processor is also compatible with all earlier Windows operating systems (Windows 2000, ME, and 98). These systems use the Socket-A method of processor mounting as shown in Figure 2-7.

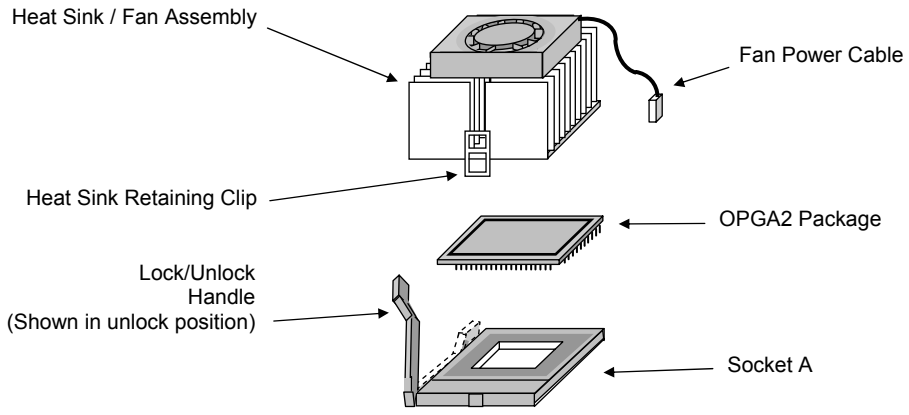


Figure 2-7. Heat Sink, Processor, and Socket Assemblies

NOTE: Heat sink types are **not** interchangeable. Also, these systems support processors using the **OPGA2 package only**.

2.4.2 CHIPSET

The D315 model uses a NVidia NForce 220 chipset while the D325 model uses the NVidia NForce2 chipset. Table 2-3 provides a comparison of the two chipset types.

Table 2-3. NVidia Chipset Comparison

Component	NForce 220	NForce 2 420
North Bridge	IGP-64	IGP-128
FSB speed (max)	266-MHz	333-MHz
Memory Bandwidth (max)	64-bit	128-bit
Graphics Processing Unit	GeForce2 MX	GeForce4 MX
AGP Interface (max)	4X	8X
South Bridge	MCP	MCP-2
PCI bus I/F	Yes	Yes
LPC bus I/F	Yes	Yes
Two IDE UATA/100 controllers	Yes	Yes
AC Link controller	Yes	Yes
IRQ controller	Yes	Yes
Power management logic	Yes	Yes
Two USB 1.1 controllers	Yes	Yes
One USB 2.0 controller	No	Yes

NOTE:
Unless otherwise indicated, all functions are common to both chipsets.

2.4.3 SUPPORT COMPONENTS

Input/output functions not provided by the chipset are handled by other support components. Some of these components also provide "housekeeping" and various other functions as well. Table 2-4 shows the functions provided by the support components.

Table 2-4.
Support Component Functions

Component Name	Function
LPC47B367 I/O Controller	Keyboard and pointing device I/F Diskette I/F Serial I/F (1) Parallel I/F (1) AGP, PCI reset generation Interrupt (IRQ) serializer Power button logic GPIO ports
AD1885 (D315) or AD1981 (d325) Audio Codec	Audio mixer Digital-to-analog converter Analog-to-digital converter Analog I/O 6-channel audio support (AD1981 only)

2.4.4 SYSTEM MEMORY

These systems use the NVidia IGP component that supports DDR SDRAM. The system board provides two sockets that accept industry-standard unbuffered DDR DIMMs.

The D315 system uses the IGP-64 controller that supports 64-bit PC2100 DDR memory and a maximum of 1 gigabyte of memory.

The d325 system uses the IGP-128 controller supporting 128-bit (when two DIMMs are installed) PC2700 DDR memory and a maximum of 2 gigabytes of memory.

2.4.5 MASS STORAGE

All models include a 3.5 inch 1.44-MB diskette drive installed as drive A. Most models also include a CD-ROM and a 20- to 80-GB hard drive. Standard hard drives feature Drive Protection System (DPS) support. All systems provide two (one primary, one secondary) PCI bus-mastering Enhanced IDE (EIDE) controllers integrated into the chipset. Each controller provides UATA/100 support for two drives for a total of four IDE devices, although the form factor will determine the actual number of drive spaces available.

2.4.6 SERIAL AND PARALLEL INTERFACES

This system includes one serial port and a parallel port accessible at the rear of the chassis. The serial interface is RS-232-C/16550-compatible and supports standard baud rates up to 115,200 as well as two high-speed baud rates of 230K and 460K, and utilizes a DB-9 connector. The parallel interface is Enhanced Parallel Port (EPP1.9) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers through a DB-25 connector.

2.4.7 UNIVERSAL SERIAL BUS INTERFACE

The Universal Serial Bus (USB) interface supports hot plugging/unplugging (Plug ’n Play) functionality for six USB ports. Two ports are accessible at the front of the unit and four ports are available at the rear of the chassis. The D315 model provides USB 1.1 support while the d325 model provides 2.0 support.

2.4.8 NETWORK INTERFACE CONTROLLER

All models feature a Network Interface Controller (NIC). The D315 model includes either a Accton 10/100 NIC featuring Wake-On-LAN or an Intel 10/100 NIC PCI card featuring WOL and AOL, depending on configuration. The d325 model features a 3Com NIC integrated on the system board.

2.4.9 GRAPHICS SUBSYSTEM

The IGP component provides AGP interface support as well as including a GeForce MX-class graphics processing unit. The system may be upgraded adding a separate AGP card to replace the integrated graphic controller.

Table 2-5 lists the key specifications of the standard graphics subsystems employed in these systems:

Table 2-5.
Standard Graphics Support Comparison

	D315	**d325**
Bus Type	AGP 4X	AGP 8X
Graphics processing unit	GeForce 2 MX	GeForce 4 MX
DAC Speed	300 MHz	300 MHz
Max. 2D Res.	1900 x 1200	1900 x 1200
Software Compatibility	S3TC DCI/DirectX, Direct Draw, MPEG 1/2,	S3TC DCI/DirectX, Direct Draw, MPEG 1/2,

2.4.10 AUDIO SUBSYSTEM

This system uses the integrated AC97 audio controller of the chipset and the Analog Devices AD1885 (D315 models) or AD1981 (d325 models) codec. These systems include microphone and line inputs and headphone and line outputs. The system includes a 3-watt output amplifier driving an internal speaker, and the headphone and microphone jacks are duplicated on both the front panel and the rear chassis panel.

2.5 SPECIFICATIONS

This section includes the environmental, electrical, and physical specifications for the Hewlett-Packard Personal Computers. Where provided, metric statistics are given in parenthesis. All specifications are subject to change without notice.

Table 2-6.
Environmental Specifications (Factory Configuration)

Parameter	Operating	Nonoperating
Ambient Air Temperature	50° to 95° F (10° to 35° C, max. rate of change ≤ 10°C/Hr)	-24° to 140° F (-30° to 60° C, max. rate of change ≤ 20°C/Hr)
Shock (w/o damage)	5 Gs [1]	20 Gs [1]
Vibration	0.000215 G^2/Hz, 10-300 Hz	0.0005 G^2/Hz, 10-500 Hz
Humidity	10-90% Rh @ 28° C max. wet bulb temperature	5-95% Rh @ 38.7° C max. wet bulb temperature
Maximum Altitude	10,000 ft (3048 m) [2]	30,000 ft (9144 m) [2]

NOTE:
[1] Peak input acceleration during an 11 ms half-sine shock pulse.
[2] Maximum rate of change: 1500 ft/min.

Table 2-7.
Electrical Specifications

Parameter	U.S.	International
Input Line Voltage:		
Nominal:	100 - 127 VAC	200 - 240 VAC
Maximum:	90 - 132 VAC	180 - 264 VAC
Input Line Frequency Range:		
Nominal:	50 - 60 Hz	50 - 60 Hz
Maximum:	47 - 63 Hz	47 - 63 Hz
Power Supply:		
Maximum Continuous Power	235 watts	235 watts
Maximum Line Current Draw	3.6 A @ 100 VAC	3.6 A @ 200 VAC

Table 2-8.
Physical Specifications

Height	14.50 in (36.83 cm)
Width	6.88 in (17.48 cm)
Depth	16.55 in (42.04 cm)
Weight (nom.) [1]	23.8 lb (10.92 kg)
Maximum Supported Weight [2]	100 lb (45.50 kg)

NOTES:

[1] System weight may vary depending on installed drives/peripherals.
[2] Assumes reasonable article(s) such as a display monitor and/or another system unit.

Table 2-9.
Diskette Drive Specifications
(Compaq SP# 278644-001)

Parameter	**Measurement**
Media Type	3.5 in 1.44 MB/720 KB diskette
Height	1/3 bay (1 in)
Bytes per Sector	512
Sectors per Track:	
High Density	18
Low Density	9
Tracks per Side:	
High Density	80
Low Density	80
Read/Write Heads	2
Average Access Time:	
Track-to-Track (high/low)	3 ms/6 ms
Average (high/low)	94 ms/169ms
Settling Time	15 ms
Latency Average	100 ms

Table 2-10.
Optical Drive Specifications

Parameter	48x CD-ROM	16/10/40x CD-RW Drive
Part number	232320-001	281749-001
Interface Type	IDE	IDE
Media Type (reading)	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA
Media Type (writing)	N/a	CD-R, CD-RW
Transfer Rate (Reads)	4.8 Kb/s (max sustained)	CD-ROM, 4.8 Kb/s; CD-ROM/CD-R, 1.5-6 Kb/s
Transfer Rate (Writes):	N/a	CD-R, 2.4 Kbps (sustained); CD-RW, 1.5 Kbps (sustained);
Capacity:		650 MB @ 12 cm
Mode 1, 12 cm	540 MB	
Mode 2, 12 cm	650 MB	
8 cm	180 MB	180 cm
Center Hole Diameter	15 mm	15 mm
Disc Diameter	8/12 cm	8/12 cm
Disc Thickness	1.2 mm	1.2 mm
Track Pitch	1.6 um	1.6 um
Laser		
Beam Divergence	53.5 +/- 1.5 °	53.5 + 1.5°
Output Power	53.6 0.14 mW	53.6 0.14 mW
Type	GaAs	GaAs
Wave Length	790 +/- 25 nm	790 +/- 25 nm
Average Access Time:		
Random	<100 ms	<120 ms
Full Stroke	<150 ms	<200 ms
Audio Output Level	0.7 Vrms	0.7 Vrms
Cache Buffer	128 KB	128 KB

Table 2-11.
Hard Drive Specifications

Parameter	20.0 GB	20.0 GB	40.0 GB	40.0 GB
Part Number	249408-001	260671-001	236421-001	286692-001
Drive Size	3.5”	3.5”	3.5”	3.5”
Interface	UATA/100	UATA/100	UATA/100	UATA/100
Transfer Rate	100 MBps	100 MBps	100 MBps	100 MBps
Drive Protection System Support?	Yes	Yes	Yes	Yes
Typical Seek Time (w/settling) [1]				
Single Track	2.0 ms	1.2 ms	1.5 ms	1.2 ms
Average	12.8 ms	8.0 ms	10.5 ms	8.0 ms
Full Stroke	28.5 ms	18 ms	23 ms	18 ms
Disk Format (logical blocks)	39,102,336	39,102,336	39,102,336	78,165,360
Rotation Speed	5400 RPM	7200 RPM	5400 RPM	7200 RPM
Drive Fault Prediction	SMART III	SMART III	SMART III	SMART III

NOTE:
Actual times may vary depending on specific drive installed.

Chapter 3
PROCESSOR/ MEMORY SUBSYSTEM

3.1 INTRODUCTION

This chapter describes the processor/memory subsystem. These systems feature the AMD Athlon XP processor and an NVidia NForce chipset (Figure 3-1).

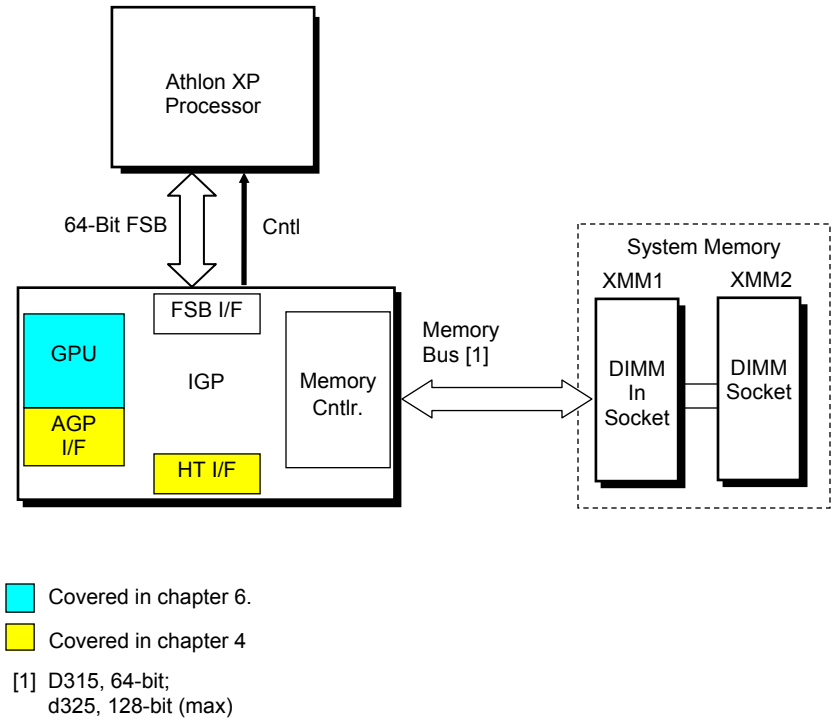


Figure 3–1. Processor/Memory Subsystem Architecture

This chapter includes the following topics:

3.2 ATHLON XP PROCESSOR

This system features an AMD Athlon XP processor in a Socket 462-compatible package mounted with a passive heat sink. The mounting socket allows the processor to be easily changed for servicing and/or upgrading.

3.2.1 PROCESSOR OVERVIEW

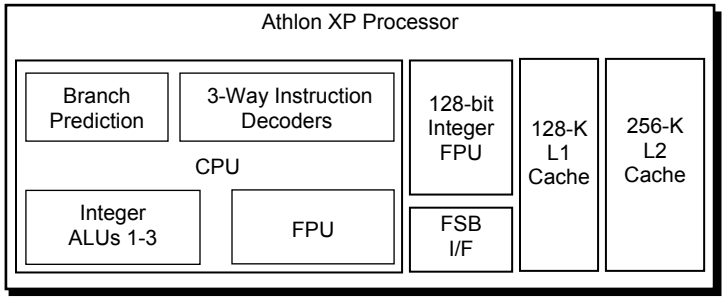
The AMD Athlon XP processor represents the latest development of AMD processors that takes advantage of the Windows XP operating system. The Athlon XP processor is well-suited for demanding applications involving digital photo manipulation, video editing, audio and video streaming over the internet, 3D modeling, and commercial desktop publishing.
Key features of the Athlon XP processor include:

- Superpipelined, superscalar technology – A nine-stage pipeline for increased processing frequencies.
- Multple x86 instruction decoders for parallel processing
- Hardware data prefetch
- Advanced Translation Look-Aside Buffer for data and instruction addresses
- Large full-speed 384-KB cache – 128-KB L1 cache and 256-KB L2 cache
- Enhanced Floating Point Processor - Executes all x87 (math co-processor), MMX, SSE, and 3DNow! instructions.
- Advanced dynamic branch prediction

The Athlon XP processor is backward-compatible with software written for most x86-type processors such as the AMD Athlon 4, AMD Duron, and Intel Pentium processors. The Athlon XP processor supports applications using MMX, SSE, and 3DNow! instructions.

Manufactured using 0.13 micron technology, the Athlon XP processor's uses a deeply-pipelined, superscalar architecture that uses three x86 instruction decoders that each feed an execution engine. Parallel execution engines provide a 3-instruction-per-clock cycle ability that is unmatched by other x86 processors. In addition, the floating pointing unit features QuantiSpeed architecture that uses three execution units that work in parallel to process as many as four 32-bit floating point results per cycle.

Figure 3-2 illustrates the internal architecture of the Athlon XP processor.



Athlon XP Type	Core Speed	Voltage	Max. Current	Max. Power
Model 6 1500+	1333 MHz	1.75 VDC	34.3 A	60.0 W
Model 6 1600+	1400 MHz	1.75 VDC	35.9 A	62.8 W
Model 6 1700+	1467 MHz	1.75 VDC	36.6 A	64.0 W
Model 8 1700+	1467 MHz	1.50 VDC	32.9 A	49.4 W
Model 6 1800+	1533 MHz	1.75 VDC	37.7 A	66.0 W
Model 8 1800+	1533 MHz	1.50 VDC	34.0 A	51.0 W
Model 6 1900+	1600 MHz	1.75 VDC	38.9 A	68.0 W
Model 8 1900+	1600 MHz	1.50 VDC	35.0 A	52.2 W
Model 6 2000+	1667 MHz	1.75 VDC	40.0 A	70.0 W
Model 8 2000+	1667 MHz “ “	1.60 VDC 1.65 VDC 1.60 VDC	37.7 A 36.5 A 38.3 A	60.3 W 60.3 W 61.3 W
Model 6 2100+	1733 MHz	1.75 VDC	41.1 A	72.0 W
Model 8 2100+	1733 MHz	1.60 VDC	38.8 A	61.1 W
Model 8 2200+	1800 MHz “	1.60 VDC “	41.2 A 39.3 A	67.9 W 62.8 W
Model 8 2400+	2000 MHz	1.65 VDC	41.4 A	68.3 W
Model 8 2600+	2133 MHz 2083 MHz	1.65 VDC “	41.4 A “	68.3 W “
Model 8 2800+	2083 MHz	1.65 VDC	41.4 A	68.3 W
Model 8 3000+	2167 MHz	1.65 VDC	45.0 A	74.3 W

Figure 3–2. AMD Athlon XP Processor Internal Architecture and Key Statistics.

The Athlon XP processor uses 0.13 micron technology that yields lower power requirements for a given processing speed. The system board supports the unit types listed in Figure 3-2.

The Athlon XP processor uses a 133-MHz (on D315 systems) or 166-MHz (on d325 systems) clock signal for the front side bus. Data transfers are qualified on the both the rising and falling edge of the clock cycle, effectively doubling the data throughput rate to 266- and 333-MHz.

The AMD Athlon XP processor is compatible with software written for Athlon 4, Duron, and most other x86 processors, but will require the latest versions of operating system software to take advantage of the specific features and functions.

3.2.2 PROCESSOR UPGRADING

This system uses the Socket A mounting socket. A replacement processor must use the same type heat sink (passive or fan cooled) as the original to ensure proper cooling.

CAUTION: The D315 model supports processor speeds up to 2.0 gigahertz. The d325 model supports processor speeds up to 2.3 GHz. Using a processor that exceeds a particular model's capability may result in equipment failure and/or damage.

NOTE: These systems ship with Athlon XP processors but do support Duron processors as well.

The heat sink is specially designed provide maximum heat transfer from the processor component.

CAUTION: Attachment of the heat sink to the processor is critical on these systems. Improper attachment of the heat sink will likely result in a thermal condition. Although the system is designed to detect thermal conditions and automatically shut down, such a condition could still result in damage to the processor component. Refer to the applicable *Service Reference Guide* for processor installation instructions.

3.3 MEMORY SUBSYSTEM

These systems provide two 184-pin DIMM sockets that accept DDR DIMMs. The D315 models ship with PC2100 DIMMs while the d325 models ship with PC2700 DIMMs.

NOTE: The DDR SDRAM DIMM "PCxxxx" reference designates bus bandwidth (i.e., a PC2100 DIMM, operating at a 266-MHz effective speed, provides a throughput of 2100 MBps (8 bytes × 266 MHz)).

These systems support DIMMs with the following specifications:

- Unbuffered, non-ECC with SPD rev. 1.0
- CL (CAS latency) = 2, 2.5, or 3
- Single or double-sided

The following table lists the differences in DIMM support between the D315 and the D325 models:

	D315	**d325**
DIMM Type (max speed)	PC2100 (266-MHz)	PC2700 (333-MHz)
Highest technology level supported	512 Mb	1024 Mb
Maximum amount supported	1 GB	2 GB

The SPD format as supported in this system (SPD rev. 1) is shown in Table 3-1. All DIMMs must yield a value of 07h (indicating DDR memory) in SPD byte 02 (i.e., **only DDR DIMMs are supported in these systems**).

The memory subsystem is controlled by the memory controller integrated into the IGP component of the NVidia NForce chipset. The D315 model supports a 64-bit wide memory array with a maximum capacity of up to 1-GB using 512-Mb memory technology. The d325 model provides (with two DIMMs installed) a 128-bit wide memory array with a maximum capacity of 2 GB using 1-Mb memory technology.

NOTE: Non-supported DIMMs will not be recognized by the BIOS during the boot sequence and therefore not be used.

The SPD address map is shown below.

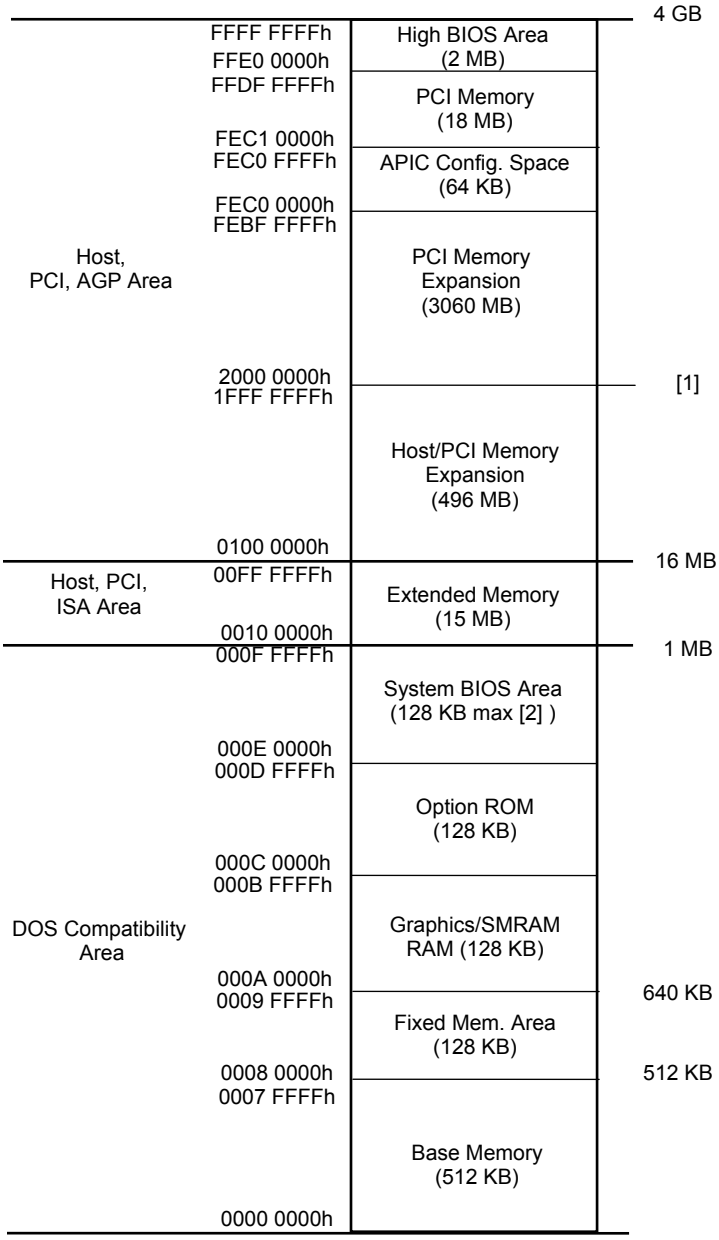
Table 3-1.
SPD Address Map (SDRAM DIMM)

Byte	Description	Notes	Byte	Description	Notes
0	No. of Bytes Written Into EEPROM	[1]	25	Min. CLK Cycle @ CL X-2	[7]
1	Total Bytes (#) In EEPROM	[2]	26	Max. Acc. Frm CLK @ CL X-2	[7]
2	Memory Type		27	Min. Row Prechge. Time	[7]
3	No. of Row Addresses On DIMM	[3]	28	Min. Row Active to Delay	[7]
4	No. of Column Addresses On DIMM		29	Min. RAS to CAS Delay	[7]
5	No. of Module Banks On DIMM		30, 31	Reserved	
6, 7	Data Width of Module		32..61	Superset Data	[7]
8	Voltage Interface Standard of DIMM		62	SPD Revision	[7]
9	Cycletime @ Max CAS Latency (CL)	[4]	63	Checksum Bytes 0-62	
10	Access From Clock	[4]	64-71	JEP-106E ID Code	[8]
11	Config. Type (Parity, Nonparity, etc.)		72	DIMM OEM Location	[8]
12	Refresh Rate/Type	[4] [5]	73-90	OEM's Part Number	[8]
13	Width, Primary DRAM		91, 92	OEM's Rev. Code	[8]
14	Error Checking Data Width		93, 94	Manufacture Date	[8]
15	Min. Clock Delay	[6]	95-98	OEM's Assembly S/N	[8]
16	Burst Lengths Supported		99-125	OEM Specific Data	[8]
17	No. of Banks For Each Mem. Device	[4]	126	Intel frequency check	
18	CAS Latencies Supported	[4]	127	Reserved	
19	CS# Latency	[4]	128-131	Compaq header "CPQ1"	[9]
20	Write Latency	[4]	132	Header checksum	[9]
21	DIMM Attributes		133-145	Unit serial number	[9] [10]
22	Memory Device Attributes		146	DIMM ID	[9] [11]
23	Min. CLK Cycle Time at CL X-1	[7]	147	Checksum	[9]
24	Max. Acc. Time From CLK @ CL X-1	[7]		Reserved	[9]

NOTES:

[1] Programmed as 128 bytes by the DIMM OEM
[2] Must be programmed to 256 bytes.
[3] High order bit defines redundant addressing: if set (1), highest order RAS# address must be re-sent as highest order CAS# address.
[4] Refer to memory manufacturer's datasheet
[5] MSb is Self Refresh flag. If set (1), assembly supports self refresh.
[6] Back-to-back random column addresses.
[7] Field format proposed to JEDEC but not defined as standard at publication time.
[8] Field specified as optional by JEDEC but required by this system.
[9] Compaq usage. This system requires that the DIMM EEPROM have this space available for reads/writes.
[10] Serial # in ASCII format (MSB is 133). Intended as backup identifier in case vender data is invalid.
Can also be used to indicate s/n mismatch and flag system adminstrator of possible system Tampering.
[11] Contains the socket # of the module (first module is "1"). Intended as backup identifier (refer to note [10]).

Figure 3-3 shows the system memory map.



NOTE:

All locations in memory are cacheable. Base memory is always mapped to DRAM. The next 128 KB fixed memory area can, through the north bridge, be mapped to DRAM or to PCI space. Graphics RAM area is mapped to PCI or AGP locations.

[1] D315 model, 1 GB; d325, 2 GB
[2] Area typically less according to need and Setup configuration. Default area is E6100-FFFFFh.

Figure 3–3. System Memory Map

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Chapter 4
SYSTEM SUPPORT

4.1 INTRODUCTION

This chapter covers subjects dealing with basic system architecture and covers the following topics:

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the systems covered in this guide. For detailed information on specific components, refer to the applicable manufacturer's documentation.

4.2 PCI BUS OVERVIEW

NOTE: This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the *PCI Local Bus Specification Revision 2.2.*

These systems implement a 32-bit Peripheral Component Interconnect (PCI) bus (spec. 2.2) operating at 33 MHz. The PCI bus handles address/data transfers through the identification of devices and functions on the bus. A device is typically defined as a component or slot that resides on the PCI bus (although some components such as the IGP and MCP or MCP-2 are organized as multiple devices). A function is defined as the end source or target of the bus transaction. A device may contain one or more functions.

In the standard configuration these systems use a hierarchy of three PCI buses (Figure 4-1). The PCI bus #0 is internal to the chipset components and is not physically accessible. The AGP bus that services the AGP slot is designated as PCI bus #1. All PCI slots reside on PCI bus #2.

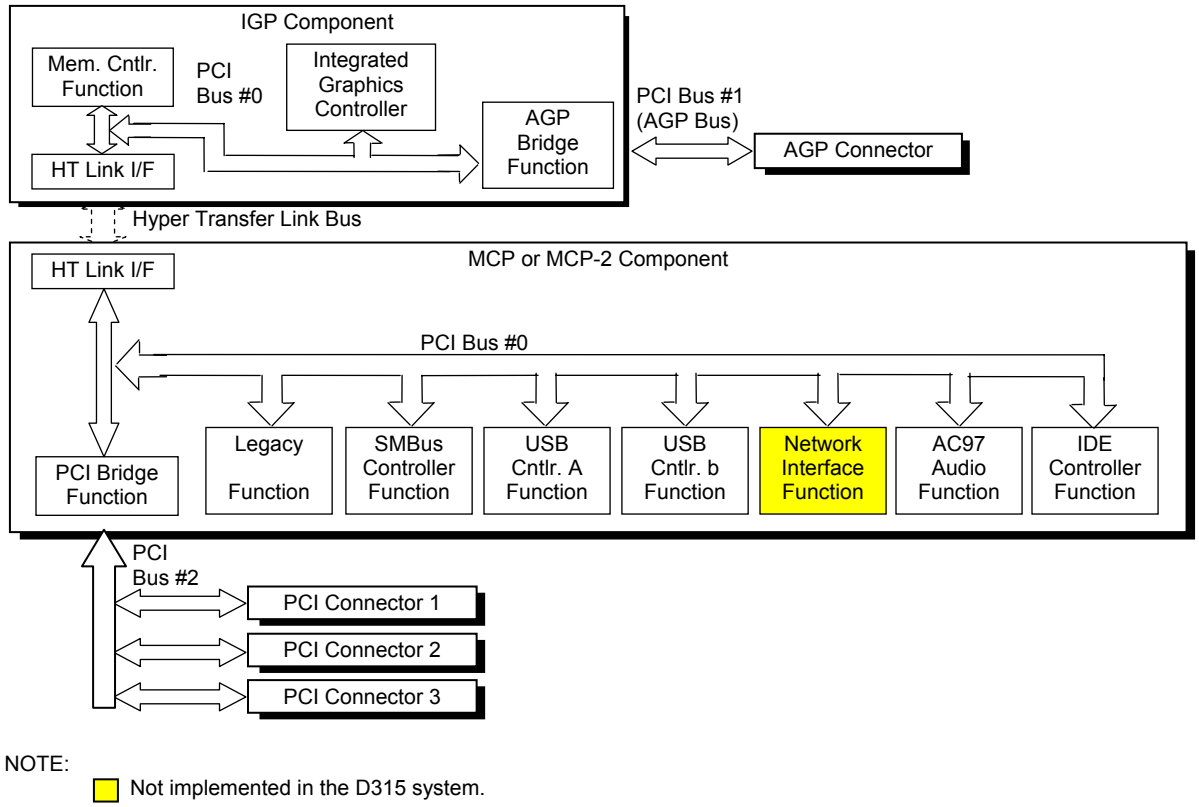


Figure 4-1. PCI Bus Devices and Functions

4.2.1 PCI BUS TRANSACTIONS

The PCI bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is realized during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing. Four types of address cycles can take place on the PCI bus; I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

4.2.1.1 I/O and Memory Cycles

For I/O and memory cycles, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for dword-level addressing and check the AD1,0 lines for burst (linear-incrementing) mode. In burst mode, subsequent data phases are conducted a dword at a time with addressing assumed to increment accordingly (four bytes at a time).

4.2.1.2 Configuration Cycles

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.2) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address register (CONFIG_ADDRESS) at 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data register (CONFIG_DATA) at 0CFCh contains the configuration data.

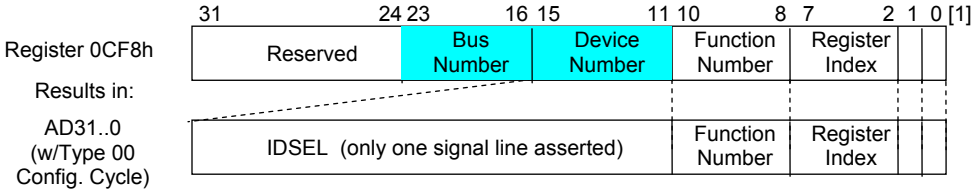
PCI Configuration Address Register
I/O Port 0CF8h, R/W, (32-bit access only)

Bit	Function
31	Configuration Enable 0 = Disabled 1 = Enable
30..24	Reserved - read/write 0s
23..16	Bus Number. Selects PCI bus
15..11	PCI Device Number. Selects PCI device for access
10..8	Function Number. Selects function of selected PCI device.
7..2	Register Index. Specifies config. reg.
1,0	Configuration Cycle Type ID. 00 = Type 0 01 = Type 1

PCI Configuration Data Register
I/O Port 0CFCh, R/W, (8-, 16-, 32-bit access)

Bit	Function
31..0	Configuration Data.

Two types of configuration cycles are used. A Type 0 (zero) cycle is targeted to a device on the PCI bus on which the cycle is running. A Type 1 cycle is targeted to a device on a downstream PCI bus as identified by bus number bits <23..16>. Figure 4-2 shows the configuration cycle format and how the loading of 0CF8h results in a Type 0 configuration cycle on the PCI bus. The Device Number (bits <15..11> determines which one of the AD31..11 lines is to be asserted high for the IDSEL signal, which acts as a "chip select" function for the PCI device to be configured. The function number (CF8h, bits <10..8>) is used to select a particular function within a PCI component.



NOTES:
[1] Bits <1,0> : 00 = Type 0 Cycle, 01 = Type 1 cycle
Type 01 cycle only. Reserved on Type 00 cycle.

Figure 4-2. Configuration Cycle

Table 4-1 shows the standard configuration of device numbers and IDSEL connections for components and slots residing on a PCI bus.

Table 4-1.
PCI Component Configuration Access

PCI Component: Function	PCI Bus #	Device #	Function #	Device ID [4]	IDSEL Wired to: [4]
IGP:					n/a
CPU Host Bridge	0	0	0	01A4h / 01E0h	
Memory Configuration	0	0	1	01Ach / 01EBh	
Memory Addr. Trans. Cntrl.	0	0	2	01ADh / 01EEh	
Miscellaneous Control	0	0	3	01AAh / 01EDh	
AGP Host	0	30	0	01B7h / 01E8h	
Graphics processing unit [1]	1	0	0	01A0h / 01F0h	
AGP slot	1	0	0	[3]	n/a
MCP:					n/a
Legacy LPC Bridge Control	0	1	0	01B2h / 0060h	
SMBus Control	0	1	1	01B4h / 0064h	
USB Controller A	0	2	0	01C2h / 0067h	
USB Controller B	0	2	1	01C2h / 0067h	
USB 2.0 Controller	0	2	2	na / 0068h	
Network interface	0	4	0	[2] / 0066h	
Audio processor		5	0	[2] / [2]	
Audio Codec	0	6	1	01B1h / 006Ah	
Modem Codec (not used)	0	6	0	01C1h / 0069h	
PCI-PCI Bridge	0	8	0	01B8h / 006Ch	
IDE Controller	0	9		01BCh / 006Dh	
PCI Connector 1 (slot 1)	2	6 / 4	[3]	[3]	AD22 / AD20
PCI Connector 2 (slot 2)	2	7 / 9	[3]	[3]	AD23 / AD25
PCI Connector 3 (slot 3)	2	8 / 10	[3]	[3]	AD24 / AD26

NOTES:
All numbers are in decimal unless otherwise indicated.
Vender ID for all functions is 10DEh.
[1] Will not be "visible" to software if an AGP card is installed in the AGP slot.
[2] Not used in this systems.
[3] Determined by installed device.
[4] D315 / d325

The register index (CF8h, bits <7..2>) identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data (Figure 4-3), of which the first 64 bytes comprise the configuration space header.

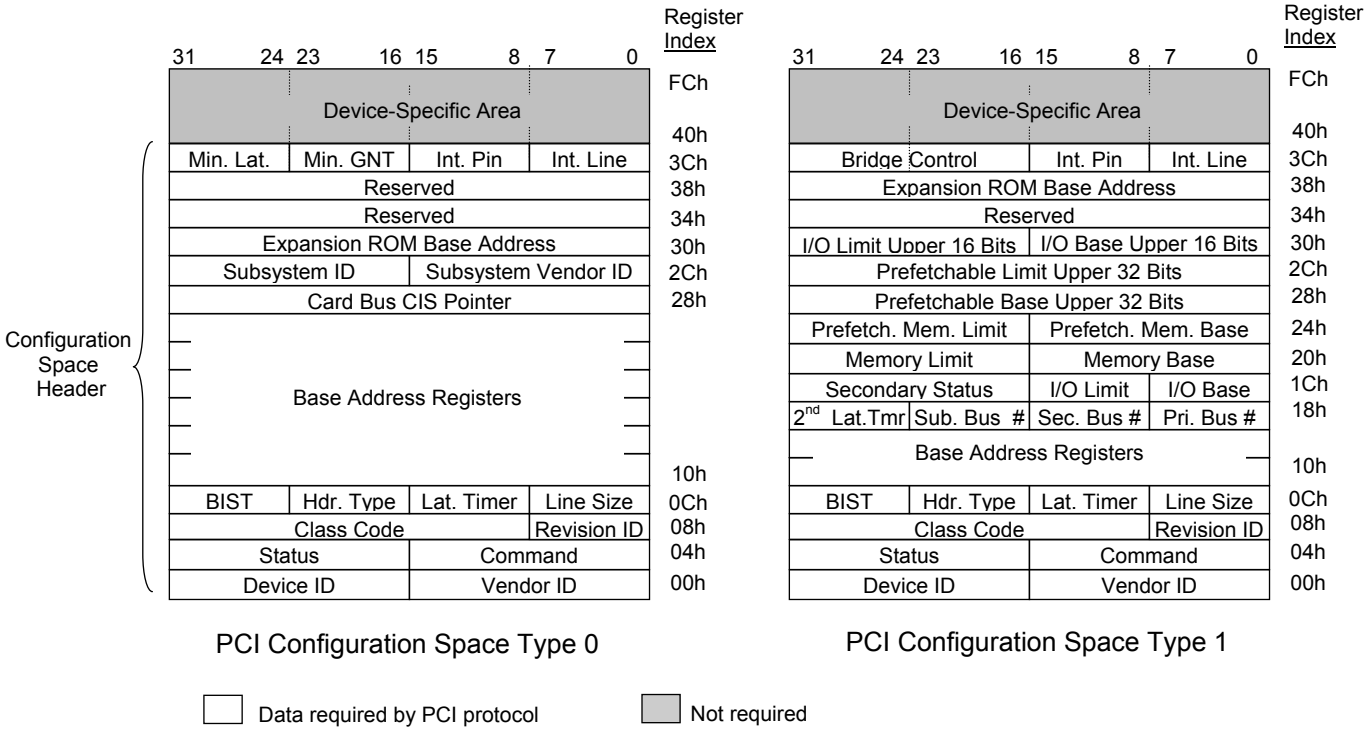


Figure 4-3. PCI Configuration Space Mapping

Each PCI device is identified with a vendor ID (assigned to the vendor by the PCI Special Interest Group) and a device ID (assigned by the vendor). The device and vendor IDs for the devices on the system board are listed in Table 4-2 (**NOTE**: only devices that are implemented in these systems are listed).

4.2.2 PCI BUS MASTER ARBITRATION

The PCI bus supports a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. The Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts its REQ*n* signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNT*n* signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-2 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-2.
PCI Bus Mastering Devices

REQ/GNT Line	Device
REQ0/GNT0	PCI Connector Slot 1
REQ1/GNT1	PCI Connector Slot 2
REQ2/GNT2	PCI Connector Slot 3
GREQ/GGNT	AGP Slot

NOTE:

PCI bus arbitration is based on a round-robin scheme that complies with the fairness algorithm specified by the PCI specification. The bus parking policy allows for the current PCI bus owner (excepting the PCI/ISA bridge) to maintain ownership of the bus as long as no request is asserted by another agent. Note that most CPU-to-DRAM and AGP-to-DRAM accesses can occur concurrently with PCI traffic, therefore reducing the need for the Host/PCI bridge to compete for PCI bus ownership.

4.2.3 OPTION ROM MAPPING

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.4 PCI INTERRUPTS

Eight interrupt signals (INTA- thru INTD-) are available for use by PCI devices. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. For more information on interrupts including PCI interrupt mapping refer to the "System Resources" section 4.4.

4.2.5 PCI POWER MANAGEMENT SUPPORT

This system complies with the PCI Power Management Interface Specification (rev 1.0). The PCI Power Management Enable (PME-) signal is supported by the chipset and allows compliant PCI and AGP peripherals to initiate the power management routine.

4.2.6 PCI SUB-BUSSES

The chipset implements two data busses that are supplementary in operation to the PCI bus:

4.2.6.1 Hyper Transfer Link Bus

The NVidia NForce chipset implements a Hyper Transfer Link bus between the IGP and the MCP components. This bus operates at 800 MHz and is transparent to software and not accessible for expansion purposes.

4.2.6.2 LPC Bus

The MCP and MCP-2 implements a Low Pin Count (LPC) bus for handling transactions to and from the LPC47B367 Super I/O Controller as well as the BIOS ROM. The LPC bus transfers data a nibble (4 bits) at a time at a 33-MHz and is generally transparent in operation. The only consideration required of the LPC bus is during the configuration of DMA channel modes (see section 4.4.3 "DMA").

4.2.7 PCI CONNECTOR

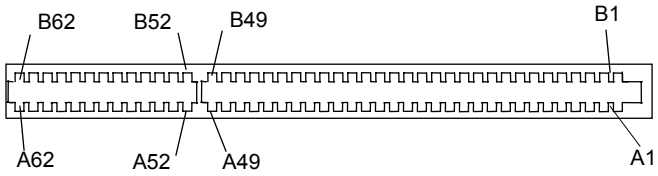


Figure 4-4. PCI Bus Connector (32-Bit Type)

Table 4-3.
PCI Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	32	AD17	AD16
02	TCK	+12 VDC	33	C/BE2-	+3.3 VDC
03	GND	TMS	34	GND	FRAME-
04	TDO	TDI	35	IRDY-	GND
05	+5 VDC	+5 VDC	36	+3.3 VDC	TRDY-
06	+5 VDC	INTA-	37	DEVSEL-	GND
07	INTB-	INTC-	38	GND	STOP-
08	INTD-	+5 VDC	39	LOCK-	+3.3 VDC
09	PRSNT1-	Reserved	40	PERR-	SDONE n
10	RSVD	+5 VDC	41	+3.3 VDC	SBO-
11	PRSNT2-	Reserved	42	SERR-	GND
12	GND	GND	43	+3.3 VDC	PAR
13	GND	GND	44	C/BE1-	AD15
14	RSVD	+3.3 AUX	45	AD14	+3.3 VDC
15	GND	RST-	46	GND	AD13
16	CLK	+5 VDC	47	AD12	AD11
17	GND	GNT-	48	AD10	GND
18	REQ-	GND	49	GND	AD09
19	+5 VDC	PME-	50	Key	Key
20	AD31	AD30	51	Key	Key
21	AD29	+3.3 VDC	52	AD08	C/BE0-
22	GND	AD28	53	AD07	+3.3 VDC
23	AD27	AD26	54	+3.3 VDC	AD06
24	AD25	GND	55	AD05	AD04
25	+3.3 VDC	AD24	56	AD03	GND
26	C/BE3-	IDSEL	57	GND	AD02
27	AD23	+3.3 VDC	58	AD01	AD00
28	GND	AD22	59	+5 VDC	+5 VDC
29	AD21	AD20	60	ACK64-	REQ64-
30	AD19	GND	61	+5 VDC	+5 VDC
31	+3.3 VDC	AD18	62	+5 VDC	+5 VDC
—	—	—	—	—	—

4.3 AGP BUS OVERVIEW

NOTE: For a detailed description of AGP bus operations refer to the *AGP Interface Specification Rev. 2.0* available at the following AGP forum web site: http://www.agpforum.org/index.htm

The Accelerated Graphics Port (AGP) bus is specifically designed as an economical yet high-performance interface for graphics adapters, especially those designed for 3D operations. The AGP interface is designed to give graphics adapters dedicated pipelined access to system memory for the purpose of off-loading texturing, z-buffering, and alpha blending used in 3D graphics operations. By off-loading a large portion of 3D data to system memory the AGP graphics adapter only requires enough memory for frame buffer (display image) refreshing.

4.3.1 BUS TRANSACTIONS

The operation of the AGP bus is based on the 66-MHz PCI specification but includes additional mechanisms to increase bandwidth. During the configuration phase the AGP bus acts in accordance with PCI protocol. Once graphics data handling operation is initiated, AGP-defined protocols take effect. The AGP graphics adapter acts generally as the AGP master, but can also behave as a "PCI" target during fast writes from the PCI bus controller.

Key differences between the AGP interface and the PCI interface are as follows:

- Address phase and associated data transfer phase are disconnected transactions. Addressing and data transferring occur as contiguous actions on the PCI bus. On the AGP bus a request for data and the transfer of data may be separated by other operations.
- Commands on the AGP bus specify system memory accesses only. Unlike the PCI bus, commands involving I/O and configuration are not required or allowed. The system memory address space used in AGP operations is the same linear space used by PCI memory space commands, but is further specified by the graphics address re-mapping table (GART) of the north bridge component.
- Data transactions on the AGP bus involve eight bytes or multiples of eight bytes. The AGP memory addressing protocol uses 8-byte boundaries as opposed to PCI's 4-byte boundaries. If a transfer of less than eight bytes is needed, the remaining bytes are filled with arbitrary data that is discarded by the target.
- Pipelined requests are defined by length or size on the AGP bus. The PCI bus defines transfer lengths with the FRAME- signal.

There are two basic types of transactions on the AGP bus: data requests (addressing) and data transfers. These actions are separate from each other.

4.3.1.1 Data Request

Requesting data is accomplished in one of two ways; either multiplexed addressing (using the AD lines for addressing/data) or demultiplexed ("sideband") addressing (using the SBA lines for addressing only and the AD lines for data only). Even though there are only eight SBA lines (as opposed to the 32 AD lines) sideband addressing maximizes efficiency and throughput by allowing the AD lines to be exclusively used for data transfers. Sideband addressing occurs at the same rate (1X, 2X, 4X, or 8X) as data transfers. The differences in rates will be discussed in the next section describing data transfers. Note also that sideband addressing is limited to 48 bits (address bits 48-63 are assumed zero). The IGP component supports both SBA and AD addressing, but the method and rate is selected by the AGP graphics adapter.

4.3.1.2 Data Transfers

Data transfers use the AD lines and occur as the result of data requests described previously. Each transaction resulting from a request involves at least eight bytes, requiring the 32 AD lines to handle at least two transfers per request. The AGP v.2.0 specification (used on D315 models) supports three transfer rates: 1X, 2X, and 4X. The AGP v3.0 specification (used on d325 models) supports a fourth transfer rate, 8X. Regardless of the rate used, the speed of the bus clock is constant at 66 MHz. The following subsections describe how the use of additional strobe signals makes possible higher transfer rates.

AGP 1X Transfers

During a AGP 1X transfer the 66-MHz CLK signal is used to qualify the control and data signals. Each 4-byte data transfer is synchronous with one CLK cycle so it takes two CLK cycles for a minimum 8-byte transfer (Figure 4-5 shows two 8-byte transfers). The GNT- and TRDY- signals retain their traditional PCI functions. The ST0..3 signals are used for priority encoding, with "000" for low priority and "001" indicating high priority. The signal level for AGP 1X transfers may be 3.3 or 1.5 VDC.

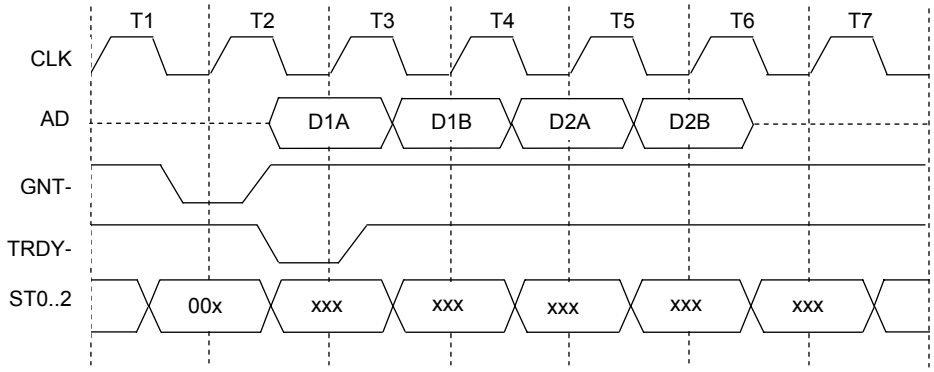


Figure 4-5. AGP 1X Data Transfer (Peak Transfer Rate: 266 MB/s)

AGP 2X Transfers

During AGP 2X transfers, clocking is basically the same as in 1X transfers except that the 66-MHz CLK signal is used to qualify only the control signals. The data bytes are latched by an additional strobe (AD_STBx) signal so that an 8-byte transfer occurs in one CLK cycle (Figure 4-6). The first four bytes (DnA) are latched by the receiving agent on the falling edge of AD_STBx and the second four bytes (DnB) are latched on the rising edge of AD_STBx. The signal level for AGP 2X transfers may be 3.3 or 1.5 VDC.

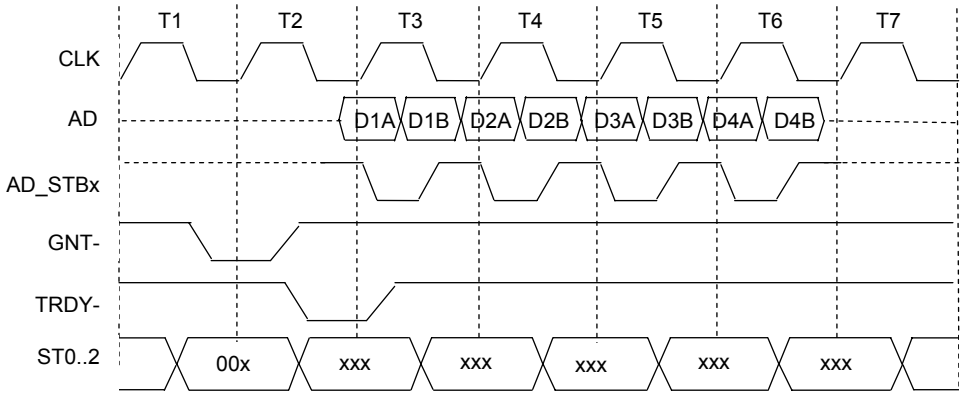


Figure 4-6. AGP 2X Data Transfer (Peak Transfer Rate: 532 MB/s)

AGP 4X Transfers

The AGP 4X transfer rate allows sixteen bytes of data to be transferred in one clock cycle. As in 2X transfers the 66-MHz CLK signal is used only for qualifying control signals while strobe signals are used to latch each 4-byte transfer on the AD lines. As shown in Figure 4-7, 4-byte block DnA is latched by the falling edge of AD_STBx while DnB is latched by the falling edge of AD_STBx-. The signal level for AGP 4X transfers is 1.5 VDC.

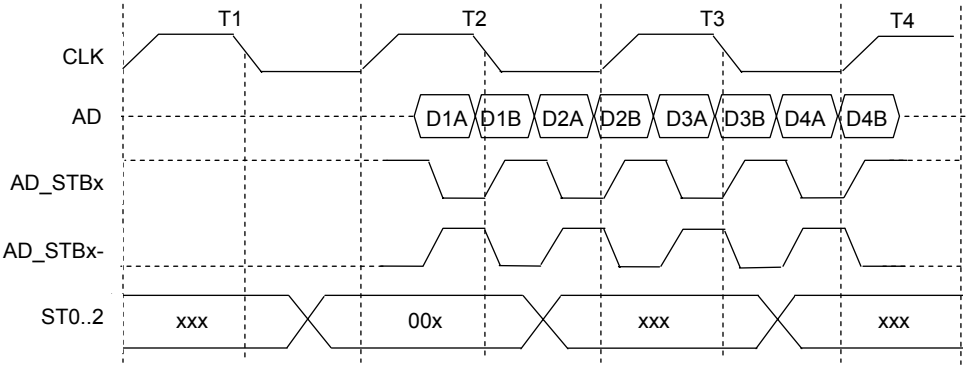


Figure 4-7. AGP 4X Data Transfer (Peak Transfer Rate: 1064 MB/s)

AGP 8X Transfers

The AGP 8X transfer rate (supported on d325 models only) allows 32 bytes of data to be transferred in one clock cycle. As with the other transfer rates the 66-MHz CLK signal is used only for qualifying control signals while strobe signals are used to latch each 4-byte transfer on the AD lines. As shown in Figure 4-8, 4-byte block DnA is latched by the falling edge of AD_STBx while DnB is latched by the falling edge of AD_STBx-. The signal level for AGP 8X transfers can be 0.8 or 1.5 VDC.

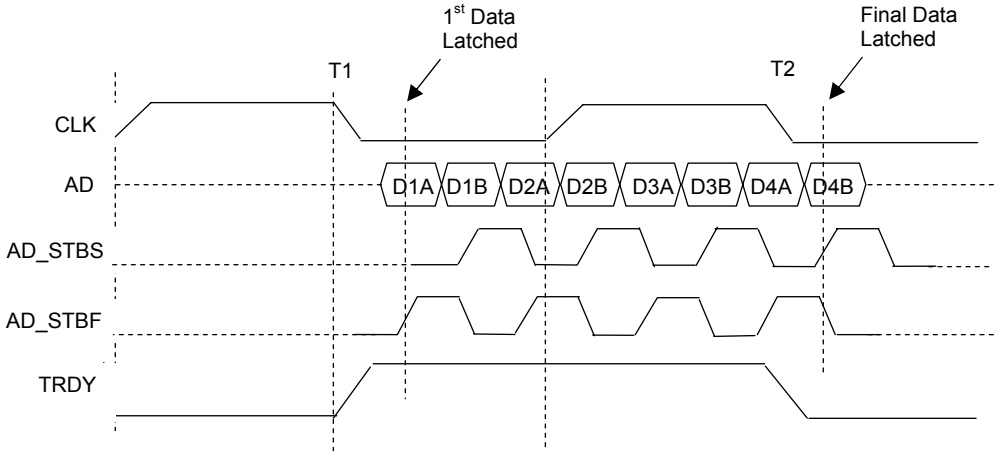


Figure 4-8. AGP 8X Data Transfer (Peak Transfer Rate: 2128 MB/s)

4.3.2 AGP CONNECTOR

Figure 4-8 shows the system's keyed AGP connector that accepts only 1.5-volt AGP adapters. The pin out is listed in Table 4-4.

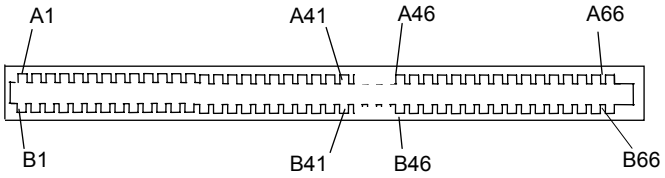


Figure 4-9. AGP Bus Connector

Table 4-4.
AGP Bus Connector Pinout

Pin	A Signal	B Signal	Pin	A Signal	B Signal	Pin	A Signal	B Signal
01	+12 VDC	OVRCNT-	23	GND	GND	45	VDD3	VDD3
02	Type Det-	VDD	24	NC	VDD3 Aux	46	TRDY-	DEVSEL-
03	NC	VDD	25	VDD3	VDD3	47	STOP-	VDDQ
04	USBN	USBP	26	PAD30	PAD31	48	PME-	PERR-
05	GND	GND	27	PAD28	PAD29	49	GND	GND
06	INTA-	INTB-	28	VDD3	VDD3	50	PAR	SERR-
07	RESET	CLK	29	PAD26	PAD27	51	PAD15	CBE1-
08	GNT-	REQ-	30	PAD24	PAD25	52	VDDQ	VDDQ
09	VDD3	VDD3	31	GND	GND	53	PAD13	PAD14
10	ST1	ST0	32	AD_STB1-	AD_STB1	54	PAD11	PAD12
11	NC	ST2	33	CBE3-	PAD23	55	GND	GND
12	PIPE-	RBF-	34	VDDQ	VDDQ	56	PAD09	PAD10
13	GND	GND	35	PAD22	PAD21	57	CBE0-	PAD08
14	WBF-	NC	36	PAD20	PAD19	58	VDDQ	VDDQ
15	SBA1	SBA0	37	GND	GND	59	AD_STB0-	AD_STB0
16	VDD3	VDD3	38	PAD18	PAD17	60	PAD06	PAD07
17	SBA3	SBA2	39	PAD16	CBE2-	61	GND	GND
18	SB_STB-	SB_STB	40	VDDQ	VDDQ	62	PAD04	PAD05
19	GND	GND	41	FRAME-	IRDY-	63	PAD02	PAD03
20	SBA5	SBA4	42	NC	VDD3 Aux	64	VDDQ	VDDQ
21	SBA7	DBA6	43	GND	GND	65	PAD00	PAD01
22	NC	NC	44	NC	NC	66	VREFGC	VREFCG

NOTES:
NC = Not connected
VDDQ = 3.3 VDC when TYPE DET- is left open by AGP 1X/2X card.
VDDQ = 1.5 VDC when TYPE DET- is grounded by AGP 4X card.
= Keyed spaces on 1.5-volt AGP connector.

4.4 SYSTEM RESOURCES

This section describes the availability and basic control of major subsystems, otherwise known as resource allocation or simply "system resources." System resources are provided on a priority basis through hardware interrupts and DMA requests and grants.

4.4.1 INTERRUPTS

The microprocessor uses two types of hardware interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor, although it may be inhibited by hardware or software means external to the microprocessor.

4.4.1.1 Maskable Interrupts

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-H (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR-) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

Figure 4-9 shows the routing of PCI and ISA interrupts. Most IRQs are routed through the I/O controller, which contains a serializing function. A serialized interrupt stream is applied to the MCP component.

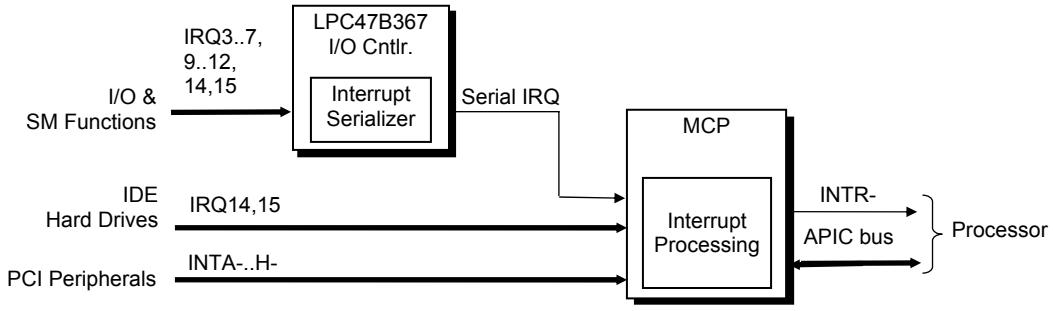


Figure 4-10. Maskable Interrupt Processing, Block Diagram

Interrupts may be processed in one of two modes (selectable through the F10 Setup utility):

- 8259 mode
- APIC mode

8259 Mode

The 8259 mode handles interrupts IRQ0-IRQ15 in the legacy (AT-system) method using 8259-equivalent logic. Table 4-5 lists the standard source configuration for maskable interrupts and their priorities in 8259 mode. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

Table 4-5.
Maskable Interrupt Priorities and Assignments

Priority	Signal Label	Source (Typical)
1	IRQ0	Interval timer 1, counter 0
2	IRQ1	Keyboard
3	IRQ8-	Real-time clock
4	IRQ9	Unused
5	IRQ10	PCI devices/slots
6	IRQ11	Audio codec
7	IRQ12	Mouse (PS/2)
8	IRQ13	Coprocessor (math)
9	IRQ14	Primary IDE controller
10	IRQ15	Secondary IDE I/F controller
11	IRQ3	Serial port (COM2)
12	IRQ4	Serial port (COM1)
13	IRQ5	Network interface controller
14	IRQ6	Diskette drive controller
15	IRQ7	Parallel port (LPT1)
--	IRQ2	NOT AVAILABLE (Cascade from interrupt controller 2)

APIC Mode

The Advanced Programmable Interrupt Controller (APIC) mode provides enhanced interrupt processing with the following advantages:

- Eliminates the processor's interrupt acknowledge cycle by using a separate (APIC) bus
- Programmable interrupt priority
- Additional interrupts (total of 24)

The APIC mode accommodates five PCI interrupt signals (INTA-..INTE-) for use by PCI devices. The PCI interrupts are evenly distributed to minimize latency and wired as follows:

MCP Int. Cntlr.		PCI Slot 1	PCI Slot 2	PCI Slot 3	AGP Slot
INTA-	Wired to	INTA-	INTD-	INTC-	INTB-
INTB-		INTB-	INTA-	INTD-	—
INTC-		INTC-	INTB-	INTA-	—
INTD-		INTD-	INTC-	INTB-	—
INTE-		—	—	—	INTA-

NOTE:
Internal functions of the MCP (USB, MAC, SMBus, Audio, IDE controllers) use INTA-.

The PCI interrupts can be configured by PCI Configuration Registers 60h..63h to share the standard ISA interrupts (IRQn).

NOTE: The APIC mode is supported by the Windows NT, Windows 2000, and Windows XP operating systems. Systems running the Windows 95 or 98 operating system will need to run in 8259 mode.

Maskable interrupt processing is controlled and monitored through standard AT-type I/O-mapped registers. These registers are listed in Table 4-6.

Table 4-6.
Maskable Interrupt Control Registers

I/O Port	Register
020h	Base Address, Int. Cntlr. 1
021h	Initialization Command Word 2-4, Int. Cntlr. 1
0A0h	Base Address, Int. Cntlr. 2
0A1h	Initialization Command Word 2-4, Int. Cntlr. 2

The initialization and operation of the interrupt control registers follows standard AT-type protocol.

4.4.1.2 Non-Maskable Interrupts

Non-maskable interrupts cannot be masked (inhibited) within the microprocessor itself but may be maskable by software using logic external to the microprocessor. There are two non-maskable interrupt signals: the NMI- and the SMI-. These signals have service priority over all maskable interrupts, with the SMI- having top priority over all interrupts including the NMI-.

NMI- Generation

The Non-maskable Interrupt (NMI-) signal can be generated by one of the following actions:

- Parity errors detected on a PCI bus (activating SERR- or PERR-).
- Microprocessor internal error (activating IERRA or IERRB)

The SERR- and PERR- signals are routed through the MCP or MCP-2 component, which in turn activates the NMI to the microprocessor.

The NMI Status Register at I/O port 061h contains NMI source and status data as follows:

NMI Status Register 61h

Bit	Function
7	NMI Status: 0 = No NMI from system board parity error. 1 = NMI requested, read only
6	IOCHK- NMI: 0 = No NMI from IOCHK- 1 = IOCHK- is active (low), NMI requested, read only
5	Interval Timer 1, Counter 2 (Speaker) Status
4	Refresh Indicator (toggles with every refresh)
3	IOCHK- NMI Enable/Disable: 0 = NMI from IOCHK- enabled 1 = NMI from IOCHK- disabled and cleared (R/W)
2	System Board Parity Error (PERR/SERR) NMI Enable: 0 = Parity error NMI enabled 1 = Parity error NMI disabled and cleared (R/W)
1	Speaker Data (R/W)
0	Inteval Timer 1, Counter 2 Gate Signal (R/W) 0 = Counter 2 disabled 1 = Counter 2 enabled

Functions not related to NMI activity.

After the active NMI has been processed, status bits <7> or <6> are cleared by pulsing bits <2> or <3> respectively.

The NMI Enable Register (070h, <7>) is used to enable/disable the NMI signal. Writing 80h to this register masks generation of the NMI-. Note that the lower six bits of register at I/O port 70h affect RTC operation and should be considered when changing NMI- generation status.

SMI- Generation

The SMI- (System Management Interrupt) is typically used for power management functions. When power management is enabled, inactivity timers are monitored. When a timer times out, SMI- is asserted and invokes the microprocessor's SMI handler. The SMI handler works with the APM BIOS to service the SMI- according to the cause of the timeout.

Although the SMI- is primarily used for power management the interrupt is also employed for the QuickLock/QuickBlank functions as well.

4.4.2 DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is a method by which a device accesses system memory without involving the microprocessor. Although the DMA method has been traditionally used to transfer blocks of data to or from an ISA I/O device, PCI devices may also use DMA operation as well. The DMA method reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

NOTE: This section describes DMA in general. For detailed information regarding DMA operation, refer to the data manual for the Intel MCP component.

The MCP component includes the equivalent of two 8237 DMA controllers cascaded together to provide eight DMA channels, each (excepting channel 4) configurable to a specific device. Table 4-7 lists the default configuration of the DMA channels.

Table 4-7.
Default DMA Channel Assignments

DMA Channel	Device ID
Controller 1 (byte transfers)	
0	Spare
1	Audio subsystem
2	Diskette drive
3	Parallel port
Controller 2 (word transfers)	
4	Cascade for controller 1
5	Spare
6	Spare
7	Spare

All channels in DMA controller 1 operate at a higher priority than those in controller 2. Note that channel 4 is not available for use other than its cascading function for controller 1. The DMA controller 2 can transfer words only on an even address boundary. The DMA controller and page register define a 24-bit address that allows data transfers within the address space of the CPU.

In addition to device configuration, each channel can be configured (through PCI Configuration Registers) for one of two modes of operation:

- LPC DMA
- PC/PCI DMA

The LPC DMA mode uses the LPC bus to communicate DMA channel control and is implemented for devices using DMA through the LPC47B367 I/O controller such as the diskette drive controller.

The PC/PCI DMA mode uses the REQ#/GNT# signals to communicate DMA channel control and is used by PCI expansion devices.

The DMA logic is accessed through two types of I/O mapped registers; page registers and controller registers.

4.4.2.1 DMA Page Registers

The DMA page register contains the eight most significant bits of the 24-bit address and works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 4-8 lists the page register port addresses.

Table 4-8.
DMA Page Register Addresses

DMA Channel	Page Register I/O Port
Controller 1 (byte transfers)	
Ch 0	087h
Ch 1	083h
Ch 2	081h
Ch 3	082h
Controller 2 (word transfers)	
Ch 4	n/a
Ch 5	08Bh
Ch 6	089h
Ch 7	08Ah
Refresh	08Fh [see note]

NOTE:
The DMA memory page register for the refresh channel must be programmed with 00h for proper operation.

The memory address is derived as follows:

24-Bit Address - Controller 1 (Byte Transfers)

8-Bit Page Register	8-Bit DMA Controller
A23..A16	A15..A00

24-Bit Address - Controller 2 (Word Transfers)

8-Bit Page Register	16-Bit DMA Controller
A23..A17	A16..A01, (A00 = 0)

Note that address line A16 from the DMA memory page register is disabled when DMA controller 2 is selected. Address line A00 is not connected to DMA controller 2 and is always 0 when word-length transfers are selected.

By not connecting A00, the following applies:

- The size of the the block of data that can be moved or addressed is measured in 16-bits (words) rather than 8-bits (bytes).
- The words must always be addressed on an even boundary.

DMA controller 1 can move up to 64 Kbytes of data per DMA transfer. DMA controller 2 can move up to 64 Kwords (128 Kbytes) of data per DMA transfer. Word DMA operations are only possible between 16-bit memory and 16-bit peripherals.

The RAM refresh is designed to perform a memory read cycle on each of the 512 row addresses in the DRAM memory space. Refresh operations are used to refresh memory on the 32-bit memory bus and the ISA bus. The refresh address is provided on lines SA00 through SA08. Address lines LA23..17, SA18,19 are driven low.

The remaining address lines are in an undefined state during the refresh cycle. The refresh operations are driven by a 69.799-KHz clock generated by Interval Timer 1, Counter 1. The refresh rate is 128 refresh cycles in 2.038 ms.

4.4.2.2 DMA Controller Registers

Table 4-9 lists the DMA Controller Registers and their I/O port addresses. Note that there is a set of registers for each DMA controller.

Table 4-9.
DMA Controller Registers

Register	Controller 1	Controller 2	R/W
Status	008h	0D0h	R
Command	008h	0D0h	W
Mode	00Bh	0D6h	W
Write Single Mask Bit	00Ah	0D4h	W
Write All Mask Bits	00Fh	0DEh	W
Software DRQx Request	009h	0D2h	W
Base and Current Address - Ch 0	000h	0C0h	W
Current Address - Ch 0	000h	0C0h	R
Base and Current Word Count - Ch 0	001h	0C2h	W
Current Word Count - Ch 0	001h	0C2h	R
Base and Current Address - Ch 1	002h	0C4h	W
Current Address - Ch 1	002h	0C4h	R
Base and Current Word Count - Ch 1	003h	0C6h	W
Current Word Count - Ch 1	003h	0C6h	R
Base and Current Address - Ch 2	004h	0C8h	W
Current Address - Ch 2	004h	0C8h	R
Base and Current Word Count - Ch 2	005h	0CAh	W
Current Word Count - Ch 2	005h	0CAh	R
Base and Current Address - Ch 3	006h	0CCh	W
Current Address - Ch 3	006h	0CCh	R
Base and Current Word Count - Ch 3	007h	0CEh	W
Current Word Count - Ch 3	007h	0CEh	R
Temporary (Command)	00Dh	0DAh	R
Reset Pointer Flip-Flop (Command)	00Ch	0D8h	W
Master Reset (Command)	00Dh	0DAh	W
Reset Mask Register (Command)	00Eh	0DCh	W

4.5 SYSTEM CLOCK DISTRIBUTION

This system uses clock synthesizers in the IGP and the MCP or MCP-2 components. A 14.31818-MHz crystal provides an input for clock circuits of the MCP.

Table 4-10 lists clock signals that are distributed between system board components. Frequencies that are used only internally in chips and components are not listed.

Table 4-10.
Clock Generation and Distribution

Frequncy	Source	Destination or Function
266 MHz	IGP	AGP feedback clock
200 MHz	IGP/MCP	Hyper Transport Bus clock
133 / 166 MHz [1]	IGP	Processor, DIMM sockets
66 MHz	IGP	AGP slot
33 MHz	IGP	APIC clock
32.768 MHz	Crystal	MCP, super I/O
25 MHz	Crystal	NIC PHY
25 MHz	NIC PHY	MCP
24.576 MHz	Crystal	Audio codec
16 MHz	IGP	APIC clock
14.31818 MHz	Crystal	MCP
14.31818 MHz	MCP	Clock buffer
14.31818 MHz	Clock buffer	IGP, super I/O
12.288 MHz	Audio codec	AC link clock

NOTE:
[1] D315 / d325

These systems uses the spread-spectrum feature of the IGP component. This feature allows BIOS to set a down spread (0.9 % on the D315, 0.5 % on the d325) to lower the possible effects of high frequency EMI. Clocks affected by the spread include those used by the processor, memory, and AGP.

4.6 REAL-TIME CLOCK AND CONFIGURATION MEMORY

The Real-time clock (RTC) and configuration memory (also referred to as "CMOS") functions are provided by the MCP component and is MC146818-compatible. As shown in the following figure, the MCP component provides 256 bytes of battery-backed RAM divided into two 128-byte configuration memory areas. The RTC uses the first 14 bytes (00-0Dh) of the standard memory area. All locations of the standard memory area (00-7Fh) can be directly accessed using conventional OUT and IN assembly language instructions through I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call.

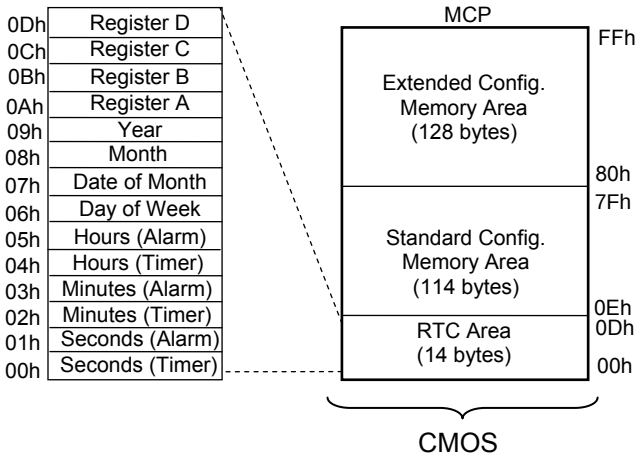


Figure 4-11. Configuration Memory Map

A lithium 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. The battery is located in a battery holder on the system board and has a life expectancy of about three years. When the battery has expired it is replaced with a Renata CR2032 or equivalent 3-VDC lithium battery.

4.6.1 CLEARING CMOS

The contents of configuration memory (including the Power-On Password) can be cleared by the following procedure:

1. Turn off the unit and disconnect the AC power cord from the outlet and/or system unit.
2. Remove the chassis hood (cover) and insure that no LEDs on the system board are illuminated.
3. On the JBAT1 header, move the jumper from pins 1 and 2 to pins 2 and 3. Leave the jumper on pins 2 and 3 for about 5 seconds. This action will ground the battery input to the CMOS circuitry.
4. Replace the jumper onto pins 1 and 2.
5. Replace the chassis hood (cover).
6. Reconnect the AC power cord to the outlet and/or system unit and reboot the system.

To clear **only** the Power-On Password refer to section 4.7.1.1.

4.6.2 CMOS ARCHIVE AND RESTORE

During the boot process the BIOS saves a copy of CMOS to the flash ROM. If the system becomes unusable, the last good copy of CMOS can be recalled using the power-override function as follows:

1. With the unit powered down, press and release the power button to initiate the boot sequence.
2. Immediately after releasing the power button, press it again and hold (typically at least four seconds) until the unit powers off again. This action will be recorded as a power button override event.
3. Press and release the power button once more, initiating the boot sequence that should detect the occurrence of an override event and load the backup copy of CMOS, allowing the system to boot.

4.6.3 STANDARD CMOS LOCATIONS

Table 4-11 and the following paragraphs describe standard configuration memory locations 0Ah-3Fh. These locations are accessible through using OUT/IN assembly language instructions using port 70/71h or BIOS function INT15, AX=E823h.

Table 4-11.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-time clock	24h	System board ID
0Eh	Diagnostic status	25h	System architecture data
0Fh	System reset code	26h	Auxiliary peripheral configuration
10h	Diskette drive type	27h	Speed control external drive
11h	Reserved	28h	Expanded/base mem. size, IRQ12
12h	Hard drive type	29h	Miscellaneous configuration
13h	Security functions	2Ah	Hard drive timeout
14h	Equipment installed	2Bh	System inactivity timeout
15h	Base memory size, low byte/KB	2Ch	Monitor timeout, Num Lock Cntrl
16h	Base memory size, high byte/KB	2Dh	Additional flags
17h	Extended memory, low byte/KB	2Eh-2Fh	Checksum of locations 10h-2Dh
18h	Extended memory, high byte/KB	30h-31h	Total extended memory tested
19h	Hard drive 1, primary controller	32h	Century
1Ah	Hard drive 2, primary controller	33h	Miscellaneous flags set by BIOS
1Bh	Hard drive 1, secondary controller	34h	International language
1Ch	Hard drive 2, secondary controller	35h	APM status flags
1Dh	Enhanced hard drive support	36h	ECC POST test single bit
1Eh	Reserved	37h-3Fh	Power-on password
1Fh	Power management functions	40-FFh	Feature Control/Status

NOTES:
Assume unmarked gaps are reserved.
Higher locations (>3Fh) contain information that should be accessed using the INT15, AX=E845h BIOS function (refer to Chapter 8 for BIOS function descriptions).

4.7 SYSTEM MANAGEMENT

This section describes functions having to do with security, power management, temperature, and overall status. These functions are handled by hardware and firmware (BIOS) and generally configured through the Setup utility.

4.7.1 SECURITY FUNCTIONS

This system includes various features that provide different levels of security. Note that this subsection describes **only the hardware functionality** (including that supported by Setup) and does not describe security features that may be provided by the operating system and application software.

4.7.1.1 Power-On Password

This system includes a power-on password, which may be enabled or disabled (cleared) through a jumper on the system board. The password is stored in configuration memory (CMOS) and if enabled and then forgotten will require that either the password be cleared (preferable solution and described below) or the entire CMOS be cleared (refer to section 4.6).

To clear only the password, use the following procedure:

1. Turn off the system and disconnect the AC power cord from the outlet and/or system unit.
2. Remove the cover (hood) as described in the appropriate *User Guide* or *Service Reference Guide*. Insure that any system board LEDs are off (not illuminated).
3. Locate the password clear header labeled JCMOS1 and move the jumper from pins 1 and 2 to pins 2 and 3.
4. Replace the cover.
5. Re-connect the AC power cord to the AC outlet and/or system unit.
6. Turn on the system. The POST routine will clear and disable the password.
7. To re-enable the password feature, repeat steps 1-6, replacing the jumper on pins 1 and 2 of header JCMOS1.

4.7.1.2 Setup Password

The Setup utility may be configured to be always changeable or changeable only by entering a password. The password is held on CMOS and, if forgotten, will require that CMOS be cleared (refer to section 4.6).

4.7.1.3 Cable Lock Provision

These systems include a chassis cutout (on the rear panel) for the attachment of a cable lock mechanism.

4.7.1.4 I/O Interface Security

The serial, parallel, USB, and diskette interfaces may be disabled individually through the Setup utility to guard against unauthorized access to a system. In addition, the ability to write to or boot from a removable media drive (such as the diskette drive) may be enabled through the Setup utility. The disabling of the serial, parallel, and diskette interfaces are a function of the LPC47B367 I/O controller. The USB ports are controlled through the MCP.

4.7.2 POWER MANAGEMENT

This system provides baseline hardware support of ACPI- and APM-compliant firmware and software. Key power-consuming components (processor, chipset, I/O controller, and fan) can be placed into a reduced power mode either automatically or by user control. The system can then be brought back up ("wake-up") by events defined by the ACPI specification. The ACPI wake-up events supported by this system are listed as follows:

ACPI Wake-Up Event	System Wakes From
Power Button	Suspend or soft-off
RTC Alarm	Suspend or soft-off
Wake On LAN (w/NIC)	Suspend or soft-off
PME	Suspend or soft-off
USB	Suspend only
Keyboard	Suspend only
Mouse	Suspend only

4.7.3 SYSTEM STATUS

These systems provide a visual indication of system boot and ROM flash status through the keyboard LEDs and operational status using bi-colored power and hard drive activity LEDs as indicated in Tables 4-12 and 4-13 respectively.

NOTE: The LED indications listed in Table 4-13 are valid only for PS/2-type keyboards. A USB keyboard will not provide LED status for the listed events, although audible (beep) indications will occur.

Table 4-12.
System Boot/ROM Flash Status LED Indications

Event	NUM Lock LED	CAPs Lock LED	Scroll Lock LED
System memory failure [1]	Blinking	Off	Off
Graphics controller failure [2]	Off	Blinking	Off
System failure prior to graphics cntlr. initialization [3]	Off	Off	Blinking
ROMPAQ diskette not present, faulty, or drive prob.	On	Off	Off
Password prompt	Off	On	Off
Invalid ROM detected - flash failed	Blinking [4]	Blinking [4]	Blinking [4]
Keyboard locked in network mode	Blinking [5]	Blinking [5]	Blinking [5]
Successful boot block ROM flash	On [6]	On [6]	On [6]

NOTES:

[1] Accompanied by 1 short, 2 long audio beeps
[2] Accompanied by 1 long, 2 short audio beeps
[3] Accompanied by 2 long, 1 short audio beeps
[4] All LEDs will blink in sync twice, accompanied by 1 long and three short audio beeps
[5] LEDs will blink in sequence (NUM Lock, then CAPs Lock, then Scroll Lock)
[6] Accompanied by rising audio tone.

Table 4-13.
System Operational Status LED Indications

System Status	D315 Power LED	d325 Power LED
S0: System on (normal operation)	Steady green	Steady green
S1: Suspend	Blinks green @ .5 Hz	Blinks green @ .5 Hz
S3: Suspend to RAM	Blinks green @ .5 Hz	Blinks green @ .5 Hz
S4: Suspend to disk	Off	Off
S5: Soft off	Off	Off
Processor not seated or installed	Steady red	Steady red
CPU thermal shutdown	See note [1]	See note [1]
No memory installed	Blinks red @ 2 Hz	Blinks red @ 2 Hz
Memory error	na	See note [2]
ROM flashing	See note [3]	See note [3]
Video error	na	See note [4]
PCA failure	na	See note [5]
Invalid ROM checksum error	na	See note [6]
System off	Off	Off

NOTE:

For both systems, HD LED is on (green) during hrd rive activity, off at all other times.
[1] Sequence; blinks red every second for 2 seconds, then off for two seconds.
[2] Sequence; blinks red five times in five seconds followed by two-second pause.
[3] Steady red when flashing ROM, then blinks green every second indicating user can restart.
[4] Sequence; blinks red six times in six seconds followed by two-second pause.
[5] Sequence; blinks red seven times in seven seconds followed by two-second pause.
[6] Sequence; blinks red eight times in eight seconds followed by two-second pause.

4.7.4 THERMAL SENSING AND COOLING

These systems feature variable-speed fans that are controlled through temperature sensing logic on the system board and/or in the power supply. Typical cooling conditions include the following:

1. Normal – Low fan speed.
2. Hot processor – ASIC directs Speed Control logic to increase speed of fan(s).
3. Hot power supply – Power supply increases speed of fan(s).
4. Sleep state – Fan(s) turned off. Hot processor or power supply will result in starting fan(s).

High and low thermal parameters are programmed into the ASIC by BIOS during POST. If the high thermal parameter is reached then the fan(s) will be turned on full speed and the Therm- signal will be asserted.

The system board provides connections for a heatsink-mounted CPU fan and a chassis fan, both which complement the power supply fan. The system supports the use of variable-speed fans that are regulated according to the temperature measured by an AMD1030 temperature controller.

4.7.4.1 Cooling for D315 Models

The temperature controller produces the Fan CMD (which varies from 0 to +2.5 VDC) that is applied to the speed control circuitry of the power supply assembly. The output of the speed control circuitry controls the power supply assembly's internal fan and is also routed back to the system board and, in the default jumper configuration, is applied as the Fan Sink signal to the negative terminal of the connected fans. The default jumper configuration also applies + 5 VDC to the positive terminal of the fans. With the Fan CMD signal being varied from +0.5 to -7 VDC, the chassis and CPU fans will be driven by a voltage from about +5 to +12 VDC, depending on the processor temperature.

In a characteristically warm environment or should the speed regulation circuitry be inadequate or fail it may be desirable to have the fans driven by a constant +12 VDC by configuring both FAN_SEL jumpers to pins 1 and 2.

Note that the power supply assembly fan operates independently of the CPU and chassis fans.

CAUTION: Both FAN_SELn jumpers must have the same configuration (jumpers on the same pins). Different jumper settings (one jumper on pins 1 and 2 and the other jumper on pins 2 and 3) may result in equipment damage.

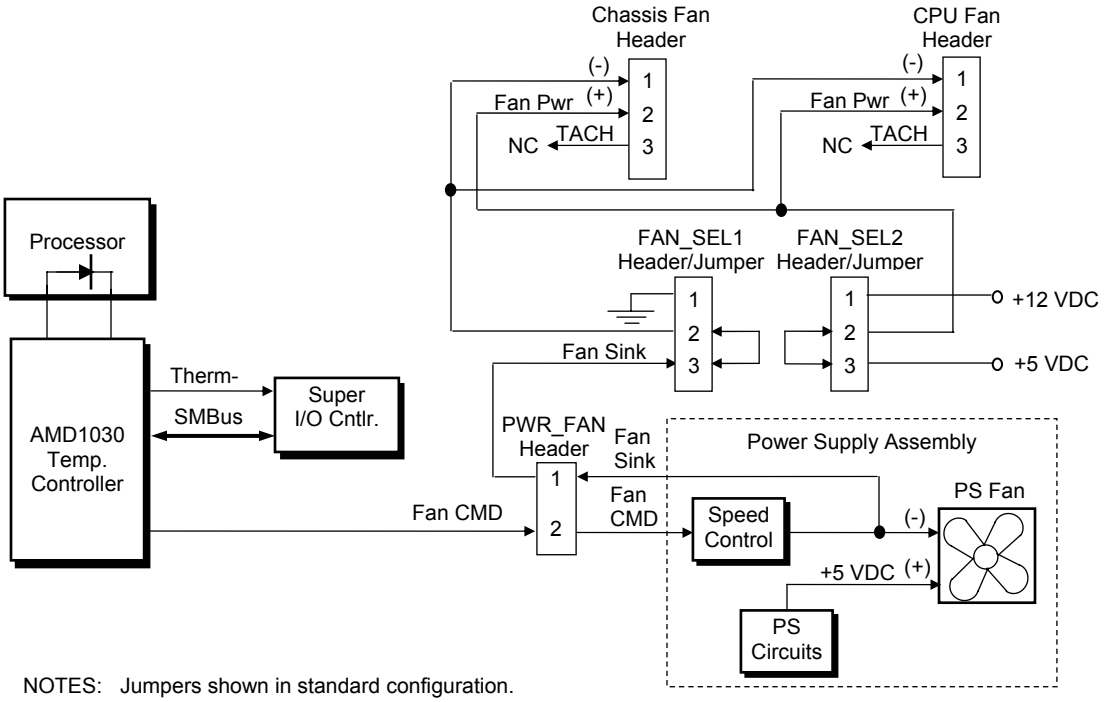


Figure 4-12. D315 Model Fan Control Block Diagram

4.7.4.2 Cooling for d325 Models

The fan control logic on the d325 model differs from the D315 system in that fans are controlled by the system board logic. The fans are driven by a constant positive 12 volts on one side and a negative voltage that is variable through the Fan Cntrl logic. A Hardware Monitor ASIC monitors the temperature of the processor and changes the duty cycle of the Fan PWM to increase or decrease fan speed based on the processor temperature. The Fan Clamp signal is initiated by the BIOS and produced by the GPIO at boot time to ensure that the fans start at boot time.

NOTE: A protection mechanism is provided where the processor threshold temperature programmed into the Hardware Monitor ASIC is temporarily set by the BIOS to a lower than normal level during the initial start up to protect against the possibility of an incorrectly installed heat sink. If during the boot period the processor's temperature reaches 100° C the hardware Monitor will assert the Therm signal causing the I/O Controller to de-assert the PS On signal, which will shut down the power supply. If the processor does not reach 100° C during the boot sequence the BIOS then re-sets the thermal threshold to the run-time level of 125° C

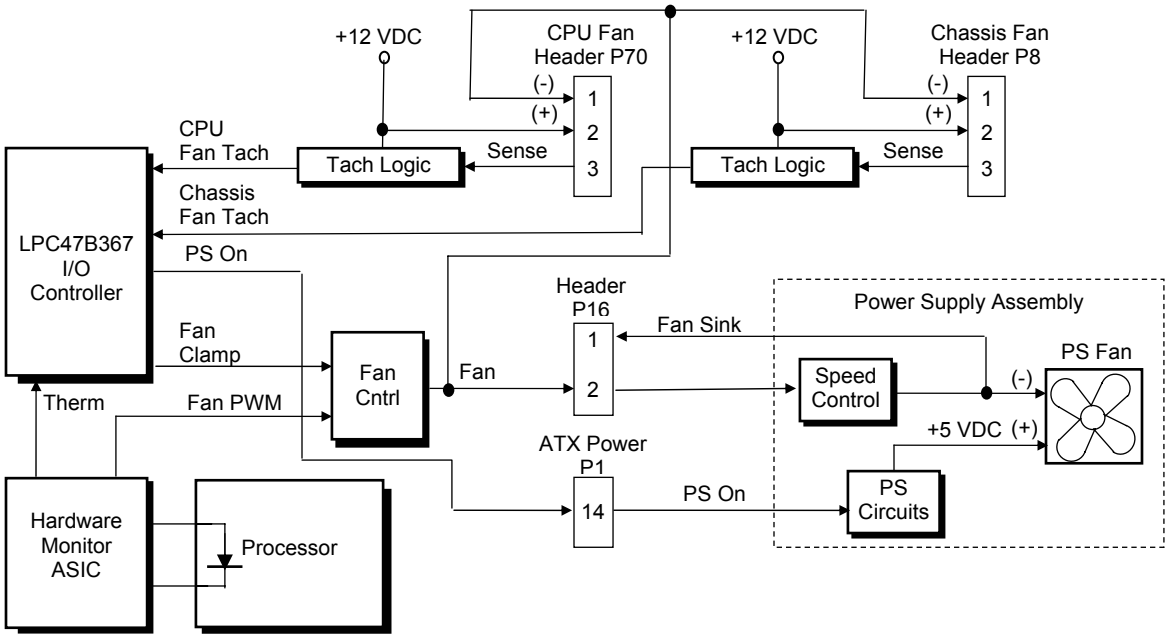


Figure 4-13. d325 Model Fan Control Functional Block Diagram

4.8 REGISTER MAP AND MISCELLANEOUS FUNCTIONS

This section contains the system I/O map and information on general-purpose functions of the MCP and I/O controller.

4.8.1 SYSTEM I/O MAP

Table 4-14 lists the fixed addresses of the input/output (I/O) ports.

Table 4-14.
System I/O Map

I/O Port	Function
0000..001Fh	DMA Controller 1
0020..002Dh	Interrupt Controller 1
002E, 002Fh	Index, Data Ports to LPC47B367 I/O Controller (primary)
0030..003Dh	Interrupt Controller
0040..0042h	Timer 1
004E, 004Fh	Index, Data Ports to LPC47B367 I/O Controller (secondary)
0050..0052h	Timer / Counter
0060..0067h	Microcontroller, NMI Controller (alternating addresses)
0070..0077h	RTC Controller
0080..0091h	DMA Controller
0092h	Port A, Fast A20/Reset Generator
0093..009Fh	DMA Controller
00A0..00B1h	Interrupt Controller 2
00B2h, 00B3h	APM Control/Status Ports
00B4..00BDh	Interrupt Controller
00C0..00DFh	DMA Controller 2
00F0h	Coprocessor error register
0170..0177h	IDE Controller 2 (active only if standard I/O space is enabled for primary drive)
01F0..01F7h	IDE Controller 1 (active only if standard I/O space is enabled for secondary drive)
0278..027Fh	Parallel Port (LPT2)
02E8..02EFh	Serial Port (COM4)
02F8..02FFh	Serial Port (COM2)
0370..0377h	Diskette Drive Controller Secondary Address
0376h	IDE Controller 2 (active only if standard I/O space is enabled for primary drive)
0378..037Fh	Parallel Port (LPT1)
03B0..03DFh	Graphics Controller
03BC..03BEh	Parallel Port (LPT3)
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6h	IDE Controller 1 (active only if standard I/O space is enabled for sec. drive)
03F8..03FFh	Serial Port (COM1)
04D0, 04D1h	Interrupt Controller
0678..067Fh	Parallel Port (LPT2)
0778..077Fh	Parallel Port (LPT1)
07BC..07BEh	Parallel Port (LPT3)
0CF8h	PCI Configuration Address (dword access only)
0CF9h	Reset Control Register
0CFCh	PCI Configuration Data (byte, word, or dword access)

NOTE:
Assume unmarked gaps are unused, reserved, or used by functions that employ variable I/O address mapping. Some ranges may include reserved addresses.

4.8.2 LPC47B367 I/O CONTROLLER FUNCTIONS

The LPC47B367 I/O controller contains various functions such as the keyboard/mouse interfaces, diskette interface, serial interfaces, and parallel interface. While the control of these interfaces uses standard AT-type I/O addressing (as described in chapter 5) the configuration of these functions uses indexed ports unique to the LPC47B367. In these systems, hardware strapping selects I/O addresses 02Eh and 02Fh at reset as the Index/Data ports for accessing the logical devices within the LPC47B367. Table 4-15 lists the PnP standard control registers for the LPC47B367.

Table 4-15.
LPC47B367 I/O Controller Control Registers

Index	Function	Reset Value
02h	Configuration Control	00h
03h	Reserved	
07h	Logical Device (Interface) Select: 00h = Diskette Drive I/F 01h = Reserved 02h = Reserved 03h = Parallel I/F 04h = Serial I/F (UART 1/Port A) 05h = Serial I/F (UART 2/Port B) 06h = Reserved 07h = Keyboard I/F 08h = Reserved 09h = Reserved 0Ah = Runtime Registers (GPIO Config.) 0Bh = SMBus Configuration	00h
20h	Super I/O ID Register (SID)	56h
21h	Revision	--
22h	Logical Device Power Control	00h
23h	Logical Device Power Management	00h
24h	PLL / Oscillator Control	04h
25h	Reserved	
26h	Configuration Address (Low Byte)	
27h	Configuration Address (High Byte)	
28-2Fh	Reserved	

NOTE:
For a detailed description of registers refer to appropriate SMC documentation.

The configuration registers are accessed through I/O registers 2Eh (index) and 2Fh (data) after the configuration phase has been activated by writing 55h to I/O port 2Eh. The desired interface (logical device) is initiated by firmware selecting logical device number of theLPC47B347 using the following sequence:

1. Write 07h to I/O register 2Eh.
2. Write value of logical device to I/O register 2Fh.
3. Write 30h to I/O register 2Eh.
4. Write 01h to I/O register 2Fh (this activates the interface).

Writing AAh to 2Eh deactivates the configuration phase.

The systems covered in this guide utilize the following specialized functions built into the LPC47B367 I/O Controller:

- Power/HD LED status indicators – The I/O controller provides color and blink control for the front panel LEDs used for indicating system events as listed below. Indications valid for both D315 and d325 unless otherwise indicated.

System Status	Power LED	HD LED	Beeps
S0: System on (normal operation)	Steady green	Green w/HD activity	None
S1: Suspend	Blinks green @ 0.5 Hz	Off	None
S3: Suspend to RAM	Blinks green @ 0.5 Hz	Off	None
S4: Suspend to disk	Off	Off	None
S5: Soft off	Off	Off	None
Processor not seated	Steady red	Off	None
ROM flashing	[1]	Off	None
No memory installed	Blinks red @ 2 Hz	Off	None
Power supply crowbar activated (D315 only)	Blinks red @ 0.5 Hz	Off	None
CPU thermal shutdown	D315 [2], d325 [3]		
Memory error (d325 only)	See note [4]	Off	5
Video error (d325 only)	See note [5]	Off	6
System board failure (d325 only)	See note [6]	Off	7
Invalid ROM checksum (d325 only)	See note [7]	Off	8
System off	Off	Off	None

NOTES:

[1] Red during flash, then blinks green @ 1 Hz when user can reboot.
[2] Repetitive sequence of 2 red blinks @ 1 Hz, followed by 2-second pause.
[3] Repetitive sequence of four red blinks @ 1 Hz followed by 2-second pause
[4] Repetitive sequence of five red blinks @ 1 Hz followed by 2-second pause.
[5] Repetitive sequence of six red blinks @ 1 Hz followed by 2-second pause.
[6] Repetitive sequence of seven red blinks @ 1 Hz followed by 2-second pause.
[7] Repetitive sequence of eight red blinks @ 1 Hz followed by 2-second pause.

- I/O security – The parallel, serial, and diskette interfaces may be disabled individually by software and the LPC47B367's disabling register locked. If the disabling register is locked, a system reset through a cold boot is required to gain access to the disabling (Device Disable) register.

- Legacy/ACPI power button mode control – The LPC47B367 receives the pulse signal from the system's power button and produces the PS On signal according to the mode (legacy or ACPI) selected. Refer to chapter 7 for more information regarding power management.

Chapter 5
INPUT/OUTPUT INTERFACES

5.1 INTRODUCTION

This chapter describes the standard (i.e., system board) interfaces that provide input and output (I/O) porting of data and specifically discusses interfaces that are controlled through I/O-mapped registers. The following I/O interfaces are covered in this chapter:

5.2 ENHANCED IDE INTERFACE

The enhanced IDE (EIDE) interface consists of primary and secondary controllers integrated into the south bridge component of the chipset. Two 40-pin IDE connectors (one for each controller) are included on the system board. Each controller can be configured independently for the following modes of operation:

- Programmed I/O (PIO) mode – CPU controls drive transactions through standard I/O mapped registers of the IDE drive.
- 8237 DMA mode – CPU offloads drive transactions using DMA protocol with transfer rates up to 16 MB/s.
- Ultra ATA/100 mode – Preferred bus mastering source-synchronous protocol providing transfer rates of 100 MB/s.

5.2.1 IDE PROGRAMMING

The IDE interface is configured as a PCI device during POST and controlled through I/O-mapped registers at runtime. Operating systems other than DOS or Windows may require using Setup (F10) for drive configuration.

5.2.1.1 IDE Configuration Registers

The IDE controller is configured as a PCI device with bus mastering capability. The PCI configuration registers for the IDE controller function (PCI device #9, function #0) are listed in Table 5-1.

Table 5-1.
IDE PCI Configuration Registers (MCP, Device 9/Function 0)

PCI Conf. Addr.	Register	Reset Value	PCI Conf. Addr.	Register	Reset Value
00, 01h	Vender ID	10DEh	3Ch	Interrupt Line	00h
02, 03h	Device ID	[1]	3Dh	Interrupt Pin	01h
04, 05h	PCI Command	0000h	3Eh	Minimum Grant	03h
06-07h	PCI Status	00B0h	3Fh	Maximum Latency	01h
08h	Revision ID	A1h	40h	Write SS Vendor ID	0000h
09 – 0Bh	Class Code	01018Ah	42h	Write SS ID	0000h
0Ch	Cache Line Size	00h	44h	Power Mgmt. Config.	01h
0Dh	Master Latency Timer	00h	45h	Next Item Pointer	00h
0Eh	Header Type	00h	46h	Power Mgmt. Capabilities	E802h
0Fh	BIST	00h	48h	Power Mgmt. Cntrl./Sts.	0000h
10 – 13h	Pri. Cmd. I/O Base Addr.	1d	4Bh	Power Mgmt. Data	00h
14 – 17h	Pri. Cntrl. I/O Base Addr.	1d	50h	IDE Config.	0000h
18 – 1Bh	Sec. CMD I/O Base Addr.	1d	58, 59h	IDE Timing	A8A8h
1C – 1Fh	Sec. Cntrl. I/O Base Addr.	1d	5A, 5Bh	IDE Timing	A8A8h
20h	Bus Mstr. I/O Base Addr.	1d	5Ch	IDE Cycle & Addr. Timing	00FFh
2Ch	Subsystem Vendor ID	0000h	5Dh	IDD Cycle & Addr. Timing	FFFFh
2Eh	Subsystem ID	0000h	60h	UDMA Mode Selection	0s
34h	Capabilities Pointer	44h	-	-	-

NOTES:
[1] D315 = 01BCh, d325 = 0065h

5.2.1.2 IDE Bus Master Control Registers

The IDE interface can perform PCI bus master operations using the registers listed in Table 5-2. These registers occupy 16 bytes of variable I/O space set by software and indicated by PCI configuration register 20h in the previous table.

Table 5-2.
IDE Bus Master Control Registers

I/O Addr. Offset	Size (Bytes)	Register	Default Value
00h	1	Bus Master IDE Command (Primary)	00h
02h	1	Bus Master IDE Status (Primary)	00h
04h	4	Bus Master IDE Descriptor Pointer (Pri.)	0000 0000h
08h	1	Bus Master IDE Command (Secondary)	00h
0Ah	2	Bus Master IDE Status (Secondary)	00h
0Ch	4	Bus Master IDE Descriptor Pointer (Sec.)	0000 0000h

NOTE:
Unspecified gaps are reserved, will return indeterminate data, and should not be written to.

5.2.2 IDE CONNECTOR

This system uses a standard 40-pin connector for the primary IDE device and connects (via a cable) to the hard drive. Note that some signals are re-defined for UATA/33 and higher modes, which require a special 80-conductor cable (supplied) designed to reduce cross-talk. Device power is supplied through a separate connector.

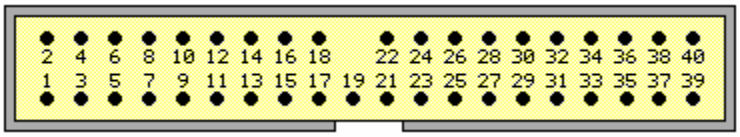


Figure 5-1. 40-Pin Primary IDE Connector (on system board).

Table 5-3.
40-Pin Primary IDE Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESET-	Reset	21	DRQ	DMA Request
2	GND	Ground	22	GND	Ground
3	DD7	Data Bit <7>	23	IOW-	I/O Write [1]
4	DD8	Data Bit <8>	24	GND	Ground
5	DD6	Data Bit <6>	25	IOR-	I/O Read [2]
6	DD9	Data Bit <9>	26	GND	Ground
7	DD5	Data Bit <5>	27	IORDY	I/O Channel Ready [3]
8	DD10	Data Bit <10>	28	CSEL	Cable Select
9	DD4	Data Bit <4>	29	DAK-	DMA Acknowledge
10	DD11	Data Bit <11>	30	GND	Ground
11	DD3	Data Bit <3>	31	IRQn	Interrupt Request [4]
12	DD12	Data Bit <12>	32	IO16-	16-bit I/O
13	DD2	Data Bit <2>	33	DA1	Address 1
14	DD13	Data Bit <13>	34	DSKPDIAG	Pass Diagnostics
15	DD1	Data Bit <1>	35	DA0	Address 0
16	DD14	Data Bit <14>	36	DA2	Address 2
17	DD0	Data Bit <0>	37	CS0-	Chip Select
18	DD15	Data Bit <15>	38	CS1-	Chip Select
19	GND	Ground	39	HDACTIVE-	Drive Active (front panel LED) [5]
20	--	Key	40	GND	Ground

NOTES:

[1] On UATA/33 and higher modes, re-defined as STOP.
[2] On UATA/33 and higher mode reads, re-defined as DMARDY-.
On UATA/33 and higher mode writes, re-defined as STROBE.
[3] On UATA/33 and higher mode reads, re-defined as STROBE-.
On UATA/33 and higher mode writes, re-defined as DMARDY-.
[4] Primary connector wired to IRQ14, secondary connector wired to IRQ15.
[5] Pin 39 is used for spindle sync and drive activity (becomes SPSYNC/DACT-) when synchronous drives are connected.

5.3 DISKETTE DRIVE INTERFACE

The diskette drive interface supports up to two diskette drives, each of which use a common cable connected to a standard 34-pin diskette drive connector. Models that come standard with a 3.5-inch 1.44-MB diskette drive will have the diskette drive installed as drive A. The drive designation is determined by which connector is used on the diskette drive cable. The drive attached to the end connector is drive A while the drive attached to the second (next to the end) connector is drive B.

On all models, the diskette drive interface function is integrated into the LPC47B367 super I/O component. The internal logic of the I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- Command phase - The controller receives the command from the system.
- Execution phase - The controller carries out the command.
- Results phase - Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechnical control function of the drive, or an operation that remains internal to the diskette drive controller. Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.

5.3.1 DISKETTE DRIVE PROGRAMMING

Programming the diskette drive interface consists of configuration, which occurs typically during POST, and control, which occurs at runtime.

5.3.1.1 Diskette Drive Interface Configuration

The diskette drive controller must be configured for a specific address and also must be enabled before it can be used. Address selection and enabling of the diskette drive interface are affected by firmware through the PnP configuration registers of the LPC47B367 I/O controller during POST.

The configuration registers are accessed through I/O registers 2Eh (index) and 2Fh (data) after the configuration phase has been activated by writing 55h to I/O port 2Eh. The diskette drive I/F is initiated by firmware selecting logical device 0 of the LPC47B367 using the following sequence:

1. Write 07h to I/O register 2Eh.
2. Write 00h to I/O register 2Fh (this selects the diskette drive I/F).
3. Write 30h to I/O register 2Eh.
4. Write 01h to I/O register 2Fh (this activates the interface).

Writing AAh to 2Eh deactivates the configuration phase. The diskette drive I/F configuration registers are listed in the following table:

Table 5-4.
Diskette Drive Interface Configuration Registers

Index Address	Function	R/W	Reset Value
30h	Activate	R/W	01h
60-61h	Base Address	R/W	03F0h
70h	Interrupt Select	R/W	06h
74h	DMA Channel Select	R/W	02h
F0h	DD Mode	R/W	02h
F1h	DD Option	R/W	00h
F2h	DD Type	R/W	FFh
F4h	DD 0	R/W	00h
F5h	DD 1	R/W	00h

For detailed configuration register information refer to the SMSC data sheet for the LPC47B367 I/O component.

5.3.1.2 Diskette Drive Interface Control

The BIOS function INT 13 provides basic control of the diskette drive interface. The diskette drive interface can be controlled by software through the LPC47B367's I/O-mapped registers listed in Table 5-5. The diskette drive controller of the LPC47B367 operates in the PC/AT mode in these systems.

Table 5-5.
Diskette Drive Interface Control Registers

Pri. Addr.	Sec. Addr.	Register	R/W
3F0h	370h	Status Register A: <7> Interrupt pending <6> Reserved (always 1) <5> STEP pin status (active high) <4> TRK 0 status (active high) <3> HDSEL status (0 = side 0, 1 = side 1) <2> INDEX status (active high) <1> WR PRTK status (0 = disk is write protected) <0> Direction (0 = outward, 1 = inward)	R
3F1h	371h	Status Register B: <7,6> Reserved (always 1's) <5> DOR bit 0 status <4> Write data toggle <3> Read data toggle <2> WGATE status (active high) <1,0> MTR 2, 1 ON- status (active high)	R
3F2h	372h	Digital Output Register (DOR): <7,6> Reserved <5,4> Motor 1, 0 enable (active high) <3> DMA enable (active high) <2> Reset (active low) <1,0> Drive select (00 = Drive 1, 01 = Drive 2, 10 = Reserved, 11 = Tape drive)	R/W
3F3h	373h	Tape Drive Register (available for compatibility)	R/W
3F4h	374h	Main Status Register (MSR): <7> Request for master (host can transfer data) (active high) <6> Transfer direction (0 – write, 1 = read) <5> non-DMA execution (active high) <4> Command busy (active high) <3,2> Reserved <1,0> Drive 1, 2 busy (active high) Data Rate Select Register (DRSR): <7> Software reset (active high) <6> Low power mode enable (active high) <5> Reserved (0) <4..2> Precompensation select (default = 000) <1,0> Data rate select (00 = 500 Kb/s, 01 = 300 Kb/s, 10 = 250 Kb/s, 11 = 2/1 Mb/s)	R W
3F5h	375h	Data Register: <7..0> Data	R/W
3F6h	376h	Reserved	--
3F7h	377h	Digital Input Register (DIR): <7> DSK CHG status (records opposite value of pin) <6..0> Reserved (0's) Configuration Control Register (CCR): <7..2> Reserved <1,0> Data rate select (00 = 500 Kb/s, 01 = 300 Kb/s, 10 = 250 Kb/s, 11 = 2/1 Mb/s)	R W

NOTE: The most recently written data rate value to either DRSR or CCR will be in effect.

5.3.2 DISKETTE DRIVE CONNECTOR

This system uses a standard 34-pin connector (refer to Figure 5-2 and Table 5-6 for the pinout) for diskette drives. Drive power is supplied through a separate connector.

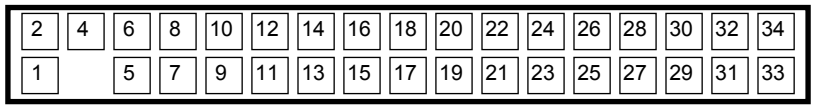


Figure 5-2. 34-Pin Diskette Drive Connector.

Table 5-6.
34-Pin Diskette Drive Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	DIR-	Drive head direction control
2	LOW DEN-	Low density select	19	GND	Ground
3	---	(KEY)	20	STEP-	Drive head track step control
4	MEDIA ID-	Media identification	21	GND	Ground
5	GND	Ground	22	WR DATA-	Write data
6	DRV 4 SEL-	Drive 4 select	23	GND	Ground
7	GND	Ground	24	WR ENABLE-	Enable for WR DATA-
8	INDEX-	Media index is detected	25	GND	Ground
9	GND	Ground	26	TRK 00-	Heads at track 00 indicator
10	MTR 1 ON-	Activates drive motor	27	GND	Ground
11	GND	Ground	28	WR PRTK-	Media write protect status
12	DRV 2 SEL-	Drive 2 select	29	GND	Ground
13	GND	Ground	30	RD DATA-	Data and clock read off disk
14	DRV 1 SEL-	Drive 1 select	31	GND	Ground
15	GND	Ground	32	SIDE SEL-	Head select (side 0 or 1)
16	MTR 2 ON-	Activates drive motor	33	GND	Ground
17	GND	Ground	34	DSK CHG-	Drive door opened indicator

5.4 SERIAL INTERFACE

All models include at least one RS-232-C type serial interface to transmit and receive asynchronous serial data with external devices. The serial interface function is provided by the LPC47B367 I/O controller component that includes two NS16C550-compatible UARTs.

The UART supports the standard baud rates up through 115200, and also special high speed rates of 239400 and 460800 baud. The baud rate of the UART is typically set to match the capability of the connected device. While most baud rates may be set at runtime, **baud rates 230400 and 460800 must be set during the configuration phase.**

5.4.1 SERIAL CONNECTOR

The serial interface uses a DB-9 connector as shown in the following figure with the pinout listed in Table 5-5.

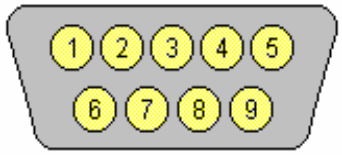


Figure 5-3. Serial Interface Connector (Male DB-9 as viewed from rear of chassis)

Table 5-7.
DB-9 Serial Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	CD	Carrier Detect	6	DSR	Data Set Ready
2	RX Data	Receive Data	7	RTS	Request To Send
3	TX Data	Transmit Data	8	CTS	Clear To Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	--	--	--

The standard RS-232-C limitation of 50 feet (or less) of cable between the DTE (computer) and DCE (modem) should be followed to minimize transmission errors. Higher baud rates may require shorter cables.

5.4.2 SERIAL INTERFACE PROGRAMMING

Programming the serial interfaces consists of configuration, which occurs during POST, and control, which occurs during runtime.

5.4.2.1 Serial Interface Configuration

The serial interface must be configured for a specific address range (COM1, COM2, etc.) and also must be activated before it can be used. Address selection and activation of the serial interface are affected through the PnP configuration registers of the LPC47B367 I/O controller.
The serial interface configuration registers are listed in the following table:

Table 5-8.
Serial Interface Configuration Registers

Index Address	Function	R/W
30h	Activate	R/W
60h	Base Address MSB	R/W
61h	Base Address LSB	R/W
70h	Interrupt Select	R/W
F0h	Mode Register	R/W

NOTE:
Refer to LPC47B367 data sheet for detailed register information.

5.4.2.2 Serial Interface Control

The BIOS function INT 14 provides basic control of the serial interface. The serial interface can be directly controlled by software through the I/O-mapped registers listed in Table 5-9.

Table 5-9.
Serial Interface Control Registers

COM1 Addr.	COM2 Addr.	Register	R/W
3F8h	2F8h	Receive Data Buffer	R
		Transmit Data Buffer	W
		Baud Rate Divisor Register 0 (when bit 7 of Line Control Reg. Is set)	W
3F9h	2F9h	Baud Rate Divisor Register 1 (when bit 7 of Line Control Reg. Is set)	W
		Interrupt Enable Register	R/W
3FAh	2FAh	Interrupt ID Register	R
		FIFO Control Register	W
3FBh	2FBh	Line Control Register	R/W
3FCh	2FCh	Modem Control Register	R/W
3FDh	2FDh	Line Status Register	R
3FEh	2FEh	Modem Status	R

5.5 PARALLEL INTERFACE

All models include a parallel interface for connection to a peripheral device that has a compatible interface, the most common being a printer. The parallel interface function is integrated into the LPC47B367 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three main modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes (and their submodes) provide complete support as specified for an IEEE 1284 parallel port.

5.5.1 STANDARD PARALLEL PORT MODE

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

The following steps define the standard procedure for communicating with a printing device:

1. The system checks the Printer Status register. If the Busy, Paper Out, or Printer Fault signals are indicated as being active, the system either waits for a status change or generates an error message.
2. The system sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control register) for at least 500 ns.
3. The system then monitors the Printer Status register for acknowledgment of the data byte before sending the next byte.

In extended mode, a direction control bit (CTR 37Ah, bit <5>) controls the latching of output data while allowing a CPU read to fetch data present on the data lines, thereby providing bi-directional parallel transfers to occur.

The SPP mode uses three registers for operation: the Data register (DTR), the Status register (STR) and the Control register (CTR). Address decoding in SPP mode includes address lines A0 and A1.

5.5.2 ENHANCED PARALLEL PORT MODE

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

Five additional registers are available in EPP mode to handle 16- and 32-bit CPU accesses with the parallel interface. Address decoding includes address lines A0, A1, and A2.

5.5.3 EXTENDED CAPABILITIES PORT MODE

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

Ten control registers are available in ECP mode to handle transfer operations. In accessing the control registers, the base address is determined by address lines A2-A9, with lines A0, A1, and A10 defining the offset address of the control register. Registers used for FIFO operations are accessed at their base address + 400h (i.e., if configured for LPT1, then 378h + 400h = 778h).

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

5.5.4 PARALLEL INTERFACE PROGRAMMING

Programming the parallel interface consists of configuration, which typically occurs during POST, and control, which occurs during runtime.

5.5.4.1 Parallel Interface Configuration

The parallel interface must be configured for a specific address range (LPT1, LPT2, etc.) and also must be enabled before it can be used. When configured for EPP or ECP mode, additional considerations must be taken into account. Address selection, enabling, and EPP/ECP mode parameters of the parallel interface are affected through the PnP configuration registers of the LPC47B367 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The parallel interface configuration registers are listed in the following table:

Table 5-10.
Parallel Interface Configuration Registers

Index Address	Function	R/W	Reset Value
30h	Activate	R/W	00h
60h	Base Address MSB	R/W	00h
61h	Base Address LSB	R/W	00h
70h	Interrupt Select	R/W	00h
74h	DMA Channel Select	R/W	04h
F0h	Mode Register	R/W	00h
F1h	Mode Register 2	R/W	00h

5.5.4.2 Parallel Interface Control

The BIOS function INT 17 provides simplified control of the parallel interface. Basic functions such as initialization, character printing, and printer status are provide by subfunctions of INT 17. The parallel interface is controllable by software through a set of I/O mapped registers. The number and type of registers available depends on the mode used (SPP, EPP, or ECP). Table 5-11 lists the parallel registers and associated functions based on mode.

Table 5-11.
Parallel Interface Control Registers

I/O Address	Register	SPP Mode Ports	EPP Mode Ports	ECP Mode Ports
Base	Data	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 1h	Printer Status	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 2h	Control	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 3h	Address	--	LPT1,2	--
Base + 4h	Data Port 0	--	LPT1,2	--
Base + 5h	Data Port 1	--	LPT1,2	--
Base + 6h	Data Port 2	--	LPT1,2	--
Base + 7h	Data Port 3	--	LPT1,2	--
Base + 400h	Parallel Data FIFO	--	--	LPT1,2,3
Base + 400h	ECP Data FIFO	--	--	LPT1,2,3
Base + 400h	Test FIFO	--	--	LPT1,2,3
Base + 400h	Configuration Register A	--	--	LPT1,2,3
Base + 401h	Configuration Register B	--	--	LPT1,2,3
Base + 402h	Extended Control Register	--	--	LPT1,2,3

Base Address:
LPT1 = 378h
LPT2 = 278h
LPT3 = 3BCh

5.5.5 PARALLEL INTERFACE CONNECTOR

Figure 5-4 and Table 5-12 show the connector and pinout of the parallel interface connector. Note that some signals are redefined depending on the port's operational mode.

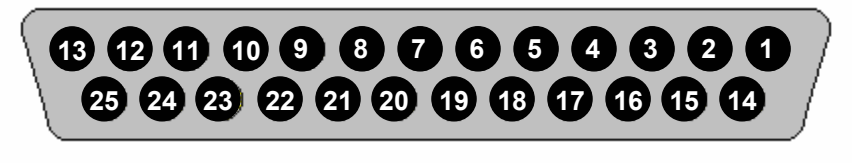


Figure 5-4. Parallel Interface Connector (Female DB-25 as viewed from rear of chassis)

Table 5-12.
DB-25 Parallel Connector Pinout

Pin	Signal	Function	Pin	Signal	Function
1	STB-	Strobe / Write [1]	14	LF-	Line Feed [2]
2	D0	Data 0	15	ERR-	Error [3]
3	D1	Data 1	16	INIT-	Initialize Paper [4]
4	D2	Data 2	17	SLCTIN-	Select In / Address. Strobe [1]
5	D3	Data 3	18	GND	Ground
6	D4	Data 4	19	GND	Ground
7	D5	Data 5	20	GND	Ground
8	D6	Data 6	21	GND	Ground
9	D7	Data 7	22	GND	Ground
10	ACK-	Acknowledge / Interrupt [1]	23	GND	Ground
11	BSY	Busy / Wait [1]	24	GND	Ground
12	PE	Paper End / User defined [1]	25	GND	Ground
13	SLCT	Select / User defined [1]	--	--	--

NOTES:
[1] Standard and ECP mode function / EPP mode function
[2] EPP mode function: Data Strobe
ECP modes: Auto Feed or Host Acknowledge
[3] EPP mode: user defined
ECP modes:Fault or Peripheral Req.
[4] EPP mode: Reset
ECP modes: Initialize or Reverse Req.

5.6 KEYBOARD/POINTING DEVICE INTERFACE

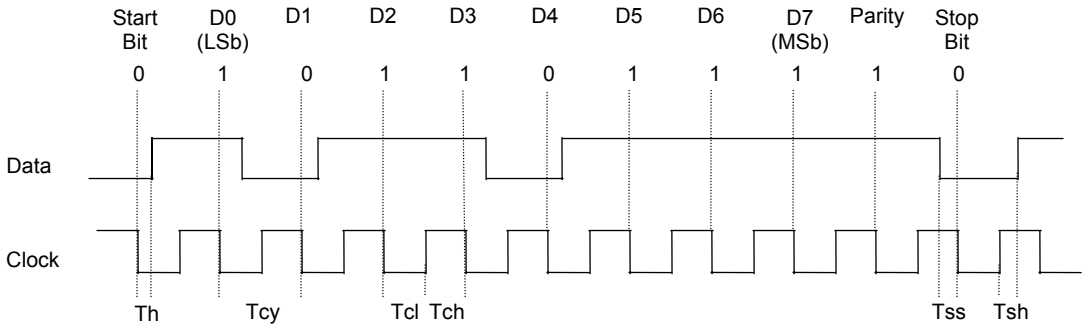
The keyboard/pointing device interface function is provided by the LPC47B367 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the "8042") to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device. This section describes the interface itself. The keyboard is discussed in the Appendix C.

5.6.1 KEYBOARD INTERFACE OPERATION

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-5). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	0 µs	80 µs
Tcl (Clock Low)	25 µs	35 µs
Tch (Clock High)	25 µs	45 µs
Th (Data Hold)	0 µs	25 µs
Tss (Stop Bit Setup)	8 µs	20 µs
Tsh (Stop Bit Hold)	15 µs	25 µs

Figure 5-5. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042 and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard. After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

Table 5-13 lists and describes commands that can be issued by the 8042 to the keyboard.

Table 5-13.
8042-To-Keyboard Commands

Command	Value	Description
Set/Reset Status Indicators	EDh	Enables LED indicators. Value EDh is followed by an option byte that specifies the indicator as follows: Bits <7..3> not used Bit <2>, Caps Lock (0 = off, 1 = on) Bit <1>, NUM Lock (0 = off, 1 = on) Bit <0>, Scroll Lock (0 = off, 1 = on)
Echo	EEh	Keyboard returns EEh when previously enabled.
Invalid Command	EFh/F1h	These commands are not acknowledged.
Select Alternate Scan Codes	F0h	Instructs the keyboard to select another set of scan codes and sends an option byte after ACK is received: 01h = Mode 1 02h = Mode 2 03h = Mode 3
Read ID	F2h	Instructs the keyboard to stop scanning and return two keyboard ID bytes.
Set Typematic Rate/Display	F3h	Instructs the keyboard to change typematic rate and delay to specified values: Bit <7>, Reserved - 0 Bits <6,5>, Delay Time 00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1000 ms Bits <4..0>, Transmission Rate: 00000 = 30.0 ms 00001 = 26.6 ms 00010 = 24.0 ms 00011 = 21.8 ms : 11111 = 2.0 ms
Enable	F4h	Instructs keyboard to clear output buffer and last typematic key and begin key scanning.
Default Disable	F5h	Resets keyboard to power-on default state and halts scanning pending next 8042 command.
Set Default	F6h	Resets keyboard to power-on default state and enable scanning.
Set Keys - Typematic	F7h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make/Brake	F8h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make	F9h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Typematic/Make/Brake	FAh	Clears keyboard buffer and sets default scan code set. [1]
Set Type Key - Typematic	FBh	Clears keyboard buffer and prepares to receive key ID. [1]
Set Type Key - Make/Brake	FCh	Clears keyboard buffer and prepares to receive key ID. [1]
Set Type Key - Make	FDh	Clears keyboard buffer and prepares to receive key ID. [1]
Resend	FEh	8042 detected error in keyboard transmission.
Reset	FFh	Resets program, runs keyboard BAT, defaults to Mode 2.

Note:
[1] Used in Mode 3 only.

5.6.2 POINTING DEVICE INTERFACE OPERATION

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

5.6.3 KEYBOARD/POINTING DEVICE INTERFACE PROGRAMMING

Programming the keyboard interface consists of configuration, which occurs during POST, and control, which occurs during runtime.

5.6.3.1 8042 Configuration

The keyboard/pointing device interface must be enabled and configured for a particular speed before it can be used. Enabling and speed parameters of the 8042 logic are affected through the PnP configuration registers of the LPC47B367 I/O controller. Enabling and speed control are automatically set by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The keyboard interface configuration registers are listed in the following table:

Table 5-14.
Keyboard Interface Configuration Registers

Index Address	Function	R/W
30h	Activate	R/W
70h	Primary Interrupt Select	R/W
72h	Secondary Interrupt Select	R/W
F0h	Reset and A20 Select	R/W

5.6.3.2 8042 Control

The BIOS function INT 16 is typically used for controlling interaction with the keyboard. Sub-functions of INT 16 conduct the basic routines of handling keyboard data (i.e., translating the keyboard's scan codes into ASCII codes). The keyboard/pointing device interface is accessed by the CPU through I/O mapped ports 60h and 64h, which provide the following functions:

- Output buffer reads
- Input buffer writes
- Status reads
- Command writes

Ports 60h and 64h can be accessed using the IN instruction for a read and the OUT instruction for a write. Prior to reading data from port 60h, the "Output Buffer Full" status bit (64h, bit <0>) should be checked to ensure data is available. Likewise, before writing a command or data, the "Input Buffer Empty" status bit (64h, bit <1>) should also be checked to ensure space is available.

I/O Port 60h

I/O port 60h is used for accessing the input and output buffers. This register is used to send and receive data from the keyboard and the pointing device. This register is also used to send the second byte of multi-byte commands to the 8042 and to receive responses from the 8042 for commands that require a response.

A read of 60h by the CPU yields the byte held in the output buffer. The output buffer holds data that has been received from the keyboard and is to be transferred to the system.

A CPU write to 60h places a data byte in the input byte buffer and sets the CMD/ DATA bit of the Status register to DATA. The input buffer is used for transferring data from the system to the keyboard. All data written to this port by the CPU will be transferred to the keyboard **except** bytes that follow a multibyte command that was written to 64h

I/O Port 64h

I/O port 64h is used for reading the status register and for writing commands. A read of 64h by the CPU will yield the status byte defined as follows:

Bit	Function
7..4	General Purpose Flags.
3	CMD/DATA Flag (reflects the state of A2 during a CPU write). 0 = Data 1 = Command
2	General Purpose Flag.
1	Input Buffer Full. Set (to 1) upon a CPU write. Cleared by IN A, DBB instruction.
0	Output Buffer Full (if set). Cleared by a CPU read of the buffer.

A CPU write to I/O port 64h places a command value into the input buffer and sets the CMD/DATA bit of the status register (bit <3>) to CMD.

Table 5-15 lists the commands that can be sent to the 8042 by the CPU. The 8042 uses IRQ1 for gaining the attention of the CPU.

Table 5-15.
CPU Commands To The 8042

Value	Command Description
20h	Put current command byte in port 60h.
60h	Load new command byte.
A4h	Test password installed. Tests whether or not a password is installed in the 8042: If FAh is returned, password is installed. If F1h is returned, no password is installed.
A5h	Load password. This multi-byte operation places a password in the 8042 using the following manner: 1. Write A5h to port 64h. 2. Write each character of the password in 9-bit scan code (translated) format to port 60h. 3. Write 00h to port 60h.
A6h	Enable security. This command places the 8042 in password lock mode following the A5h command. The correct password must then be entered before further communication with the 8042 is allowed.
A7h	Disable pointing device. This command sets bit <5> of the 8042 command byte, pulling the clock line of the pointing device interface low.
A8h	Enable pointing device. This command clears bit <5> of the 8042 command byte, activating the clock line of the pointing device interface.
A9h	Test the clock and data lines of the pointing device interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
AAh	Initialization. This command causes the 8042 to inhibit the keyboard and pointing device and places 55h into the output buffer.
ABh	Test the clock and data lines of the keyboard interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
ADh	Disable keyboard command (sets bit <4> of the 8042 command byte).
AEh	Enable keyboard command (clears bit <4> of the 8042 command byte).
C0h	Read input port of the 8042. This command directs the 8042 to transfer the contents of the input port to the output buffer so that they can be read at port 60h.
C2h	Poll Input Port High. This command directs the 8042 to place bits <7..4> of the input port into the upper half of the status byte on a continous basis until another command is received.
C3h	Poll Input Port Low. This command directs the 8042 to place bits <3..0> of the input port into the lower half of the status byte on a continous basis until another command is received.
D0h	Read output port. This command directs the 8042 to transfer the contents of the output port to the output buffer so that they can be read at port 60h.
D1h	Write output port. This command directs the 8042 to place the next byte written to port 60h into the output port (only bit <1> can be changed).
D2h	Echo keyboard data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the keyboard. No 11-to-9 bit translation takes place but an interrupt (IRQ1) is generated if enabled.
D3h	Echo pointing device data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the pointing device. An interrupt (IRQ12) is generated if enabled.
D4h	Write to pointing device. Directs the 8042 to send the next byte written to 60h to the pointing device.
E0h	Read test inputs. Directs the 8042 to transfer the test bits 1 and 0 into bits <1,0> of the output buffer.
F0h-FFh	Pulse output port. Controls the pulsing of bits <3..0> of the output port (0 = pulse, 1 = don't pulse). Note that pulsing bit <0> will reset the system.

5.6.4 KEYBOARD/POINTING DEVICE INTERFACE CONNECTOR

These systems provide separate PS/2 connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-6 and Table 5-16 show the connector and pinout of the keyboard/pointing device interface connectors.

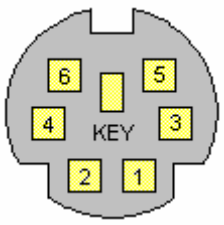


Figure 5-6. Keyboard or Pointing Device Interface Connector
(as viewed from rear of chassis)

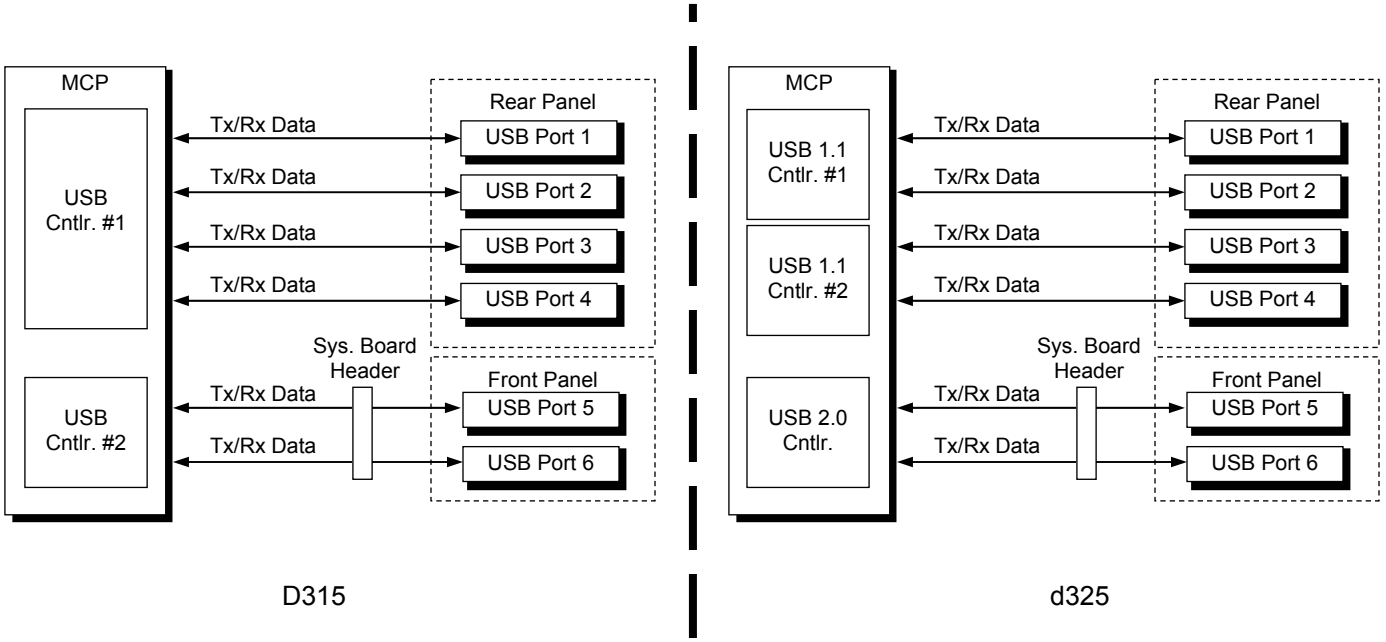
Table 5-16.
Keyboard/Pointing Device Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DATA	Data	4	+ 5 VDC	Power
2	NC	Not Connected	5	CLK	Clock
3	GND	Ground	6	NC	Not Connected

5.7 UNIVERSAL SERIAL BUS INTERFACE

The Universal Serial Bus (USB) interface provides asynchronous/isochronous data transfers with compatible peripherals such as keyboards, printers, or modems. This high-speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems.

All models provide six USB ports; four rear-mounted ports and two ports accessible in the front. The system dynamically makes the port-to-controller configuration based on the bandwidth demands of the connected USB peripheral devices.



Difference Matrix		
Function	**D315**	**D325**
USB Controller Type: Controller #1 Controller #2 Controller #3	 USB 1.1 USB 1.1 na	 USB 1.1 USB 1.1 USB 2.0
Port-to-Controller Type Configuration Options	3 per controller, 2 to one, or 4 to another	6 to 1.1, 4 to 1.1 & 2 to 2.0, 3 to 1.1 & 3 to 2.0, 2 to 1.1 & 4 to 2.0, 6 to 2.0

Figure 5-7. USB I/F Block Diagram and Difference Matrix

5.7.1 USB DATA FORMATS

The USB I/F uses non-return-to-zero inverted (NRZI) encoding for data transmissions, in which a 1 is represented by no change (between bit times) in signal level and a 0 is represented by a change in signal level. Bit stuffing is employed prior to NRZ1 encoding so that in the event a string of 1's is transmitted (normally resulting in a steady signal level) a 0 is inserted after every six consecutive 1's to ensure adequate signal transitions in the data stream. The USB transmissions consist of packets using one of four types of formats (Figure 5-8) that include two or more of seven field types.

- Sync Field – 8-bit field that starts every packet and is used by the receiver to align the incoming signal with the local clock.
- Packet Identifier (PID) Field – 8-bit field sent with every packet to identify the attributes (in. out, start-of-frame (SOF), setup, data, acknowledge, stall, preamble) and the degree of error correction to be applied.
- Address Field – 7-bit field that provides source information required in token packets.
- Endpoint Field – 4-bit field that provides destination information required in token packets.
- Frame Field – 11-bit field sent in Start-of-Frame (SOF) packets that are incremented by the host and sent only at the start of each frame.
- Data Field – 0-1023-byte field of data.
- Cyclic Redundancy Check (CRC) Field – 5- or 16-bit field used to check transmission integrity.

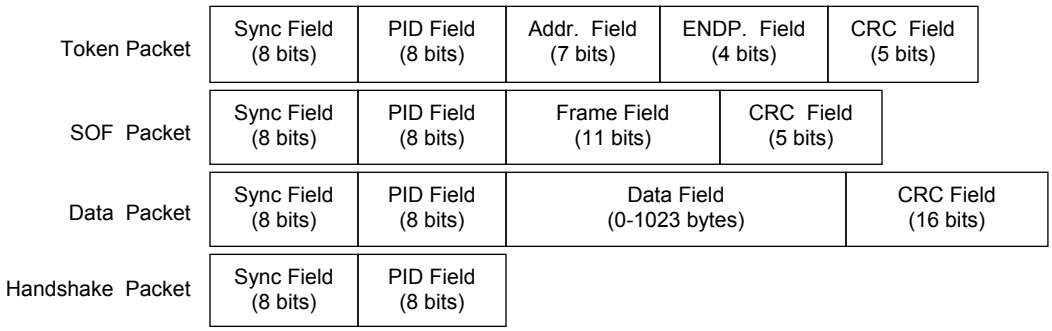


Figure 5-8. USB Packet Formats

Data is transferred LSb first. A cyclic redundancy check (CRC) is applied to all packets (except a handshake packet). A packet causing a CRC error is generally completely ignored by the receiver.

5.7.2 USB PROGRAMMING

Programming the USB interface consists of configuration, which typically occurs during POST, and control, which occurs at runtime.

5.7.2.1 USB Configuration

Each USB controller functions as a PCI device within the MCP component and is configured using PCI Configuration Registers as listed in Table 5-17.

Table 5-17.
USB Interface Configuration Registers

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vender ID	10DEh	0Fh	BIST	00h
02, 03h	Device ID	[1]	10h	OHCI Memory Base Addr.	0s
04, 05h	PCI Command	0200h	3Ch	Interrupt Line	00h
06, 07h	PCI Status	00B0h	3Dh	Interrupt Pin	01h
08h	Revision ID	A1h	3Eh	Minimum Grant	03h
09h	Class Code	0C0310h	3Fh	Maximum Latency	01h
0Ch	Cache Line Size	00h	46h	Power Mgmt. Capabilities	FE02h
0Dh	Latency Timer	00	4Ch	Specific Configuration	[2]
0Eh	Header Type	00h	50h	USB Port Mapping	[3]

NOTE:
[1] For D315 = 01C2h; for D325 = 0067h (Cntlr #1), 0067h (Cntlr #2), or 0068h (Cntlr #3)
[2] USB #1 = 02h
USB #2 = 03h
[3] The BIOS will configure this register for 2/4 operation.

5.7.2.2 USB Control

The USB is controlled through I/O registers as listed in table 5-18.

Table 5-18.
USB Control Registers

I/O Addr.	Register	Default Value
00, 01h	Command	0000h
02, 03h	Status	0000h
04, 05h	Interrupt Enable	0000h
06, 07	Frame Number	0000h
08, 0B	Frame List Base Address	0000h
0Ch	Start of Frame Modify	40h
10, 11h	Port 1 Status/Control	0080h
12, 13h	Port 2 Status/Control	0080h
18h	Test Data	00h

5.7.3 USB CONNECTOR

These systems provide type-A USB ports as shown in Figure 5-9 below.

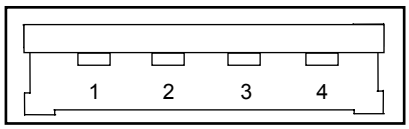


Figure 5-9. Universal Serial Bus Connector

Table 5-19.
USB Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	Vcc	+5 VDC	3	USB+	Data (plus)
2	USB-	Data (minus)	4	GND	Ground

5.7.4 USB CABLE DATA

The recommended cable length between the host and the USB device should be no longer than sixteen feet for full-channel (12 MB/s) operation, depending on cable specification (see following table).

Table 5-20.
USB Cable Length Data

Conductor Size	Resistance	Maximum Length
20 AWG	0.036 Ω	16.4 ft (5.00 m)
22 AWG	0.057 Ω	9.94 ft (3.03 m)
24 AWG	0.091 Ω	6.82 ft (2.08 m)
26 AWG	0.145 Ω	4.30 ft (1.31 m)
28 AWG	0.232 Ω	2.66 ft (0.81 m)

NOTE:
For sub-channel (1.5 MB/s) operation and/or when using sub-standard cable shorter lengths may be allowable and/or necessary.

The shield, chassis ground, and power ground should be tied together at the host end but left unconnected at the device end to avoid ground loops.

Color code:

Signal	Insulation color
Data +	Green
Data -	White
Vcc	Red
Ground	Black

5.8 AUDIO SUBSYSTEM

This system includes an embedded Sound Blaster-compatible audio subsystem with front panel-accessible headphone and microphone jacks.

5.8.1 FUNCTIONAL ANALYSIS

A block diagram of the audio subsystem is shown in Figure 5-10. These systems use the AC'97 Audio Controller of the MCP component to access and control an Analog Devices AD1885 or AD1981B Audio Codec, which provides the analog-to-digital (ADC) and digital-to-analog (DAC) conversions as well as the mixing functions. All control functions such as volume, audio source selection, and sampling rate are controlled through software over the PCI bus through the AC97 Audio Controller of the MCP component. Control data and digital audio streams (record and playback) are transferred between the Audio Controller and the Audio Codec over the AC97 Link Bus.

This system incorporates Business Audio, which has the codec stereo analog output applied through headphone jacks and switch logic to a mono 3-watt amplifier that drives a 16-ohm speaker. The switch logic allows the system to provide headphone functionality with or without the front panel assembly installed.

The analog interfaces allowing connection to external audio devices include:

Mic In - This input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a condenser microphone with an impedance of 10-K ohms. This is the default recording input after a system reset. Either the front or rear panel microphone jack is available for use (but **not** simultaneously).

Line In - This input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a high-impedance (10k-ohm) audio source such as a tape deck.

Headphones Out - This input uses a three-conductor (stereo) mini-jack that is designed for connecting a set of 16-ohm (nom.) stereo headphones or powered speakers. Plugging into the Headphones jack mutes the signal to the internal speaker.

Line Out - This output uses a three-conductor (stereo) mini-jack for connecting left and right channel line-level signals (20-K ohm impedance). A typical connection would be to a tape recorder's Line In (Record In) jacks, an amplifier's Line In jacks, or to powered speakers that contain amplifiers. Plugging into the Line Out mutes the internal speaker.

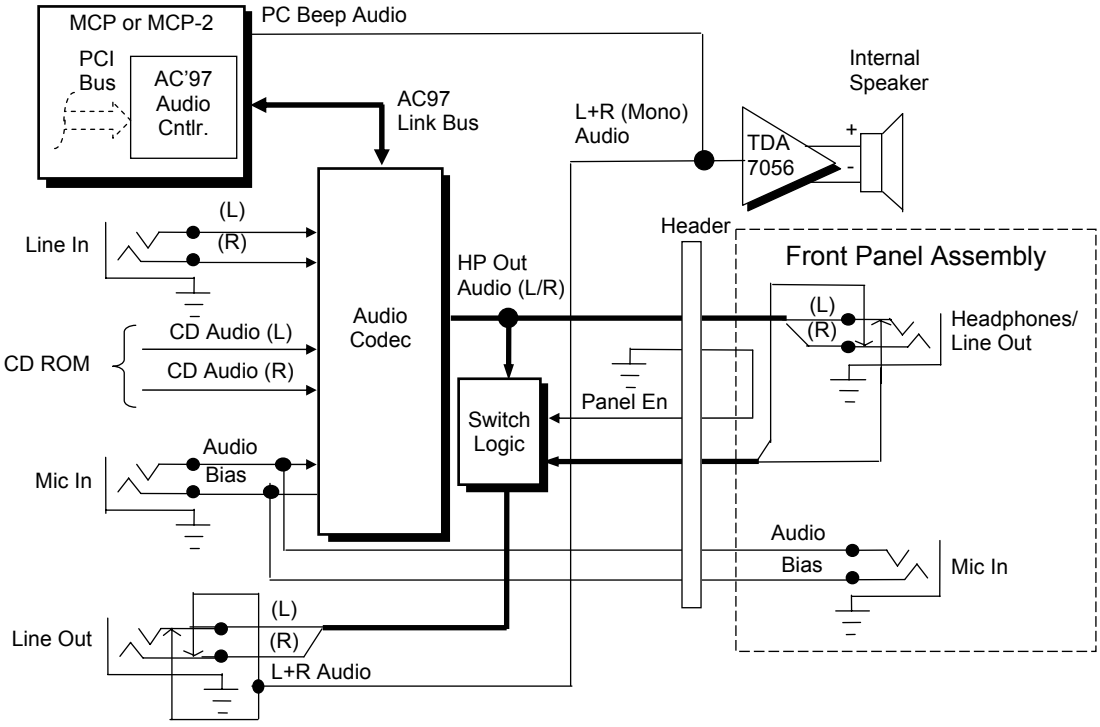


Figure 5-10. Audio Subsystem Functional Block Diagram

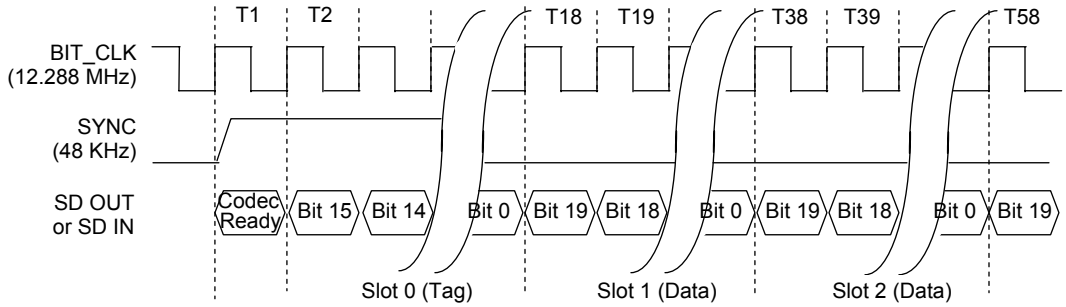
5.8.2 AC97 AUDIO CONTROLLER

The AC97 Audio Controller is a PCI device (device 6/function 0) that is integrated into the MCP component and supports the following functions:

- Read/write access to audio codec registers
- 16-bit stereo PCM output @ up to 48 KHz sampling
- 16-bit stereo PCM input @ up to 48 KHz sampling
- Acoustic echo correction for microphone
- AC'97 Link Bus
- ACPI power management

5.8.3 AC97 LINK BUS

The audio controller and the audio codec communicate over a five-signal AC97 Link Bus (Figure 5-11). The AC97 Link Bus includes two serial data lines (SD OUT/SD IN) that transfer control and PCM audio data serially to and from the audio codec using a time-division multiplexed (TDM) protocol. The data lines are qualified by a 12.288 MHz BIT_CLK signal driven by the audio codec. Data is transferred in frames synchronized by the 48-KHz SYNC signal, which is derived from the clock signal and driven by the audio controller. The SYNC signal is high during the frame's tag phase then falls during T17 and remains low during the data phase. A frame consists of one 16-bit tag slot followed by twelve 20-bit data slots. When asserted (typically during a power cycle), the RESET- signal (not shown) will reset all audio registers to their default values.



Slot	Description
0	Bit 15: Frame valid bit Bits 14-3: Slots 1-12 valid bits Bits 2-0: Codec ID
1	Command address: Bit 19, R/W; Bits 18..12, reg. Index; Bits 11..0, reserved.
2	Command data
3	Bits 19-4: PCM audio data, left channel (SD OUT, playback; SD IN, record) Bits 3-0 all zeros
4	Bits 19-4: PCM audio data, right channel (SD OUT, playback; SD IN, record) Bits 3-0 all zeros
5	Modem codec data (not used in this system)
6-11	Reserved
12	I/O control

Figure 5-11. AC'97 Link Bus Protocol

5.8.4 AUDIO CODEC

The audio codec provides pulse code modulation (PCM) coding and decoding of audio information as well as the selection and/or mixing of analog channels. As shown in Figure 5-12, analog audio from a microphone, tape, or CD can be selected and, if to be recorded (saved) onto a disk drive, routed through an analog-to-digital converter (ADC). The resulting left and right PCM record data are muxed into a time-division-multiplexed (TDM) data stream (SD IN signal) that is routed to the audio controller. Playback (PB) audio takes the reverse path from the audio controller to the audio codec as SD OUT data and is decoded and processed by the digital-to-analog converter (DAC). The codec supports simultaneous record and playback of stereo (left and right) audio. The Sample Rate Generator may be set for sampling frequencies up to 48 KHz.

Analog audio may then be routed through 3D stereo enhancement processor or bypassed to the output selector (SEL). The integrated analog mixer provides the computer control-console functionality handling multiple audio inputs.

The D315 and D325 models use the Analog Devices AD1885 and the AD1981B respectively. These devices differ in that the AD1885 includes a 3D analog processor while the AD1981B includes an equalizer as well as SPDIF support.

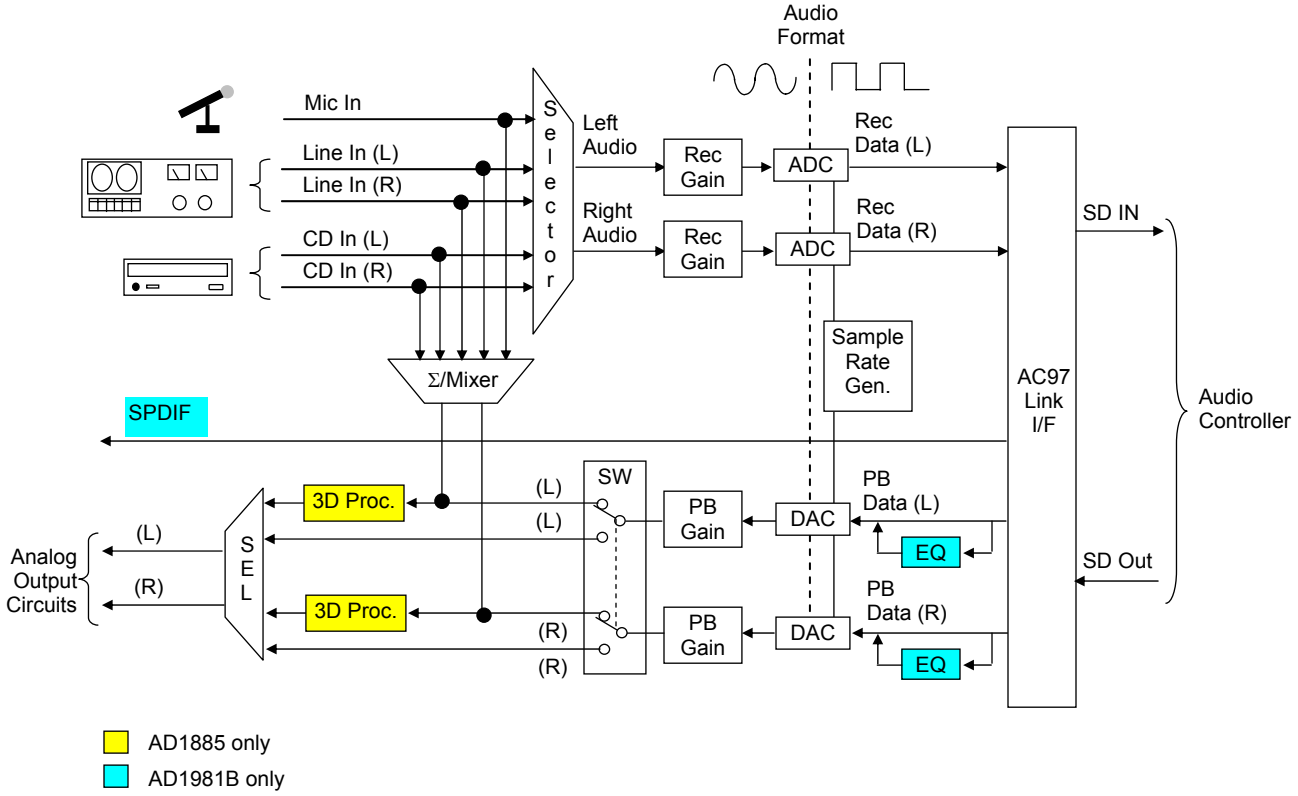


Figure 5-12. Audio Codec Functional Block Diagram and Difference Matrix

5.8.5 AUDIO PROGRAMMING

Audio subsystem programming consists configuration, typically accomplished during POST, and control, which occurs during runtime.

5.8.5.1 Audio Configuration

The audio subsystem is configured according to PCI protocol through the AC'97 audio controller function of the MCP. Table 5-21 lists the key PCI configuration registers of the audio subsystem.

Table 5-21.
AC'97 Audio Controller
PCI Configuration Registers (MCP Device 36Function 0)

PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vender ID	10DEh	10 – 13h	Audio Base Addr.	1d
02-03h	Device ID	01B1h	14 – 17h	Audio Bus Mstr. Addr.	1d
04-05h	PCI Command	0200h	18 – 1Bh	Audio Mem. Base Addr.	0s
06-07h	PCI Status	00B0h	34h	Capabilities Pointer	44h
08h	Revision ID	A1h	3Ch	Interrupt Line	00h
09h	Class Code	040100h	3Dh	Interrupt Pin	01h
0Ch	Cache Line Size	00h	3Eh	Minimum Grant	02h
0Dh	Latency Timer	00h	3Fh	Maximum Latency	05h
0Eh	Header Type	80h	44h	Power Management Config.	01h
0Fh	BIST	00h	46h	Power Mgmnt. Capabilities	FE02h

5.8.5.2 Audio Control

The audio subsystem is controlled through a set of indexed registers that physically reside in the audio codec . The register addresses are decoded by the audio controller and forwarded to the audio codec over the AC97 Link Bus previously described. The audio codec's control registers (Table 5-22) are mapped into 64 kilobytes of variable I/O space.

Table 5-22.
AC'97 Audio Codec Control Registers

Offset Addr. / Register	Value On Reset	Offset Addr. / Register	Value On Reset	Offset Addr. / Register	Value On Reset
00h Reset	0100h	14h Video Vol.	8808h	28h Ext. Audio ID.	0001h
02h Master Vol.	8000h	16h Aux Vol.	8808h	2Ah Ext. Audio Ctrl/Sts	0000h
04h Reserved	--	18h PCM Out Vol.	8808h	2Ch PCM DAC SRate	BB80h
06h Mono Mstr. Vol.	8000h	1Ah Record Sel.	0000h	32h PCM ADC SRate	BB80h
08h Reserved	--	1Ch Record Gain	8000h	34h Reserved	--
0Ah PC Beep Vol.	8000h	1Eh Reserved	--	72h Reserved	--
0Ch Phone In Vol.	8008h	20h Gen. Purpose	0000h	74h Serial Config.	7x0xh
0Eh Mic Vol.	8008h	22h 3D Control	0000h	76h Misc. Control Bits	0404h
10h Line In Vol.	8808h	24h Reserved	--	7Ch Vender ID1	4144h
12h CD Vol.	8808h	26h Pwr Mgnt.	000xh	7Eh Vender ID2	5340h

5.8.6 AUDIO SPECIFICATIONS

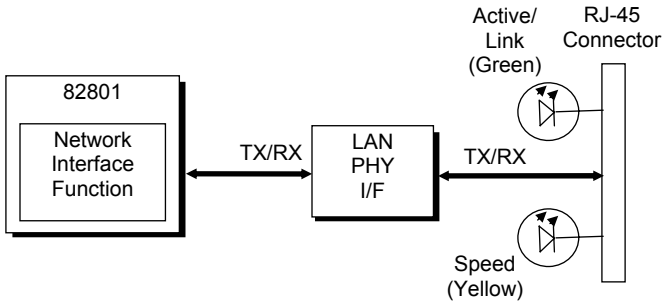
The specifications for the integrated AC'97 audio subsystem are listed in Table 5-23. The specifications listed are applicable to both D315 and d325 systems.

Table 5-23.
AC97 Audio Subsystem Specifications

Parameter	Measurement
Sampling Rate	7040 KHz to 48 KHz
Resolution	16 bit
Nominal Input Voltage:	
Mic In (w/+20 db gain)	.283 Vp-p
Line In	2.83 Vp-p
Impedance:	
Mic In	1 K ohms (nom)
Line In	10 K ohms (min)
Line Out	800 ohms
Signal-to-Noise Ratio (input to Line Out)	90 db (nom)
Frequency Response (-3db to Line Output):	
Line Input	20 Hz – 20 KHz
Mic Input	100 Hz – 12 KHz
A/D (PC record)	
Line input	20 Hz – 19.2 KHz
Mic input	100 Hz – 8.8 Khz
D/A (PC playback)	20 Hz – 19.2 KHz
Max. Power Output (with 10% THD):	3 watts (into 16 ohms)
Input Gain Attenuation Range	-46.5 db
Master Volume Range	-94.5 db
Frequency Response:	
Codec	20-20 KHz
Speaker	450 - 4000 Hz

5.9 NETWORK INTERFACE CONTROLLER

The HP d325 system includes a 10/100 Mbps network interface controller (NIC) consisting of a 82562-equivalent controller integrated into the 82801 ICH component coupled with a physical interface (PHY) component and an RJ-45 jack with integral status LEDs (Figure 5-13). The support firmware is contained in the system (BIOS) ROM. The NIC can operate in half- or full-duplex modes, and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification. Transmit and receive FIFOs of 3 kilobytes each reduce the chance of overrun while waiting for bus access.



LED	Function
Green	Activity/Link: Indicates network activity and link pulse reception.
Yellow	Speed: Indicates link detection in 100 MB/s mode (always on if 100Base-Tx is forced).

Figure 5-13. Network Interface Controller Block Diagram

The Network Interface Controller includes the following features:

- Fast Ethernet controller with 32-bit architecture and 3-KB TX/RX buffers.
- Dual-mode support with auto-switching between 10BASE-T and 100BASE-TX.
- Power down and Wake up support in both APM and ACPI environments (PME- and WOL).
- Alert-on-LAN (AOL v1.0) support.
- Link and Activity LED indicator drivers
- AOL support for upgrade card

The controller features high and low priority queues and provides priority-packet processing for networks that can support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (under-sized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run.

The NIC uses 3.3 VDC auxiliary power, which allows the controller to support Wake-On-LAN (WOL) and Alert-On-LAN (AOL) functions while the main system is powered down.

NOTE: For the WOL and AOL features to function as described in the following paragraphs, the system unit must be plugged into a live AC outlet. Controlling unit power through a switchable power strip will, with the strip turned off, disable WOL and AOL functionality.

5.9.1 WAKE ON LAN SUPPORT

The NIC supports the Wired-for-Management (WfM) standard of Wake-On-LAN (WOL) that allows the system to be booted up from a powered-down or low-power condition upon the detection of special packets received over a network. The NIC receives 3.3 VDC auxiliary power while the system unit is powered down in order to process special packets. The detection of a Magic Packet by the NIC results in the PME- signal on the PCI bus to be asserted, initiating system wake-up from an ACPI S1 or S3 state.

5.9.2 ALERT ON LAN SUPPORT

Alert-On-LAN (AOL) support allows the NIC to communicate the occurrence of certain events over a network even while the system unit is powered off. In a system-off (powered down) condition the network function of the 82801 ICH component receives auxiliary +3.3 VDC power (derived from the +5 VDC auxiliary power from the power supply assembly). Certain events (listed in Table 5-24) will result in the network function of the ICH to transmit an appropriate pre-constructed message over the network to a system management console.

Reportable AOL events are listed in the following table:

Table 5-24.
AOL Events

Event	Description
BIOS Failure	System fails to boot successfully.
OS Problem	System fails to load operating system after POST.
Missing/Faulty Processor	Processor fails to fetch first instruction.
Thermal Condition	Thermal ASIC reports high temperature.
Heartbeat	Indication of system's network presence (sent approximately every 30 seconds in normal operation).

The AOL implementation requirements are as follows:

1. Intel PRO/100 VM Network Connection drivers 3.80 or later (available from Compaq).
2. Intel Alert-On-LAN Utilities, version 2.5 (available from Compaq).
3. Management console running one of the following:
   a. HP OpenView Network Node Manager 6.x
   b. Intel LANDesk Client Manager
   c. Sample Application Console from the Intel AOL Utilities (item #2 above)

5.9.3 POWER MANAGEMENT SUPPORT

The NIC features Wired-for-Management (WfM) support providing system wake up from network events (WOL) as well as generating system status messages (AOL) and supports both APM and ACPI power management environments. The controller receives 3.3 VDC (auxiliary) power as long as the system is plugged into a live AC receptacle, allowing support of wake-up events occuring over a network while the system is powered down or in a low-power state.

5.9.3.1 APM Environment

The Advanced Power Management (APM) functionality of system wake up is implemented through the system's APM-compliant BIOS and the controller's Magic Packet-compliant hardware. This environment bypasses operating system (OS) intervention allowing a plugged in unit to be turned on remotely over the network (i.e., "remote wake up"). In APM mode the controller will respond upon receiving a Magic Packet, which is a packet where the node's address is repeated 16 times. Upon Magic packet detection, the controller initiates the boot sequence.

5.9.3.2 ACPI Environment

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS **and is the default power management mode**. The following wakeup events may be individually enabled/disabled through the supplied software driver:

- Magic Packet – Packet with node address repeated 16 times in data portion

NOTE: The following functions are supported in NDIS5 drivers but implemented through remote management software applications (such as LanDesk).

- Individual address match – Packet with matching user-defined byte mask
- Multicast address match – Packet with matching user-defined sample frame
- ARP (address resolution protocol) packet
- Flexible packet filtering – Packets that match defined CRC signature

The PROSet Application software (pre-installed and accessed through the System Tray or Windows Control Panel) allows configuration of operational parameters such as WOL and duplex mode.

5.9.4 NIC PROGRAMMING

Programming the NIC consists of configuration, which occurs during POST, and control, which occurs at runtime.

5.9.4.1 Configuration

The network interface function is a PCI device and configured though PCI configuration space registers using PCI protocol described in chapter 4. The PCI configuration registers are listed in the following table:

Table 5-25.
NIC Controller PCI Configuration Registers (ICH Device 8/Function 0)

PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vender ID	8086h	2E, 2Fh	Subsystem ID	0000h
02-03h	Device ID	[1]	34h	Capabilities Pointer	DCh
04-05h	PCI Command	0000h	3Ch	Interrupt Line	00h
06-07h	PCI Status	0290h	3Dh	Interrupt Pin	01h
08h	Revision ID	Xxh	3Eh	Min. Grant	08h
09-0Bh	Class Code	0002h	3E, 3Fh	Max. Latency	38h
0Dh	Latency Timer	00h	DCh	Capability ID	01h
0Eh	Header Type	00h	DDh	Next Item Pointer	00h
10-13h	Cntrl. Reg. Base Addr. (Mem)	8	DE, DFh	Pwr. Mgmt. Functions	FE21h
14-17h	Cntrl. Reg. Base Addr. (I/O)	1	E0, E1h	Pwr. Mgmt. Cntrl./Sts	0000h
2C, 2Dh	Subsystem Vender ID	0000h	E3h	Data	--

NOTE:
Assume unmarked gaps are reserved and/or not used.
[1] ICH2 = 2449h
ICH4 = 103Ah

5.9.4.2 Control

The 82562 controller is controlled though registers that may be mapped in system memory space or variable I/O space. The registers are listed in the following table:

Table 5-26.
NIC Control Registers

Offset Addr. / Register	No. of Bytes	Offset Addr. / Register	No. of Bytes
00h SCB Status	2	19h Flow Control Register	2
02h SCB Command	2	1Bh PMDR	1
04h SCB General Pointer	4	1Ch General Control	1
08h PORT	4	1Dh General Status	1
0Ch Flash Control Reg.	2	1E-2Fh Reserved	10
0Eh EEPROM Control Reg.	2	30h Function Event Register	4
10h Mgmt. Data I/F Cntrl. Reg.	4	34h Function Event Mask Register	4
14h Rx Direct Mem. Access Byte Cnt.	4	38h Function Present State Register	4
18h Early Receive Interrupt	1	20h Force Event Register	4

Not implemented in these systems (CardBus registers).

5.9.5 NIC CONNECTOR

Figure 5-14 shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

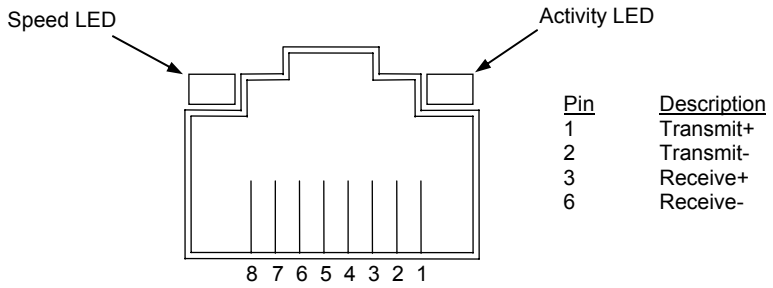


Figure 5-14. Ethernet TPE Connector (RJ-45, viewed from card edge)

5.9.6 NIC SPECIFICATIONS

Table 5-27.
NIC Specifications

Parameter	
Modes Supported	10BASE-T half duplex @ 10 MB/s 10Base-T full duplex @ 20 MB/s 100BASE-TX half duplex @ 100 MB/s 100Base-TX full duplex @ 200 MB/s
Standards Compliance	IEEE 802.2 IEEE 802.3 & 802.3u IEEE Intel priority packet (801.1p)
OS Driver Support	MS-DOS MS Windows 3.1 MS Windows 95 (pre-OSR2), 98, and 2000 Professional, XP Home, XP Pro MS Windows NT 3.51 & 4.0 Novell Netware 3.x, 4.x, 5x Novell Netware/IntraNetWare SCO UnixWare 7 OpenServer
Boot ROM Support	Intel PRO/100 Boot Agent (PXE 3.0, RPL)
F12 BIOS Support	Yes
Bus Inteface	PCI 2.2
Power Management Support	APM, ACPI, PCI Power Management Spec.

Chapter 6
INTEGRATED GRAPHICS SUBSYSTEM

6.1 INTRODUCTION

This chapter describes graphics subsystem that is integrated into the IGP component on the system board. This graphics subsystem employs the use of system memory to provide efficient, economical 2D and 3D performance.

Upgrading these systems is accomplished by installing a separate AGP graphics card in the AGP slot. The system will detect an AGP graphics controller card during the boot sequence and disable the integrated graphics controller of IGP.

This chapter covers the following subjects:

6.2 FUNCTIONAL DESCRIPTION

The NVidia NForce 220 chipset includes a graphics processing unit (GPU) integrated into the integrated graphics processor (IGP) component (Figure 6-1). The graphics controller can directly drive an external, analog multi-scan monitor at resolutions up to and including 1920 x 1440 pixels. The GPU includes a memory management feature that allocates portions of system memory for use as the frame buffer and for storing textures and 3D effects.

These systems may be upgraded by installing a separate AGP graphics card in the AGP slot, which disables the onboard IGC.

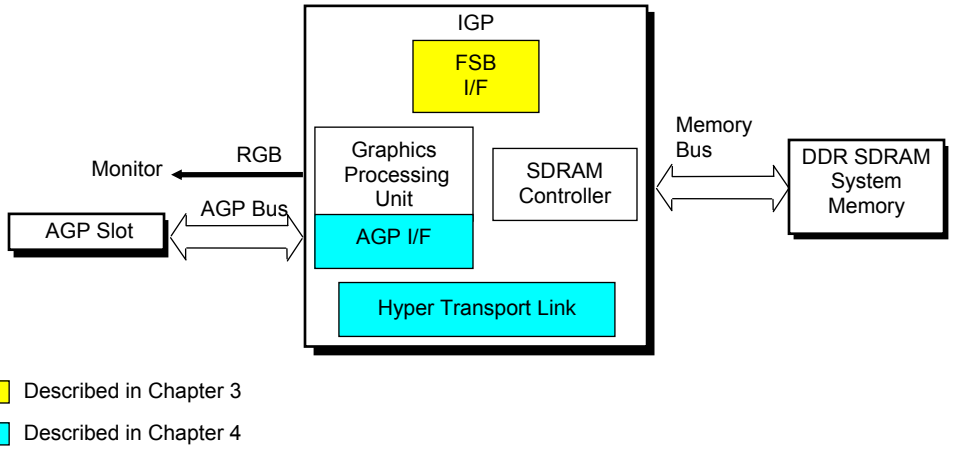
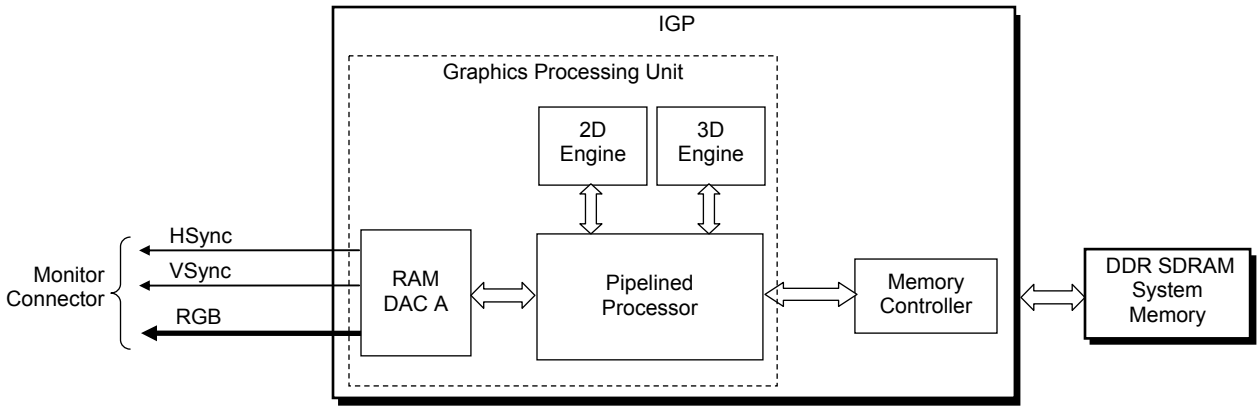


Figure 6-1. IGP-Based Graphics, Block diagram

The GPU is based on the NVidia GeForce-class of graphics controller and includes the following features:

- Transform and lighting engines.
- Per-pixel shading rasterizer.
- 256-bit 2D 3D accelerator.
- Dual-pixel pipeline with full-speed processing of two textures per pixel
- Analog monitor resolution support up to 1920 x 1440

Figure 6-2 shows the block diagram of the graphics processing unit. The GPU includes 256-bit 2D and 3D engines that work with a multi-pipelined processor. The processor provides hardware-assisted MPEG-2 decoding for DVD and HDTV video playback in resolutions up to 1280 x 720.



Difference Matrix

Feature	D315	d325
NVidia controller type	GeForce2 MX	GeForce4 MX
Pipeline performance	350 Mpixels/sec 700 texels fill rate	380 Mpixels/sec 760 texels fill rate
Transform & lighting engine rate	20 Mtriangeles/sec	24 Mtriangles/sec

Figure 6-2. IGP Graphics Controller Block diagram and Difference Matrix

The GPU works with the SDRAM Memory Controller to use a portion of system memory for instructions, textures, and frame (display) buffering. The SDRAM Memory Controller dynamically allocates display and texture memory amounts according to the needs of the application running on the system.

6.3 DISPLAY MODES

The GPU supports the following 2D display modes based on the 64-bit support of system memory:

Table 6-1.
GPU Graphics Display Modes

Resolution	Bits per pixel	Color Depth	Max. Vertical Refresh Rate
640 x 480	8	256	85
640 x 480	16	65K	85
640 x 480	24	16.7M	85
800 x 600	8	256	85
800 x 600	16	65K	85
800 x 600	24	16.7M	85
1024 x 768	8	256	85
1024 x 768	16	65K	85
1024 x 768	24	16.7M	85
1280 x 1024	8	256	85
1280 x 1024	16	65K	85
1280 x 1024	24	16.7M	85
1600 x 1200	8	256	85
1600 x 1200	16	65K	85
1600 x 1200	32	16.7M	85
1900 x 1440	8	256	85
1900 x 1440	16	65K	85
1920 x 1080	8	256	85
1920 x 1080	16	65K	85
1920 x 1200	8	256	85
1920 x 1200	16	65K	85
1920 x 1200	32	16.7M	85
1920 x 1440	8	256	75
1920 x 1440	16	65K	75
1920 x 1440	32	16.7M	75

NOTE:
2D resolutions shown.

The GPU features a 350-MHz RAMDAC that can directly drive an analog multiscan monitor up to a 2D resolution of 1920 x 1440 with 32-bit color at 75 Hz.

6.4 PROGRAMMING

The IGP's integrated graphics processing unit is configured using PCI configuration registers listed in Table 6-2.

Table 6-2.
Graphics Processing Unit PCI Configuration Registers (Device 0, Function 0, Bus 1)

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vendor ID	10DEh	2E, 2Fh	Subsystem ID	[2]
02, 03h	Device ID	[1]	30-33h	Vid. BIOS Base Addr.	[2]
04, 05h	Command	[2]	34h	Capabilities Pointer	[2]
06, 07h	Status	[2]	3Ch	Interrupt Line	[2]
08h	Revision ID	[2]	3Dh	Interrupt Pin	[2]
09-0Bh	Class Code	[2]	3Eh	Min. Grant	[2]
0Eh	Header Type	[2]	3Fh	Max. Latency	[2]
0Fh	BIST	[2]	DC, DDh	Pwr. Mgmt. Capabilities	[2]
10-13h	Memory Range Addr.	[2]	DE, DFh	Pwr. Mgmt. Capabilites	[2]
14-17h	Mem. Map Range Addr.	[2]	E0, E1h	Pwr. Mgmt. Control	[2]
2C, 2Dh	Subsys. Vendor ID	[2]	E2-FFh	Reserved	[2]

NOTE:
[1] D315, = 01A0h; d325, = 01F0h
[2] Refer to NVidia documentation for detailed register descriptions and values.

The GPU is controlled through memory-mapped registers by the appropriate software driver.

6.5 UPGRADING IGP-BASED GRAPHICS

The IGP-based graphics subsystem of these systems is upgradeable by installing an AGP graphics card into the AGP slot. The upgrade procedure is as follows:

1. Shut down the system through the operating system.
2. Unplug the power cord from the rear of the system unit.
3. Remove the chassis cover.
4. Install the AGP card into the AGP slot.
5. Replace the chassis cover.
6. Reconnect the power cord to the system unit.
7. Power up the system unit.

The BIOS will detect the presence of the AGP card and disable the GPU of the IGP.

6.6 VGA MONITOR CONNECTOR

The D315 model provides a standard VGA connector (Figure 6-3) for attaching an analog video monitor. The D325 model provides two VGA connectors.

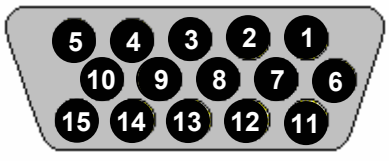


Figure 6-3. VGA Monitor Connector, (Female DB-15, as viewed from rear).

Table 6-3.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	PWR	+5 VDC (fused) [1]
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	NC	Not Connected
4	NC	Not Connected	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSync	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

NOTES:
[1] Fuse automatically resets when excessive load is removed.

Chapter 7
POWER and SIGNAL DISTRIBUTION

7.1 INTRODUCTION

This chapter describes the power supply and method of general power and signal distribution. Topics covered in this chapter include:

7.2 POWER SUPPLY ASSEMBLY/CONTROL

These systems features a power supply assembly that is controlled through programmable logic (Figure 7-1).

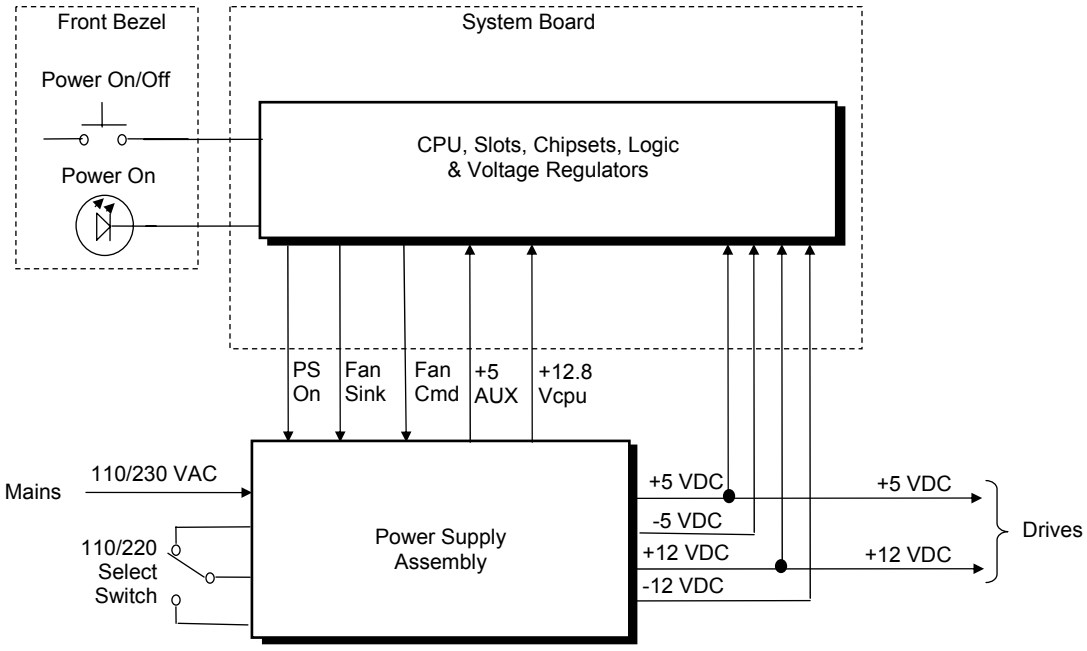


Figure 7-1. Power Distribution and Control, Block Diagram

7.2.1 POWER SUPPLY ASSEMBLY

The D315 models use a 220-watt power supply assembly with the specifications listed in the following table:

Table 7-1.
220-Watt Power Supply Assembly Specifications

	Range/ Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
115VAC setting	90 - 132 VAC	--	--	--	--
230VAC setting	180 - 264 VAC				
Line Frequency	47 - 63 Hz	--	--	--	--
Constant Input (AC) Current	--	--	6.00 A	--	--
+3.33 VDC Output	+/- 4%	1.0 A	15.0 A	15.0 A	50 mV
+5 VDC Output	+/- 5 %	1.0 A	11.0 A	11.0 A	50 mV
+5.05 AUX Output	+/- 4 %	0.0 A	3.00 A	3.00 A	50 mV
+12 VDC Output	+/- 5 %	0.1 A	5.00 A	7.50 A	120 mV
+12.8 VDC Output (Vcpu)	+/- 12 %	0.0 A	7.50 A	7.50 A	200 mV
-12 VDC Output	+/- 10 %	0.0 A	0.15 A	0.15 A	200 mV

NOTES:
[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.
[2] Surge duration no longer than 10 seconds with 12-volt tolerance +/- 10%.

The D325 models use a 240-watt power supply assembly with the specifications listed in the following table:

Table 7-2.
240-Watt Power Supply Assembly Specifications

	Range/ Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
115VAC setting	90 - 132 VAC	--	--	--	--
230VAC setting	180 - 264 VAC				
Line Frequency	47 - 63 Hz	--	--	--	--
Constant Input (AC) Current	--	--	6.00 A	--	--
+3.33 VDC Output	+/- 3.3%	1.0 A	19.0 A	19.0 A	50 mV
+5.08 VDC Output	+/- 3.3 %	1.0 A	14.0 A	14.0 A	50 mV
+5.08 AUX Output	+/- 4 %	0.0 A	3.00 A	3.00 A	50 mV
+12 VDC Output	+/- 5 %	0.1 A	5.00 A	7.50 A	120 mV
+12.8 VDC Output (Vcpu)	+14/- 10 %	0.0 A	9.00 A	9.00 A	200 mV
-12 VDC Output	+/- 10 %	0.0 A	0.15 A	0.15 A	200 mV

NOTES:
[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.
[2] Surge duration no longer than 10 seconds with 12-volt tolerance +/- 10%.

7.2.2 POWER CONTROL

The power supply assembly is controlled digitally by the PS On signal (Figure 7-1). When PS On is asserted, the Power Supply Assembly is activated and all voltage outputs are produced. When PS On is de-asserted, the Power Supply Assembly is off and all voltages (except +5 AUX) are not generated. **Note that the +5 AUX voltage is always produced as long as the system is connected to a live AC source.**

7.2.2.1 Power Button

The PS On signal is typically controlled through the Power Button which, when pressed and released, applies a negative (grounding) pulse to the power control logic. The resultant action of pressing the power button depends on the state and mode of the system at that time and is described as follows:

System State	Pressed Power Button Results In:
Off	Negative pulse, of which the falling edge results in power control logic asserting PS On signal to Power Supply Assembly, which then initializes. ACPI four-second counter is not active.
On, ACPI Disabled	Negative pulse, of which the falling edge causes power control logic to de-assert the PS On signal. ACPI four-second counter is not active.
On, ACPI Enabled	Pressed and Released Under Four Seconds: Negative pulse, of which the falling edge causes power control logic to generate SMI-, set a bit in the SMI source register, set a bit for button status, and start four-second counter. Software should clear the button status bit within four seconds and the Suspend state is entered. If the status bit is not cleared by software in four seconds PS On is de-asserted and the power supply assembly shuts down (this operation is meant as a guard if the OS is hung). Pressed and Held At least Four Seconds Before Release: If the button is held in for at least four seconds and then released, PS On is negated, de-activating the power supply.

7.2.2.2 Wake Up Events

The PS On signal can be activated with a power "wake-up" of the system due to the occurrence of a magic packet, serial port ring, or PCI power management (PME) event. These events can be individually enabled through the Setup utility to wake up the system from a sleep (low power) state.

NOTE: Wake-up functionality requires that certain circuits receive auxiliary power while the system is turned off. The system unit must be plugged into a live AC outlet for wake up events to function. **Using an AC power strip to control system unit power will disable wake-up event functionality.**

The wake up sequence for each event occurs as follows:

Wake-On-LAN

The network interface controller (NIC) can be configured for detection of a "Magic Packet" and wake the system up from sleep mode through the assertion of the PME- signal on the PCI bus. Refer to Chapter 5, section 5.9, "Network Interface Controller" for more information.

Power Management Event

A power management event that asserts the PME- signal on the PCI bus can be enabled to cause the power control logic to generate the PS On. Note that the PCI card must be PCI ver. 2.2 compliant to support this function.

7.2.3 POWER MANAGEMENT

These systems include power management functions designed to conserve energy. These functions are provided by a combination of hardware, firmware (BIOS) and software. The system provides the following power management features:

- ACPI v1.0b compliant (ACPI modes C1, C2, S1, and S3,)
- API 1.2 compliant (D315 only)
- U.S. EPA Energy Star compliant

Table 7-2 shows the comparison in power states.

Table 7-2.
System Power States

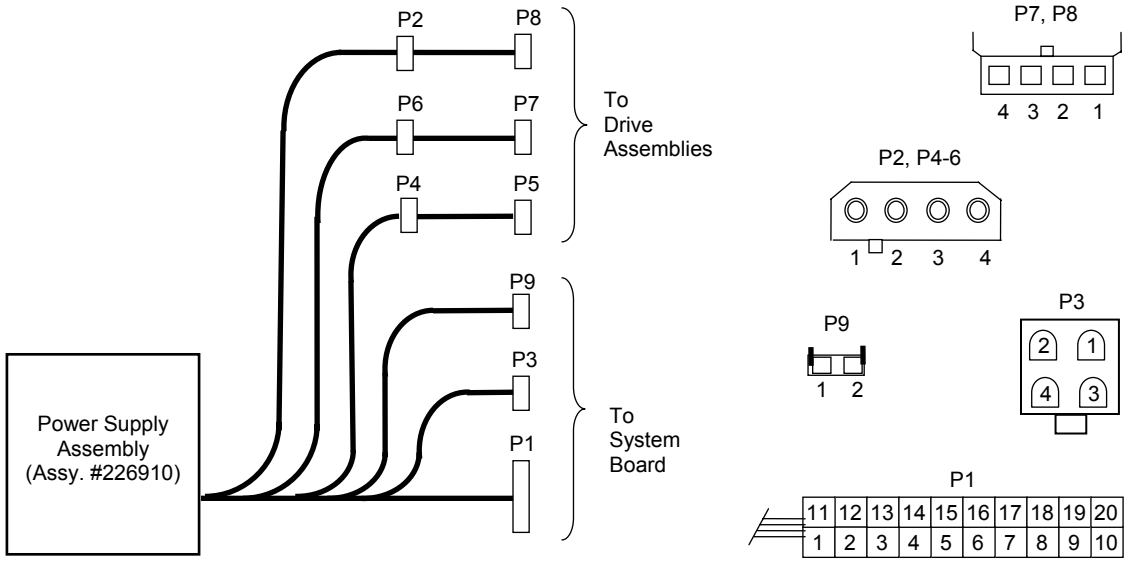
Power State	System Condition	Power Consumption	Transition To S0 by [2]	OS Restart Required
G0, S0, D0	System fully on. OS and application is running, all components.	Maximum	N/A	No
G1, S1, C1, D1	System on, CPU is executing and data is held in memory. Some peripheral subsystems may be on low power. Monitor is blanked.	Low	< 2 sec after keyboard or pointing device action	No
G1, S2/3, C2, D2 (Standby/ suspend)	System on, CPU not executing, cache data lost. Memory is holding data, display and I/O subsystems on low power.	Low	< 5 sec. after keyboard, pointing device, or power button action	No
G1, S4, D3 (Hibernation)	System off. CPU, memory, and most subsystems shut down. Memory image saved to disk for recall on power up.	Low	<25 sec. after power button action	Yes
G2, S5, $D3_{cold}$	System off. All components either completely shut down or receiving minimum power to perform system wake-up.	Minimum	<35 sec. after power button action	Yes
G3	System off (mechanical). No power to any internal components except RTC circuit. [1]	None	—	—

NOTES:
G*n* = Global state.
S*n* = Sleep state.
C*n* = ACPI state.
D*n* = PCI state.
[1] Power cord is disconnected for this condition.
[2] Actual transition time dependent on OS and/or application software.

7.3 POWER DISTRIBUTION

7.3.1 3.3/5/12 VDC DISTRIBUTION

The power supply assembly includes a multi-connector cable assembly that routes DC power to the system board as well as to the individual drive assemblies. Figure 7-2 shows the power supply cabling for D315 models while figure 7-3 shows the power supply cabling for the d325 model.



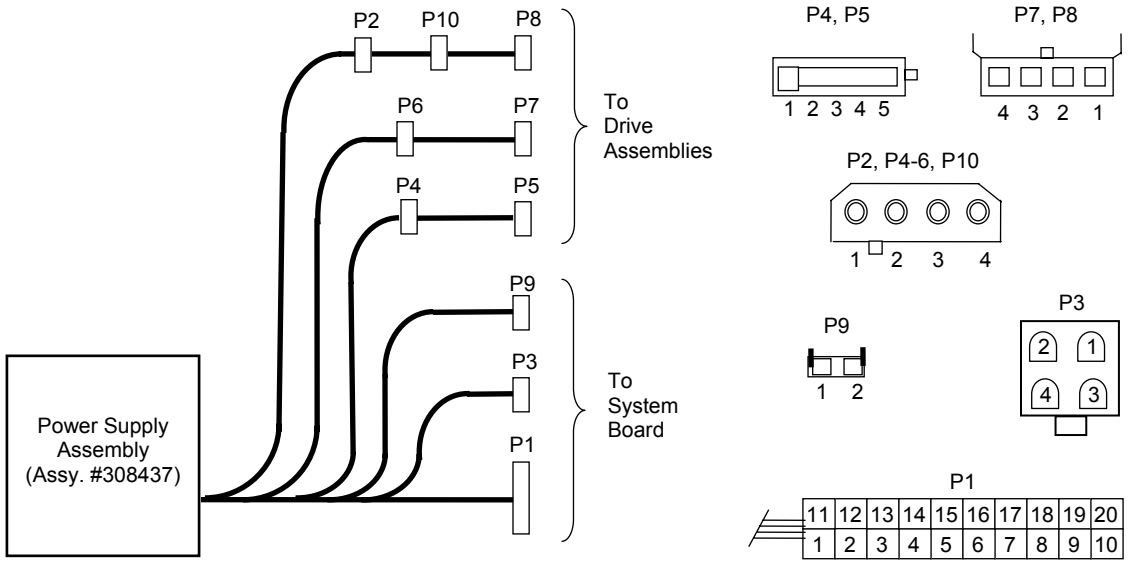
Conn.	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
P1	+3.3	+3.3	RTN	+5	RTN	+5	RTN	POK	+5 Aux	+12
P1 [1]	+3.3	-12	RTN	PS On	RTN	RTN	RTN	NC	+5	+5
P2, 4-6	+12	GND	GND	+5						
P3	GND	GND	+12.8	+12.8						
P7, 8	+5	GND	GND	+12						
P9	FS	FC								

NOTES:

Connectors not shown to scale.
All + and - values are VDC.
RTN = Return (signal ground)
GND = Power ground
RS = Remote sense
POK = Power OK
NC = Not connected
FS = Fan Sink
FC = Fan Command
[1] This row represents pins 11 - 20 of connector P1

Figure 7-2. D315 Model Power Cable Diagram

Figure 7-3 shows the power supply cabling for the d325 model.



Conn.	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
P1	+3.3	+3.3	RTN	+5	RTN	+5	RTN	POK	+5 Aux	+12
P1 [1]	+3.3	-12	RTN	PS On	RTN	RTN	RTN	NC	+5	+5
P4, 5	+3.3	RTN	+5	RTN	+12					
P6, 10	+12	GND	GND	+5						
P3	GND	GND	+12.8	+12.8						
P7, 8	+5	GND	GND	+12						
P9	NC	FC								

NOTES:

Connectors not shown to scale.
All + and - values are VDC.
RTN = Return (signal ground)
GND = Power ground
RS = Remote sense
POK = Power OK
NC = Not connected
FC = Fan Command
[1] This row represents pins 11 - 20 of connector P1

Figure 7-3. d325 Model Power Cable Diagram

7.3.2 LOW VOLTAGE PRODUCTION/DISTRIBUTION

Voltages less than 3.3 VDC including processor core (VCore) voltage are produced through regulator circuitry (Figure 7-4) on the system board.

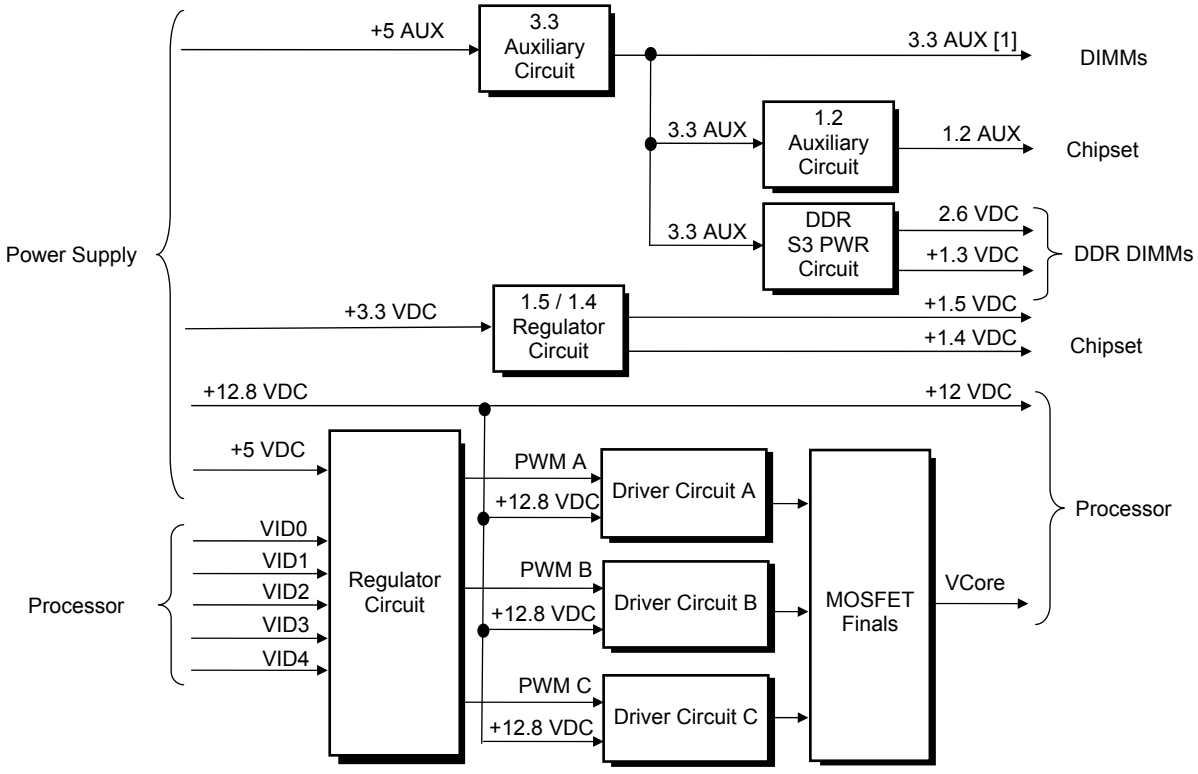


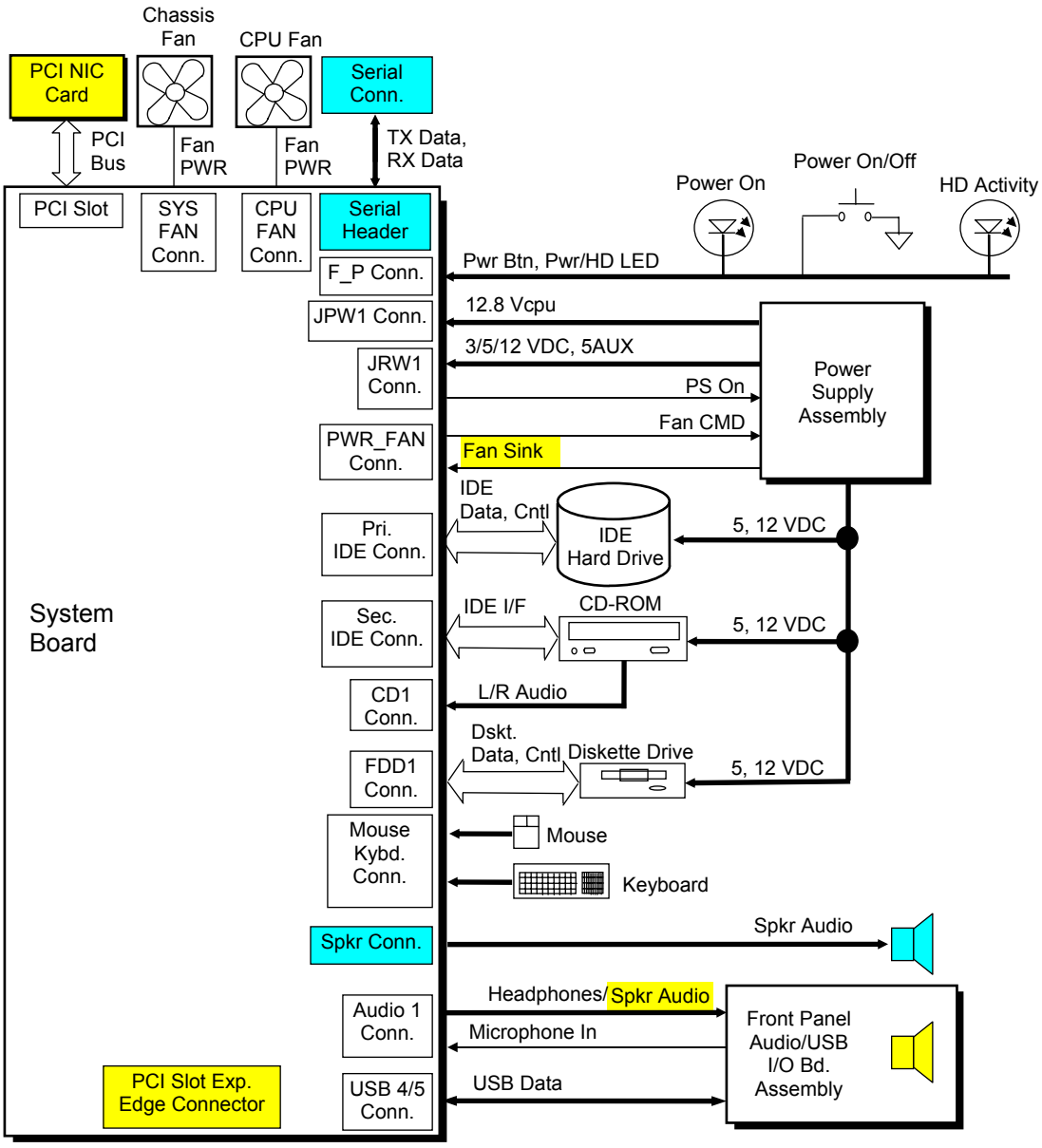
Figure 7-4. Low Voltage Supply and Distribution Diagram

The regulator produces the VCore (processor core) voltage according to the strapping of signals VID4..0 by the processor. The possible voltages available are listed as follows:

VID 4..0	VCore	VID 4..0	VCore	VID 4..0	VCore
00000	1.850	01011	1.575	10110	1.300
00001	1.825	01100	1.550	10111	1.275
00010	1.800	01101	1.525	11000	1.250
00011	1.775	01110	1.500	11001	1.225
00100	1.750	01111	1.475	11010	1.200
00101	1.725	10000	1.450	11011	1.175
00110	1.700	10001	1.425	11100	1.150
00111	1.675	10010	1.400	11101	1.125
01000	1.650	10011	1.375	11110	1.100
01001	1.625	10100	1.350	11111	Off
01010	1.600	10101	1.325	--	--

7.4 SIGNAL DISTRIBUTION

Figure 7-5 shows general signal distribution between the main subassemblies of the system units.



NOTES:

Applies to both D315 and d325 models unless otherwise indicated.
D315 models only.
d325 m odels only.

Figure 7-5. Signal Distribution Diagram

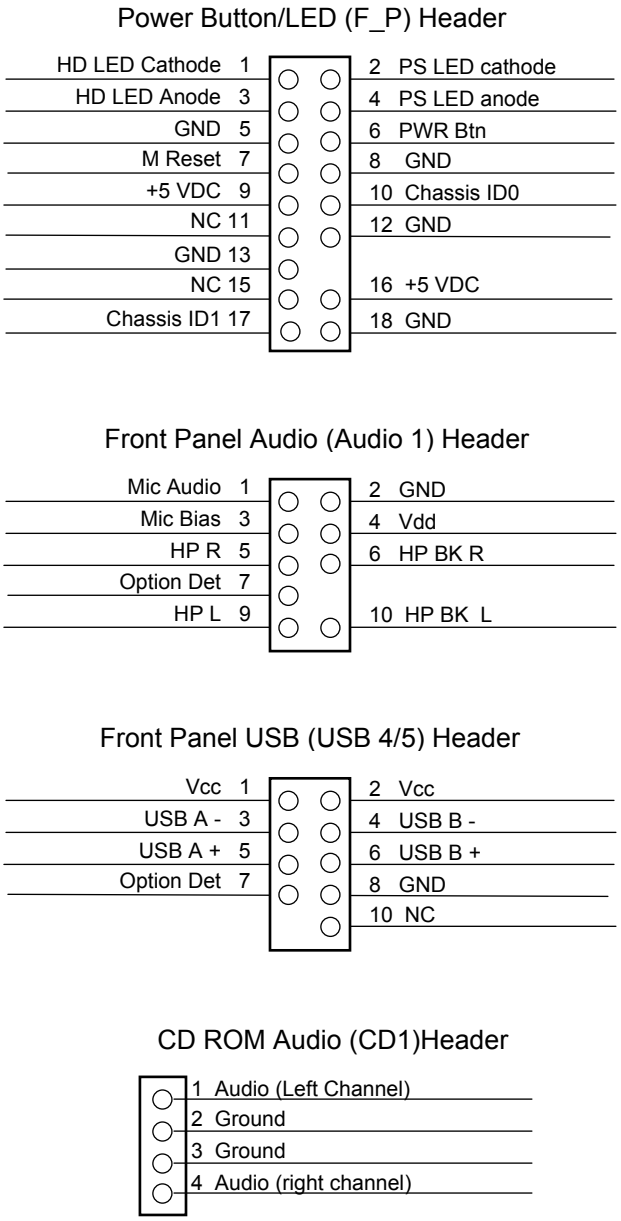


Figure 7-6. Miscellaneous Header Pinouts

Chapter 8
SYSTEM BIOS

8.1 INTRODUCTION

The Basic Input/Output System (BIOS) of the computer is a collection of machine language programs stored as firmware in read-only memory (ROM). The ROM includes such functions as Power-On Self Test (POST), VGA BIOS, PCI device initialization, Plug 'n Play support, ACPI power management activities, and the Setup utility. The firmware contained in the BIOS ROM supports the following operating systems and specifications:

- Windows 95, 98SE, 2000, XP Home, XP Professional, and Mandrake Linux 8.2
- Windows NT 4.0 (SP6 required for PnP support)
- OS/2 ver 2.1 and OS/2 Warp
- SCO Unix
- DMI 2.1
- Intel Wired for Management (WfM) ver. 2.2
- Wake-On-LAN (WOL)
- ACPI and OnNow
- SMBIOS 2.3.1
- PC98/99/00 and NetPC
- BIOS Boot Specification 1.01
- Enhanced Disk Drive Specification 3.0
- "El Torito" Bootable CD-ROM Format Specification 1.0
- ATAPI Removeable Media Device BIOS Specification 1.0

The BIOS firmware is contained in a flash ROM component. The runtime portion of the BIOS resides in a 128KB block from E0000h to FFFFFh.
This chapter includes the following topics:

8.2 ROM FLASHING/UPGRADING

The system BIOS firmware is contained in a flash ROM device that can be re-written with BIOS code (using the ROMPaq utility or a remote flash program) allowing easy upgrading, including changing the splash screen displayed during the POST routine.

Upgrading the BIOS is not normally required but may be necessary if changes are made to the unit's operating system, hard drive, or processor. All BIOS ROM upgrades are available directly from Hewlett-Packard. Flashing is done either locally with the CPQFLASH or HPQFlash Windows program, a ROMPaq diskette, or remotely using the network boot function (described in the section 8.3.2).

This system includes 64 KB of write-protected boot block ROM that provides a way to recover from a failed flashing of the system BIOS ROM. If the BIOS ROM fails the flash check, the boot block code provides the minimum amount of support necessary to allow booting the system from the diskette drive and re-flashing the system ROM with a ROMPaq diskette. Note that if an administrator password has been set in the system the boot block will prompt for this password by illuminating the caps lock keyboard LED and displaying a message if video support is available. A PS/2 keyboard must be used during bootblock operation.

Since video may not be available during the initial boot sequence the boot block routine uses the Num Lock, Caps Lock, and Scroll Lock LEDs of the PS/2 keyboard to communicate the status of the ROM flash as follows:

Table 8-1.
Boot Block Codes

Num Lock LED	Cap Lock LED	Scroll Lock LED	Meaning
Off	On	Off	Administrator password required.
On	Off	Off	Boot failed. Reset required for retry.
Off	Off	On	Flash failed.
On	On	On	Flash complete.

8.3 BOOT FUNCTIONS

The BIOS supports various functions related to the boot process, including those that occur during the Power On Self-Test (POST) routine.

8.3.1 BOOT DEVICE ORDER

The default boot device order is as follows:

1. IDE CD-ROM drive (EL Torito CD images)
2. Diskette drive (A)
3. MultiBay device (A: or CD-ROM) if applicable
4. USB device
5. Hard drive (C)
6. Network interface controller

The order can be changed in the ROM-based Setup utility (accessed by pressing F10 when so prompted during POST). Entries are displayed only if the actual device is attached, with the exception of the USB device, which is always displayed even if a USB storage device is not present. The hot IPL option is available through F9 during the POST routine. The order defined by the Setup (F10) can be overridden once by pressing the F9 key during the boot process.

8.3.2 NETWORK BOOT (F12) SUPPORT

The BIOS supports booting the system to a network server. The function is accessed by pressing the F12 key when prompted at the lower right hand corner of the display during POST. Booting to a network server allows for such functions as:

- Flashing a ROM on a system without a functional operating system (OS).
- Installing an OS.
- Installing an application.

8.3.3 MEMORY DETECTION AND CONFIGURATION

This system uses the Serial Presence Detect (SPD) method of determining the installed DIMM configuration. The BIOS communicates with an EEPROM on each DIMM through the SMBus to obtain data on the following DIMM parameters:

- Presence
- Size
- Type
- Timing/CAS latency
- Memory speed

NOTE: Refer to Chapter 3, "Processor/Memory Subsystem" for the SPD format and DIMM data specific to this system.

The BIOS performs memory detection and configuration with the following steps:

1. Program the buffer strength control registers based on SPD data and the DIMM slots that are populated.
2. Determine the common CAS latency that can be supported by the DIMMs.
3. Determine the memory size for each DIMM and program the graphics controller accordingly.
4. Enable refresh
5. Determine if the memory configuration will allow for double-clocked 133-MHz memory operation and program the memory clock and IGP (see note below)

NOTE: The BIOS must read a value of 07h (indicating DDR) from SPD byte 02h of each DIMM in order to validate the memory.

8.3.4 BOOT ERROR CODES

The BIOS provides visual and audible indications of a failed system boot by using the keyboard LEDs and the system speaker. The error conditions are listed in the following table.

Table 8-2. Boot Error Codes

Visual [1]	Audible	Meaning
Num Lock LED blinks	1 short, 2 long beeps	System memory not present or incompatible.
Scroll Lock LED blinks	2 long, 1 short beeps	Hardware failure before graphics initialization.
Caps Lock LED blinks	1 long, 2 short beeps	Graphics controller not present or failed to initialize.
Num, Caps, Scroll Lock LEDs blink	1 long, 3 short beeps	ROM failure.
Num, Caps, Scroll Lock LEDs blink in sequence	none	Network service mode

NOTE:
[1] Provided with PS/2 keyboard only.

8.4 SETUP UTILITY

The Setup utility (stored in ROM) allows the user to configure system functions involving security, power management, and system resources. The Setup utility is ROM-based and invoked when the F10 key is pressed during the time the F10 prompt is displayed in the lower right-hand corner of the screen during the POST routine. Highlights of the Setup utility are described in the following table.

NOTE: Support for Computer Setup options may vary depending on your specific hardware configuration.

Table 8-3. Setup Utility Functions

Table 8-3.
Setup Utility Functions

Heading	Option	Description
File	System Information	Lists: Product name Processor type/speed/stepping Cache size (L1/L2) FSB frequency Integrated MAC address System ROM (includes family name and version) Chassis serial number Asset tracking number Integrated MAC for embedded, enabled NIC (if applicable)
	About	Displays copyright notice.
	Set Time and Date	Allows you to set system time and date.
	Save to Diskette	Saves system configuration, including CMOS, to a blank, formatted 1.44-MB diskette.
	Restore from Diskette	Restores system configuration, including CMOS, from a diskette.
	Set Defaults and Exit	Restores factory default settings, which includes clearing any established passwords.
	Ignore Changes and Exit	Exits Computer Setup without applying or saving any changes.
	Save Changes and Exit	Saves changes to system configuration and exits Computer Setup.
Storage	Device Configuration	Lists all installed storage devices. The following options appear when a device is selected: **Diskette Type** (For legacy diskette drives only) Identifies the highest capacity media type accepted by the diskette drive. Options are 3.5" 1.44 MB and 5.25" 1.2 MB. **Drive Emulation** Allows you to select a drive emulation type for a storage device. (For example, a Zip drive can be made bootable by selecting hard disk or diskette emulation.) Selecting “None” prevents the device from being accessed by BIOS or though DOS. Operating systems that use their own mass storage drivers will not be affected by choosing “None.” **Transfer Mode** (IDE devices only) Specifies the active data transfer mode. Options (subject to device capabilities) are PIO 0, Max PIO, Enhanced DMA, Ultra DMA 0, and Max UDMA.

Continued

Table 8-3. Setup Utility Functions *Continued*

Heading	Option	Description
Storage *(continued)*	Device Configuration *(continued)*	**Translation Mode** (IDE disks only) Lets you select the translation mode to be used for the device. This enables the BIOS to access disks partitioned and formatted on other systems and may be necessary for users of older versions of Unix (e.g., SCO Unix version 3.2). Options are Bit-Shift, LBA Assisted, User, and None.
		 **CAUTION:** Ordinarily, the translation mode selected automatically by the BIOS should not be changed. If the selected translation mode is not compatible with the translation mode that was active when the disk was partitioned and formatted, the data on the disk will be inaccessible.
		Translation Parameters (IDE Disks only) Allows you to specify the parameters (logical cylinders, heads, and sectors per track) used by the BIOS to translate disk I/O requests (from the operating system or an application) into terms the hard drive can accept. Logical cylinders may not exceed 1024. The number of heads may not exceed 256. The number of sectors per track may not exceed 63. These fields are only visible and changeable when the drive translation mode is set to User. **Multisector Transfers** (IDE ATA devices on*ly*) Specifies how many sectors are transferred per multi-sector PIO operation. Options (subject to device capabilities) are Disabled, 8, and 16.
	Storage Options	**Removable Media Boot** Enables/disables ability to boot the system from removable media. **Note**: After saving changes to Removable Media Boot, the computer will restart. Turn the computer off, then on, manually.
		Removable Media Write Enables/disables ability to write data to removable media. **Note**: This feature applies only to legacy diskette, IDE LS-120 Superdisk, and IDE PD-CD drives.
		Primary IDE Controller Allows you to enable or disable the primary IDE controller.
		Secondary IDE Controller Allows you to enable or disable the secondary IDE controller.
		BIOS IDE DMA Transfers Allows the user to enable or disable the use of IDE DMA transfers by the BIOS. Default setting is “enabled.”
		Diskette MBR Validation Allows you to enable or disable strict validation of the diskette Master Boot Record (MBR). **Note:** If you use a bootable diskette image that you *know* to be valid, and it does not boot with Diskette MBR Validation enabled, you may need to disable this option in order to use the diskette.

Continued

Table 8-3. Setup Utility Functions *Continued*

Heading	Option	Description
Storage *(continued)*	DPS Self-Test	Allows user to execute self-tests on IDE hard drives capable of performing the Drive Protection System (DPS) self-tests. Note: This selection will only appear when at least one drive capable of performing the IDE DPS self-tests is attached to the system
	Boot Order	Allows user to specify the order in which attached peripheral devices (such as diskette drive, hard drive, CD-ROM, or network interface card) are checked for a bootable operating system image. Each device on the list may be individually excluded from or included for consideration as a bootable operating system source. **Note**: MS-DOS drive lettering assignments may not apply after a non-MS-DOS operating system has started. To boot **one time** from a device other than the default device specified in Boot Order, restart the computer and press F9 when the F10=Setup message appears on the screen. When POST is completed, a list of bootable devices is displayed. Use the arrow keys to select a device and press the Enter key.
	Controller Order	Allows user to specify order of attached hard drive controllers. First controller will have priority in boot sequence and will be recognized as drive C (if any devices are attached). This selection will not appear if all hard drives are attached to embedded IDE controllers.
Security	Setup Password	Allows user to set and enable setup (administrator) password. **Note**: If the setup password is set, it is required to change Computer Setup options, flash the ROM, and make changes to certain plug and play settings under Windows. Also, this password must be set in order to use some Compaq remote security tools. See the *Troubleshooting Guide* for more information.
	Power-On Password	Allows user to set and enable power-on password. See the *Troubleshooting Guide* for more information.
	Password Options	Allows user to: Prompt password on warm boot. Enable/disable network server mode. **Note:** This selection will appear only if a power-on password is set. Specify whether password is required for warm boot (CTRL+ALT+DEL). **Note**: This selection is available only when Network Server Mode is disabled. See the *Desktop Management Guide* for more information.
	Smart Cover	Allows user to: Enable/disable the Smart Cover Lock Enable/disable Smart Cover Sensor. **Notify User** alerts the user that the sensor has detected that the cover has been removed**. Setup Password** requires that the setup password be entered to boot the computer if the sensor detects that the cover has been removed. Feature supported on select models only. Refer to the *Desktop Management Guide* for more information.

Continued

Table 8-3. Setup Utility Functions *Continued*

Heading	Option	Description
Security *(continued)*	Device Security	Enables/disables serial, parallel, and USB ports, system audio, and network controller.
	Network Service Boot	Enables/disables the computer's ability to boot from an operating system installed on a network server. (Feature available on NIC models only; the network controller must reside on the PCI bus or be embedded on the system board.)
	System IDs	Allows user to set: Asset tag (16-byte identifier) and Ownership Tag (80-byte identifier displayed during POST) - Refer to the *Desktop Management* guide for more information Keyboard locale setting (e.g., English or German) for System ID entry.
	DriveLock (Select models only. Appears only when at least one drive that supports DriveLock is attached)	Allows user to assign or modify a master or user password for select IDE hard drives. Whe enabled, user is prompted to enter a password, which is necessary for accessing the hard drive.
	Master Boot Record Security	Allows user to enable or disable Master Boot Record (MBR) Security. When enabled, the BIOS rejects all requests to write to the MBR on the current bootable disk. Each time the computer is powered on or rebooted, the BIOS compares the MBR of the current bootable disk to the previously-saved MBR. If changes are detected, you are given the option of saving the MBR on the current bootable disk, restoring the previously-saved MBR, or disabling MBR Security. You must know the setup password, if one is set. **Note**: Disable MBR Security before intentionally changing the formatting or partitioning of the current bootable disk. Several disk utilities (such as FDISK and FORMAT) attempt to update the MBR. If MBR Security is enabled and disk accesses are being serviced by the BIOS, write requests to the MBR are rejected, causing the utilities to report errors. If MBR Security is enabled and disk accesses are being serviced by the operating system, any MBR change will be detected by the BIOS during the next reboot, and an MBR Security warning message will be displayed.
	Save Master Boot Record	Saves a backup copy of the Master Boot Record of the current bootable disk. **Note**: Only appears if MBR Security is enabled.
	Restore Master Boot Record	Restores the backup Master Boot Record to the current bootable disk. **Note**: Only appears if all of the following conditions are true: MBR Security is enabled A backup copy of the MBR has been previously saved The current bootable disk is the same disk from which the backup copy of the MBR was saved.

Continued

Table 8-3. Setup Utility Functions *Continued*

Heading	Option	Description
Advanced (Advanced users only)	Power-On Options	Allows user to set: POST mode (QuickBoot, FullBoot, or FullBoot every 1-30 days) POST messages (enable/disable) Safe POST (enable/disable) POST delay (in seconds: none, 5, 10, 15, 20) F9 prompt (anable/disable) F10 prompt (enable/disable) F12 prompt (enable/disable) Option ROM prompt (enable/disable) Remote wakeup boot sequence (remote server/local hard drive) After power loss (off/on) If you connect your computer to an electric power strip, and would like to turn on power to the computer using the switch on the power strip, set this option to on. **Note:** If you turn off power to your computer using the switch on a power strip, you will not be able to use the suspend/sleep feature or the Remote Management features. UUID (Universal Unique Identifier) (enable/disable) I/O ACPI Mode (enable/disable) ACPI/USB buffers @ Top of Memory (enable/disable) No Keyboard Mode (enable/disable)
	Onboard Devices	Allows you to set resources for or disable onboard system devices (diskette controller, serial port, parallel port).
	PCI Devices	Lists currently installed PCI devices and their IRQ settings. Allows you to reconfigure IRQ settings for these devices or to disable them entirely.

Continued

Table 8-3. Setup Utility Functions *Continued*

Heading	Option	Description
Advanced *(continued)*	Bus Options	Allows user to enable or disable: PCI bus mastering, which allows a PCI device to take control of the PCI bus PCI SERR# Generation. PCI VGA palette snooping, which sets the VGA palette snooping bit in PCI configuration space; this is only needed with more than one graphics controller installed
	Device Options	Allows user to set: Printer mode (bi-directional, EPP & ECP, output only) Num Lock state at power-on (off/on) S5 Wake On LAN (enable/disable WOL from S5 with integrated NIC only) Processor cache (enable/disable) Processor Number (enable/disable) for Pentium III processors. ACPI S3 support (enable/disable). S3 is an ACPI (advanced configuration and power interface) sleep state that some add-in hardware options may not support. AGP Aperture size (options vary depending on platform) allows you to modify the size of your AGP aperture size window. NIC PxE Option ROM Download (enable/disable) ACPI Video Repost, HD Reset, and PS2 Mouse wake up (enable/disable) Frame Buffer Size (AUTO, 16, 32, 64, 128) Monitor Tracking (enable/disable) C1 Halt Disconnect (enable/disable) Integrated Video (enable/disable) [visible only when a PCI video card is installed]
	PCI VGA Configuration	Appears only if there are multiple PCI video adapters in the system. Allows users to specify which VGA controller will be the “boot” or primary VGA controller.

8.5 CLIENT MANAGEMENT FUNCTIONS

Table 8-4 is a partial list of the client management BIOS functions supported by the systems covered in this guide. These functions, designed to support intelligent manageability applications, are Compaq-specific unless otherwise indicated.

Table 8-4.
Client Management Functions (INT15)

AX	Function	Mode
E800h	Get system ID	Real, 16-, & 32-bit Prot.
E813h	Get monitor data	Real, 16-, & 32-bit Prot.
E814h	Get system revision	Real, 16-, & 32-bit Prot.
E816h	Get temperature status	Real, 16-, & 32-bit Prot.
E817h	Get drive attribute	Real
E818h	Get drive off-line test	Real
E819h	Get chassis serial number	Real, 16-, & 32-bit Prot.
E820h [1]	Get system memory map	Real
E81Ah	Write chassis serial number	Real
E81Bh	Get hard drive threshold	Real
E81Eh	Get hard drive ID	Real
E827h	DIMM EEPROM Access	Real, 16-, & 32-bit Prot.

NOTE:
[1] Industry standard function.

All 32-bit protected-mode functions are accessed by using the industry-standard BIOS32 Service Directory. Using the service directory involves three steps:

1. Locating the service directory.
2. Using the service directory to obtain the entry point for the client management functions.
3. Calling the client management service to perform the desired function.

The BIOS32 Service Directory is a 16-byte block that begins on a 16-byte boundary between the physical address range of 0E0000h-0FFFFFh. The format is as follows:

Offset	No. Bytes	Description
00h	4	Service identifier (four ASCII characters)
04h	4	Entry point for the BIOS32 Service Directory
08h	1	Revision level
09h	1	Length of data structure (no. of 16-byte units)
0Ah	1	Checksum (should add up to 00h)
0Bh	5	Reserved (all 0s)

To support Windows NT an additional table to the BIOS32 table has been defined to contain 32-bit pointers for the DDC locations. The Windows NT extension table is as follows:

```
; Extension to BIOS SERVICE directory table (next paragraph)

        db      "32OS"          ; sig
        db      2               ; number of entries in table
        db      "$DDC"          ; DDC POST buffer sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; byte size
        db      "$ERB"          ; ESCD sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; bytes size
```

The service identifier for client management functions is "$CLM." Once the service identifier is found and the checksum verified, a FAR call is invoked using the value specified at offset 04h to retrieve the CM services entry point. The following entry conditions are used for calling the Desktop Management service directory:

```
INPUT:
        EAX             = Service Identifier [$CLM]
        EBX (31..8)     = Reserved
        EBX (7..0)      = Must be set to 00h
        CS              = Code selector set to encompass the physical page holding
                          entry point as well as the immediately following physical page.
                          It must have the same base. CS is execute/read.
        DS              = Data selector set to encompass the physical page holding
                          entry point as well as the immediately following physical page.
                          It must have the same base. DS is read only.
        SS              = Stack selector must provide at least 1K of stack space and be 32-bit.
        (I/O permissions must be provided so that the BIOS can support as necessary)

OUTPUT:
        AL              = Return code:
                          00h, requested service is present
                          80h, requested service is not present
                          81h, un-implemented function specified in BL
                          86h and CF=1, function not supported
        EBX             = Physical address to use as the selector BASE for the service
        ECX             = Value to use as the selector LIMIT for the service
        EDX             = Entry point for the service relative to the BASE returned in EBX
```

The following subsections provide a brief description of key Client Management functions.

8.5.1 SYSTEM ID AND ROM TYPE

Applications can use the INT 15, AX=E800h BIOS function to identify the type of system. This function will return the system ID in the BX register. These systems have the following IDs and ROM family types:

System	System ID	ROM Family	PnP ID
Compaq D315 Personal Computer	07D0h	686Y4	CPQ0047
Compaq D325 Personal Computer	0830h	786A5	CPQ0059

The ROM family and version numbers can be verified with the Setup utility or the Compaq Insight Manager or Diagnostics applications.

8.5.2 EDID RETRIEVE

The BIOS function INT 15, AX=E813h is a tri-modal call that retrieves the VESA extended display identification data (EDID). Two subfunctions are provided: AX=E813h BH=00h retrieves the EDID information while AX=E813h BX=01h determines the level of DDC support.

Input:

AX = E813h
BH = 00 Get EDID .
BH = 01 Get DDC support level

If BH = 00 then
DS:(E)SI = Pointer to a buffer (128 bytes) where ROM will return block
If 32-bit protected mode then
DS:(E)SI = Pointer to $DDC location

Output:
(Successful)

If BH = 0:
DS:SI=Buffer with EDID file.
CX = Number of bytes written
CF = 0
AH =00h Completion of command

If BH = 1:
BH = System DDC support
<0>=1 DDC1 support
<1>=1 DDC2 support
BL = Monitor DDC support
<0>=1 DDC1 support
<1>=1 DDC2 support
<2>=1 Screen blanked during transfer

(Failure)

CF = 1
AH = 86h or 87h

8.5.3 TEMPERATURE STATUS

The BIOS includes a function (INT15, AX=E816h) to retrieve the status of a system's interior temperature. This function allows an application to check whether the temperature situation is at a Normal, Caution, or Critical condition.

8.5.4 DRIVE FAULT PREDICTION

The Compaq BIOS directly supports Drive Fault Prediction for IDE-type hard drives. This feature is provided through two Client Management BIOS calls. Function INT 15, AX=E817h is used to retrieve a 512-byte block of drive attribute data while the INT 15, AX=E81Bh is used to retrieve the drive's warranty threshold data. If data is returned indicating possible failure then the following message is displayed:

"1720-SMART Hard Drive detects imminent failure"

8.6 POWER MANAGEMENT FUNCTIONS

The BIOS provides two types of power management support: independent PM support ACPI support.

NOTE: The D315 models support both the independent PM (aka "APM") and the ACPI Modes. The d325 models support only the ACPI mode.

8.6.1 INDEPENDENT PM SUPPORT (D315 only)

The BIOS can provide power management (PM) of the system independently from an operating system that doesn't support APM (including DOS, Unix, NT & older versions of OS/2). In the Independent PM environment the BIOS and hardware timers determine when to switch the system to a different power state. State switching is not reported to the OS.

8.6.1.1 Staying Awake In Independent PM

There are two "Time-out to Standy" timers used in independent PM: the System Timer and the IDE Hard Drive Timer.

System Timer

In POST, the BIOS enables a timer in the south bridge component that generates an SMI once per minute. When the BIOS detects the SMI it checks status bits in the south bridge for device activity. If any of the device activity status bits are set at the time of the 1-minute SMI, BIOS resets the time-out minute countdown. The system timer can be configured through the Setup utility for counting down 0, 5, 10, 15, 20, 30, 40, 50, 60, 120, 180, or 240 minutes. The following devices are checked for activity:

- Keyboard
- Mouse
- Serial port(s)
- Parallel port
- IDE primary controller

NOTE: The secondary controller is NOT included. This is done to support auto-sense of a CD-ROM insertion (auto-run) in case Windows or NT is running. ote also that SCSI drive management is the responsibility of the SCSI river. Any IDE hard drive access resets the hard drive timer.

IDE Hard Drive Timer

During POST, an inactivity timer each IDE hard drive is set to control hard drive spin down. Although this activity is independent of the system timer, the system will not go to sleep until the primary IDE controller has been inactive for the **system** time-out time. The hard drive timer can be configured through the Setup utility for being disabled or counting down 10, 15, 20, 30, 60, 120, 180, or 240 minutes, after which time the hard drive will spin down.

8.6.1.2 Going to Sleep in Independent PM

When a time-out timer expires, Standby for that timer occurs.

System Standby

When the system acquires the Standby mode the BIOS blanks the screen. Since the hard drive inactivity timer is in the drive and triggered by drive access, the system can be in Standby with the hard drives still spinning (awake).

NOTE: The BIOS does not turn the fan(s) off (as on previous products).

IDE Hard Drive Standby

During hard drive standby the platters stop spinning. Depending on drive type, some hard drives will also cut power to some of the drive electronics that are not needed. The drives can be in this state with the system still awake.

8.6.1.3 Suspend

Suspend is not supported in the Independent PM mode.

8.6.1.4 System OFF

When the system is turned Off but still plugged into a live AC outlet the NIC, ICH2, and I/O components continue to receive auxiliary power in order to power-up as the result of a Magic Packet™ being received over a network. Some NICs are able to wake up a system from Standby in PM, most require their Windows/NT driver to reset them after one wake-up.

8.6.1.5 Waking Up in Independent PM

Activity of either of the following devices will cause the system to wake up with the screen restored:

- Keyboard
- Mouse (if driver installed)

The hard drive will not spin up until it is accessed. Any hard drive access will cause it to wake up and resume spinning. Since the BIOS returns to the currently running software, it is possible for the drive to spin up while the system is in Standby with the screen blanked.

8.6.2 ACPI SUPPORT

These systems meet the hardware and firmware requirements for being ACPI compliant. This system supports the following ACPI functions:

- PM timer
- Power button
- Power button override
- RTC alarm
- Sleep/Wake logic (S1,S3, S4 (Windows 2000), S5)
- C1 state (Halt)
- PCI Power Management Event (PME)

8.7 USB LEGACY SUPPORT

The BIOS ROM checks the USB port, during POST, for the presence of a USB keyboard. This allows a system with only a USB keyboard to be used during ROM-based setup and also on a system with an OS that does not include a USB driver.

On such a system a keystroke will generate an SMI and the SMI handler will retrieve the data from the device and convert it to PS/2 data. The data will be passed to the keyboard controller and processed as in the PS/2 interface. Changing the delay and/or typematic rate of a USB keyboard though BIOS function INT 16 is not supported.

Appendix A
ERROR MESSAGES AND CODES

A.1 INTRODUCTION

This appendix lists the error codes and a brief description of the probable cause of the error.

NOTE: Errors listed in this appendix are applicable **only** for systems running hp/Compaq BIOS.

NOTE: Not all errors listed in this appendix may be applicable to a particular system model and/or configuration.

A.2 BEEP/KEYBOARD LED CODES

NOTE: Beep and LED indictions listed in Table A-1 apply only to Compaq-branded models. Refer to the Chapter 8 for beep/LED indications on HP-branded models.

Table A-1.
Beep/Keyboard LED Codes

Beeps	LED [1]	Probable Cause
1 short, 2 long	NUM lock blinking	Base memory failure.
1 long, 2 short	CAP lock blinking	Video/graphics controller failure.
2 long, 1 short	Scroll lock blinking	System failure (prior to video initialization).
1 long, 3 short	(None)	Boot block executing
None	All three blink in sequence	Keyboard locked in network mode.
None	NUM lock steady on	ROMPAQ diskette not present, bad, or drive not ready.
None	CAP lock steady on	Password prompt.
None	All three blink together	ROM flash failed.
None	All three steady on	Successful ROM flash.

NOTE:
[1] PS/2 keyboard only.

A.3 POWER-ON SELF TEST (POST) MESSAGES

Table A-2.
Power-On Self Test (POST) Messages

Error Message	Probable Cause
Invalid Electronic Serial Number	Chassis serial number is corrupt. Use Setup to enter a valid number.
Network Server Mode Active (w/o kybd)	System is in network mode.
101-Option ROM Checksum Error	A device's option ROM has failed/is bad.
102-system Board Failure	Failed ESCD write, A20, timer, or DMA controller.
150-Safe POST Active	An option ROM failed to execute on a previous boot.
162-System Options Not Set	Invalid checksum, RTC lost power, or invalid configuration.
163-Time & Date Not Set	Date and time information in CMOS is not valid.
164-Memory Size Error	Memory has been added or removed.
201-Memory Error	Memory test failed.
213-Incompatible Memory Module	BIOS detected installed DIMM(s) as being not compatible.
216-Memory Size Exceeds Max	Installed memory exceeds the maximum supported by the system.
217-DIMM Configuration Warning	Unbalanced memory configuration.
301-Keyboard Error	Keyboard interface test failed (improper connection or stuck key).
303-Keyboard Controller Error	Keyboard buffer failed empty (8042 failure or stuck key).
304-Keyboard/System Unit Error	Keyboard controller failed self-test.
404-Parallel Port Address Conflict	Current parallel port address is conflicting with another device.
417-Network Interface Card Failure	NIC BIOS could not read Device ID of embedded NIC.
510-Splash Image Corrupt	Corrupted splash screen image. Restore default image w/ROMPAQ.
511-CPU Fan Not Detected	Processor heat sink fan is not connected.
512-Chassis Fan Not Detected	Chassis fan is not connected.
601-Diskette Controller Error	Diskette drive removed since previous boot.
912-Computer Cover Removed Since Last System Start Up	Cover (hood) removal has been detected by the Smart Cover Sensor.
917-Expansion Riser Not Detected	Expansion (backplane) board not seated properly.
1156-Serial Port A Cable Not Detected	Cable from serial port header to I/O connector is missing or not connected properly.
1157-Front Cables Not Detected	Cable from front panel USB and audio connectors is missing or not connected properly.
1720-SMART Hard Drive Detects Imminent Failure	SMART circuitry on an IDE drive has detected possible equipment failure.
1721-SMART SCSI Hard Drive Detects Imminent Failure	SMART circuitry on a SCSI drive has detected possible equipment failure.
1801-Microcode Patch Error	A processor is installed for which the BIOS ROM has no patch. Check for ROM update.
1998-Master Boot Record Backup Has Been Lost	Backup copy of the hard drive master boot record is corrupted. Use Setup to restore the backup from the hard drive.
1999-Master Boot Record Has Changed. Press Any Key To Enter Setup to Restore the MBR.	If Master Boot Record Security is enabled, this message indicates that the MBR has changed since the backup was made.
2000-Master boot Record hard drive has changed	The hard drive has been changed. Use Setup to create a backup of the new hard drive.

A.4 SYSTEM ERROR MESSAGES (1xx-xx)

Table A-3.
System Error Messages

Message	Probable Cause	Message	Probable Cause
101	Option ROM error	110-01	Programmable timer load data test failed
102	System board failure (see note)	110-02	Programmable timer dynamic test failed
103	System board failure	110-03	Program timer 2 load data test failed
104-01	Master int. cntlr. test fialed	111-01	Refresh detect test failed
104-02	Slave int. cntlr. test failed	112-01	Speed test Slow mode out of range
104-03	Int. cntlr. SW RTC inoperative	112-02	Speed test Mixed mode out of range
105-01	Port 61 bit <6> not at zero	112-03	Speed test Fast mode out of range
105-02	Port 61 bit <5> not at zero	112-04	Speed test unable to enter Slow mode
105-03	Port 61 bit <3> not at zero	112-05	Speed test unable to enter Mixed mode
105-04	Port 61 bit <1> not at zero	112-06	Speed test unable to enter Fast mode
105-05	Port 61 bit <0> not at zero	112-07	Speed test system error
105-06	Port 61 bit <5> not at one	112-08	Unable to enter Auto mode in speed test
105-07	Port 61 bit <3> not at one	112-09	Unable to enter High mode in speed test
105-08	Port 61 bit <1> not at one	112-10	Speed test High mode out of range
105-09	Port 61 bit <0> not at one	112-11	Speed test Auto mode out of range
105-10	Port 61 I/O test failed	112-12	Speed test variable speed mode inop.
105-11	Port 61 bit <7> not at zero	113-01	Protected mode test failed
105-12	Port 61 bit <2> not at zero	114-01	Speaker test failed
105-13	No int. generated by failsafe timer	116-xx	Way 0 read/write test failed
105-14	NMI not triggered by failsafe timer	162-xx	Sys. options failed (mismatch in drive type)
106-01	Keyboard controller test failed	163-xx	Time and date not set
107-01	CMOS RAM test failed	164-xx	Memory size
108-02	CMOS interrupt test failed	199-00	Installed devices test failed
108-03	CMOS not properly initialized (int.test)		
109-01	CMOS clock load data test failed		
109-02	CMOS clock rollover test failed		
109-03	CMOS not properly initialized (clk test)		

NOTE: A 102 message code may be caused by one of a variety of processor-related problems that may be solved by replacing the processor, although system board replacement may be needed.

A.5 MEMORY ERROR MESSAGES (2xx-xx)

Table A-4.
Memory Error Messages

Message	Probable Cause
200-04	Real memory size changed
200-05	Extended memory size changed
200-06	Invalid memory configuration
200-07	Extended memory size changed
200-08	CLIM memory size changed
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
202-02	Failed RAM/ROM map test
202-03	Failed RAM/ROM protect test
203-01	Memory read/write test failed
203-02	Error while saving block in read/write test
203-03	Error while restoring block in read/write test
204-01	Memory address test failed
204-02	Error while saving block in address test
204-03	Error while restoring block in address test
204-04	A20 address test failed
204-05	Page hit address test failed
205-01	Walking I/O test failed
205-02	Error while saving block in walking I/O test
205-03	Error while restoring block in walking I/O test
206-xx	Increment pattern test failed
207-xx	ECC failure
210-01	Memory increment pattern test
210-02	Error while saving memory during increment pattern test
210-03	Error while restoring memory during increment pattern test
211-01	Memory random pattern test
211-02	Error while saving memory during random memory pattern test
211-03	Error while restoring memory during random memory pattern test
213-xx	Incompatible DIMM in slot x
214-xx	Noise test failed
215-xx	Random address test

A.6 KEYBOARD ERROR MESSAGES (30x-xx)

Table A-5.
Keyboard Error Messages

Message	Probable Cause	Message	Probable Cause
300-xx	Failed ID test	303-05	LED test, LED command test failed
301-01	Kybd short test, 8042 self-test failed	303-06	LED test, LED command test failed
301-02	Kybd short test, interface test failed	303-07	LED test, LED command test failed
301-03	Kybd short test, echo test failed	303-08	LED test, command byte restore test failed
301-04	Kybd short test, kybd reset failed	303-09	LED test, LEDs failed to light
301-05	Kybd short test, kybd reset failed	304-01	Keyboard repeat key test failed
302-xx	Failed individual key test	304-02	Unable to enter mode 3
302-01	Kybd long test failed	304-03	Incorrect scan code from keyboard
303-01	LED test, 8042 self-test failed	304-04	No Make code observed
303-02	LED test, reset test failed	304-05	Cannot /disable repeat key feature
303-03	LED test, reset failed	304-06	Unable to return to Normal mode
303-04	LED test, LED command test failed	--	--

A.7 PRINTER ERROR MESSAGES (4xx-xx)

Table A-6.
Printer Error Messages

Message	Probable Cause	Message	Probable Cause
401-01	Printer failed or not connected	402-11	Interrupt test, data/cntrl. reg. failed
402-01	Printer data register failed	402-12	Interrupt test and loopback test failed
402-02	Printer control register failed	402-13	Int. test, LpBk. test., and data register failed
402-03	Data and control registers failed	402-14	Int. test, LpBk. test., and cntrl. register failed
402-04	Loopback test failed	402-15	Int. test, LpBk. test., and data/cntrl. reg. failed
402-05	Loopback test and data reg. failed	402-16	Unexpected interrupt received
402-06	Loopback test and cntrl. reg. failed	402-01	Printer pattern test failed
402-07	Loopback tst, data/cntrl. reg. failed	403-xx	Printer pattern test failed
402-08	Interrupt test failed	404-xx	Parallel port address conflict
402-09	Interrupt test and data reg. failed	498-00	Printer failed or not connected
402-10	Interrupt test and control reg. failed	--	--

A.8 VIDEO (GRAPHICS) ERROR MESSAGES (5xx-xx)

Table A-7.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
501-01	Video controller test failed	508-01	320x200 mode, color set 0 test failed
502-01	Video memory test failed	509-01	320x200 mode, color set 1 test failed
503-01	Video attribute test failed	510-01	640x200 mode test failed
504-01	Video character set test failed	511-01	Screen memory page test failed
505-01	80x25 mode, 9x14 cell test failed	512-01	Gray scale test failed
506-01	80x25 mode, 8x8 cell test failed	514-01	White screen test failed
507-01	40x25 mode test failed	516-01	Noise pattern test failed

See Table A-14 for additional video (graphics) messages.

A.9 DISKETTE DRIVE ERROR MESSAGES (6xx-xx)

Table A-8.
Diskette Drive Error Messages

Message	Probable Cause	Message	Probable Cause
6xx-01	Exceeded maximum soft error limit	6xx-20	Failed to get drive type
6xx-02	Exceeded maximum hard error limit	6xx-21	Failed to get change line status
6xx-03	Previously exceeded max soft limit	6xx-22	Failed to clear change line status
6xx-04	Previously exceeded max hard limit	6xx-23	Failed to set drive type in ID media
6xx-05	Failed to reset controller	6xx-24	Failed to read diskette media
6xx-06	Fatal error while reading	6xx-25	Failed to verify diskette media
6xx-07	Fatal error while writing	6xx-26	Failed to read media in speed test
6xx-08	Failed compare of R/W buffers	6xx-27	Failed speed limits
6xx-09	Failed to format a tract	6xx-28	Failed write-protect test
6xx-10	Failed sector wrap test	--	--

600-xx = Diskette drive ID test
601-xx = Diskette drive format
602-xx = Diskette read test
603-xx = Diskette drive R/W compare test
604-xx = Diskette drive random seek test
605-xx = Diskette drive ID media
606-xx = Diskette drive speed test
607-xx = Diskette drive wrap test
608-xx = Diskette drive write-protect test
609-xx = Diskette drive reset controller test
610-xx = Diskette drive change line test
611-xx = Pri. diskette drive port addr. conflict
612-xx = Sec. diskette drive port addr. conflict
694-00 = Pin 34 not cut on 360-KB drive
697-00 = Diskette type error
698-00 = Drive speed not within limits
699-00 = Drive/media ID error (run Setup)

A.10 SERIAL INTERFACE ERROR MESSAGES (11xx-xx)

Table A-9.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1101-01	UART DLAB bit failure	1101-13	UART cntrl. signal interrupt failure
1101-02	Line input or UART fault	1101-14	DRVR/RCVR data failure
1101-03	Address line fault	1109-01	Clock register initialization failure
1101-04	Data line fault	1109-02	Clock register rollover failure
1101-05	UART cntrl. signal failure	1109-03	Clock reset failure
1101-06	UART THRE bit failure	1109-04	Input line or clock failure
1101-07	UART Data RDY bit failure	1109-05	Address line fault
1101-08	UART TX/RX buffer failure	1109-06	Data line fault
1101-09	Interrupt circuit failure	1150-xx	Comm port setup error (run Setup)
1101-10	COM1 set to invalid INT	1151-xx	COM1 address conflict
1101-11	COM2 set to invalid INT	1152-xx	COM2 address conflict
1101-12	DRVR/RCVR cntrl. signal failure	1155-xx	COM port address conflict

A.11 MODEM COMMUNICATIONS ERROR MESSAGES (12xx-xx)

Table A-10.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1201-XX	Modem internal loopback test	1204-03	Data block retry limit reached [4]
1201-01	UART DLAB bit failure	1204-04	RX exceeded carrier lost limit
1201-02	Line input or UART failure	1204-05	TX exceeded carrier lost limit
1201-03	Address line failure	1204-06	Time-out waiting for dial tone
1201-04	Data line fault	1204-07	Dial number string too long
1201-05	UART control signal failure	1204-08	Modem time-out waiting for remote response
1201-06	UART THRE bit failure	1204-09	Modem exceeded maximum redial limit
1201-07	UART DATA READY bit failure	1204-10	Line quality prevented remote response
1201-08	UART TX/RX buffer failure	1204-11	Modem time-out waiting for remote connection
1201-09	Interrupt circuit failure	1205-XX	Modem auto answer test
1201-10	COM1 set to invalid inturrupt	1205-01	Time-out waiting for SYNC [5]
1201-11	COM2 set to invalid	1205-02	Time-out waiting for response [5]
1201-12	DRVR/RCVR control signal failure	1205-03	Data block retry limit reached [5]
1201-13	UART control signal interrupt failure	1205-04	RX exceeded carrier lost limit
1201-14	DRVR/RCVR data failure	1205-05	TX exceeded carrier lost limit
1201-15	Modem detection failure	1205-06	Time-out waiting for dial tone
1201-16	Modem ROM, checksum failure	1205-07	Dial number string too long
1201-17	Tone detect failure	1205-08	Modem time-out waiting for remote response
1202-XX	Modem internal test	1205-09	Modem exceeded maximum redial limit
1202-01	Time-out waiting for SYNC [1]	1205-10	Line quality prevented remote response
1202-02	Time-out waiting for response [1]	1205-11	Modem time-out waiting for remote connection
1202-03	Data block retry limit reached [1]	1206-XX	Dial multi-frequency tone test
1202-11	Time-out waiting for SYNC [2]	1206-17	Tone detection failure
1202-12	Time-out waiting for response [2]	1210-XX	Modem direct connect test
1202-13	Data block retry limit reached [2]	1210-01	Time-out waiting for SYNC [6]
1202-21	Time-out waiting for SYNC [3]	1210-02	Time-out waiting for response [6]
1202-22	Time-out waiting for response [3]	1210-03	Data block retry limit reached [6]
1202-23	Data block retry limit reached [3]	1210-04	RX exceeded carrier lost limit
1203-XX	Modem external termination test	1210-05	TX exceeded carrier lost limit
1203-01	Modem external TIP/RING failure	1210-06	Time-out waiting for dial tone
1203-02	Modem external data TIP/RING fail	1210-07	Dial number string too long
1203-03	Modem line termination failure	1210-08	Modem time-out waiting for remote response
1204-XX	Modem auto originate test	1210-09	Modem exceeded maximum redial limit
1204-01	Time-out waiting for SYNC [4]	1210-10	Line quality prevented remote response
1204-02	Time-out waiting for response [4]	1210-11	Modem time-out waiting for remote connection

NOTES:

[1] Local loopback mode
[2] Analog loopback originate mode
[3] Analog loopback answer mode
[4] Modem auto originate test
[5] Modem auto answer test
[6] Modem direct connect test

A.12 SYSTEM STATUS ERROR MESSAGES (16xx-xx)

Table A-11.
System Status Error Messages

Message	Probable Cause
1601-xx	Temperature violation
1611-xx	Fan failure

A.13 HARD DRIVE ERROR MESSAGES (17xx-xx)

Table A-12.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
17xx-01	Exceeded max. soft error limit	17xx-51	Failed I/O read test
17xx-02	Exceeded max. Hard error limit	17xx-52	Failed file I/O compare test
17xx-03	Previously exceeded max. soft error limit	17xx-53	Failed drive/head register test
17xx-04	Previously exceeded max.hard error limit	17xx-54	Failed digital input register test
17xx-05	Failed to reset controller	17xx-55	Cylinder 1 error
17xx-06	Fatal error while reading	17xx-56	Failed controller RAM diagnostics
17xx-07	Fatal error while writing	17xx-57	Failed controller-to-drive diagnostics
17xx-08	Failed compare of R/W buffers	17xx-58	Failed to write sector buffer
17xx-09	Failed to format a track	17xx-59	Failed to read sector buffer
17xx-10	Failed diskette sector wrap during read	17xx-60	Failed uncorrectable ECC error
17xx-19	Cntlr. failed to deallocate bad sectors	17xx-62	Failed correctable ECC error
17xx-40	Cylinder 0 error	17xx-63	Failed soft error rate
17xx-41	Drive not ready	17xx-65	Exceeded max. bad sectors per track
17xx-42	Failed to recalibrate drive	17xx-66	Failed to initialize drive parameter
17xx-43	Failed to format a bad track	17xx-67	Failed to write long
17xx-44	Failed controller diagnostics	17xx-68	Failed to read long
17xx-45	Failed to get drive parameters from ROM	17xx-69	Failed to read drive size
17xx-46	Invalid drive parameters from ROM	17xx-70	Failed translate mode
17xx-47	Failed to park heads	17xx-71	Failed non-translate mode
17xx-48	Failed to move hard drive table to RAM	17xx-72	Bad track limit exceeded
17xx-49	Failed to read media in file write test	17xx-73	Previously exceeded bad track limit
17xx-50	Failed I/O write test	--	--

NOTE:

xx = 00, Hard drive ID test
xx = 01, Hard drive format test
xx = 02, Hard drive read test
xx = 03, Hard drive read/write compare test
xx = 04, Hard drive random seek test
xx = 05, Hard drive controller test
xx = 06, Hard drive ready test
xx = 07, Hard drive recalibrate test
xx = 08, Hard drive format bad track test
xx = 09, Hard drive reset controller test
xx = 10, Hard drive park head test
xx = 14, Hard drive file write test
xx = 15, Hard drive head select test
xx = 16, Hard drive conditional format test
xx = 17, Hard drive ECC test
xx = 19, Hard drive power mode test
xx = 20, SMART drive detects imminent failure
xx = 21, SCSI hard drive imminent failure
xx = 24, Net work preparation test
xx = 36, Drive monitoring test
xx = 71, Pri. IDE controller address conflict
xx = 72, Sec. IDE controller address conflict
xx = 80, Disk 0 failure
xx = 81, Disk 1 failure
xx = 82, Pri. IDE controller failure
xx = 90, Disk 0 failure
xx = 91, Disk 1 failure
xx = 92, Se. controller failure
xx = 93, Sec. Controller or disk failure
xx = 99, Invalid hard drive type

A.14 HARD DRIVE ERROR MESSAGES (19xx-xx)

Table A-13.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
19xx-01	Drive not installed	19xx-21	Got servo pulses second time but not first
19xx-02	Cartridge not installed	19xx-22	Never got to EOT after servo check
19xx-03	Tape motion error	19xx-23	Change line unset
19xx-04	Drive busy erro	19xx-24	Write-protect error
19xx-05	Track seek error	19xx-25	Unable to erase cartridge
19xx-06	Tape write-protect error	19xx-26	Cannot identify drive
19xx-07	Tape already Servo Written	19xx-27	Drive not compatible with controller
19xx-08	Unable to Servo Write	19xx-28	Format gap error
19xx-09	Unable to format	19xx-30	Exception bit not set
19xx-10	Format mode error	19xx-31	Unexpected drive status
19xx-11	Drive recalibration error	19xx-32	Device fault
19xx-12	Tape not Servo Written	19xx-33	Illegal command
19xx-13	Tape not formatted	19xx-34	No data detected
19xx-14	Drive time-out error	19xx-35	Power-on reset occurred
19xx-15	Sensor error flag	19xx-36	Failed to set FLEX format mode
19xx-16	Block locate (block ID) error	19xx-37	Failed to reset FLEX format mode
19xx-17	Soft error limit exceeded	19xx-38	Data mismatch on directory track
19xx-18	Hard error limit exceeded	19xx-39	Data mismatch on track 0
19xx-19	Write (probably ID) error	19xx-40	Failed self-test
19xx-20	NEC fatal error	19xx-91	Power lost during test

1900-xx = Tape ID test failed
1901-xx = Tape servo write failed
1902-xx = Tape format failed
1903-xx = Tape drive sensor test failed
1904-xx = Tape BOT/EOT test failed
1905-xx = Tape read test failed
1906-xx = Tape R/W compare test failed
1907-xx = Tape write-protect failed

A.15 VIDEO (GRAPHICS) ERROR MESSAGES (24xx-xx)

Table A-14.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
2402-01	Video memory test failed	2418-02	EGA shadow RAM test failed
2403-01	Video attribute test failed	2419-01	EGA ROM checksum test failed
2404-01	Video character set test failed	2420-01	EGA attribute test failed
2405-01	80x25 mode, 9x14 cell test failed	2421-01	640x200 mode test failed
2406-01	80x25 mode, 8x8 cell test failed	2422-01	640x350 16-color set test failed
2407-01	40x25 mode test failed	2423-01	640x350 64-color set test failed
2408-01	320x200 mode color set 0 test failed	2424-01	EGA Mono. text mode test failed
2409-01	320x200 mode color set 1 test failed	2425-01	EGA Mono. graphics mode test failed
2410-01	640x200 mode test failed	2431-01	640x480 graphics mode test failed
2411-01	Screen memory page test failed	2432-01	320x200 256-color set test failed
2412-01	Gray scale test failed	2448-01	Advanced VGA controller test failed
2414-01	White screen test failed	2451-01	132-column AVGA test failed
2416-01	Noise pattern test failed	2456-01	AVGA 256-color test failed
2417-01	Lightpen text test failed, no response	2458-xx	AVGA BitBLT test failed
2417-02	Lightpen text test failed, invalid response	2468-xx	AVGA DAC test failed
2417-03	Lightpen graphics test failed, no resp.	2477-xx	AVGA data path test failed
2417-04	Lightpen graphics tst failed, invalid resp.	2478-xx	AVGA BitBLT test failed
2418-01	EGA memory test failed	2480-xx	AVGA linedraw test failed

A.16 AUDIO ERROR MESSAGES (3206-xx)

Table A-15.
Audio Error Message

Message	Probable Cause
3206-xx	Audio subsystem internal error

A.17 DVD/CD-ROM ERROR MESSAGES (33xx-xx)

Table A-16.
DVD/CD-ROM Drive Error Messages

Message	Probable Cause
3301-xx	Drive test failed
3305-xx	Seek test failed

See Table A-18 for additional messages.

A.18 NETWORK INTERFACE ERROR MESSAGES (60xx-xx)

Table A-17.
Network Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6000-xx	Pointing device interface error	6054-xx	Token ring configuration test failed
6014-xx	Ethernet configuration test failed	6056-xx	Token ring reset test failed
6016-xx	Ethernet reset test failed	6068-xx	Token ring int. loopback test failed
6028-xx	Ethernet int. loopback test failed	6069-xx	Token ring ext. loopback test failed
6029-xx	Ethernet ext. loopback test failed	6089-xx	Token ring open

A.19 SCSI INTERFACE ERROR MESSAGES (65xx-xx, 66xx-xx, 67xx-xx)

Table A-18.
SCSI Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6nyy-02	Drive not installed	6nyy-33	Illegal controller command
6nyy-03	Media not installed	6nyy-34	Invalid SCSI bus phase
6nyy-05	Seek failure	6nyy-35	Invalid SCSI bus phase
6nyy-06	Drive timed out	6nyy-36	Invalid SCSI bus phase
6nyy-07	Drive busy	6nyy-39	Error status from drive
6nyy-08	Drive already reserved	6nyy-40	Drive timed out
6nyy-09	Reserved	6nyy-41	SSI bus stayed busy
6nyy-10	Reserved	6nyy-42	ACK/REQ lines bad
6nyy-11	Media soft error	6nyy-43	ACK did not deassert
6nyy-12	Drive not ready	6nyy-44	Parity error
6nyy-13	Media error	6nyy-50	Data pins bad
6nyy-14	Drive hardware error	6nyy-51	Data line 7 bad
6nyy-15	Illegal drive command	6nyy-52	MSG, C/D, or I/O lines bad
6nyy-16	Media was changed	6nyy-53	BSY never went busy
6nyy-17	Tape write-protected	6nyy-54	BSY stayed busy
6nyy-18	No data detected	6nyy-60	Controller CONFIG-1 register fault
6nyy-21	Drive command aborted	6nyy-61	Controller CONFIG-2 register fault
6nyy-24	Media hard error	6nyy-65	Media not unloaded
6nyy-25	Reserved	6nyy-90	Fan failure
6nyy-30	Controller timed out	6nyy-91	Over temperature condition
6nyy-31	Unrecoverable error	6nyy-92	Side panel not installed
6nyy-32	Controller/drive not connected	6nyy-99	Autoloader reported tape not loaded properly

n = 5, Hard drive
= 6, CD-ROM drive
= 7, Tape drive.

yy = 00, ID
= 03, Power check
= 05, Read
= 06, SA/Media
= 08, Controller
= 23, Random read
= 28, Media load/unload

A.20 POINTING DEVICE INTERFACE ERROR MESSAGES (8601-xx)

Table A-19.
Pointing Device Interface Error Messages

Message	Probable Cause	Message	Probable Cause
8601-01	Mouse ID fails	8601-07	Right block not selected
8601-02	Left mouse button is inoperative	8601-08	Timeout occurred
8601-03	Left mouse button is stuck closed	8601-09	Mouse loopback test failed
8601-04	Right mouse button is inoperative	8601-10	Pointing device is inoperative
8601-05	Right mouse button is stuck closed	8602-xx	I/F test failed
8601-06	Left block not selected	--	--

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Appendix B
ASCII CHARACTER SET

B.1 INTRODUCTION

This appendix lists, in Table B-1, the 256-character ASCII code set including the decimal and hexadecimal values. All ASCII symbols may be called while in DOS or using standard text-mode editors by using the combination keystroke of holding the **Alt** key and using the Numeric Keypad to enter the decimal value of the symbol. The extended ASCII characters (decimals 128-255) can only be called using the **Alt** + Numeric Keypad keys.

NOTE: Regarding keystrokes, refer to notes at the end of the table. Applications may interpret multiple keystroke accesses differently or ignore them completely.

Table B-1.
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
0	00	Blank	32	20	Space	64	40	@	96	60	‘
1	01	☺	33	21	!	65	41	A	97	61	a
2	02	☻	34	22	“	66	42	B	98	62	b
3	03	♥	35	23	#	67	43	C	99	63	c
4	04	♦	36	24	$	68	44	D	100	64	d
5	05	♣	37	25	%	69	45	E	101	65	e
6	06	♠	38	26	&	70	46	F	102	66	f
7	07	•	39	27	‘	71	47	G	103	67	g
8	08	◘	40	28	(	72	48	H	104	68	h
9	09	○	41	29	)	73	49	I	105	69	I
10	0A	◙	42	2A	*	74	4A	J	106	6A	j
11	0B	♂	43	2B	+	75	4B	K	107	6B	k
12	0C	♀	44	2C	`	76	4C	L	108	6C	l
13	0D	♪	45	2D	-	77	4D	M	109	6D	m
14	0E	♫	46	2E	.	78	4E	N	110	6E	n
15	0F	☼	47	2F	/	79	4F	O	111	6F	o
16	10	►	48	30	0	80	50	P	112	70	p
17	11	◄	49	31	1	81	51	Q	113	71	q
18	12	↕	50	32	2	82	52	R	114	72	r
19	13	‼	51	33	3	83	53	S	115	73	s
20	14	¶	52	34	4	84	54	T	116	74	t
21	15	§	53	35	5	85	55	U	117	75	u
22	16	▬	54	36	6	86	56	V	118	76	v
23	17	↨	55	37	7	87	57	W	119	77	w
24	18	↑	56	38	8	88	58	X	120	78	x
25	19	↓	57	39	9	89	59	Y	121	79	y
26	1A	→	58	3A	:	90	5A	Z	122	7A	z
27	1B	←	59	3B	;	91	5B	[	123	7B	{
28	1C	∟	60	3C	<	92	5C	\	124	7C	|
29	1D	↔	61	3D	=	93	5D	]	125	7D	}
30	1E	▲	62	3E	>	94	5E	^	126	7E	~
31	1F	▼	63	3F	?	95	5F	_	127	7F	△ [1]

Continued

Table B-1. ASCII Code Set *(Continued)*

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
128	80	Ç	160	A0	á	192	C0	└	224	E0	α
129	81	ü	161	A1	í	193	C1	┴	225	E1	ß
130	82	é	162	A2	ó	194	C2	┬	226	E2	Γ
131	83	â	163	A3	ú	195	C3	├	227	E3	π
132	84	ä	164	A4	ñ	196	C4	─	228	E4	Σ
133	85	à	165	A5	Ñ	197	C5	┼	229	E5	σ
134	86	å	166	A6	ª	198	C6	╞	230	E6	µ
135	87	ç	167	A7	º	199	C7	╟	231	E7	τ
136	88	ê	168	A8	¿	200	C8	╚	232	E8	Φ
137	89	ë	169	A9	⌐	201	C9	╔	233	E9	Θ
138	8A	è	170	AA	¬	202	CA	╩	234	EA	Ω
139	8B	ï	171	AB	½	203	CB	╦	235	EB	δ
140	8C	î	172	AC	¼	204	CC	╠	236	EC	∞
141	8D	ì	173	AD	¡	205	CD	═	237	ED	φ
142	8E	Ä	174	AE	«	206	CE	╬	238	EE	ε
143	8F	Å	175	AF	»	207	CF	╧	239	EF	∩
144	90	É	176	B0	░	208	D0	╨	240	F0	≡
145	91	æ	177	B1	▒	209	D1	╤	241	F1	±
146	92	Æ	178	B2	▓	210	D2	╥	242	F2	≥
147	93	ô	179	B3	│	211	D3	╙	243	F3	≤
148	94	ö	180	B4	┤	212	D4	╘	244	F4	⌠
149	95	ò	181	B5	╡	213	D5	╒	245	F5	⌡
150	96	û	182	B6	╢	214	D6	╓	246	F6	÷
151	97	ù	183	B7	╖	215	D7	╫	247	F7	≈
152	98	ÿ	184	B8	╕	216	D8	╪	248	F8	°
153	99	Ö	185	B9	╣	217	D9	┘	249	F9	∙
154	9A	Ü	186	BA	║	218	DA	┌	250	FA	·
155	9B	¢	187	BB	╗	219	DB	█	251	FB	√
156	9C	£	188	BC	╝	220	DC	▄	252	FC	ⁿ
157	9D	¥	189	BD	╜	221	DD	▌	253	FD	²
158	9E	₧	190	BE	╛	222	DE	▐	254	FE	■
159	9F	ƒ	191	BF	┐	223	DF	▀	255	FF	Blank

NOTES:

[1] Symbol not displayed.

Keystroke Guide:

Dec #	Keystroke(s)
0	Ctrl 2
1-26	Ctrl A thru Z respectively
27	Ctrl [
28	Ctrl
29	Ctrl]
30	Ctrl 6
31	Ctrl -
32	Space Bar
33-43	Shift and key w/corresponding symbol
44-47	Key w/corresponding symbol
48-57	Key w/corresponding symbol, numerical keypad w/Num Lock active
58	Shift and key w/corresponding symbol
59	Key w/corresponding symbol
60	Shift and key w/corresponding symbol
61	Key w/corresponding symbol
62-64	Shift and key w/corresponding symbol
65-90	Shift and key w/corresponding symbol or key w/corresponding symbol and Caps Lock active
91-93	Key w/corresponding symbol
94, 95	Shift and key w/corresponding symbol
96	Key w/corresponding symbol
97-126	Key w/corresponding symbol or Shift and key w/corresponding symbol and Caps Lock active
127	Ctrl -
128-255	Alt and decimal digit(s) of desired character

Appendix C
KEYBOARD

C.1 INTRODUCTION

This appendix describes the HP/Compaq keyboard that is included as standard with the system unit. The keyboard complies with the industry-standard classification of an "enhanced keyboard" and includes a separate cursor control key cluster, twelve "function" keys, and enhanced programmability for additional functions.
This appendix covers the following keyboard types:

- Standard enhanced keyboard.
- Space-Saver Windows-version keyboard featuring additional keys for specific support of the Windows operating system.
- Easy Access keyboard with additional buttons for internet accessibility functions.

Only one type of keyboard is supplied with each system. Other types may be available as an option.

> **NOTE:** This appendix discusses only the keyboard unit. The keyboard interface is a function of the system unit and is discussed in Chapter 5, Input/Output Interfaces.

Topics covered in this appendix include the following:

C.2 KEYSTROKE PROCESSING

A functional block diagram of the keystroke processing elements is shown in Figure C-1. Power (+5 VDC) is obtained from the system through the PS/2-type interface. The keyboard uses a Z86C14 (or equivalent) microprocessor. The Z86C14 scans the key matrix drivers every 10 ms for pressed keys while at the same time monitoring communications with the keyboard interface of the system unit. When a key is pressed, a Make code is generated. A Break code is generated when the key is released. The Make and Break codes are collectively referred to as scan codes. All keys generate Make and Break codes with the exception of the Pause key, which generates a Make code only.

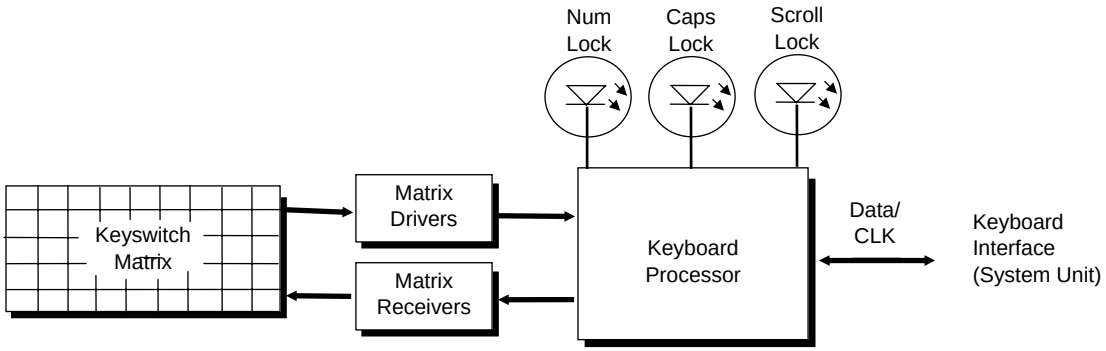


Figure C–1. Keystroke Processing Elements, Block Diagram

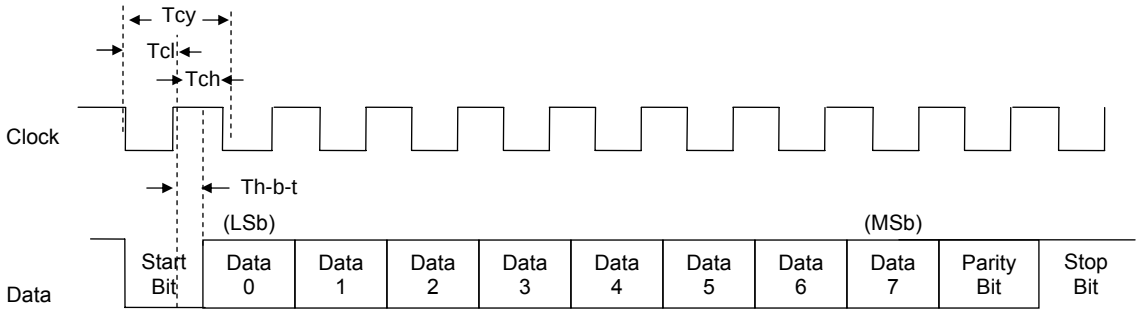
When the system is turned on, the keyboard processor generates a Power-On Reset (POR) signal after a period of 150 ms to 2 seconds. The keyboard undergoes a Basic Assurance Test (BAT) that checks for shorted keys and basic operation of the keyboard processor. The BAT takes from 300 to 500 ms to complete.

If the keyboard fails the BAT, an error code is sent to the CPU and the keyboard is disabled until an input command is received. After successful completion of the POR and BAT, a completion code (AAh) is sent to the CPU and the scanning process begins.

The keyboard processor includes a 16-byte FIFO buffer for holding scan codes until the system is ready to receive them. Response and typematic codes are not buffered. If the buffer is full (16 bytes held) a 17th byte of a successive scan code results in an overrun condition and the overrun code replaces the scan code byte and any additional scan code data (and the respective key strokes) are lost. Multi-byte sequences must fit entirely into the buffer before the respective keystroke can be registered.

C.2.1 PS/2-TYPE KEYBOARD TRANSMISSIONS

The PS/2-type keyboard sends two main types of data to the system; commands (or responses to system commands) and keystroke scan codes. Before the keyboard sends data to the system (specifically, to the 8042-type logic within the system), the keyboard verifies the clock and data lines to the system. If the clock signal is low (0), the keyboard recognizes the inhibited state and loads the data into a buffer. Once the inhibited state is removed, the data is sent to the system. Keyboard-to-system transfers (in the default mode) consist of 11 bits as shown in Figure C-2.



Parameter	Minimum	Nominal	Maximum
Tcy (clock cycle)	60 us	--	80 us
Tcl (clock low)	30 us	41 us	50 us
Tch (clock high)	30 us	--	40 us
Th-b-t (high-before-transmit)	--	20 us	--

Figure C–2. PS/2 Keyboard-To-System Transmission, Timing Diagram

The system can halt keyboard transmission by setting the clock signal low. The keyboard checks the clock line every 60 µs to verify the state of the signal. If a low is detected, the keyboard will finish the current transmission **if** the rising edge of the clock pulse for the parity bit has not occurred. The system uses the same timing relationships during reads (typically with slightly reduced time periods).

The enhanced keyboard has three operating modes:

- Mode 1 - PC-XT compatible
- Mode 2 - PC-AT compatible (default)
- Mode 3 - Select mode (keys are programmable as to make-only, break-only, typematic)

Modes can be selected by the user or set by the system. Mode 2 is the default mode. Each mode produces a different set of scan codes. When a key is pressed, the keyboard processor sends that key's make code to the 8042 logic of the system unit. The When the key is released, a release code is transmitted as well (except for the Pause key, which produces only a make code). The 8042-type logic of the system unit responds to scan code reception by asserting IRQ1, which is processed by the interrupt logic and serviced by the CPU with an interrupt service routine. The service routine takes the appropriate action based on which key was pressed.

C.2.2 USB-TYPE KEYBOARD TRANSMISSIONS

The USB-type keyboard sends essentially the same information to the system that the PS/2 keyboard does except that the data receives additional NRZI encoding and formatting (prior to leaving the keyboard) to comply with the USB I/F specification (discussed in chapter 5 of this guide).

Packets received at the system's USB I/F and decoded as originating from the keyboard result in an SMI being generated. An SMI handler routine is invoked that decodes the data and transfers the information to the 8042 keyboard controller where normal (legacy) keyboard processing takes place.

C.2.3 KEYBOARD LAYOUTS

Figures C-3 through C-8 show the key layouts for keyboards shipped with Compaq systems. Actual styling details including location of the Compaq logo as well as the numbers lock, caps lock, and scroll lock LEDs may vary.

C.2.3.1 Standard Enhanced Keyboards

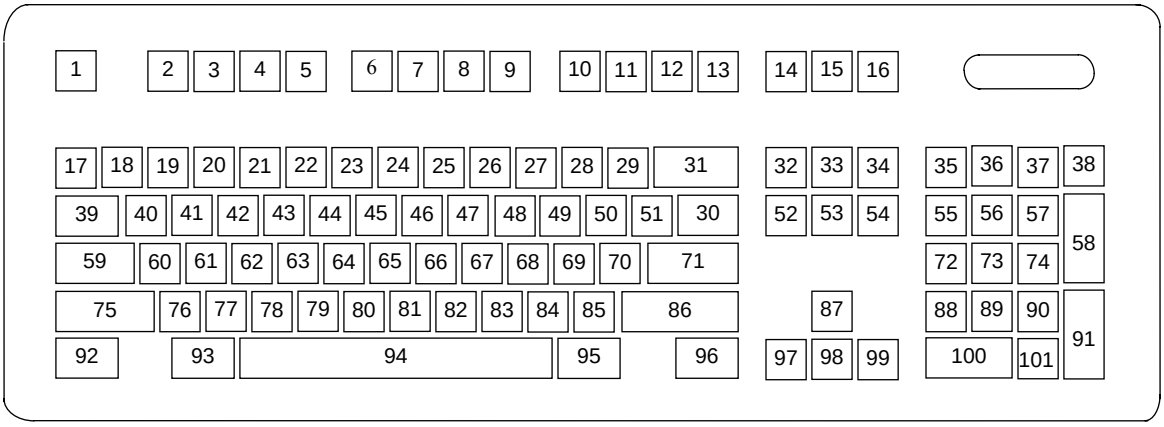


Figure C–3. U.S. English (101-Key) Keyboard Key Positions

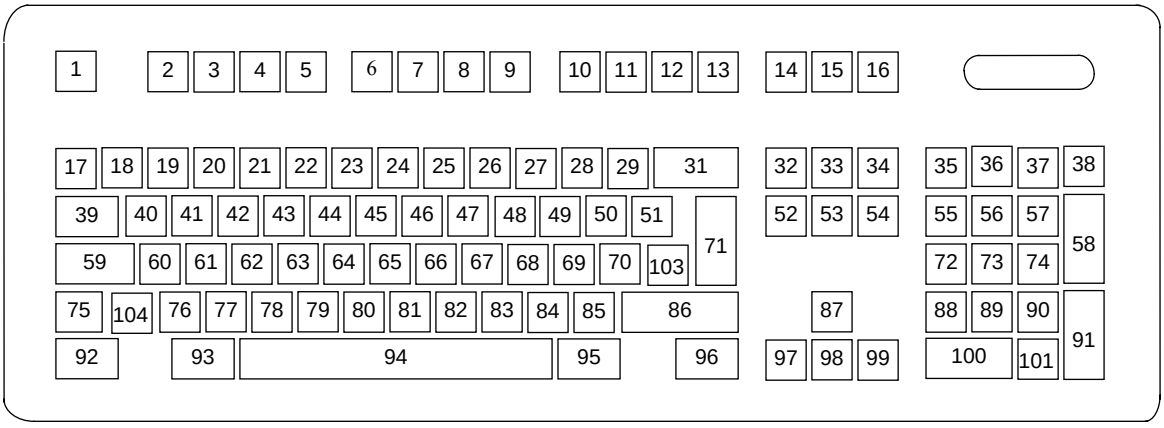


Figure C–4. National (102-Key) Keyboard Key Positions

C.2.3.2 Windows Enhanced Keyboards

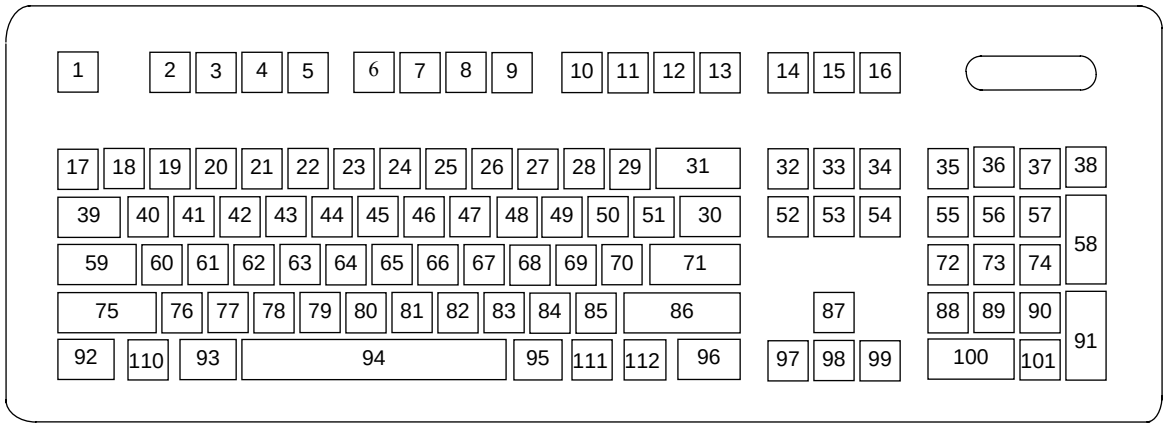


Figure C–5. U.S. English Windows (101W-Key) Keyboard Key Positions

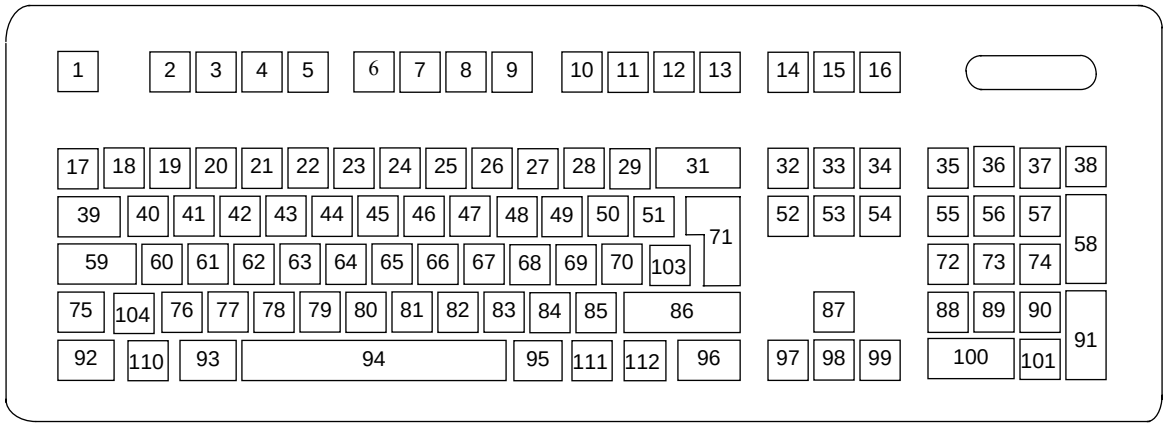
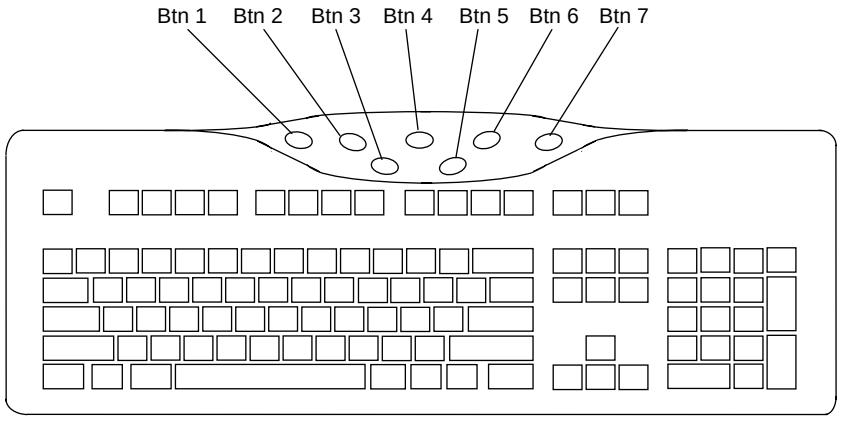


Figure C–6. National Windows (102W-Key) Keyboard Key Positions

C.2.3.3 Easy Access Keyboards

The Easy Access keyboard is a Windows Enhanced-type keyboard that includes special buttons allowing quick internet navigation. Depending on system, either a 7-button or an 8-button layout may be supplied.

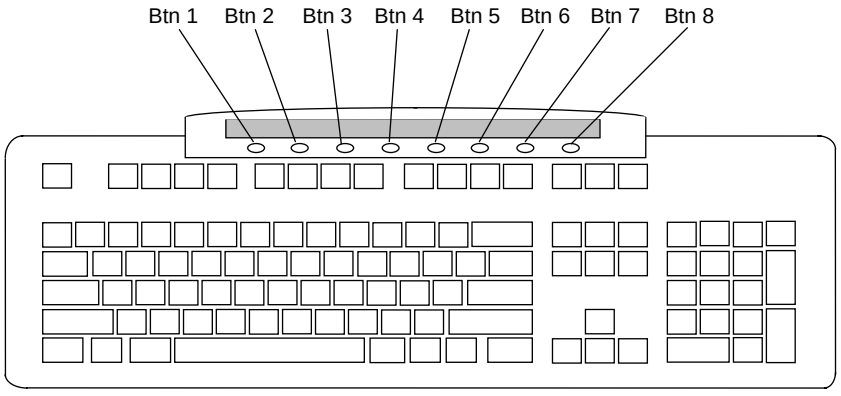
The 7-button Easy Access Keyboard uses the layout shown in Figure C-7 and is available with either a legacy PS/2-type connection or a Universal Serial Bus (USB) type connection.



NOTE:
Main key positions same as Windows Enhanced (Figures C-5 or C-6).

Figure C–7. 7-Button Easy Access Keyboard Layout

The 8-button Easy Access Keyboard uses the layout shown in Figure C-8 and uses the PS/2-type connection.



NOTE:
Main key positions same as Windows Enhanced (Figures C-5 or C-6).

Figure C–8. 8-Button Easy Access Keyboard Layout

C.2.4 KEYS

All keys generate a Make code (when pressed) and a Break code (when released) with the exception of the **Pause** key (pos. 16), which produces a Make code only. All keys with the exception of the **Pause** and Easy Access keys are also typematic, although the typematic action of the **Shift**, **Ctrl**, **Alt**, **Num Lock**, **Scroll Lock**, **Caps Lock**, and **Ins** keys is suppressed by the BIOS. Typematic keys, when held down longer than 500 ms, send the Make code repetitively at a 10-12 Hz rate until the key is released. If more than one key is held down, the last key pressed will be typematic.

C.2.4.1 Special Single-Keystroke Functions

The following keys provide the intended function in most applications and environments.

Caps Lock - The **Caps Lock** key (pos. 59), when pressed and released, invokes a BIOS routine that turns on the caps lock LED and shifts into upper case key positions 40-49, 60-68, and 76-82. When pressed and released again, these keys revert to the lower case state and the LED is turned off. Use of the **Shift** key will reverse which state these keys are in based on the **Caps Lock** key.

Num Lock - The **Num Lock** key (pos. 32), when pressed and released, invokes a BIOS routine that turns on the num lock LED and shifts into upper case key positions 55-57, 72-74, 88-90, 100, and 101. When pressed and released again, these keys revert to the lower case state and the LED is turned off.

The following keys provide special functions that require specific support by the application.

Print Scrn - The **Print Scrn** (pos. 14) key can, when pressed, generate an interrupt that initiates a print routine. This function may be inhibited by the application.

Scroll Lock - The **Scroll Lock** key (pos. 15) when pressed and released, invokes a BIOS routine that turns on the scroll lock LED and inhibits movement of the cursor. When pressed and released again, the LED is turned off and the function is removed. This keystroke is always serviced by the BIOS (as indicated by the LED) but may be inhibited or ignored by the application.

Pause - The **Pause** (pos. 16) key, when pressed, can be used to cause the keyboard interrupt to loop, i.e., wait for another key to be pressed. This can be used to momentarily suspend an operation. The key that is pressed to resume operation is discarded. This function may be ignored by the application.

The **Esc**, **Fn** (function), **Insert**, **Home**, **Page Up**/**Down**, **Delete**, and **End** keys operate at the discretion of the application software.

C.2.4.2 Multi-Keystroke Functions

Shift - The **Shift** key (pos. 75/86), when held down, produces a shift state (upper case) for keys in positions 17-29, 30, 39-51, 60-70, and 76-85 as long as the **Caps Lock** key (pos. 59) is toggled off. If the **Caps Lock** key is toggled on, then a held **Shift** key produces the lower (normal) case for the identified pressed keys. The **Shift** key also reverses the **Num Lock** state of key positions 55-57, 72, 74, 88-90, 100, and 101.

Ctrl - The **Ctrl** keys (pos. 92/96) can be used in conjunction with keys in positions 1-13, 16, 17-34, 39-54, 60-71, and 76-84. The application determines the actual function. Both **Ctrl** key positions provide identical functionality. The pressed combination of **Ctrl** and **Break** (pos. 16) results in the generation of BIOS function INT 1Bh. This software interrupt provides a method of exiting an application and generally halts execution of the current program.

Alt - The **Alt** keys (pos. 93/95) can be used in conjunction with the same keys available for use with the **Ctrl** keys with the exception that position 14 (**SysRq**) is available instead of position 16 (**Break**). The **Alt** key can also be used in conjunction with the numeric keypad keys (pos. 55-57, 72-74, and 88-90) to enter the decimal value of an ASCII character code from 1-255. The application determines the actual function of the keystrokes. Both **Alt** key positions provide identical functionality. The combination keystroke of **Alt** and **SysRq** results in software interrupt 15h, AX=8500h being executed. It is up to the application to use or not use this BIOS function.

The **Ctrl** and **Alt** keys can be used together in conjunction with keys in positions 1-13, 17-34, 39-54, 60-71, and 76-84. The **Ctrl** and **Alt** key positions used and the sequence in which they are pressed make no difference as long as they are held down at the time the third key is pressed. The **Ctrl**, **Alt,** and **Delete** keystroke combination (required twice if in the Windows environment) initiates a system reset (warm boot) that is handled by the BIOS.

C.2.4.3 Windows Keystrokes

Windows-enhanced keyboards include three additional key positions. Key positions 110 and 111 (marked with the Windows logo) have the same functionality and are used by themselves or in combination with other keys to perform specific "hot-key" type functions for the Windows operating system. The defined functions of the Windows logo keys are listed as follows:

Keystroke	Function
Window Logo	Open Start menu
Window Logo + F1	Display pop-up menu for the selected object
Window Logo + TAB	Activate next task bar button
Window Logo + E	Explore my computer
Window Logo + F	Find document
Window Logo + CTRL + F	Find computer
Window Logo + M	Minimize all
Shift + Window Logo + M	Undo minimize all
Window Logo + R	Display Run dialog box
Window Logo + PAUSE	Perform system function
Window Logo + 0-9	Reserved for OEM use (see following text)

The combination keystroke of the Window Logo + 1-0 keys are reserved for OEM use for auxiliary functions (speaker volume, monitor brightness, password, etc.).

Key position 112 (marked with an application window icon) is used in combination with other keys for invoking Windows application functions.

C.2.4.4 Easy Access Keystrokes

The Easy Access keyboards (Figures C-7 and C-8) include additional keys (also referred to as buttons) used to streamline internet access and navigation.

These buttons, which can be re-programmed to provide other functions, have the default functionality described below:

7-Button Easy Access Keyboard:

Button #	Description	Default Function
1	Check email	Email
2	Go to community	Emoney
3	Extra web site	Compaq web site
4	Go to favorite web site	AltaVista web site
5	Internet search	Search
6	Instant answer	Travel expenses
7	E-commerce	Shopping

8-Button Easy Access Keyboard:

Button #	Description	Default Function
1	Go to favorite web site	Customer web site of choice
2	Go to AltaVista	AltaVista web site
3	Search	AltaVista search engine
4	Check Email	Launches user Email
5	Business Community	Industry specification info
6	Market Monitor	Launches Bloomberg market monitor
7	Meeting Center	Links to user's project center
8	News/PC Lock	News retrieval service

All buttons may be re-programmed by the user through the Easy Access utility.

C.2.5 KEYBOARD COMMANDS

Table C-1 lists the commands that the keyboard can send to the system (specifically, to the 8042-type logic).

Table C-1.
Keyboard-to-System Commands

Command	Value	Description
Key Detection Error/Over/run	00h [1] FFh [2]	Indicates to the system that a switch closure couldn't be identified.
BAT Completion	AAh	Indicates to the system that the BAT has been successful.
BAT Failure	FCh	Indicates failure of the BAT by the keyboard.
Echo	EEh	Indicates that the Echo command was received by the keyboard.
Acknowledge (ACK)	FAh	Issued by the keyboard as a response to valid system inputs (except the Echo and Resend commands).
Resend	FEh	Issued by the keyboard following an invalid input.
Keyboard ID	83ABh	Upon receipt of the Read ID command from the system, the keyboard issues the ACK command followed by the two IDS bytes.

Note:
[1] Modes 2 and 3.
[2] Mode 1 only.

C.2.6 SCAN CODES

The scan codes generated by the keyboard processor are determined by the mode the keyboard is operating in.

- Mode 1: In Mode 1 operation, the keyboard generates scan codes compatible with 8088-/8086-based systems. To enter Mode 1, the scan code translation function of the keyboard controller must be disabled. Since translation is not performed, the scan codes generated in Mode 1 are identical to the codes required by BIOS. Mode 1 is initiated by sending command F0h with the 01h option byte. Applications can obtain system codes and status information by using BIOS function INT 16h with AH=00h, 01h, and 02h.

- Mode 2: Mode 2 is the default mode for keyboard operation. In this mode, the 8042 logic translates the make codes from the keyboard processor into the codes required by the BIOS. This mode was made necessary with the development of the Enhanced III keyboard, which includes additional functions over earlier standard keyboards. Applications should use BIOS function INT 16h, with AH=10h, 11h, and 12h for obtaining codes and status data. In Mode 2, the keyboard generates the Break code, a two-byte sequence that consists of a Make code immediately preceded by F0h (i.e., Break code for 0Eh is "F0h 0Eh").

- Mode 3: Mode 3 generates a different scan code set from Modes 1 and 2. Code translation must be disabled since translation for this mode cannot be done.

Table C-2.
Keyboard Scan Codes

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
1	Esc	01/81	76/F0 76	08/na
2	F1	3B/BB	05/F0 05	07/na
3	F2	3C/BC	06/F0 06	0F/na
4	F3	3D/BD	04/F0 04	17/na
5	F4	3E/BE	0C/F0 0C	1F/na
6	F5	3F/BF	03/F0 03	27/na
7	F6	40/C0	0B/F0 0B	2F/na
8	F7	41/C1	83/F0 83	37/na
9	F8	42/C2	0A/F0 0A	3F/na
10	F9	43/C3	01/FO 01	47/na
11	F10	44/C4	09/F0 09	4F/na
12	F11	57/D7	78/F0 78	56/na
13	F12	58/D8	07/F0 07	5E/na
14	Print Scrn	E0 2A E0 37/E0 B7 E0 AA E0 37/E0 B7 [1] [2] 54/84 [3]	E0 2A E0 7C/E0 F0 7C E0 F0 12 E0 7C/E0 F0 7C [1] [2] 84/F0 84 [3]	57/na
15	Scroll Lock	46/C6	7E/F0 7E	5F/na
16	Pause	E1 1D 45 E1 9D C5/na E0 46 E0 C6/na [3]	E1 14 77 E1 F0 14 F0 77/na E0 7E E0 F0 7E/na [3]	62/na
17	`	29/A9	0E/F0 E0	0E/F0 0E
18	1	02/82	16/F0 16	46/F0 46
19	2	03/83	1E/F0 1E	1E/F0 1E
20	3	04/84	26/F0 26	26/F0 26
21	4	05/85	25/F0 25	25/F0 25
22	5	06/86	2E/F0 2E	2E/F0 2E
23	6	07/87	36/F0 36	36/F0 36
24	7	08/88	3D/F0 3D	3D/F0 3D
25	8	09/89	3E/F0 3E	3E/F0 3E
26	9	0A/8A	46/F0 46	46/F0 46
27	0	0B/8B	45/F0 45	45/F0 45
28	-	0C/8C	4E/F0 4E	4E/F0 4E
29	=	0D/8D	55/F0 55	55/F0 55
30	\	2B/AB	5D/F0 5D	5C/F0 5C
31	Backspace	0E/8E	66/F0 66	66/F0 66
32	Insert	E0 52/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 52/E0 D2 E0 AA [6]	E0 70/E0 F0 70 E0 F0 12 E0 70/E0 F0 70 E0 12 [5] E0 12 E0 70/E0 F0 70 E0 F0 12 [6]	67/na
33	Home	E0 47/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 47/E0 C7 E0 AA [6]	E0 6C/E0 F0 6C E0 F0 12 E0 6C/E0 F0 6C E0 12 [5] E0 12 E0 6C/E0 F0 6C E0 F0 12 [6]	6E/na
34	Page Up	E0 49/E0 C7 E0 AA E0 49/E0 C9 E0 2A [4] E0 2A E0 49/E0 C9 E0 AA [6]	E0 7D/E0 F0 7D E0 F0 12 E0 7D/E0 F0 7D E0 12 [5] E0 12 E0 7D/E0 F0 7D E0 F0 12 [6]	6F/na
35	Num Lock	45/C5	77/F0 77	76/na
36	/	E0 35/E0 B5 E0 AA E0 35/E0 B5 E0 2A [1]	E0 4A/E0 F0 4A E0 F0 12 E0 4A/E0 F0 4A E0 12 [1]	77/na
37	*	37/B7	7C/F0 7C	7E/na
38	-	4A/CA	7B/F0 7B	84/na
39	Tab	0F/8F	0D/F0 0D	0D/na
40	Q	10/90	15/F0 15	15/na

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key Pos	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
41	W	11/91	1D/F0 1D	1D/F0 1D
42	E	12/92	24/F0 24	24/F0 24
43	R	13/93	2D/F0 2D	2D/F0 2D
44	T	14/94	2C/F0 2C	2C/F0 2C
45	Y	15/95	35/F0 35	35/F0 35
46	U	16/96	3C/F0 3C	3C/F0 3C
47	I	17/97	43/F0 43	43/F0 43
48	O	18/98	44/F0 44	44/F0 44
49	P	19/99	4D/F0 4D	4D/F0 4D
50	[	1A/9A	54/F0 54	54/F0 54
51	]	1B/9B	5B/F0 5B	5B/F0 5B
52	Delete	E0 53/E0 D3 E0 AA E0 53/E0 D3 E0 2A [4] E0 2A E0 53/E0 D3 E0 AA [6]	E0 71/E0 F0 71 E0 F0 12 E0 71/E0 F0 71 E0 12 [5] E0 12 E0 71/E0 F0 71 E0 F0 12 [6]	64/F0 64
53	End	E0 4F/E0 CF E0 AA E0 4F/E0 CF E0 2A [4] E0 2A E0 4F/E0 CF E0 AA [6]	E0 69/E0 F0 69 E0 F0 12 E0 69/E0 F0 69 E0 12 [5] E0 12 E0 69/E0 F0 69 E0 F0 12 [6]	65/F0 65
54	Page Down	E0 51/E0 D1 E0 AA E0 51/E0 D1 E0 2A [4] E0 @a E0 51/E0 D1 E0 AA [6]	E0 7A/E0 F0 7A E0 F0 12 E0 7A/E0 F0 7A E0 12 [5] E0 12 E0 7A/E0 F0 7A E0 F0 12 [6]	6D/F0 6D
55	7	47/C7 [6]	6C/F0 6C [6]	6C/na [6]
56	8	48/C8 [6]	75/F0 75 [6]	75/na [6]
57	9	49/C9 [6]	7D/F0 7D [6]	7D/na [6]
58	+	4E/CE [6]	79/F0 79 [6]	7C/F0 7C
59	Caps Lock	3A/BA	58/F0 58	14/F0 14
60	A	1E/9E	1C/F0 1C	1C/F0 1C
61	S	1F/9F	1B/F0 1B	1B/F0 1B
62	D	20/A0	23/F0 23	23/F0 23
63	F	21/A1	2B/F0 2B	2B/F0 2B
64	G	22/A2	34/F0 34	34/F0 34
65	H	23/A3	33/F0 33	33/F0 33
66	J	24/A4	3B/F0 3B	3B/F0 3B
67	K	25/A5	42/F0 42	42/F0 42
68	L	26/A6	4B/F0 4B	4B/F0 4B
69	;	27/A7	4C/F0 4C	4C/F0 4C
70	‘	28/A8	52/F0 52	52/F0 52
71	Enter	1C/9C	5A/F0 5A	5A/F0 5A
72	4	4B/CB [6]	6B/F0 6B [6]	6B/na [6]
73	5	4C/CC [6]	73/F0 73 [6]	73/na [6]
74	6	4D/CD [6]	74/F0 74 [6]	74/na [6]
75	Shift (left)	2A/AA	12/F0 12	12/F0 12
76	Z	2C/AC	1A/F0 1A	1A/F0 1A
77	X	2D/AD	22/F0 22	22/F0 22
78	C	2E/AE	21/F0 21	21/F0 21
79	V	2F/AF	2A/F0 2A	2A/F0 2A
80	B	30/B0	32/F0 32	32/F0 32

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
81	N	31/B1	31/F0 31	31/F0 31
82	M	32/B2	3A/F0 3A	3A/F0 3A
83	,	33/B3	41/F0 41	41/F0 41
84	.	34/B4	49/F0 49	49/F0 49
85	/	35/B5	4A/F0 4A	4A/F0 4A
86	Shift (right)	36/B6	59/F0 59	59/F0 59
87		E0 48/E0 C8 E0 AA E0 48/E0 C8 E0 2A [4] E0 2A E0 48/E0 C8 E0 AA [6]	E0 75/E0 F0 75 E0 F0 12 E0 75/E0 F0 75 E0 12 [5] E0 12 E0 75/E0 F0 75 E0 F0 12 [6]	63/F0 63
88	1	4F/CF [6]	69/F0 69 [6]	69/na [6]
89	2	50/D0 [6]	72/F0 72 [6]	72/na [6]
90	3	51/D1 [6]	7A/F0 7A [6]	7A/na [6]
91	Enter	E0 1C/E0 9C	E0 5A/F0 E0 5A	79/F0 79[6]
92	Ctrl (left)	1D/9D	14/F0 14	11/F0 11
93	Alt (left)	38/B8	11/F0 11	19/F0 19
94	(Space)	39/B9	29/F0 29	29/F0 29
95	Alt (right)	E0 38/E0 B8	E0 11/F0 E0 11	39/na
96	Ctrl (right)	E0 1D/E0 9D	E0 14/F0 E0 14	58/na
97		E0 4B/E0 CB E0 AA E0 4B/E0 CB E0 2A [4] E0 2A E0 4B/E0 CB E0 AA [6]	E0 6B/Eo F0 6B E0 F0 12 E0 6B/E0 F0 6B E0 12[5] E0 12 E0 6B/E0 F0 6B E0 F0 12[6]	61/F0 61
98		E0 50/E0 D0 E0 AA E0 50/E0 D0 E0 2A [4] E0 2A E0 50/E0 D0 E0 AA [6]	E0 72/E0 F0 72 E0 F0 12 E0 72/E0 F0 72 E0 12[5] E0 12 E0 72/E0 F0 72 E0 F0 12[6]	60/F0 60
99		E0 4D/E0 CD E0 AA E0 4D/E0 CD E0 2A [4] E0 2A E0 4D/E0 CD E0 AA [6]	E0 74/E0 F0 74 E0 F0 12 E0 74/E0 F0 74 E0 12[5] E0 12 E0 74/E0 F0 74 E0 F0 12[6]	6A/F0 6A
100	0	52/D2 [6]	70/F0 70 [6]	70/na [6]
101	.	53/D3 [6]	71/F0 71 [6]	71/na [6]
102	na	7E/FE	6D/F0 6D	7B/F0 7B
103	na	2B/AB	5D/F0 5D	53/F0 53
104	na	36/D6	61/F0 61	13/F0 13
110	(Win95) [7]	E0 5B/E0 DB E0 AA E0 5B/E0 DB E0 2A [4] E0 2A E0 5B/E0 DB E0 AA [6]	E0 1F/E0 F0 1F E0 F0 12 E0 1F/E0 F0 1F E0 12 [5] E0 12 E0 1F/E0 F0 1F E0 F0 12 [6]	8B/F0 8B
111	(Win95) [7]	E0 5C/E0 DC E0 AA E0 5C/E0 DC E0 2A [4] E0 2A E0 5C/E0 DC E0 AA [6]	E0 2F/E0 F0 27 E0 F0 12 E0 27/E0 F0 27 E0 12 [5] E0 12 E0 27/E0 F0 27 E0 F0 12 [6]	8C/F0 8C
112	(Win Apps) [7]	E0 5D/E0 DD E0 AA E0 5D/E0 DD E0 2A [4] E0 2A E0 5D E0 DD E0 AA [6]	E0 2F/E0 F0 2F E0 F0 12 E0 2F/E0 F0 2F E0 12 [5] E0 12 E0 2F/E0 F0 2F E0 F0 12 [6	8D/F0 8D

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key		Make / Break Codes (Hex)		
Pos.	**Legend**	**Mode 1**	**Mode 2**	**Mode 3**
Btn 1	[8]	E0 1E/E0 9E	E0 1C/E0 F0 1C	95/F0 95
Btn 2	[8]	E0 26/E0 A6	E0 4B/E0 F0 4B	9C/F0 9C
Btn 3	[8]	E0 25/E0 A5	E0 42/E0 F0 42	9D/F0 9D
Btn 4	[8]	E0 23/E0 A3	E0 33/E0 F0 33	9A/F0 9A
Btn 5	[8]	E0 21/E0 A1	E0 2B/E0 F0 2B	99/F0 99
Btn 6	[8]	E0 12/E0 92	E0 24/E0 F0 24	96/F0 96
Btn 7	[8]	E0 32/E0 B2	E0 3A/E0 F0 3A	97/F0 97
Btn 1	[9]	E0 23/E0 A3	E0 33/E0 F0 33	9A/F0 9A
Btn 2	[9]	E0 1F/E0 9F	E0 1B/E0 F0 1B	80/F0 80
Btn 3	[9]	E0 1A/E0 9A	E0 54/E0 F0 54	99/F0 99
Btn 4	[9]	E0 1E/E0 9E	E0 1C/E0 F0 1C	95/F0 95
Btn 5	[9]	E0 13/E0 93	E0 2D/E0 F0 2D	0C/F0 0C
Btn 6	[9]	E0 14/E0 94	E0 2C/E0 F0 2C	9D/F0 9D
Btn 7	[9]	E0 15/E0 95	E0 35/E0 F0 35	96/F0 96
Btn 8	[9]	E0 1B/E0 9B	E0 5B/E0 F0 5B	97/F0 97

NOTES:

All codes assume Shift, Ctrl, and Alt keys inactive unless otherwise noted.
NA = Not applicable
[1] Shift (left) key active.
[2] Ctrl key active.
[3] Alt key active.
[4] Left Shift key active. For active right Shift key, substitute AA/2A make/break codes for B6/36 codes.
[5] Left Shift key active. For active right Shift key, substitute F0 12/12 make/break codes for F0 59/59 codes.
[6] Num Lock key active.
[7] Windows keyboards only.
[8] 7-Button Easy Access keyboard.
[9] 8-Button Easy Access keyboard.

C.3 CONNECTORS

Two types of keyboard interfaces are used in HP/Compaq systems: PS/2-type and USB-type. System units that provide a PS/2 connector will ship with a PS/2-type keyboard but may also support simultaneous connection of a USB keyboard. Systems that do not provide a PS/2 interface will ship with a USB keyboard. For a detailed description of the PS/2 and USB interfaces refer to Chapter 5 "Input/Output" of this guide. The keyboard cable connectors and their pinouts are described in the following figures:

Pin	Function
1	Data
2	Not connected
3	Ground
4	+5 VDC
5	Clock
6	Not connected

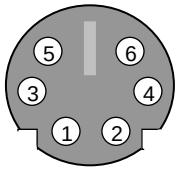


Figure C–9. PS/2 Keyboard Cable Connector (Male)

Pin	Function
1	+5 VDC
2	Data (-)
3	Data (+)
4	Ground

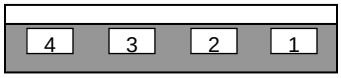


Figure C–10. USB Keyboard Cable Connector (Male)

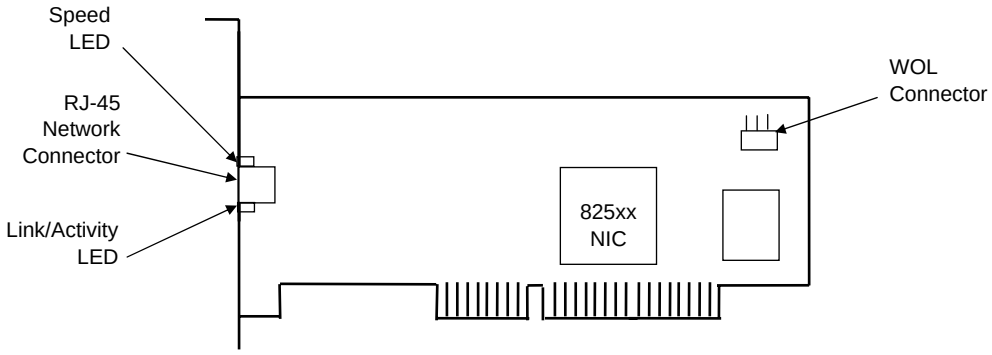
Appendix D
COMPAQ/INTEL
NETWORK INTERFACE CONTROLLER ADAPTERS

D.1 INTRODUCTION

This appendix describes Compaq/Intel Network Interface Controller adapters that may be included in the standard configuration on some models and available as options for all models. This appendix describes the following devices:

- Compaq/Intel PRO/100+ Management Adapter (SP# 116188-001)
- Compaq/Intel PRO/100 S Management Adapter (SP# 215774-001)

Each adapter card installs in a PCI slot to provide a system with network interface capability. **Unless otherwise indicated, the following information applies to both adapter cards.**



NOTES:

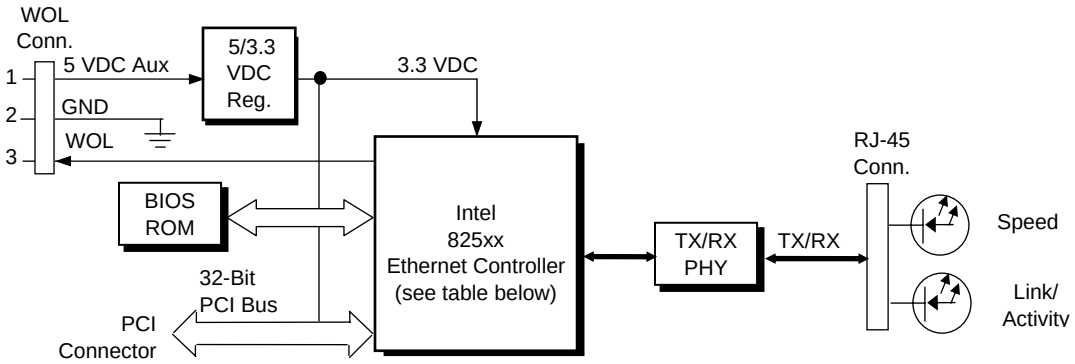
PRO/100+ Management Adapter, PCA# 108897
PRO/100 S Management Adapter, PCA# 213464

Figure D-1. Intel PRO/100+ or PRO/100 S Management Adapter Card Layout

This appendix covers the following subjects:

D.2 FUNCTIONAL DESCRIPTION

The Intel PRO/100+ and the PRO/100 S Management Adapters are based on the Intel 82559 and 82550 Ethernet Controllers (respectively) supported by firmware in flash ROM (see figure below). Each adapter can operate in half- or full-duplex modes and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification. Transmit and receive FIFOs of three kilobytes each reduce the chance of overrun while waiting for bus access. Each card includes an on-board 5/3.3 VDC regulator circuit and WOL connector in support of Wake-On-LAN functionality.



Controller Type	Featured on
82559	Intel PRO/100+ Management Adapter
82550	Intel PRO/100 S Management Adapter

Figure D-2. Intel PRP/100+ Management Adapter, Block diagram

Key features of these adapters include:

- 3-KB transmit and 3-KB receive FIFOs
- PCI ver. 2.2 compliant (PME- support)
- Dual-mode support with auto-switching between 10BASE-T and 100BASE-TX
- Both APM and ACPI power management compliant
- D0-D3 power state wake event support
- Boot ROM with PXE and RPL support

The 82559 and 82550 controllers feature high and low priority queues and provides priority-packet processing for networks that support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (undersized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run. An EEPROM is used to store identification, configuration, and connection parameters.

The 82550 controller provides all the functionality of the 82559 plus IP security (IPSEC) support through a hardware accelerator engine.

D.2.1 AOL FUNCTION

The adapter's Alert-On-LAN (AOL) function provides a AOL-compliant system unit with the ability to communicate system status to a management console, even while the system is powered down. When installed in an AOL-compliant system, the adapter receives alert messages from the system's south bridge over the PCI bus. Each alert message decoded by the adapter results in a pre-constructed status message being transmitted over the network to a management console.

Alert-On-LAN functionality occurs independent of software, driver, or even processor intervention. The adapter can report following conditions:

- System tampering – Removal of the chassis cover
- BIOS failure – System fails to boot successfully
- OS problem – System fails to load operating system after boot
- Missing/faulty processor – Processor fails to fetch first instruction
- Thermal condition – High temperature detected in system
- Heartbeat – Indication of system's presence on the network (sent approximately every 30 seconds)

△ **NOTE:** The system unit must be plugged into a live AC outlet for the AOL function to be operative. **Controlling a system unit's power through an AC outlet strip will, when the strip is turned off, disable AOL functionality.**

The AOL implementation requirements are as follows:

1. System unit featuring the 810, 810e, 820, or 850 (or later) chipset.
2. Intel PRO/100+ Management Adapter Driver 3.1 or later (available from HP/Compaq).
3. Client-side utility agent software (available from HP/Compaq).
4. Management console running one of the following:
   a. HP OpenView Network Node Manager 6.x.
   b. Intel LANDesk Client Manager.
   c. Compaq Insight Manager.

D.2.2 WAKE UP FUNCTIONS

The adapter provides two types of wake-up signaling: the PME- signal and the WOL signal.

The adapter provides PME- signal support for systems compliant with PCI ver. 2.2. The detection of any wake event results in the adapter's assertion of the PME- signal, which can be used by the system unit to initiate the power-up sequence. System software is responsible for the clearing the PME- signal.

The adapter also includes a WOL interface for systems supporting that method of wake-up. The adapter asserts the WOL signal for 50 milliseconds upon detection of a Magic Packet. The WOL signal is routed to the system unit (through a three-conductor cable connection) for initializing a power-up sequence.

D.2.3 IPSEC FUNCTION

The 82550 controller used on the Intel PRO/100 S Management Adapter includes an encryption engine that provides on-the-fly encryption and/or authentication of transmit data without additional use of system memory and software. This function, referred to as IP security (IPSEC), uses a configurable algorithm and established Data Encryption Standards (DES) to provide high performance (full transmission rate) encryption. Received IPSEC data frames are re-submitted to the controller for processing and then returned to the driver.

Key features of IPSEC support include:

- Encryption capability of 56-bit DES to 168-bit 3DES
- Out-of-order processing of non-security transmit frames during security mode
- SHA-1 and MD-5 authentication with optional HMAC cryptographic hashing

D.3 POWER MANAGEMENT SUPPORT

These adapters support APM and ACPI power management environments as well as the Wired-for-Management (WfM) and Wake-On-LAN (WOL) standards. The adapter is designed to be powered up as long as the system unit is plugged into a live AC outlet to provide system "wake-up" functionality. Power is provided by either the auxiliary 3.3 VDC power rail of the PCI bus (when installed in systems compliant with PCI ver. 2.2) or by auxiliary 5 VDC through the WOL connector.

NOTE: Controlling a system unit's power through an AC outlet strip will**, with the strip turned off, disable wake-up functionality.**

D.3.1 APM ENVIRONMENT

The Advanced Power Management (APM) functionality of system wake up is implemented through the system's APM-compliant BIOS and Magic Packet-compliant hardware. This environment is not dependent on operating system (OS) intervention allowing a unit plugged into a live AC outlet to be turned on remotely over the network (i.e., "remote wake-up") even if the OS has not been installed. In APM mode the controller will respond upon receiving a Magic Packet, which is a packet where the node's address is repeated 16 times. Upon Magic Packet reception, the adapter asserts the PME- signal (on the PCI bus) resulting in the system unit's power control logic turning on the system and initiating the boot sequence. After the boot sequence the BIOS clears the PME- signal so that subsequent wake up events will be detected.

D.3.2 ACPI ENVIRONMENT

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS (such as Windows NT 5.0) and is the default power management mode. The following wake up events may be individually enabled/disabled through the software driver supplied with the adapter:

- Magic Packet – Packet with node address repeated 16 times in data portion.
- Individual address match – Directed acket with matching user-defined byte mask.
- Multicast address match – Directed packet with matching user-defined sample frame.
- ARP (address resolution protocol) packet
- Flexible packet filtering – Packets that match defined CRC signature.
- NBT query (under Ipv4)
- IPX Diagnostic
- TCO packet
- VLAN Type

When an enabled event is received the controller asserts the PME- signal that is used to initiate the wakeup sequence.

D.4 ADAPTER PROGRAMMING

Programming the adapter consists of configuration, which occurs during POST, and control, which occurs at runtime.

D.4.1 CONFIGURATION

The adapter's 82559 or 82550 NIC controller is a PCI device and configured though PCI configuration space registers using PCI protocol described in chapter 4 of this guide. The PCI configuration registers are listed in the following table:

Table D-1.
PCI Configuration Registers

PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vender ID	8086h	10-13h	Cntrl. Reg. Base Addr. (Mem)	0000h
02-03h	Device ID	1229h	14-17h	Cntrl. Reg. Base Addr. (I/O)	00h
04-05h	PCI Command	0000h	18-1Bh	Flash Mem. Base Addr.	00h
06-07h	PCI Status	0280h	2C-2Dh	Subsystem Vender ID	
08h	Revision ID	xxh	2E-2Fh	Subsystem ID	
09-0Bh	Class Code	01h	30-33h	Expansion ROM Base Addr.	
0Ch	Cache Line Size	01h	34h	Cap-Ptr	
0Dh	Latency Timer	04h	3C-3D	Interrupt Line/Pin	
0Eh	Header Type	00h	3E-3Fh	Min Gnt/Max Lat	
0Fh	BIST	00h	DC-E3h	Power Mgmt. Functions	

NOTE:
Assume unmarked gaps are reserved and/or not used.

D.4.2 CONTROL

The adapter's 82559 or 82550 controller is controlled though registers that may be mapped in system memory space or variable I/O space. The registers are listed in the following table:

Table D-2.
Control Registers

Offset Addr. / Register	No. of Bytes	Offset Addr. / Register	No. of Bytes
00h SCB Status	2	19h Flow Control Register	2
02h SCB Command	2	1Bh PMDR	1
04h SCB General Pointer	4	1Ch General Control	1
08h PORT	4	1Dh General Status	1
0Ch Flash Control Reg.	2	1E-2Fh Reserved	10
0Eh EEPROM Control Reg.	2	30h Function Event Register	4
10h Mgmt. Data I/F Cntrl. Reg.	4	34h Function Event Mask Register	4
14h Rx Direct Mem. Access Byte Cnt.	4	38h Function Present State Register	4
18h Early Receive Interrupt	1	20h Force Event Register	4

Not implemented in these systems (CardBus registers).

D.5 NETWORK CONNECTOR

The figure below shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

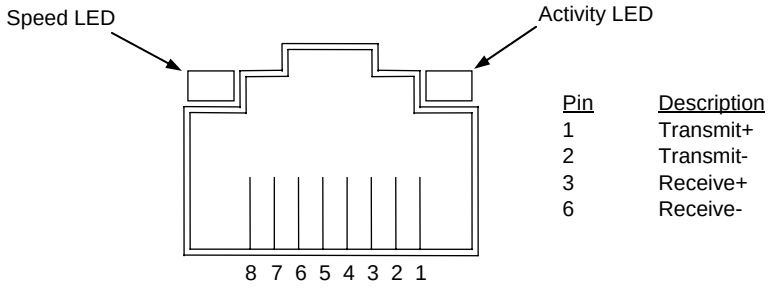


Figure D-3. Ethernet TPE Connector (RJ-45, viewed from card edge)

D.6 ADAPTER SPECIFICATIONS

Table D-3.
Adapter Specifications

Parameter	
Modes Supported	10BASE-T half duplex @ 10 MB/s 10Base-T full duplex @ 20 MB/s 100BASE-TX half duplex @ 100 MB/s 100Base-TX full duplex @ 200 MB/s
Encryption Standards (82550 only)	DES/3DES, HMAC SHA-1, MD5
Standards Compliance	IEEE VLAN (802.1A) IEEE 802.2 IEEE 802.3 & 802.3u IEEE Intel priority packet (801.1p)
OS Driver Support	MS Windows 95,98, 2000, XP, Mandrake Linux 8.2 MS Windows NT 3.51 & 4.0 Novell Netware 3.11, 3.12, & 4.1x; 5 Server Sunsoft Solaris SCO UnixWare Open Desktop OpenServer
Boot ROM Support	Intel PRO/100 Boot Agent (PXE 2.0, RPL)
F12 BIOS Support	Yes
Bus Inteface	PCI 2.2
Power Management Support	APM, ACPI, PCI Power Management Spec.
Power Comsumption	0.750 mW (max)

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