HUAWEI ME919Bs Series LTE LGA Module

Hardware Guide

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About This Document

Revision History

Document Version	Date	Chapter	Descriptions
01	2017-10-10	-	Creation
02	2017-12-11	Title Page	Deleted the content about the Privacy Policy
		3.4.2	Added the notes about the Table 3-7 Parameters description
		6.4	Updated the Figure 6-1 Dimensions (unit: mm)
		6.7.2	Updated the Figure 6-11 ME919Bs Series LTE LGA module Footprint design (unit: mm)
03	2018-02-23	2.2	Updated the note for extended operating temperature of Table 2-1 Features
04	2019-06-19	-	Add: ME919Bs-127bNb ME919Bs-821bNb ME919Bs-567bNb

Contents

1 Introduction

This document describes the hardware application interfaces and air interfaces provided by HUAWEI ME919Bs series LTE LGA module.

This document helps hardware engineers to understand the interface specifications, electrical features and related product information of the ME919Bs module.

Products	Bands
ME919Bs-127bN/ ME919Bs-127bNb	**LTE FDD:** B1/B3/B7/B8/B20/B28 **LTE TDD:** B38 **WCDMA/HSPA+:** B1/B8 **GSM/GPRS/EDGE:** 900/1800 MHz **CA:** B1+B3, B3+B3, B3+B7, B3+B20, B3+B28, B3+B38, B7+B20, B7+B28 **GPS:** GPS L1, GLONASS L1, Galileo L1
ME919Bs-567bN/ ME919Bs-567bNb	**LTE FDD:** B2/B4/B5/B7/B12/B13/B29 **WCDMA/HSPA+:** B2/B4/B5 **GSM/GPRS/EDGE:** 850/1900 MHz **CA:** B2+B5, B2+B12, B2+B29, B4+B5, B4+B7, B4+B12, B4+B29, B2+B4, B2+B13, B4+B13 **GPS:** GPS L1
ME919Bs-821bN/ ME919Bs-821bNb	**LTE FDD:** B1/B3/B5/B8/B19 **LTE TDD:** B38/B39/B40/B41 (CUCC&CMCC) **WCDMA/HSPA+:** B1/B5/B8/B19 **TDSCDMA:** B34/B39 **GSM/GPRS/EDGE:** 900/1800 MHz **CA:** B1+B3, B1+B8, B1+B19, B3+B19, B3+B3, B3+B5, B3+B8, B38+B38, B39+B39, B39+B41, B40+B40, B41+B41 **GPS:** GPS L1, Beidou B1

2 Overall Description

2.1 About This Chapter

This chapter mainly describes the general description of the module, including:

- Function Overview
- Circuit Block Diagram
- Application Block Diagram

2.2 Function Overview

Table 2-1 Features

Feature	Description
Physical Dimensions	Dimensions (L × W × H): 35 mm × 35 mm × 3.15 mm Weight: about 8.5 g
Operating Temperature	Normal operating temperature: –30°C to +75°C Extended operating temperature[1]: –40°C to +85°C
Storage Temperature	–40°C to +95°C
Humidity	RH5% to RH95%
Power Voltage	DC 3.8 V to 4.2 V (typical value is 4.0 V)
Antenna Interface	WWAN MAIN antenna pad x 1 WWAN AUX antenna pad x 1 GPS antenna pad x 1
SMS	Supporting MO and MT Supporting formats of TEXT and PDU

Feature	Description
Data Services	LTE Cat 6 (300/50 Mbps @ 40 MHz BW) LTE Cat 4 (150/50 Mbps @ 20 MHz BW) DC-HSPA+: 42/5.76 Mbps HSPA+: 21/5.76 Mbps EDGE DL: 236.8 kbps/UL: 236.8 kbps (Multislot Class 12) GPRS DL: 85.6 kbps/UL: 85.6 kbps (Multislot Class 12) GSM: 9.6 kbps/14.4 kbps

NOTE

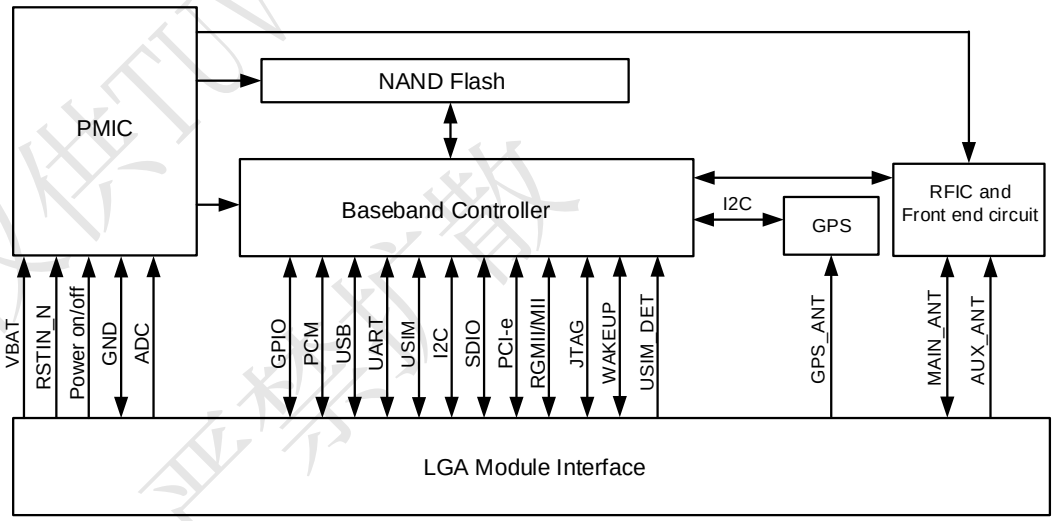
[1]: When the module works at –40°C to –30°C or 75°C to 85°C, **NOT** all its RF performances comply with 3GPP specifications, but still can make and receive voice calls, SMS and data calls.

2.3 Circuit Block Diagram

The module is developed based on Huawei's Balong platform. Figure 2-1 shows the circuit block diagram. The major functional units contain the following parts:

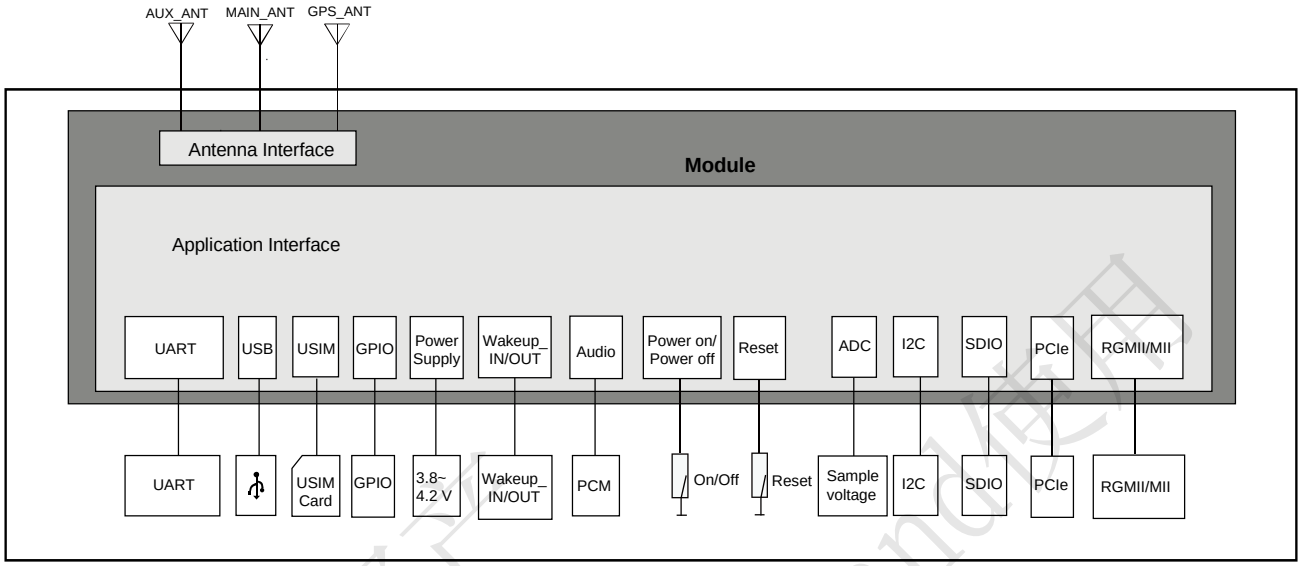
- Power Management
- Baseband Controller
- Nand Flash
- RF Circuit
- GPS Circuit

Figure 2-1 Circuit block diagram of the module



2.4 Application Block Diagram

Figure 2-2 Application block diagram of the module



UART Interface:	The module supports four UART interfaces. Three are 4-wire UARTs, and the other one is 2-wire UART, which is only for debugging.
USB Interface:	The USB interface supports USB 2.0 high speed standard.
USIM Interface:	The USIM interface provides the interface for a USIM card.
GPIO:	General Purpose I/O pins
External Power Supply:	DC 4 V is recommended.
Audio Interface:	The module supports one PCM interface.
RF Pad:	RF antenna interface
ADC Interface:	Analog-to-Digital Converter
I2C Interface:	Inter-Integrated Circuit
SDIO Interface:	Secure Digital Input and Output (SD3.0)
PCIe Interface	Peripheral Component Interface Express
RGMII Interface	Reduced Gigabit Media Independent Interface
MII Interface	Media Independent Interface

3 Description of the Application Interfaces

3.1 About This Chapter

This chapter mainly describes the external application interfaces of the module, including:

- LGA Interface
- Power Interface
- Signal Control Interface
- UART Interface
- USB Interface
- USIM Card Interface
- Audio Interface
- GPIO Interface
- GPS PPS Interface
- ADC Interface
- JTAG Interface
- I2C Interface
- SDIO Interface
- PCIe Interface
- RGMII/MII Interface
- RF Antenna Interface
- Reserved Pins
- Interface States in Sleep Mode
- Test Points Design

3.2 LGA Interface

The ME919Bs LGA module uses the 336-pin LGA as its external interface.

Figure 3-1 Sequence of LGA interface (**Top view**)

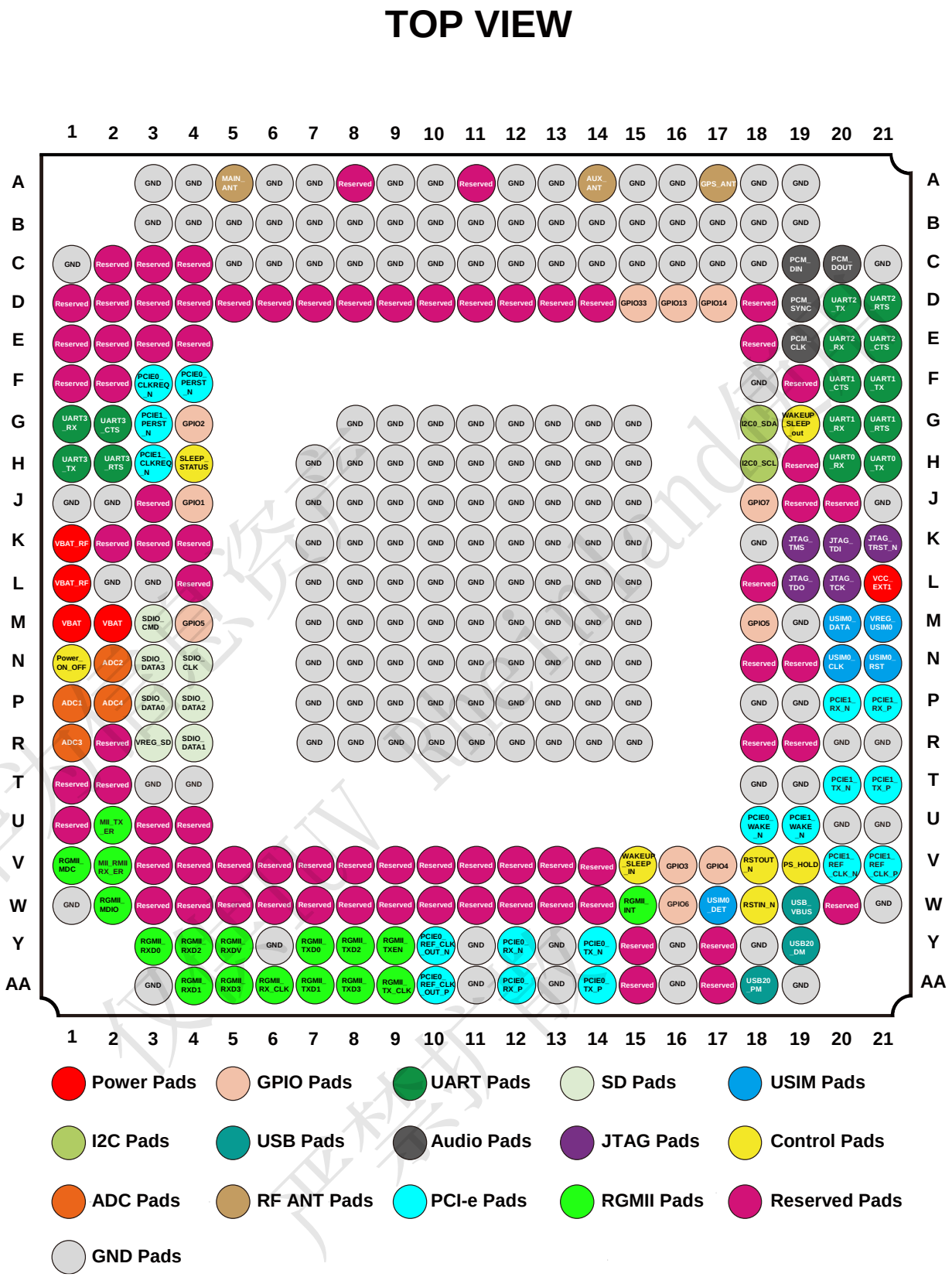


Figure 3-2 Appearance of the module (**Without Label**)

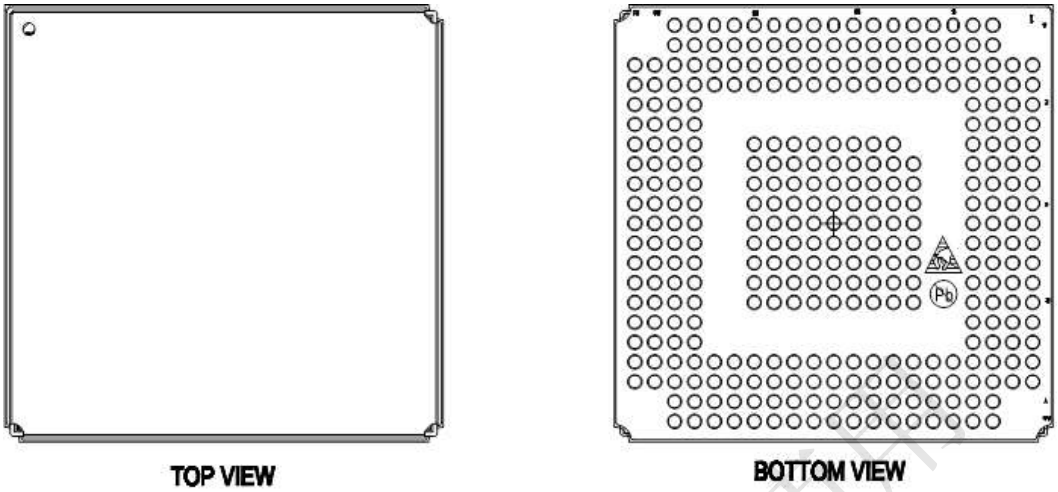


Table 3-1 Definitions of pins on the LGA interface

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
M1	VBAT	-	PI	Power supply of PMIC	3.8–4.2
M2	VBAT	-	PI	Power supply of PMIC	3.8–4.2
K1	VBAT_RF	-	PI	Power supply of RFIC	3.8–4.2
L1	VBAT_RF	-	PI	Power supply of RFIC	3.8–4.2
L21	VCC_EXT1	-	PO	Module output 1.8V voltage	1.8
J4	GPIO1	-	I/O	General Purpose I/O pin	1.8
G4	GPIO2	-	I/O	General Purpose I/O pin	1.8
V16	GPIO3	-	I/O	General Purpose I/O pin	1.8
V17	GPIO4	-	I/O	General Purpose I/O pin	1.8
M4	GPIO5	-	I/O	General Purpose I/O pin	1.8
W16	GPIO6	-	I/O	General Purpose I/O pin	1.8
J18	GPIO7	-	I/O	General Purpose I/O pin	1.8
D16	GPIO13	-	I/O	General Purpose I/O pin	1.8
D17	GPIO14	-	I/O	General Purpose I/O pin	1.8
M18	GPIO15	-	I/O	General Purpose I/O pin	1.8
D15	GPIO33	-	I/O	General Purpose I/O pin	1.8
H21	UART0_TX	-	O	UART0 transmit data output for debug	1.8

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
H20	UART0_RX	-	I	UART0 receive data input for debug	1.8
F21	UART1_TX	-	O	UART1 transmit data output	1.8
G20	UART1_RX	-	I	UART1 receive data input	1.8
G21	UART1_RTS	-	O	UART1 request to send	1.8
F20	UART1_CTS	-	I	UART1 clear to send	1.8
D20	UART2_TX	-	O	UART2 transmit data output	1.8
E20	UART2_RX	-	I	UART2 receive data input	1.8
D21	UART2_RTS	-	O	UART2 request to send	1.8
E21	UART2_CTS	-	I	UART2 clear to send	1.8
H1	UART3_TX	-	O	UART3 transmit data output	1.8
G1	UART3_RX	-	I	UART3 receive data input	1.8
H2	UART3_RTS	-	O	UART3 request to send	1.8
G2	UART3_CTS	-	I	UART3 clear to send	1.8
R3	VREG_SD	-	PO	Power supply for SDIO	2.85
N4	SDIO_CLK	-	O	Secure digital clock	1.8/2.85
M3	SDIO_CMD	-	I/O	Secure digital command	1.8/2.85
P3	SDIO_DATA0	-	I/O	Secure digital data bit 0	1.8/2.85
R4	SDIO_DATA1	-	I/O	Secure digital data bit 1	1.8/2.85
P4	SDIO_DATA2	-	I/O	Secure digital data bit 2	1.8/2.85
N3	SDIO_DATA3	-	I/O	Secure digital data bit 3	1.8/2.85
J3	Reserved	-	-	Reserved for future use	-
M21	VREG_USIM0	-	PO	Power source for SIM card	1.8/3.0
N20	USIM0_CLK	-	O	SIM clock	1.8/3.0
M20	USIM0_DATA	-	I/O	SIM data	1.8/3.0
N21	USIM0_RST	-	O	SIM reset	1.8/3.0
W17	USIM0_DET	-	I	SIM card detect	1.8
H18	I2C0_SCL	-	O	I2C clock and it is an open drain	1.8
G18	I2C0_SDA	-	I/O	I2C data and it is an open drain	1.8
W19	USB_VBUS	-	PI	USB_VBUS detection voltage	5

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
W20	Reserved	-	-	Reserved for future use	-
AA18	USB20_DP	-	I/O	USB2.0 differential data - plus	-
Y19	USB20_DM	-	I/O	USB2.0 differential data - minus	-
AA17	Reserved	-	-	Reserved for future use	-
Y17	Reserved	-	-	Reserved for future use	-
AA15	Reserved	-	-	Reserved for future use	-
Y15	Reserved	-	-	Reserved for future use	-
D19	PCM_SYNC	I2S_SYNC	O	PCM interface sync signal	1.8
C19	PCM_DIN	I2S_DIN	I	PCM data input	1.8
C20	PCM_DOUT	I2S_DOUT	O	PCM data output	1.8
E19	PCM_CLK	I2S_CLK	O	PCM interface clock	1.8
J19	Reserved	-	-	Reserved for future use	-
L20	JTAG_TCK	-	I	JTAG clock input	1.8
K20	JTAG_TDI	-	I	JTAG test data input	1.8
L19	JTAG_TDO	-	O	JTAG test data output	1.8
K19	JTAG_TMS	-	I	JTAG test mode select	1.8
K21	JTAG_TRST_N	-	I	JTAG reset	1.8
J20	Reserved	-	-	Reserved for future use	-
V14	Reserved	-	-	Reserved for future use	-
N1	Power_ON_OFF	-	I	Power on and power off signal	1.8
V19	PS_HOLD	-	O	Indicates whether the PMIC finished the power procedure or not. It is recommended to be connected to a test point.	1.8
W18	RSTIN_N	-	I	Reset input signal	1.8
V18	RSTOUT_N	-	O	Reset output signal, indicate the reset of PMIC. It is recommended to be connected to a test point.	1.8
V15	WAKEUP_SLEEP_IN	-	I	Module sleep status control pin	1.8

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
G19	WAKEUP_SLEEP_OUT	-	O	Module to wake up the host	1.8
H4	SLEEP_STATUS	-	O	Indicates sleep status of module	1.8
U1	Reserved	-	-	Reserved for future use	-
T1	Reserved	-	-	Reserved for future use	-
P1	ADC1	-	I	ADC input signal	0–1.8
N2	ADC2	-	I	ADC input signal	0–1.8
R1	ADC3	-	I	ADC input signal	0–1.8
P2	ADC4	-	I	ADC input signal	0–1.8
R2	Reserved	-	-	Reserved for future use	-
T2	Reserved	-	-	Reserved for future use	-
A5	MAIN_ANT	-	-	Main antenna	-
A14	AUX_ANT	-	-	AUX antenna	-
A8	Reserved	-	-	Reserved for future use	-
A11	Reserved	-	-	Reserved for future use	-
A17	GPS_ANT	-	-	GPS antenna	-
F3	PCIE0_CLKREQ_N	GPIO34	PCIE: I GPIO: I/O	PCIe0 clock request (active-low) or General Purpose I/O pin	1.8
U18	PCIE0_WAKE_N	GPIO16	PCIE: I GPIO: I/O	PCIe0 client wake up (active-low) or General Purpose I/O pin	1.8
F4	PCIE0_PERST_N	GPIO17	PCIE: O GPIO: I/O	PCIe0 client reset (active-low) or General Purpose I/O pin	1.8
AA14	PCIE0_TX_P	-	O	PCIe0 transmit – plus	-
Y14	PCIE0_TX_N	-	O	PCIe0 transmit – minus	-
AA12	PCIE0_RX_P	-	I	PCIe0 receive – plus	-
Y12	PCIE0_RX_N	-	I	PCIe0 receive – minus	-
AA10	PCIE0_REF_CLK_P	-	O	PCIe0 differential reference clock - plus	-
Y10	PCIE0_REF_CLK_N	-	O	PCIe0 differential reference clock - minus	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
H3	PCIE1_CLKREQ_N	GPIO8	PCIE: I GPIO:I/O	PCIe1 clock request (open drain requires external 100 k PU, active-low) or General Purpose I/O pin	1.8
U19	PCIE1_WAKE_N	GPIO9	PCIE: I GPIO: I/O	PCIe1 client wake up (active-low) or General Purpose I/O pin	1.8
G3	PCIE1_PERST_N	GPIO10	PCIE: O GPIO: I/O	PCIe1 client reset (active-low) or General Purpose I/O pin	1.8
T21	PCIE1_TX_P	-	O	PCIe1 transmit – plus	-
T20	PCIE1_TX_N	-	O	PCIe1 transmit – minus	-
P21	PCIE1_RX_P	-	I	PCIe1 receive – plus	-
P20	PCIE1_RX_N	-	I	PCIe1 receive – minus	-
V21	PCIE1_REF_CLK_P	-	O	PCIe1 differential reference clock - plus	-
V20	PCIE1_REF_CLK_N	-	O	PCIe1 differential reference clock - minus	-
AA9	RGMII_TX_CLK / MII_TX_CLK	GPIO18	RGMII: O MII: I GPIO: I/O	RGMII/MII transmit clock or General Purpose I/O pin	1.8
AA6	RGMII_RX_CLK/ MII_RX_CLK	GPIO19	RGMII/MII: O GPIO: I/O	RGMII/MII receive clock or General Purpose I/O pin	1.8
Y5	RGMII_RXDV/ MII_RXDV	GPIO20	RGMII/MII: I GPIO: I/O	RGMII/MII received data valid or General Purpose I/O pin	1.8
Y3	RGMII_RXD0/ MII_RXD0	GPIO21	RGMII/MII: I GPIO: I/O	RGMII/MII received data 0 or General Purpose I/O pin	1.8
AA4	RGMII_RXD1/ MII_RXD1	GPIO22	RGMII/MII: I GPIO: I/O	RGMII/MII received data 1 or General Purpose I/O pin	1.8
Y4	RGMII_RXD2/ MII_RXD2	GPIO23	RGMII/MII: I GPIO:I/O	RGMII/MII received data 2 or General Purpose I/O pin	1.8
AA5	RGMII_RXD3/ MII_RXD3	GPIO24	RGMII/MII: I GPIO:I/O	RGMII/MII received data 3 or General Purpose I/O pin	1.8

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
Y9	RGMII_TXEN/ MII_TXEN	GPIO25	RGMII/MII: O GPIO:I/O	RGMII/MII transmit enable (active-high) or General Purpose I/O pin	1.8
Y7	RGMII_TXD0/ MII_TXD0	GPIO26	RGMII/MII: O GPIO:I/O	RGMII/MII transmit data 0 or General Purpose I/O pin	1.8
AA7	RGMII_TXD1/ MII_TXD1	GPIO27	RGMII/MII: O GPIO:I/O	RGMII/MII transmit data 1 or General Purpose I/O pin	1.8
Y8	RGMII_TXD2/ MII_TXD2	GPIO28	RGMII/MII: O GPIO:I/O	RGMII/MII transmit data 2 or General Purpose I/O pin	1.8
AA8	RGMII_TXD3/ MII_TXD3	GPIO29	RGMII/MII: O GPIO:I/O	RGMII/MII transmit data 3 or General Purpose I/O pin	1.8
V1	RGMII_MDC/ MII_MDC	GPIO30	RGMII/MII: O GPIO:I/O	Management data clock reference or General Purpose I/O pin	1.8
W2	RGMII_MDIO/ MII_MDIO	GPIO31	I/O	Management data I/O, open drain or General Purpose I/O pin.	1.8
W15	RGMII_INT/ MII_INT/GPIO	GPIO32	RGMII/MII: I GPIO:I/O	RGMII interrupt signal or General Purpose I/O pin	1.8
U2	MII_TX_ER	GPIO11	MII:O GPIO:I/O	Transmit error or General Purpose I/O pin	1.8
V2	MII_RMII_RX_ER	GPIO12	MII:I GPIO:I/O	Receive error or General Purpose I/O pin	1.8
H19	FAST_USB_LOAD	-	I	USB Fast boot (active low), leave a test pin	1.8
K3	Reserved	-	-	Reserved for future use	-
K2	Reserved	-	-	Reserved for future use	-
F19	Reserved	-	-	Reserved for future use	-
L18	Reserved	-	-	Reserved for future use	-
K4	Reserved	-	-	Reserved for future use	-
L4	Reserved	-	-	Reserved for future use	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
N18	Reserved	-	-	Reserved for future use	-
E18	Reserved	-	-	Reserved for future use	-
D18	Reserved	-	-	Reserved for future use	-
N19	Reserved	-	-	Reserved for future use	-
R19	Reserved	-	-	Reserved for future use	-
R18	Reserved	-	-	Reserved for future use	-
D5	Reserved	-	-	Reserved for future use	-
D6	Reserved	-	-	Reserved for future use	-
D7	Reserved	-	-	Reserved for future use	-
D8	Reserved	-	-	Reserved for future use	-
E4	Reserved	-	-	Reserved for future use	-
D4	Reserved	-	-	Reserved for future use	-
E3	Reserved	-	-	Reserved for future use	-
D3	Reserved	-	-	Reserved for future use	-
E2	Reserved	-	-	Reserved for future use	-
D2	Reserved	-	-	Reserved for future use	-
E1	Reserved	-	-	Reserved for future use	-
D1	Reserved	-	-	Reserved for future use	-
F2	Reserved	-	-	Reserved for future use	-
F1	Reserved	-	-	Reserved for future use	-
C2	Reserved	-	-	Reserved for future use	-
C3	Reserved	-	-	Reserved for future use	-
C4	Reserved	-	-	Reserved for future use	-
D9	Reserved	-	-	Reserved for future use	-
D10	Reserved	-	-	Reserved for future use	-
V11	Reserved	-	-	Reserved for future use	-
V12	Reserved	-	-	Reserved for future use	-
V13	Reserved	-	-	Reserved for future use	-
D11	Reserved	-	-	Reserved for future use	-
D12	Reserved	-	-	Reserved for future use	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
D13	Reserved	-	-	Reserved for future use	-
D14	GPS_PPS_OUT	-	O	Reserved pin Reserved for GPS_PPS_OUT pin This pin output PPS (pulse per second) signal.	2.85
W11	Reserved	-	-	Reserved for future use	-
W12	Reserved	-	-	Reserved for future use	-
W13	Reserved	-	-	Reserved for future use	-
W14	Reserved	-	-	Reserved for future use	-
U3	Reserved	-	-	Reserved for future use	-
U4	Reserved	-	-	Reserved for future use	-
V3	Reserved	-	-	Reserved for future use	-
V4	Reserved	-	-	Reserved for future use	-
V5	Reserved	-	-	Reserved for future use	-
V6	Reserved	-	-	Reserved for future use	-
V7	Reserved	-	-	Reserved for future use	-
V8	Reserved	-	-	Reserved for future use	-
V9	Reserved	-	-	Reserved for future use	-
V10	Reserved	-	-	Reserved for future use	-
W3	Reserved	-	-	Reserved for future use	-
W4	Reserved	-	-	Reserved for future use	-
W5	Reserved	-	-	Reserved for future use	-
W6	Reserved	-	-	Reserved for future use	-
W7	Reserved	-	-	Reserved for future use	-
W8	Reserved	-	-	Reserved for future use	-
W9	Reserved	-	-	Reserved for future use	-
W10	Reserved	-	-	Reserved for future use	-
C21	GND	-	-	GND	-
J21	GND	-	-	GND	-
R21	GND	-	-	GND	-
U21	GND	-	-	GND	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
W21	GND	-	-	GND	-
R20	GND	-	-	GND	-
U20	GND	-	-	GND	-
A19	GND	-	-	GND	-
B19	GND	-	-	GND	-
P19	GND	-	-	GND	-
M19	GND	-	-	GND	-
T19	GND	-	-	GND	-
AA19	GND	-	-	GND	-
A18	GND	-	-	GND	-
B18	GND	-	-	GND	-
C18	GND	-	-	GND	-
F18	GND	-	-	GND	-
K18	GND	-	-	GND	-
P18	GND	-	-	GND	-
T18	GND	-	-	GND	-
Y18	GND	-	-	GND	-
B17	GND	-	-	GND	-
C17	GND	-	-	GND	-
A16	GND	-	-	GND	-
B16	GND	-	-	GND	-
C16	GND	-	-	GND	-
Y16	GND	-	-	GND	-
AA16	GND	-	-	GND	-
A15	GND	-	-	GND	-
B15	GND	-	-	GND	-
C15	GND	-	-	GND	-
G15	GND	-	-	GND	-
H15	GND	-	-	GND	-
J15	GND	-	-	GND	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
K15	GND	-	-	GND	-
L15	GND	-	-	GND	-
M15	GND	-	-	GND	-
N15	GND	-	-	GND	-
P15	GND	-	-	GND	-
R15	GND	-	-	GND	-
B14	GND	-	-	GND	-
C14	GND	-	-	GND	-
G14	GND	-	-	GND	-
H14	GND	-	-	GND	-
J14	GND	-	-	GND	-
K14	GND	-	-	GND	-
L14	GND	-	-	GND	-
M14	GND	-	-	GND	-
N14	GND	-	-	GND	-
P14	GND	-	-	GND	-
R14	GND	-	-	GND	-
A13	GND	-	-	GND	-
B13	GND	-	-	GND	-
C13	GND	-	-	GND	-
G13	GND	-	-	GND	-
H13	GND	-	-	GND	-
J13	GND	-	-	GND	-
K13	GND	-	-	GND	-
L13	GND	-	-	GND	-
M13	GND	-	-	GND	-
N13	GND	-	-	GND	-
P13	GND	-	-	GND	-
R13	GND	-	-	GND	-
Y13	GND	-	-	GND	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
AA13	GND	-	-	GND	-
A12	GND	-	-	GND	-
B12	GND	-	-	GND	-
C12	GND	-	-	GND	-
G12	GND	-	-	GND	-
H12	GND	-	-	GND	-
J12	GND	-	-	GND	-
K12	GND	-	-	GND	-
L12	GND	-	-	GND	-
M12	GND	-	-	GND	-
N12	GND	-	-	GND	-
P12	GND	-	-	GND	-
R12	GND	-	-	GND	-
B11	GND	-	-	GND	-
C11	GND	-	-	GND	-
G11	GND	-	-	GND	-
H11	GND	-	-	GND	-
J11	GND	-	-	GND	-
K11	GND	-	-	GND	-
L11	GND	-	-	GND	-
M11	GND	-	-	GND	-
N11	GND	-	-	GND	-
P11	GND	-	-	GND	-
R11	GND	-	-	GND	-
Y11	GND	-	-	GND	-
AA11	GND	-	-	GND	-
A10	GND	-	-	GND	-
B10	GND	-	-	GND	-
C10	GND	-	-	GND	-
G10	GND	-	-	GND	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
H10	GND	-	-	GND	-
J10	GND	-	-	GND	-
K10	GND	-	-	GND	-
L10	GND	-	-	GND	-
M10	GND	-	-	GND	-
N10	GND	-	-	GND	-
P10	GND	-	-	GND	-
R10	GND	-	-	GND	-
A9	GND	-	-	GND	-
B9	GND	-	-	GND	-
C9	GND	-	-	GND	-
G9	GND	-	-	GND	-
H9	GND	-	-	GND	-
J9	GND	-	-	GND	-
K9	GND	-	-	GND	-
L9	GND	-	-	GND	-
M9	GND	-	-	GND	-
N9	GND	-	-	GND	-
P9	GND	-	-	GND	-
R9	GND	-	-	GND	-
B8	GND	-	-	GND	-
C8	GND	-	-	GND	-
G8	GND	-	-	GND	-
H8	GND	-	-	GND	-
J8	GND	-	-	GND	-
K8	GND	-	-	GND	-
L8	GND	-	-	GND	-
M8	GND	-	-	GND	-
N8	GND	-	-	GND	-
P8	GND	-	-	GND	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
R8	GND	-	-	GND	-
A7	GND	-	-	GND	-
B7	GND	-	-	GND	-
C7	GND	-	-	GND	-
R7	GND	-	-	GND	-
H7	GND	-	-	GND	-
J7	GND	-	-	GND	-
K7	GND	-	-	GND	-
L7	GND	-	-	GND	-
M7	GND	-	-	GND	-
N7	GND	-	-	GND	-
P7	GND	-	-	GND	-
A6	GND	-	-	GND	-
B6	GND	-	-	GND	-
C6	GND	-	-	GND	-
Y6	GND	-	-	GND	-
B5	GND	-	-	GND	-
C5	GND	-	-	GND	-
A4	GND	-	-	GND	-
B4	GND	-	-	GND	-
T4	GND	-	-	GND	-
A3	GND	-	-	GND	-
B3	GND	-	-	GND	-
T3	GND	-	-	GND	-
L3	GND	-	-	GND	-
AA3	GND	-	-	GND	-
J2	GND	-	-	GND	-
L2	GND	-	-	GND	-
C1	GND	-	-	GND	-
J1	GND	-	-	GND	-

Pin	Pin Name		Pad	Description	Voltage (V)
	Normal	MUX			
W1	GND	-	-	GND	-

NOTE

- **P** indicates power pins; **PI** indicates input power pins; **PO** indicates output power pins; **I** indicates pins for signal input; **O** indicates pins for signal output; **I/O** indicates pins bidirectional.
- The **Reserved** pins are internally connected to the module. Therefore, these pins should not be used, otherwise they may cause problems. Please contact with us for more details about this information.

3.3 Power Interface

3.3.1 Overview

The power supply part of the module contains:

- VBAT and VBAT_RF pins for the power supply input
- VCC_EXT1 pin for external power output
- VREG_USIM0 pin for USIM0 card power output
- VREG_SD pin for SDIO power output

Table 3-2 Definitions of the pins on the power supply interface

Pin No.	Pin Name	Pad	Description	Comment
M1, M2,	VBAT	PI	Power supply input. The rising time of VBAT must be greater than 100 µs.	Input power is 3.8–4.2 V. The typical voltage is 4.0 V. Those power pins are used for PMIC.
K1, L1	VBAT_RF	PI	Power supply input. The rising time of VBAT must be greater than 100 µs.	Input power is 3.8–4.2 V. The typical voltage is 4.0 V. Those power pins are used for RFIC.
L21	VCC_EXT1	PO	Pin for external power output	Module output power is 1.8 V. And the current is less than 10 mA. It is on when the module enters the sleep mode.
M21	VREG_USIM0	PO	Power supply for USIM card	Module output power of USIM0
R3	VREG_SD	PO	SDIO power supply	Module output power for SDIO
Include 155 pins	GND	-	Thermal Ground Pad	-

3.3.2 Input Power Supply Interface

Input power supply interfaces are VBAT and VBAT_RF.

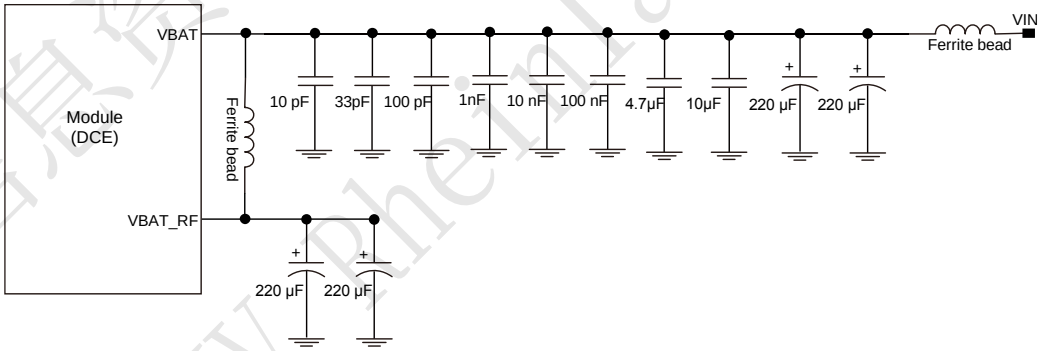
When the module works normally, power is supplied through the VBAT and VBAT_RF pins and the voltage ranges from 3.8 V to 4.2 V (typical value is 4.0 V).

When the module works at GSM mode and transmits signals at the maximum power, the transient peak current may reach 2.75 A due to the differences in actual network environments. In this case, the input power voltage will drop. In order to guarantee good wireless performance, please make sure that the voltage does not drop below 3.8 V in any case. Otherwise, exceptions such as restart of the module may occur.

A LDO (Low Dropout Regulator) or switch power with current output of more than 3 A is recommended for external power supply. Furthermore, four 220 µF or above energy storage capacitors are connected in parallel at the power interface of the module. In addition, to reduce the impact of channel impedance on voltage drop, it is recommended to try to shorten the power supply circuit of the VBAT interface.

Figure 3-3 shows the recommended power circuit.

Figure 3-3 Recommended power circuit



When the system power restarts, a discharge circuit is recommended to make sure the power voltage drops below 1.2 V for 100 ms at least. If Power_ON_OFF is asserted when the VBAT is between 1.2 V to 3.8 V, the module may enter an unexpected status.

Figure 3-4 Power supply time sequence for power cycling

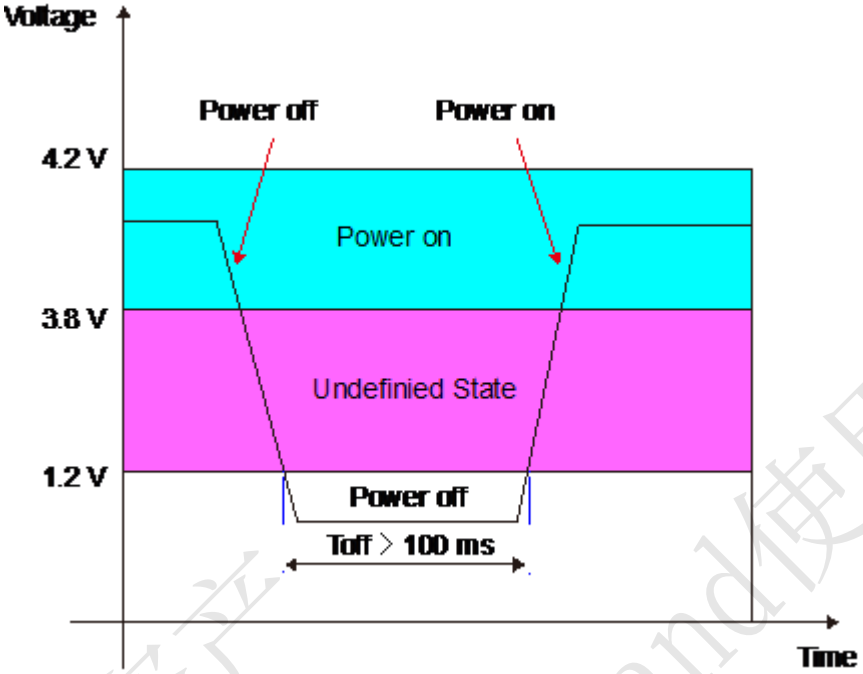


Table 3-3 Parameters description

Parameter	Remarks	Time (Min.)	Unit
T_{off}	Power off time	100	ms

NOTE
The rising time of input power should be 100 µs at least.

3.3.3 Output Power Supply Interface

Output power supply interfaces are VCC_EXT1, VREG_USIM0 and VREG_SD.

Table 3-4 Output power supply interface signals

Pin Name	Typ. (V)	Typ. (mA)
VCC_EXT1	1.8	10
VREG_USIM0	1.8/3.0	50
VREG_SD	2.85	50

Through the VCC_EXT1, the module can supply 1.8 V power externally with an output current of 10 mA (typical value) for external level conversion or other applications. If the module is in sleep mode, the output power supply interface is in the low power

consumption state (< 500 μA). If the module is in power down mode, the output power supply is in the disabled state.

Through the VREG_USIM0, the module can supply 1.8 V or 3.0 V power for the USIM card.

The VREG_SD pin can supply a 2.85 V voltage, and the typical output current of VREG_SD is 50 mA.

3.4 Signal Control Interface

3.4.1 Overview

The signal control part of the interface in the module consists of the following:

- Power_ON_OFF pin
- PS_HOLD pin
- RSTIN_N pin
- RSTOUT_N pin
- WAKEUP_SLEEP_IN pin
- WAKEUP_SLEEP_OUT pin
- SLEEP_STATUS pin

Table 3-5 Definitions of the pins on the signal control interface

Pin	Pin Name	Pad	Description	Typ. (V)
N1	Power_ON_OFF	I	Power on and power off signal.	1.8
V19	PS_HOLD	O	Indicates whether the PMIC finishes the power procedure or not. It is recommended to be connected to a test point.	1.8
W18	RSTIN_N	I	Reset input signal.	1.8
V18	RSTOUT_N	O	Reset output signal, indicating the reset of PMIC. It is recommended to be connected to a test point.	1.8
V15	WAKEUP_SLEEP_IN	I	The host sets the module into sleep or wakes up the module. H: sleep mode is disabled. L: sleep mode is enabled (default value)	1.8
G19	WAKEUP_SLEEP_OUT	O	Module wakes up the host. H: wake up the host. L: do not wake up the host (default value)	1.8
H4	SLEEP_STATUS	O	Indicates sleep status of module. H: the module is in wakeup mode. L: the module is in sleep mode.	1.8

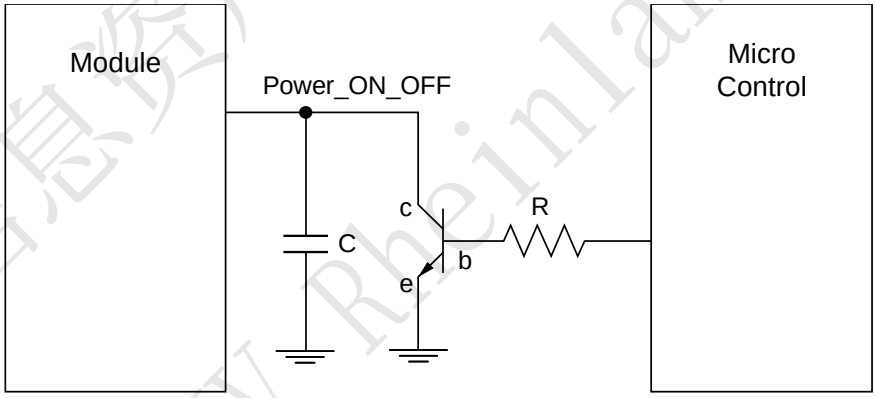
3.4.2 Power_ON_OFF Pin

The module can be powered on/off by the Power_ON_OFF pin.

Table 3-6 Two states of Power_ON_OFF

Item	Pin state	Description
1	Active-Low (when the module is in power-off state.)	The module is powered on. Power_ON_OFF pin should be pulled down for 1s at least.
2	Active-Low (when the module is in power-on state.)	The module is powered off. Power_ON_OFF pin should be pulled down for 4–6s.

Figure 3-5 Recommended connections of the Power_ON_OFF pin



Power_ON_OFF Time Sequence

After supply power has been applied and is stable, the Power_ON_OFF signal is pulled down, and then the module will boot up.

During power on timing, please make sure the VBAT is stable, see Figure 3-6

Figure 3-6 Recommended power on timing sequence

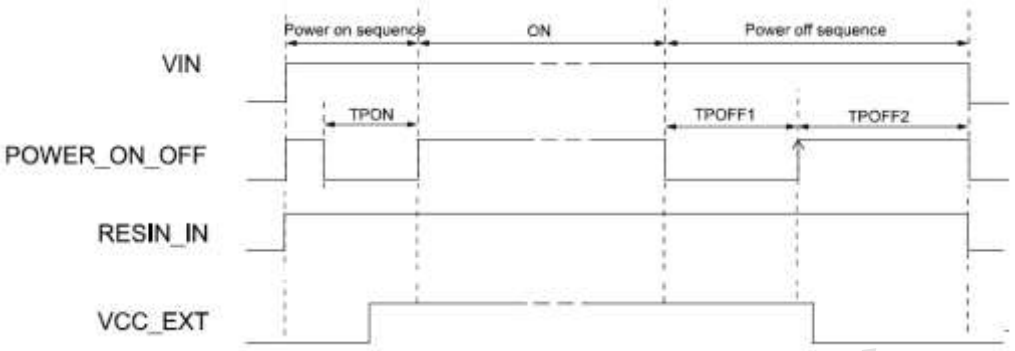


Table 3-7 Parameters description

Parameter	Comments	Time (Nominal values)	Unit
T_{PON}	Power_ON_OFF turn on time	>1.0	s
T_{POFF1}	Power_ON_OFF turn off time	4.0–6.0	s
T_{POFF2}	Power supply remaining time after giving the Power_ON_OFF signal to the module	>5.0	s

NOTE

If the power supply for the module would be switched off, please ensure it occurs at least 5s after giving the POWER_ON_OFF signal to the module.

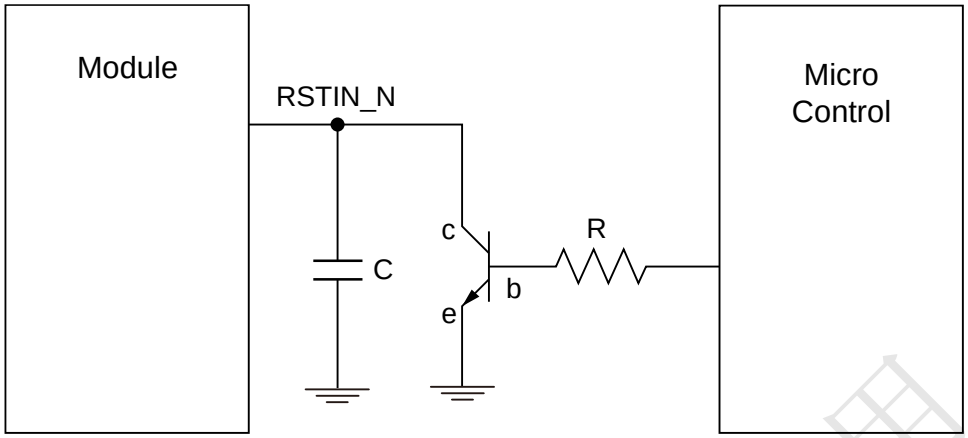
3.4.3 PS_HOLD Pin

The PS_HOLD pin is an indicated PMIC power-on signal. Please connect this pin to a test point.

3.4.4 RSTIN_N Signal

The RSTIN_N pin is used to reset the module's system. When the software stops responding, the RSTIN_N pin can be pulled down to reset the hardware.

Figure 3-7 Recommended connections of the RSTIN_N pin

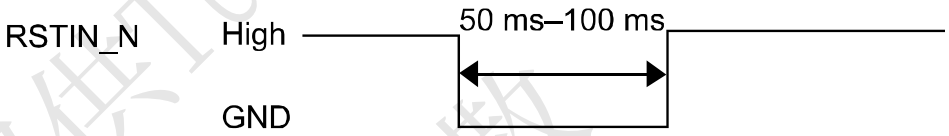


CAUTION

As the RSTIN_N and Power_ON_OFF pins are relatively sensitive, it is recommended to place a 10 nF–0.1 µF capacitor near the RSTIN_N and Power_ON_OFF pins of the interface for filtering. In addition, when you design a circuit on the PCB of the interface board, it is recommended that the circuit length not exceed 20 mm and that the circuit be kept at a distance of 2.54 mm (100 mil) at least from the PCB edge. Furthermore, it is recommended to wrap the area adjacent to the signal wire with a ground wire. Otherwise, the module may be reset due to interference.

The module supports hardware reset function. If the software of the module stops responding, you can reset the hardware through the RSTIN_N pin as shown in Figure 3-8 .When a low-level pulse is supplied through the RSTIN_N pin, the hardware will be reset. After the hardware is reset, the software starts powering on the module and reports relevant information according to the actual settings.

Figure 3-8 Reset pulse timing



3.4.5 RSTOUT_N Pin

The RSTOUT_N pin is a reset signal. It is used to indicate that the PMIC is under reset. It is recommended to connect this pin to a test point.

3.4.6 WAKEUP_SLEEP_IN Pin

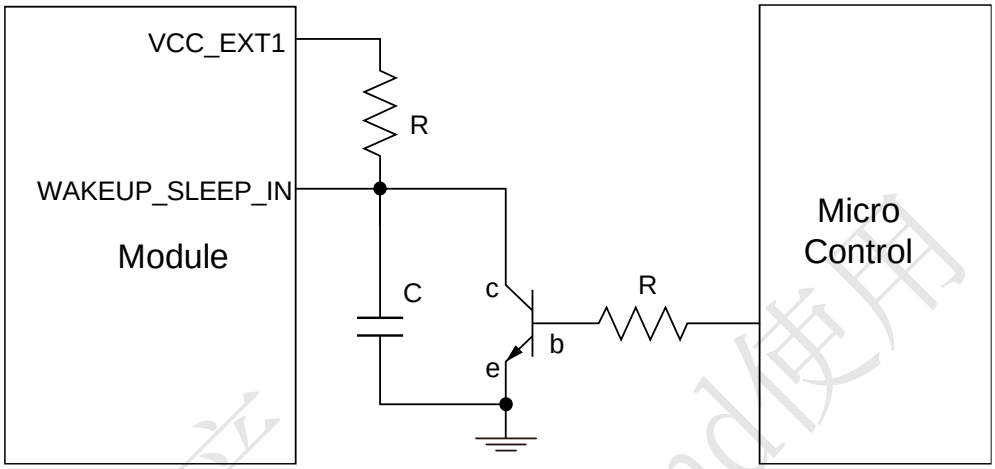
WAKEUP_SLEEP_IN pin is the authorization signal of the module entering sleep mode.

- When WAKEUP_SLEEP_IN pin is in high level, the module cannot enter sleep mode.

- When WAKEUP_SLEEP_IN pin is in low level, the module can enter sleep mode. (default)

If this pin is not connected, it will keep in low level by default.

Figure 3-9 Recommended connections of the WAKEUP_SLEEP_IN pin



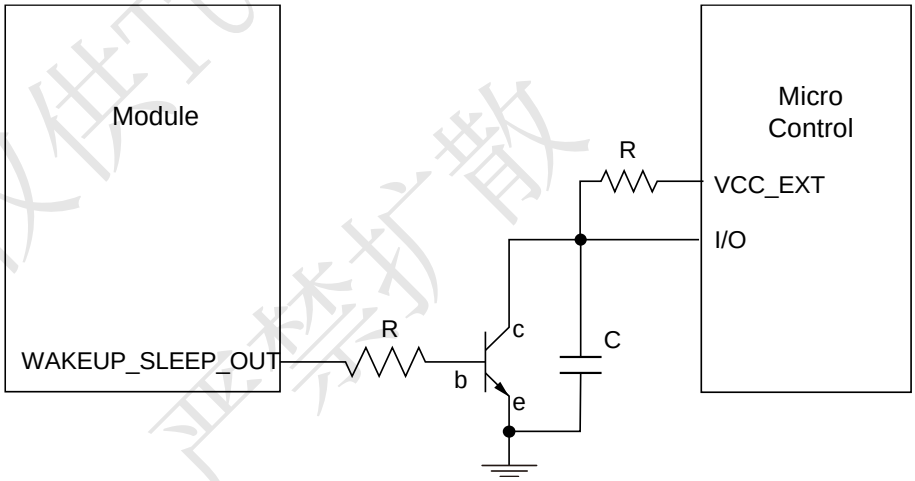
NOTE
The pull-up resistor should not be greater than 22 kΩ.

3.4.7 WAKEUP_SLEEP_OUT Pin

The WAKEUP_SLEEP_OUT pin is used to wake up the external devices.

- When WAKEUP_SLEEP_OUT pin is in high level, the module wakes up the host.
- When WAKEUP_SLEEP_OUT pin is in low level, the module cannot wake up the host. (default)

Figure 3-10 Recommended connections of the WAKEUP_SLEEP_OUT pin

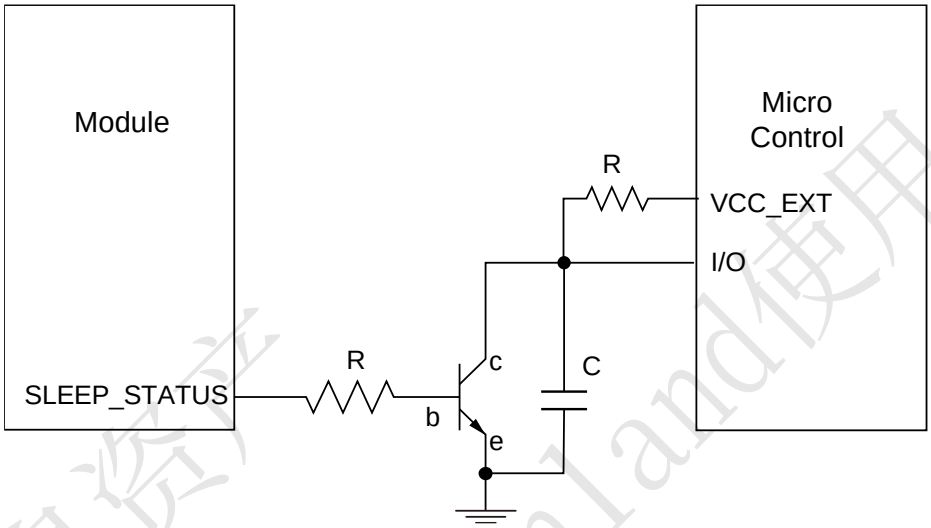


3.4.8 SLEEP_STATUS Pin

The SLEEP_STATUS pin is used to indicate the sleep status of the module.

- When SLEEP_STATUS pin is in high level, the module enters wakeup mode.
- When SLEEP_STATUS pin is in low level, the module enters sleep mode.

Figure 3-11 Recommended connections of the SLEEP_STATUS pin



3.5 UART Interface

The module provides three 4-wire UART interfaces and one 2-wire UART interface. As the UART interface supports signal control through standard modem handshake, Software commands are entered and serial communication is performed through the UART interface.

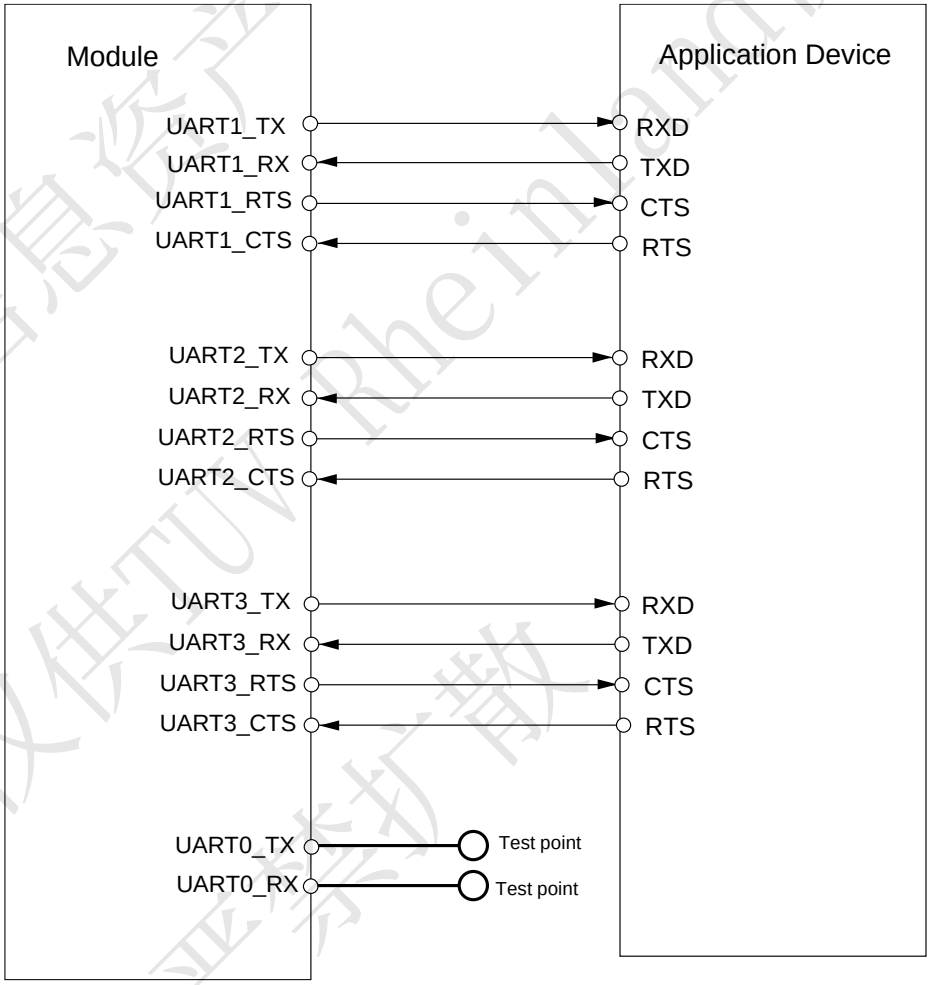
The 2-wire UART is for debugging only. Customers should layout two test points for them in case of system troubleshooting and analysis.

Table 3-8 UART interface signals

Pin No.	Pin Name	Pad Type	Description	Typ. (V)
H21	UART0_TX	O	UART0 transmit data output for debug	1.8
H20	UART0_RX	I	UART0 receive data input for debug	1.8
F21	UART1_TX	O	UART1 transmit data output	1.8
G20	UART1_RX	I	UART1 receive data input	1.8
G21	UART1_RTS	O	UART1 request to send	1.8
F20	UART1_CTS	I	UART1 clear to send	1.8
D20	UART2_TX	O	UART2 transmit data output	1.8

Pin No.	Pin Name	Pad Type	Description	Typ. (V)
E20	UART2_RX	I	UART2 receive data input	1.8
D21	UART2_RTS	O	UART2 request to send	1.8
E21	UART2_CTS	I	UART2 clear to send	1.8
H1	UART3_TX	O	UART3 transmit data output	1.8
G1	UART3_RX	I	UART3 receive data input	1.8
H2	UART3_RTS	O	UART3 request to send	1.8
G2	UART3_CTS	I	UART3 clear to send	1.8

Figure 3-12 Recommended connection of the UART interface in the module with the host



NOTE

- The UART cannot wake up the module from the sleep status, but you can wake it up by pulling up the WAKEUP_SLEEP_IN signal for 1s instead.
- The level of RS-232 transceivers must match that of the module.
- It is recommended that customers set the pins related to UART0 interface as test points on the user interface board for debugging.

3.6 USB Interface

The module is compliant with USB 2.0. It is recommended to connect the USB20_DP and USB20_DM to test points.

Table 3-9 Definition of the USB interface

Pin No.	Pin Name	Pad Type	Description	Typ.(v)
W20	Reserved	-	Reserved for USB ID pin	-
AA18	USB20_DP	I/O	USB2.0 differential data – plus	-
Y19	USB20_DM	I/O	USB2.0 differential data – minus	-
AA17	Reserved	-	Reserved for USB30_TXp	-
Y17	Reserved	-	Reserved for USB30_TXn	-
AA15	Reserved	-	Reserved for USB30_RXp	-
Y15	Reserved	-	Reserved for USB30_RXn	-
W19	USB_VBUS	PI	USB_VBUS detection voltage	5

3.7 USIM Card Interface

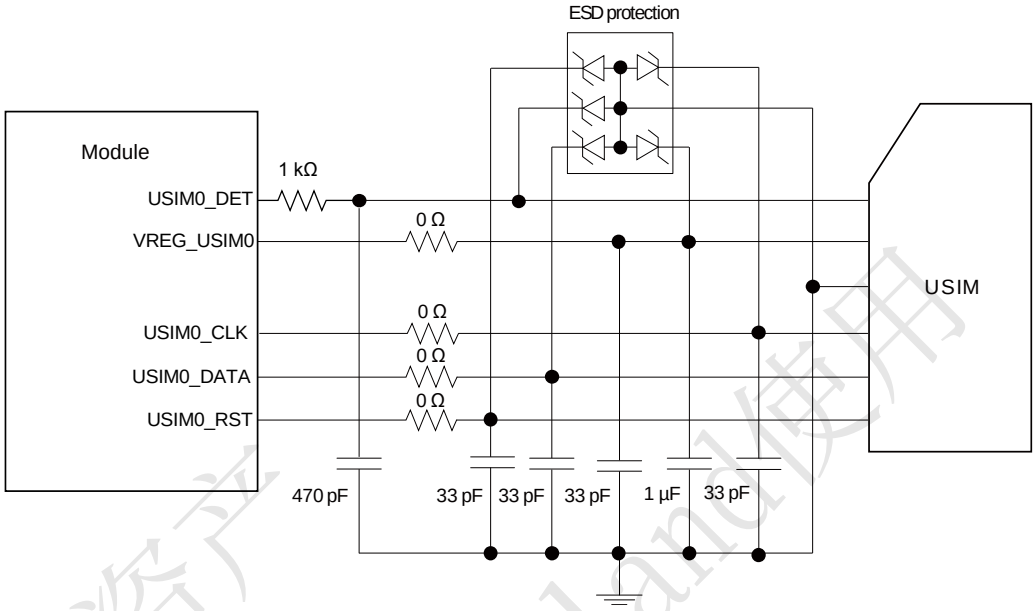
The module provides a USIM card interface complying with the ISO 7816-3 standard and supports both Class B and Class C USIM cards.

Table 3-10 USIM card interface signals

Pin No.	Pin Name	Pad Type	Description	Typ. (V)
N21	USIM0_RST	O	USIM card reset	1.8/3.0
M20	USIM0_DATA	I/O	USIM card data	1.8/3.0
N20	USIM0_CLK	O	USIM card clock	1.8/3.0
M21	VREG_USIM0	PO	Power supply for USIM card.	1.8/3.0
W17	USIM0_DET	I	USIM detection	1.8

As the module is not equipped with a USIM socket, you need to place a USIM socket on the user interface board. Figure 3-13 shows the circuit of the USIM card interface.

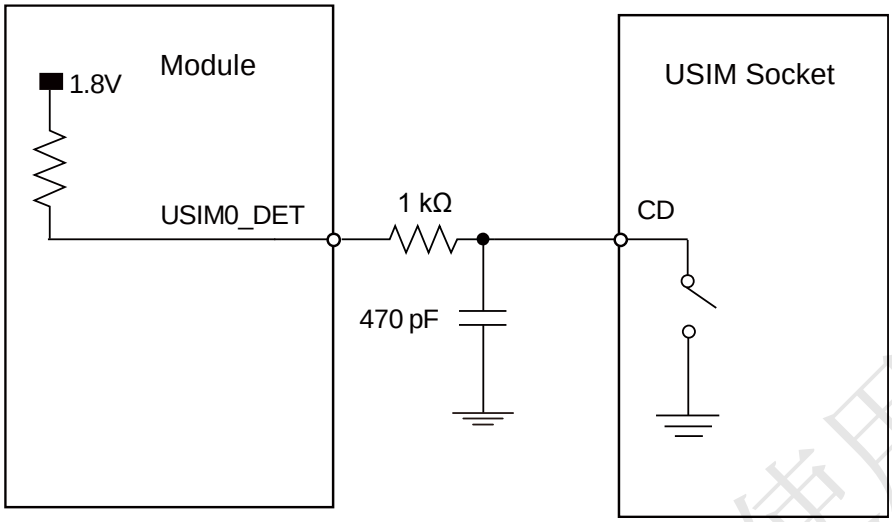
Figure 3-13 Recommended circuit of the USIM card interface



CAUTION

- The ESD protection component should choose low capacitance (< 10 pF).
- To meet the requirements of 3GPP TS 51.010-1 protocols and EMC (Electromagnetic Compatibility) authentication, the USIM card socket should be placed near the LGA interface (it is recommended that the PCB circuit connecting the LGA interface with the USIM card socket not exceed 100 mm), because a long circuit may lead to wave distortion, thus signal quality is affected.
- The area adjacent to the USIM0_CLK and USIM0_DATA signal wires is recommended to wrap with a ground wire. The GND pin of the USIM socket and the USIM card must be well connected to the module power GND pin.
- A resistor is placed on the USIM0_CLK and USIM0_DATA pins in series for testing USIM card.
- A 33 pF capacitor and 1 µF capacitor are placed between the VREG_USIM0 and GND pins in parallel (If VREG_USIM0 circuit is too long, a larger capacitance such as 4.7 µF can be employed). Three 33 pF capacitors are placed between the USIM0_DATA/USIM0_RST/USIM0_CLK and GND pins in parallel to filter interference from RF signals.
- It is recommended to take ESD (Electrostatic Discharge) protection measures near the USIM card socket. The TVS (Transient Voltage Suppressor) diode with Vrwm of 5 V and junction capacitance less than 10 pF must be placed as close as possible to the USIM socket, and the GND pin of the ESD protection component must be well connected to the module power GND pin.

Figure 3-14 Recommended connections of the USIM0_DET pin



CD is a pin that detects whether USIM card is in the USIM socket or not.

- If the USIM card is present, USIM0_DET pin keeps high, and the CD is open.
- If the USIM card is absent, USIM0_DET pin keeps low, and the CD is connected to ground.
- If the hot swapping function of the SIM card is not used, the pin shall be floated.

3.8 Audio Interface

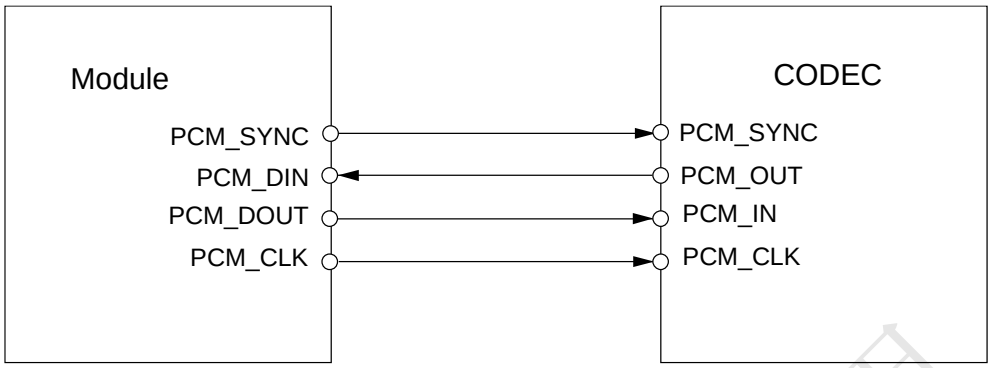
The module provides one PCM (Pulse Code Modulation) digital audio interface. Table 3-11 lists the signals on the digital audio interface.

Table 3-11 Signals on the digital audio interface

Pin No.	Pin Name	Pad Type	Description	Typ. (V)	Comments
D19	PCM_SYNC	O	PCM interface sync	1.8	The pin is output when the module is used as PCM master.
C19	PCM_DIN	I	PCM interface data in	1.8	-
C20	PCM_DOUT	O	PCM interface data out	1.8	-
E19	PCM_CLK	O	PCM interface clock	1.8	The pin is output when the module is used as PCM master.

The module PCM interface enables communication with an external codec to support linear format.

Figure 3-15 Recommended circuit diagram of the interface of the PCM (The module is used as PCM master)



NOTE
The signal level of codec must match that of the module.

3.9 GPIO Interface

The module provides GPIO pins for customers to use controlling signals which work at 1.8 V CMOS logic level. Some GPIOs are multiplex with other function pins.

All GPIOs can support interrupt function and input or output function when the module is in active mode. How to trigger the interruption is configured by software.

- When the module enters sleep mode, only M4/U19/U18/W15 can support interrupt function.
- When the module enters sleep mode, only M4/U19/U18/W15 can support high output drive ability. Other GPIOs drive ability is very small and only can drive a transistor.

Table 3-12 Signals on the GPIO interface

Pin	Pin Name		Description	Typ.(V)	Interrupt during sleep mode
	Normal	MUX			
J4	GPIO1	-	General Purpose I/O pin	1.8	-
G4	GPIO2	-	General Purpose I/O pin	1.8	-
V16	GPIO3	-	General Purpose I/O pin	1.8	-
V17	GPIO4	-	General Purpose I/O pin	1.8	-
M4	GPIO5	-	General Purpose I/O pin	1.8	YES
W16	GPIO6	-	General Purpose I/O pin	1.8	-
J18	GPIO7	-	General Purpose I/O pin	1.8	-

Pin	Pin Name		Description	Typ.(V)	Interrupt during sleep mode
	Normal	MUX			
H3	PCIE1_CLKREQ_N	GPIO8	PCIe1 clock request. If used in PCIe, Open drain requires external 100 k PU or General Purpose I/O pin	1.8	-
U19	PCIE1_WAKE_N	GPIO9	PCIe1 client wake up or General Purpose I/O pin	1.8	YES
G3	PCIE1_PERST_N	GPIO10	PCIe1 client reset or General Purpose I/O pin	1.8	-
U2	MII_TX_ER	GPIO11	Transmit error or General Purpose I/O pin	1.8	-
V2	MII_RMII_RX_ER	GPIO12	Receive error or General Purpose I/O pin	1.8	-
D16	GPIO13	-	General Purpose I/O pin	1.8	-
D17	GPIO14	-	General Purpose I/O pin	1.8	-
M18	GPIO15	-	General Purpose I/O pin	1.8	-
D15	GPIO33	-	General Purpose I/O pin	1.8	-
F3	PCIE0_CLKREQ_N	GPIO34	PCIe0 clock request. Open drain requires external 100 k PU or General Purpose I/O pin	1.8	-
U18	PCIE0_WAKE_N	GPIO16	PCIe0 client wake up or General Purpose I/O pin	1.8	YES
F4	PCIE0_PERST_N	GPIO17	PCIe0 client reset or General Purpose I/O pin	1.8	-
AA9	RGMII_TX_CLK/MII_TX_CLK	GPIO18	RGMII/MII transmit clock or General Purpose I/O pin	1.8	-
AA6	RGMII_RX_CLK/MII_RX_CLK	GPIO19	RGMII/MII receive clock or General Purpose I/O pin	1.8	-
Y5	RGMII_RXDV/MII_RXDV	GPIO20	RGMII/MII received data valid or General Purpose I/O pin	1.8	-
Y3	RGMII_RXD0/MII_RXD0	GPIO21	RGMII/MII received data 0 or General Purpose I/O pin	1.8	-
AA4	RGMII_RXD1/MII_RXD1	GPIO22	RGMII/MII received data 1 or General Purpose I/O pin	1.8	-
Y4	RGMII_RXD2/MII_RXD2	GPIO23	RGMII/MII received data 2 or General Purpose I/O pin	1.8	-

Pin	Pin Name		Description	Typ.(V)	Interrupt during sleep mode
	Normal	MUX			
AA5	RGMII_RXD3/MII_RXD3	GPIO24	RGMII/MII received data 3 or General Purpose I/O pin	1.8	-
Y9	RGMII_TXEN/MII_TXEN	GPIO25	RGMII/MII transmit enable or General Purpose I/O pin	1.8	-
Y7	RGMII_TXD0/MII_TXD0	GPIO26	RGMII/MII transmit data 0 or General Purpose I/O pin	1.8	-
AA7	RGMII_TXD1/MII_TXD1	GPIO27	RGMII/MII transmit data 1 or General Purpose I/O pin	1.8	-
Y8	RGMII_TXD2/MII_TXD2	GPIO28	RGMII/MII transmit data 2 or General Purpose I/O pin	1.8	-
AA8	RGMII_TXD3/MII_TXD3	GPIO29	RGMII/MII transmit data 3 or General Purpose I/O pin	1.8	-
V1	RGMII_MDC/MII_MDC	GPIO30	Management data clock reference or General Purpose I/O pin	1.8	-
W2	RGMII_MDIO/MII_MDIO	GPIO31	Management data or General Purpose I/O pin	1.8	-
W15	RGMII_INT/MII_INT/GPIO	GPIO32	RGMII/MII interrupt signal or General Purpose I/O pin	1.8	YES

3.10 GPS PPS Interface

The module will output PPS (pulse per second) interface. This function is under development, in the hardware reversed. Please connect this pin to GPIO in module. The voltage is 2.85 V.

Table 3-13 Signals on the GPS PPS interface

PIN No.	Pin Name	Pad Type	Description	Typ. (V)
D14	GPS_PPS_OUT	O	Reversed pin for GPS_PPS_OUT. This pin outputs PPS (pulse per second) signal.	2.85

3.11 ADC Interface

The module provides four ADC interfaces.

Table 3-14 Signals on the ADC interface

PIN No.	Pin Name	Pad Type	Description	Max voltage. (V)
P1	ADC1	I	Conversion interface for analog signals to digital signals	1.8
N2	ADC2	I	Conversion interface for analog signals to digital signals	1.8
R1	ADC3	I	Conversion interface for analog signals to digital signals	1.8
P2	ADC4	I	Conversion interface for analog signals to digital signals	1.8

Table 3-15 Parameter of ADC interface

Parameter	Value
Full scale voltage	1.8 V
Input voltage	0.05–1.75 V
INL	±4LSB
DNL	±2LSB
1LSB	0.00044 V
Offset	±20LSB
Gain error	1% of full scale voltage (max)

3.12 JTAG Interface

The module provides JTAG interface. Table 3-16 shows the signals on the JTAG interface. It is recommended to reserve 5 pins as test points on the user interface board for tracing and debugging.

Table 3-16 JTAG interface signals

Pin No.	Pin Name	Pad Type	Description	Typ. (V)
J19	Reserved	-	Reserved for JTAG	-
L20	JTAG_TCK	I	JTAG clock input	1.8

Pin No.	Pin Name	Pad Type	Description	Typ. (V)
K20	JTAG_TDI	I	JTAG test data input	1.8
L19	JTAG_TDO	O	JTAG test data output	1.8
K19	JTAG_TMS	I	JTAG test mode select	1.8
K21	JTAG_TRST_N	I	JTAG reset	1.8

3.13 I2C Interface

The module provides I2C interface. The I2C interface is open drain type and requires external PU to 1.8 V.

Table 3-17 I2C interface signals

Pin No.	Pin Name	Pad Type	Description	Typ. (V)
G18	I2C0_SDA	I/O	I2C data	1.8
H18	I2C0_SCL	O	I2C clock	1.8

3.14 SDIO Interface

The module provides SDIO interface, and the voltage of the SDIO can be configured by software.

Table 3-18 SDIO interface signals

Pin No.	Pin Name	Pad Type	Description	Typ. (V)
R3	VREG_SD	PO	SDIO power supply	2.85
N4	SDIO_CLK	O	Secure digital clock; impedance match: 33 Ω damping resistor.	1.8/2.85
M3	SDIO_CMD	I/O	Secure digital command	1.8/2.85
P3	SDIO_DATA0	I/O	Secure digital data bit 0	1.8/2.85
R4	SDIO_DATA1	I/O	Secure digital data bit 1	1.8/2.85
P4	SDIO_DATA2	I/O	Secure digital data bit 2	1.8/2.85
N3	SDIO_DATA3	I/O	Secure digital data bit 3	1.8/2.85

3.15 PCIe Interface

The module provides two PCIe interfaces separately.

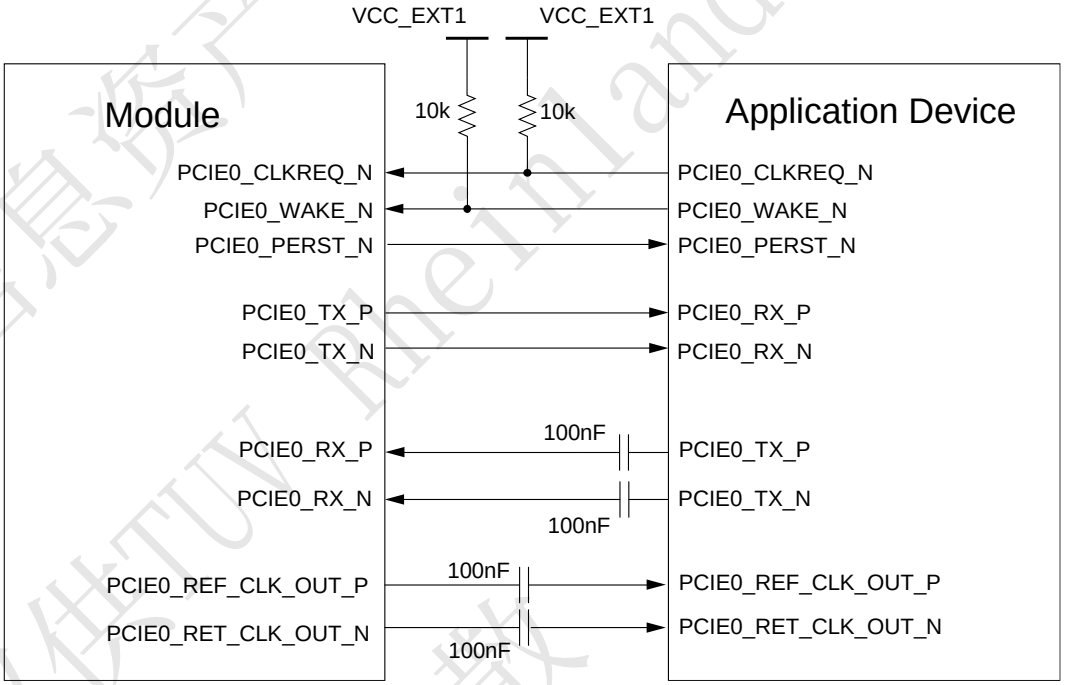
Table 3-19 PCIe interface signals

Pin	Pin Name	Pad Type	Description	Typ. (V)
F3	PCIE0_CLKREQ_N	I	PCIe0 clock request. (Open drain requires external 10 k PU, active low)	1.8
U18	PCIE0_WAKE_N	I	PCIe0 client wake up. (Open drain requires external 10 k PU, active low)	1.8
F4	PCIE0_PERST_N	O	PCIe0 client reset (active-low)	1.8
AA14	PCIE0_TX_P	O	PCIe0 transmit – plus	-
Y14	PCIE0_TX_N	O	PCIe0 transmit – minus	-
AA12	PCIE0_RX_P	I	PCIe0 receive – plus	-
Y12	PCIE0_RX_N	I	PCIe0 receive – minus	-
AA10	PCIE0_REF_CLK_P	O	PCIe0 differential reference clock: plus	-
Y10	PCIE0_REF_CLK_N	O	PCIe0 differential reference clock: minus	-
H3	PCIE1_CLKREQ_N	I	PCIe1 clock request. (Open drain requires external 10 k PU, active low)	1.8
U19	PCIE1_WAKE_N	I	PCIe1 client wake up. (Open drain requires external 10 k PU, active low)	1.8
G3	PCIE1_PERST_N	O	PCIe1 client reset (active-low)	1.8
T21	PCIE1_TX_P	O	PCIe1 transmit – plus	-
T20	PCIE1_TX_N	O	PCIe1 transmit – minus	-
P21	PCIE1_RX_P	I	PCIe1 receive – plus	-

Pin	Pin Name	Pad Type	Description	Typ. (V)
P20	PCIE1_RX_N	I	PCIe1 receive – minus	-
V21	PCIE1_REF_CLK_P	O	PCIe1 differential reference clock - plus	-
V20	PCIE1_REF_CLK_N	O	PCIe1 differential reference clock - minus	-

It is recommended that the differential clock output signals of PCIe interface should be connected as Figure 3-16 . Two 100 nF capacitors inner module are separately placed on the TX signal in series. In addition, two 100 nF capacitors placed on the differential clock output signals in series are used for DC blocking.

Figure 3-16 Recommended circuit of the PCIe interface



3.16 RGMII/MII Interface

The module provides RGMII/MII interfaces as below.

Pin No.	RGMII		MII	
	Name	IO	Name	IO
AA9	RGMII_TX_CLK	O	MII_TX_CLK	I

Pin No.	RGMII		MII	
	Name	IO	Name	IO
AA6	RGMII_RX_CLK	I	MII_RX_CLK	I
Y5	RGMII_RXDV	I	MII_RXDV	I
Y3	RGMII_RXD0	I	MII_RXD0	I
AA4	RGMII_RXD1	I	MII_RXD1	I
Y4	RGMII_RXD2	I	MII_RXD2	I
AA5	RGMII_RXD3	I	MII_RXD3	I
Y9	RGMII_TXEN	O	MII_TXEN	O
Y7	RGMII_TXD0	O	MII_TXD0	O
AA7	RGMII_TXD1	O	MII_TXD1	O
Y8	RGMII_TXD2	O	MII_TXD2	O
AA8	RGMII_TXD3	O	MII_TXD3	O
V1	RGMII_MDC	O	MDC	O
W2	RGMII_MDIO	I/O	MDIO	I/O
U2	-	-	MII_TX_ER	O
V2	-	-	MII_RMII_RX_ER	I
W15	RGMII_INT	I	MII_INT	I

Table 3-20 lists RGMII interface signals.

Table 3-20 RGMII interface signals

Pin No.	Pin Name	IO	Description	Typ. (V)
AA9	RGMII_TX_CLK	O	RGMII transmit clock. Adding a 33 Ω damping resistor	1.8
AA6	RGMII_RX_CLK	I	RGMII receive clock. Adding a 33 Ω damping resistor	1.8
Y5	RGMII_RXDV	I	RGMII receive data valid	1.8
Y3	RGMII_RXD0	I	RGMII received data 0	1.8
AA4	RGMII_RXD1	I	RGMII received data 1	1.8
Y4	RGMII_RXD2	I	RGMII received data 2	1.8
AA5	RGMII_RXD3	I	RGMII received data 3	1.8

Pin No.	Pin Name	IO	Description	Typ. (V)
Y9	RGMII_TXEN	O	RGMII transmit enable (active-high)	1.8
Y7	RGMII_TXD0	O	RGMII transmit data 0. Adding a 33 Ω damping resistor	1.8
AA7	RGMII_TXD1	O	RGMII transmit data 1. Adding a 33 Ω damping resistor	1.8
Y8	RGMII_TXD2	O	RGMII transmit data 2. Adding a 33 Ω damping resistor	1.8
AA8	RGMII_TXD3	O	RGMII transmit data 3. Adding a 33 Ω damping resistor	1.8
V1	RGMII_MDC	O	Management data clock reference	1.8
W2	RGMII_MDIO	I/O	Management data. Add a 4.7 kΩ resistor up to VCC_EXT1	1.8
W15	RGMII_INT	I	RGMII interrupt signal	1.8

Figure 3-17 is recommended circuit of the RGMII interface.

Figure 3-17 Recommended circuit of the RGMII interface

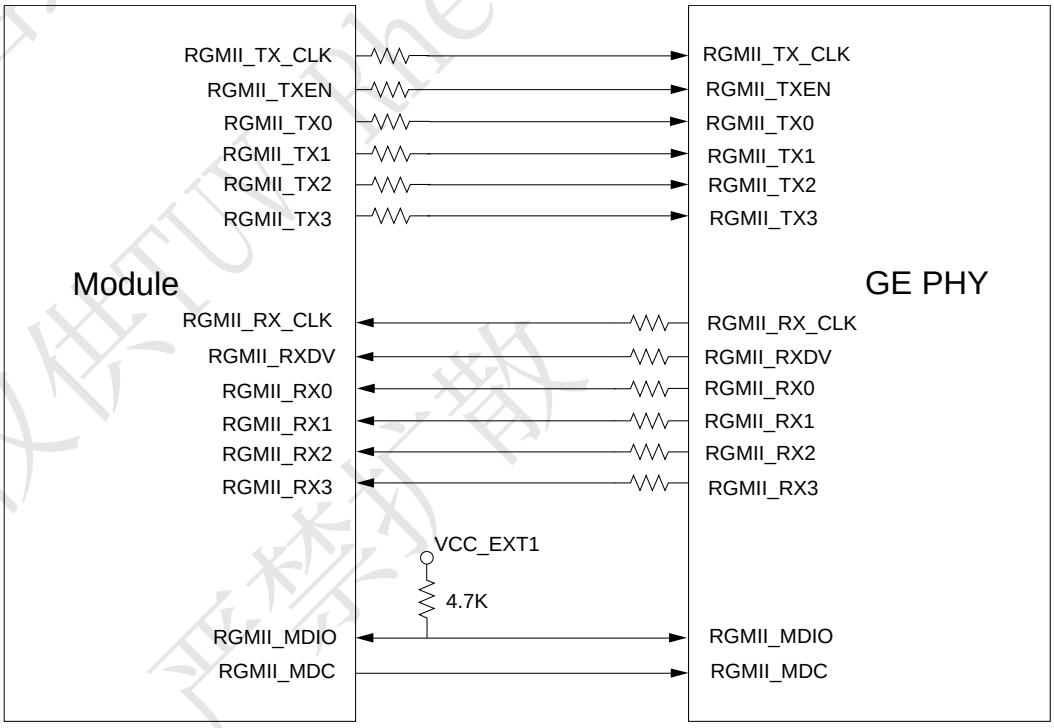


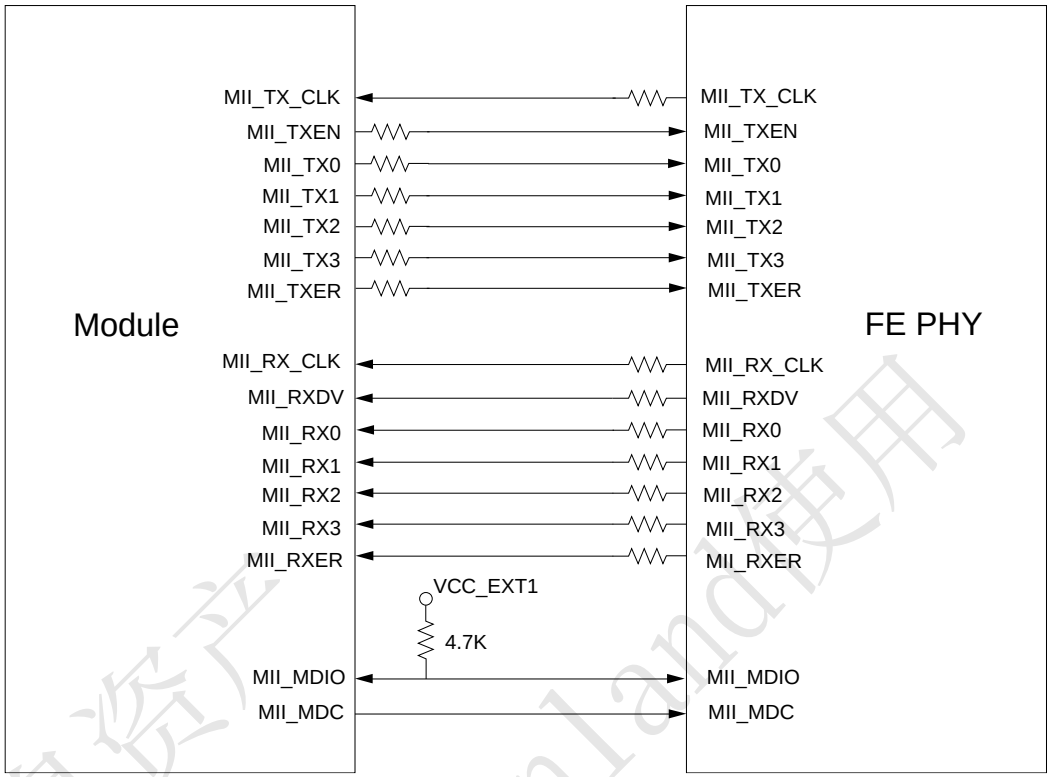
Table 3-21 lists MII interface signals.

Table 3-21 MII interface signals

Pin No.	Pin Name	IO	Description	Typ. (V)
AA9	MII_TX_CLK	I	MII transmit clock. Adding a 33 Ω damping resistor	1.8
AA6	MII_RX_CLK	I	MII receive clock. Adding a 33 Ω damping resistor	1.8
Y5	MII_RXDV	I	MII receive data valid	1.8
Y3	MII_RXD0	I	MII received data 0	1.8
AA4	MII_RXD1	I	MII received data 1	1.8
Y4	MII_RXD2	I	MII received data 2	1.8
AA5	MII_RXD3	I	MII received data 3	1.8
Y9	MII_TXEN	O	MII transmit enable(active-high)	1.8
Y7	MII_TXD0	O	MII transmit data 0. Adding a 33 Ω damping resistor	1.8
AA7	MII_TXD1	O	MII transmit data 1. Adding a 33 Ω damping resistor	1.8
Y8	MII_TXD2	O	MII transmit data 2. Adding a 33 Ω damping resistor	1.8
AA8	MII_TXD3	O	MII transmit data 3. Adding a 33 Ω damping resistor	1.8
V1	MII_MDC	O	Management data clock reference	1.8
W2	MII_MDIO	I/O	Management data. Adding a 4.7 kΩ resistor up to VCC_EXT1	1.8
U2	MII_TX_ER	O	Transmit Error. H: the TX data is error and not valid TX_ER does not work under 10Mbps.	1.8
V2	MII_RMII_RX_ER	I	Receive Error H: the RX data is error and not valid RX_ER does not work under 10Mbps.	1.8
W15	MII_INT	I	MII interrupt signal	1.8

Figure 3-18 is recommended circuit of the MII interface.

Figure 3-18 Recommended circuit of the MII interface



3.17 RF Antenna Interface

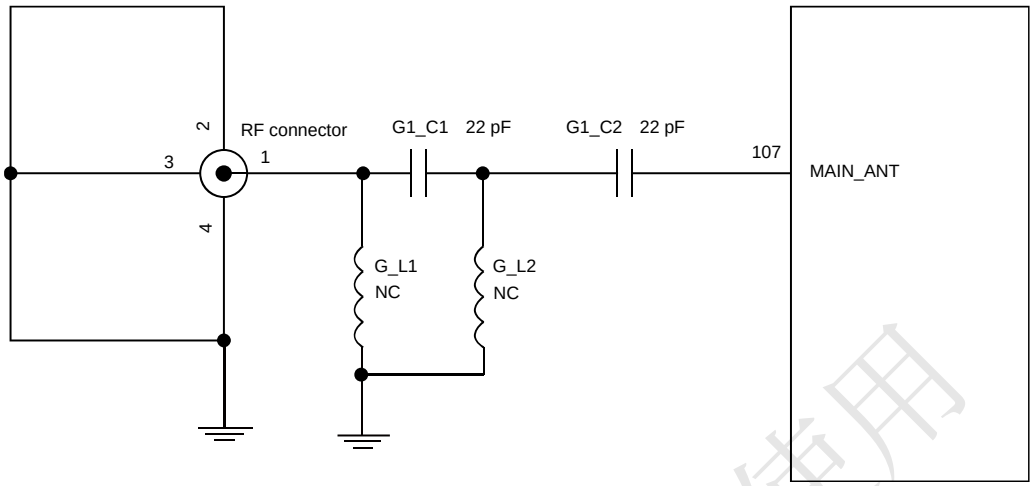
The module provides three antenna pads (MAIN_ANT, AUX_ANT and GPS_ANT) for connecting the external antennas.

Table 3-22 Definition of the antenna pads

Pin No.	Pin Name	Description
A5	MAIN_ANT	RF primary antenna pad
A14	AUX_ANT	RF diversity antenna pad
A17	GPS_ANT	RF GPS antenna pad

Route the antenna pad as close to antenna connector as possible. In addition, the impedance of RF signal traces must be 50 Ω.

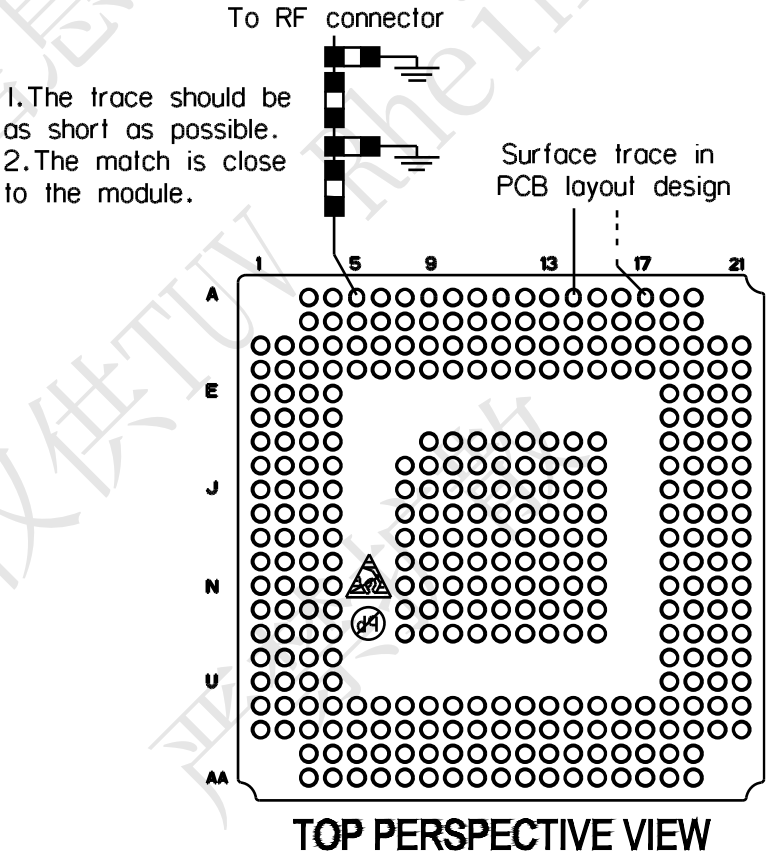
Figure 3-19 RF signal trace design about MAIN_ANT for reference (the same for AUX_ANT and GPS_ANT)



NOTE

To ensure good ILPC performance, the VSWR should be less than 1.2 from 1700 MHz to 2100 MHz.

Figure 3-20 RF signal layout design about MAIN_ANT for reference (the same for AUX_ANT and GPS_ANT)



For the PCB designed by the user, the impedance of all the RF signal tracks must be 50 Ω. Generally, the impedance depends on the medium factor, track width, and distance from the floor.

In order to reflect the rules of design, Figure 3-21 to Figure 3-24 indicate the complete structure of the microstrip and stripline with an impedance of 50 Ω as well as the reference design for stack.

Figure 3-21 Complete structure of the microstrip

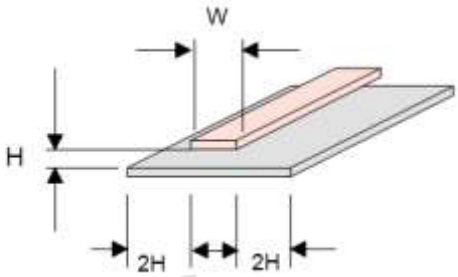


Figure 3-22 Complete structure of the stripline

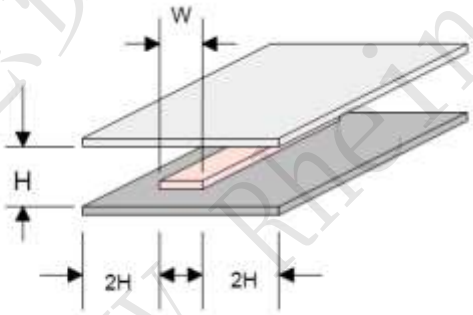


Figure 3-23 Pad for the RF interface

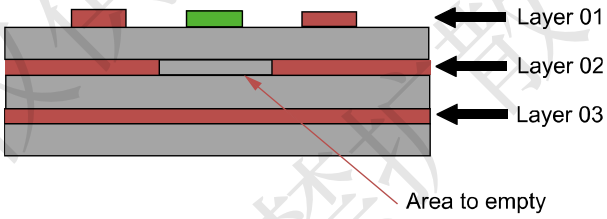
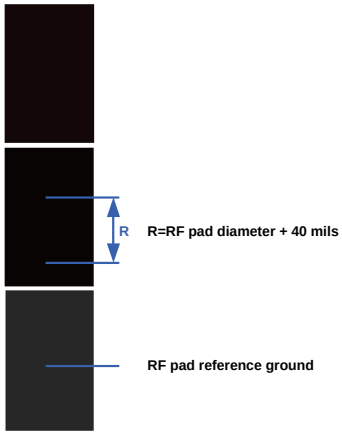


Figure 3-24 RF Pad design



Please use impedance simulation tool to calculate RF MAIN pad impedance. The RF MAIN pad diameter is 1mm. The RF MAIN pad impedance is calculated to be lower than 50 Ω by the impedance simulation tool. Since the target impedance is 50 Ω for RF trace, the recommended solution is to carve out the copper area of the second layer that projected by the RF MAIN pad at top layer. How many layers to be carved out depends on the PCB permittivity, track width, and distance from the floor of PCB. Our target is to make the RF MAIN pad impedance as close to 50 Ω as possible.

3.18 Reserved Pins

The module provides some reserved pins. All reserved pins cannot be used by the customer. **All of them should be Not Connected**.

3.19 Interface States in Sleep Mode

Table 3-23 shows the interface states after the module is powered on and when module is in sleep mode.

Table 3-23 Interface states in sleep mode

Interface	Signal	Pad Type (Power_on , Initialization Completed)	Pad Type (Module in Sleep Mode)
USIM	USIM0_DET	I	Input/HW_PU
	USIM0_DATA	I/O	Keeper/HW_PU
	USIM0_CLK	O	Keeper
	USIM0_RST	O	Keeper
UART	UART0_RX	I	Keeper
	UART0_TX	O	Keeper

Interface	Signal	Pad Type (Power_on , Initialization Completed)	Pad Type (Module in Sleep Mode)
	UART1_TX	O	Keeper
	UART1_RX	I	Keeper
	UART1_CTS	I	Keeper
	UART1_RTS	O	Keeper
	UART2_CTS	I	Keeper
	UART2_RX	I	Keeper
	UART2_RTS	O	Keeper
	UART2_TX	O	Keeper
	UART3_CTS	I	Keeper
	UART3_RX	I	Keeper
	UART3_RTS	O	Keeper
	UART3_TX	O	Keeper
USB	USB20_DM	I/O	Keeper
	USB20_DP	I/O	Keeper
PCM	PCM_SYNC	O	Keeper
	PCM_DOUT	O	Keeper
	PCM_CLK	O	Keeper
	PCM_DIN	I	Keeper
GPIO	GPIO1	I/O	Keeper
	GPIO2	I/O	Keeper
	GPIO3	I/O	Keeper
	GPIO4	I/O	Keeper
	GPIO5	I/O	Keeper
	GPIO6	I/O	Keeper
	GPIO7	I/O	Keeper
	GPIO8	I/O	Keeper
	GPIO9	I/O	Keeper
	GPIO10	I/O	Keeper
	GPIO11	I/O	Keeper
	GPIO12	I/O	Keeper

Interface	Signal	Pad Type (Power_on , Initialization Completed)	Pad Type (Module in Sleep Mode)
	GPIO13	I/O	Keeper
I2C	I2C0_SDA	I/O	Keeper
	I2C0_SCL	O	Keeper
Control Signal	LED_MODE	O	Keeper
	LED_STATUS	O	Keeper
	SLEEP_STATUS	O	O/SW_PD
	WAKEUP_SLEEP_OUT	O	Keeper
	WAKEUP_SLEEP_IN	I	I/SW_PD
SDIO	SDIO_DATA0	I/O	Keeper
	SDIO_DATA1	I/O	Keeper
	SDIO_DATA2	I/O	Keeper
	SDIO_DATA3	I/O	Keeper
	SDIO_CMD	I/O	Keeper
	SDIO_CLK	O	Keeper
ADC	ADC1	I	Keeper
	ADC2	I	Keeper
	ADC3	I	Keeper
	ADC4	I	Keeper

NOTE
HW_PD=pull-down by hardware; HW_PU=pull-up by hardware; SW_PD=pull-down by software; SW_PU=pull-up by software; NP=no pull; Keeper=remain the state following the feature.

3.20 Test Points Design

In the process of debugging when the module is embedded into the integrated equipment, test points play an important role. Some problems related to the module can be quickly resolved when test points are properly designed.

1. The test points below must be designed in the customer board:
   - JTAG test points: It is the most common method of debugging.
   - USB test points: USB is the most important communication channel between module and AP (host). Not only test points should be placed, but also a 0 ohm series resistor should be placed on USB_D+/USB_D- signal. The resistor can

be welded off when necessary, then the USB of module is cut off from AP and can be connected to PC to do some analysis.

- PS_HOLD: It indicates whether the PMIC finished the power procedure or not.
- POWER_ON_OFF, RSTIN_N: They are some of the most important signals, test points should be placed.
- UART0: UART0 is used for printing the log information.
- VBAT: Not only test points should be placed, but also a series magnetic bead should be placed on VBAT signal. The magnetic bead can be welded off when necessary, then the power of module is cut off from customer board and can be connected to external power to do analysis about problems related to power interference.
- VCC_EXT1: To judge whether the module is powered on or not.
- FAST_USB_LOAD: To keep the module fast booting through USB (active low).

2. The test points which are ADC, SLEEP_STATUS, GPIO, PCM, SIM, UART0, WAKEUP_SLEEP_IN and WAKEUP_SLEEP_OUT should be placed according to the requirement in the customer board, except the two cases below:
   - The corresponding signal is not used.
   - The corresponding signal is used, but there is already someplace else can be tested, such as SIM socket pin.

4 RF Specifications

4.1 About This Chapter

This chapter describes the RF specifications of the module, including:

- Operating Frequencies
- Conducted RF Measurement
- Conducted Rx Sensitivity and Tx Power
- Antenna Design Requirements
- Suggestions about LTE and Wi-Fi Co-existence

4.2 Operating Frequencies

Table 4-1 –Table 4-3 show the RF bands supported.

Table 4-1 RF bands supported by ME919Bs-127bN/bNb

Operating Band	Tx	Rx
UMTS Band 1	1920–1980 MHz	2110–2170 MHz
UMTS Band 8	880–915 MHz	925–960 MHz
GSM 900	880–915 MHz	925–960 MHz
GSM 1800	1710–1785 MHz	1805–1880 MHz
LTE Band 1	1920–1980 MHz	2110–2170 MHz
LTE Band 3	1710–1785 MHz	1805–1880 MHz
LTE Band 7	2500–2570 MHz	2620–2690 MHz
LTE Band 8	880–915 MHz	925–960 MHz
LTE Band 20	832–862 MHz	791–821 MHz
LTE Band 28	703–748 MHz	758–803 MHz

Operating Band	Tx	Rx
LTE Band 38	2570–2620 MHz	2570–2620 MHz
GPS L1	-	1574.42–1576.42 MHz
GLONASS L1	-	1597.55–1605.89 MHz

Table 4-2 RF bands supported by ME919Bs-567bN/bNb

Operating Band	Tx	Rx
UMTS Band 2	1850–1910 MHz	1930–1990 MHz
UMTS Band 4	1710–1755 MHz	2110–2155 MHz
UMTS Band 5	824–849 MHz	869–894 MHz
GSM 850	824 MHz–849 MHz	869–894 MHz
GSM 1900	1850–1910 MHz	1930–1990 MHz
LTE Band 2	1850–1910 MHz	1930–1990 MHz
LTE Band 4	1710–1755MHz	2110–2155MHz
LTE Band 5	824–849 MHz	869–894 MHz
LTE Band 7	2500–2570 MHz	2620–2690 MHz
LTE Band 12	699–716 MHz	729–746 MHz
LTE Band 13	777–787 MHz	746–756 MHz
LTE Band 29	-	717–728 MHz
GPS L1	-	1574.42–1576.42 MHz

Table 4-3 RF bands supported by ME919Bs-821bN/bNb

Operating Band	Tx	Rx
UMTS Band 1	1920–1980 MHz	2110–2170 MHz
UMTS Band 8	880–915 MHz	925–960 MHz
UMTS Band 5	824–849 MHz	869–894 MHz
UMTS Band 19	830–845 MHz	875–890 MHz
TDSCDMA Band 34	2010–2025 MHz	2010–2025 MHz
TDSCDMA Band 39	1880–1920 MHz	1880–1920 MHz
GSM 900	880–915 MHz	925–960 MHz
GSM 1800	1710–1785 MHz	1805–1880 MHz

Operating Band	Tx	Rx
LTE Band 1	1920–1980 MHz	2110–2170 MHz
LTE Band 3	1710–1785 MHz	1805–1880 MHz
LTE Band 5	824–849 MHz	869–894 MHz
LTE Band 8	880–915 MHz	925–960 MHz
LTE Band 19	830–845 MHz	875–890 MHz
LTE Band 38	2570–2620 MHz	2570–2620 MHz
LTE Band 39	1880–1920 MHz	1880–1920 MHz
LTE Band 40	2300–2400 MHz	2300–2400 MHz
LTE Band 41	2555–2635 MHz	2555–2635 MHz
GPS L1	-	1574.42–1576.42 MHz
Beidou B1	-	1559.052–1563.144 MHz

NOTE

[1]: Normal operating bandwidth of LTE Band B40: 2300–2370 MHz (CMCC&CUCC only).

4.3 Conducted RF Measurement

4.3.1 Test Environment

Test instrument	R&S CMU200, R&S CMW500, Anritsu MT8820C, GSS6700 multi-gnss simulator
Power supply	KEITHLEY 2306, Agilent 66319
RF cable for testing	L08-C014-350 of DRAKA COMTEQ or Rosenberger Cable length: 29 cm

NOTE

- The compensation for different frequency bands relates to the cable and the test environment.
- The instrument compensation needs to be set according to the actual cable conditions.

4.3.2 Test Standards

Huawei modules meet all 3GPP test standards relating to 2G, 3G and LTE. Each module passes strict tests at the factory and thus the quality of the modules is guaranteed.

4.4 Conducted Rx Sensitivity and Tx Power

4.4.1 Conducted Receive Sensitivity

The conducted receive sensitivity is a key parameter that indicates the receiver performance of the module. The conducted receive sensitivity refers to the weakest signal that the module at the antenna port can receive. The bit error rate (BER) must meet the 3GPP protocol requirements in the case of the minimum signal.

The **3GPP Protocol Claim** column inTable 4-4 –Table 4-6 lists the required minimum values, and the **Test Value** column lists the tested values of the module under 4 V voltage and normal temperature.

Table 4-4 Conducted Rx sensitivity of ME919Bs-127bN/bNb

Item		3GPP Protocol Claim (dBm)	Test Value (dBm)		
			Min.	Typ.	Max.
GSM 900	GMSK (BER < 2.44%)	< –102	-	-108	-
	8PSK (MCS5, BLER < 10%)	< –98	-	-109.5	-
GSM 1800	GMSK (BER < 2.44%)	< –102	-	-107	-
	8PSK (MCS5, BLER < 10%)	< –98	-	-108	-
UMTS Band 1 (BER < 0.1%)		< –106.7	-	-108	-
UMTS Band 8 (BER < 0.1%)		< –103.7	-	-109	-
LTE Band 1 RX (Main+AUX,10 MHz)		< –97	-	-100	-
LTE Band 3 RX (Main+AUX,10 MHz)		< –94	-	-100	-
LTE Band 7 RX (Main+AUX,10 MHz)		< –95	-	-99.8	-
LTE Band 8 RX (Main+AUX,10 MHz)		< –94	-	-100.2	-
LTE Band 20 RX (Main+AUX,10 MHz)		< –94	-	-102	-
LTE Band 28 RX (Main+AUX,10 MHz)		< –95.5	-	-101.5	-
LTE Band 38 RX (Main+AUX,10 MHz)		< –97	-	-100.5	-
GNSS Cold Start Sensitivity		-	-	-146.5	-
GNSS Tracking Sensitivity		-	-	-159	-

Table 4-5 Conducted Rx sensitivity of ME919Bs-567bN/bNb

Item		3GPP Protocol Claim (dBm)	Test Value (dBm)		
			Min.	Typ.	Max.
GSM 850	GMSK (BER < 2.44%)	< –102	-	-108	-
	8PSK (MCS5, BLER < 10%)	< –98	-	-110.5	-
GSM 1900	GMSK (BER < 2.44%)	< –102	-	-107	-
	8PSK (MCS5, BLER < 10%)	< –98	-	-108	-
UMTS Band 2 (BER < 0.1%)		< –104.7	-	-109	-
UMTS Band 4 (BER < 0.1%)		< –106.7	-	-109	-
UMTS Band 5 (BER < 0.1%)		< –104.7	-	-110	-
LTE Band 2 RX (Main+AUX,10 MHz)		< –97	-	-100	-
LTE Band 4 RX (Main+AUX,10 MHz)		< –94	-	-100	-
LTE Band 5 RX (Main+AUX,10 MHz)		< –95	-	-103.5	-
LTE Band 7 RX (Main+AUX,10 MHz)		< –94	-	-100	-
LTE Band 12 RX (Main+AUX,10 MHz)		< –94	-	-102.2	-
LTE Band 13 RX (Main+AUX,10 MHz)		< –94	-	-102.2	-
LTE Band 29 RX (Main+AUX,10 MHz)		< –94	-	-104.2	-
GNSS Cold Start Sensitivity		-	-	-146.5	-
GNSS Tracking Sensitivity		-	-	-159	-

Table 4-6 conducted Rx sensitivity of ME919Bs-821bN/bNb

Item		3GPP Protocol Claim (dBm)	Test Value (dBm)		
			Min.	Typ.	Max.
GSM 900	GMSK (BER < 2.44%)	< –102	-	-109.5	-
	8PSK (MCS5, BLER < 10%)	< –98	-	-109.3	-
GSM 1800	GMSK (BER < 2.44%)	< –102	-	-109.2	-
	8PSK (MCS5, BLER < 10%)	< –98	-	-109	-
UMTS Band 1 (BER < 0.1%)		< –106.7	-	-109.5	-
UMTS Band 5 (BER < 0.1%)		< –104.7	-	-111	-

Item	3GPP Protocol Claim (dBm)	Test Value (dBm)		
		Min.	Typ.	Max.
UMTS Band 8 (BER < 0.1%)	< –103.7	-	-110	-
UMTS Band 19 (BER < 0.1%)	< –106.7	-	-110	-
TDSCDMA Band 34	< –108	-	-109.5	-
TDSCDMA Band 39	< –108	-	-109.5	-
LTE Band 1 RX (Main+AUX,10 MHz)	< –97	-	-100	-
LTE Band 3 RX (Main+AUX,10 MHz)	< –94	-	-100.3	-
LTE Band 5 RX (Main+AUX,10 MHz)	< –95	-	-101.3	-
LTE Band 8 RX (Main+AUX,10 MHz)	< –94	-	-102	-
LTE Band 19 RX (Main+AUX,10 MHz)	< –94	-	-101	-
LTE Band 38 RX (Main+AUX,10 MHz)	< –97	-	-100	-
LTE Band 39 RX (Main+AUX,10 MHz)	< –97	-	-100	-
LTE Band 40 RX (Main+AUX,10 MHz)	< –97	-	-101	-
LTE Band 41 RX (Main+AUX,10 MHz)	< –95	-	-100.5	-
GNSS Cold Start Sensitivity	-	-	-146.5	-
GNSS Tracking Sensitivity	-	-	-159	-

4.4.2 Conducted Transmit Power

The conducted transmit power is another indicator that measures the performance of the module. The conducted transmit power refers to the maximum power that the module tested at the antenna port can transmit. According to the 3GPP protocol, the required transmit power varies with the power class.

Table 4-7 –Table 4-9 list the required ranges of the conducted transmit power of the module under 4 V voltage and normal temperature. The tested values listed in the **Test Value** column must range from the minimum power to the maximum power.

Table 4-7 Conducted Tx power of ME919Bs-127bN/bNb

Item		3GPP Protocol Claim (dBm)	Test Value (dBm)		
			Min.	Typ.	Max.
GSM 900	GMSK (1Tx Slot)	31–35	31	32.5	34
	8PSK (1Tx Slot)	24–30	25.5	27	28.5
GSM 1800	GMSK (1Tx Slot)	28–30	28	29.5	31
	8PSK (1Tx Slot)	22–29	24.5	26	27.5

Item	3GPP Protocol Claim (dBm)	Test Value (dBm)		
		Min.	Typ.	Max.
UMTS Band 1	21–25	21.5	23	24.5
UMTS Band 8	21–25	22	23.5	25
LTE Band 1	21–25	21	22.5	24
LTE Band 3	21–25	21	22.5	24
LTE Band 7	21–25	21	22	23.5
LTE Band 8	21–25	21.5	23	24.5
LTE Band 20	21–25	21.5	23	24.5
LTE Band 28	21–25	21.5	23	24.5
LTE Band 38	21–25	21	22	23.5

Table 4-8 Conducted Tx power of ME919Bs-567bN/bNb

Item	3GPP Protocol Claim (dBm)	Test Value (dBm)		
		Min.	Typ.	Max.
GMSK (1Tx Slot)	31–35	31	32.5	34
8PSK (1Tx Slot)	24–30	25.5	27	28.5
GMSK (1Tx Slot)	28–30	28	29.5	31
8PSK (1Tx Slot)	22–29	24.5	26	27.5
UMTS Band 2	21–25	21.5	23	24.5
UMTS Band 4	21–25	21.5	23	24.5
UMTS Band 5	21–25	22	23.5	25
LTE Band 2	21–25	21	22.5	24
LTE Band 4	21–25	21	22.5	24
LTE Band 5	21–25	21.5	23	24.5
LTE Band 7	21–25	21	22	23.5
LTE Band 12	21–25	21.5	23	24.5
LTE Band 13	21–25	21.5	23	24.5

Table 4-9 Conducted Tx power of ME919Bs-821bN/bNb

Item	3GPP Protocol Claim (dBm)	Test Value (dBm)		
		Min.	Typ.	Max.
GMSK (1Tx Slot)	31–35	31	32.5	34
8PSK (1Tx Slot)	24–30	25.5	27	28.5
GMSK (1Tx Slot)	28–30	28	29.5	31
8PSK (1Tx Slot)	22–29	24.5	26	27.5
UMTS Band 1	21–25	21	23	24.5
TDSCDMA Band 34	21–25	22	23.5	25
TDSCDMA Band 39	21–25	22	23.5	25
UMTS Band 5	21–25	22	23.5	25
UMTS Band 8	21–25	22	23.5	25
UMTS Band 19	21–25	22	23.5	25
LTE Band 1	21–25	21	22.5	24
LTE Band 3	21–25	21	22.5	24
LTE Band 5	21–25	21.5	23	24.5
LTE Band 8	21–25	21.5	23	24.5
LTE Band 19	21–25	21.5	23	24.5
LTE Band 38	21–25	21	22	23.5
LTE Band 39	21–25	21	22.5	24
LTE Band 40	21–25	21	22	23.5
LTE Band 41	21–25	21	22	23.5

NOTE

Maximum Power Reduction (MPR) and Additional Maximum Power Reduction (A-MPR) of LTE is according to 3GPP TS 36.521-1 as below.

Modulation	RB Allocation	MPR (dB)
QPSK	≥ 1 RB, ≤ Partial RB	0
QPSK	> Partial RB	≤ 1
16QAM	≥ 1 RB, ≤ Partial RB	≤ 1
16QAM	> Partial RB	≤ 2

4.5 Antenna Design Requirements

4.5.1 Antenna Design Indicators

Antenna Efficiency

Antenna efficiency is the ratio of the input power to the radiated or received power of an antenna. The radiated power of an antenna is always lower than the input power due to the following antenna losses: return loss, material loss, and coupling loss. The efficiency of an antenna relates to its electrical dimensions. To be specific, the antenna efficiency increases with the electrical dimensions. In addition, the transmission cable from the antenna port of the module to the antenna is also part of the antenna. The cable loss increases with the cable length and the frequency. It is recommended that the cable loss should be as low as possible.

To ensure high radio performance of the module, the antenna efficiency (free space) is recommended as below:

- Efficiency of the primary antenna: ≥ 40% (below 960 MHz); ≥ 50% (over 1710 MHz).
- Efficiency of the diversity antenna: ≥ half of the efficiency of the primary antenna in receiving band.

In addition, the efficiency should be tested with the transmission cable.

S11 or VSWR

S11 indicates the degree to which the input impedance of an antenna matches the reference impedance (50 Ω). S11 shows the resonance feature and impedance bandwidth of an antenna. Voltage standing wave ratio (VSWR) is another expression of S11. S11 relates to the antenna efficiency. S11 can be measured with a vector analyzer.

The S11 value for the antenna of the module is recommended as below:

- S11 of the primary antenna ≤ –6 dB.
- S11 of the diversity antenna ≤ –6 dB.
- S11 of the GNSS antenna ≤ –10 dB.

Isolation

For a wireless device with multiple antennas, the power of different antennas is coupled with each other. Antenna isolation is used to measure the power coupling. The power radiated by an antenna might be received by an adjacent antenna, which decreases the antenna radiation efficiency and affects the running of other devices. To avoid this problem, evaluate the antenna isolation as sufficiently as possible at the early stage of antenna design.

Antenna isolation depends on the following factors:

- Distance between antennas
- Antenna type
- Antenna direction

The primary antenna must be placed as close to the module as possible to minimize the cable length. The diversity antenna needs to be installed perpendicularly to the primary antenna. The diversity antenna can be placed farther away from the module. Antenna isolation can be measured with a two-port vector network analyzer.

The antenna isolation is recommended as below:

- Isolation between the primary and diversity antennas ≤ –12 dB
- Isolation between the primary (diversity) antenna and the GNSS antenna ≤ –25 dB
- Isolation between the primary (diversity) antenna and the Wi-Fi antenna ≤ –25 dB

Polarization

The polarization of an antenna is the orientation of the electric field vector that rotates with time in the direction of maximum radiation.

The linear polarization is recommended for the antenna of the module.

Envelope Correlation Coefficient

The envelope correlation coefficient indicates the correlation between different antennas (primary antenna and diversity antenna) in a multi-antenna system. The correlation coefficient shows the similarity of radiation patterns, that is, amplitude and phase, of the antennas. The ideal correlation coefficient of a diversity antenna system is 0. A small value of the envelope correlation coefficient between the primary antenna and the diversity antenna indicates a high diversity gain. The envelope correlation coefficient depends on the following factors:

- Distance between antennas
- Antenna type
- Antenna direction

The antenna correlation coefficient differs from the antenna isolation. Sufficient antenna isolation does not represent a satisfactory correlation coefficient. For this reason, the two indicators need to be evaluated separately.

For the antennas, the recommended envelope correlation coefficient between the primary antenna and the diversity antenna is smaller than 0.5.

Radiation Pattern

The radiation pattern of an antenna reflects the radiation features of the antenna in the remote field region. The radiation pattern of an antenna commonly describes the power or field strength of the radiated electromagnetic waves in various directions from the antenna. The power or field strength varies with the angular coordinates (θ and φ), but is independent of the radial coordinates.

The radiation pattern of half wave dipole antennas is omnidirectional in the horizontal plane, and the incident waves of base stations are often in the horizontal plane. For this reason, the receiving performance is optimal.

The radiation pattern for the antenna of the module is recommended as below,

Primary/diversity antenna: omnidirectional.

In addition, the pattern of the diversity antenna should be complementary with that of the primary antenna.

Gain and Directivity

The radiation pattern of an antenna represents the field strength of the radiated electromagnetic waves in all directions, but not the power density that the antenna radiates in the specific direction. The directivity of an antenna, however, measures the power density that the antenna radiates.

Gain, as another important parameter of antennas, correlates closely to the directivity. The gain of an antenna takes both the directivity and the efficiency of the antenna into account. The appropriate antenna gain prolongs the service life of relevant batteries.

The antenna gain of the module is recommended as below:

- Gain of the primary antenna ≤ 2 dBi
- Gain of the diversity antenna ≤ 2 dBi

NOTE

- The antenna consists of the antenna body and the relevant RF transmission cable. Take the RF transmission cable into account when measuring any of the preceding antenna indicators.
- Huawei cooperates with various famous antenna suppliers who are able to make suggestions on antenna design, for example, Amphenol, Skycross, etc.

4.5.2 Interference

Besides the antenna performance, the interference on the user board also affects the radio performance (especially the TIS) of the module. To guarantee high performance of the module, the interference sources on the user board must be properly controlled.

On the user board, there are various interference sources, such as the LCD, CPU, audio circuits, and power supply. All the interference sources emit interference signals that affect the normal operation of the module. For example, the module sensitivity can be decreased due to interference signals. Therefore, during the design, need to consider how to reduce the effects of interference sources on the module. It is recommended to take the following measures:

- Use an LCD with optimized performance.
- Shield the LCD interference signals.
- Shield the signal cable of the board.
- Design filter circuits.

Huawei is able to make technical suggestions on radio performance improvement of the module.

4.5.3 GSM/WCDMA/LTE Antenna Requirements

The antenna for the module must fulfill the requirements as shown in Table 4-10 .

Table 4-10 Requirements for GSM/WCDMA/LTE antenna

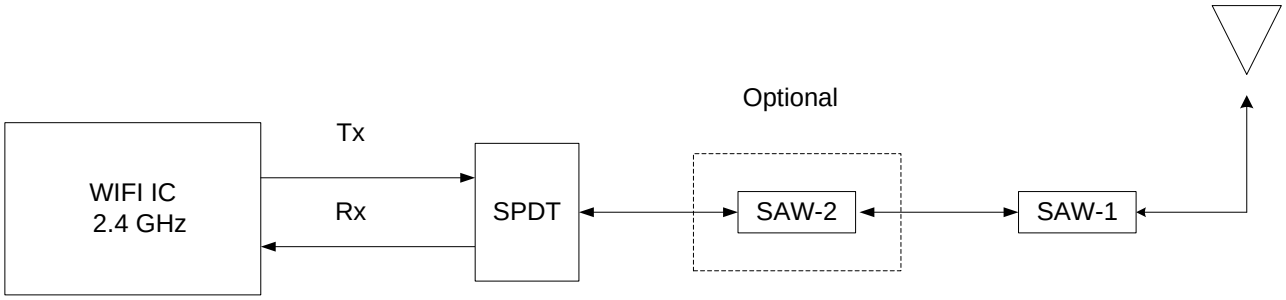
Frequency range	Depending on frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s).
Bandwidth of primary antenna	70 MHz in GSM 850 80 MHz in GSM 900 170 MHz in GSM 1800 140 MHz in GSM 1900 250 MHz in WCDMA/LTE Band 1 140 MHz in WCDMA/LTE Band 2 445 MHz in WCDMA/LTE Band 4 70 MHz in WCDMA/LTE Band 5 80 MHz in WCDMA/LTE Band 8 60 MHz in WCDMA/LTE Band 19 170 MHz in LTE Band 3 190 MHz in LTE Band 7 47 MHz in LTE Band 12 41 MHz in LTE Band 13 71 MHz in LTE Band 20 100 MHz in LTE Band 28 12 MHz in LTE Band 29 15 MHz in LTE Band 34 50 MHz in LTE Band 38 40 MHz in LTE Band 39 70 MHz in LTE Band 40 80 MHz in LTE Band 41

Bandwidth of diversity antenna	60 MHz in WCDMA/LTE Band 1 60 MHz in WCDMA/LTE Band 2 45 MHz in WCDMA/LTE Band 4 25 MHz in WCDMA/LTE Band 5 35 MHz in WCDMA/LTE Band 8 15 MHz in WCDMA/LTE Band 19 75 MHz in LTE Band 3 70 MHz in LTE Band 7 17 MHz in LTE Band 12 10 MHz in LTE Band 13 12 MHz in LTE Band 17 30 MHz in LTE Band 20 45 MHz in LTE Band 28 12 MHz in LTE Band 29 15 MHz in LTE Band 34 50 MHz in LTE Band 38 40 MHz in LTE Band 39 70 MHz in LTE Band 40 80 MHz in LTE Band 41
Gain	≤ 2 dBi
Impedance	50 Ω
VSWR absolute max	≤ 3:1
VSWR recommended	≤ 2:1

4.6 Suggestions about LTE and Wi-Fi Co-existence

The working frequency range of Wi-Fi (2400–2489 MHz) is close to that of LTE. For LTE and Wi-Fi co-existence, some system-level measures must be taken into consideration. While some measures have been taken on the module, it is recommended that one or two SAW filters be added to the Wi-Fi device, as shown in Figure 4-1 .

Figure 4-1 Recommended Structure



1. It is recommended that the system should be added Wi-Fi SAW filter to guarantee good attenuation in the LTE transmit Band (mainly Band 7), otherwise, LTE Band output power will block Wi-Fi receiver.
2. The good isolation between LTE antenna and Wi-Fi antenna is more than 25 dB.
3. After one or two SAW filters are added, the isolation between the antennas can be increased to more than 60 dB. If this isolation is still insufficient, close some channels.

5 Electrical Features

5.1 About This Chapter

This chapter describes the electrical features of the interfaces in the module, including:

- Absolute Ratings
- Operating and Storage Temperatures and Humidity
- Electrical Features of Application Interfaces
- Power Supply Features
- EMC and ESD Features

5.2 Absolute Ratings

WARNING

Table 5-1 lists the absolute ratings for the module. Using the module beyond these conditions may result in permanent damage to the module.

Table 5-1 Absolute ratings

Symbol	Specification	Min.	Max.	Unit
VBAT	External power voltage	–0.3	4.5	V

5.3 Operating and Storage Temperatures and Humidity

Table 5-2 lists the operating and storage temperatures and humidity for the ME919Bs LGA module.

Table 5-2 Operating and storage temperatures and humidity

Specification	Min.	Max.	Unit
Normal operating temperature	–30	+75	°C
Extended operating temperature[1]	–40	+85	°C
Ambient storage temperature	–40	+95	°C
Moisture	5	95	%

NOTE

[1]: When the module works at –40°C to –30°C and 75°C to 85°C, **NOT** all its RF performances comply with 3GPP specifications.

5.4 Electrical Features of Application Interfaces

Table 5-3 Electrical features of Digital Pins (GPIO/I2C/PCM/UART/SPI/RGMII/MII/Control GPIO)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Logic high-level input voltage	1.17	1.98	V
V_{IL}	Logic low-level input voltage	–0.3	0.63	V
V_{OH}	Logic high-level output voltage	1.35	-	V
V_{OL}	Logic low-level output voltage	-	0.45	V
I_{OH}	High-level output current @ VOL (max)	4	-	mA
I_{OL}	Low-level output current @ VOL (max)	4	-	mA
Rpu	Pull-up Resistor inner module	28	50	kΩ
Rpd	Pull-down Resistor inner module	28	50	kΩ

Table 5-4 Electrical features of Digital Pins in the I/O supply domain of the USIM Interface (Some parameters differs from VDD=1.8/3.0 V)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Logic high-level input voltage	0.625*VDD (3.0 V) 1.27 (1.8 V)	VDD + 0.3 (3.0 V) 2.00 (1.8 V)	V

Parameter	Description	Min.	Max.	Unit
V_{IL}	Logic low-level input voltage	-0.3	0.25*VDD (3.0 V) 0.58 (1.8 V)	V
V_{OH}	Logic high-level output voltage	0.75*VDD (3.0 V) 1.40 (1.8 V)	-	V
V_{OL}	Logic low-level output voltage	-	0.125*VDD (3.0 V) 0.45 (1.8 V)	V

Table 5-5 Electrical features of Digital Pins in the I/O supply domain of the SDIO Interface (VREG_SD=1.8 V)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Logic high-level input voltage	1.27	3.15	V
V_{IL}	Logic low-level input voltage	-0.3	0.58	V
V_{OH}	Logic high-level output voltage	1.4	-	V
V_{OL}	Logic low-level output voltage	-	0.45	V

Table 5-6 Electrical features of Digital Pins in the I/O supply domain of the SDIO Interface (VREG_SD=2.85 V)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Logic high-level input voltage	1.875	3.15	V
V_{IL}	Logic low-level input voltage	-0.3	0.7125	V
V_{OH}	Logic high-level output voltage	2.25	-	V
V_{OL}	Logic low-level output voltage	-	0.375	V

5.5 Power Supply Features

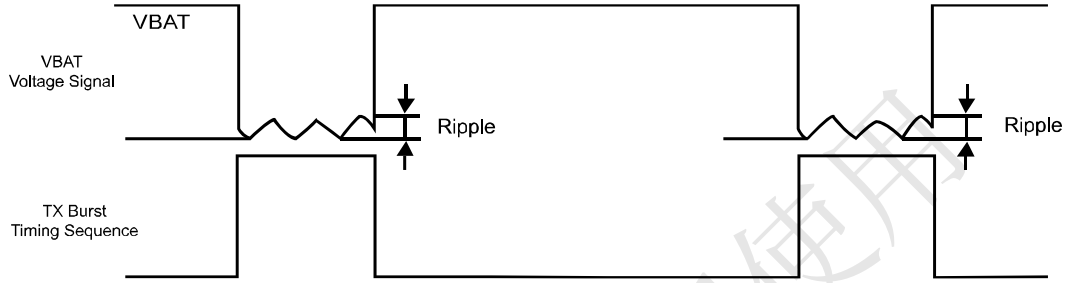
5.5.1 Input Power Supply

Table 5-7 lists the requirements for input power of the ME919Bs LGA module.

Table 5-7 Requirements for input power

Parameter	Min.	Typ.	Max.	Ripple	Unit
VBAT	3.8	4.0	4.2	0.05	V

Figure 5-1 Power supply during burst emission



NOTE

The VBAT minimum value must be guaranteed during the burst (with 2.8 A Peak in GPRS or GSM mode).

Table 5-8 Requirements for input current

Power	Peak (GSM 1 slot)	Normal (WCDMA)	Normal (LTE)
VBAT	2.8 A	1.4 A	1.4 A

5.5.2 Power Consumption

The power consumptions of the module in different scenarios are listed in Table 5-9 to Table 5-18 respectively.

The power consumption listed in this section are tested when the power supply of the module is normal voltage (4.0 V), and all of test values are measured at room temperature.

Table 5-9 Averaged power off DC power consumption

Description	Test Value (Unit: μA)	Notes/Configuration
	Typical	
The module is turned off	150	Normal voltage (4.0 V) is ON.

Table 5-10 Averaged standby DC power consumption of the ME919Bs-127bN/bNb

Description		Test Value (Unit: mA)	Notes/Configuration
		Typical	
Standby Mode	LTE	2.2	Module is powered up. DRX cycle=7 (1.28s) Module is registered on the network. USB is in suspend.
	HSPA /WCDMA	1.5	Module is powered up DRX cycle=8 (2.56s) Module is registered on the network. USB is in suspend.
	GPRS/EDGE	2.2	Module is powered up MFRMS=5 (1.18s) Module is registered on the network. USB is in suspend.
	Radio Off	1.0	Module is powered up. RF is disabled USB is in suspend.

Table 5-11 Averaged standby DC power consumption of the ME919Bs-567bN/bNb

Description		Test Value (Unit: mA)	Notes/Configuration
		Typical	
Standby Mode	LTE	2.2	Module is powered up. DRX cycle=7 (1.28s) Module is registered on the network. USB is in suspend.
	HSPA /WCDMA	1.5	Module is powered up DRX cycle=8 (2.56s) Module is registered on the network. USB is in suspend.
	GPRS /EDGE	2.2	Module is powered up MFRMS=5 (1.18s) Module is registered on the network. USB is in suspend.

Description		Test Value (Unit: mA)	Notes/Configuration
		Typical	
	Radio Off	1.0	Module is powered up. RF is disabled USB is in suspend.

Table 5-12 Averaged standby DC power consumption of the ME919Bs-821bN/bNb

Description		Test Value (Unit: mA)	Notes/Configuration
		Typical	
Standby Mode	LTE	2.2	Module is powered up. DRX cycle=7 (1.28s) Module is registered on the network. USB is in suspend.
	HSPA /WCDMA	1.5	Module is powered up DRX cycle=8 (2.56s) Module is registered on the network. USB is in suspend.
	TDSCDMA	1.5	Module is powered up DRX cycle=8 (2.56s) Module is registered on the network. USB is in suspend.
	GPRS /EDGE	2.2	Module is powered up MFRMS=5 (1.18s) Module is registered on the network. USB is in suspend.
	Radio Off	1.0	Module is powered up. RF is disabled USB is in suspend.

Table 5-13 Averaged data transmission DC power consumption of ME919Bs-127bN/bNb (LTE/WCDMA/HSDPA)

Description	Bands	Max. average current consumption	Unit	Power (dBm)
LTE	Band 1	360	mA	1 dBm Tx Power

Description	Bands	Max. average current consumption	Unit	Power (dBm)
		550		10 dBm Tx Power
		900		Max Tx Power
	Band 3	360	mA	1 dBm Tx Power
		540		10 dBm Tx Power
		950		Max Tx Power
	Band 7	430	mA	1 dBm Tx Power
		560		10 dBm Tx Power
		1000		Max Tx Power
	Band 8	360	mA	1 dBm Tx Power
		550		10 dBm Tx Power
		900		Max Tx Power
	Band 20	360	mA	1 dBm Tx Power
		540		10 dBm Tx Power
		950		Max Tx Power
	Band 28	370	mA	1 dBm Tx Power
		520		10 dBm Tx Power
		950		Max Tx Power
	Band 38	350	mA	1 dBm Tx Power
		400		10 dBm Tx Power
		450		Max Tx Power
WCDMA	Band 1	310	mA	1 dBm Tx Power
		510		10 dBm Tx Power
		930		Max Tx Power
	Band 8	310	mA	1 dBm Tx Power
		510		10 dBm Tx Power
		930		Max Tx Power
HSDPA	Band 1	320	mA	1 dBm Tx Power
		520		10 dBm Tx Power
		930		Max Tx Power
	Band 8	320	mA	1 dBm Tx Power

Description	Bands	Max. average current consumption	Unit	Power (dBm)
		520		10 dBm Tx Power
		930		Max Tx Power

Table 5-14 Averaged DC power consumption of ME919Bs-127bN/bNb (GSM/GPRS/EDGE)

Description	Max. average current consumption	Unit	PCL	Configuration
GPRS 900	460	mA	5	1 Up/1 Down
	610			2 Up/1 Down
	770			4 Up/1 Down
	330	mA	10	1 Up/1 Down
	420			2 Up/1 Down
	610			4 Up/1 Down
GPRS 1800	400	mA	0	1 Up/1 Down
	510			2 Up/1 Down
	650			4 Up/1 Down
	280	mA	10	1 Up/1 Down
	340			2 Up/1 Down
	430			4 Up/1 Down
EDGE 900	370	mA	8	1 Up/1 Down
	500			2 Up/1 Down
	700			4 Up/1 Down
	340	mA	15	1 Up/1 Down
	460			2 Up/1 Down
	690			4 Up/1 Down
EDGE 1800	350	mA	2	1 Up/1 Down
	470			2 Up/1 Down
	640			4 Up/1 Down
	330	mA	10	1 Up/1 Down
	430			2 Up/1 Down

Description	Max. average current consumption	Unit	PCL	Configuration
	620			4 Up/1 Down

Table 5-15 Averaged data transmission DC power consumption of ME919Bs-567bN/bNb (LTE/WCDMA/HSDPA)

Description	Bands	Max. average current consumption	Unit	Power (dBm)
LTE	Band 2	280	mA	1 dBm Tx Power
		440		10 dBm Tx Power
		700		Max Tx Power
	Band 4	260	mA	1 dBm Tx Power
		420		10 dBm Tx Power
		720		Max Tx Power
	Band 5	250	mA	1 dBm Tx Power
		440		10 dBm Tx Power
		840		Max Tx Power
	Band 7	340	mA	1 dBm Tx Power
		470		10 dBm Tx Power
		850		Max Tx Power
	Band 12	300	mA	1 dBm Tx Power
		410		10 dBm Tx Power
		790		Max Tx Power
	Band 13	260	mA	1 dBm Tx Power
		410		10 dBm Tx Power
		770		Max Tx Power
	Band 29	-	mA	1 dBm Tx Power
				10 dBm Tx Power
				Max Tx Power
WCDMA	Band 2	220	mA	1 dBm Tx Power
		410		10 dBm Tx Power
		730		Max Tx Power

Description	Bands	Max. average current consumption	Unit	Power (dBm)
	Band 4	200	mA	1 dBm Tx Power
		410		10 dBm Tx Power
		800		Max Tx Power
	Band 5	210	mA	1 dBm Tx Power
		400		10 dBm Tx Power
		780		Max Tx Power
HSDPA	Band 2	220	mA	1 dBm Tx Power
		400		10 dBm Tx Power
		750		Max Tx Power
	Band 4	200	mA	1 dBm Tx Power
		400		10 dBm Tx Power
		780		Max Tx Power
	Band 5	200	mA	1 dBm Tx Power
		380		10 dBm Tx Power
		780		Max Tx Power

Table 5-16 Averaged DC power consumption of ME919Bs-567bN/bNb (GSM/GPRS/EDGE)

Description	Max. average current consumption	Unit	PCL	Configuration
GPRS 850	320	mA	5	1 Up/1 Down
	450			2 Up/1 Down
	650			4 Up/1 Down
	200	mA	10	1 Up/1 Down
	280			2 Up/1 Down
	630			4 Up/1 Down
GPRS 1900	250	mA	0	1 Up/1 Down
	340			2 Up/1 Down
	490			4 Up/1 Down
	160	mA	10	1 Up/1 Down

Description	Max. average current consumption	Unit	PCL	Configuration
	220			2 Up/1 Down
	350			4 Up/1 Down
EDGE 850	260	mA	8	1 Up/1 Down
	370			2 Up/1 Down
	650			4 Up/1 Down
	230	mA	15	1 Up/1 Down
	350			2 Up/1 Down
	620			4 Up/1 Down
EDGE 1900	230	mA	2	1 Up/1 Down
	340			2 Up/1 Down
	600			4 Up/1 Down
	210	mA	10	1 Up/1 Down
	320			2 Up/1 Down
	580			4 Up/1 Down

Table 5-17 Averaged data transmission DC power consumption of ME919Bs-821bN/bNb (LTE/WCDMA/HSDPA)

Description	Bands	Max. average current consumption	Unit	Power (dBm)
LTE	Band 1	310	mA	1 dBm Tx Power
		460		10 dBm Tx Power
		830		Max Tx Power
	Band 3	320	mA	1 dBm Tx Power
		480		10 dBm Tx Power
		820		Max Tx Power
	Band 5	310	mA	1 dBm Tx Power
		460		10 dBm Tx Power
		880		Max Tx Power
	Band 8	310	mA	1 dBm Tx Power
		520		10 dBm Tx Power

Description	Bands	Max. average current consumption	Unit	Power (dBm)
		850		Max Tx Power
	Band 19	310	mA	1 dBm Tx Power
		460		10 dBm Tx Power
		900		Max Tx Power
	Band 38	280	mA	1 dBm Tx Power
		310		10 dBm Tx Power
		450		Max Tx Power
	Band 39	270	mA	1 dBm Tx Power
		320		10 dBm Tx Power
		400		Max Tx Power
	Band 40	300	mA	1 dBm Tx Power
		350		10 dBm Tx Power
		580		Max Tx Power
	Band 41	280	mA	1 dBm Tx Power
		330		10 dBm Tx Power
		460		Max Tx Power
WCDMA	Band 1	260	mA	1 dBm Tx Power
		460		10 dBm Tx Power
		840		Max Tx Power
	Band 5	234	mA	1 dBm Tx Power
		400		10 dBm Tx Power
		833		Max Tx Power
	Band 8	270	mA	1 dBm Tx Power
		450		10 dBm Tx Power
		790		Max Tx Power
	Band 19	236	mA	1 dBm Tx Power
		405		10 dBm Tx Power
		846		Max Tx Power
HSDPA	Band 1	270	mA	1 dBm Tx Power
		480		10 dBm Tx Power

Description	Bands	Max. average current consumption	Unit	Power (dBm)
		830		Max Tx Power
	Band 5	235	mA	1 dBm Tx Power
		405		10 dBm Tx Power
		826		Max Tx Power
	Band 8	260	mA	1 dBm Tx Power
		460		10 dBm Tx Power
		800		Max Tx Power
	Band 19	234	mA	1 dBm Tx Power
		404		10 dBm Tx Power
		843		Max Tx Power
TDSCDMA	Band 34	130	mA	1 dBm Tx Power
		140		10 dBm Tx Power
		180		Max Tx Power
	Band 39	130	mA	1 dBm Tx Power
		140		10 dBm Tx Power
		180		Max Tx Power

Table 5-18 Averaged DC power consumption of ME919Bs-821bN/bNb (GSM/GPRS/EDGE)

Description	Max. average current consumption	Unit	PCL	Configuration
GPRS 900	400	mA	5	1 Up/1 Down
	550			2 Up/1 Down
	740			4 Up/1 Down
	270	mA	10	1 Up/1 Down
	360			2 Up/1 Down
	550			4 Up/1 Down
GPRS 1800	330	mA	0	1 Up/1 Down
	440			2 Up/1 Down
	600			4 Up/1 Down

Description	Max. average current consumption	Unit	PCL	Configuration
	220	mA	10	1 Up/1 Down
	270			2 Up/1 Down
	370			4 Up/1 Down
EDGE 900	320	mA	8	1 Up/1 Down
	450			2 Up/1 Down
	690			4 Up/1 Down
	290	mA	15	1 Up/1 Down
	410			2 Up/1 Down
	660			4 Up/1 Down
EDGE 1800	300	mA	2	1 Up/1 Down
	410			2 Up/1 Down
	600			4 Up/1 Down
	270	mA	10	1 Up/1 Down
	380			2 Up/1 Down
	590			4 Up/1 Down

NOTE

- All power consumption test configuration can be referenced by GSM Association Official Document TS.09: Battery Life Measurement and Current Consumption Technique.
- LTE test condition: 10/20 MHz bandwidth, QPSK, 1 RB when testing max. Tx power and full RB when testing 0 dBm or 10 dBm.
- Current in the standby mode indicates module enters the sleep mode

Table 5-19 Averaged GPS operation DC power consumption

Description	Test Value (Unit: mA)	Notes/Configuration
	Typical	
GPS fixing	180	RF is disabled; USB is in active; The Rx power of GPS is –130 dBm.
GPS tracking	180	

NOTE

- All GPS operations is tested with external LNA.
- To ensure good performance, GPS active antenna (passive antenna+ LNA+SAW) is recommended to use.

5.6 EMC and ESD Features

5.6.1 EMC Design Comments

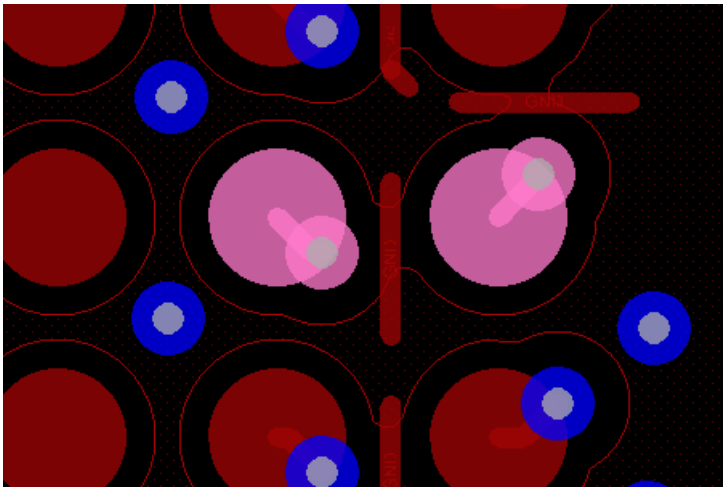
- Attention should be paid to static control in the manufacture, assembly, packaging, handling and storage process to reduce electrostatic damage to HUAWEI module.
- RSE (Radiated Spurious Emission) may exceed the limit defined by EN301489 if the antenna port is protected by TVS (Transient Voltage Suppressor), which is resolved by making some adjustment on RF match circuit.
- TVS should be added on the USB port for ESD protection, and the parasitic capacitance of TVS on D+/D- signal should be less than 2 pF. Common-mode inductor should be added in parallel on D+/D- signal.
- TVS should be added on the USIM interface for ESD protection. The parasitic capacitance of TVS on USIM signal should be less than 10 pF;
- Resistors in parallel and a 10 nF capacitance should be added on RSTIN_N and POWER_ON_OFF signal to avoid shaking, and the distance between the capacitor and the related pins should be less than 100 mil.
- PCB routing should be V-type rather than T-type for TVS (Transient Voltage Suppressor).
- An integrated ground plane is necessary for EMC design.

5.6.2 EMC Design Reference Guide

Please pay attention to the following requirements for the high speed interface EMI:

1. USB 2.0 and PCIE
   - Differential signals pair should be routed as symmetrically as possible.
   - Differential signals should be routed on the PCB inner layer. The fanout via should be placed as close to the LGA pad as possible.
   - Use as few changing layers as possible.
   - Place the GND via near the differential signal via.
2. SDIO/RGMII/MII
   - The fanout via should be located as close to the LGA pad as possible. as shown in Figure 5-2 .
   - The CLK signal trace must be routed near the GND trace on two sides, and GND vias must be placed at regular intervals.
   - The trace air gap must be more than 10 mil if there is a long distance between data signals and they are being routed in parallel mode.
   - SDIO/RGMII/MII data signals and signals of other types should be separated with a GND trace, or the trace air gap must be more than 3 w.

Figure 5-2 SDIO/RGMII/MII fanout example



3. LGA module shielding

   The fanout via and matching components of the SDIO/RGMII/MII should be placed within the shielding cover if the user's product has low radiation emissions requirements.

5.6.3 ESD Environment Control

- The electrostatic discharge protected area (EPA) must have an ESD floor whose surface resistance and system resistance are greater than 1 x 10^4 Ω while less than 1 x 10^9 Ω.
- The EPA must have a sound ground system without loose ground wires, and the ground resistance must be less than 4 Ω.
- The workbench for handling ESD sensitive components must be equipped with common ground points, the wrist strap jack, and ESD pad. The resistance between the jack and common ground point must be less than 4 Ω. The surface resistance and system resistance of the ESD pad must be less than 1 x 10^9 Ω.
- The EPA must use the ESD two-circuit wrist strap, and the wrist strap must be connected to the dedicated jack. The crocodile clip must not be connected to the ground.
- The ESD sensitive components, the processing equipment, test equipment, tools, and devices must be connected to the ground properly. The indexes are as follows:
  - Hard ground resistance < 4 Ω
  - 1 x 10^5 Ω ≤ Soft ground resistance < 1 x 10^9 Ω
  - 1 x 10^5 Ω ≤ ICT fixture soft ground resistance < 1 x 10^{11} Ω
  - The electronic screwdriver and electronic soldering iron can be easily oxidized. Their ground resistance must be less than 20 Ω.
- The parts of the equipment, devices, and tools that touch the ESD sensitive components and moving parts that are close to the ESD sensitive components must be made of ESD materials and have sound ground connection. The parts that are not made of ESD materials must be handled with ESD treatment, such as painting the ESD coating or ionization treatment (check that the friction voltage is less than 100 V).

- Key parts in the production equipment (parts that touch the ESD sensitive components or parts that are within 30 cm away from the ESD sensitive components), including the conveyor belt, conveyor chain, guide wheel, and SMT nozzle, must all be made of ESD materials and be connected to the ground properly (check that the friction voltage is less than 100 V).
- Engineers that touch IC chips, boards, modules, and other ESD sensitive components and assemblies must wear ESD wrist straps, ESD gloves, or ESD finger cots properly. Engineers that sit when handling the components must all wear ESD wrist straps.
- Noticeable ESD warning signs must be attached to the packages and placement areas of ESD sensitive components and assemblies.
- Boards and IC chips must not be stacked randomly or be placed with other ESD components.
- Effective shielding measures must be taken on the ESD sensitive materials that are transported or stored outside the EPA.

NOTE

The module does not include any protection against overvoltage.

6 Process Specifications

6.1 About This Chapter

This chapter describes the process design and mechanical specification of the module, including:

- Storage Requirement
- Moisture Sensitivity
- Dimensions
- Packaging
- Label
- Customer PCB Design
- Thermal Design Solution
- Assembly Processes
- Specification of Rework

6.2 Storage Requirement

The module must be stored and sealed properly in vacuum package under a temperature below 40°C and the relative humidity less than 90% in order to ensure the weldability within 12 months.

6.3 Moisture Sensitivity

- The moisture sensitivity is level 3.
- After unpacking, the module must be assembled within 168 hours under the environmental conditions that the temperature is lower than 30°C and the relative humidity is less than 60%. If the preceding conditions cannot be met, the module needs to be baked according to the parameters specified in Table 6-1 .

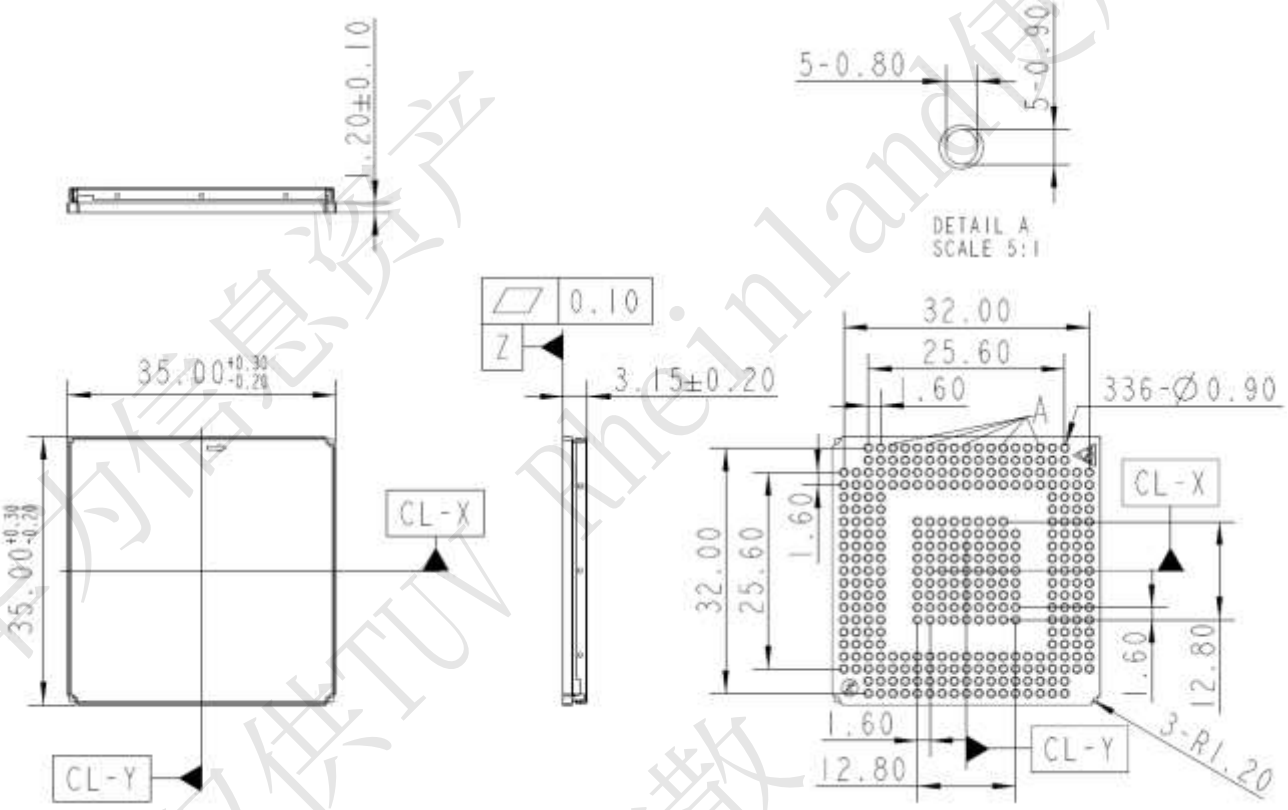
Table 6-1 Baking parameters

Baking Temperature	Baking Condition	Baking Duration	Remarks
125°C±5°C	Relative humidity ≤ 60%	8 hours	-

NOTE
Moving, storing, and processing the product must comply with IPC/JEDEC J-STD-033.

6.4 Dimensions

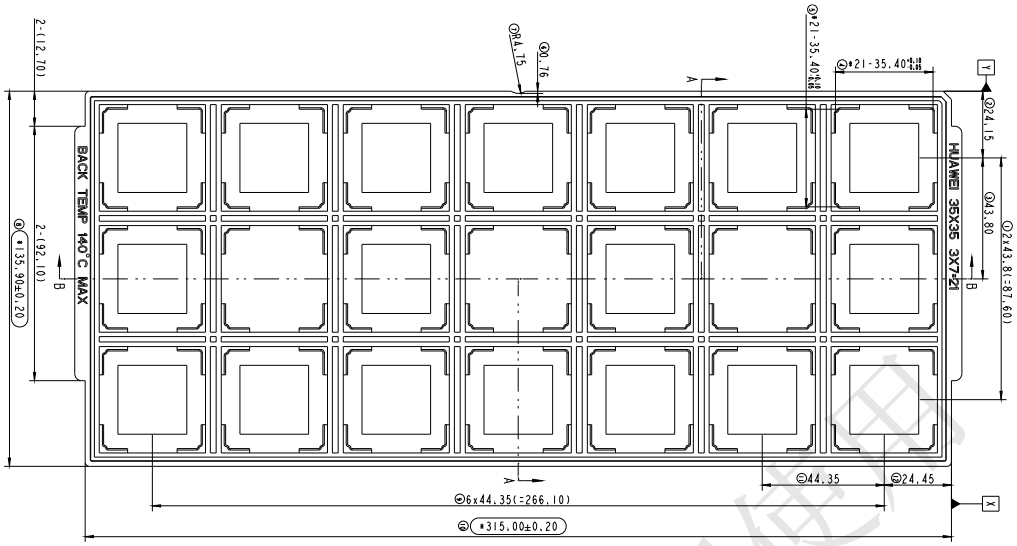
Figure 6-1 Dimensions (unit: mm)



6.5 Packaging

Huawei LGA module uses five layers ESD pallet, anti-vibration foam and vacuum packing into cartons.

Figure 6-2 ESD tray (Unit: mm)



NOTE

The pallet dimensions comply with JEDEC PUBLICATION 95 DESIGN GUIDE 4.10-1/D.

The following figures show the details of packaging.

Figure 6-3 Tray packaging

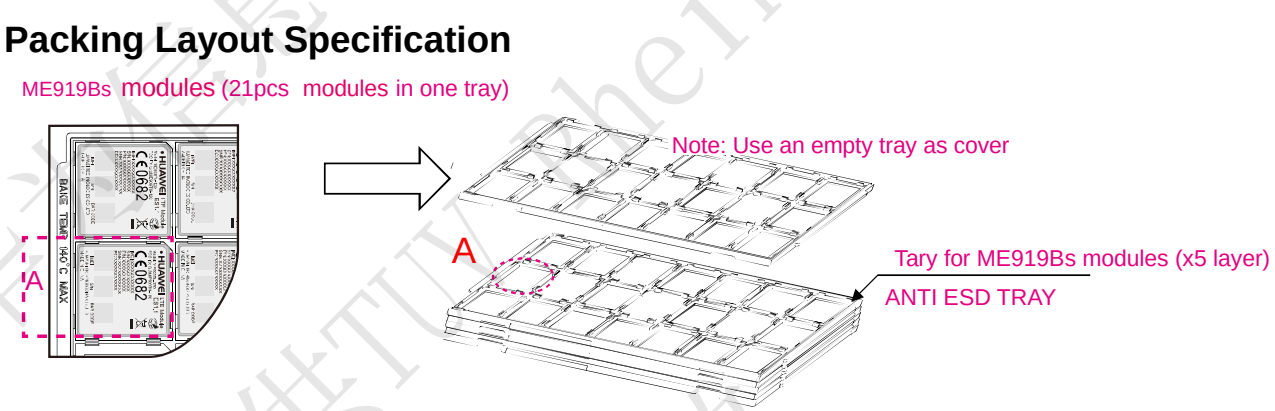


Figure 6-4 ESD packaging

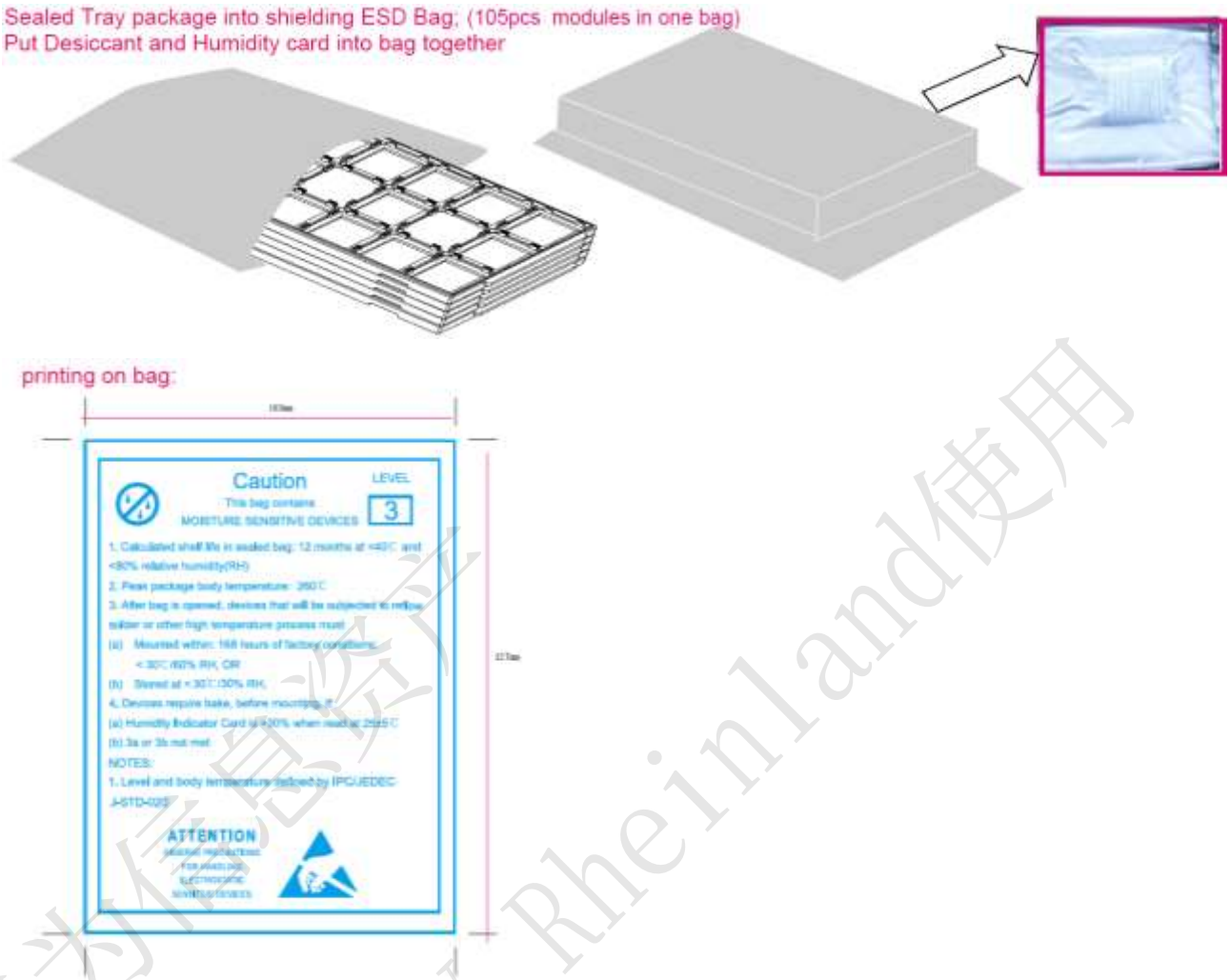


Figure 6-5 Sponge packaing

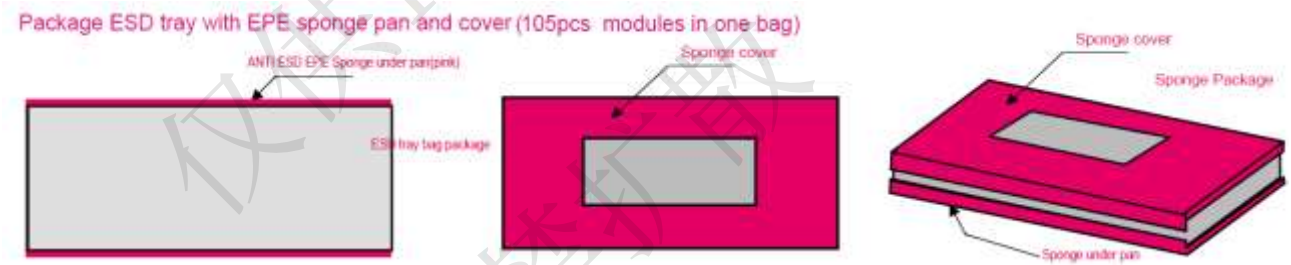


Figure 6-6 Medium carton packaging

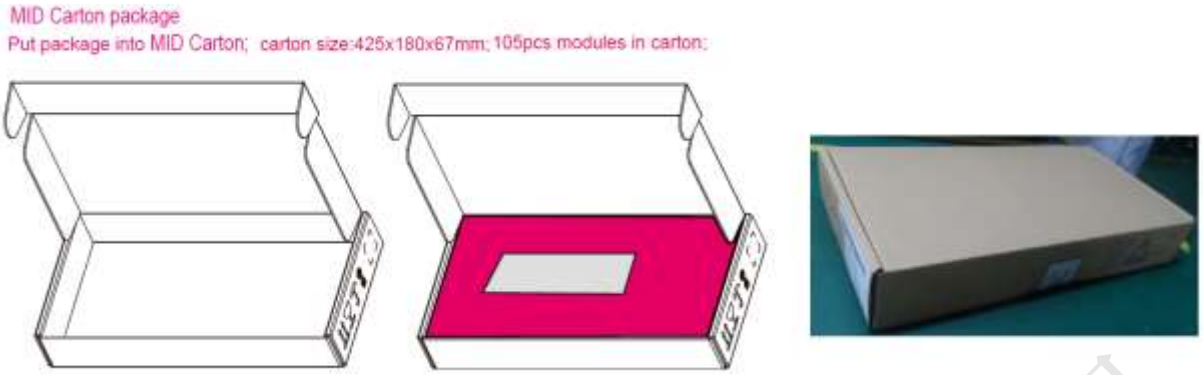


Figure 6-7 Large carton packaging

NOTE

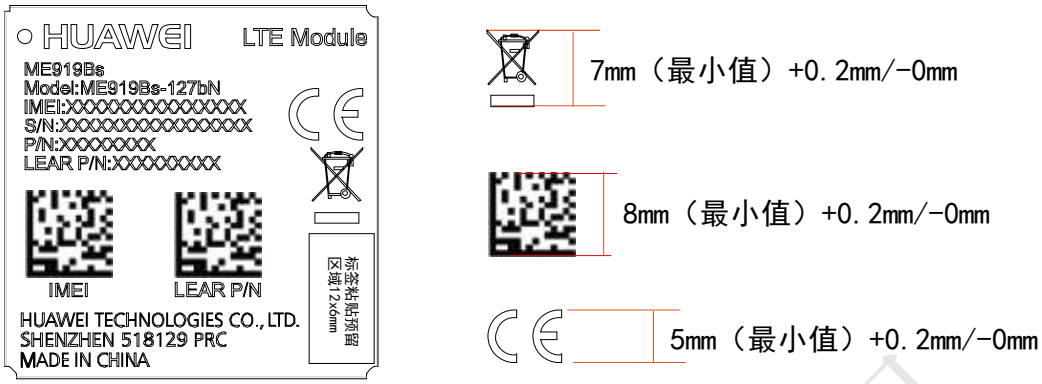
When unpacking:

- To avoid ESD damage, hands must not touch the module directly.
- Avoid the LGA pads contact other object to ensure there is no pollutant on the pads.
- Avoid unexpected drop.

6.6 Label

Laser carving is adopted on the module label.

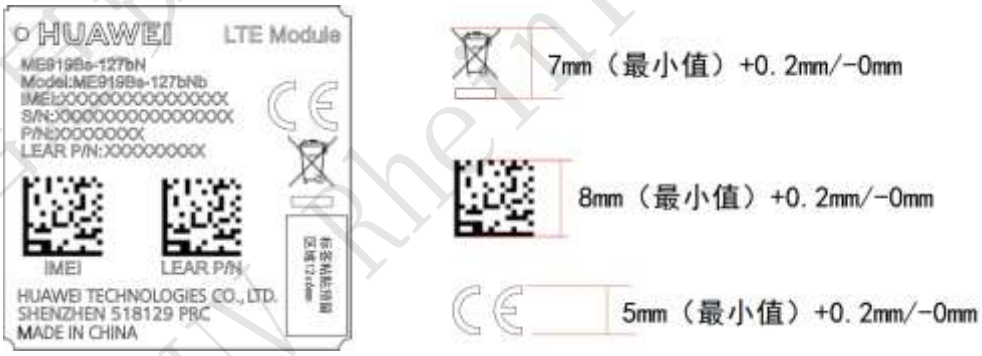
Figure 6-8 ME919Bs-127bN Label



NOTE

- S/N is HUAWEI serial number.
- P/N is HUAWEI part number.
- The picture mentioned above is only for reference.

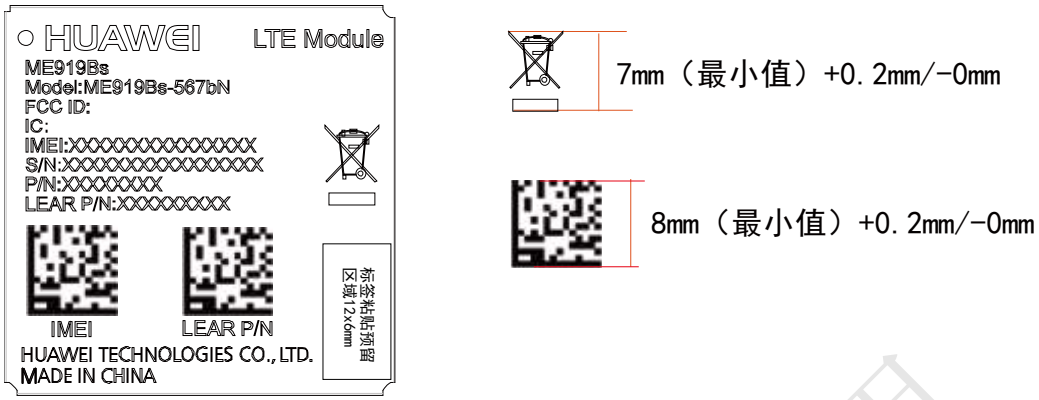
Figure 6-9 ME919Bs-127bNb Label



NOTE

- S/N is HUAWEI serial number.
- P/N is HUAWEI part number.
- The picture mentioned above is only for reference.

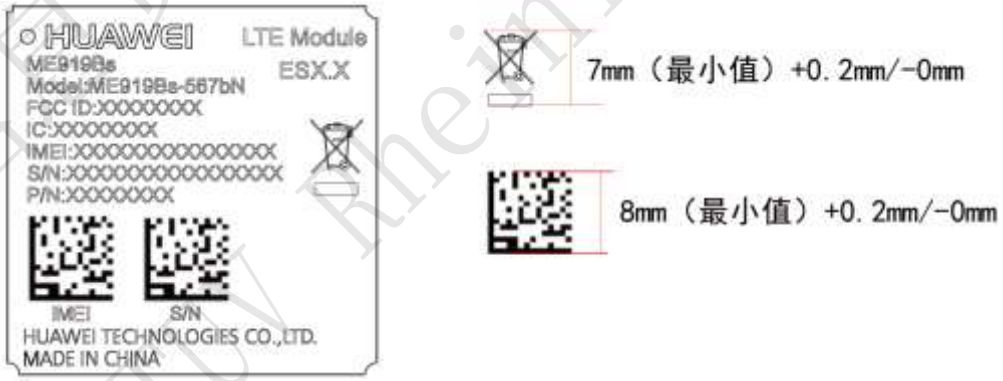
Figure 6-10 ME919Bs-567bN Label



NOTE

- S/N is HUAWEI serial number.
- P/N is HUAWEI part number.
- The picture mentioned above is only for reference.

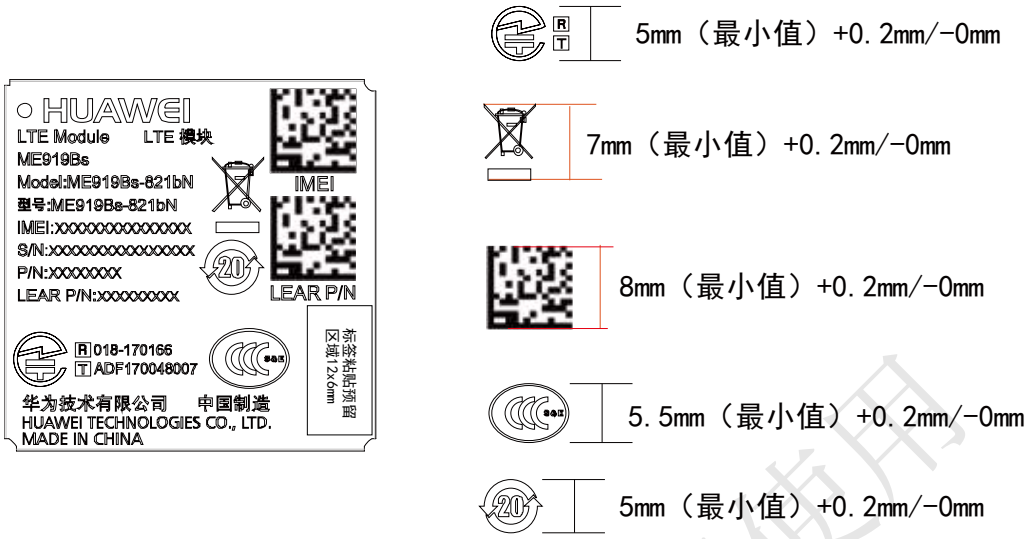
Figure 6-11 ME919Bs-567bNb Label



NOTE

- S/N is HUAWEI serial number.
- P/N is HUAWEI part number.
- The picture mentioned above is only for reference.

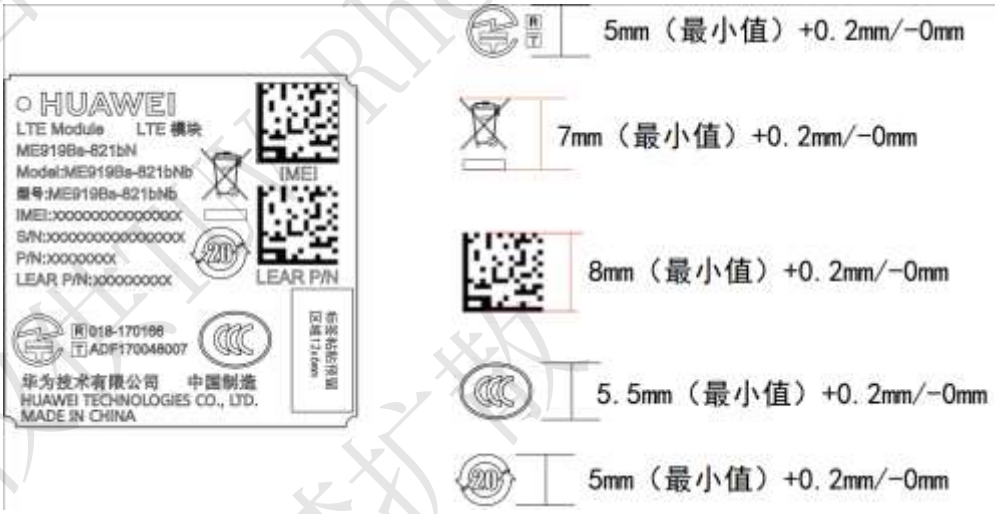
Figure 6-12 ME919Bs-821bN Label



NOTE

- S/N is HUAWEI serial number.
- P/N is HUAWEI part number.
- The picture mentioned above is only for reference.

Figure 6-13 ME919Bs-821bNb Label



NOTE

- S/N is HUAWEI serial number.
- P/N is HUAWEI part number.
- The picture mentioned above is only for reference.

6.7 Customer PCB Design

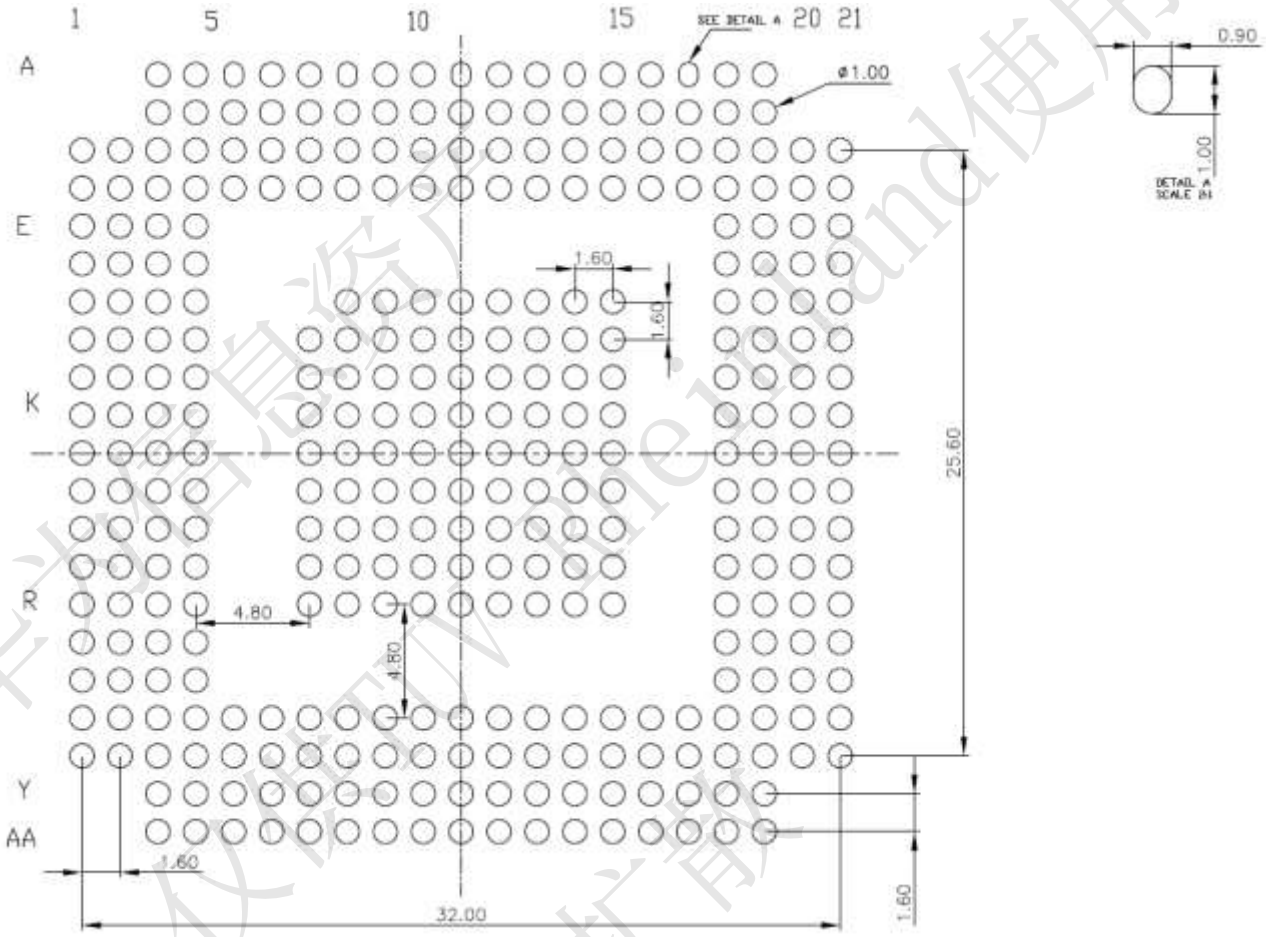
6.7.1 PCB Surface Finish

The PCB surface finish recommended is ENIG (Electroless Nickel Immersion Gold). OSP (Organic Solderability Preservative) may also be used, but ENIG is priority.

6.7.2 PCB Pad Design

To achieve assembly yields and solder joints of high reliability, it is recommended that the PCB pad size be designed as follows:

Figure 6-14 ME919Bs Series LTE LGA module Footprint design (unit: mm)



TOP PERSPECTIVE VIEW

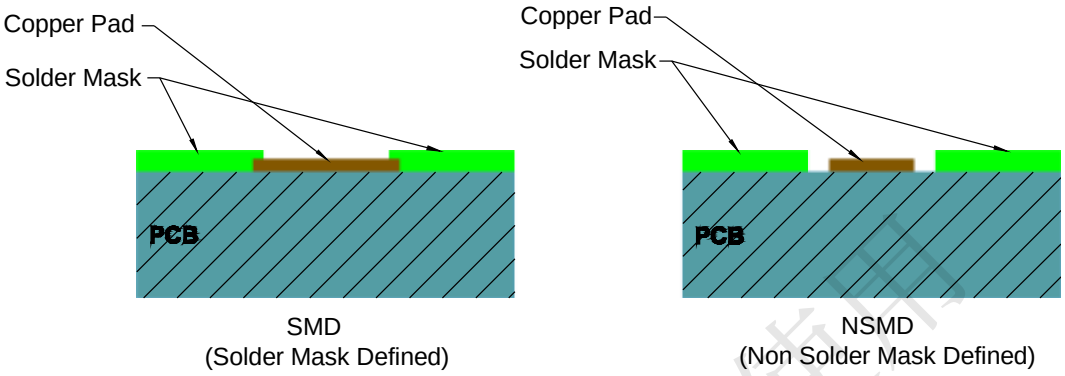
NOTES:RF PIN*5:A5 A8 A11 A14 A17(DETAIL A)

6.7.3 Solder Mask

NSMD (Non Solder Mask Defined) is recommended. In addition, the solder mask of the NSMD pad design is larger than the pad so the reliability of the solder joint can be improved.

The solder mask must be 100–150 μm larger than the pad, that is, the single side of the solder mask must be 50–75 μm larger than the pad. The specific size depends on the processing capability of the PCB manufacturer.

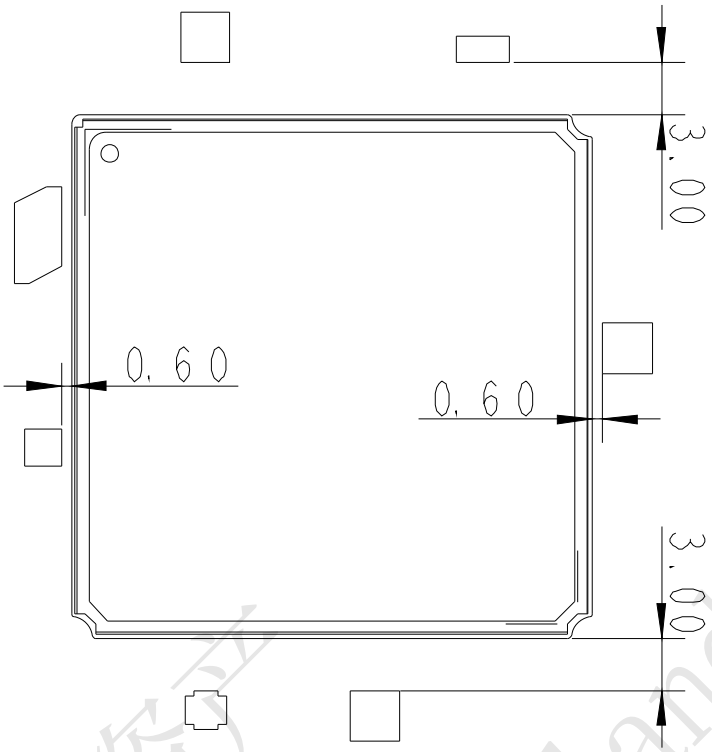
Figure 6-15 Solder Mask design



6.7.4 Requirements on PCB Layout

- To reduce deformation, a thickness of PCB at least 1.0 mm is recommended.
- Other devices must be located more than 3 mm (5 mm recommended) away from the two parallel sides of the LGA module (rework requirement), and other sides with 0.6 mm. The minimum distance between the LGA module and the PCB edge is 0.3 mm.
- When the PCB layout is double sided, the module must be placed on the second side for assembly so as to avoid module dropped from PCB or component (located in module) re-melding defects caused by uneven weight.

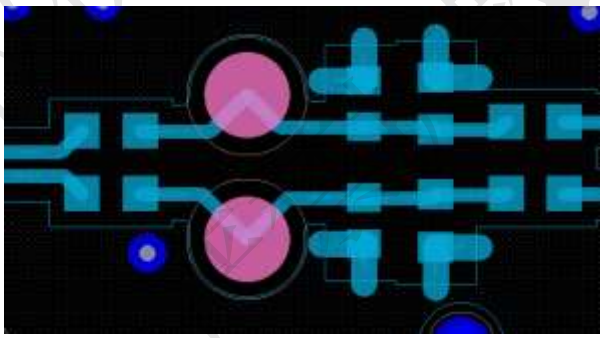
Figure 6-16 PCB Layout (unit: mm) (Top View)



USB Layout guides are as below:

1. The differential impedance of USB2.0 should meet 90 Ω+/-10%.
2. The skew of USB20_DP/USB20_DM is less than 20 mil.
3. Add test pad on USB2.0 differential signals for test requirement if necessary, and suggest following the rules below:
   - Test pad is as small as possible (recommended diameter 24 mil), two pads are as close as possible (suggest center distance 50 mil).
   - Test pad is on USB2.0 trace, don't rout stub from USB2.0 differential pair trace to connect test pad.
   - Ensure that the immediate ground plane layer under the test point is void.

Figure 6-17 USB2.0 test pad routing suggestion



SDIO Layout guides are as below:

1. The air gap between CLK trace and data/control trace should be more than 15 mil, the air gap between data trace to data/control trace should be more than 10mil for SDIO bus.
2. Suggest the skew of data/control to CLK should be less than 200 mil and 300 mil for SDIO3.0 and SDIO2.0 respectively.

PCIe Layout guides are as below:

1. The differential impedance of PCIE0 and PCIE1 should meet 100 Ω+/-10%.
2. The skew of differential pair N and P should be less than 5 mil, PCIE0 and PCIE1 are the same.
3. Suggest the trace air gap between TX, RX and CLK differential pair is more than 35 mil, PCIE0 and PCIE1 are the same.

RGMII/MII Layout guides are as below:

1. The air gap between CLK trace and data/control trace should be more than 15 mil, the air gap between data trace and data/control trace should be more than 10 mil for RGMII/MII bus.
2. The acceptable skew of data/control to CLK should be on the base of timing analysis for RGMII/MII bus.
3. Damping resistor for TXD and TX_CLK should be near TXD and TX_CLK pad.

Blue area design guide on PCB Layout:

Figure 6-18 Recommended Routing Keep-out area design of PCB Layout (Top View)

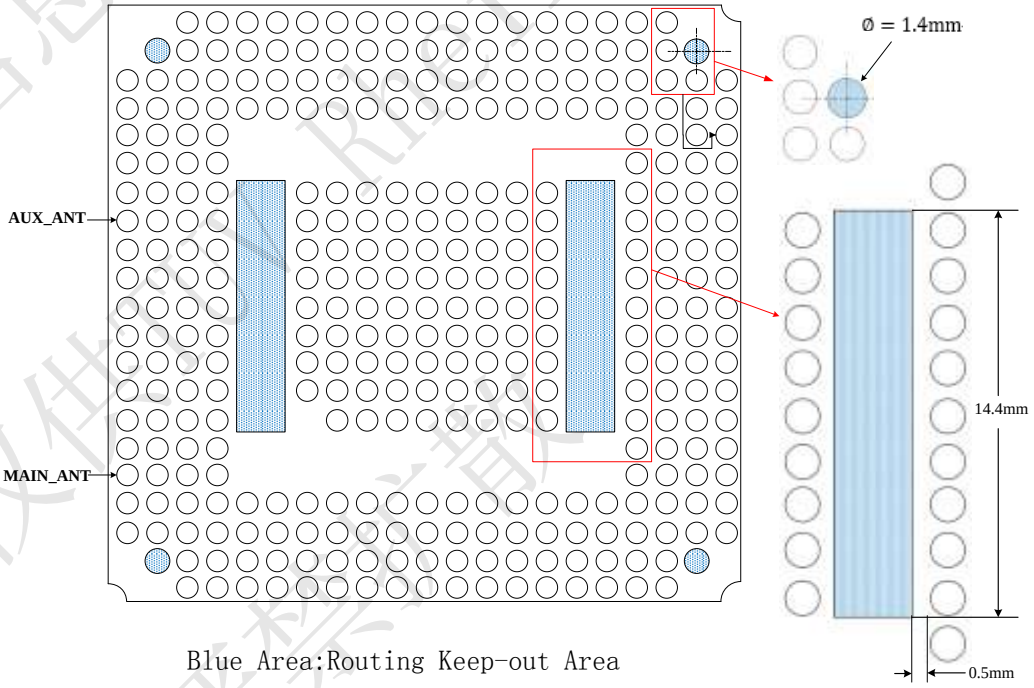


Figure 6-18 shows the recommended Routing Keep-out area design of PCB Layout (Top View).

NOTE

Do not layout signal vias in this area, because there are GND pins on module side. If user requires to layout signal vias in the area, fill the via hole with solder mask. If user layouts GND vias in the area, there will be no problem.

6.8 Thermal Design Solution

When the module works in the maximum power condition, the module has high power consumption (for details, see 5.5.2). To improve the module reliability and stability, focus on the thermal design of the device to speed up heat dissipation. For thermal characteristics of the ME919Bs LGA module, you can refer to Operating and Storage Temperatures and Humidity.

Take the following heat dissipation measures:

- The copper size on the PCB should be 75 mm x 75 mm or larger.
- All copper ground layers of the PCB must be connected to each other through via-holes.
- Increase the quantity of the PCB ground planes.
- The ground planes should be as continuous as possible.
- If a fan is deployed, place the module at the cold air inlet.
- Use heat sink, thermal conductive material and product enclosure to enhance the heat dissipation of the module.
  - Use anodized heat sink on the shielding case or the customer PCB on bottom side for optimal heat dissipation. The recommended heat sink dimensions are 75 mm x 75 mm x1.2 mm or larger.
  - The material of the heat sink should adopt the higher thermal conductivity metallic materials, e.g. Al or Cu.
  - The recommended thermal conductivity of the thermal conductive material is 1.0 W/m-k or higher (recommended manufacturers: Laird or Bergquist).
  - Conductive material should obey the following rule: after the heat sink is fastened to the shielding case, the compression amount of the thermal conductive material accounts for 15% to 30% of the thermal conductive material size.
  - Conductive material should be as thin as possible.
  - The recommended material of the enclosure is metallic materials, especially you can add pin fin on the enclosure surface.
  - If the heat sink is installed above the shielding case, you should attach the thermal conductive material between the shielding case and the heat sink; if the heat sink is installed below the bottom side of the customer PCB, you should attach the thermal conductive material between the customer PCB and the heat sink, as shown in Figure 6-19 and Figure 6-20 . Preferably, we recommend the heat sink be installed below the bottom side of the customer PCB.
  - Use more pin fins to enlarge heat dissipation area.

Figure 6-19 Adding heat sink to the module for optimal heat dissipation

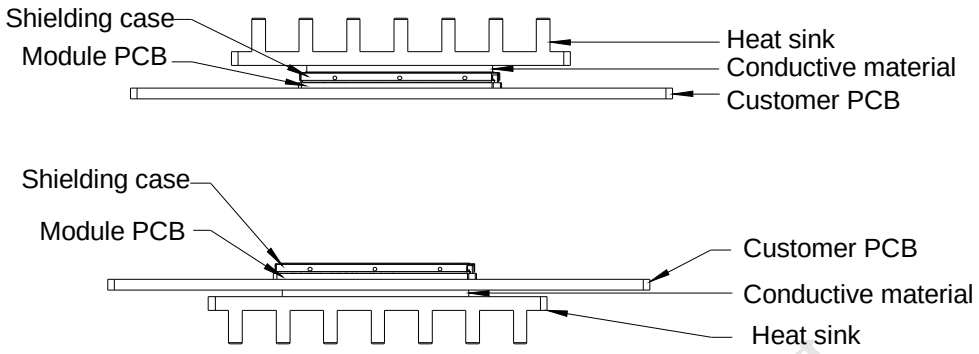
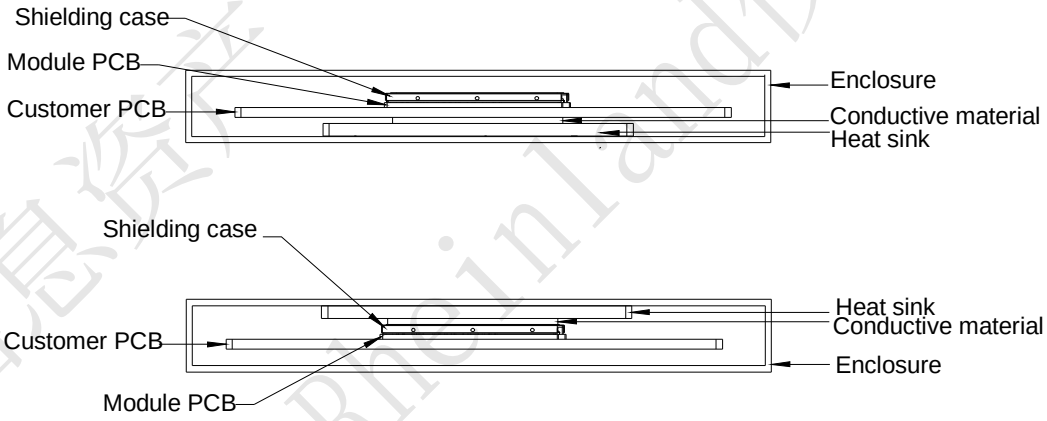


Figure 6-20 Adding enclosure to enhance the heat dissipation of the module



6.9 Assembly Processes

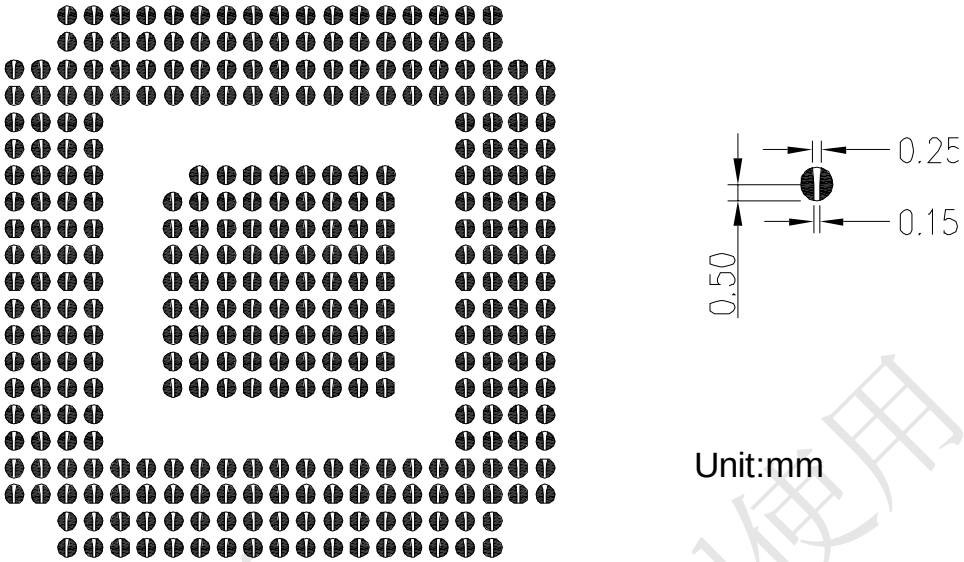
6.9.1 Overview

- Tray modules are required at SMT lines, because LGA modules are placed on ESD pallets.
- Reflow ovens with at least seven temperature zones are recommended.
- Use reflow ovens or rework stations for soldering, because LGA modules have large solder pads and cannot be soldered manually.

6.9.2 Stencil Design

It is recommended that the stencil for the LGA module be 0.15 mm in thickness. For the stencil design, see Figure 6-21 .

Figure 6-21 Recommended stencil design of LGA module (Unit: mm)



NOTE

The stencil design has been qualified for HUAWEI motherboard assembly, customers can adjust the parameters by their motherboard design and process situation to assure LGA soldering quality and no defect.

6.9.3 Reflow Profile

The module can only be reflowed once. For the soldering temperature of the LGA module, see Figure 6-22 .

Figure 6-22 Reflow profile

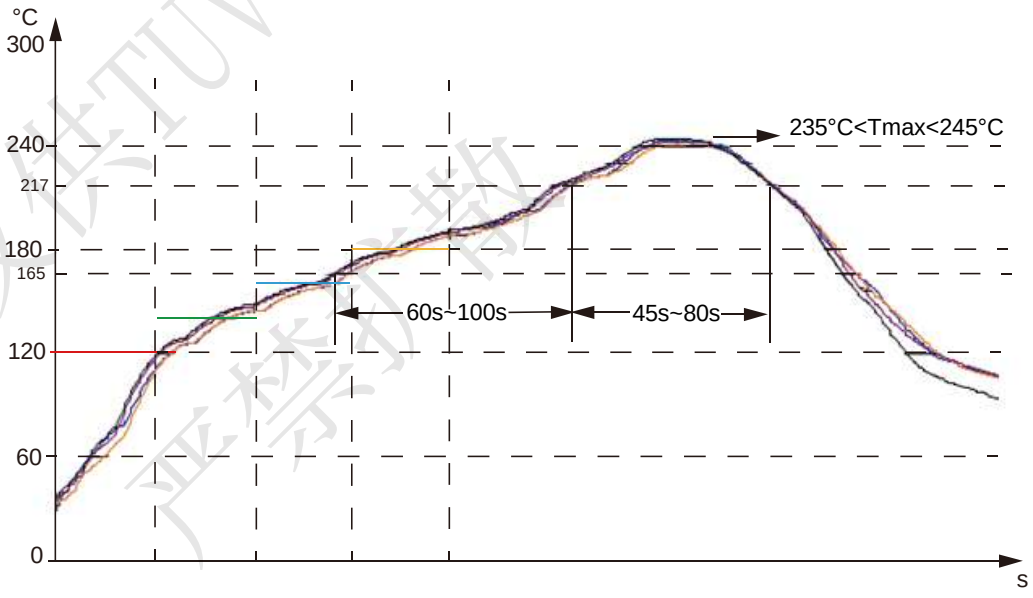
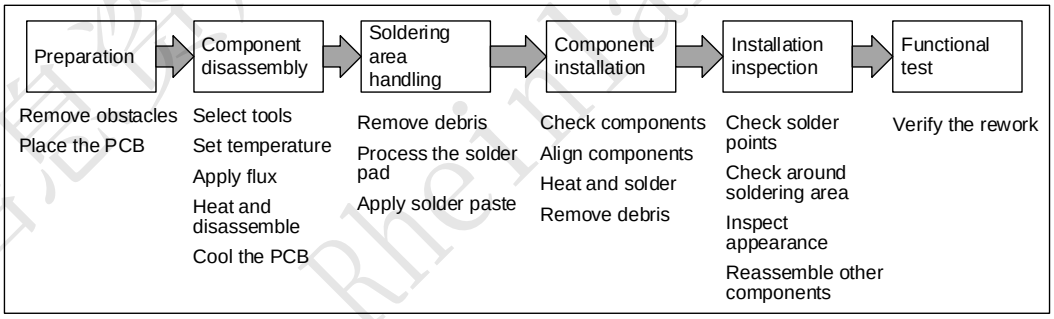


Table 6-2 Reflow parameters

Temperature Zone	Time	Key Parameter
Preheat zone (40–165°C)	-	Heating rate: 0.5–2°C/s
Soak zone (165–217°C)	(t1–t2): 60–100s	-
Reflow zone (> 217°C)	(t3–t4): 45–80s	Peak reflow temperature: 235–245°C
Cooling zone	Cooling rate: 2°C/s ≤ Slope ≤ 5°C/s	

6.10 Specification of Rework

6.10.1 Process of Rework



6.10.2 Preparations of Rework

- Remove barrier or devices that can't stand high temperature before rework.
- If the device to be reworked is beyond the storage period, bake the device according to Table 6-1 .

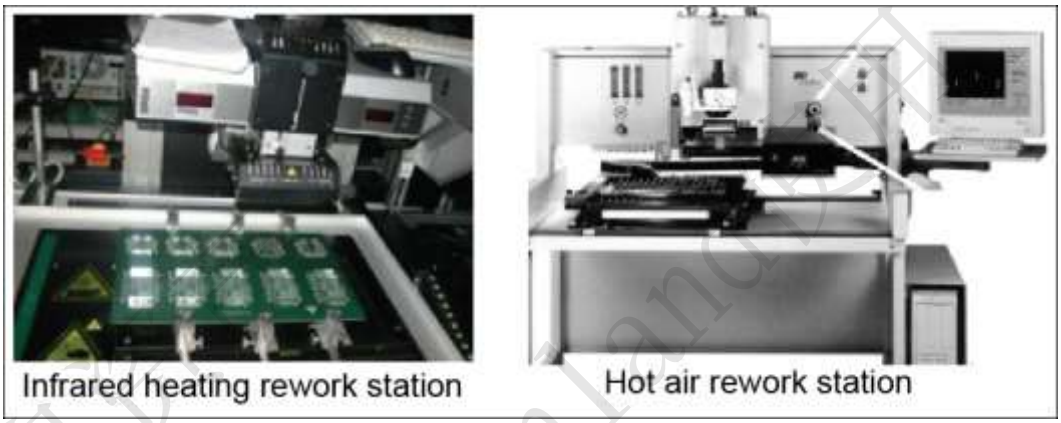
6.10.3 Removing of the Module

The solder is molten and reflowed through heating during the module removing process. The heating rate must be quick but controllable in order to melt all the solder joints simultaneously. Pay attention to protect the module, PCB, neighboring devices, and their solder joints against heating or mechanical damages.

NOTE

- The LGA module has many solder pads and the pads are large. Therefore, common soldering irons and heat guns cannot be used in the rework. Rework must be done by using either infrared heating rework stations or hot air rework stations. Infrared heating rework stations are preferred, because they can heat components without touching them. In addition, infrared heating rework stations produce less solder debris and less impact on modules, while hot air rework stations may cause shift of other components not to be reworked.
- You must not reuse the module after disassembly from PCB during rework.
- It is proposed that a special clamp is used to remove the module.

Figure 6-23 Equipment used for rework



6.10.4 Welding Area Treatment

Step 1 Remove the old solder by using a soldering iron and solder braid that can wet the solder.

Step 2 Clean the pad and remove the flux residuals.

Step 3 Solder pre-filling.

Before the module is installed on a board, apply some solder paste to the pad of the module by using the rework fixture and stencil or apply some solder paste to the pad on the PCB by using a rework stencil.

NOTE

It is recommended that a fixture and a mini-stencil should be made to apply the solder paste in the rework.

6.10.5 Module Installation

Install the module precisely on the Motherboard and ensure the right installation direction of the module and the reliability of the electrical connection with the PCB. It is recommended that the module be preheated in order to ensure that the temperature of all parts to be soldered is uniform during the reflow process. The solder quickly reflows upon heating so the parts are soldered reliably. The solder joints undergo proper reflow duration at a preset temperature to form a favorable Inter-metallic Compound (IMC). During the module SMT installation, it is recommended to install the module by recognizing the module pad, not by recognizing the module outline.

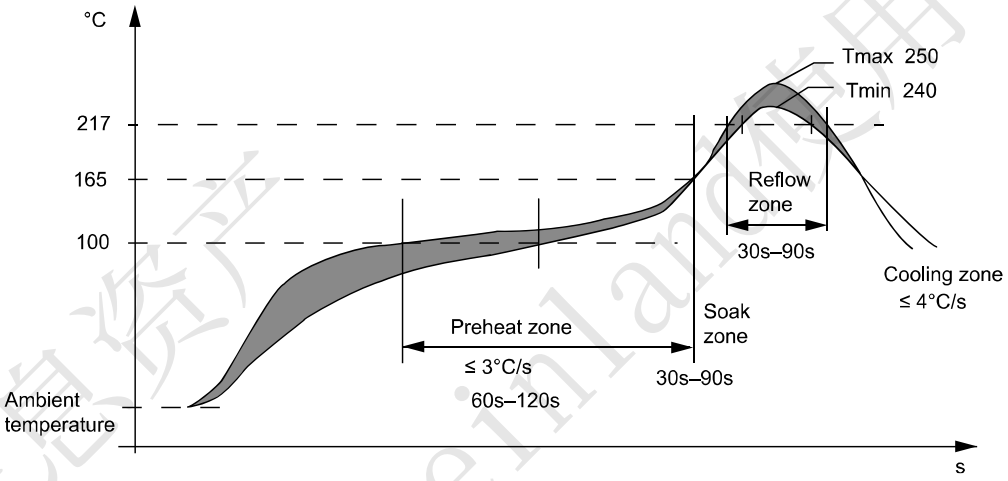
NOTE

- It is recommended that a special clamp be used to pick the module when the module is installed on the pad after applied with some solder.
- A special rework device must be used for the rework.

6.10.6 Specifications of Rework

Temperature parameter of rework: for either removing or welding the module, the heating rate during the rework must be equal to or smaller than 3°C/s, and the peak temperature should be in the range of 240°C to 250°C. The following parameters are recommended during the rework.

Figure 6-24 Temperature graph of rework



7 Certifications

7.1 About This Chapter

This chapter gives a general description of certifications of the module.

7.2 Certifications

NOTE

Table 7-1 –Table 7-3 show certifications of the module have been implemented. For more demands, please contact us for more details about this information.

Table 7-1 Product certifications of ME919Bs-127bN/bNb

Certification	Status
GCF	√
CE	√

Table 7-2 Product certifications of ME919Bs-567bN/bNb

Certification	Model name
FCC	√
IC	√
PTCRB	√

Table 7-3 Product certifications of ME919Bs-821bN/bNb

Certification	Model name
CCC	√
KCC	√
Jate	√

Certification	Model name
Telec	√

8 Safety Information

Read the safety information carefully to ensure the correct and safe use of your wireless device. Applicable safety information must be observed.

8.1 Interference

Power off your wireless device if using the device is prohibited. Do not use the wireless device when it causes danger or interference with electric devices.

8.2 Medical Device

- Power off your wireless device and follow the rules and regulations set forth by the hospitals and health care facilities.
- Some wireless devices may affect the performance of the hearing aids. For any such problems, consult your service provider.
- Pacemaker manufacturers recommend that a minimum distance of 15 cm be maintained between the wireless device and a pacemaker to prevent potential interference with the pacemaker. If you use an electronic medical device, consult the doctor or device manufacturer to confirm whether the radio wave affects the operation of this device.

8.3 Area with Inflammables and Explosives

To prevent explosions and fires in areas that are stored with inflammable and explosive devices, power off your wireless device and observe the rules. Areas stored with inflammables and explosives include but are not limited to the following:

- Gas station
- Fuel depot (such as the bunk below the deck of a ship)
- Container/Vehicle for storing or transporting fuels or chemical products
- Area where the air contains chemical substances and particles (such as granule, dust, or metal powder)
- Area indicated with the "Explosives" sign

- Area indicated with the "Power off bi-direction wireless equipment" sign
- Area where you are generally suggested to stop the engine of a vehicle

8.4 Traffic Security

- Observe local laws and regulations while using the wireless device. To prevent accidents, do not use your wireless device while driving.
- RF signals may affect electronic systems of motor vehicles. For more information, consult the vehicle manufacturer.
- In a motor vehicle, do not place the wireless device over the air bag or in the air bag deployment area. Otherwise, the wireless device may hurt you owing to the strong force when the air bag inflates.

8.5 Airline Security

Observe the rules and regulations of airline companies. When boarding or approaching a plane, power off your wireless device. Otherwise, the radio signal of the wireless device may interfere with the plane control signals.

8.6 Safety of Children

Do not allow children to use the wireless device without guidance. Small and sharp components of the wireless device may cause danger to children or cause suffocation if children swallow the components.

8.7 Environment Protection

Observe the local regulations regarding the disposal of your packaging materials, used wireless device and accessories, and promote their recycling.

8.8 WEEE Approval

The wireless device is in compliance with the essential requirements and other relevant provisions of the Waste Electrical and Electronic Equipment Directive 2012/19/EU (WEEE Directive).

8.9 RoHS Approval

The wireless device is in compliance with the restriction of the use of certain hazardous substances in electrical and electronic equipment Directive 2011/65/EU (RoHS Directive).

8.10 Laws and Regulations Observance

Observe laws and regulations when using your wireless device. Respect the privacy and legal rights of the others.

8.11 Care and Maintenance

It is normal that your wireless device gets hot when you use or charge it. Before you clean or maintain the wireless device, stop all applications and power off the wireless device.

- Use your wireless device and accessories with care and in clean environment. Keep the wireless device from a fire or a lit cigarette.
- Protect your wireless device and accessories from water and vapour and keep them dry.
- Do not drop, throw or bend your wireless device.
- Clean your wireless device with a piece of damp and soft antistatic cloth. Do not use any chemical agents (such as alcohol and benzene), chemical detergent, or powder to clean it.
- Do not leave your wireless device and accessories in a place with a considerably low or high temperature.
- Use only accessories of the wireless device approved by the manufacture. Contact the authorized service center for any abnormity of the wireless device or accessories.
- Do not dismantle the wireless device or accessories. Otherwise, the wireless device and accessories are not covered by the warranty.
- The device should be installed and operated with a minimum distance of 20 cm between the radiator and your body.

8.12 Emergency Call

This wireless device functions through receiving and transmitting radio signals. Therefore, the connection cannot be guaranteed in all conditions. In an emergency, you should not rely solely on the wireless device for essential communications.

8.13 Regulatory Information

8.13.1 EU Regulatory Conformance

Statement

Hereby, Huawei Technologies Co., Ltd. declares that this device is in compliance with the essential requirements and other relevant provisions of Directive 2014/53/EU.

The most recent and valid version of the DoC (declaration of conformity) can be viewed at http://consumer.huawei.com/certification.

This device may be operated in all member states of the EU.

Observe national and local regulations where the device is used.

This device may be restricted for use, depending on the local network.

Frequency Bands and Power

(a) Frequency bands in which the radio equipment operates: Some bands may not be available in all countries or all areas. Please contact the local carrier for more details.

(b) Maximum radio-frequency power transmitted in the frequency bands in which the radio equipment operates: The maximum power for all bands is less than the highest limit value specified in the related Harmonized Standard.

The frequency bands and transmitting power (radiated and/or conducted) nominal limits applicable to this radio equipment are as follows:

UMTS Band 1 TX/RX:1920–1980 MHz, 2110–2170 MHz, UMTS Band 8 TX/RX: 880–915 MHz, 925–960 MHz, GSM 900 TX/RX: 880–915 MHz, 925–960 MHz, DCS 1800 TX/RX: 1710–1785 MHz, 1805–1880 MHz, LTE Band 1 TX/RX: 1920–1980 MHz, 2110–2170 MHz, LTE Band 3 TX/RX: 1710–1785 MHz, 1805–1880 MHz, LTE Band 7 TX/RX: 2500–2570 MHz, 2620–2690 MHz, LTE Band 8 TX/RX: 880–915 MHz, 925–960 MHz, LTE Band 20 TX/RX: 832–862 MHz, 791–821 MHz, LTE Band 28 TX/RX: 703–748 MHz, 758–803 MHz, LTE Band 38 TX/RX: 2570–2620 MHz, 2570–2620 MHz, GPRS 900: 33 dBm [+/-2 dB], EDGE 900: 27 dBm [+/-3 dB], WCDMA 900/1800/2100: 24 dBm [+1/-3 dB], GPRS 1800: 30 dBm [+/-2 dB], EDGE 1800: 26 dBm [+/-3 dB], LTE B1/B3/B7/B8/B20/B28/B38: 23 dBm [+1/-3 dB].

Software Information

Software updates will be released by the manufacturer to fix bugs or enhance functions after the product has been released. All software versions released by the manufacturer have been verified and are still compliant with the related rules.

All RF parameters (for example, frequency range and output power) are not accessible to the user, and cannot be changed by the user.

For the most recent information about accessories and software, please see the DoC (declaration of conformity) at http://consumer.huawei.com/certification.

9 Acronyms and Abbreviations

Acronym or Abbreviation	Expansion
3GPP	Third Generation Partnership Project
8PSK	8 Phase Shift Keying
ADC	Analog To Digital Converter
AMPR	Additional Maximum Power Reduction
AP	Access Point
AUX	Auxiliary
BC	Band Class
BER	Bit Error Rate
BLER	Block Error Rate
BIOS	Basic Input Output System
CCC	China Compulsory Certification
CDMA	Code Division Multiple Access
CE	European Conformity
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CS	Circuit Switched
DC	Direct Current
DCE	Data Communication Equipment
DL	Down Link
DMA	Direct Memory Access
DTE	Data Terminal Equipment
DRX	Discontinuous Reception
DVK	Development Kit
ECC	Envelope Correlation Coefficient
EDGE	Enhanced Data Rate for GSM Evolution

Acronym or Abbreviation	Expansion
EIA	Electronic Industries Association
EMC	Electromagnetic Compatibility
ENIG	Electroless Nickel Immersion Gold
EPA	Electrostatic Discharge Protected Area
ESD	Electrostatic Discharge
EU	European Union
EVDO	Evolution Data Optimized
FCC	Federal Communications Commission
FDD	Frequency Division Duplex
GMSK	Gaussian Minimum Shift-frequency Keying
GPIO	General Purpose I/O
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
GLONASS	Global Navigation Satellite System
GNSS	Global Navigation Satellite System
HBM	Human Body Model
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSPA+	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IC	Integrated Circuit
ILPC	Inner Loop Power Control
IMC	Inter Metallic Compound
IMT	International Mobile Telephony
ISO	International Standards Organization
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array

Acronym or Abbreviation	Expansion
LPF	Low Pass Filter
LTE	Long Term Evolution
MCP	Multi Chip Package
MCS	Modulation and Coding Scheme
MPR	Maximum Power Reduction
MO	Mobile Originated
MT	Mobile Terminated
NC	Not Connected
NTC	Negative Temperature Coefficient
NSMD	Non Solder Mask Defined
OC	Open Collector
PA	Power Amplifier
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PID	Product Identity
PMIC	Power Management Integrated Circuit
PS	Packet Switched
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RH	Relative Humidity
RHCP	Right Hand Circular Polarization
RoHS	Restriction of the Use of Certain Hazardous Substances
RSE	Radiated Spurious Emission
RUIM	Removable User Identity Module
RX	Receive
SAW	Surface Acoustic Wave
SIMO	Single Input Multiple Output

Acronym or Abbreviation	Expansion
SMS	Short Message Service
SMT	Surface Mounting Technology
TBD	To Be Determined
TDD	Time Division Duplex
TIS	Total Isotropic Sensitivity
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Up Link
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VID	Vendor Identity
VPP	Voltage Programming Power
VSWR	Voltage Standing Wave Ratio
WEEE	Waste Electrical and Electronic Equipment
WCDMA	Wideband Code Division Multiple Access
WWAN	Wireless Wide Area Network