nanoNode Integration Specification

Preliminary

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nanoNode Integration Specification - Preliminary

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Revision History

Revision	Release Date	Change Description
X1	May 11, 2016	Initial release.
X2	June 3, 2016	■ Updated: ❒ Address ❒ WAKE definition ❒ Block diagram ❒ Antenna design ■ Clarified various other areas of the document.
X3	June 6, 2016	■ IC to ISED and other minor regulatory changes.

1 Overview

This document provides a brief overview of the RPMA™ Network as well as guidelines allowing an integrator to design a Host product that utilizes the nanoNode and ensures that the system meets all of its technical objectives and requirements.

1.1 RPMA™ Network

Ingenu has developed RPMA, a wireless technology providing the world's best coverage, capacity, long life, and interoperability for IOT devices. The RPMA Network is comprised of Nodes (end points with RF Modems) and Access Points (APs). The nanoNode is one variant of the Nodes offered by Ingenu. The nanoNode is designed to easily integrate, with the addition of an applications processor, with any sensor, enabling robust wireless communication with any AP. An AP typically provides coverage to up to 64K nodes with a footprint of 50-300 sqmi (75-450 sqkm). Ingenu is aggressively deploying the Machine Network ™, providing nationwide coverage in the US. A number of operators have licensed RPMA for global deployments (over 50 countries at the time of this writing). A nanoNode comes from the factory enabled to join any available network, worldwide.

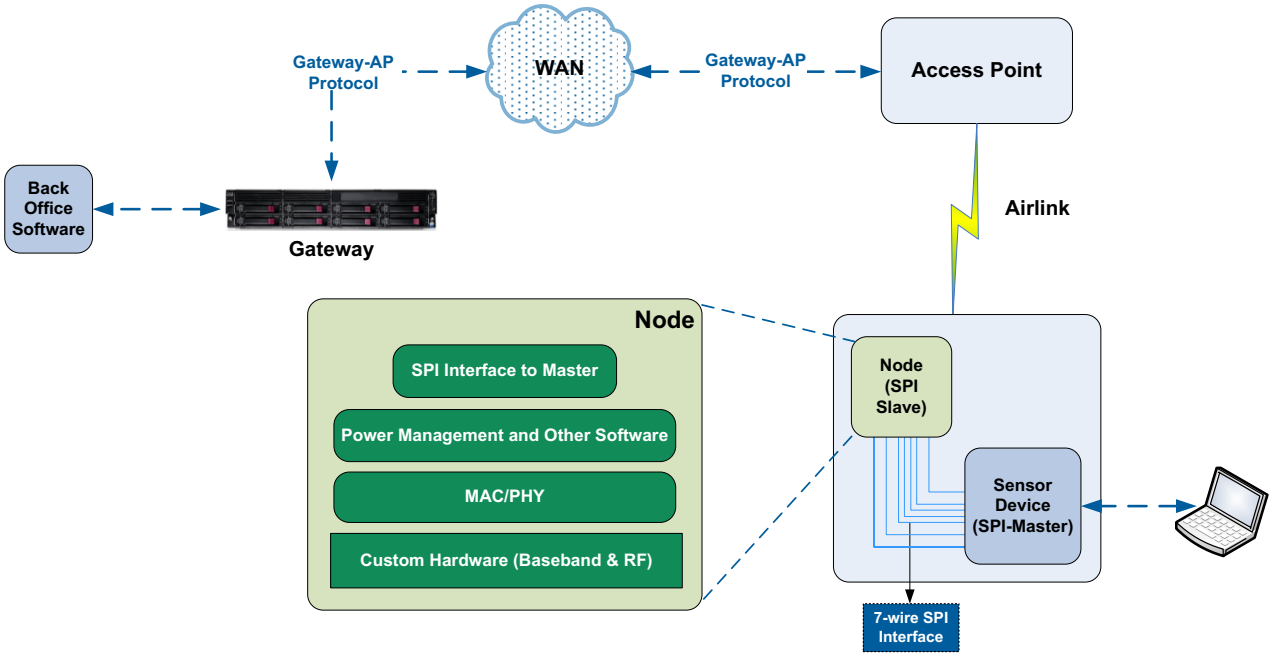


Figure 1. RPMA™ Network

1.2 nanoNode

The nanoNode is a small form factor wireless network module that easily integrates with a microcontroller or applications processor using a Serial Peripheral Interface (SPI). The top side of the printed circuit board (PCB) is enclosed with a radio frequency (RF) shield. The nanoNode

is an LGA-style module designed to be soldered directly onto a host board via SMT processes. For details, see Appendix B: PCB Land Pattern and Keepouts.

Table 1. nanoNode Specifications

nanoNode (PN 550-0083-00)	
Dimensions (per unit)	33.02 mm x 22.86 mm 1.3 inches x 0.9 inches
Weight (per unit)	5.36 grams (0 .190 ounces)
Transmit Power	+23.3 dBm (maximum)
RX Sensitivity	-133 dBm (nominal)

For more mechanical details about the nanoNode, refer to the mechanical drawing in Appendix G: nanoNode Mechanical Drawing. To order, use the part numbers provided above.

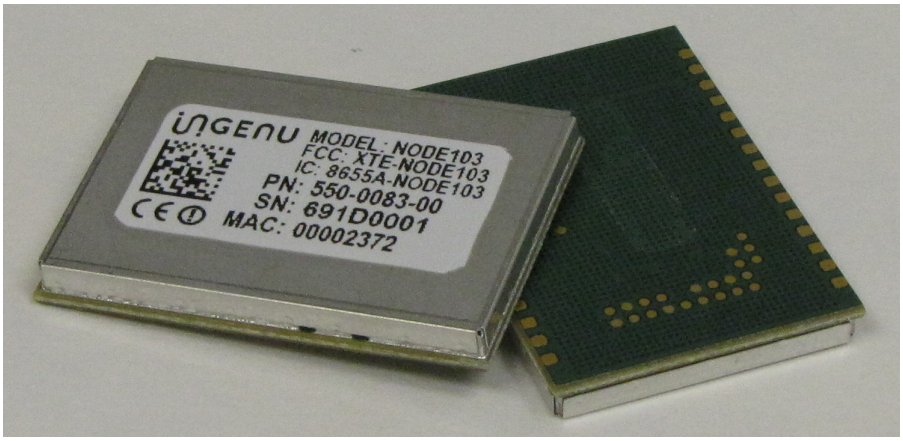


Figure 2. nanoNode (Top and Bottom Views)

The following figure shows how a nanoNode interfaces with a Host application, running on an applications processor.

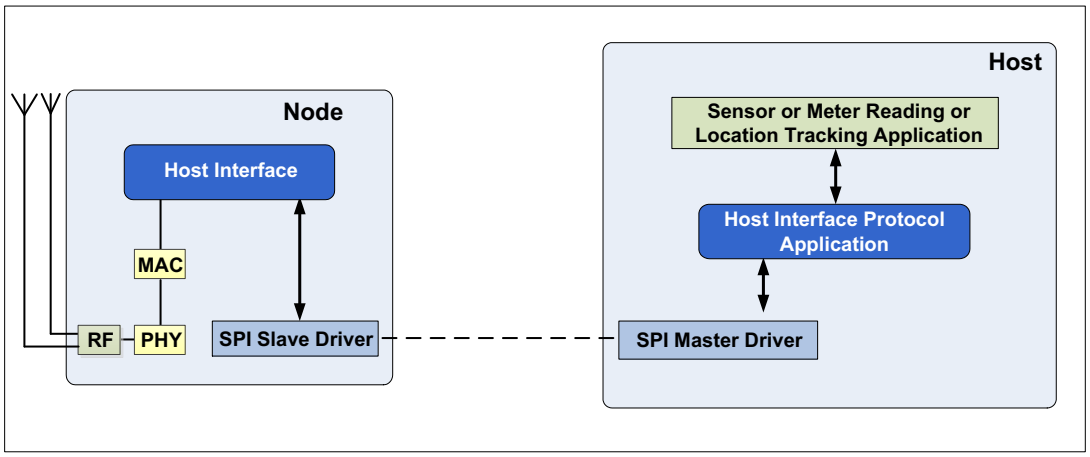


Figure 3. Typical Application Diagram

1.3 References/Tools

The following documents are referenced and provide more detail.

- **EMC Compliance Guide (010-0037-00)**
  Provides information for "driving" the Node through various modes in order to perform regulatory tests for FCC and ETSI.

  NOTE: The nanoNode is FCC modular certified. Many device partners have only been able to do a paper filing, rather than full compliance testing.

- **ATE Transmit Test Mode Guide (010-0089-00)**
  This guide provides commands for integrators to factory test the device's transmitter and antenna ports.

- **Provisioning Guide (010-0074-00)**
  Describes the function and use of the software packages used to configure a node for a target network. Note: in the near future the provisioning step will not be required for global and US public networks.

- **rACM Developer Guide (010-0105-00)**
  Describes the necessary steps to build, download, and test the reference Application Communication Module (rACM) software. It is used by external partners in the development of a sensor application on the reference host platform using RPMA™ technology. The rACM software serves as a design template and is optimized for very low power usage applications and battery-powered systems.

- **Host Common Software Integration Application Note (010-0024-00)**
  Describes the software interfaces and implementation considerations regarding the Host Common software component – a library of portable C code which facilitates all interactions between a host applications and an RPMA™ Network Node. Device partners compile in the Host Common library on their apps processor. It abstracts and handles all Host-to-Node communications.

- **rACM**
  The rACM is Ingenu's evaluation platform for the following types of Nodes:

  - rACM2 (550-0095-00) for nanoNode
  - rACM1 (550-0038-00) for microNode
  - rCAM1 (550-0038-00) for dNode

  The rACM platforms provide documentation, software, and ready-made binaries for the Node family of modems.

- **Application Note: Ethertronics 1001013 Antenna (010-0139-00)**
  Provides guidelines for design and layout for the Ethertronics 1001013 FR4-based surface mount antenna.

2 DC and AC Characteristics

2.1 Absolute Maximum Ratings

Operating outside of these ranges may damage the unit.

The nanoNode is MSL 3-rated and should be handled as an MSL 3 device per IPC/JEDEC J-STD-033 (latest revision). See section 11.3 for further information.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C
Vbatt Input Voltage	2.2	6.0	V
3.3V Supply	3.1	3.5	V
Digital Interface Signals, 3.3V nominal	3.0	3.6	V

2.2 Recommended Operating Conditions

Table 3. Operating Conditions

Parameter	Min	Max	Unit
Input voltage, VBATT	2.2	5.5	V
3.3V Input	3.2	3.4	V
Ambient Temperature, Ta	-40	85	°C

The following characteristics apply across the -40°C to +85°C temperature range unless otherwise noted.

Table 4. Operating Characteristics

Description	Min	Typ	Max	Units
DC Characteristics				
Voltage – Vbatt	2.2	3.3	5.5	Volt
Off Current – Note 1	0.05	0.1	2.0	µA
Deep Sleep Current - Note 1	10	15	30	µA
Idle Current – Note 1	10	15	22	mA
Receive Current – Note 1	75	85	90	mA
nanoNode: Transmit Current – Note 2	200	245	300	mA

Description	Min	Typ	Max	Units
Digital				
VOL – Voltage Output, Low (4mA sink)	0		0.4	V
VOH – Voltage Output High (4mA source)	2.4		3.3	V
SPI Clock – Note 11	0.1		8.6	MHz
Environmental				
Operating Temperature	-40		+85	°C
Storage Temp	-40		+85	°C
Humidity – non-condensing	5		95	%
Ramp Temperature (maximum rate at which operating temperature should change)			30	°C/Hr.
MTBF (nanoNode)		6.4		MHrs
Receiver				
Receiver Sensitivity – Note 3	-130	-133	-135	dBm
Receiver Image Reject	38	45	50	dB
Noise Figure	3.5	4.8	5.5	dB
Input IP3 (high LNA gain mode)		-11		dBm
Maximum RF input level for specification compliance			-20	dBm
General RF Characteristics				
Frequency Range – Note 4	2402		~2482	MHz
Channel Spacing	N/A	1.99	N/A	MHz
Transmitter				
Maximum RF Conducted Power –Note 5 FCC/IC markets: ETSI markets:	 8.5	 23.3 9.5	 10.0	 dBm dBm
Carrier Rejection	-35	-40	-50	dBc
Signal Modulation		DSSS-DBPSK		
Signal Bandwidth		1.0		MHz
BT Factor		0.3		
Peak to Average Ratio		2.3		dB
Spectral bandwidth at maximum RF power: -6dB BW -20dB BW		 0.96 1.75		 MHz MHz
ACPR – Note 6			-30	dBc
Harmonics – Note 7			-43	dBm
Transmit Power Level Accuracy – Note 8			±1.5	dB

Description	Min	Typ	Max	Units
Transmitter Spurious Outputs – Note 9 30MHz to 2400MHz: 2482MHz to 8000MHz:			 < -43 < -43	 dBm dBm
VSWR Tolerance Maximum VSWR for spec compliance – Note 10: Maximum VSWR for stability.			 1.5:1 9:1	

NOTES:

1. Tested at 3.3V input, +25C. Please note the following:
   a. There are power differences between the Voltage/Current numbers in this table and the data provided in Figure 4, Figure 5, and Figure 6. These figures show representative characterization of Power over Voltage/Temperature characterization and are representative behavior.
   b. The Table 4 refers to a maximal current draw that the Host system should be designed to accommodate.
2. Measured at:
   - nanoNode: +23.3 dBm TX output (Typ=50Ω), 3.3 V, range includes VSWR ≤ 1.5:1 (Po not compensated).
3. Sensitivity at maximum DL spreading factor of 11 (2048) with 10% FER.
4. The upper frequency range is market dependent:
   a. FCC/ISED: CH38; 2475.63 MHz.
   b. ETSI: CH40; 2475.63 Hz.
   c. Japan: CH41; 2481.60 MHz.
5. Maximum TX RF power:
   nanoNode: This is limited by FCC/IC grant to 23.3 dBm in these markets. Transmit power is configured during network join time to meet country-specific deployment and regulatory requirements. The configurable range is 0 – 23.3 dBm in 1 dB integer increments. For non-integer Power such as 23.3dBm, the Node's MAX_TX Power must be set to 24dBm to force a maximum calibrated value.
6. Spec and test method comes from FCC 15.247(d); Band Edge Emissions, 2 MHz offset.
7. At any TX power level, VSWR ≤ 3:1. Harmonics fall into FCC restricted bands.
8. Estimated sum of all contributors with VSWR ≤ 1.5:1. Normal link mode.
9. At any TX power level, VSWR ≤ 3:1. Applies to spurious, not ACPR or harmonics. Generally the largest spurious output outside the 2.40-2.48GHz band is at 2/3LO and 4/3LO.
10. Maximum VSWR for spec compliance applies at 25°C only. Slightly degraded ACPR/mask and power variation can be expected at temperature extremes.
11. The SPI clock has a maximum rate of 26 MHz/3 and a minimum of 100 kHz. There is no physical limitation on the minimum clock rate but the 100 kHz is deemed "marginal" and is not absolute. Depending on the data traffic model and level of debug traffic, 100 kHz may cause a backup of SPI traffic, which then causes buffer overflow conditions. The application must be validated to ensure that the SPI clock is sufficient to support required traffic.

2.3 Effects of Temperature and Voltage

The nanoNode is based largely on Complementary Metal–Oxide–Semiconductor (CMOS) technology. The current drain of CMOS circuitry can vary substantially over Temperature. The RF circuitry and its performance also vary substantially over Temperature.

The nanoNode utilizes two main power domains:

1. VBATT - 2.2-5.5V.

   This Powers the low current supervisory/housekeeping circuitry of the node, used while the node is asleep. This voltage supply must be continuous, not under software control. The node autonomously wakes up and synchronizes to the network periodically, without any knowledge by the host apps processor. Figure 4 shows the effect of VBatt on deep sleep power consumption.

2. 3.3V Supply

   This domain needs a 3.3V input when WAKE is asserted "High." This power domain is used for a majority of processing, transceiver, and RF Power Amplifier circuitry within the Node. These blocks require a lot of power compared to the VBATT domain and the Node asserts WAKE only when this power (voltage) is required.

The following graphs show the relative differences across the operating voltages and their effect on current consumption.

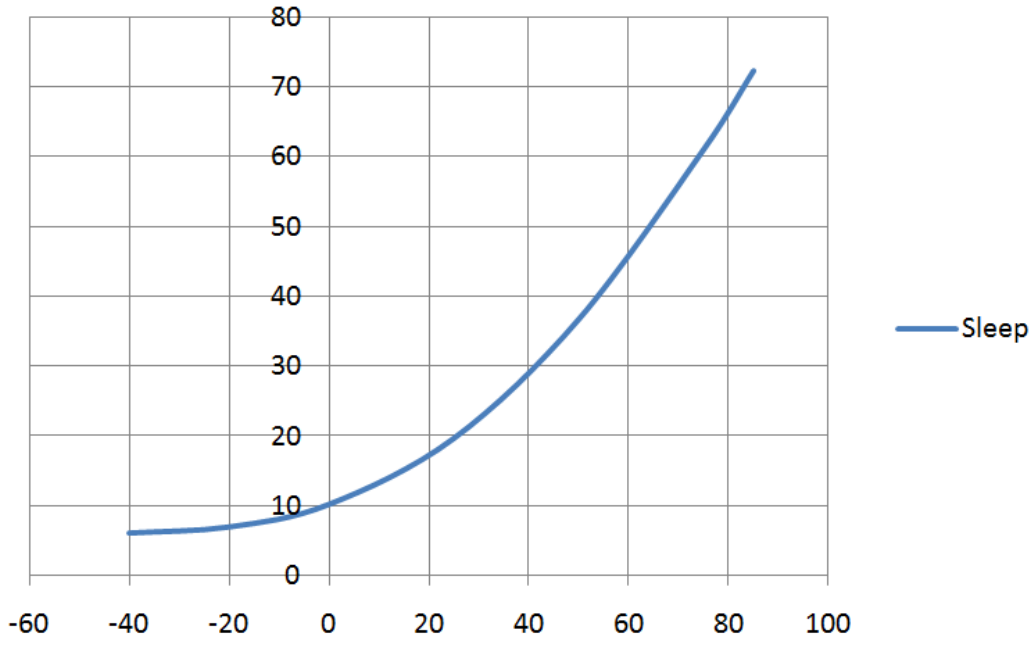


Figure 4. Sleep Current (µA) vs Temperature (°C) at 3.3V Input

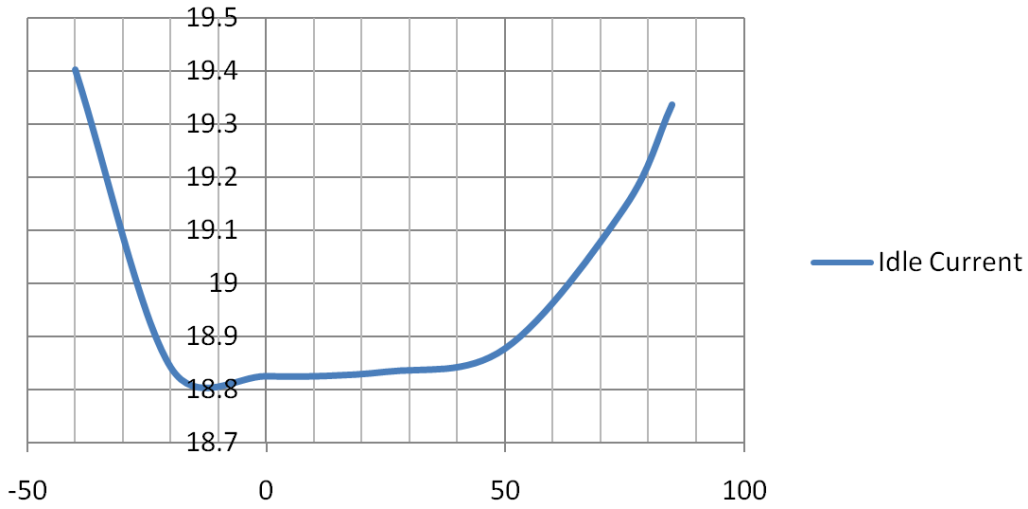


Figure 5. Idle Current (mA) vs Temperature (°C) at 3.3V Input

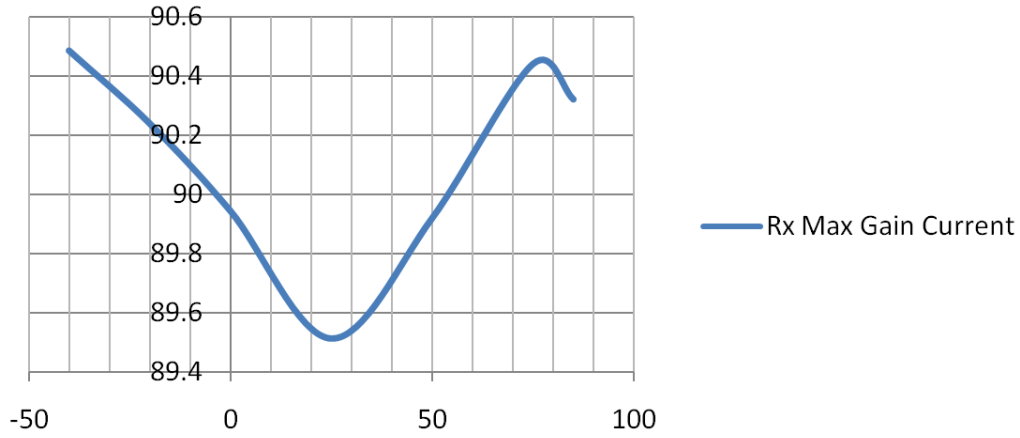


Figure 6. Max Rx Gain Current (mA) vs Temperature (°C) at 3.3V Input

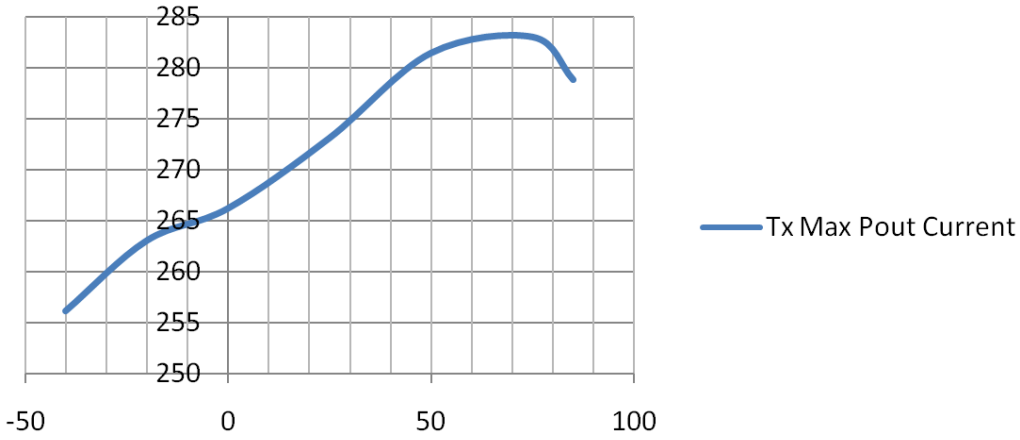


Figure 7. Max Tx (23.3 dBm) Current (mA) vs Temperature (°C) at 3.3V Input

3 Electrical Interface

This chapter describes the electrical interface of the nanoNode and how the Host processor controls for the nanoNode.

NOTE: Appendix C provides a pin comparison between the nanoNode and the microNode.

Table 5. nanoNode Pin Descriptions

Pin #	Pin Name	Signal Direction Relative to nanoNode	Signal Type	Comment
1	WAKE	Output	CMOS_O*	This is a 1.8V output signal that reflects the status of the Node's power state. When WAKE is "high" the Node is active in Idle, RX, or TX states. When WAKE is "low", the Node's 3.3V is internally gated OFF and the Node is in its lowest power state. This signal is to be used for "battery operating modes", as describe in Figure 28
2,5,8,11,14,17,20,23,24,26,28,29,30	Ground	Power	Power	Ground return. Should be low RF impedance to a solid ground plane of the Host
4	3V3	Power	Power	The 3.3V can be continuously supplied(line powered) or only when the WAKE pin is asserted "high"(battery powered). This power domain is high power (internal CPU, Transceiver, and RF PA) and should be decoupled with a low ESR, high capacitance Capacitor.
3	VBATT	Power	Power	Input power to the nanoNode. This power domain is low current but is used 100% of the time to supply internal Supervisory domains.
18	SRQ	Output	CMOS_O	SPI Slave Request
19	SRDY	Output	CMOS_O	SPI Slave Ready
6	SCLK	Input	CMOS_I	SPI Clock
7	MISO	Output	CMOS_O	SPI Master Input Slave Output

Pin #	Pin Name	Signal Direction Relative to nanoNode	Signal Type	Comment
9	CS	Input	CMOS_I	SPI Chip Select(Note other slaves are prohibited on the SPI interface, but this pin must be controlled by the Host Common Library). It **CANNOT** be tied low on the PCB.
10	MOSI	Input	CMOS_I	SPI Master Output Slave Input
12	MRQ	Input	CMOS_I	SPI Master Request
21	ON_OFF	Input	CMOS_A	This is used to turn ON/OFF the Internal Power supplies of the nanoNode. It is controlled by the Host Common Library. ■ Low: Node consumes <1uA ■ High: Node is active and will run through a wide range of power states.
13	TOUT	Output	CMOS_O	TOUT is a normally low signal that pulses high in response to specific Network Timing Events. It allows an application to trigger a measurement with sub-1ms accuracy.
22	RF_TXENA	Output	CMOS_O	This signal is used to indicate status of the Power Amplifier for the nanoNode: ■ Low = OFF ■ High = Enabled (Transmitting) The rise edge can be used to trigger a Host CPU's ADC read of VBATT (battery voltage while under maximum load).
25, 27	RF1, RF2	RF RX/TX	50 Ohm	These are the RF ports for the nanoNode. They are 50 Ohm port, DC coupled. RF1 is required but both are desired for antenna diversity. Single port or dual antenna port can be configured in the provisioning process.
16	RF_SHDN	RF Shutdown	CMOS_O	This pin indicates the status of the RF Transceiver for the nanoNode: ■ Low = Shutdown ■ High = Active ■ It can be used for WIFI/BT coexistence, and to reduce power supply current during low power states (see 3.1.3)

Pin #	Pin Name	Signal Direction Relative to nanoNode	Signal Type	Comment
15	TIME_QUAL	Output	CMOS_O	This pin is reserved and should be left as Do Not Connect.

NOTES:

1. The VDD of the internal logic of the nanoNode is 3.3Volt.
2. The Host is the SPI Master and the nanoNode is the SPI Slave.
3. CMOS_I: The Node input voltages are 3.3V CMOS levels. VIH = 2.0V (minimum) and VIL = 0.8V (maximum).
4. CMOS_O: The Node output voltages are 3.3V CMOS levels (4mA). VOH = 2.4V (minimum) and VOL = 0.4V (maximum).
5. SPI inputs to the node (SCLK, MOSI, CS) must be tri-stated or driven low when the node may be sleeping (MRQ and SRQ are both low). See section 5: SPI Interface and Sequences for more details.

3.1 Signal Descriptions

3.1.1 GND

Ground is the Host CPU's ground to enable a common reference between CPU and Node.

3.1.2 VBATT

This supplies a low current 2.2 V – 5.5 V for the Node's internal supervisory circuitry. This pin should be decoupled with a 0.1 µF capacitor on the Host processor board.

3.1.3 3V3

This pin drives the CPU, Transceiver, RF PA section of the module. It can consume up to 800 mW. Allow for bypassing with a 47 µF low ESR cap (bulk) and a 0.1 µF ceramic cap for optimal performance. Depending on the Host design, there are some nuances that are important regarding this signal:

- 3.3 V can be supplied continuously or only when the WAKE signal is asserted "high.", for battery powered applications.
- The Node runs through various operating states when 3.3V is supplied.
  - If the Node internally is in an state that requires no RF, the 3.3 V can be "noisy" (+/-100 mV ripple). The RF state is defined by the RF_SHDN pin. This allows the Host's 3.3 V regulator to work in low quiescent (power save) modes.
  - If the Node internally is active and does require RF, the 3.3 V must be "clean" (+/-20mV ripple). This forces the Host's 3.3V supply into a high precision mode and forcing a high quiescent current of that regulator.

This switching of "noisy" and "clean" becomes clear (and important) when working with battery operated devices and optimal low power drain.

3.1.4 ON_OFF

This input signal controls the power-on of the LDO circuitry for the nanoNode. This signal is controlled by the Host Common Library, compiled onto the user's apps processor. For reference only: It must be shut off prior to starting the nanoNode power-up sequence as defined in section 5.4: Startup (Power On) Sequence. After the nanoNode powers up, this signal is to remain logic high during normal operational modes. This pin dually serves a power on/off function as well as a Node Reset function.

3.1.5 MRQ

The MRQ (Master Request) is the Host's normal way of waking the nanoNode to initiate SPI communications. Logic "High" forces the nanoNode awake. This signal is controlled by the Host Common Library, compiled onto the user's application processor.

3.1.6 SRDY

SRDY (Slave Ready) is an indication from the nanoNode that it has fully booted its internal Firmware image, initialized its Hardware and Interfaces, and is ready for communication (arbitration) with the Host. Logic "High" indicates the nanoNode is ready for communications. This signal is controlled/handled by the Host Common Library, compiled onto the user's application processor.

3.1.7 SRQ

The SRQ (Slave Request) signal is an indication from the nanoNode that it wants the Host's attention. When SRQ is asserted "High," the Host must read the Status registers of nanoNode. If SRQ is "High," SRDY will also be "High." This signal is controlled/handled by the Host Common Library, compiled onto the user's application processor.

3.1.8 SPI System

The SPI system is the generic term used for all SPI signals (MOSI, MISO, CS, SCLK) to be set up for SPI communications to occur between Host and nanoNode. The nanoNode SPI is the Slave in the Master/Slave communications and is defined in section 5.2: SPI Mode and Timing.

IMPORTANT NOTES:

1. Other SPI slaves are not allowed to share the SPI signals.
2. CS must be controlled by the Host Common Library API to guarantee correct sequencing. Specifically, the user must ensure that the SPI CS is active (low) for the whole duration of a message transfer, with no gaps. This is implemented in HOST_CMN_HAL_ExchangeMsg in host_cmn_hal_k20.c, in the rACM example code, and must be duplicated for your particular apps processor.

3.1.9 TOUT

This signal is a Time Synchronizing signal that pulses high upon specific network timing events.

3.1.10 RF_TXENA

This signal indicates when the device is transmitting. When transmitting, it is recommended that the Host processor use this opportunity as a trigger to read the system "Vbatt" power line to show battery voltage under maximum load.

3.1.11 RF_SHDN

This Node signal indicates status of the RF Transceiver of the nanoNode. If low, the transceiver sleeps (no RX and no TX). This output of the module (3.3 V) indicates when the RF transceiver is on or off. When RF_SHDN is high, the RF is "ON" (RX or TX). In the RF "ON" mode, the module needs a "clean" 3.3 V (low ripple).

3.1.12 RF1 and RF2

These are the RF ports (RX and TX) of the Node. They are DC-coupled, 50 Ohm and require special Host routing of PCB. RF1 is the primary antenna and is always required. RF2 is a secondary antenna that the Node can use for Antenna Diversity. A single or dual antenna (diversity) system can be configured during the Provisioning process. For best results ensure the load termination (antenna) has a VSWR of 1.5:1 or better (return loss < -10 dB).

3.1.13 TIME_QUAL

This signal is reserved for Ingenu.

3.2 Environmental

3.2.1 ESD

The nanoNode is designed to be a truly embedded module and can almost be considered an IC. The nanoNode is to be placed as a direct-connect to the Host CPU. Therefore, the nanoNode has inherent minimal electrostatic discharge (ESD) protection on its I/O.

Table 6. ESD Information

ESD Model	Class and Minimum Voltage
HBM	Class 1C (>1000V)
MM	Class A (>100V)

RF pins have inherent ESD robustness due to the RF antenna cross switch and survive the 1 kV HBM test. With a shunt 27 nH inductor at the RF pin, the pin can survive direct 8 kV ESD strikes.

If the application is intended for harsh ESD or lightning strike scenarios it is recommended that the Integrator take extra precautions to guard against accidental resets or ESD damage.

3.2.2 Harsh Environments

The nanoNode employs miniature surface-mounted components in its assembly. If the target design is intended for high humidity or salt environments and intended to have a long service life, it is recommended that the designer take necessary precautions to guard against prolonged exposure to moisture and other contaminants. A sealed enclosure (IP67 or IP68) or potting may be required in extreme environments.

4 Applications

This chapter describes two major methods of implementing the nanoNode: Powered and battery operated modes.

1. **Powered Operating Mode**

   "Powered" refers to the Host board and its power supply. Specifically, it refers to a good solid, consistent power supply – such as an AC powered source. In this type of usage case, the Host can potentially supply a good clean 3.3 V rail (pin 4) without regard to extreme detail of optimizing power consumption.

2. **Battery Operated Mode**

   This mode refers to a battery operated device in which extreme care and attention is applied to reducing overall power consumption. All details and all modes of power consumption are considered and optimized.

4.1 Powered Operating Mode

In this scenario, the Host and Node's power consumption is not really a consideration. In this case, the Host can take an input Voltage and convert to a 100% duty 3.3 V supply. This would be applied to:

- Host CPU
- VBATT of nanoNode
- 3V3 of nanoNode

In this case, the node will internally turn the 3.3 V rail ON/OFF as it is required. The Node attempts to gate this internal supply OFF to conserve power, when it can. The HW status of the 3.3V supply is the WAKE signal (3.3V = "ON" if WAKE is High). When the 3.3V is internally gated off, the Node consumes virtually no power on that supply.

However, the Host CPU is always powered by 3.3 V – the operating level of the Host-nanoNode SPI interface. The nanoNode requires a full 3.3 V during SPI transfers. For a wired example of the Powered circuitry, refer to Figure 27. Powered Example.

4.2 Battery Operated Mode

Battery operating mode offers a much more challenging design constraint. The goal is to reduce current consumption where possible. To this conservation goal, see Figure 28. Lithium Battery Example.

The assumption in this design goal is to use a long life battery such as Lithium battery/cell. These primary cells offer:

- Extreme low self-discharge
- Long life

- Wide operating temperatures
  - High capacity
  - 2.2 V – 3.6 V direct voltage over the operating temperature and discharge characteristics of the cell

In this case, assume that:

- The VBATT pin of the Node is connected directly to the cell (2.2 V – 3.6 V).
- The 3V3 signal of the Node is connected directly to the 3.3 V regulator. The regulator is turned ON/OFF depending on the state of the WAKE pin of the Node.
- The CPU uses an indirect path through a dual Schottky diode to permit seamless switching/transition from battery voltage to 3.3 V.
- Most modern CPUs used for this type of application have the following characteristics:
  - Operate at 1.8 V – 3.6 V
  - Low sleep current (1 – 2 µA with full SRAM retention for fast wakeup)
  - Pins that use interrupts to wake the processor from deep sleep

The following sections describe the major operating states and power supply modes.

4.2.1 Sleep Mode Assumptions

1. The Node is powered "on" (ON_OFF = high).
2. The Node is in sleep mode when in the WAKE state (WAKE = low).
3. The Node is consuming minimal current through its VBATT pin.
4. 3V3 is off and is not required by the Host or Node.
5. The Host CPU can run off the "natural voltage" of the cell only drawing microAmps of current.

4.2.2 Active Mode

When the Node awakens (WAKE = high) and the 3.3 V power supply is turned "on":

- The Node uses the supplied 3.3 V as required.
- The voltage of the CPU ramps to the higher of the following: cell voltage or 3.3 V supply.
- The 3.3 V on the Host and the Node permits the Node to fully function on the RPMA network and also allows Host-Node SPI communications.

A Texas Instruments TPS63000 3.3 V buck/boost regulator (or equivalent) is recommended for nanoNode applications. This has some unique benefits:

- When in high efficiency mode (PS/SYNC = low), the regulator outputs a loose 3.3 V with +/-100 mV ripple. In this mode, its quiescent current is only 50 µA.
- When in low efficiency (but "clean" output) mode (PS/SYNC = high), the regulator is within +/-20 mV ripple but consumes a 0.6 mA quiescent current.

These operating modes align well with the Node's operating modes as defined by the RF_SHDN pin:

- When tight regulation (low ripple) is required by the RF of the Node:
  - RF_SHDN = high
  - PS/SYNC = high
- When the Node does not need tight regulation and is in a moderately low power mode, RF_SHDN is low (and PS/SYNC is low).

Other design considerations for optimal low power are as follows:

1. Reduce capacitance in the 3.3V domain. Extra capacitors require charging each time the 3.3 V is on.
2. Ensure all software and CPU configurations set CPU pins to low power states.
3. Use high value resistors such as 1 M or greater for pull-ups/pull-downs where possible.

5 SPI Interface and Sequences

5.1 SPI System Interface Overview

The SPI slave interface is currently the only supported interface for Host-to-Node communication. The SPI System interface is controlled/handled by the Host Common Library, compiled onto the user's apps processor. The following section (all of section 5) is informational only.

NOTE: The nanoNode must be the only SPI slave on the bus.

The SPI slave interface provides communication with an external Host through a 7-wire interface. The Host is the SPI master and the nanoNode is the SPI slave. In addition to the four standard SPI signals, three additional signals are used to complement the SPI bus: MRQ, SRQ, and SRDY. The additional signals are included to support nanoNode state transitions and bi-directional message traffic.

The SPI signals include four that are controlled by the master and three that are controlled by the slave.

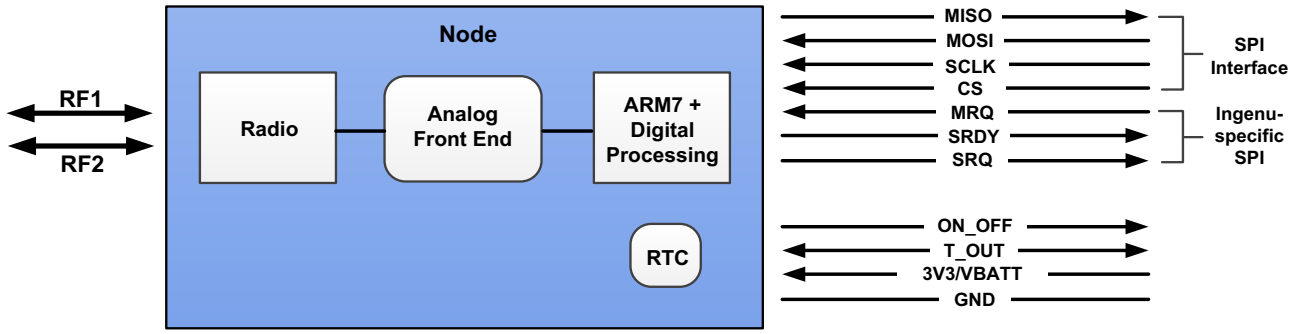
Master-controlled Signals (Host)

- MOSI
- SCLK
- CS
- MRQ

Slave-controlled Signals (nanoNode)

- MISO
- SRQ
- SRDY

When MRQ and SRQ are low, the remaining Master controlled signals (MOSI, SCLK, and CS) must be held low or tri-stated. This is to prevent these signals from back-driving the nanoNode (Slave) that may be in deep sleep. When either MRQ or SRQ assert high, the Master should set each of the three signals appropriately according to their standard usage. No pull-up resistors should ever be applied to any signals on the nanoNode since it often needs to fall into a Deep Sleep mode (all internal regulators turned off).



5.2 SPI Mode and Timing

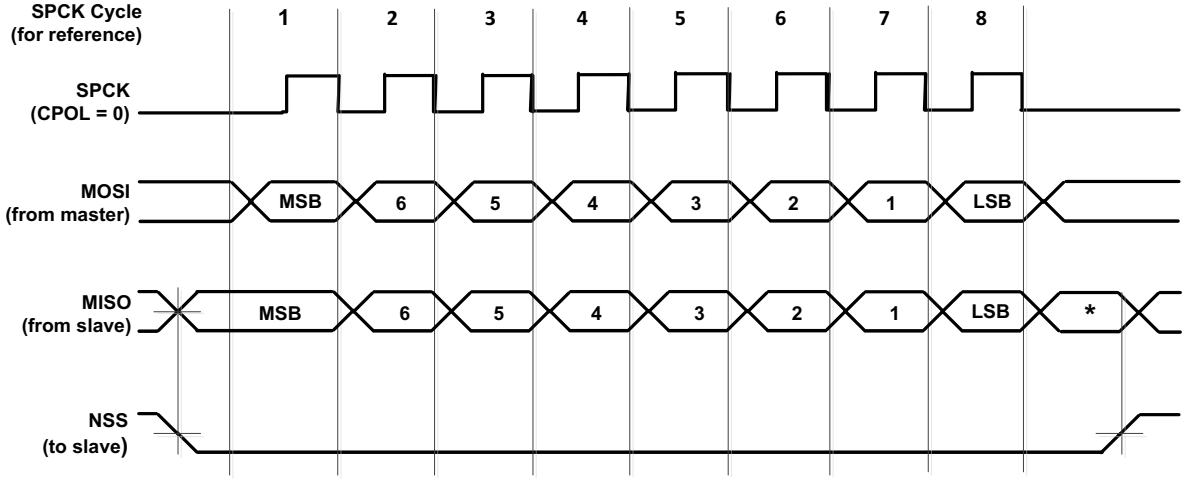


Figure 8. SPI Timing, CPOL = 0, CPHA = 0

5.3 Host Initialization

What is described here is the initialization of the Host, its operating software, and the control sequences used to drive the nanoNode.

Due to specific clock and memory requirements, the nanoNode must go through specific Initialization and Wake sequences.

NOTE: Some CPUs have internal pull-up resistors that are active after Power On Reset. Through CMOS leakage, the Host CPU can supply voltages to the nanoNode I/O bus prior to the Host CPU fully initializing and disabling the pull-up resistors. It must be noted that during the brief initialization period, the POWER_ON signal must be "low." Activating the POWER_ON signal with other nanoNode signals being pulled "high" can cause CMOS latchup within the nanoNode.

5.4 Startup (Power On) Sequence

During, and immediately after Power On Reset (POR), the Host has no control of its I/O power states. For instance, some CPUs have GPIO that tri-state or act as inputs during power up. Other CPU brands have programmable pull-ups on its I/O and need the Host CPU to disable those pull-ups for the Host's GPIO to work correctly with the nanoNode. This setup and configuration of GPIO takes a finite time during the Host boot process. This is detailed in the following figure.

Whereas the power-up sequence is described here, it is recommended the Integrator not attempt this entire startup sequence without assistance. Ingenu offers a formal and controlled library to help with this startup and communication interface. For more information, refer to the *rACM Developer Guide (010-0105-00)* and the *Host Common Software Integration Application Note (010-0024-00)*. These documents are described in section 1.3: References/Tools.

The initial sequencing of the 3.3V and Vbatt rails are:

- Both 3.3V and Vbatt van be applied simultaneously, or
- The Vbatt can rise first if 3.3V follows within 1mS, but
- the 3.3V should never rise prior to Vbatt.

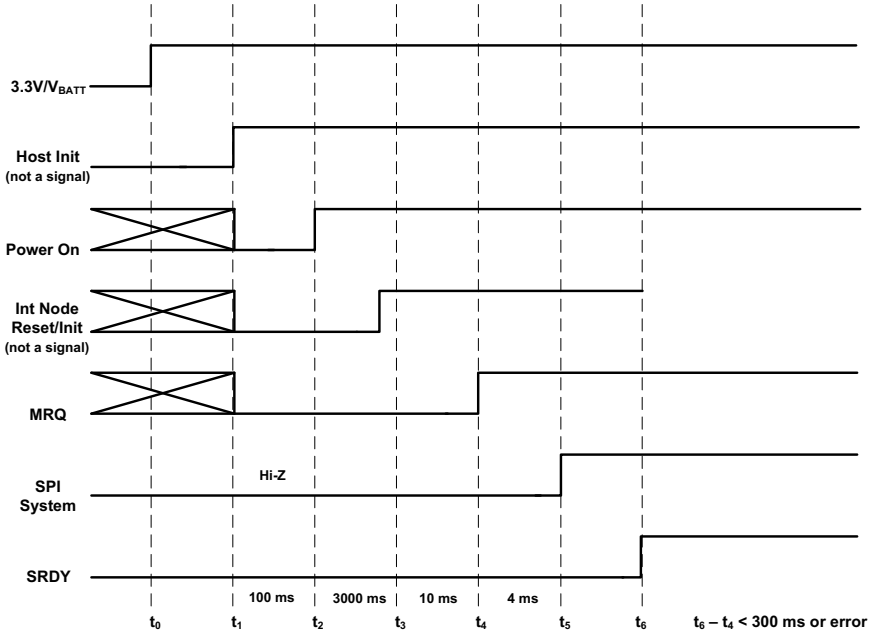


Figure 9. nanoNode Power-up Timing Sequence

The timing sequence shown in Figure 9 above is described below. **NOTE:** The timing shown in the figure is not to scale.

- **t0 → t1** This phase is where the Host's System power has been applied and the Host Software must power up and initialize the GPIO interfaces for the nanoNode to the required states defined at time t1. The t1 state becomes "TRUE" indicating the Host sets all the GPIO to a known and controlled state (Low).
- **t2** At t2 state, all the output signals to the nanoNode are set low and the Power On Signal is set high. This turns on the internal LDO regulators of the nanoNode to initiate a power up sequence. The time between t1-t2 is approximately 100 ms, or longer. Assert ON_OFF "high" starts an internal clock (32 K) and releases an internal reset pin which may take up to 3 seconds to stabilize.
- **t3** t3 is when the Host releases the nanoNode from its Reset state. This time allows the 32 kHz of the nanoNode to turn on and stabilize. The time between t2-t3 is 1 second, or longer.
- **t4** t4 signals the start of the Host wanting to initiate communications (arbitration) with the nanoNode. The Host raises MRQ to turn on various circuitries. The time between t3-t4 is 10 ms, or longer.

- **t5** After the assertion of t_4, the nanoNode begins its "wake sequence." The nanoNode must boot, initialize its operating system and hardware and when it is ready for communications it raises its SRDY signal back to the Host. At this point, communications (Arbitration) can begin.
- **t6** At this point the nanoNode signals its readiness by asserting the SRDY pin. The Host can now begin communications with the nanoNode.

5.5 Wake Sequence

The nanoNode will often go into sleep mode even though ON_OFF is "high" (active). To begin Node-Host communications, the host must ensure the nanoNode is awake. The nanoNode can be awakened in two manners:

- MRQ assertion from the Host. The Host desires communications with the nanoNode and awakens the nanoNode by asserting the MRQ line. This is a Synchronous Wake Sequence.
- The nanoNode can "self-awaken" due to network events. In this case, a timer internal to the nanoNode "pops" and triggers the nanoNode to "wake." When the nanoNode is awake it asserts its SRDY as a matter of course to indicate to the Host (if it needs to) that it can start communicating with the nanoNode while it is awake. This is an Asynchronous Wake Sequence.

5.5.1 Wake Sequence (Synchronous)

The following sequence demonstrates the timing required of the Host to awaken the nanoNode from a sleep state.

Assumptions:

- The nanoNode has been previously Powered On and Arbitrated.
- The power (VBATT) has remained stable and the nanoNode has not been Reset (Reset is set to tri-state/float).

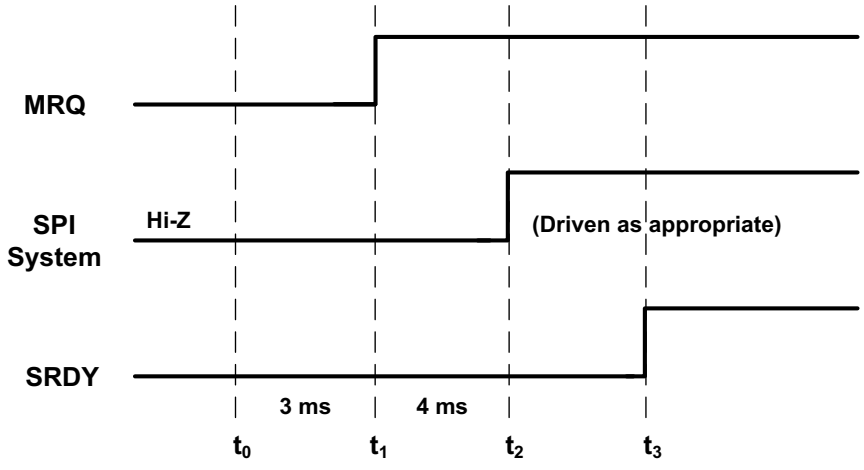


Figure 10. Host-Initiated nanoNode Wake Sequence – SRDY Low (Synchronous)

The timing sequence shown in Figure 10 above is described below. **NOTE:** The timing shown in the figure is not to scale.

- **t0** The Host desires to wake the nanoNode and asserts MRQ high.
- **t0 → t1** After MRQ has gone High, the Host's SPI system and other I/O can be enabled. Asserting the MRQ has enabled the internal I/O power supply of the nanoNode and the Host's SPI can be enabled 4 ms after the rise of MRQ.
- **t1 → t2** After the initial assertion of MRQ, the nanoNode has to internally power up and initialize its systems. When it is ready to communicate it will assert its SRDY line to signal it is now ready for SPI interaction. From MRQ assertion until the nanoNode is ready, takes about 80 ms.
- **t3** The nanoNode is now ready to fully communicate with the Host.

5.5.2 Wake Sequence (Asynchronous)

In this scenario, the nanoNode is already awake due to a networking event (SRDY is already High) and the Host wants to communicate with the nanoNode while it is awake. The Host asserts MRQ to ensure that the nanoNode stays awake during its communication cycle.

NOTE: The timing shown in the figure is not to scale.

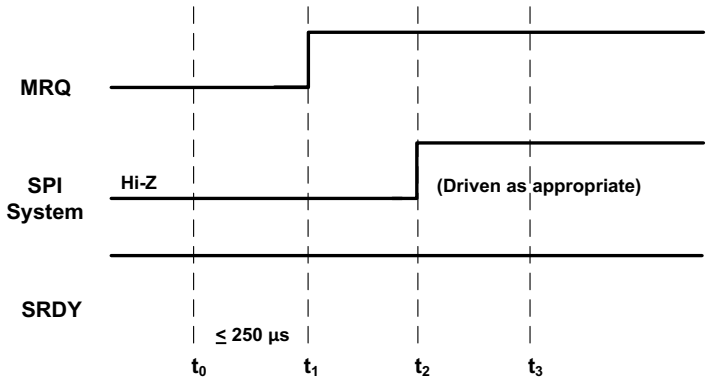


Figure 11. Host-Initiated nanoNode Wake Sequence – SRDY High (Asynchronous)

5.6 Host-Driven Reset Sequence

If the nanoNode fails to communicate (or similar), it may be necessary to "Reset" the nanoNode. The following figure shows the proper sequence to reset the device.

NOTE 1: Resetting the device causes it to go through an RPMA Cold Acquisition process to reacquire the network.

NOTE 2: The timing shown in the figure is not to scale.

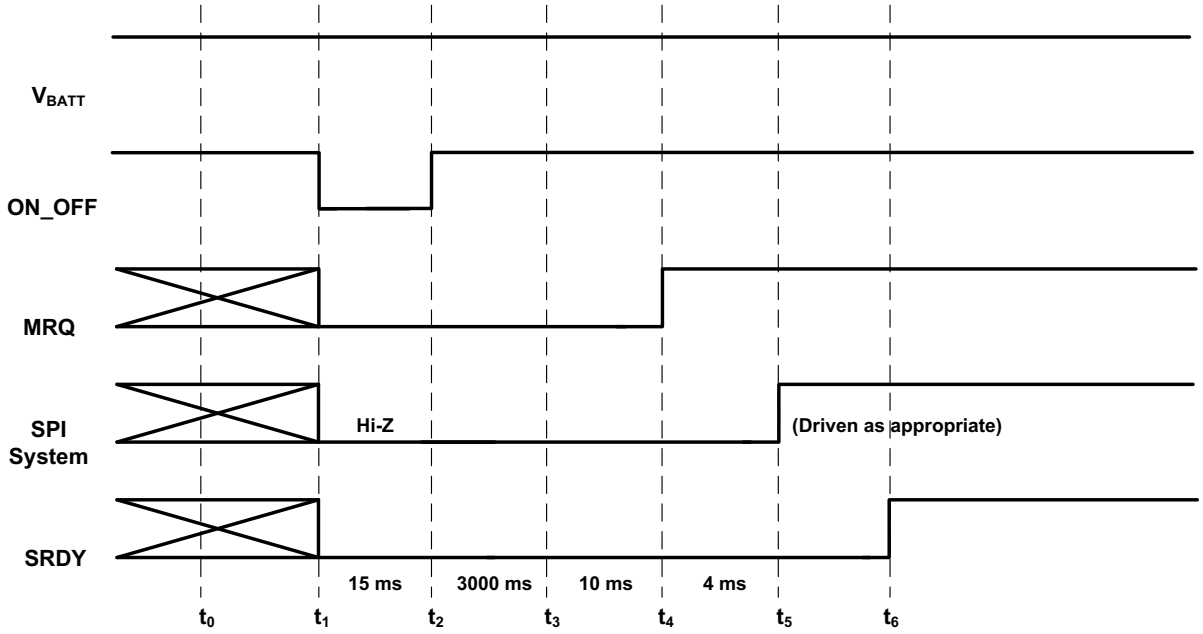


Figure 12. Host-Driven Reset Sequence

5.7 Host MRQ Release/nanoNode Allowed to Sleep Sequence

If the Host determines there are no more messages or SPI transactions required, it nominally de-asserts the MRQ to allow the nanoNode to fall back to Deep Sleep (lowest power mode). The figure below shows how this is sequenced by the Host/nanoNode. A small delay in de-asserting SRDY is enforced to prevent quick toggling (waking) of the nanoNode.

NOTE: The timing shown in the figure is not to scale.

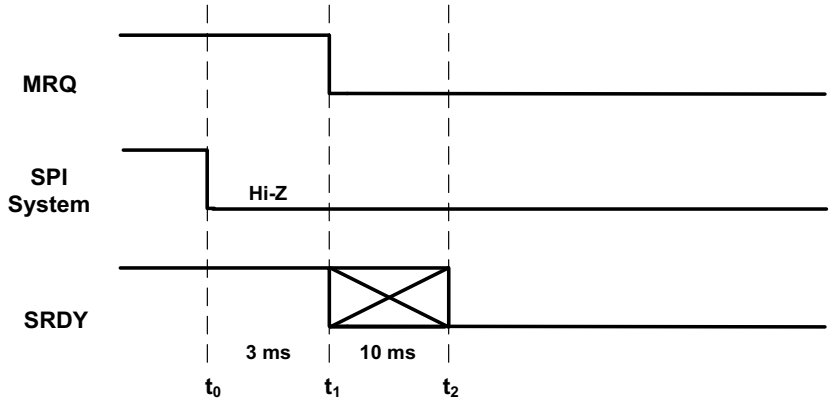


Figure 13. Host MRQ Release/nanoNode Allowed to Sleep Sequence

6 Power States

Ingenu can provide partners with tools to accurately predict battery life for their particular application. We recommend that partners use these tools. This section is provided for reference only.

The nanoNode has a number of states it runs through during its various operating modes.

General comments:

- The nanoNode accepts a wide input voltage range (2.2 V – 5.5 V on VBATT).
- The nanoNode has low drop out (LDO) regulators that will operate 100% of the time the nanoNode is powered (ON_OFF signal set to high).
- The nanoNode requires either a fixed or switched 3.3 V supply on its 3V3 pin.

The nanoNode always tries to minimize its power consumption but is largely driven by network operating states and modes of operation. This document does not describe all of the modes in detail but, in general, there are two main operating modes for the nanoNode:

1. **Continuous Mode**
   In this mode, the nanoNode is ON (awake) at least 50% of the time (100% of its RX cycle). The nanoNode starts up, searches for the network, locks on, and Joins. In this mode, the nanoNode is nominally in RX or TX mode (radio is ON and in a high power consumption state), or in an Idle state where the clocks and CPU are ON but the radio is OFF (moderately low power mode). The continuous mode is usually for applications where the Host and nanoNode are AC-powered and system current consumption is not an issue.
2. **Slotted Mode**
   This mode has the nanoNode falling into a Deep Sleep state—the lowest power state of the nanoNode. In this mode, the nanoNode is mostly powered down except for a couple of low power LDO Regulators. The nanoNode can sleep for hours at a time if the network is configured to allow this.

The power states are described in the following sections.

6.1 Operating States

This section describes the various operating states within the operational modes.

6.1.1 Power Off State

When the nanoNode is totally non-functional, the Host can set the POWER_ON signal Low to deactivate the circuitry of the nanoNode. This should NOT be confused with Deep Sleep states where the nanoNode mostly sleeps yet maintains key network timers to wake up synchronously with network activity. If awakened from the Power Off state, the nanoNode must go through a very power-hungry search/acquisition algorithm to re-acquire the RPMA Network.

6.1.2 Deep Sleep State

The nanoNode shuts off all its power regulators except a couple low quiescent LDO regulators. These regulators keep a minimal amount of circuitry alive for tracking network timers, enable a 32 kHz clock, and some minor interface circuitry.

6.1.3 Oscillator Calibration State

When the nanoNode is in Deep Sleep state, it attempts to maintain accuracy of its low power 32 kHz clock to enable faster network synchronizing when it wakes up. The CPU of the nanoNode is not activated during this calibration state. The nanoNode will periodically (and briefly) wake up in a very low power mode to calibrate its 32 kHz clock to its very accurate 26 MHz clock. This is especially important when the temperature varies substantially causing the 32 kHz oscillator to drift. This is illustrated in the following figure.

This plot is an example of the nanoNode performing a self-calibration of its 32 kHz oscillator. The pulses represent the TCXO being turned on periodically to perform the calibration. The nanoNode wakes itself from Deep Sleep, Calibrates, and then falls back to sleep. Minimal power is consumed during this self-calibration process. As can be seen, the nanoNode does this approximately every 900 seconds.

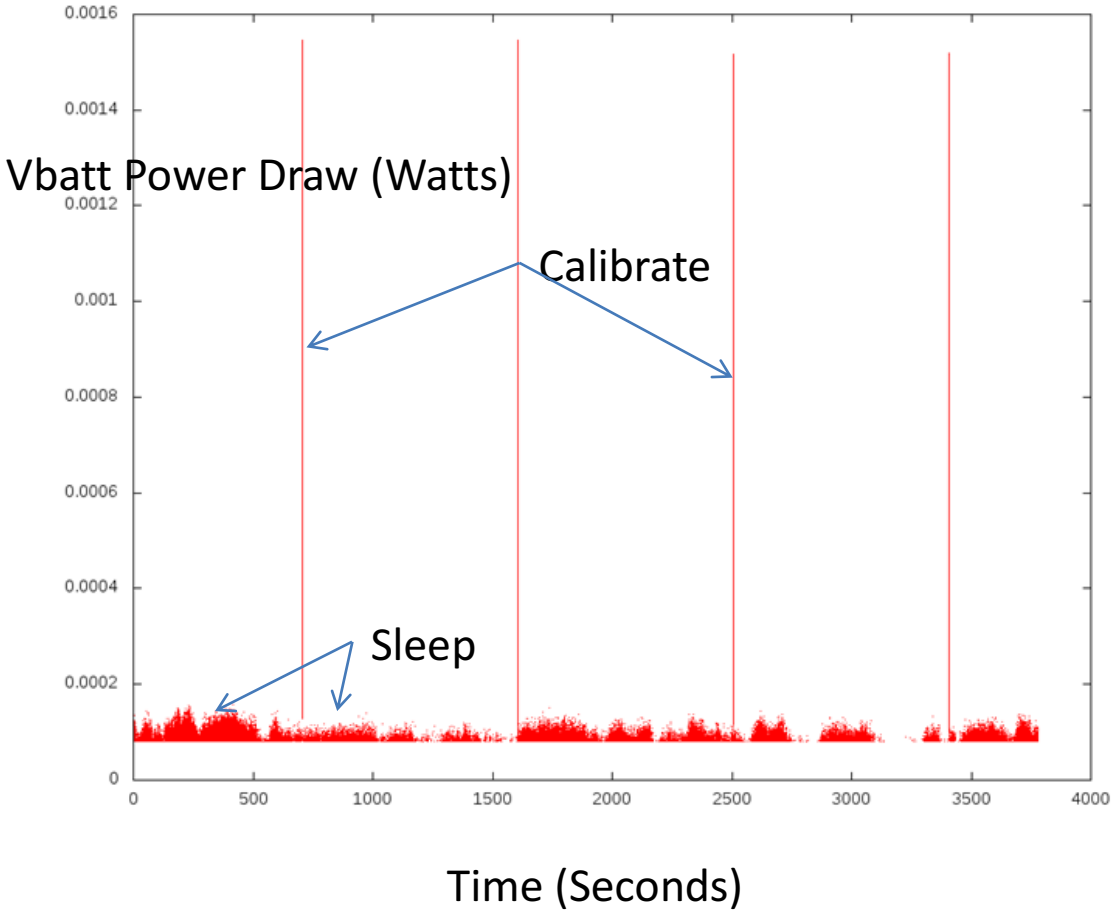


Figure 14. nanoNode Oscillator Calibration: Current (Amps) vs Time (Seconds)

6.1.4 Idle State

Idle state has various sub-states but generally refers to a state where the nanoNode is "awake" and its system clock is on, the CPU is awake, but the RF is OFF.

6.1.5 RX State

The nanoNode turns on all its clocks, the main CPU and the RF in an RX-only state. The RF transceiver, in RX state, consumes a moderate amount of power.

6.1.6 TX State

When the nanoNode transmits, it uses a variable transmit power that is correlated to its received RSSI. In this state, the nanoNode is likely at its highest power states, but this is somewhat dependent on RSSI. The worst case state (maximum power) is shown in Figure 15. This is at approximately 23.3 dBm output power. This is the highest power state for the nanoNode.

6.2 System

As noted, the nanoNode can go through various states of Deep Sleep, Idle, RX, and TX. The plot shown in the following figure provides a representative nanoNode waking up and going through these states and transitions.

All systems are different and current consumption is affected by many factors.

- Network coverage. How much TX power does a nanoNode need to transmit its data?
- Temperature range
- Operating Voltage
- Continuous mode vs Slotted mode: What is the Uplink Interval?
- Amount of data in the data model
- Quality of Service (QoS) for data delivery

All of the factors indicated above must be examined carefully and plotted to understand the end result in current profiles and expected battery life projections.

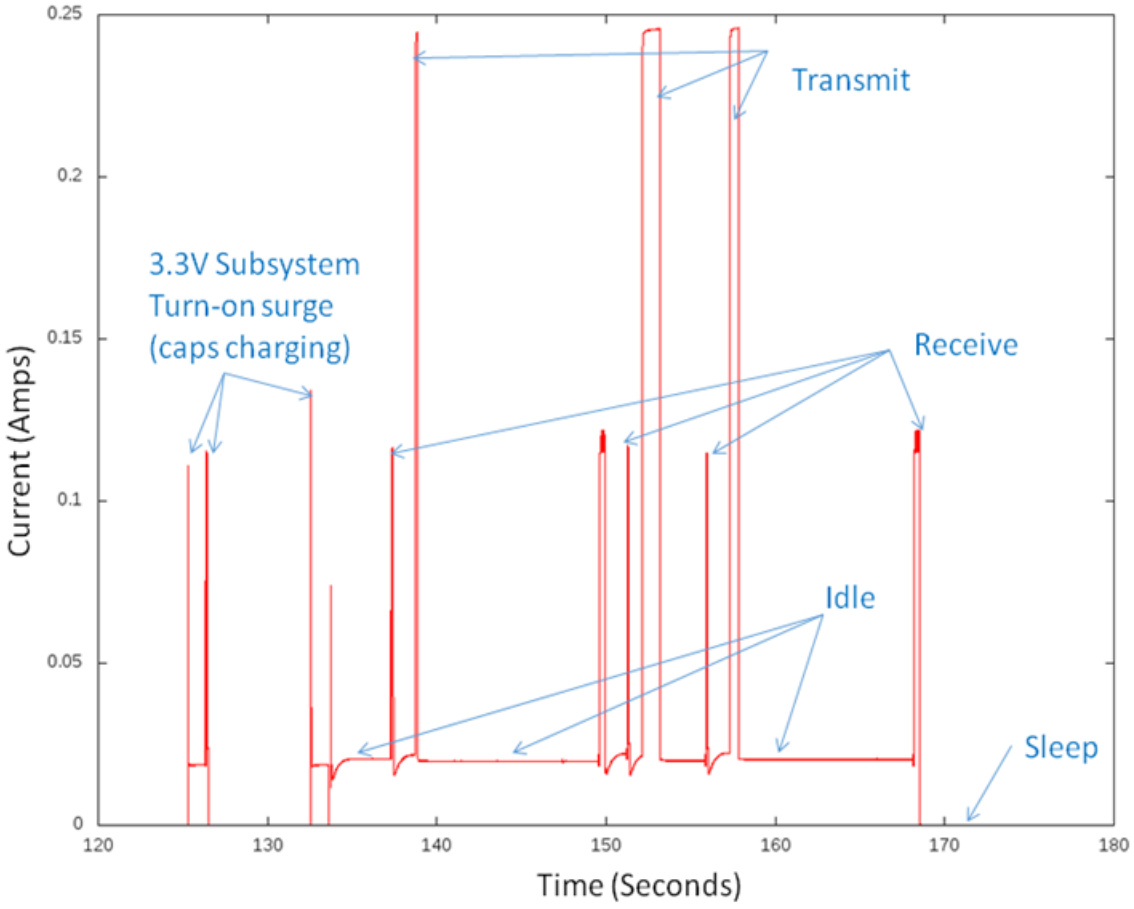


Figure 15. Representative Current Consumption During Deep Sleep, Idle, RX, and TX; x16 Spreading Factor

The plot shown in the figure above represents the nominal transitions for the nanoNode from Deep Sleep, Idle, Receive, and Transmit states. In this case, a TX spreading factor of 16 is used. It is important that the Host designer understand the System operating profile, operating voltages, different operating modes of the nanoNode and the ultimate effect on System power consumption. Of course, this is especially true if a battery powered device is being considered.

7 SPI Messaging Protocol

The SPI Messaging between the Host processor and the node is controlled/handled by the Host Common Library, compiled onto the user's apps processor. The following section (all of Chapter 7) is informational only.

The details of Host/Node messaging are typically not necessary for integrators to implement. The rACM application code (supplied by Ingenu) is a working example of a Host Common integration on an NXP (formerly Freescale) K20.

7.1 Arbitration

Arbitration is the process a Host uses to signal to the Node that it supports the bi-directional messaging protocol. The arbitration sequence is designed to reduce the probability that an arbitrary non-Host transfer sequence can mirror a valid arbitration sequence.

Arbitration consists of both Host and Node transmitting an arbitration request/reply pair. After a defined turn-around delay, both transmit a validation request/reply. The turn-around delay avoids race conditions between Host and Node and provides enough time to allow ISR execution to complete before the next SPI transfer.

If the Node does not reply to the Host request, the Host needs to wait for a turn-around delay and retry the arbitration request.

The Host must perform the arbitration sequence before any other SPI Bus communication can take place between the Host and the Node.

The Host must initiate this arbitration sequence on boot up. Additionally, the Host must perform the arbitration sequence when the Node sends to the Host an arbitration message. This can occur due to the Node going into Deep Sleep and then waking up. Since the Node requires the arbitration sequence after waking from Deep Sleep and since the Host is not aware of when the Node goes to Deep Sleep, the Host must be able to detect that the Node is requesting arbitration and the Host must then reset its Host interface state machine and perform arbitration. For more information on the Host interface SPI bus state machine, refer to section 7.3: Host Interface SPI Bus State Machine.

7.2 Message Protocol

Host-to-Node transfers use master message command pairs and Node-to-Host transfers use slave message command pairs. Both transfers use identical command sequences with only the encoding of the commands differing. The command sequence for a message transfer consists of a request/acknowledgement pair followed by a defined turn-around delay and then a message composed of a header pair and a payload.

Variable length payloads are supported by encoding the payload size in the second half of the message request. The second half of the message reply contains the available receive buffer size. If the message payload size exceeds the receive buffer size, then a new request must be made after a turn-around delay with a payload size that does not exceed the receive buffer size.

After a successful message request transfer, the Host waits a turn-around delay and then initiates the transfer with a message header command. The payload immediately follows the header and, if necessary, is zero padded to match the payload size indicated in the message request. After the payload, the Host waits a turn-around delay before proceeding with any other further messages.

The Host interface SPI bus is a standard SPI bus (with MISO, MOSI, CS, and SCLK) with the addition of three lines (MRQ, SRQ, and SRDY). These three additional lines are used to provide the Host with the ability to wake up the Node over the SPI Bus as well as providing the Node with the ability to prompt the Host to begin a SPI Bus transaction. The Node is also exceptional in that it must be the only slave present on the SPI Bus, since MOSI, CS, and SCLK must be undriven (tri-stated) any time that MRQ is low.

Before any message is communicated over the SPI Bus, the MRQ and SRDY lines must be high. The Host guarantees this by pulling the MRQ line high and waiting for the Node to pull the SRDY line high. The Host cannot proceed with SPI Bus communication until both of these lines are high. Once MRQ and SRDY are high, the Host, being SPI Bus master, can continue with a normal SPI Bus transaction.

When the Node wishes to communicate with the Host, it pulls the SRQ line high. The Host must have the ability to detect this and start a SPI Bus transaction (by first pulling the MRQ high and waiting for SRDY to go high). A standard SPI Bus transaction is described and illustrated in Figure 18.

Message exchanges between Host and Node are shown below in Figure 16.

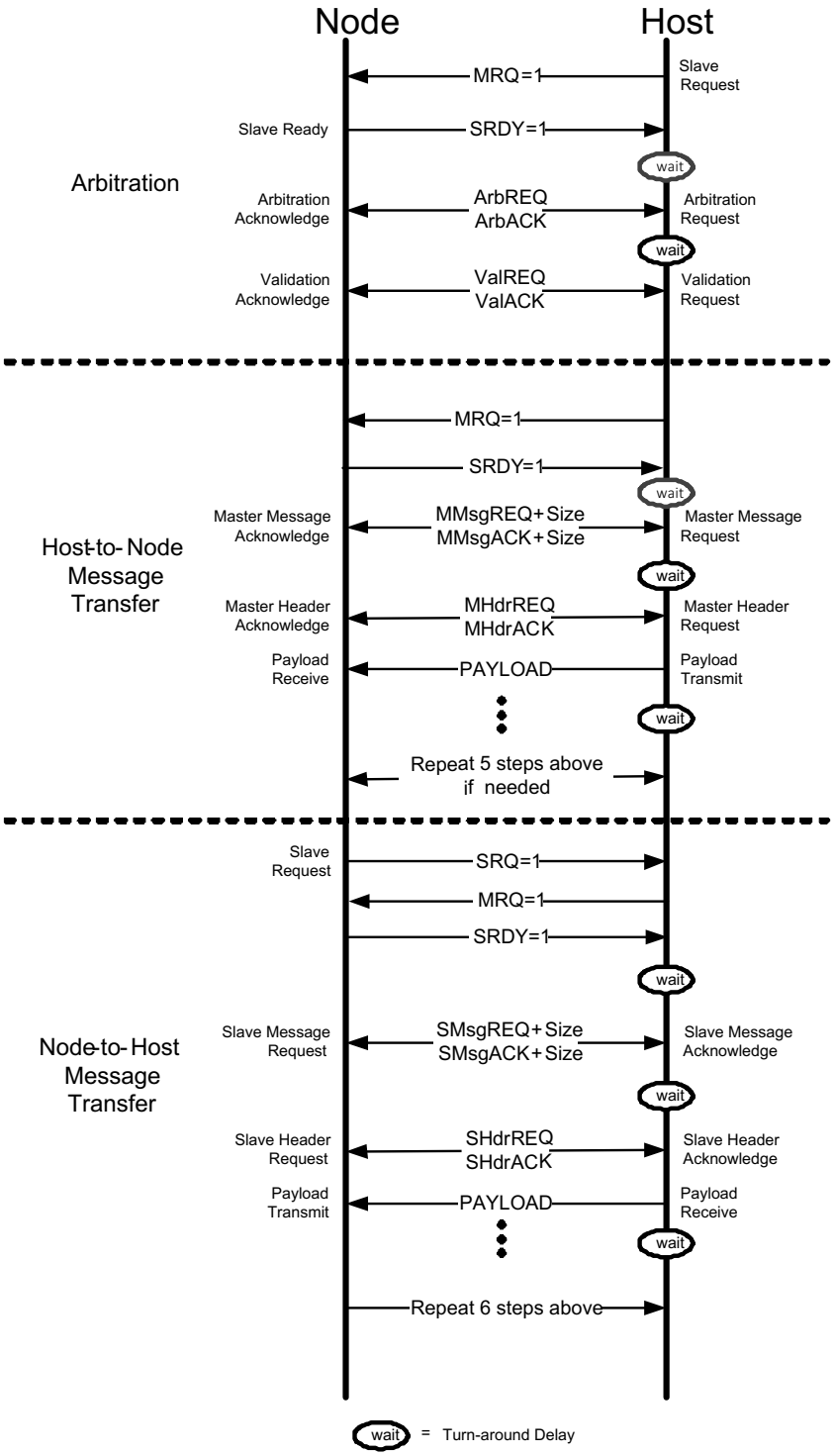


Figure 16. SPI Master and Slave Message Sequences

In each of the request/acknowledge command pairs shown, the top command is transmitted by the Host (master) and the bottom command is transmitted by the Node (slave). The wait

bubbles indicate a predefined turn-around delay which provides ISR processing time and avoids race conditions between Host and Node.

7.3 Host Interface SPI Bus State Machine

This section illustrates the sequence of messages that can take place on the Host interface SPI bus. The design and implementation of the actual state machine on the Host software is up to the Host software designer. This diagram is provided to demonstrate the message sequence over the SPI Bus. Note the usage of the turn-around delay, which is required in between each step of message exchange. This delay is required by the Node and is currently defined as having a time of 200 µs.

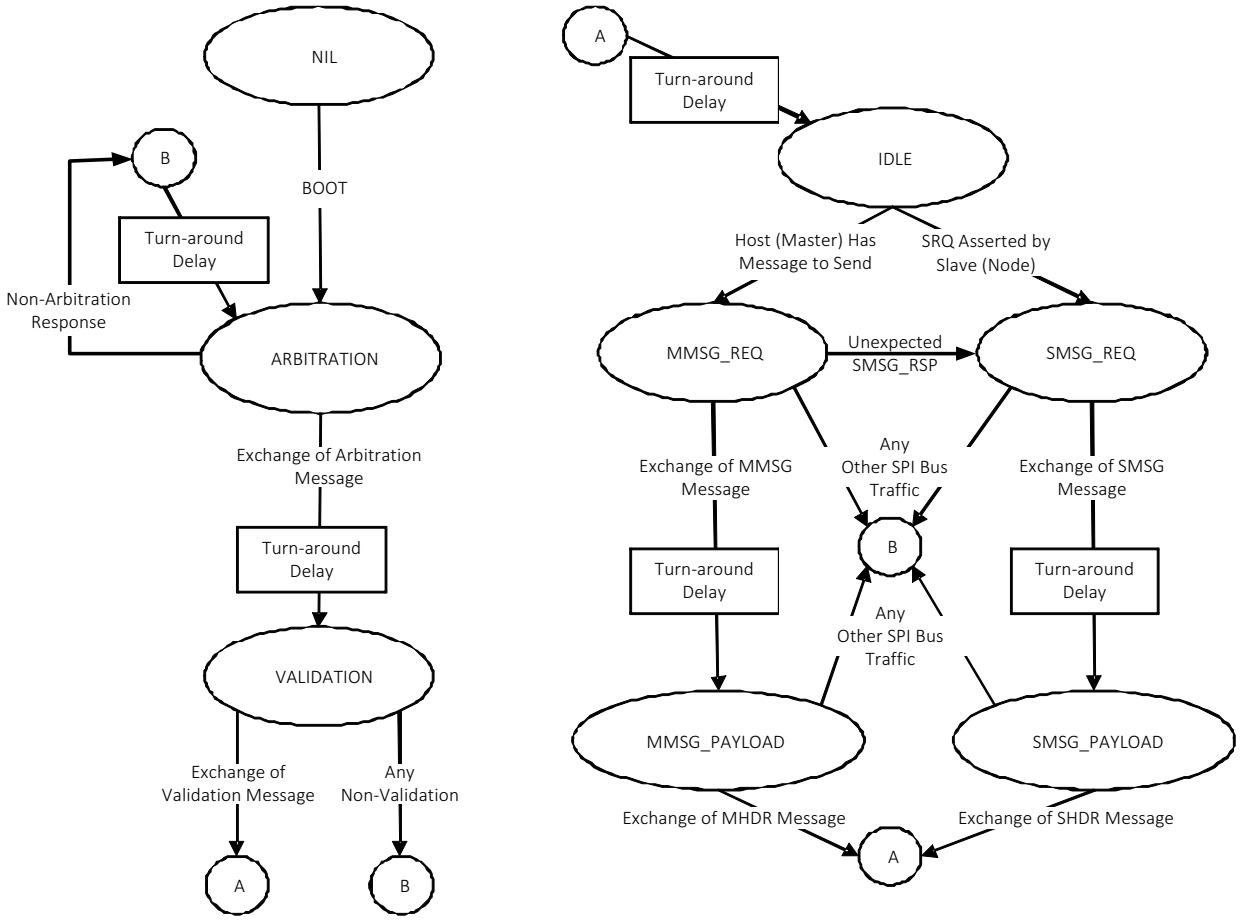


Figure 17. Host Interface SPI Bus State Machine

7.4 SPI Bus Timing Example

This section provides an example illustration of an exchange of messages first from master (Host) to slave (Node) and then from slave (Node) to master (Host). Each step in the timing sequence is described below:

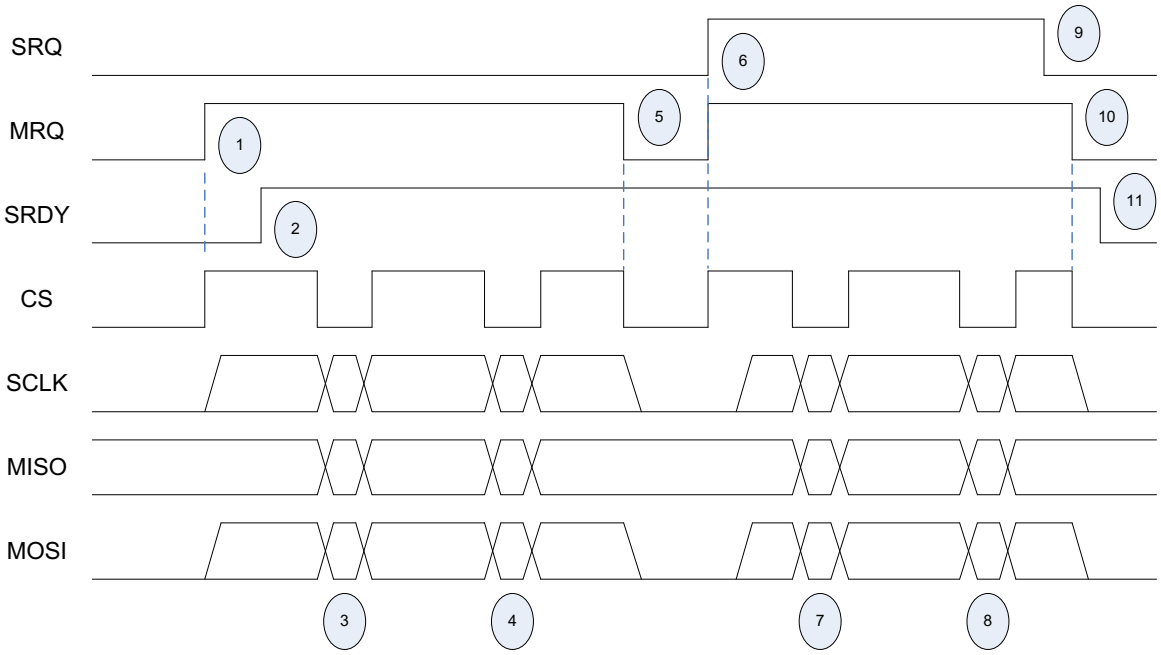


Figure 18. SPI Timing Example

Note that MRQ state transitions must respect the timing requirements shown in Chapter 5.

The following items pertain to the numbered bubbles above:

1. Host has a message that it desires to send to Node. The first thing that it does is drive MRQ and CS high.
2. The Host then waits for the Node to drive SRDY high. No SPI bus transaction with the Node can occur before this.
3. After SRDY is high, the Host can start with the SPI data transaction. This is accomplished by driving the Node CS line low and then having the Host toggle the SCLK, and MOSI lines and having the Node toggle the MISO line according to the data to be transferred. The SPI Host interface specifies that first a MMsg pair is exchanged.
4. A MHdr pair is exchanged. Note that the payload of the message is appended to the MHdr.
5. The Host detects that the transaction is complete and that it does not wish to send more messages to the Node at this time. It drives the MRQ line low. Since MRQ is low, CS, SCLK and MOSI are tri-stated.
6. At some time in the future, the Node desires to send a message to the Host. It indicates this to the Host by driving SRQ high. Since SRQ is high, the Host drives MRQ and then CS high. It then waits for SRDY to go high, which it already is.

7. The Host starts the SPI data transaction. This is accomplished by driving the Node CS line low and then having the Host toggle the SCLK, and MOSI lines and having the Node toggle the MISO line according to the data to be transferred. The SPI Host interface specifies that first a SMsg pair is exchanged.
8. A SHdr pair is exchanged. Note that the payload of the message is appended to the SHdr.
9. The Node detects that the transaction is complete and that it does not wish to send more messages to the Host at this time. It drives the SRQ line low.
10. The Host detects that SRQ has gone low and that it does not have any messages to send to the Node. It drives the MRQ line low. Since MRQ is low, CS, SCLK and MOSI are tri-stated.
11. The Node drives the SRDY line low after MRQ goes low.

7.5 Host Message SPI Example

This section provides an example Host message exchange from master (Host) to slave (Node). In this example, the Host is sending a version request message.

This example is a zoomed-in view of the example provided previously in Figure 18. This section covers what happens in step 3, which includes the two SPI exchanges initiated by the Host.

With any SPI Host interface message, first an MMsg or SMsg pair must be exchanged. This pair contains information on how big the message is (from the message originator) and how much message queue space is available (on the message destination).

The following diagram shows such an example:

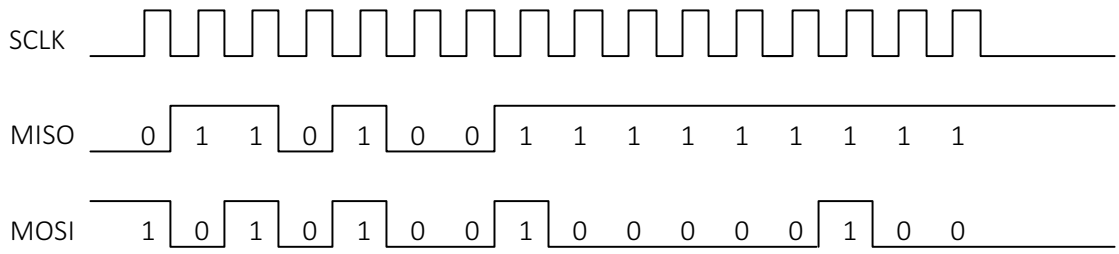


Figure 19. Host Message on SPI – MMsg Pair

The SPI clock edging is configurable with a polarity and phase. In order to communicate with the Node, the SPI clock polarity must be set to "the inactive state value of SPI clock is logic level zero" and the SPI clock phase must be set to "data is captured on the leading edge of SPI clock and changed on the following edge of SPI clock." This means that the data lines (both MISO and MOSI) are read on the SCLK rising edge and are set or cleared on the SCLK falling edge, and is commonly referred to as CPOL=0, CPHA=0.

This illustration shows that the bit streams for MISO and MOSI are:

- MISO: 0110100111111111
- MOSI: 1010100100000100

These bits indicate:

MISO: from slave to master (01)
length of message=2 (10)
opcode=MMsgACK (1001)
buffer size=255 (11111111)

MOSI: from master to slave (10)
length of message=2 (10)
opcode =MMsgREQ (1001)
payload size=4 (00000100)

An MMsg pair or SMsg pair is immediately followed by the corresponding MHdr pair or SHdr pair. This is illustrated below:

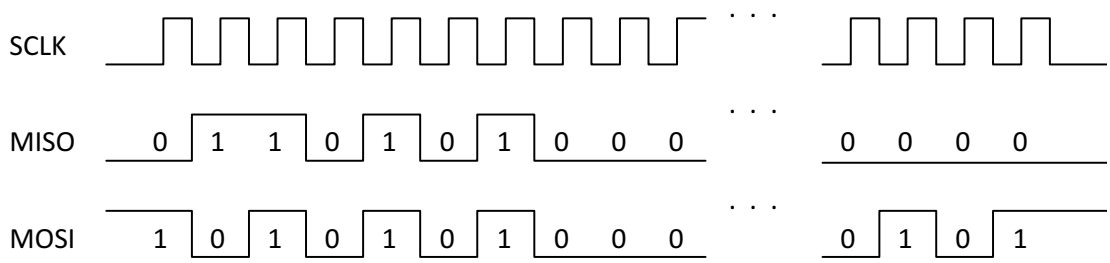


Figure 20. Host Message on SPI – MHdr Pair

For purpose of brevity, this timing diagram shows only a portion of the data exchange. The complete bit streams for MISO and MOSI are as follows:

- MISO: 0110101000000001000000000000000000000000000000000000000000000000000000000000000000000000000000000000
- MOSI: 1010101000000001000010000000000000001010101000000111100001111000010100101101001 00

These bits indicate:

MISO: from slave to master (01)
length of message=2 (10)
opcode=MHdrACK (1010)
Hard coded byte=1 (00000001)
Unused Extra Data (0000……0)

MOSI: from master to slave (10)
length of message=2 (10)
opcode =MhdrREQ (1010)
Hard coded byte=1 (00000001)
Payload:

length=8 (0000100000000000)

message type=VERSION (0001010101000000)

trailing sequence (11110000111100001010010110100101)

- The payload is Little Endian. The least significant byte is transmitted over SPI first.
- All MHdr and SHdr payloads are terminated by the fixed trailing sequence 11110000111100001010010110100101.
- The example above shows a message going from master to slave, thereby having a payload in the master to slave direction appended at the end of the MhdrREQ and no payload appended at the end of the MhdrACK.

7.6 Host Message "Connect" SPI Example

This section provides an example Host message exchange of the CONNECT message from master/Host to slave/Node and subsequent response from the slave to the master.

The timing is similar to the timing illustrated in the previous section, but the data and length of data is different.

The steps involved in this exchange are as follows:

The Host desires to send the CONNECT message to the Node. As described in the previous section, this starts with an MmsgREQ/MmsgACK exchange over the SPI bus.

- MISO: 0110100111111111
- MOSI: 1010100100000110

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MMsgACK (1001)

buffer size=255 (11111111)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MmsgREQ (1001)

payload size=6 (00000110)

The MMsg exchange is followed by the MHdr exchange, which includes the payload of the CONNECT message.

- MISO: 0110101000000001000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000
- MOSI: 1010101000000001000011000000000000001100100100000000000000010000000000000000000000000011110000111100001010010110100101

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MHdrACK (1010)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MhdrREQ (1010)

Hard coded byte=1 (00000001)

Payload:

length=12 (0000110000000000)

message type=CONNECT (0011001001000000)

host interface=True (00000001000000000000000000000000)

trailing sequence (11110000111100001010010110100101)

The payload of the message includes first the length, which is the number of bytes in the payload including the length and the trailing sequence.

It is followed by the message type, which in this case is 0x4032, and corresponds with CONNECT.

The CONNECT message has a 4-byte field that is a Boolean flag specifying whether or not the Node should send asynchronous SPI messages to the Host. To specify that the Node should send messages to the Host, the value of 0x00000001 is used.

It is then followed by the standard fixed trailing sequence.

This message exchange is followed by a Node-initiated message exchange for the purpose of sending an ACK of the CONNECT message to the Host. This starts with a SmsgREQ/SMsgACK exchange over the SPI bus.

- MISO: 0110101100000100
- MOSI: 1010101111111111

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=SMsgACK (1011)

buffer size=255 (11111111)

payload size=4 (00000100)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =SmsgREQ (1011)

buffer size=255 (11111111)

The SMsg exchange is followed by the SHdr exchange, which includes the payload of the ACK message.

- MISO: 0110110000000001000010000000000000110000000000001111000011110000101001 0110100101
- MOSI: 1010110000000001000000000000000000000000000000000000000000000000000000000000000000000000

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=SHdrACK (1100)

Hard coded byte=1 (00000001)

Payload:

length=8 (0000100000000000)

message type=ACK (0011000000000000)

trailing sequence (11110000111100001010010110100101)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =ShdrREQ (1100)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

8 nanoNode Provisioning

Provisioning a node consists of updating (if necessary) node firmware version, applying a configuration to the node, and providing security keys to the node. The node configuration and security keys must match the target network where the node will be deployed and, after provisioning, the node-specific key must be provided to the network operator. The provisioning software package is used to perform these steps. For further information, please see the *Provisioning Guide (0010-0074-00)*.

In the near future, the provisioning step will not be required for Global and U.S. public networks. Pre-Provisioned Nodes will be the default of what ships from the factory.

9 Antenna Diversity

The nanoNode supports Antenna Diversity for optimal System performance. In many cases, the nanoNode and Host system are mounted in fixed locations that often experience nulls in the RF coverage. Antenna Diversity can help with optimization of the RX and TX paths. In marginal coverage areas, an RF null could easily disadvantage the nanoNode to force it to transmit at a higher TX Power (more battery energy) or cause network loss and frequent rescanning to reacquire the network (again, more energy).

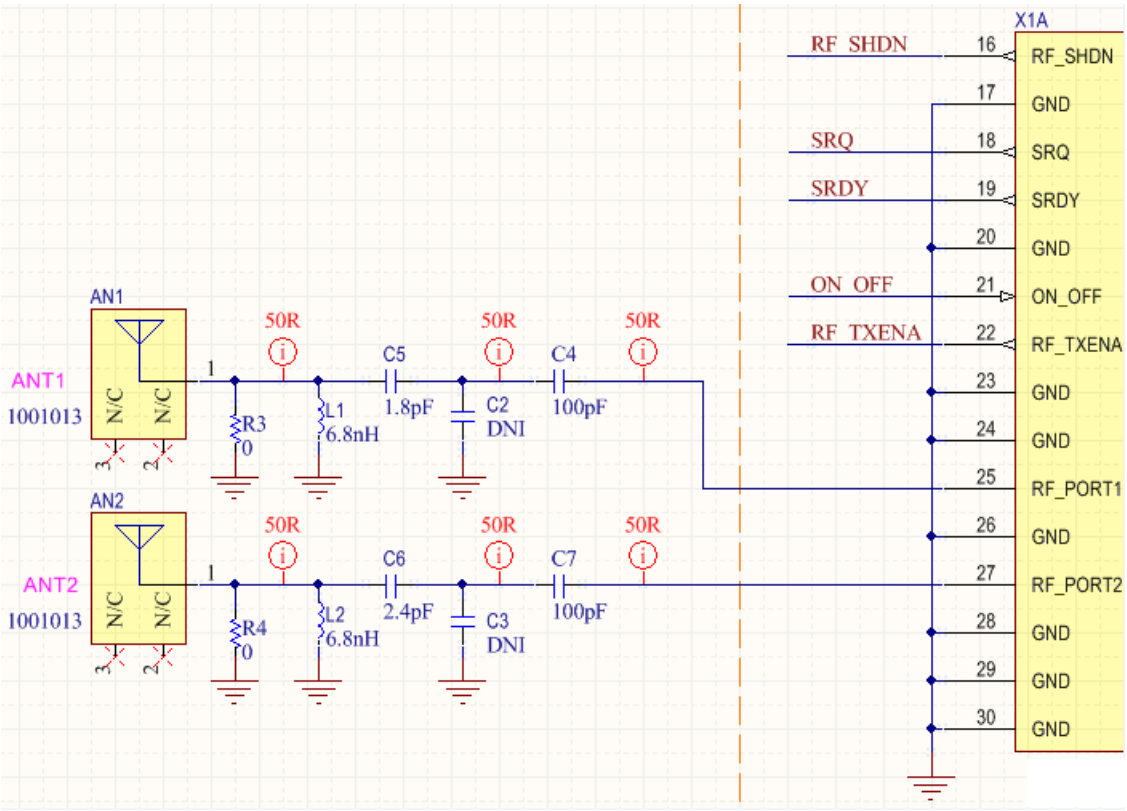


Figure 21. Antenna Diversity with Ethertronics

9.1 Antenna Design Considerations

- Good antenna design is also crucial to success. It is important to consider some pertinent issues. Ingenu and our partners provide a service to review your PCB layout to ensure good RF design practices have been followed. Ingenu and our partners provide a service to field test the antenna performance of your device, vs. a perfect reference. Over time we have found that good RF performance is possible, even in tight enclosures, if we work cooperatively.

- Ceramic antennas can work well but may sometimes have issues. Careful testing must be done to ensure desired gains and radiation patterns.
- The product must be researched in conjunction to the Access Point, its deployment, and its antenna radiation pattern. Nominally the Access Point will be mounted on a tower or mountain with a downward tilt. The nanoNode and System may be mounted vertically or horizontally—forcing requirements on the optimal radiation pattern of the nanoNode.
- The antenna must be well matched and with low loss between nanoNode and antenna. It is important to follow the manufacturer's recommendations. The use of low tolerance ceramic capacitors and low tolerance thin film inductors are recommended. Examples include the Murata GJM series of capacitors and LQP series of inductors. If using stripline RF port feeds, care must be employed to ensure low loss and proper impedance. The antenna match may change when fully integrated into a product. Is advised to recheck the match after full integration. During tuning this may require the use of so called "RF pigtails" in an ad hoc fashion. If the Bill of Materials (BOM) cost will allow, a special connector can be implemented to support this verification/optimization.
- Metallic objects nearby to the antenna can affect radiation gains, patterns, and power match. Typically anything within about 4-5 inches can affect the match significantly particularly if the nearby metal is resonant at 2.4 GHz. A little pattern distortion usually is not of too much concern unless deep wide angular nulls in the antenna pattern results. Other types of pattern distortion can be caused by absorptive losses due to lossy dielectrics nearby the antenna, which represents real power loss dissipated as heat in the loss object. This represents power that is completely lost and not radiated in a useful direction.
- Noisy System clocks with harmonics can fall into the operating band of the nanoNode and can be picked up by the antennas—degrading sensitivity, or causing Electromagnetic Compatibility (EMC) regulatory issues.

9.2 Diversity Considerations

The operating frequency of the nanoNode is the ISM 2.4 GHz band. This has a wavelength of 12.3 cm in air. For optimal null/peak diversity detection, the antennas must be separated by at least 2.5" (5 cm). It is a good idea on the diversity antenna to orient it 90 degrees from the main antenna in order to improve the polarization diversity and increase spatial de-correlation.

Practical ground plane-independent antennas are preferable to those that require the printed circuit board (PCB) copper for the antenna counterpoise. Examples of these are dipole antennas and some chip patch antennas. However these can be cost adders in certain cases. It should be noted however that some chip antennas that use the PCB for ground return have been shown to produce reasonable performance.

10 Regulatory Considerations

The nanoNode uses LGA pads for its RF ports. This lowers the unit cost and provides greater host configuration flexibility in the final application. Modular certifications (FCC, ISED, ETSI, Japan and others) have been obtained for the nanoNode. The existence of the modular certification minimizes cost and time to market for customers. The certification documents and the results of the certification tests are available to system integrators upon request.

The modular certification of the nanoNode can be re-used by customers that utilize an equivalent layout and stack-up as our reference design platform. Additional testing for verification purposes may still be required per FCC or other regulatory body guidelines and requirements but will vary on a case-by-case basis. Customers are advised to consult with the regulatory compliance test house of their choice for the best way to proceed.

Additionally, Ingenu has prepared certification guidelines on how to use the software and system tools required for certification. Some markets (such as FCC/ISED) are fairly straight forward for certification and are largely TX Spectrum-based. Other markets may require a much more sophisticated FER process involving an Access Point and Quick Start System. These procedures are defined in the document entitled *EMC Compliance Guide (010-0037-00).* This document also includes hints and recommendations to help make the process as easy as possible. For more information about this document, see section 1.3: References/Tools.

10.1 Block Diagram

Some regulatory domains require a block diagram of the module for their documentation similar to that shown in the following figure.

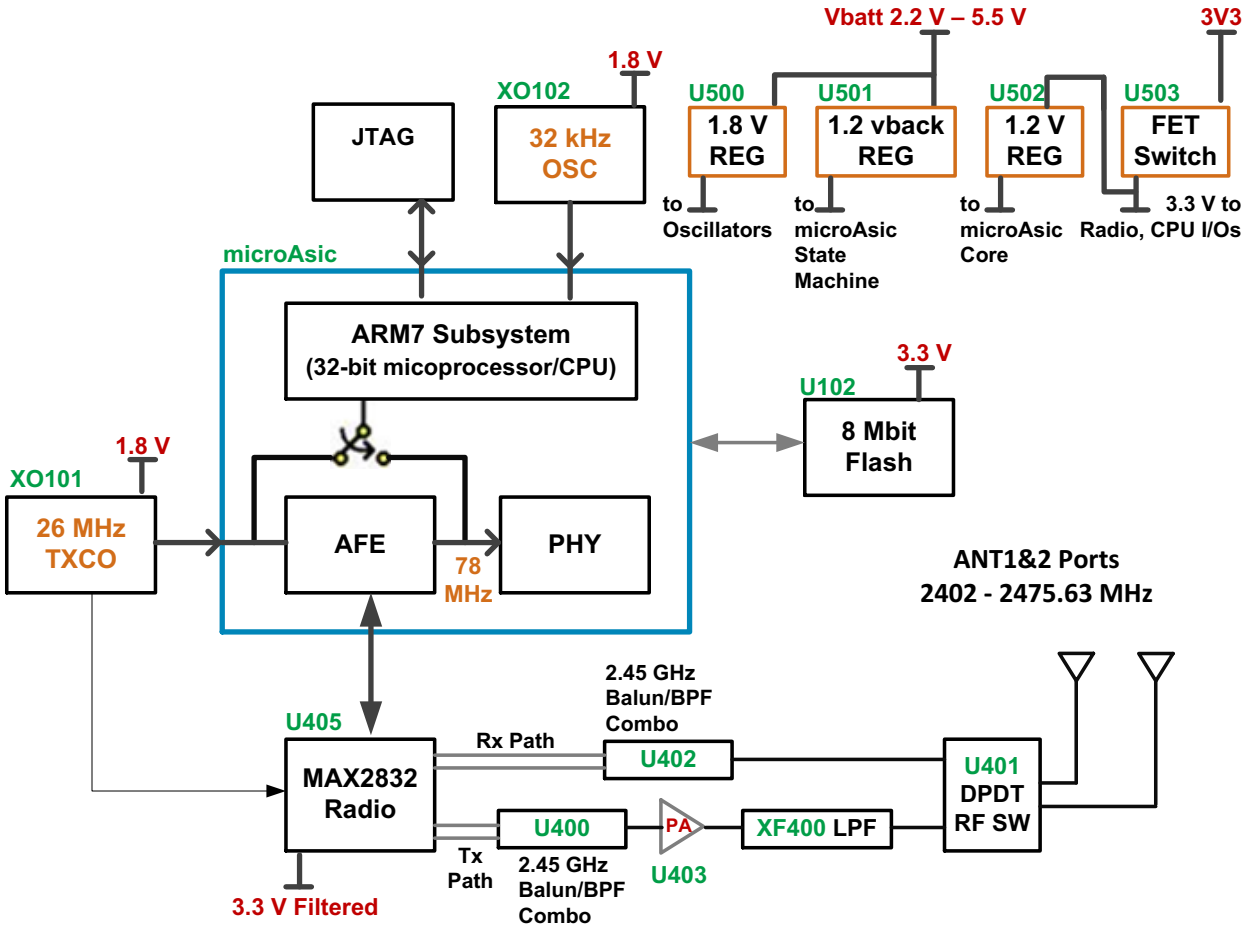


Figure 22. nanoNode Block Diagram

10.2 Antennas

This nanoNode has two antenna ports that have been certified to operate with the antennas listed below. To adhere to these certifications requires the antennas to be of the types specified below and of lower gain. In all instances, the combinations of nanoNode maximum transmit power and antenna gain must not exceed the regulatory Effective Isotropic Radiated Power (EIRP). Antennas that are not of the specified type or are of greater gain are strictly prohibited for use with the nanoNode, per EMC certifications. The required antenna impedance is 50 ohms.

Table 7. nanoNode: EMC Certified Antennas

Application	Manufacturer	Part Number	Gain	Type	Connector	Comment
FCC/ISED All	Laird	0600-00012	9 dBi	Monopole	MMCX	
ETSI, Generic	Ethertronics	1001013	2.1 dBi	Monopole	Internal PCB chip antenna	10 dBm EIRP

Application	Manufacturer	Part Number	Gain	Type	Connector	Comment
ETSI, C.1	Laird	0600-00012	5 dBi	Monopole	MMCX	27 dBm EIRP (per EN 300 440 - 1 Annex C.1) must not be exceeded

10.2.1 Host Antenna Trace Design

To connect RF signal from the module's RF pins to the antenna, RF connector, or matching network, 50 ohm-controlled impedance traces should be used. Vias may be used to transition the RF from one signal layer to another signal layer.

The following controlled impedance RF traces (i.e., microstrip types) are allowed:

- Surface microstrip
- Surface coplanar waveguide (CPWG)
- Surface ground-backed CPWG
- Embedded microstrip
- Embedded CPWG
- Embedded ground-backed CPWG
- Stripline
- Asymmetrical stripline

10.2.2 Controlled Impedance Trace Design

10.2.2.1 Dimensions

The controlled impedance trace should have dimensions that correspond to 50 ohm ± 10% no matter what the specific microstrip type is. The specific design depends on trace width, thickness, dielectric constant, and distance to grounds. These dimensional factors are controlled by the PCB fabrication shop. From a design perspective, on the PCB fabrication drawing, clearly mark that the microstrip trace requires controlled impedance of 50 ohm ± 10%. Also specify that the PCB shop must test to confirm that the impedance is within 10% of 50 ohms.

10.2.2.2 Ground Planes

All microstrip types except surface CPWG and embedded CPWG requires ground planes either above the RF trace, below the RF trace, or both above and below the RF trace. In these cases with ground planes, the RF trace must not cross any splits in the ground plane. The ground plane directly above and below the RF trace must be continuous.

10.2.2.3 Matching Network

A matching network may be used at the module's RF pin to ensure good 50 ohm transition between the host board and the module. Another matching network may be used on the antenna side of the controlled impedance trace to match the antenna to 50 ohms.

10.2.2.4 Stitching Vias

Ample ground stitching vias should be used around the connectors, trace, and module. It is recommended that a via stitching pattern be used with no more than 0.25" separation between adjacent vias.

10.2.2.5 Isolation

Since the RF signal coming from the module has already been filtered, there is no isolation requirement.

10.2.2.6 Example RF Trace Design

The following figure shows surface-ground backed CPWG design with 22 mil trace width, 15 mil gap-to-surface ground plane, 2 mil thick top layer (1/2 oz copper + plating), 14 mil dielectric thickness to solid ground plane underneath, and a FR-4 dielectric constant of 4.4. This configuration achieves the desired 50 ohm ± 10% for the controlled impedance. Note that in this design, a pi-matching network exists to match the antenna. This is recommended but not necessary if the antenna is already matched with VSWR of 1.5:1 or better. Note that antennas should not have gain at the harmonic frequencies and only dipole-type antennas should be used. Antennas with gain at the fundamental frequency of more than 9 dBi should not be used.

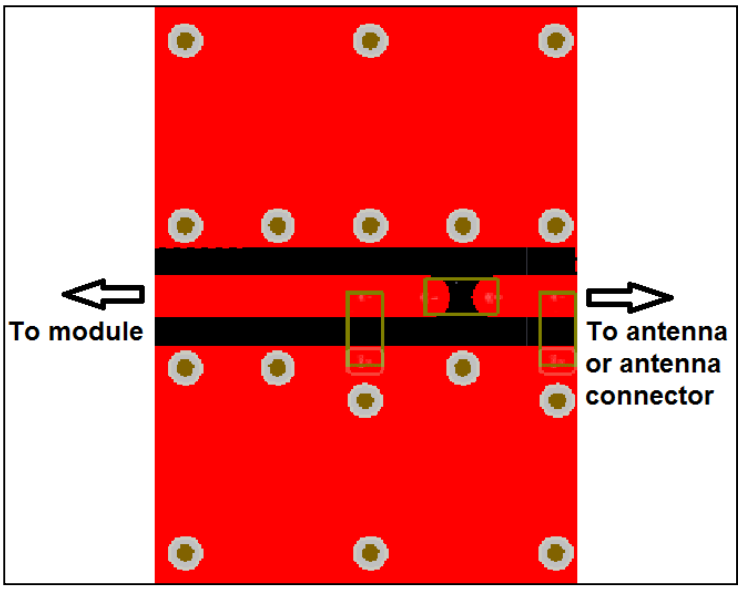


Figure 23. Controlled Impedance RF Trace Design

Other controlled impedance RF trace configurations are acceptable as long as the characteristic impedance stays within the boundary limit of 50 ohm ± 10%. Most PCB fabrication shops can adjust the trace width of the controlled impedance traces such that 50 ohms is maintained. The PCB shop must guarantee the impedance of the traces to within the 50 ohm ± 10% boundary limit by impedance testing the PCBs.

10.3 Certifications

The nanoNode is designed to meet regulations for world-wide use. It is certified in the United States, Canada, and Europe as a Limited Single Module. The certifications currently achieved are listed in the following table.

Table 8. nanoNode Certifications

Country	Certifying Agency	Certification(s)
United States	Federal Communications Commission (FCC)	■ 15.247 for RF TX bandwidth, power, conducted and radiated emissions.
Canada	Innovation, Science and Economic Development Canada (Formerly Industry Canada)	■ RSS247, includes FCC tests and ISED-specific tests (RX radiated emissions).
Europe	European Telecommunications Standards Institute (ETSI)	■ 300 440-1 and 440-2, ETSI Emissions. ■ 301 489-1, ETSI Immunity.

Additional details can be found in the document entitled *EMC Compliance Guide (010-0037-00)* referenced in Chapter 1: Overview.

The integrator of the final product is often required to do additional compliance tests. The integration application and market will determine specifics. The integrator is advised to consult with local experts in compliance certifications for complete information.

- **FCC/ISED**
  The nanoNode is Single-Modular Certified, therefore the final product may only need Class B unintentional radiator and powerline conducted emissions tests. This should be done with the actual production antenna and power supply. Please refer to appendix B for PCB design considerations.

Customers are free to follow one of three paths in their final product evaluations:

- Class I permissive change: Customers can use one of Ingenu approved antenna types shown above that are of equal and lesser gain along with the antenna PCB reference designs. This path allows customers to use On-Ramp Wireless' certifications (owned by Ingenu). While ideal from the perspective of program cost and schedule, the ability to reuse this antenna is highly dependent on the application.

- Class II Permissive change: If there are minor changes when integrating the module and application with the FCC or ISED the On-Ramp Wireless certifications can still be used. These changes could be a higher antenna gain, different PCB characteristics, or collocated transmitters as an example. In the case of FCC/IC EMC certifications, if a different antenna type or higher gain antenna is used, it is required that the final product be recertified with the nanoNode.
- New FCC ID: Customers can obtain a new FCC ID for their product with the Ingenu approved modules. In this case it is up to the manufacturer of the host equipment to arrange certification. Any support documentation is available from On-Ramp Wireless.

  NOTE: For customers opting to re-certify on their own with different layout, stack-ups, and antennas, etc., it is important that the nanoNode is presented with a 50Ω load. To that end, it is recommended that the RF trace from the nanoNode to the antenna be outfitted with a Pi network, near the antenna, for matching during the development phase of a host board.

- **ETSI**
  Europe's system is a self-declaration system. There are no documents to submit or certification grants to obtain. One must have the passing test results available for all applicable requirements at any time if challenged. The nanoNode has been verified and qualified for two operational scenarios under EN 300 440-1:
  - Generic with a maximum of 10 dBm EIRP (2402 – 2475.63 MHz)
  - Annex C.1 with a maximum of 27 dBm EIRP (2447 – 2452.94 MHz)

  The actual minimum/maximum channel frequencies are shown below.

Table 9. nanoNode Minimum/Maximum Channel Frequencies for Annex C.1 Applications

Node Type	Minimum/Maximum Channel Frequencies
nanoNode	2447 – 2452.94 MHz

- Other countries will vary.

10.4 FCC Warnings

This device complies with part 15 of the Federal Communications Commission (FCC) Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

WARNING: This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the instructions, this equipment may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Re-orient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

10.5 ISED Warnings

CAN ICES-3 (B)/NMB-3(B)

Canadian Two Part Warning Statement:

The installer of this radio equipment must ensure that the antenna is located or pointed so that it does not emit RF field in excess of Health Canada limits for the general population. Consult Safety Code 6 which is obtainable from Health Canada's website http://www.hc-sc.gc.ca/index-eng.php.

This device complies with Innovation, Science and Economic Development (ISED) licence-exempt RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference, and

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

To reduce potential radio interference to other users, select the antenna type and its gain so that the equivalent isotropically radiated power (EIRP) is not more than that permitted for successful communication.

L'installateur de cet équipement de radio doit veiller à ce que l'antenne est située ou est pointée de façon à ne pas dégager de champ RF dépassant les limites de Santé Canada pour la population générale. Consulter le Code de sécurité 6 qui peut être obtenu sur le site Web de Santé Canada http://www.hc-sc.gc.ca/index-eng.php

Cet appareil se conforme aux Cahiers des charges sur les Normes Radioélectriques (CNR) d'Industrie Canada applicables aux appareils de radio exempté de licence. Son fonctionnement se soumis aux deux conditions suivantes :

(1) l'appareil ne doit pas produire d' interférences, et

(2) l'utilisateur de l'appareil doit accepter tout interférences radioélectrique subi, même si les interférences sont susceptible d'en compromettre le fonctionnement.

Pour réduire les interférences radioélectrique pour les autres utilisateurs, sélectionnez le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (PIRE) ne soit pas supérieure à celle permise pour réussir une communication.

10.6 ETSI Warnings

None known.

10.7 Usage

This device is only authorized for use in fixed and mobile applications. This device cannot be collocated with other wireless transmitters without performing simultaneous transmission evaluation.

nanoNode RF Certification IDs:

- FCC ID: XTE-NODE103
- IC: 8655A-NODE103

10.7.1 Product Labels

If the nanoNode is visible in a product, the label showing the FCC ID and ISED designators (listed above) must be visible from the exterior of the product. A representative nanoNode label is shown below.

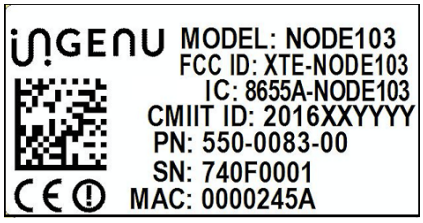


Figure 24. Product Label

If the nanoNode is contained within a product and is ***not*** visible, a label showing the FCC ID and ISED designators (listed above) must be affixed to the exterior of the device containing the nanoNode. The exterior label must state the following:

Contains FCC ID: XTE-NODE103, ISED: 8655A- NODE103

10.7.2 RF Exposure Statement

The air interface supports operation on channels in the 2402 MHz –2475.63 MHz range for FCC/ISED and ETSI regulatory domains. Before the nanoNode becomes operational, it must undergo a Provisioning procedure, during which critical information required for operation is entered into the device and stored in non-volatile storage. It is during the initial commissioning procedure that the regulatory domain, under which the device will operate, is set. Subsequent configuration of the device during operation is checked against the commissioned regulatory domain and non-permitted channels or transmit power levels are rejected and the device will not transmit until a permissible configuration per the commissioned regulatory domain is set.

10.8 WEEE Directive

The WEEE directives do not apply to nanoNodes as they are not considered "end products" that would put them under the WEEE initiatives in the EU.

10.9 REACH Directive

The nanoNodes are REACH compliant under 1907/2006/EC. This certification is located in Appendix D.

10.10 RoHS Directive

The nanoNodes comply with RoHS directive 2002/95/EC. Ingenu has received Certificates of Conformance (CoC) for all components, printed circuit boards, and contract manufacturers for the nanoNodes. The RoHS Certification of Conformance is provided in Appendix D.

10.11 Export Compliance

The nanoNode complies with the export requirements of the Bureau of Industry and Security and relevant information is provided below. For details relating to export compliance for the nanoNode, refer to the CCATS numbers provided in the following table.

Table 10. ECCN and CCATS Information

ECCN	CCATS
ECCN 5A002a.1	G164372

11 Manufacturing Considerations

This section deals with manufacturing details such as:

- Design of Host PCB for mounting the nanoNode
- The manufacturing process and soldering profile
- The validation and configuration of the nanoNode after the assembly process

11.1 Mechanical Outline

The nanoNode is a bottom termination component (BTC) that is designed to be directly surface-mounted onto a Host PCB. All signals (including power, grounds, RF, and digital interface) are brought through the 30 bottom terminations of the module. The mechanical outline of the PCB is detailed in Appendix G: nanoNode Mechanical Drawing.

11.2 Host PCB Constraints

For Host layout, please refer to Appendix B: PCB Land Pattern. It is important to use the recommended land pattern as well as consider coplanarity of the Host in order to get optimal yield in manufacturing. Coplanarity is defined as the bow and twist of the nanoNode and Host PCBs. Careful measurements of the nanoNode have been made such that it meets flatness specifications.

11.3 Handling Procedures for nanoNode

The nanoNodes are packaged in trays that are then sealed in moisture-barrier bags. The nanoNode printed circuit assemblies are moisture sensitive to MSL Class III per IPC/JEDEC J-STD-033.

The nanoNode is manufactured using lead free, no clean processes. It is recommended that the module ***not*** be washed due to the difficulty of ensuring cleanliness after processing.

All processes used to manufacture the nanoNode are RoHS compliant. The following is recommended:

- Solder Type: SAC305 ROLO/No Clean per IPC J-STD-004
- Solder Wire Type: SAC305 ROLO/No Clean per IPC-J-STD-006
- SMT Reflow Profile: Per IPC-7530
- Workmanship: Per IPC-A-610
- Cleaning and Cleanliness Testing: Per J-STD-001 (Requirements for Soldered Electrical Electronic Assemblies)

12 Errata

Degraded RF Channels

Ingenu and our partners are deploying networks globally. We carefully manage the frequency allocations of these networks to avoid using the 3 (out of 38 possible) RF channels described below. Ingenu networks can deploy overlapping coverage (ie. all Access Points) on a single 1MHz RF channel. The other channels are held in reserve for future use or special cases. Three lower performing channels are listed below, for reference.

The nanoNode uses a Channel scheme such as the following:

- Channel 1 = 2402 MHz and each successive channel is 1.99 MHz offset to that Channel 1.
- Channel 2 = 2403.99 MHz
- Channel 3 = 2405.98 MHz
- Etc.

The nanoNode uses a 26 MHz reference clock for processing and for the direct conversion radio. It has been found that 26 MHz harmonics can create strong tones that cause some RF sensitivity degradation on these harmonic channels.

- 93*26 MHz = 2418 MHz. This affects channel 9.
- 94*26 MHz = 2444 MHz. This affects channel 22.
- 95*26 MHz = 2470 MHz. This affects channel 35.

System integrators should NOT use these 3 channels as nanoNode RX sensitivity can be degraded by a nominal 3-10 dB.

Appendix A Abbreviations and Terms

Abbreviation/Term	Definition
ACPR	Adjacent Channel Power Ratio
AGC	Automatic Gain Control
ALC	Automatic Level Control
AP	Access Point
API	Application Programming Interface
ASIC	Application-Specific Integrated Circuit
ATE	Automated Test Equipment
BOM	Bill of Materials
BW	Bandwidth
CCATS	Commodity Classification Automated Tracking System. An alphanumeric code assigned by the Bureau of Industry and Security (BIS) to products that it has classified against the Export Administration Regulations (EAR).
CMOS	Complementary Metal-Oxide-Semiconductor
CPOL	Clock Polarity (for SPI)
CPU	Central Processing Unit
DBPSK	Differential Binary Phase Shift Keying
DFS	Dynamic Frequency Selection
DPLL	Digital Phase-Locked Loop
DSSS	Direct Sequence Spread Spectrum
EIRP	Effective Isotropic Radiated Power
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FER	Frame Error Rate
GND	Ground
GPIO	General Purpose Input/Output
HBM	Human Body Model
ISED (IC)	Innovation, Science and Economic Development Canada (Formerly Industry Canada
IIP_3	Input Third-Order Intercept Point

Abbreviation/Term	Definition
LDO	Low Drop Out
LNA	Low Noise Amplifier
LO	Local Oscillator
MISO	Master Input, Slave Output
MM	Machine Model
MOSI	Master Output, Slave Input
MRQ	Master Request
MSL	Moisture Sensitivity Level
nanoNode	A small form factor, wireless network module developed by Ingenu that works in combination with various devices and sensors and communicates data to an Access Point.
Node	The generic term used interchangeably with nanoNode.
OTA	Over-the-Air
Po	"Power Output" for the RF Transmitter
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
POR	Power On Reset
QoS	Quality of Service
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMA	Return Merchandise Authorization
RoHS	Restriction of Hazardous Substances
RPMA	Random Phase Multiple Access. The Ingenu proprietary wireless communication technology and network.
RP-SMA	Reverse Polarity Subminiature version A connector
RSSI	Receive Signal Strength Indicator
RT	Remote Terminal
RTC	Real Time Clock
RX	Receive/Receiver
SCLK	Serial Clock
SMT	Surface Mount Technology
SNR	Signal-to-Noise Ratio
SPI	Synchronous Peripheral Interface
SRAM	Static Random Access Memory
SRDY	Slave Ready
SRQ	Slave Request

Abbreviation/Term	Definition
TCXO	Temperature Compensated Crystal Oscillator
TX	Transmit/Transmitter
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio
XO	Crystal Oscillator

Appendix B PCB Land Pattern and Keepouts

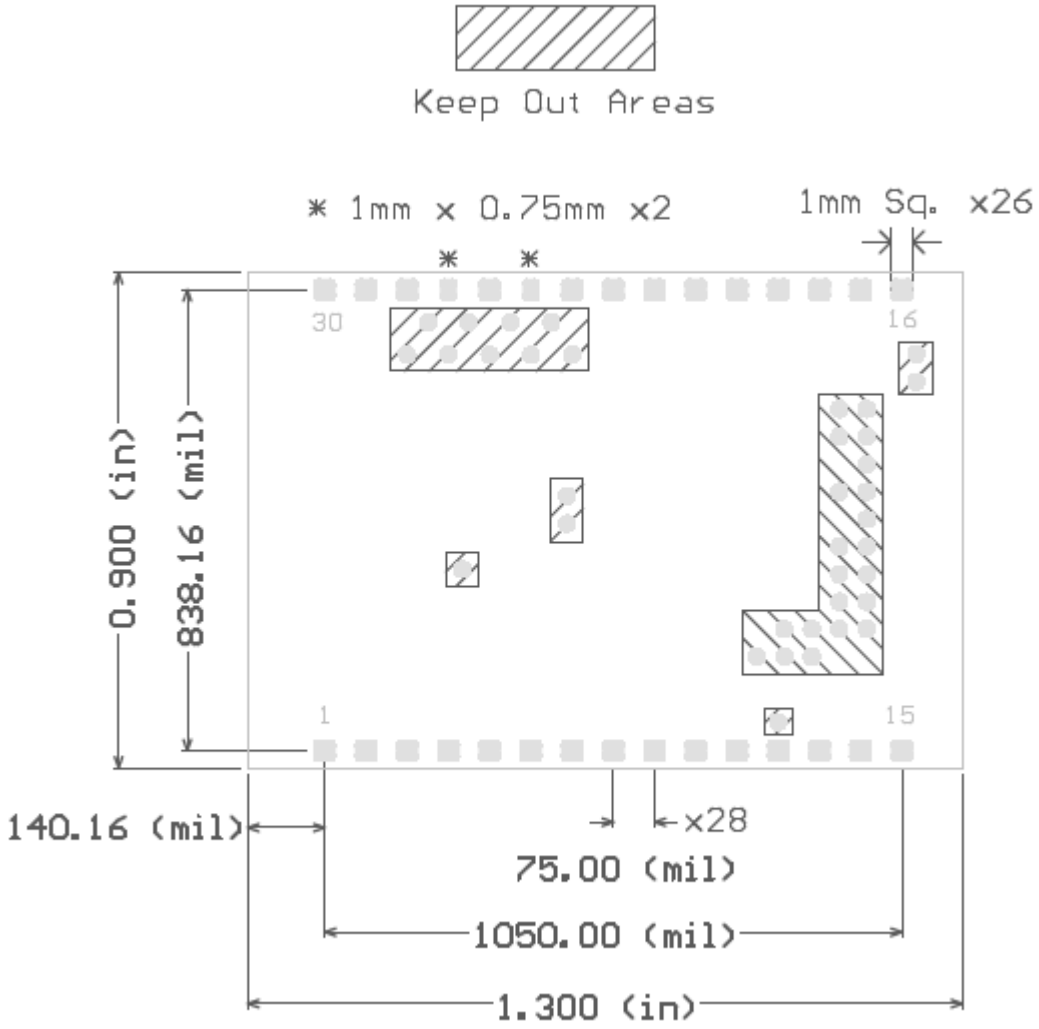


Figure 25. nanoNode PCB Land Pattern

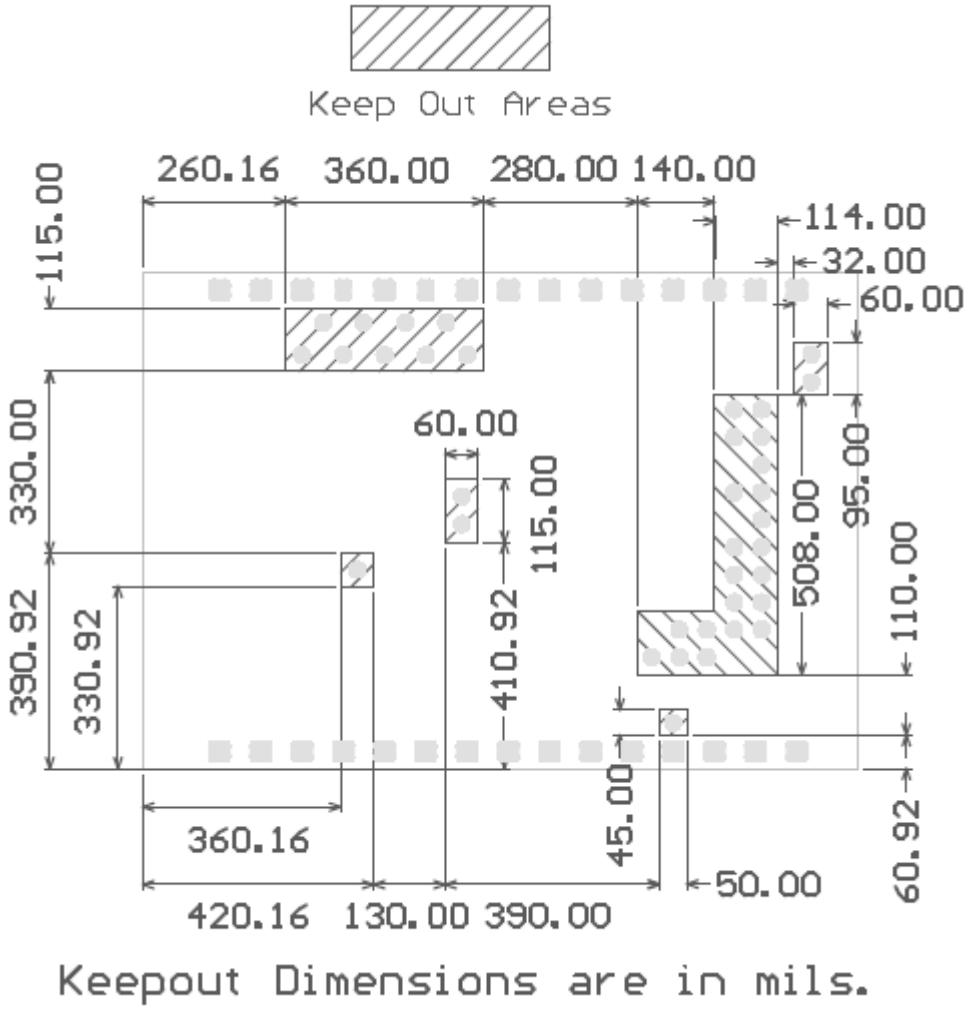


Figure 26. nanoNode PCB Land Pattern Keepouts

Appendix C nanoNode/microNode Pin Comparison

The following table provides a pin comparison between the nanoNode and the microNode.

Table 11. nanoNode/microNode Pin Comparison

microNode Pin #	Name	nanoNode Pin #	Signal Direction Relative to nanoNode	Signal Type	Comment	microNode to nanoNode Comparison
-		1	WAKE	CMOS_O	Output of nanoNode to indicate Awake (RX/TX = High) or Sleep mode (WAKE = Low)	nanoNode uses this to control external 3.3V power supplies, but is not applicable for microNode
1, 2, 3, 4, 7, 10, 11,14, 17, 20, 21, 26, 30, 31, 34, 35, 37, 38, 40	Ground	2, 5, 8, 11, 14, 17, 20, 23, 24, 26, 28, 29, 30	Power	Power	Ground return. Should be low RF impedance to a solid ground plane of the Host	Same
5, 6	VBATT		Power	Power	Input power, 2.2-5.5V.	Same
-	-	4	Power	Power	POWER	3.3 Volts, unique to nanoNode
8	SRQ	18	Output	CMOS_O	Slave Request	Same
9	SRDY	19	Output	CMOS_O	Slave Ready	Same
12	SCLK	6	Input	CMOS_I	SPI Clock	Same
13	MISO	7	Output	CMOS_O	SPI Master Input Slave Output	Same
15	CS	9	Input	CMOS_I	SPI Chip Select	Same

microNode Pin #	Name	nanoNode Pin #	Signal Direction Relative to nanoNode	Signal Type	Comment	microNode to nanoNode Comparison
16	MOSI	10	Input	CMOS_I	SPI Master Output Slave Input	Same
18	MRQ	12	Input	CMOS_I	Master Request	Same
19	3V3	4	Power: ■ microNode: output ■ nanoNode: Input	Power	Power	Different: ■ The microNode supplies a nominal 3.3V T/R switch. ■ The nanoNode requires this as an input.
22	RESET_N	N/A	■ MicroNode: Input ■ nanoNode: N/A	OC_1	RESET input	Different: ■ microNode has this pin ■ nanoNode does not have this pin
23	USTATUS	N/A	I/O	CMOS_O, CMOS_I	USTATUS. To be used by the nanoNode as a GPIO. Undefined at this time. Float for now.	Different: ■ microNode has this pin ■ nanoNode does not have this pin
24	POWER_ON	21	Input	CMOS_A	This is used to turn ON/OFF the Internal Power supplies of the nanoNode.	Same
25	ANT_SEL	N/A	Output	CMOS_O	This is used by the nanoNode to control its antennas for diversity.	Different: ■ microNode has this pin ■ nanoNode does not have this pin
27	UART_SIN	N/A	Input	CMOS_I	UART Serial input. Not supported at this time.	Different: ■ microNode has this pin ■ nanoNode does not have this pin
28	UART_SOUT	N/A	Output	CMOS_O	UART Serial output. Not supported at this time.	Different: ■ microNode has this pin ■ nanoNode does not have this pin

microNode Pin #	Name	nanoNode Pin #	Signal Direction Relative to nanoNode	Signal Type	Comment	microNode to nanoNode Comparison
29	TOUT	13	Output	CMOS_O	TOUT is a normally low signal that pulses high in response to specific Network Timing Events	Same
32	RF_PAEN_EXT	N/A	Input	CMOS_I	This is used to force the PA off. It is internally pulled low. Do not connect at this time.	Different: ■ microNode has this pin ■ nanoNode does not have this pin
33	RF_TXENA	22	Output	CMOS_O	This signal is used to indicate status of the Power Amplifier for the nanoNode: Low = OFF High = Enabled (Transmitting)	Same
36	RF1	25 (RF1), 27 (RF2)	RF RX/TX	50 Ohm	This is the RF input/output for the nanoNode. It is a 50 Ohm castellated "pin."	■ microNode has this pin ■ nanoNode has two ports: RF1 (primary) and ANT2 (secondary
39	RF_SHDN		RF Shutdown	CMOS_O	This pin indicates the status of the RF Transceiver for the nanoNode: Low = Shutdown High = Active	Same
N/A	TIME_QUAL	15	Output	CMOS_O	This pin is used by the Extender for Node-based timing derivation.	■ microNode does not have this pin ■ nanoNode has this pin. Do Not Connect.

1. OC_1
2. CMOS_A
   a. The CMOS_A pin is used to control two Analog Regulators and their Enable pins.
   b. The pin has hysteresis.
      - Going High (Active): V input High is 1.2V

- Going Low (OFF): V input Low is 0.4V

c. When the nanoNode is ON, this pin consumes a nominal 0.2 µA but as maximum of 2 µA over the entire temperature range.

3. CMOS_I

   The Node input voltages are 3.3V CMOS levels. VIH = 2.0V (minimum) and VIL = 0.8V (maximum).

4. CMOS_O

   The Node output voltages are 3.3V CMOS levels (4mA). VOH = 2.4V (minimum) and VOL = 0.4V (maximum).

5. SPI inputs to the node (SCLK, MOSI, CS) must be tri-stated or driven low when the node may be sleeping (MRQ and SRQ are both low). See section 5: SPI Interface and Sequences for more details.

Appendix D REACH and RoHS Compliance

FLEXTRONICS

CERTIFICATION OF CONFORMANCE

We hereby declare that the products(ORWH-550-0022-00, ORWH-550-0006-00, ORWH-550-0026-00, ORWH-550-0015-00, ORWH-550-0017-00) supplied are assembled and produced together with homogeneous materials and processes that are comply with RoHS (2011/65/EU) and REACH (1907/2006/EC) to the best of our knowledge.

This certificate of compliance does not in any way serve to certify that any product itself (including its constituent components) manufactured by Flextronics (Nanjing) Technology Co., Ltd or any production materials which have been specified by the customer is in compliance with such laws/regulations.

Flextronics (Nanjing) Technology Co., Ltd

(Date, 11th February 2014)

FEHSP-4.4.6-08-F002

Appendix E RMA Process

For full details about the Return Material Authorization (RMA) process, refer to the document entitled *Return Material Authorization Procedure (008-0013-00).*To obtain an *RMA Request Form*, contact your Ingenu representative and request document number *007-0003-00*.

The diagrams/schematics in this appendix are provided as examples.

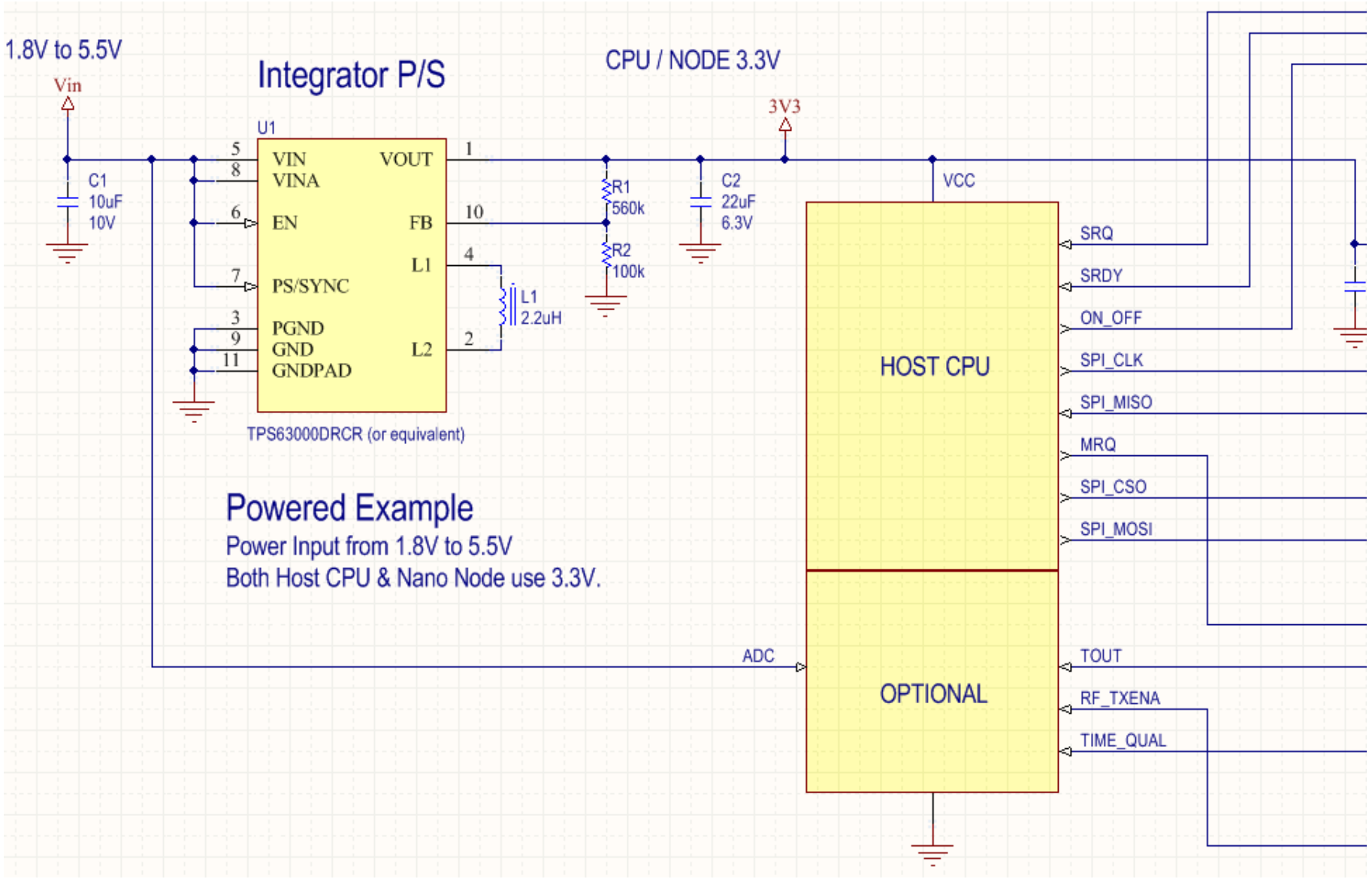


Figure 27. Powered Example

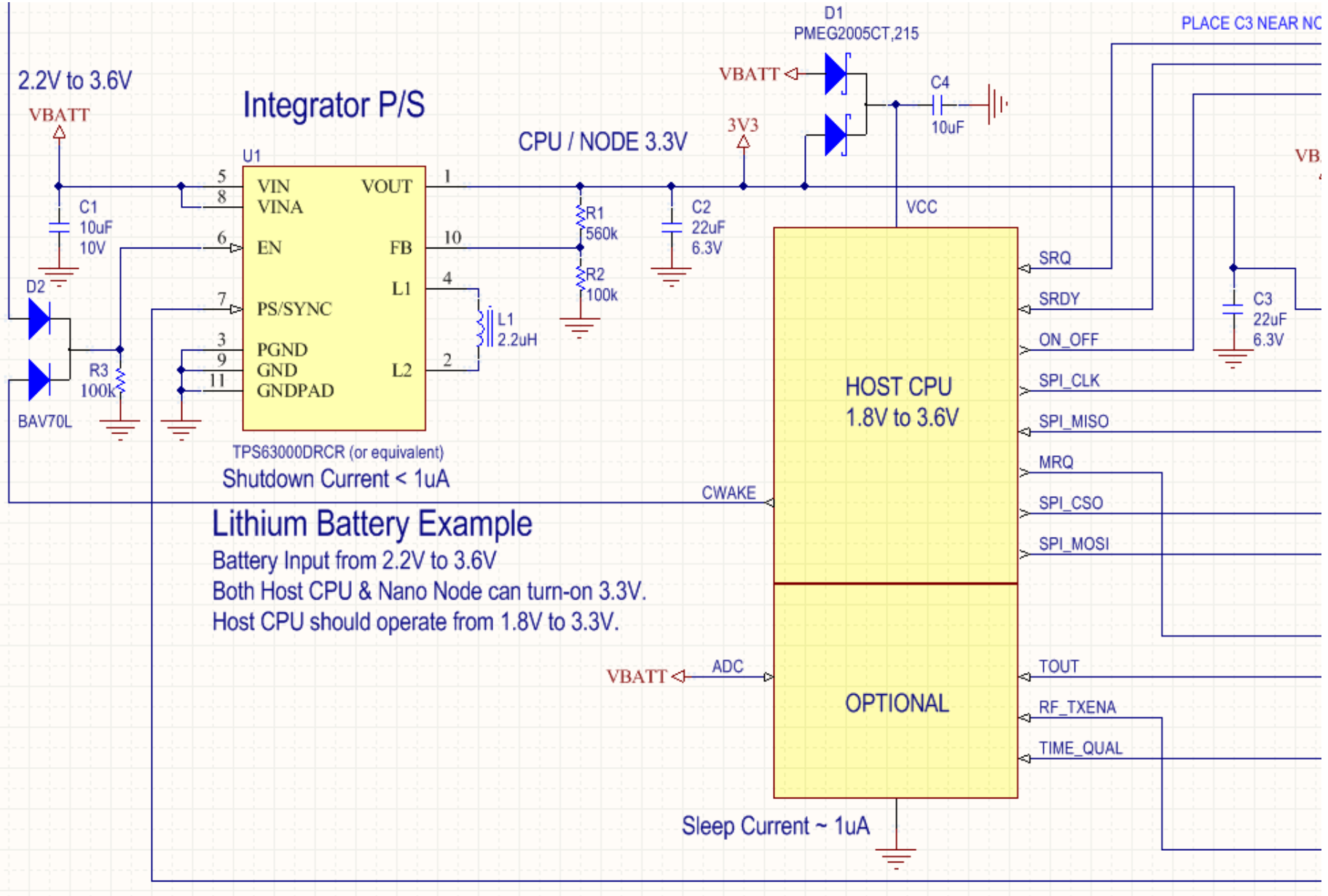
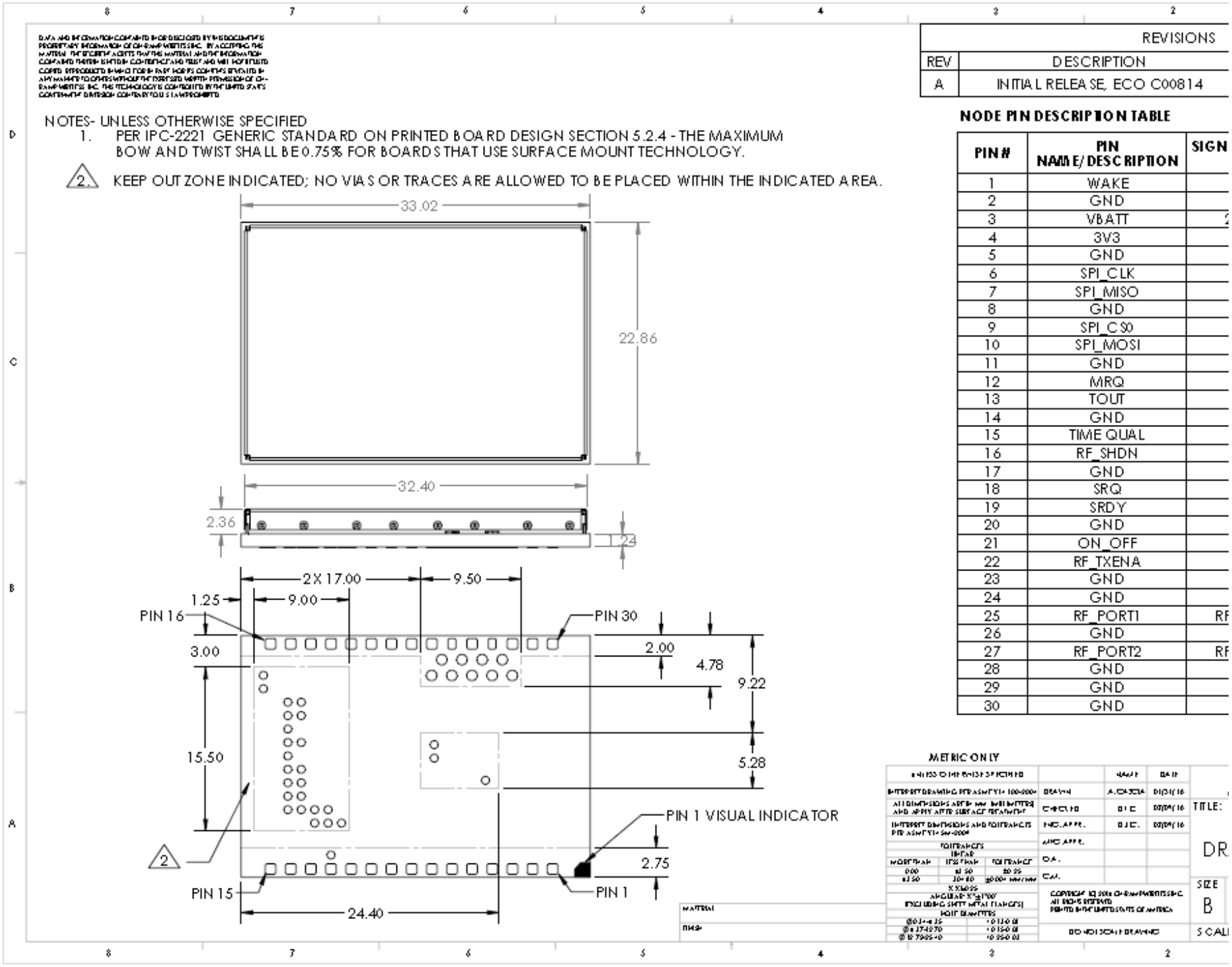


Figure 28. Lithium Battery Example

The mechanical drawing provides the dimensions of the nanoNode only and does not reflect the current labeling of the product.



NODE PIN DESCRIPTION TABLE

PIN #	PIN NAME/ DESCRIPTION	SIGN
1	WAKE	
2	GND	
3	VBATT	2
4	3V3	
5	GND	
6	SPI_CLK	
7	SPI_MISO	
8	GND	
9	SPI_CS0	
10	SPI_MOSI	
11	GND	
12	MRQ	
13	TOUT	
14	GND	
15	TIME QUAL	
16	RF_SHDN	
17	GND	
18	SRQ	
19	SRDY	
20	GND	
21	ON_OFF	
22	RF_TXENA	
23	GND	
24	GND	
25	RF_PORT1	RF
26	GND	
27	RF_PORT2	RF
28	GND	
29	GND	
30	GND	