dNode Integration Specification

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dNode Integration Specification

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Revision History

Revision	Release Date	Change Description
A	May 24, 2012	Initial release.
B	July 11, 2012	Updated the Maximum RF Conducted Power and clarified antenna configuration and defaults.

1 Overview

This document provides a brief overview of the Ultra-Link Processing™ (ULP) wireless network as well as guidelines allowing an integrator to design a Host product that utilizes the dNode and ensures that the system meets all of its technical objectives and requirements to enable remote wireless communication.

1.1 ULP Wireless Network

The On-Ramp Wireless ULP network is comprised of dNodes and Access Points (AP) and operates in the unlicensed 2.4 ISM band at a receive-sensitivity of -142 dBm. The dNode is designed to easily integrate, through standard interfaces, with sensors enabling robust wireless communication with one or more Access Points interfaced with a customer's local or wide area network.

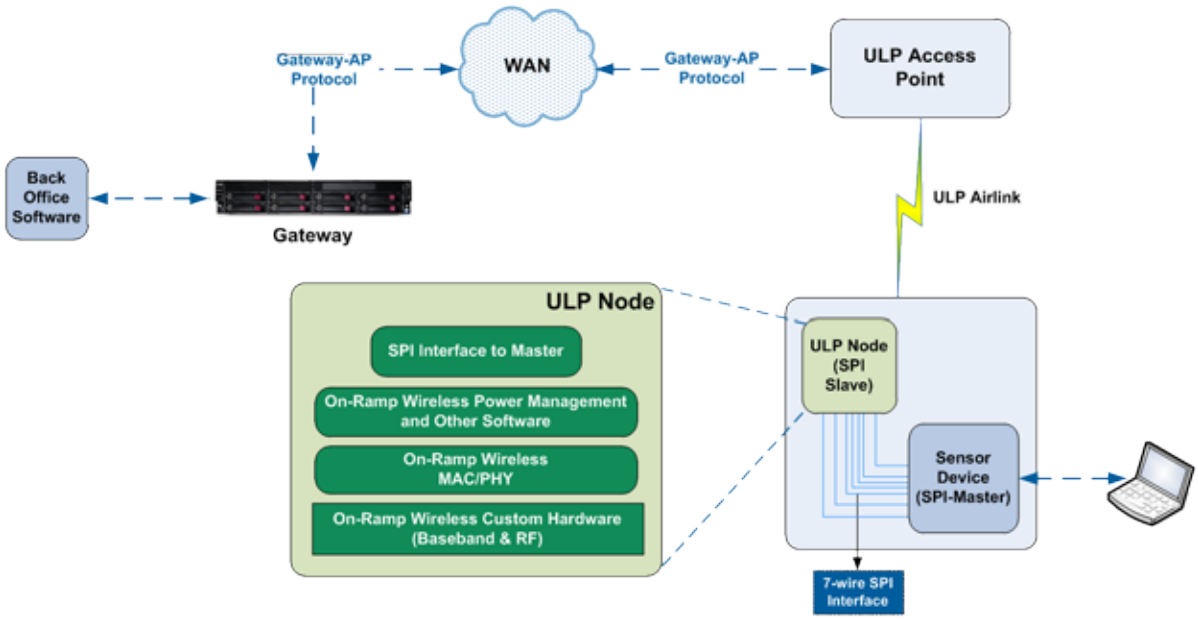


Figure 1. On-Ramp Wireless ULP Network

1.2 dNode

The ULP dNode is a third generation, small form factor wireless network module that easily integrates with various devices and sensors using an industry standard Serial Peripheral Interface (SPI). Most of the top side of the printed circuit board (PCB) is enclosed with a radio frequency (RF) shield except for the two RF connectors. The RF connectors are MMCX (Jack) receptacles. The PCB bottom side consists of two single-row, 0.1 in pitch (2.54mm) headers, J701 and J703.

Figure 2. dNode (Top and Bottom Views)

The following figure shows how a dNode interfaces with a Host application.

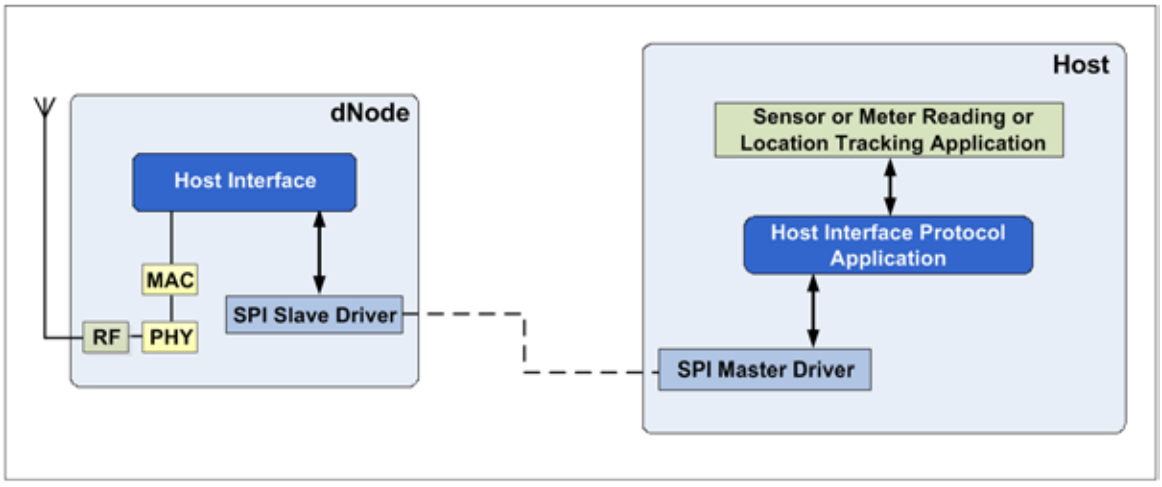


Figure 3. Typical Application Diagram

1.3 Referenced Documents

The following documents are referenced and provide more detail.

- **ULP Node Interface Library (UNIL) (010-0066-00)**
  Provides information about the library of portable C code provided by On-Ramp Wireless which can be integrated into a customer's existing software architecture.
- **UNIL API (010-0072-00)**
  Provides details relating to the UNIL Application Programming Interface.
- **ULP Node Host Message Specification (014-0020-00)**
  Provides details relating to Node Host messages.
- **Node FCC/IC/ETSI EMC Compliance Test Procedures (009-0021-00)**
  Describes and explains the FCC/IC/ETSI EMC compliance tests and how to use On-Ramp Wireless's configuration software for these tests.
- **NPT User Guide (010-0060-00)**
  Describes setup, configuration, and use of a collection of utilities called Node Provisioning Tools (NPT) used for Node provisioning.

2 DC and AC Characteristics

2.1 Absolute Maximum Ratings

Operating outside of these ranges may damage the unit.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-40	85	ºC
Operating Temperature	-40	85	ºC
Input Voltage	2.5	5.5	V

2.2 Recommended Operating Conditions

Table 2. Operating Conditions

Parameter	Min	Max	Unit
Input voltage, VBATT	2.5	5.5	V
Ambient Temperature, Ta	-40	85	ºC

The following characteristics apply across the -40°C to +85°C temperature range unless otherwise noted.

Table 3. Operating Characteristics

Description	Min	Typ	Max	Units
DC Characteristics				
Voltage – VBATT	2.5	3.6	5.5	Volt
Off Current – Note 1	0.05	0.1	2.0	µA
Deep Sleep Current - Note 1	10	20	40	µA
Idle Current – Note 1	10	15	25	mA
Receive Current – Note 1	75	85	90	mA
Transmit Current – Note 2	200	245	280	mA
Digital				
VOL – Voltage Output, Low (4mA sink)	0		0.1	V
VOH – Voltage Output High (4mA source)	2.4		3.2	V
Environmental				
Operating Temperature	-40		+85	°C
Storage Temp	-40		+85	°C
Humidity – non-condensing	5		95	%

Description	Min	Typ	Max	Units
Ramp Temperature (maximum rate at which operating temperature should change)			30	°C/Hr.
Receiver				
Receiver Sensitivity – Note 3	-130	-133	-135	dBm
Receiver Image Reject	38	45	50	dB
Noise Figure	3.5	5.0	6.7	dB
Input IP3 (high LNA gain mode)		-11		dBm
Maximum RF input level for specification compliance			-20	dBm
General RF Characteristics				
Frequency Range – Note 4	2402		~2482	MHz
Channel Spacing	N/A	1.99	N/A	MHz
Transmitter				
Maximum RF Conducted Power –Note 5 FCC/IC markets: ETSI markets:	 19.5 8.5	 20.4 9.5	 20.9 10.0	 dBm dBm
Carrier Rejection	-35	-40	-50	dBc
Signal Modulation		DSSS-DBPSK		
Signal Bandwidth		1.0		MHz
BT Factor		0.3		
Peak to Average Ratio		2.3		dB
Spectral bandwidth at maximum RF power: -6dB BW -20dB BW		 0.96 1.75		 MHz MHz
ACPR – Note 6			-30	dBc
Harmonics – Note 7			-43	dBm
Transmit Power Level Accuracy – Note 8			±1.5	dB
Transmitter Spurious Outputs – Note 9 30MHz to 2400MHz: 2482MHz to 8000MHz:			 < -43 < -43	 dBm dBm
VSWR Tolerance Maximum VSWR for spec compliance – Note 10: Maximum VSWR for stability.			 1.5:1 9:1	

NOTES:

1. Tested at 3.6V input.
2. Measured at 20.9 dBm TX output (Typ=50W), 3.6V, range includes VSWR ≤ 1.5:1 (Po not compensated).
3. Sensitivity at maximum spreading factor of 13 (8192) with 10% FER.
4. The upper frequency range is market dependent:
   a. FCC/IC: CH38; 2475.63 MHz.
   b. ETSI: CH40; 2479.61 MHz.

c. Japan: CH41; 2481.60 MHz.

5. Maximum TX RF power is limited by FCC/IC grant to 20.9 dBm in these markets.
6. Spec and test method comes from FCC 15.247(d); Band Edge Emissions, 2 MHz offset.
7. At any TX power level, VSWR ≤ 3:1. Harmonics fall into FCC restricted bands.
8. Estimated sum of all contributors with VSWR ≤ 1.5:1. Normal link mode.
9. At any TX power level, VSWR ≤ 3:1. Applies to spurious, not ACPR or harmonics. Generally the largest spurious output outside the 2.40-2.48GHz band is at 2/3LO and 4/3LO.
10. Maximum VSWR for spec compliance applies at 25°C only. Slightly degraded ACPR/mask and power variation can be expected at temperature extremes.

2.3 Effects of Temperature and Voltage

The dNode is based largely on Complementary Metal–Oxide–Semiconductor (CMOS) technology. The current drain of CMOS circuitry can vary substantially over Temperature. The RF circuitry and its performance also vary substantially over Temperature.

The dNode utilizes two main power domains when it is functioning:

1. **LDO Regulators that work from 2.5V up to 5.5V.**
   These are enabled when the POWER_ON signal for the dNode is active. These can act as a linear load as voltage increases from minimum to maximum – although these circuits do not normally consume much power.

2. **Switching power domains.**
   When the dNode wakes up to communicate with the Host or for networking events, its switching regulators are enabled. These buck-boost switching regulators supply the 3.3V and other logic supplies over the input range of 2.5-5.5V. The power efficiency of these regulators change dramatically over input voltage, load levels, and temperature. Nominally, the power efficiency is best at 3-4.0V. The efficiency becomes poor below 3.0V and is moderately efficient at the higher input levels.

The following graphs show the relative differences across the operating voltages and their effect on current consumption.

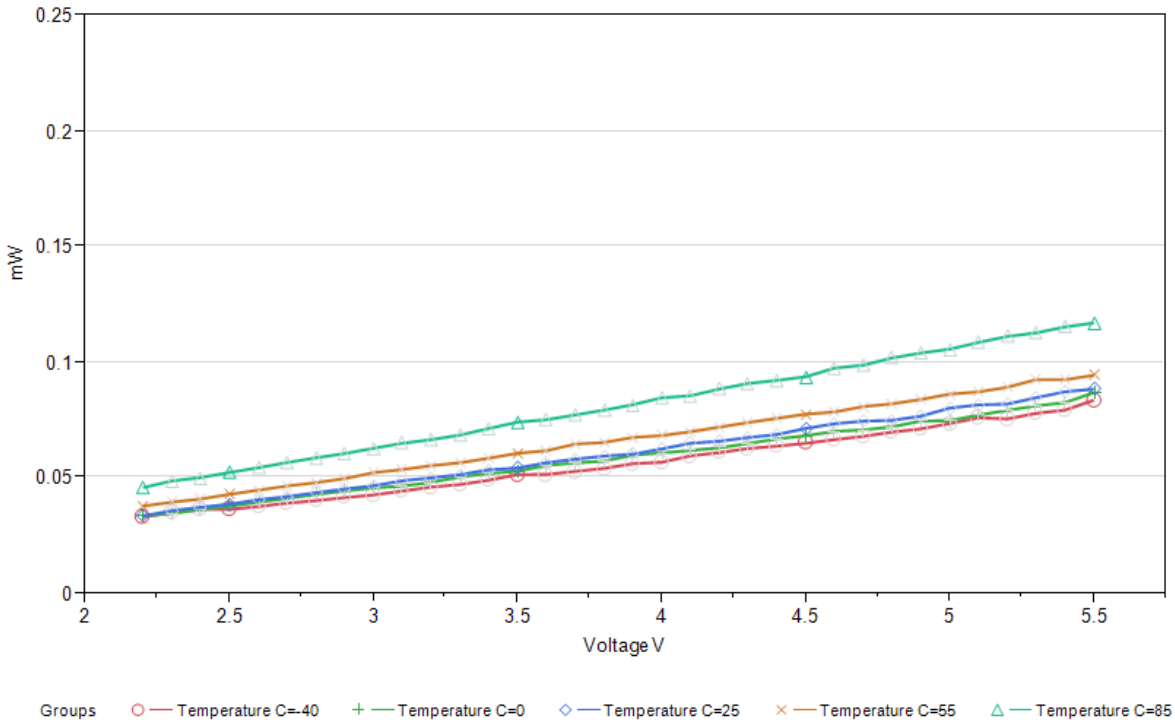


Figure 4. dNode Deep Sleep Power Consumption (mW Power vs Voltage Input)

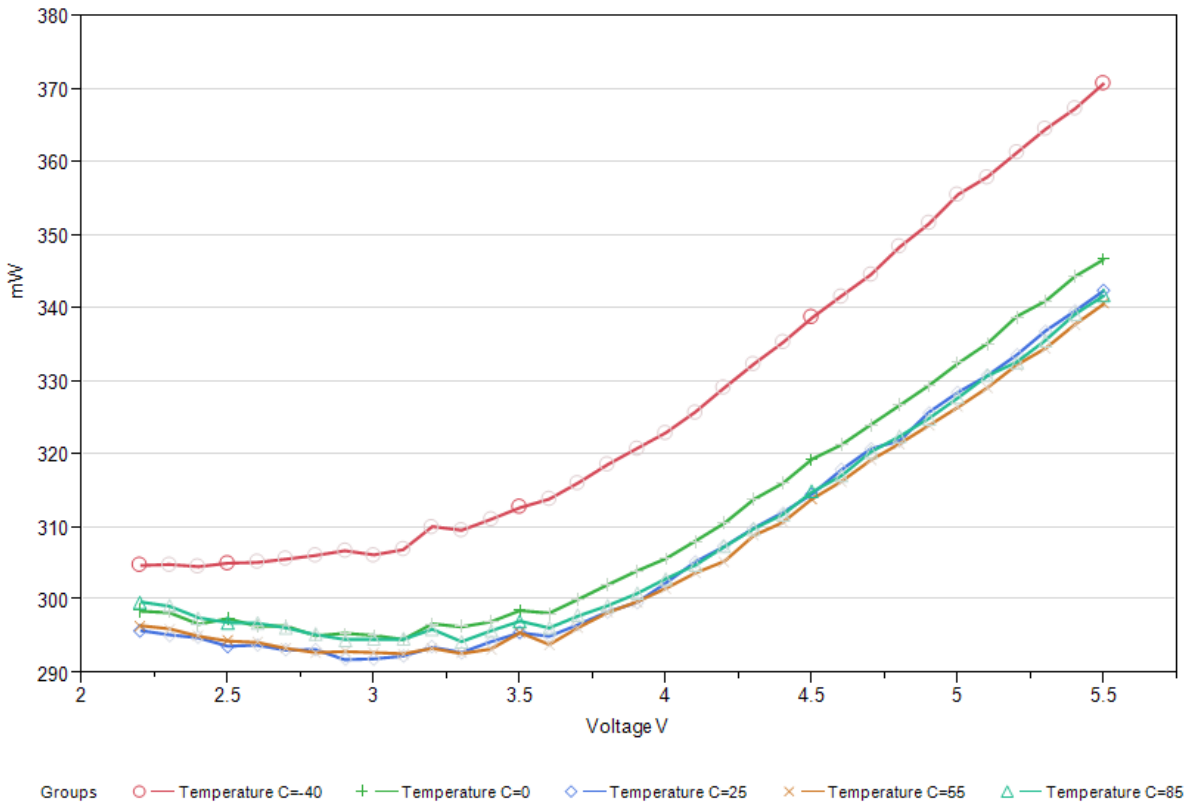


Figure 5. RX State Power Consumption (mW Power vs VBATT Input)

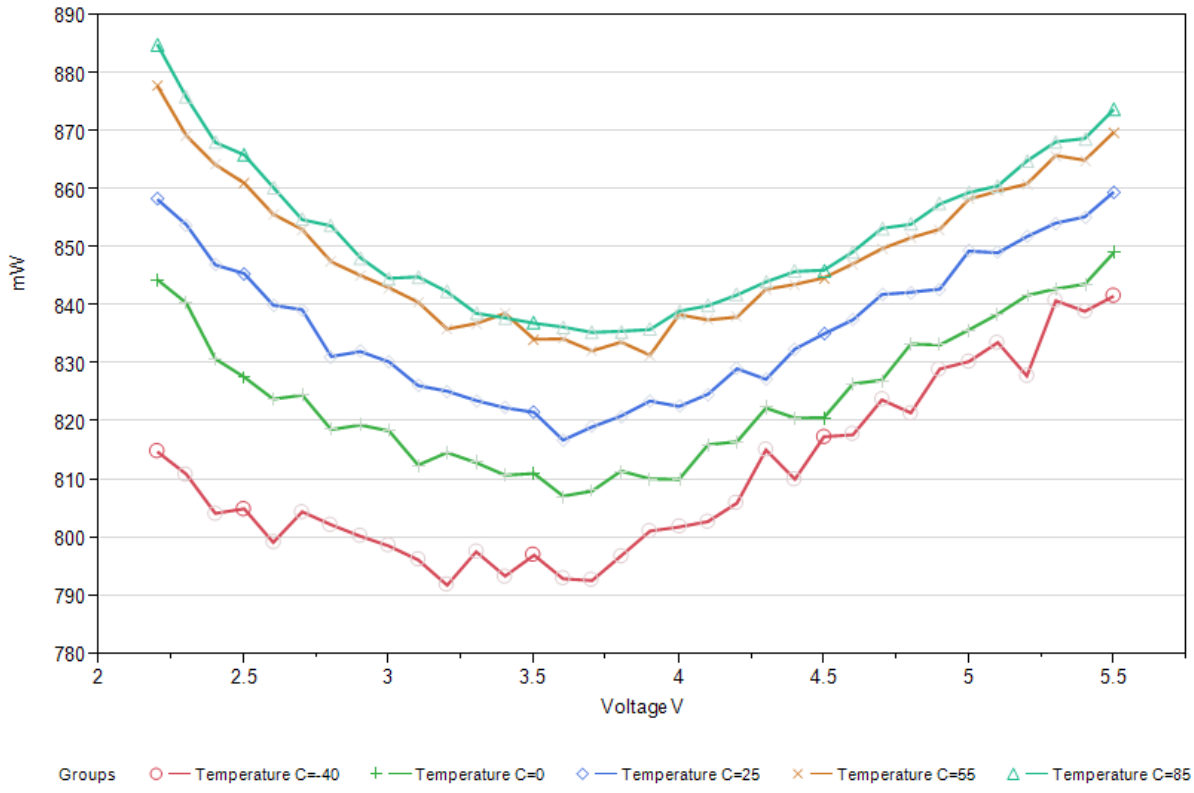


Figure 6. TX Power Consumption at 20.9 dBm (mW Power vs VBATT Input)

3 Electrical Interface

This chapter describes the electrical interface of the dNode and how the Host processor controls the dNode.

3.1 Signal Connectors

- The PCB bottom side consists of two single-row 0.1 inch pitch (2.54 mm) headers, J701 and J703. All user interfaces to the dNode, with the exception of RF, are through these two connectors.
- The header mating contacts are 0.228 inch (5.8 mm).
- J701, 1x10 SIP headers, 2.54 mm pitch, 5.8 mm long
- J703, 1x10 SIP headers, 2.54 mm pitch, 5.8mm long

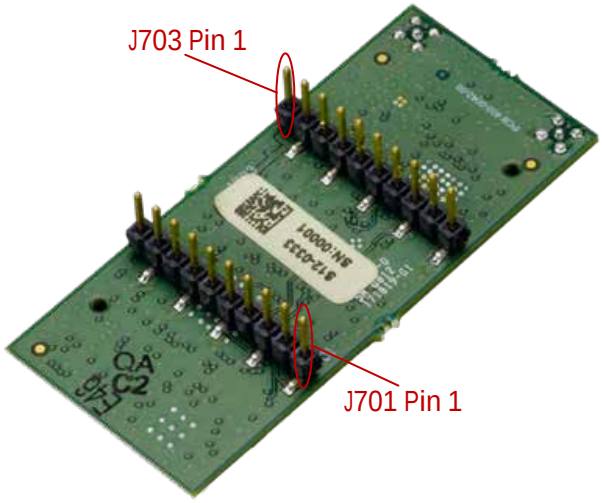


Figure 7. Bottom of the dNode Showing the J701 and J703 Pins on the Signal Connectors

3.2 Pin Descriptions

Table 4. dNode J701 Pin Descriptions

J701 Pin #	Pin Name	Signal Direction Relative to dNode	Signal Type	Polarity	Comment
1	Not Used		Not Used		DO NOT CONNECT
2	Not Used		Not Used		DO NOT CONNECT

J701 Pin #	Pin Name	Signal Direction Relative to dNode	Signal Type	Polarity	Comment
3	T_OUT	Output	CMOS_O	Active High	Time Sync Pulse
4	RESET	Input	CMOS_I	Active Low	dNode Reset
5	SPI_CS	Input	CMOS_I	Active Low	SPI Chip Select
6	SPI_SCLK	Input	CMOS_I		Serial Clock
7	SPI_MOSI	Input	CMOS_I	Active High	Master Out Slave In
8	SPI_MISO	Output	CMOS_O	Active High	Master In Slave Out
9	GND	Ground	Power		
10	GND	Ground	Power		

Table 5. dNode J703 Pin Descriptions

J703 Pin #	Pin Name	Signal Direction Relative to dNode	Signal Type	Polarity	Comment
1	VBATT	Power	Power		
2	VBATT	Power	Power		
3	RXD1		Reserved		DO NOT CONNECT
4	TXD1		Reserved		DO NOT CONNECT
5	GND	Ground	Power		
6	SPI_MRQ	Input	CMOS_I	Active High	Master Request
7	SPI_SRQ	Output	CMOS_O	Active High	Slave Request
8	SPI_SRDY	Output	CMOS_O	Active High	Slave Ready
9	GND	Ground	Power		
10	GND	Ground	Power		

Table 6. dNode Antenna Pin Descriptions

Pin Name	Signal Direction Relative to dNode	Signal Type
Antenna 1	Input/Output – Default*	50 Ohm RF
Antenna 2	Input/Output	50 Ohm RF

* The antennas for the dNode can be configured as a single antenna device or a diversity antenna device (both antennas). When the dNode configuration is set to single antenna, Antenna 1 is the default. This antenna configuration is set by the NPT. For further details, see the *NPT User Guide (010-0060-00).*

3.3 Signal Descriptions

3.3.1 VBATT

This is the main power to the dNode. This needs a low impedance source to the Host's power source. It is recommended that the Host have provision for up to a 100 µF low ESR capacitor. It is likely this capacitor is not required if low impedance design rules are followed.

3.3.2 RESET_N

The RESET_N pin serves a dual purpose. In an effort to ensure a pin for pin compatibility to On-Ramp Wireless' eNode, the Reset pin serves a dual electrical purpose: Reset and Power On.

- When the RESET_N pin is asserted Low, the Power to the dNode is turned off. The resultant current is nominally under 1µA. This is a valid and supported state. The eNode did not have this function, but the microNode does support a Power Off function that is split over two pins (POWER_ON and RESET_N). During the Reset of the dNode, all other signals to the dNode are either low or floating, providing no electrical energy to the powered off device.
- When the dNode is released from Reset, it wakes up and its regulators turn on. After the dNode has been successfully awakened, it asserts its SRDY to indicate that it is ready for communication.

3.3.3 MRQ

The MRQ (Master Request) is the Host's normal way of waking the dNode to initiate SPI communications. Logic "High" forces the dNode awake.

3.3.4 SRDY

SRDY (Slave Ready) is an indication from the dNode that it has fully booted its internal Firmware image, initialized its Hardware and Interfaces, and is ready for communication (arbitration) with the Host. Logic "High" indicates the dNode is ready for communications.

3.3.5 SRQ

The SRQ (Slave Request) signal is an indication from the dNode that it wants the Host's attention. When SRQ is asserted "High," the Host must read the Status registers of dNode. If SRQ is "High," SRDY will also be "High."

3.3.6 USTATUS

USTATUS is currently undefined. In software it can be either an Input or Output. Currently it is configured as an input. The Host should not use this signal.

3.3.7 SPI System

The SPI system is the generic term used for all SPI signals (MOSI, MISO, CS, SCLK) to be set up for SPI communications to occur between Host and dNode.

The dNode SPI is the Slave in the Master/Slave communications and is defined in section 4.2: SPI Mode and Timing.

3.3.8 RF

The dNode supports two MMCX ports. These two ports are required for antenna diversity. Each port is a nominal 50 Ohms. For best results, ensure that the load termination (antenna) has a VSWR of 1.5:1 or better (return loss < -14 dB).

3.4 Environmental

3.4.1 ESD

The dNode is designed to be a truly embedded module and can almost be considered an IC. The dNode is to be placed as a direct-connect to the Host CPU. Therefore, the dNode has inherent minimal electrostatic discharge (ESD) protection on its I/O.

Table 7. ESD Information

ESD Model	Class and Minimum Voltage
HBM	Class 1C (>1000V)
MM	Class A (>100V)

The RF port does have some protection in the form of an inductor to ground, thus allowing some robustness to direct ESD strikes.

If the application is intended for harsh ESD or lightning strike scenarios it is recommended that the Integrator take extra precautions to guard against accidental resets or ESD damage.

3.4.2 Harsh Environments

The dNode employs two 10-pin SIP connectors for mount onto the host. A robust socket, such as a machined pin, can be used for the dNode. This initially adds cost but eases potential replacement costs for large scale provisioning. For truly robust applications, it is recommended that the dNode be soldered to the Host platform. If the target design is intended for high humidity or salt environments and long service life, it is recommended that the designer take necessary precautions to guard against prolonged exposure to moisture and other contaminants. A sealed enclosure (IP68) or potting may be required in extreme environments.

4 SPI Interface and Sequences

4.1 SPI System Interface Overview

The SPI slave interface is currently the only supported interface for Host-to-Node communication.

NOTE: The dNode must be the only SPI slave on the bus.

The SPI slave interface provides communication with an external Host through a 7-wire interface. The Host is the SPI master and the dNode is the SPI slave. In addition to the four standard SPI signals, three additional signals are used to complement the SPI bus: MRQ, SRQ, and SRDY. The additional signals are included to support dNode state transitions and bi-directional message traffic.

The SPI signals include four that are controlled by the master and three that are controlled by the slave.

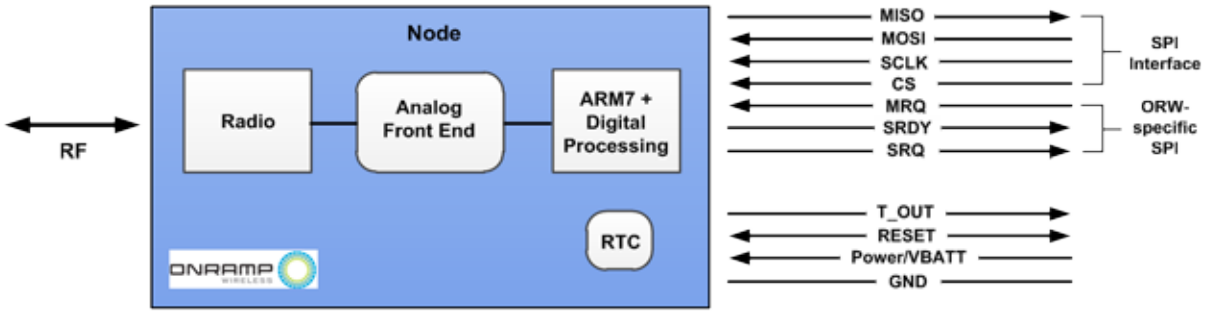
Master-controlled Signals

- MOSI
- SCLK
- CS
- MRQ

Slave-controlled Signals

- MISO
- SRQ
- SRDY

When MRQ and SRQ are low, the remaining master controlled signals (MOSI, SCLK, and CS) must be tri-stated. This is to prevent these signals from back-driving the dNode slave that may be in deep sleep. When either MRQ or SRQ assert high, the master should set each of the three signals appropriately according to their standard usage. See the following sections for timing details. No pull-up resistors should ever be applied to any signals on the dNode.



4.2 SPI Mode and Timing

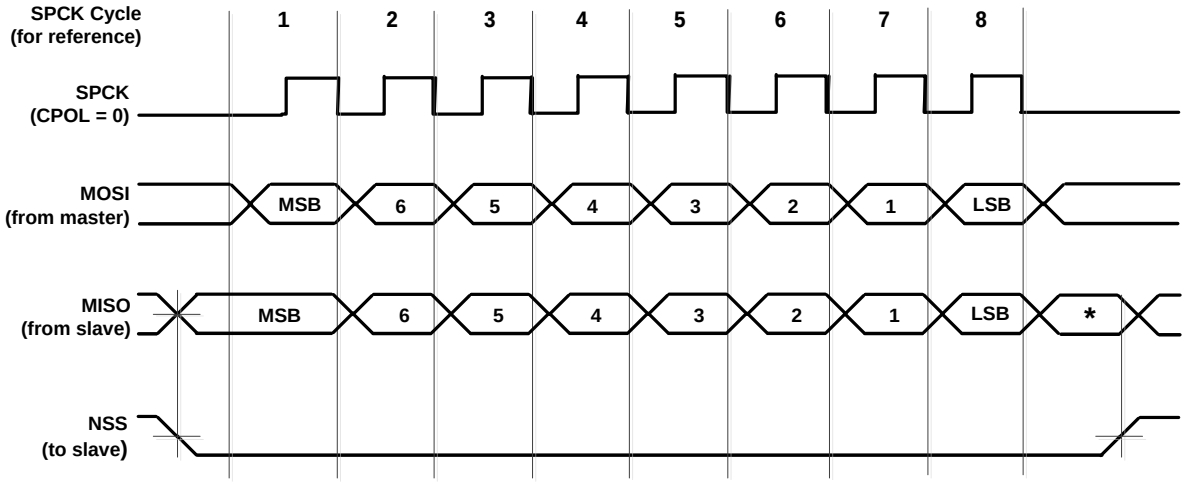


Figure 8. SPI Timing, CPOL = 0, CPHA = 0

4.3 Startup (Power On) Sequence

During, and immediately after Power On Reset (POR), the Host has no control of its I/O power states. For instance, some CPUs have GPIO that tri-state or act as inputs during power up. Other CPU brands have programmable pull-ups on its I/O and need the Host CPU to disable those pull-ups for the Host's GPIO to work correctly with the dNode. This setup and configuration of GPIO takes a finite time during the Host boot process. This is detailed in the following figure.

Whereas the power-on sequence is described here, it is recommended that the Integrator not attempt this entire startup sequence without assistance. On-Ramp Wireless offers a formal and controlled library to help with this startup and communication interface called UNIL. This is fully documented and released by On-Ramp Wireless. The UNIL tracks all details of the lower (physical) and higher (messages) layers of the Host-Node communications. For more information on UNIL see the documents referenced in chapter 1 at the beginning of this document.

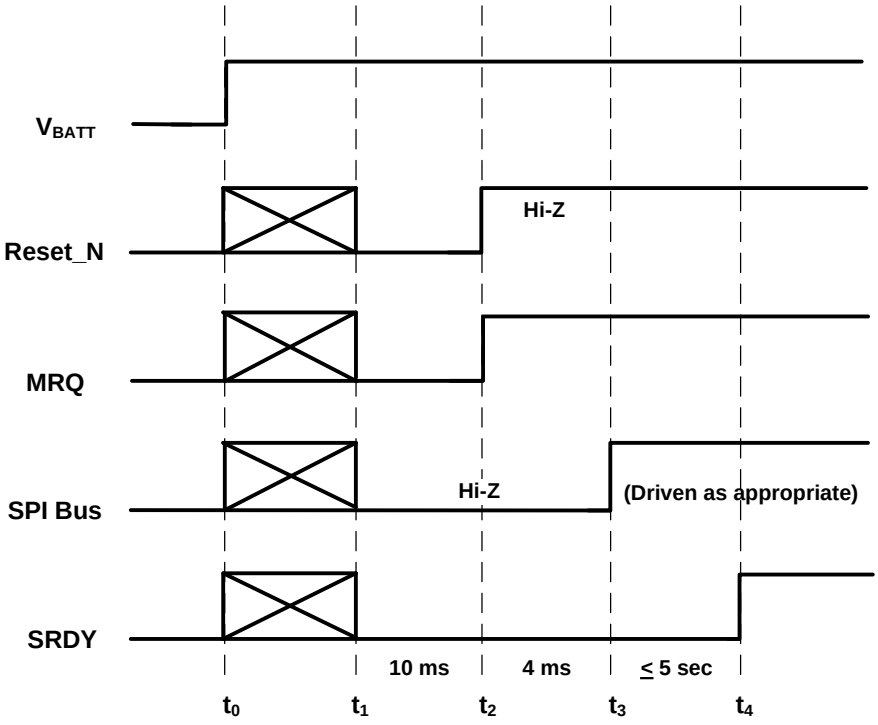


Figure 9. dNode Host-driven Initial Power-up Sequence

The timing sequence shown in the figure above is described below. **NOTE:** The timing shown in the figure is not to scale.

- **t0** This transition shows the power-up and possible random states of Host I/O, before the Host is able to properly configure its pins. It is strongly recommended that the selected Host CPU be a type that tri-states its pins upon power-up.
- **t1** When the Host gains control of its I/O, Reset_N should be driven low, MRQ driven low, the SPI lines tri-stated, and SRDY from the node is expected to be low. This reset state should be held for 10 ms.
- **t2** After 10 ms, Reset_N should be released to float and MRQ is driven high.
- **t3** The SPI bus should be enabled 4 ms after Reset_N is released.
- **t4** SRDY going high shows the Node is fully awake and initialized. This state facilitates Host-Node arbitration sequence and communications. t3 – t4 may take several seconds over temperature and voltage extremes. Timeout should be 5 seconds or more.

4.4 Wake Sequence

The dNode can be awakened in two manners:

- MRQ assertion from the Host. The Host desires communications with the dNode and awakens the dNode by asserting the MRQ line. This is a Synchronous Wake Sequence.

- The dNode can “self-awaken” due to network events. In this case, a timer internal to the dNode “pops” and triggers the dNode to “Wake.” When the dNode is awake it asserts its SRDY as a matter of course to indicate to the Host (if it needs to) that it can start communicating with the dNode while it is awake. This is an Asynchronous Wake Sequence.

4.4.1 Wake Sequence (Synchronous)

The following sequence demonstrates the timing required of the Host to awaken the dNode from a sleep state.

Assumptions:

- The dNode has been previously Powered On and Arbitrated.
- The power (VBATT) has remained stable and the dNode has not been Reset (Reset is set to tri-state/float).

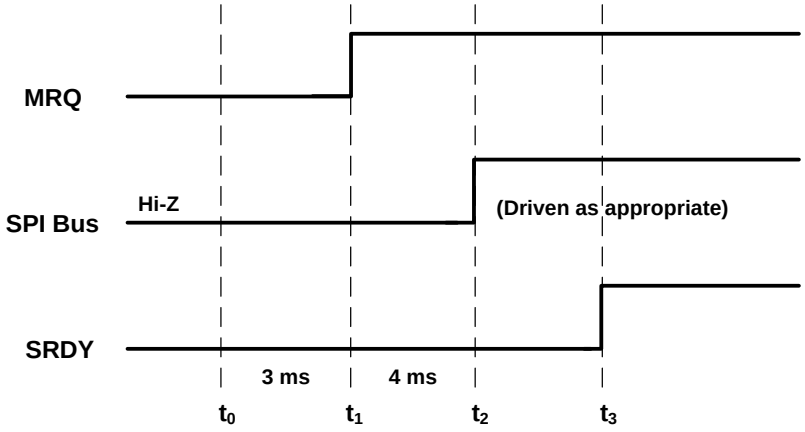


Figure 10. Host-Initiated dNode Wake Sequence – SRDY Low (Synchronous)

The timing sequence shown in the figure above is described below. **NOTE:** The timing shown in the figure is not to scale.

- **t0** The Host decides to communicate with the dNode, checks SRDY, and determines it is low.
- **t0 à t1** The Host ensures that SRDY has been low for at least 3 ms, then at t1, raises MRQ.
- **t1 à t2** Asserting MRQ begins internal dNode supply sequencing. The SPI bus must remain disabled (tri-stated) for 4 ms after MRQ rises, at which point the SPI bus may be enabled.
- **t2 à t3** After the initial assertion of MRQ, the dNode has to internally power up and initialize its systems. When it is ready to communicate it will assert its SRDY line to signal it is now ready for SPI interaction. From MRQ assertion until the dNode is ready,which takes about 80 ms.
- **t3** The dNode is now ready to communicate with the Host.

4.4.2 Wake Sequence (Asynchronous)

In this scenario, the dNode is already awake due to a networking event (SRDY is already High) and the Host wants to communicate with the dNode while it is awake. The Host asserts MRQ to ensure that the dNode stays awake during its communication cycle.

NOTE: The timing shown in the figure is not to scale.

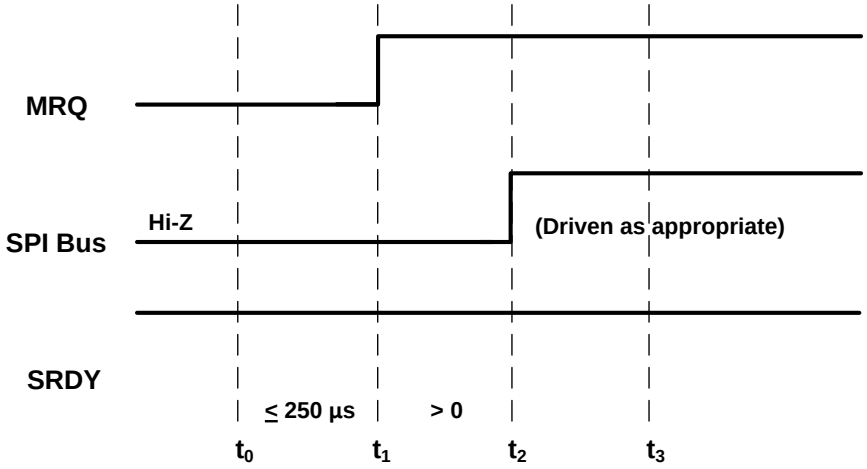


Figure 11. Host-Initiated dNode Wake Sequence – SRDY High (Asynchronous)

The timing sequence shown in the figure above is described below. **NOTE:** The timing shown in the figure is not to scale.

- **t0** The Host decides to communicate with the dNode, checks SRDY, and determines it is high.
- **t0 à t1** The Host must assert MRQ within 250 microseconds to avoid race conditions on SRDY falling just after the host checks its state.
- **t1 à t2** The SPI bus must be tri-stated until after MRQ is asserted. However, the SPI bus can be enabled immediately after MRQ is asserted and messaging can begin immediately thereafter.

4.5 Host-Driven Reset Sequence

If the dNode fails to communicate (or similar), it may be necessary to Reset the dNode. The following figure shows the proper sequence to reset the device.

NOTE: Resetting the device causes it to go through a Cold Acquisition process to reacquire the network.

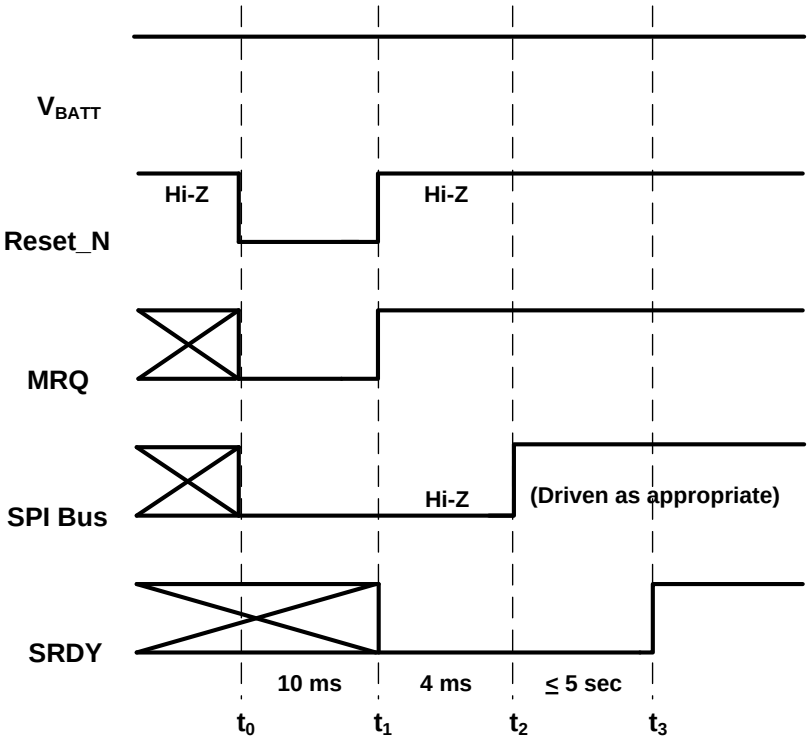


Figure 12. Host-Driven Reset Sequence

The timing sequence shown in the figure above is described below. **NOTE:** The timing shown in the figure is not to scale.

- **t0** The host decides to reset the dNode. The SPI Bus is tristated, the MRQ is driven low, and then Reset_N is driven low.
- **t1** Reset_N is held low for 10 ms and then released back to floating.
- **t2** The SPI bus should be enabled 4 ms after Reset_N is released.
- **t3** SRDY going high shows the Node is fully awake and initialized. This state facilitates Host-Node arbitration sequence and communications. t3 – t4 may take several seconds over temperature and voltage extremes. Timeout should be 5 seconds or more.

4.6 Host MRQ Release/dNode Allowed to Sleep Sequence

If the Host determines there are no more messages or SPI transactions required, it should disable the interface to allow the dNode to fall back to Deep Sleep (lowest power mode). As the figure below indicates, the SPI bus must be disabled (tri-stated) before MRQ is de-asserted. These operations can be performed back to back.

NOTE: The timing shown in the figure is not to scale.

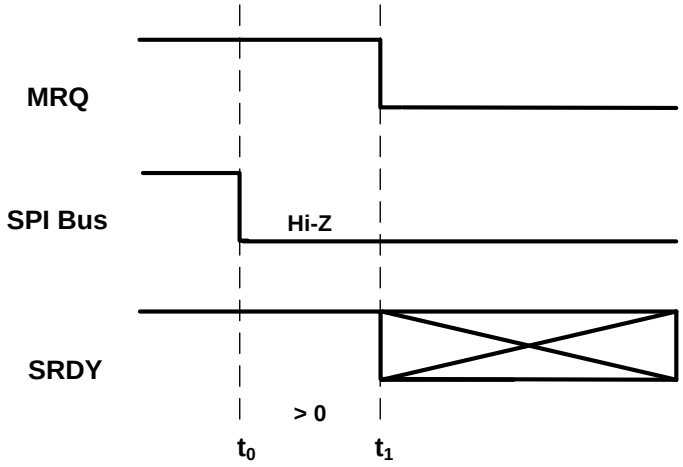


Figure 13. Host MRQ Release/dNode Allowed to Sleep Sequence

5 Power States

The dNode has a number of states it runs through during its various operating modes.

General comments:

1. The dNode accepts a wide input voltage range (2.5-5.5V).
2. The dNode has low drop out (LDO) regulators that will operate 100% of the time the dNode is powered (RESET_N signal set high or left floating by the Host).
3. There are 3.3V/1.2V Buck/Boost Switching regulators that use the wide input range to drive key RF and Digital circuits. The 3.3V regulator is only turned on in certain active operating states of the dNode.

The dNode tries to minimize its power consumption but is largely driven by network operating states and ULP modes of operation. This document does not describe all of the modes in detail but, in general, there are two main operating modes for the dNode:

- **Continuous Mode**
  In this mode, the dNode is ON (awake) at least 50% of the time (100% of its RX cycle). The dNode starts up, searches for the network, locks on, and Joins. In this mode, the dNode nominally is either in RX or TX modes (radio is ON and in a high power consumption state), or in an Idle state where the clocks and CPU are ON but the radio is OFF (moderately low power mode). The continuous mode is usually for applications where the Host and dNode are AC-powered and system current consumption is not an issue.
- **Slotted Mode**
  This mode has the dNode falling into a Deep Sleep state – the lowest power state of the dNode. In this mode, the dNode is mostly powered down – except for a couple of low power LDO Regulators. The dNode can sleep for hours at a time if the network is configured to allow this.

The power states are described in the following sections.

5.1 Operating States

This section describes the various operating states within the operational modes.

5.1.1 Power Off State

When the dNode is totally non-functional, the Host can set the RESET_N signal Low to deactivate the circuitry of the dNode. This should NOT be confused with Deep Sleep states where the dNode mostly sleeps yet maintains key network timers to wake up synchronously with network activity. If awakened from the Power Off/Reset state, the dNode must go through a very power-hungry search/acquisition algorithm to re-acquire the ULP network.

5.1.2 Deep Sleep State

The dNode shuts off all its power regulators except a couple low quiescent LDO regulators. These regulators keep a minimal amount of circuitry alive for tracking network timers, enable a 32 kHz clock, and some minor interface circuitry.

5.1.3 Oscillator Calibration State

When the dNode is in Deep Sleep state, it attempts to maintain accuracy of its low power 32 kHz clock to enable faster network synchronizing when it wakes up. The CPU of the dNode is not activated during this calibration state. The dNode will periodically, and briefly, Wake in a very low power mode to calibrate its 32 kHz clock to its very accurate 26 MHz clock. This is especially important when the temperature varies substantially causing the 32 kHz oscillator to drift. This is illustrated in the following figure.

This plot is an example of the dNode performing a self-calibration of its 32 kHz oscillator. The pulses represent the TCXO being turned on periodically to perform the calibration. The dNode Wakes itself from Deep Sleep, Calibrates, and then falls back to sleep. Minimal power is consumed during this self-calibration process. As can be seen, the dNode does this approximately every 900 seconds.

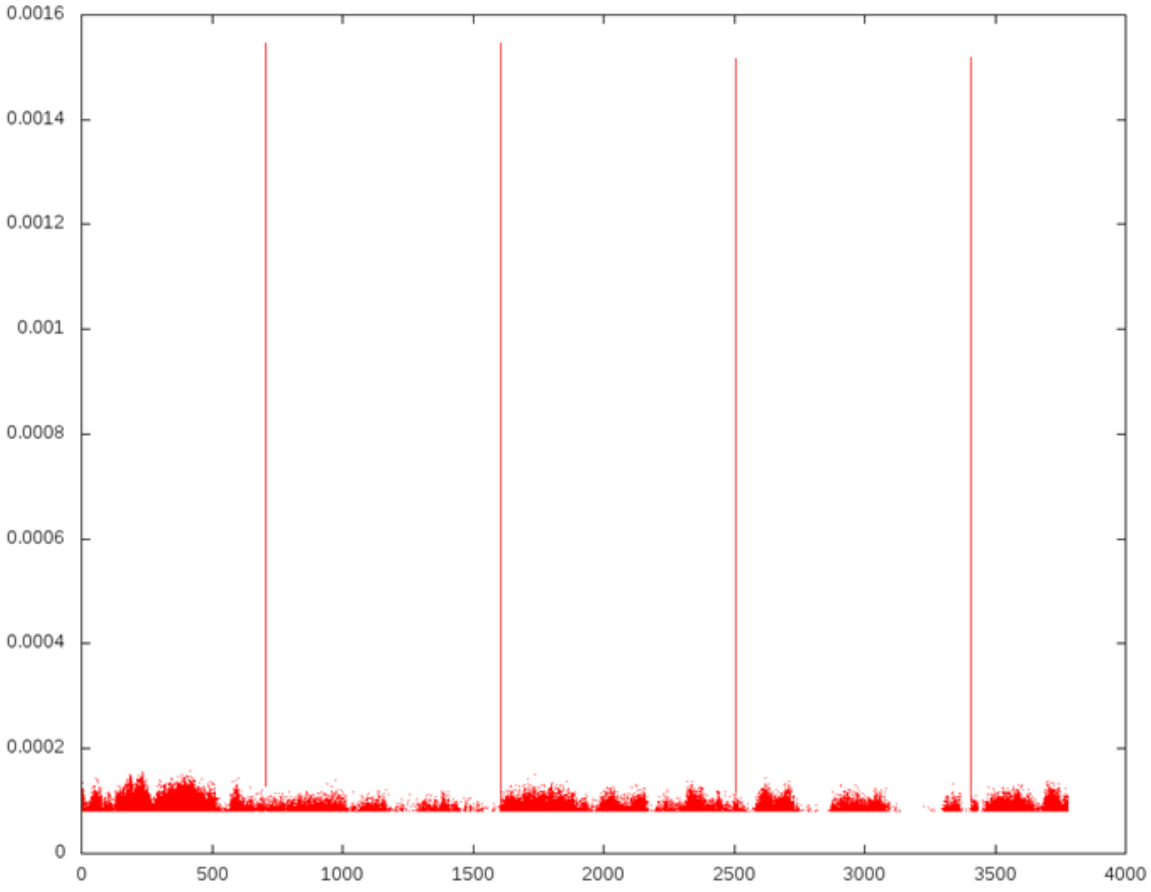


Figure 14. dNode Oscillator Calibration: Current (Amps) vs Time (Seconds)

5.1.4 Idle State

Idle state has various sub-states but generally refers to a state where the dNode is “awake” and its system clock is on, the CPU is awake, but the RF is OFF.

5.1.5 RX State

The dNode turns on all its clocks, the main CPU and the RF in an RX-only state. The RF transceiver, in RX state, consumes a moderate amount of power.

5.1.6 TX State

When the dNode transmits, it uses a variable transmit power that is correlated to its received RSSI. In this state, the dNode is likely at its highest power states, but this is somewhat dependent on RSSI. The worst case state (maximum power) is shown in Figure 15. This is at approximately 20.9 dBm output power. This is the dNode’s highest power state.

5.2 System

As noted, the dNode can go through various states of Deep Sleep, Idle, RX, and TX. The plot shown in the following figure provides a representative dNode waking up and going through these states and transitions.

All ULPs are different and current consumption is affected by many factors.

- Network coverage. How much TX power does a dNode need to transmit its data?
- Temperature range
- Operating Voltage
- Continuous mode vs Slotted mode: What is the Uplink Interval?
- Amount of data in the data model
- Quality of Service (QoS) for data delivery

All of the factors indicated above must be examined carefully and plotted to understand the end result in current profiles and expected battery life projections.

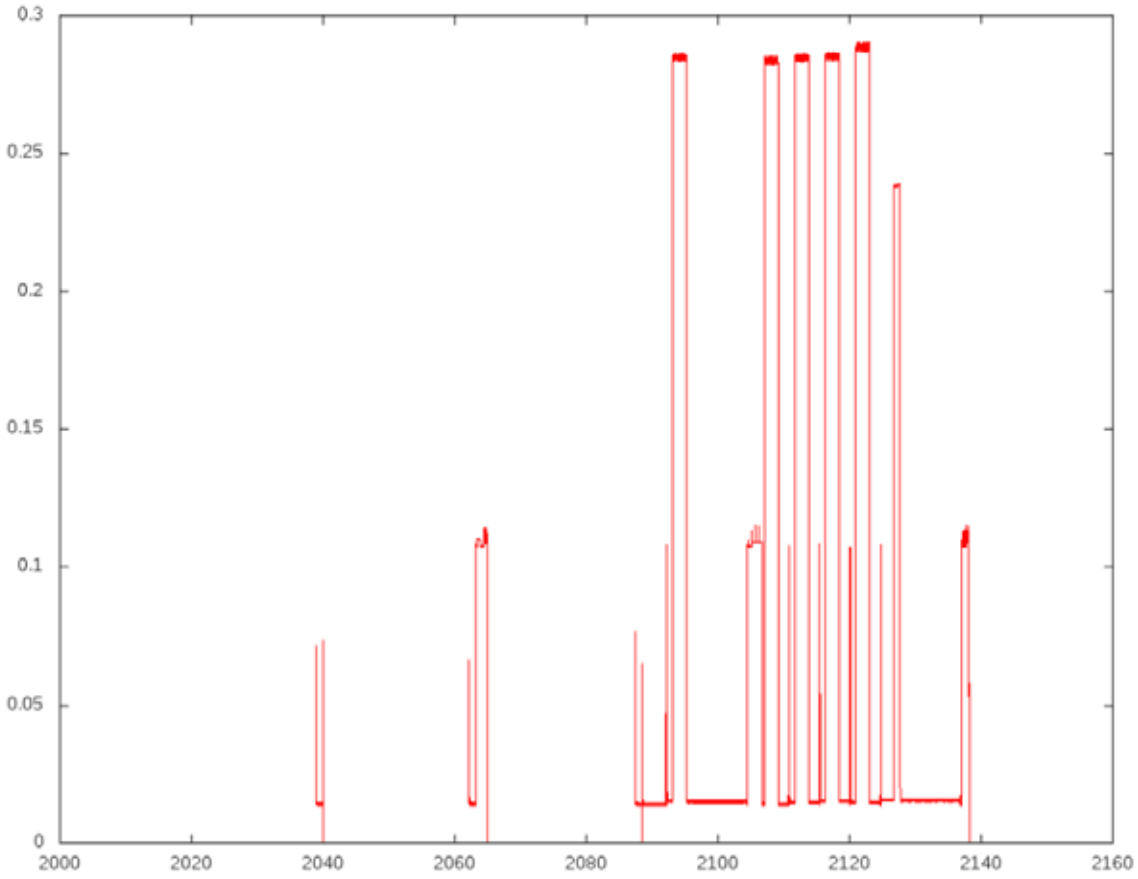


Figure 15. Representative Current Consumption During Deep Sleep, Idle, RX, and TX; x16 Spreading Factor (Amps vs Seconds)

The plot shown in the figure above represents the nominal transitions for the dNode from Deep Sleep, Idle, Receive, and Transmit states. In this case, a TX spreading factor of 16 is used. It is important that the Host designer understand the System operating profile, operating voltages, different operating modes of the dNode and the ultimate effect on System power consumption. Of course, this is especially true if a battery powered device is being considered.

6 Messaging Protocol

The details of Host/Node messaging are typically not necessary for integrators to implement, given the functional interface provided by the *ULP Node Interface Library (UNIL) (010-0066-00)* and *UNIL API (010-0072-00)*. However, low-level understanding of the SPI protocol used may be critical in resolving Host interface issues.

For mid-level details of the messages that may be sent over this interface, refer to *ULP Node Host Message Specification (014-0020-00)*.

6.1 Arbitration

Arbitration is the process a Host uses to signal to the Node that it supports the On-Ramp Wireless bi-directional messaging protocol. The arbitration sequence is designed to reduce the probability that an arbitrary non-Host transfer sequence can mirror a valid arbitration sequence.

Arbitration consists of both Host and Node transmitting an arbitration request/reply pair. After a defined turn-around delay, both transmit a validation request/reply. The turn-around delay avoids race conditions between Host and Node and provides enough time to allow ISR execution to complete before the next SPI transfer.

If the Node does not reply to the Host request, the Host needs to wait for a turn-around delay and retry the arbitration request.

The Host must perform the arbitration sequence before any other SPI Bus communication can take place between the Host and the Node.

The Host must initiate this arbitration sequence on boot up. Additionally, the Host must perform the arbitration sequence when the Node sends to the Host an arbitration message. This can occur due to the Node going into Deep Sleep and then waking up. Since the Node requires the arbitration sequence after waking from Deep Sleep and since the Host is not aware of when the Node goes to Deep Sleep, the Host must be able to detect that the Node is requesting arbitration and the Host must then reset its Host interface state machine and perform arbitration. For more information on the Host interface SPI bus state machine, refer to section 6.3: Host Interface SPI Bus State Machine.

6.2 Message Protocol

Host-to-Node transfers use master message command pairs and Node-to-Host transfers use slave message command pairs. Both transfers use identical command sequences with only the encoding of the commands differing. The command sequence for a message transfer consists of a request/acknowledgement pair followed by a defined turn-around delay and then a message composed of a header pair and a payload.

Variable length payloads are supported by encoding the payload size in the second half of the message request. The second half of the message reply contains the available receive buffer

size. If the message payload size exceeds the receive buffer size, then a new request must be made after a turn-around delay with a payload size that does not exceed the receive buffer size.

After a successful message request transfer, the Host waits a turn-around delay and then initiates the transfer with a message header command. The payload immediately follows the header and, if necessary, is zero padded to match the payload size indicated in the message request.

After the payload, the Host waits a turn-around delay before proceeding with any other further messages.

The Host interface SPI bus is a standard SPI bus (with MISO, MOSI, CS, and SCLK) with the addition of three lines (MRQ, SRQ, and SRDY). These three additional lines are used to provide the Host with the ability to wake up the Node over the SPI Bus as well as providing the Node with the ability to prompt the Host to begin a SPI Bus transaction. The Node is also exceptional in that it must be the only slave present on the SPI Bus, since MOSI, CS, and SCLK must be undriven (tri-stated) any time that MRQ is low.

Before any message is communicated over the SPI Bus, the MRQ and SRDY lines must be high. The Host guarantees this by pulling the MRQ line high and waiting for the Node to pull the SRDY line high. The Host cannot proceed with SPI Bus communication until both of these lines are high. Once MRQ and SRDY are high, the Host, being SPI Bus master, can continue with a normal SPI Bus transaction.

When the Node wishes to communicate with the Host, it pulls the SRQ line high. The Host must have the ability to detect this and start a SPI Bus transaction (by first pulling the MRQ high and waiting for SRDY to go high). A standard SPI Bus transaction is described and illustrated in Figure 18.

Message exchanges between Host and Node are shown below in Figure 16.

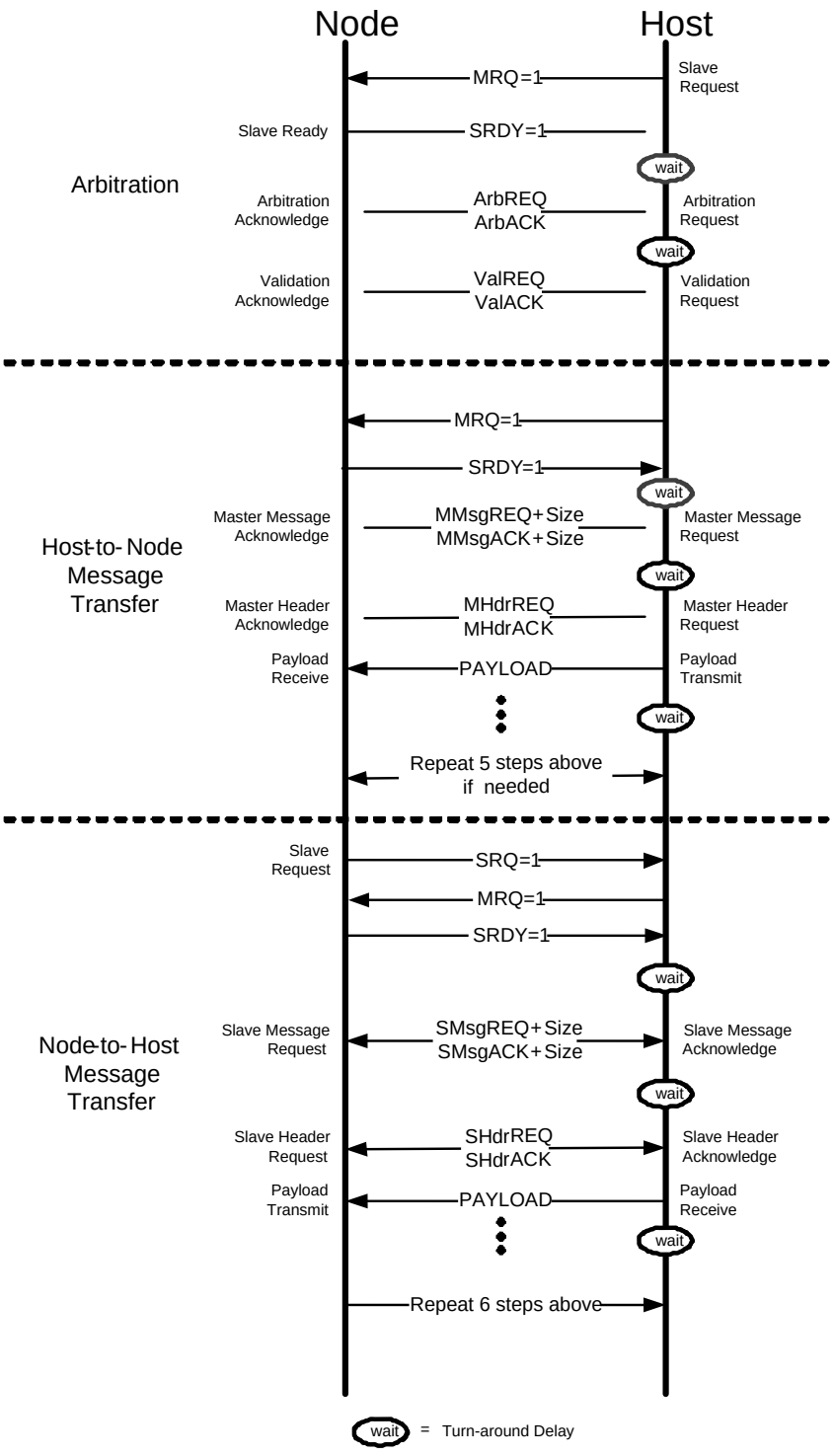


Figure 16. SPI Master and Slave Message Sequences

In each of the request/acknowledge command pairs shown, the top command is transmitted by the Host (master) and the bottom command is transmitted by the Node (slave). The wait

bubbles indicate a predefined turn-around delay which provides ISR processing time and avoids race conditions between Host and Node.

6.3 Host Interface SPI Bus State Machine

This section illustrates the sequence of messages that can take place on the Host interface SPI bus. The design and implementation of the actual state machine on the Host software is up to the Host software designer. This diagram is provided to demonstrate the message sequence over the SPI Bus. Note the usage of the turn-around delay, which is required in between each step of message exchange. This delay is required by the Node and is currently defined as having a time of 200 µs.

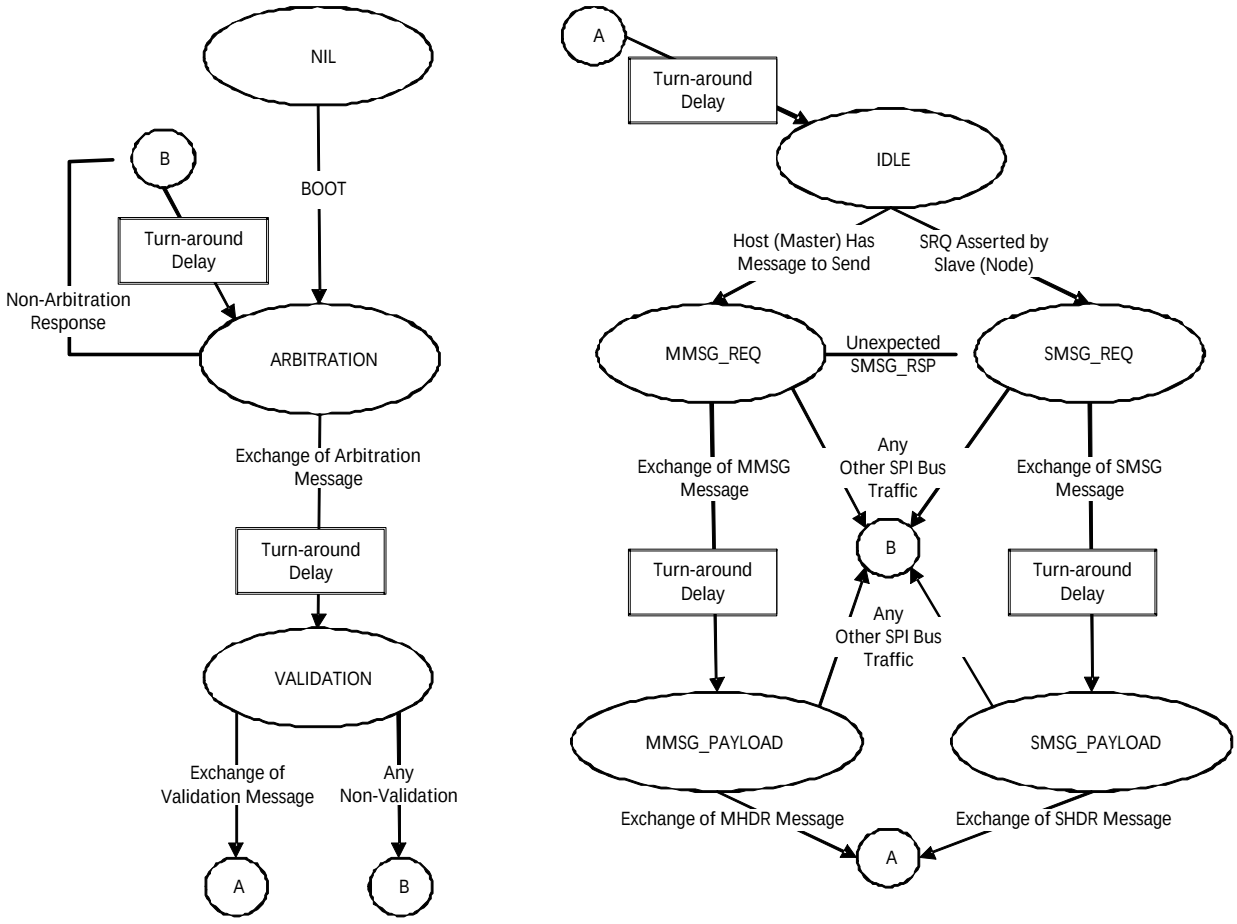


Figure 17. Host Interface SPI Bus State Machine

6.4 SPI Bus Timing Example

This section provides an example illustration of an exchange of messages first from master (Host) to slave (Node) and then from slave (Node) to master (Host). Each step in the timing sequence is described below:

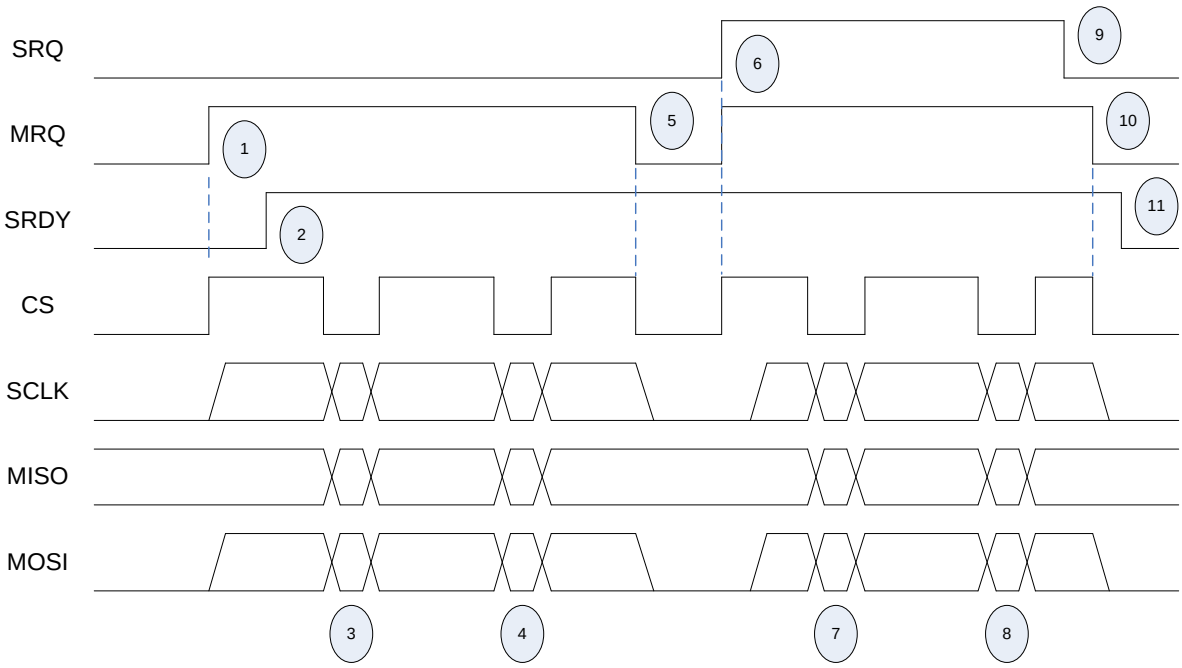


Figure 18. SPI Timing Example

Note that MRQ state transitions must respect the timing requirements shown in chapter 4.

The following items pertain to the numbered bubbles above:

1. Host has a message that it desires to send to Node. The first thing that it does is drive MRQ and CS high.
2. The Host then waits for the Node to drive SRDY high. No SPI bus transaction with the Node can occur before this.
3. After SRDY is high, the Host can start with the SPI data transaction. This is accomplished by driving the Node CS line low and then having the Host toggle the SCLK, and MOSI lines and having the Node toggle the MISO line according to the data to be transferred. The SPI Host interface specifies that first a MMsg pair is exchanged.
4. A MHdr pair is exchanged. Note that the payload of the message is appended to the MHdr.
5. The Host detects that the transaction is complete and that it does not wish to send more messages to the Node at this time. It drives the MRQ line low. Since MRQ is low, CS, SCLK and MOSI are tri-stated.

6. At some time in the future, the Node desires to send a message to the Host. It indicates this to the Host by driving SRQ high. Since SRQ is high, the Host drives MRQ and then CS high. It then waits for SRDY to go high, which it already is.
7. The Host starts the SPI data transaction. This is accomplished by driving the Node CS line low and then having the Host toggle the SCLK, and MOSI lines and having the Node toggle the MISO line according to the data to be transferred. The SPI Host interface specifies that first a SMsg pair is exchanged.
8. A SHdr pair is exchanged. Note that the payload of the message is appended to the SHdr.
9. The Node detects that the transaction is complete and that it does not wish to send more messages to the Host at this time. It drives the SRQ line low.
10. The Host detects that SRQ has gone low and that it does not have any messages to send to the Node. It drives the MRQ line low. Since MRQ is low, CS, SCLK and MOSI are tri-stated.
11. The Node drives the SRDY line low after MRQ goes low.

6.5 Host Message SPI Example

This section provides an example Host message exchange from master (Host) to slave (Node). In this example, the Host is sending a version request message.

This example is a zoomed-in view of the example provided previously in Figure 18. This section covers what happens in step 3, which includes the two SPI exchanges initiated by the Host.

With any SPI Host interface message, first an MMsg or SMsg pair must be exchanged. This pair contains information on how big the message is (from the message originator) and how much message queue space is available (on the message destination).

The following diagram shows such an example:

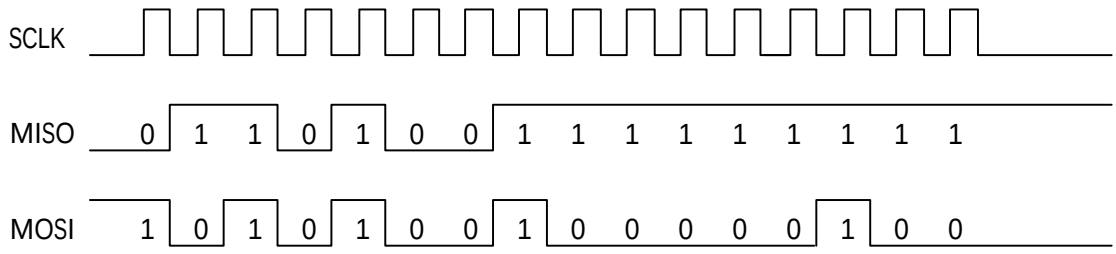


Figure 19. Host Message on SPI – MMsg Pair

The SPI clock edging is configurable with a polarity and phase. In order to communicate with the Node, the SPI clock polarity must be set to “the inactive state value of SPI clock is logic level zero” and the SPI clock phase must be set to “data is captured on the leading edge of SPI clock and changed on the following edge of SPI clock.” This means that the data lines (both MISO and

MOSI) are read on the SCLK rising edge and are set or cleared on the SCLK falling edge, and is commonly referred to as CPOL=0, CPHA=0.

This illustration shows that the bit streams for MISO and MOSI are:

- MISO: 0110100111111111
- MOSI: 1010100100000100

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MMsgACK (1001)

buffer size=255 (11111111)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MMsgREQ (1001)

payload size=4 (00000100)

An MMsg pair or SMsg pair is immediately followed by the corresponding MHdr pair or SHdr pair. This is illustrated below:

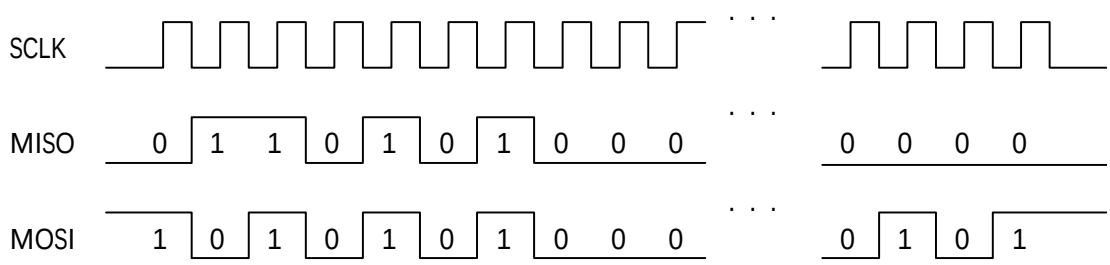


Figure 20. Host Message on SPI – MHdr Pair

For purpose of brevity, this timing diagram shows only a portion of the data exchange. The complete bit streams for MISO and MOSI are as follows:

- MISO: 011010100000000100000000000000000000000000000000000000000000000000000000000000000000000000000000
- MOSI: 101010100000000100001000000000000001010101000000111100001111000010100101101001 01

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MHdrACK (1010)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MhdrREQ (1010)

Hard coded byte=1 (00000001)

Payload:

length=8 (0000100000000000)

message type=VERSION (0001010101000000)

trailing sequence (11110000111100001010010110100101)

- The payload is Little Endian. The least significant byte is transmitted over SPI first.
- All MHdr and SHdr payloads are terminated by the fixed trailing sequence 11110000111100001010010110100101.
- The example above shows a message going from master to slave, thereby having a payload in the master to slave direction appended at the end of the MhdrREQ and no payload appended at the end of the MhdrACK.

6.6 Host Message "Connect" SPI Example

This section provides an example Host message exchange of the CONNECT message from master/Host to slave/Node and subsequent response from the slave to the master.

The timing is similar to the timing illustrated in the previous section, but the data and length of data is different.

The steps involved in this exchange are as follows:

The Host desires to send the CONNECT message to the Node. As described in the previous section, this starts with an MmsgREQ/MmsgACK exchange over the SPI bus.

- MISO: 0110100111111111
- MOSI: 1010100100000110

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MMsgACK (1001)

buffer size=255 (11111111)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MmsgREQ (1001)

payload size=6 (00000110)

The MMsg exchange is followed by the MHdr exchange, which includes the payload of the CONNECT message.

- MISO: 01101010000000010000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000
- MOSI: 10101010000000010000110000000000001100100100000000000001000000000000000000001111000011110000101001011010010 1

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MHdrACK (1010)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MhdrREQ (1010)

Hard coded byte=1 (00000001)

Payload:

length=12 (0000110000000000)

message type=CONNECT (0011001001000000)

host interface=True (00000001000000000000000000000000)

trailing sequence (11110000111100001010010110100101)

The payload of the message includes first the length, which is the number of bytes in the payload including the length and the trailing sequence.

It is followed by the message type, which in this case is 0x4032, and corresponds with CONNECT.

The CONNECT message has a 4-byte field that is a Boolean flag specifying whether or not the Node should send asynchronous SPI messages to the Host. To specify that the Node should send messages to the Host, the value of 0x00000001 is used.

It is then followed by the standard fixed trailing sequence.

This message exchange is followed by a Node-initiated message exchange for the purpose of sending an ACK of the CONNECT message to the Host. This starts with a SmsgREQ/SMsgACK exchange over the SPI bus.

- MISO: 0110101100000100
- MOSI: 1010101111111111

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=SMsgACK (1011)

buffer size=255 (11111111)

payload size=4 (00000100)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =SmsgREQ (1011)

buffer size=255 (11111111)

The SMsg exchange is followed by the SHdr exchange, which includes the payload of the ACK message.

- MISO: 01101100000000010000100000000000001100000000000011110000111100001010010110100101
- MOSI: 10101100000000010000000000000000000000000000000000000000000000000000000000000000000000000000

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=SHdrACK (1100)

Hard coded byte=1 (00000001)

Payload:

length=8 (0000100000000000)

message type=ACK (0011000000000000)

trailing sequence (11110000111100001010010110100101)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =ShdrREQ (1100)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

7 dNode Configuration

Node Provisioning Tools (NPT) are used for Node provisioning. Complete provisioning of Nodes involves three distinct utilities:

1. Node Software Upgrade Utility (sw_upgrade.py)
   This utility is used for upgrading the Node firmware.
2. Node Flash Configuration Utility (config_node.py)
   This utility is used for programming Node flash configuration parameters.
3. Node Key Provisioning Utility (provision_node_keys.py)
   This utility is used for programming Node Over-the-Air (OTA) security keys.

For details about Node Provisioning Tools, refer to the *NPT User Guide (010-0060-00).*

8 Antenna Diversity

The dNode supports Antenna Diversity for optimal System performance. In many cases, the dNode and Host system are mounted in fixed locations that often experience nulls in the RF spectrum. Antenna Diversity can help with optimization of the RX and TX paths. In marginal coverage areas, an RF null could easily disadvantage the dNode to enforce it to transmit at a higher TX Power (more current) or causes network loss and frequent rescanning to reacquire the network (again, more current). These scenarios produce customer dissatisfaction as well as increased battery drain. The dNode has two MMCX antenna ports that can be configured for diversity through the Node Provisioning Tools (NPT). The antennas should be mounted a minimum of 2.5" (7 cm) apart.

8.1 Antenna Design Requirements

Good antenna design and placement is also crucial to success. It is important to consider some pertinent issues.

- Ceramic antennas can work well but may sometimes have issues. Careful testing must be done to ensure desired gains and radiation patterns.
- The product must be researched in conjunction with the AP, its deployment, and its antenna radiation pattern. Nominally the AP will be mounted on a tower or mountain with a downward tilt. The dNode and System may be mounted vertically or horizontally, forcing requirements on the dNode's optimal radiation pattern.
- The antenna must be well-matched and with low loss between the dNode and the antenna. It is important to follow the manufacturer's recommendations.
- Metallic objects nearby to the antenna can affect radiation gains, patterns, and power match. Typically anything within 4 to 5 inches can affect the match significantly, particularly if the nearby metal is resonant at 2.4 GHz. A little pattern distortion is usually not too concerning unless deep wide angular nulls in the antenna pattern results. Other types of pattern distortion can be caused by absorptive losses due to lossy dielectrics nearby the antenna, which represents real power loss dissipated as heat in the loss object. This represents power that is completely lost and not radiated in a useful direction.
- Noisy system clocks with harmonics can fall into the operating band of the dNode and can be picked up by the antennas degrading sensitivity or causing Electromagnetic Compatibility (EMC) regulatory failures.

8.2 Diversity Considerations

The operating frequency of the dNode is the ISM 2.4GHz band. This has a wavelength of 12.3 cm in air. For optimal null/peak diversity detection, the antennas must be separated by at least 2.5" (5 cm). It is a good idea on the diversity antenna to orient it 90 degrees from the main antenna in order to improve on polarization diversity between antennas in addition to spatial de-correlation.

9 Regulatory Considerations

The dNode uses two MMCX connectors for its RF ports. On-Ramp Wireless provides FCC/IC modular approval certification as well as ETSI certification for the dNode. The dNode was certified on an On-Ramp Wireless application platform known as the eHost. These documents and results are available to System Integrators to ensure that the product can be certified.

Additionally, On-Ramp Wireless has prepared certification guidelines on how to use the software and system tools required for certification. Some markets (such as FCC/IC) are fairly straight forward for certification and are largely TX Spectrum-based. Other markets (such as ETSI) require a much more sophisticated FER process involving an Access Point and Quick Start System. These procedures are defined in the document entitled *Node FCC/IC/ETSI EMC Compliance Test Procedures (009-0021-00).* This document also includes hints and recommendations to help make the process as easy as possible. For more information about this document, see the list of documents referenced in Chapter 1: Overview.

9.1 Block Diagram

Some regulatory domains require a block diagram of the module for their documentation similar to that shown in the following figure.

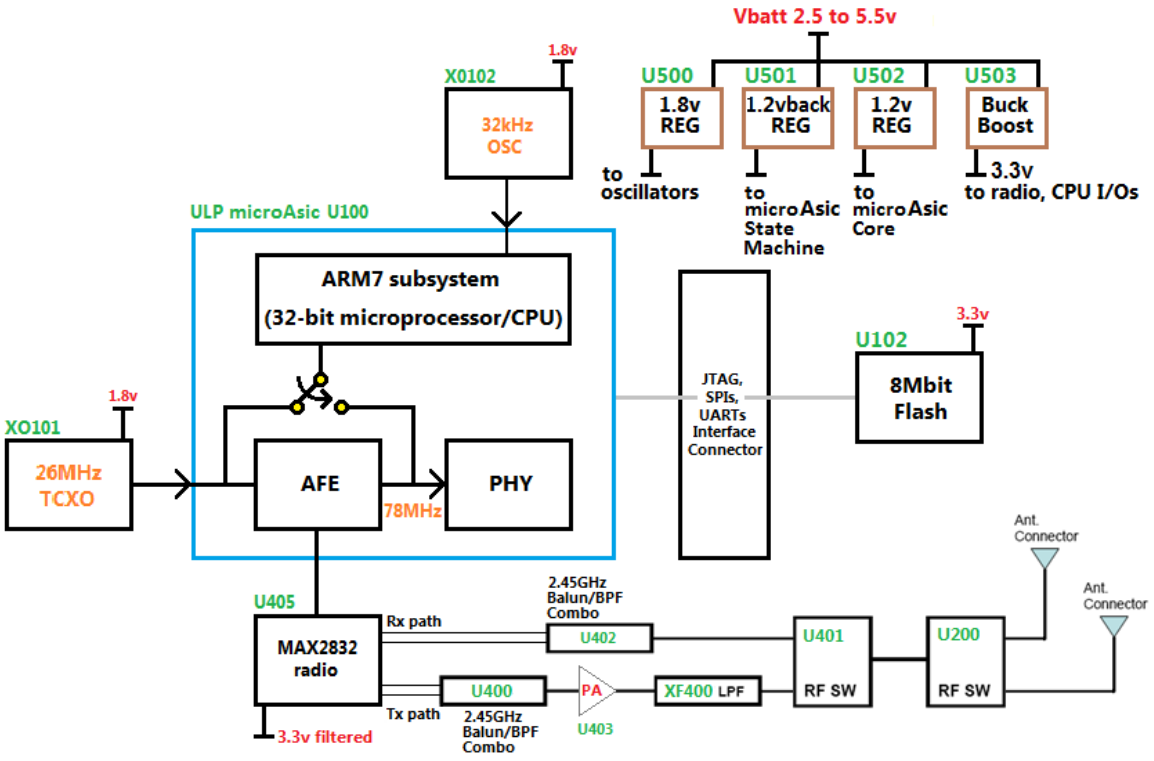


Figure 21. dNode Block Diagram

9.2 Certifications

The dNode is designed to meet regulations for world-wide use. It is has modular approval certification in the United States and Canada, and ETSI certification in Europe. The certifications currently achieved are listed in the following table.

Table 8. dNode Certifications

Country	Certifying Agency	Certification(s)
United States	Federal Communications Commission (FCC)	n 15.207 for powerline conducted emissions. n 15.215 for RF TX bandwidth, power, conducted and radiated emissions.
Canada	Industry Canada (IC)	n RSS210e, includes FCC tests and IC-specific tests (RX radiated emissions).
Europe	European Telecommunications Standards Institute (ETSI)	n 300 440-1 and 440-2, ETSI Emissions. n 301 489-1, ETSI Immunity.

Additional details can be found in the document entitled *Node FCC/IC/ETSI EMC Compliance Test Procedures (009-0021-00)* referenced in Chapter 1: Overview.

The integrator of the final product is often required to do additional compliance tests. The integration application and market will determine specifics. The integrator is advised to consult with local experts in compliance certifications for complete information.

- **FCC/IC**
  The dNode is Single-Modular Certified, therefore the final product may only need Class B unintentional radiator and powerline conducted emissions tests. This should be done with the actual production antenna.
- **ETSI**
  Europe's system is a self-declaration system. There are no documents to submit or certification grants to obtain. One must have the passing test results available for all applicable requirements at any time if challenged.
- Other countries will vary.

9.3 FCC Warnings

This device complies with part 15 of the Federal Communications Commission (FCC) Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

WARNING: This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the instructions, this equipment may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Re-orient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

9.4 IC Warnings

The installer of this radio equipment must ensure that the antenna is located or pointed so that it does not emit RF field in excess of Health Canada limits for the general population. Consult Safety Code 6 which is obtainable from Health Canada's website http://www.hc-sc.gc.ca/index-eng.php.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

To reduce potential radio interference to other users, select the antenna type and its gain so that the equivalent isotropically radiated power (EIRP) is not more than that permitted for successful communication.

Canadian Two Part Warning Statement:

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

9.5 ETSI Warnings

None known.

9.6 Usage

FCC ID: XTE-ULPD100. IC: 8655A-ULPD100. This device is only authorized for use in fixed and mobile applications. To meet FCC and other national radio frequency (RF) exposure requirements, the antenna for this device must be installed to ensure a separation distance of at least 20cm (8 inches) from the antenna to a person.

9.6.1 Note to Integrators

A label showing the FCC ID and IC designators, listed above, must be affixed to the exterior of any device containing the dNode (if the dNode is not visible). The exterior label must include: *Contains FCC ID: XTE-ULPD100, IC: 8655A-ULPD100*.

9.6.2 RF Exposure Statement

The air interface supports operation on channels in the 2402 MHz – 2476 MHz range for FCC/IC regulatory domains and 2402 MHz – 2481 MHz for the ETSI regulatory domain.

Before the ULP dNode becomes operational, it must undergo a commissioning procedure, during which critical information required for operation is entered into the device and stored in non-volatile storage. It is during the initial commissioning procedure that the regulatory domain, under which the device will operate, is set. Subsequent configuration of the device during operation is checked against the commissioned regulatory domain and non-permitted channels or transmit power levels are rejected and the device will not transmit until a permissible configuration per the commissioned regulatory domain is set.

9.7 Antennas

This dNode has been certified to operate with the antenna listed below. To adhere to these certifications requires the antenna to have a peak gain of 2 dBi or less and to have monopole construction (Omnidirectional pattern). Antennas that do not have monopole construction or a gain greater than 2 dBi are strictly prohibited for use with the dNode, per On-Ramp Wireless' EMC certifications. The required antenna impedance is 50 ohms.

Table 9. On-Ramp Wireless EMC Certified Antenna

Manufacturer	Part Number	Gain	Type	Connector	Comment
L-com	HG2402RD-RSF	2 dBi	Monopole	RP-SMA Plug	MMCX Plug to RP-SMA Jack adaptor required.

Customers are free to follow one of two paths in their final product:

- Customers can use On-Ramp Wireless' antenna type with a gain ≤ 2 dBi. This path allows customers to use On-Ramp Wireless' certifications. While ideal from the perspective of

program cost and schedule, the ability to reuse this antenna is highly dependent on the application.

- Customers can recertify the final product with any antenna type and gain desired. In the case of FCC/IC EMC certifications, it is almost always required for the final product to be recertified with the dNode. If this is the case, note that the recertification is the required time to introduce the final product's actual antenna.

10 Design Considerations for the Host

The dNode has two 10-pin Single Inline Package (SIP) headers that allow for two Host mounting methods: Socketed and Direct Solder.

10.1 Host Mounting Method: Socketed

The Socketed Host mounting method is preferred since it permits easy insertion, removal, and network provisioning of the dNode on a separate Host. It is important to follow some layout constraints and the recommended design guidelines of the socket manufacturer. It is important to use a high quality socket with very low impedance. Some less expensive sockets have been found to generate high resistance on their pins over time. This is especially true with the all-important Vbatt and Ground pins of the dNode. A representative high quality socket has been found to be: Mill-Max PN 834-43-010-10-001000. For details about Mill-Max Series 834/835 series SIP sockets, refer to www.mill-max.com.

10.1.1 Host PCB Land Pattern

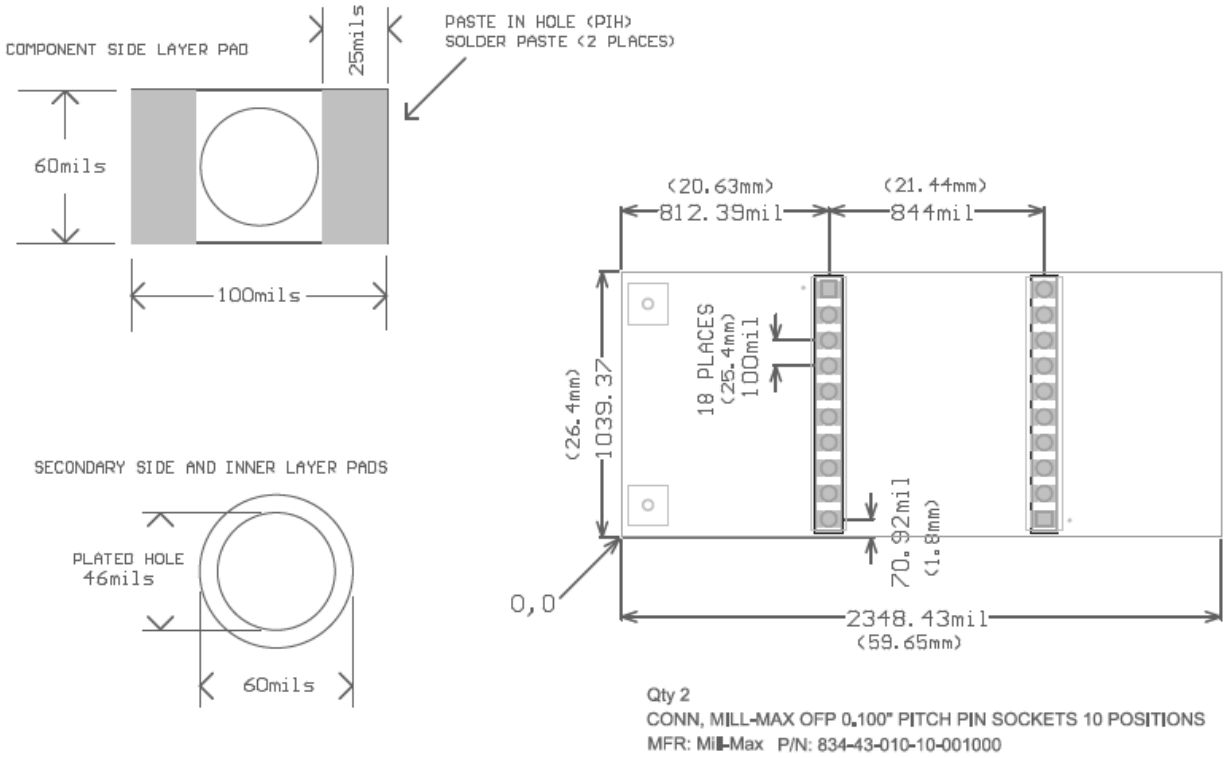


Figure 22. Host PCB Land Pattern – Mill-Max Socket

10.1.2 Pad Stack for Mill-Max Series 834

Paste In Hole (PIH) soldering technique allows for installation of the Mill-Max 834 series connectors during the SMD reflow process. As shown below, the component side pad is a large rounded rectangular (100x60 mils) and all other pads are 60 mil round pads, with all pads using a plated drill hole of 46 mils.

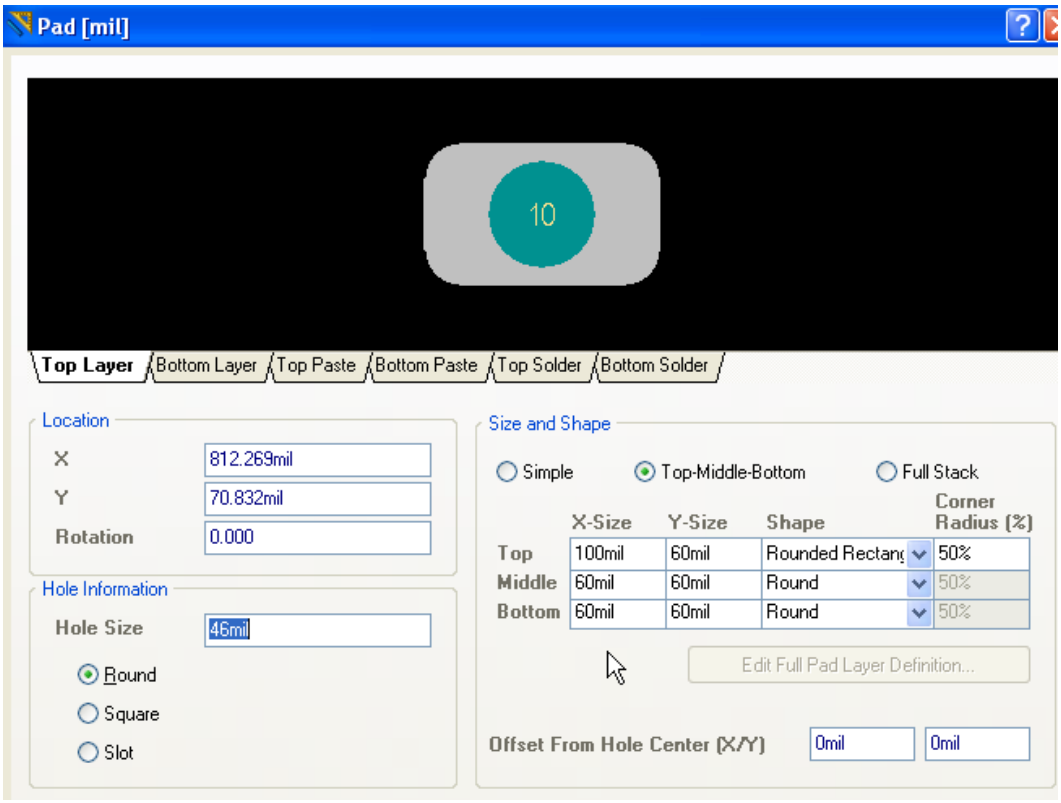


Figure 23. Pad Stack for Mill-Max Series 834

10.2 Host Mounting Method: Direct Solder

The Direct Solder method of mounting the dNode gives little flexibility in insertion/removal but is the least expensive and can provide Low resistance on the Vbatt/Ground paths. PCB layout considerations are provided below.

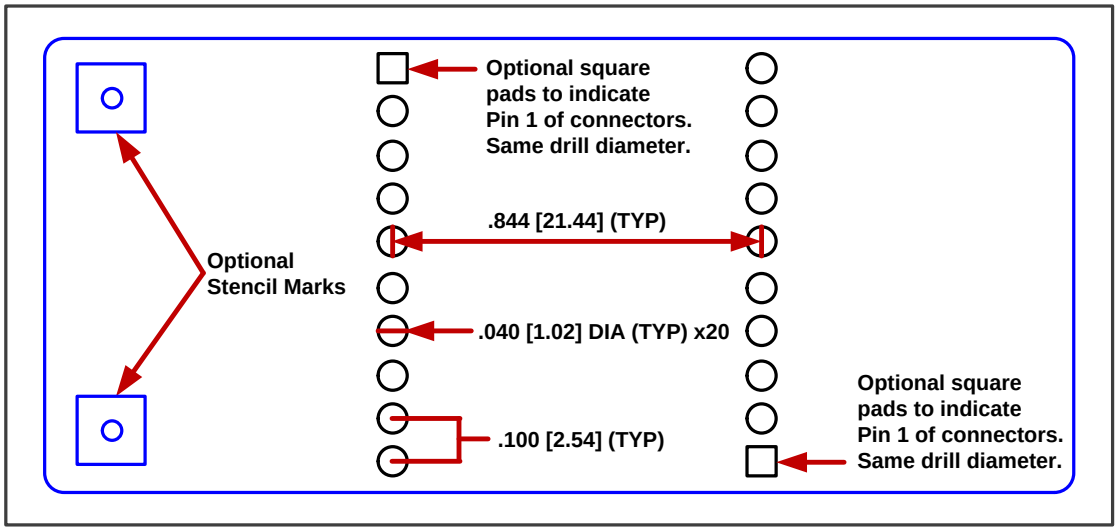


Figure 24. Host PCB Land Pattern – Direct Solder

11 Errata

Degraded RF Channels

The dNode uses a Channel scheme such as the following:

- Channel 1 = 2402 MHz and each successive channel is 1.99 MHz offset to that Channel 1.
- Channel 2 = 2403.99 MHz
- Channel 3 = 2405.98 MHz
- Etc.

The dNode uses a 26 MHz reference clock for processing and for the direct conversion radio. It has been found that 26 MHz harmonics can create strong tones that cause some RF sensitivity degradation on these harmonic channels.

- 93*26 MHz = 2418 MHz. This affects channel 9.
- 94*26 MHz = 2444 MHz. This affects channel 22.
- 95*26 MHz = 2470 MHz. This affects channel 35.

System integrators should NOT use these 3 channels as dNode RX sensitivity can be degraded by a nominal 3-10 dB.

Refer to On-Ramp Wireless Issues #2319 and #2616.

Appendix A Abbreviations and Terms

Abbreviation/Term	Definition
AGC	Automatic Gain Control
ALC	Automatic Level Control
AP	Access Point (this product)
API	Application Programming Interface
ASIC	Application-Specific Integrated Circuit
BOM	Bill of Materials
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
CPOL	Clock Polarity (for SPI)
CPU	Central Processing Unit
DFS	Dynamic Frequency Selection
dNode	Third generation of the ULP wireless module that integrates with OEM sensors and communicates sensor data to an Access Point.
DPLL	Digital Phase-Locked Loop
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FER	Frame Error Rate
GND	Ground
GPIO	General Purpose Input/Output
HBM	Human Body Model
IC	Industry Canada
IIP3	Input Third-Order Intercept Point
LDO	Low Drop Out
LNA	Low Noise Amplifier
LO	Local Oscillator
microNode	Second generation of the ULP wireless module that integrates with OEM sensors and communicates sensor data to an Access Point.
MISO	Master Input, Slave Output
MM	Machine Model
MOSI	Master Output, Slave Input
MRQ	Master Request
MSL	Moisture Sensitivity Level
Node	The generic term used interchangeably with eNode, microNode, or dNode.
NPT	Node Provisioning Tools

Abbreviation/Term	Definition
OTA	Over-the-Air
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
POR	Power On Reset
QoS	Quality of Service
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RoHS	Restriction of Hazardous Substances
RSSI	Receive Signal Strength Indicator
RT	Remote Terminal
RTC	Real Time Clock
RX	Receive/Receiver
SCLK	Serial Clock
SMT	Surface Mount Technology
SNR	Signal-to-Noise Ratio
SPI	Synchronous Peripheral Interface
SRDY	Slave Ready
SRQ	Slave Request
TX	Transmit/Transmitter
UART	Universal Asynchronous Receiver/Transmitter
ULP	Ultra-Link Processing™. On-Ramp Wireless proprietary wireless communication technology.
UNIL	ULP Node Interface Library
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator
VSWR	Voltage Standing Wave Ratio
XO	Crystal Oscillator

Appendix B dNode Mechanical Drawing

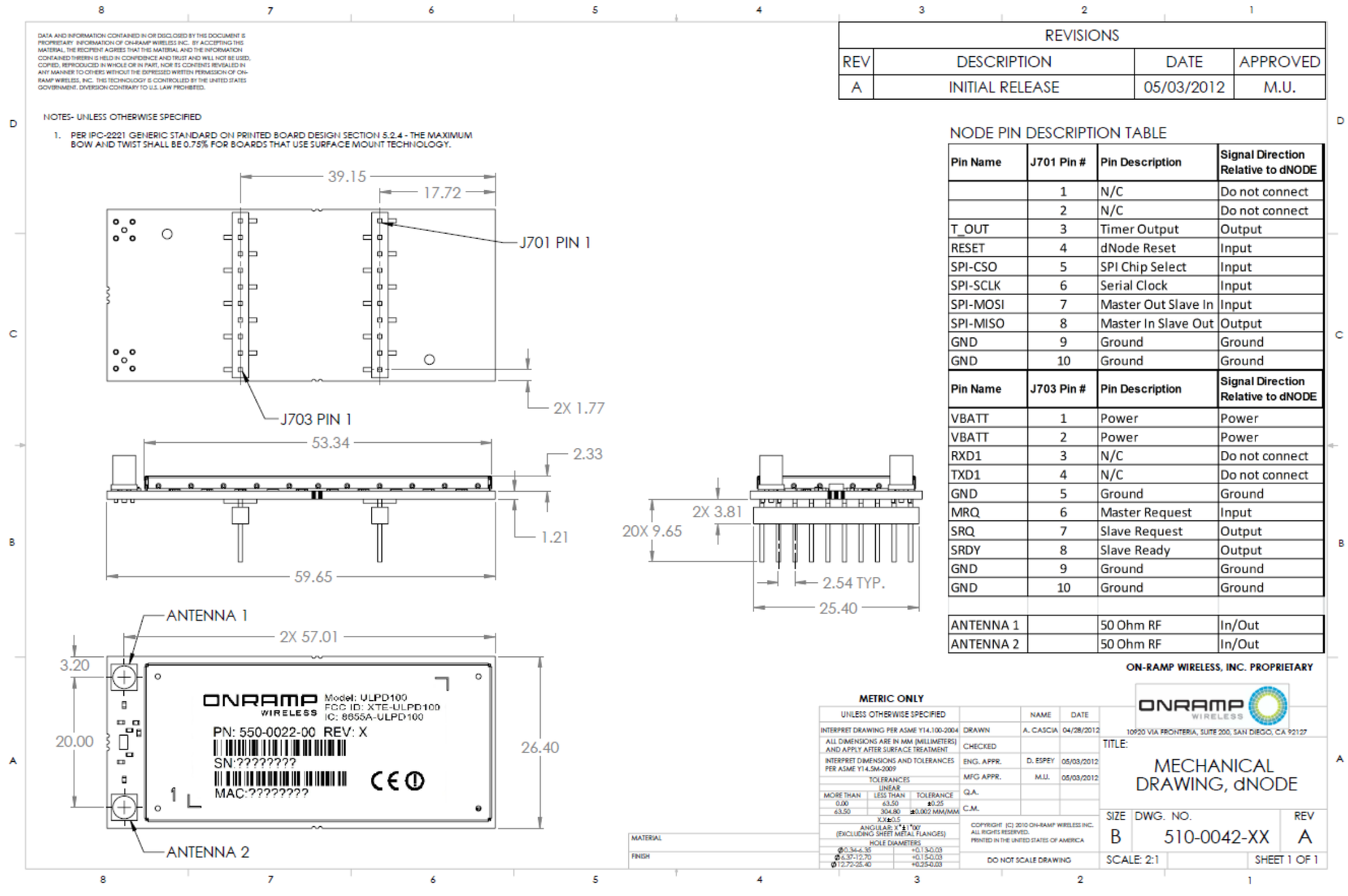


Figure 25. dNode Mechanical Dimensions