Ultra-Link Processing™

eNode User Manual

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Version	Date	Author	Remarks
1.0	2/12/10	ORW	Initial Release
1.1	2/29/10	ORW	Updated with certification comments (Sect 4.3 and 4.4)

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2 SCOPE

2.1 WHAT DOES THIS DOCUMENT COVER?

This document describes the On-Ramp Wireless Ultra-Link Processing™ (ULP) eNode. It describes the use of the eNode within a ULP wireless packet data network and the hardware and software interfaces of the device.

2.2 WHO SHOULD USE THIS MANUAL?

Customers integrating On-Ramp's eNode module in to their sensor and location tracking systems, referred to as Hosts in this document. For additional details on host application integration with the eNode please refer to the eNode Specifications and Programming Guide.

2.3 REFERENCE DOCUMENTS

3 INTRODUCTION

The ULP wireless packet data network, comprised of eNodes and Access Points operates at a breakthrough receive sensitivity of -142 dBm. This dramatic increase in receive sensitivity allows for a wireless range of 2,000 miles in free space and 25x the range (600x the coverage) of typical wireless sensor systems while maintaining a small and low-cost form factor with multi-year battery operation.

The ULP eNode is designed to easily integrate, via standard interfaces, with sensors enabling robust wireless communication with one or more Access Points interfaced with a customer's local or wide area network.

Each Access Point supports tens of thousands of sensors and can simultaneously demodulate signals from up to a 1000 sensors using a unique patented multiple access scheme. With 172 dB of total allowable path loss (FCC/IC regulatory regions) the ULP network can easily be deployed using a star topology configuration, overcoming the limitations of legacy wireless sensor networks (802.11, 802.15.4, 900 MHz FHSS) that require complicated mesh protocols to extend range or operate in a capacity limited simplex mode.

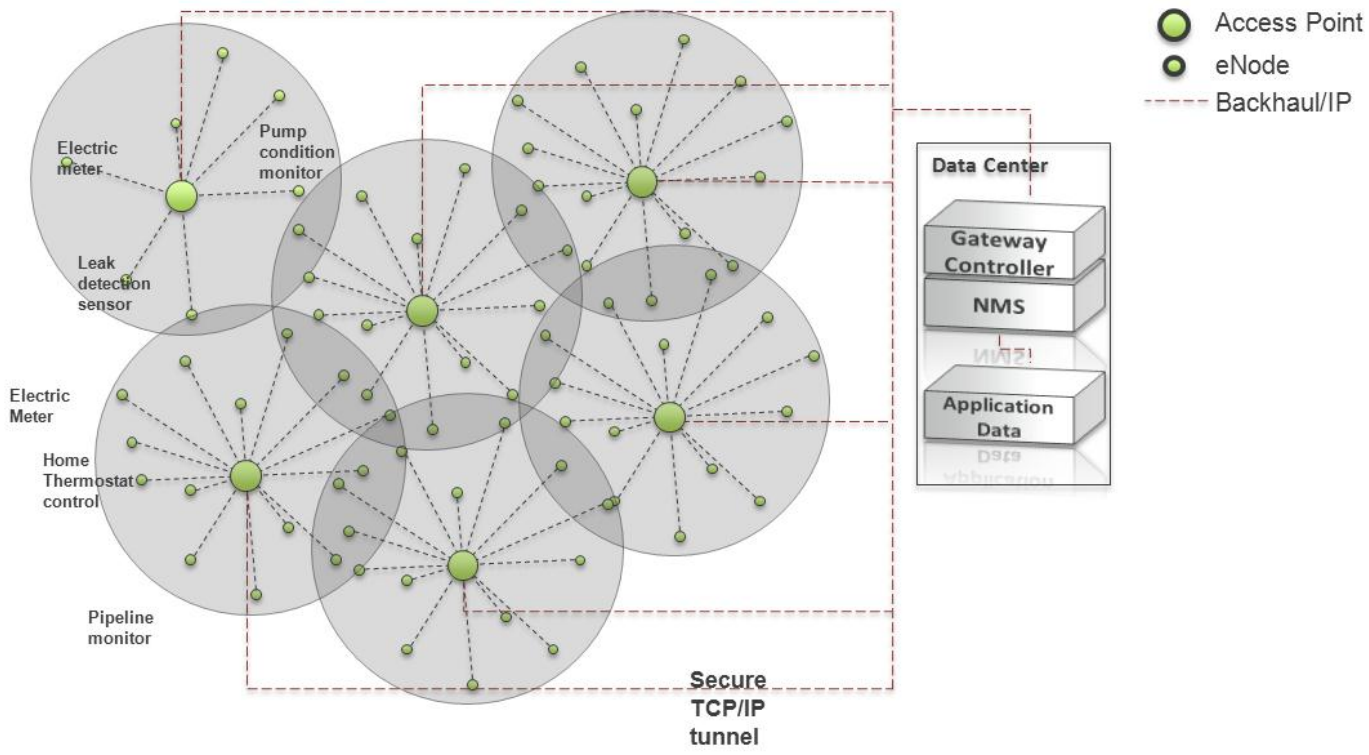

Figure 1 On-Ramp Wireless ULP Network

4 APPROVALS

The eNode has been designed to meet regulations for world-wide use.

4.1 FCC

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.
—Increase the separation between the equipment and receiver.
—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
—Consult the dealer or an experienced radio/TV technician for help.

4.2 INDUSTRY CANADA

The installer of this radio equipment must ensure that the antenna is located or pointed such that it does not emit RF field in excess of Health Canada limits for the general population; consult Safety Code 6, obtainable from Heath Canada's website www.hc-sc.gc.ca/rpb.

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

4.3 USAGE

FCC ID: XTE-ULPENODE100. IC: 8655A-ULPENODE100. This device is only authorized for use in mobile applications. To meet FCC and other national RF exposure requirements the antenna for this device must be installed to ensure a separation distance of at least 20cm (8 inches) from the antenna to a person.

4.4 ANTENNAS

This device has been designed to operate with the antennas listed below, and having a maximum gain of 5 dB. Antennas not included in this list or having a gain greater than 5 dB are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

5 dB omni-directional antenna
2 dB omni-directional antenna
1 dB omni-directional antenna

5 ENODE OVERVIEW AND INTERFACES

The eNode platform provides ULP modem functionality on the client side. The eNode platform handles PHY & MAC layers (L1 and L2) for the ULP technology. The eNode platform supports interfacing over Serial Peripheral Interface (SPI).

The eNode easily integrates with Sensor or Locating tracking system using the software and hardware interfaces supported. The eNode acts as the slave device and expects the host board to act as master.

5.1 HARDWARE INTERFACE

5.1.1 SPI SLAVE INTERFACE

The SPI Slave eNode Interface provides communication with an external host via a serial peripheral interface (SPI). The host is the SPI master and the eNode is the SPI slave. In addition to the standard SPI signals, a host-to-node wakeup request, a node-to-host status and a node-to-host transmit request are included to support eNode state transitions and bi-directional message traffic.

5.1.2 PIN DESCRIPTION

Pin Name	Pin #	Pin Description	Type		Remark
			Master	Slave	
SPI-MISO	J701, 8	Master In Slave Out	In	Out	SPI Bus data line in the direction of slave to master.
SPI-MOSI	J701, 7	Master Out Slave In	Out	In	SPI Bus data line in the direction of master to slave.
SPI-SCLK	J701, 6	Serial Clock	Out	In	SPI Bus clock driven by master. Depending on how polarity and phase are configured, this clock's edges indicate when the data on MISO and MOSI are valid.
SPI-MRQ	J703, 6	Master Request	Out	In	Driven by the master to indicate to slave that SPI activity needs to take place. If the slave is sleeping, this signal will wake it up. When the slave detects this signal high, it must respond by driving Slave Ready high.
SPI-SRDY	J703, 7	Slave Ready	In	Out	Driven by the slave to indicate to the master that it is awake and ready to perform SPI Bus transactions.
SPI-SRQ	J703, 8	Slave Request	In	Out	Driven by the slave to indicate that it wishes to send a message over SPI Bus to the master. This is necessary since master drives the clock and this gives the slave a way to inform the master that the slave wishes the clock to be driven.
SPI-CS0	J701, 5	SPI Chip Select	Out	In	Used by Master to select which slave it is communicating with over SPI Bus
RXD0	J701, 1	Serial 0 Receive	Out	In	Reserved for future use.
TXD0	J701, 2	Serial 0 Transmit	In	Out	Reserved for future use.
T_OUT	J701, 3				TBD
RESET	J701, 4	eNode Reset	Out	In	Provides Host with ability to reset the eNode.
RXD1	J703, 3	Serial 1 Receive			Reserved for future use
TXD1	J703, 4	Serial 1 Transmit			Reserved for future use
VBATT1	J703, 1				
VBATT2	J703, 2				
GND	J701, 9				
GND	J701, 10				
GND	J703, 5				
GND	J703, 9				
GND	J703, 10				

Table 1 ***eNode Pin Description***

5.1.3 ELECTRICAL CHARACTERISTICS

- Module signals are defined as CMOS compatible 3V levels. The actual 3V levels could be between 3.0V and 3.6V.
- The eNode board converts the input voltage (VBATT) to its own required voltage levels. The input voltage range is 2.4V to 5.5V.
- The board can consume up to two (2) watts during transmission, its maximum power mode. The power supply to the eNode must be able to supply enough current at a given operating voltage to provide two (2) watts.
- The eNode is specified to operate over a temperature range of -40C to +85C ambient temperature.
- SPI signals are part of the 7-wire SPI interface system
- RX/TX Are part of the UART. UART Devices are reserved for future use for general Modem communications.

5.1.4 ENODE DIMENSIONS

The figure below shows the eNode dimensions.

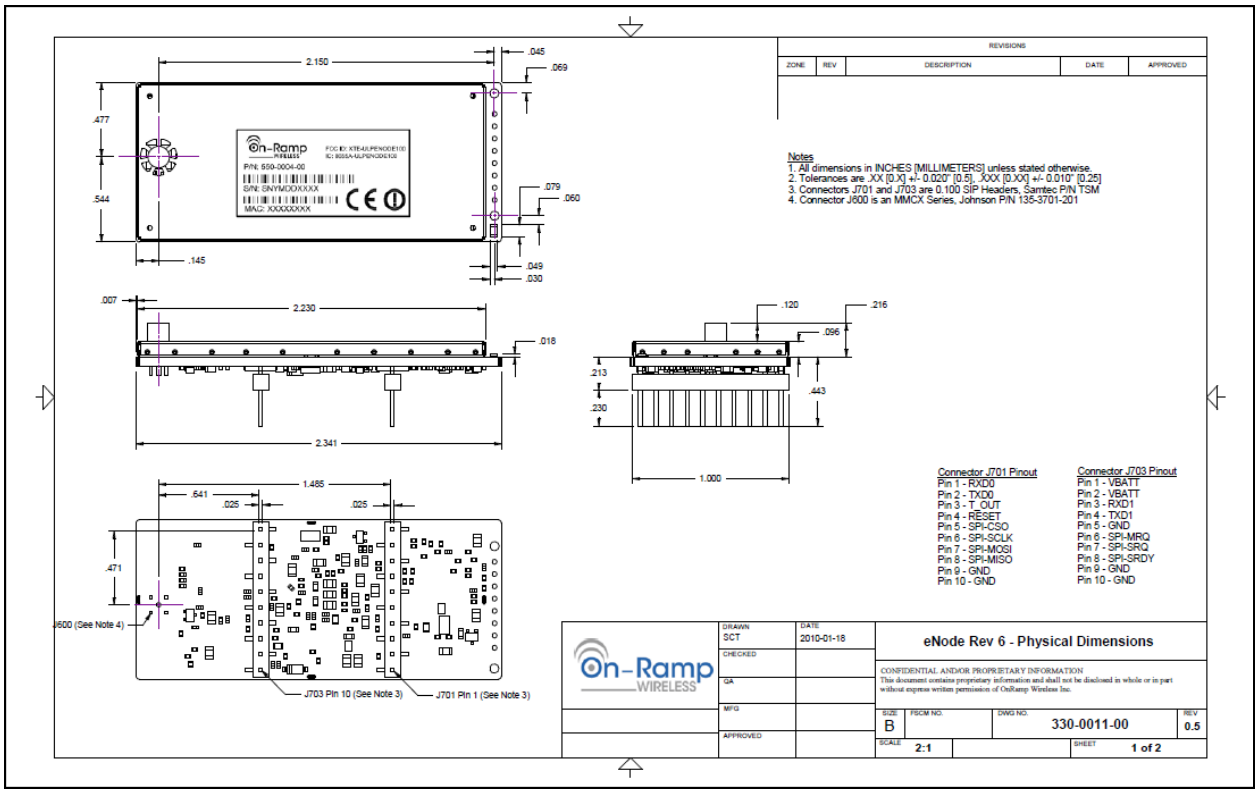

Figure 2 eNode Mechanical Dimensions

5.2 SOFTWARE INTERFACE

On-Ramp's eNode platform's Software Interface includes the node resident SPI driver for the Interface Hardware and the node resident messaging application. While the driver enables the hardware for data transfer, the messaging application implements user level messages which enable the host to control the behavior of the node. Using these messages the host can control the eNode all the way from integration to deployment, including commissioning and configuration.

The SPI driver initializes and manages the SPI hardware. Together with SPI hardware, the driver implements the SPI interface. On-Ramp's SPI Interface has additional features that support sleep & wake-up requests.

The Host interface provides functionality described in next section. The host interface layer is hardware independent and can run on SPI.

Note: The SPI Master driver and Host Interface Protocol application on the host need to be developed by the owner of the 'host'. They are not provided by On-Ramp. Some sample code is available.

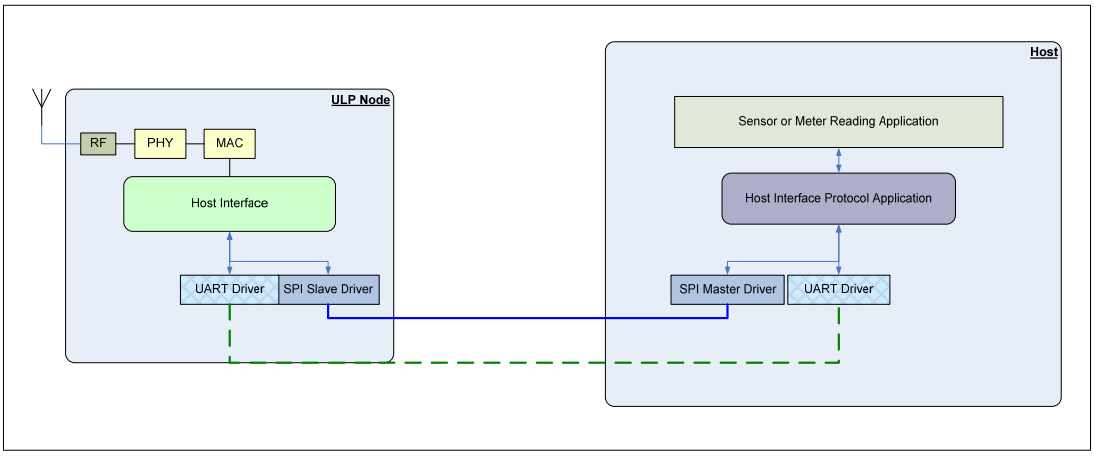

Figure 3 eNode SPI interface

5.3 HOST INTERFACE

5.3.1 FUNCTIONAL DESCRIPTION

The host interface supports the higher layer messages for:

- Commissioning the eNode from the Host
- Configuring the eNode from the Host
- Controlling the startup and steady state behavior of the eNode
- Transferring payload data to and from the Host
- Upgrading the Software on the eNode. [Future releases]
- Executing a set of diagnostic tests on the eNode. [Future releases]
- Collecting debug data from the eNode. [Future releases]

The messages can be broadly classified as Debug, Configuration, and User Data messages.

5.3.2 HOST INTERFACE PROTOCOL

On-Ramp's ULP eNode's host interface supports reliable transfer of messages between the host and eNode over SPI. To support this functionality:

- Explicit 'Connect' and 'Disconnect' messages are supported.
- Each host-to-node message is acknowledged. This is useful in reliability and also for back-pressure, where the host needs to slow down or stop sending messages to the eNode. The node-to-host messages do not have any acknowledgements. The eNode will not wait for acknowledgements. The eNode expects the host to be able to receive all messages and keep up with the eNode.
- For the SPI interface, the host (being the SPI master) is expected to be fast enough so as to not block various operations at the eNode. If this is violated, the eNode will miss RX/TX events.

The SPI Driver provides methods for basic bit/byte transport. To do that there are SPI message requests, SPI message headers and SPI payload. The SPI payload contains the Host Interface message.

5.3.3 SIGNAL DESCRIPTION

Pin Name	Pin Description	Type	
		Master	Slave
MISO	Master In Slave Out	In	Out
MOSI	Master Out Slave In	Out	In
SCLK	Serial Clock	Out	In
SS	Slave Select	Out	In
MRQ	Master Request	Out	In
SRDY	Slave Ready	In	Out
SRQ	Slave Request	In	Out

Table 2 eNode SPI Signal Definition

5.3.4 MASTER REQUEST / SLAVE READY

Before initiating transfers to and from the node, the host must ensure the node is awake and ready to receive SPI traffic by driving MRQ high and waiting for the node SPI slave to drive SRDY high. A high level on MRQ will wake up a sleeping node and will prevent the node from going back to sleep.

5.3.5 SLAVE REQUEST

The node requests a message transfer from node-to-host by driving the SRQ high. Hosts that support bi-directional SPI traffic respond to SRQ by sending a message request to the node after the completion of any ongoing transfers.

5.3.6 OTHER SIGNALS

Other signals i.e. MISO, MOSI, SCLK, SS are as per SPI Standard.

5.3.7 SPI INTERFACE DRIVER

The node SPI Slave Interface software driver provides a messaging protocol for interfacing to a host device running an On-Ramp host SPI master driver and for interfacing to a device running its own driver.

The On-Ramp host SPI master driver uses a messaging protocol that is active only after the host has completed an arbitration sequence. This allows the node to pass traffic across the SPI interface to both a host and a non-host device.

5.4 SOFTWARE UPGRADE PROTOCOL

5.4.1 OVERVIEW

The node supports upgrading of its software via the host SPI interface. This mechanism allows a host which has access to a new software image to transfer the image to an attached node in small pieces and have them written to flash. After the entire image has been transferred the node is powered cycled to boot the new software image.

5.4.2 REQUIREMENTS

The node must be in the idle state when a software upgrade is attempted. The duration of an upgrade cycle is dependent on the host but is at least 180 seconds.

Power must be maintained during an upgrade cycle. Power loss during an upgrade cycle will result in a non-functional node.

5.5 NOTES AND RECOMMENDATIONS

- The eNode processor is based on ARM and hence Little Endian.
- At the SPI interface level
  - Arbitration needs to be typically done at startup time and after exiting out of deep sleep modes. In addition to the normal case, the eNode supports Arbitration at-will. When the host initiates arbitration, the eNode will comply. This could be used to exit out of error conditions.
  - eNode to Host communication takes priority over Host to eNode, as there are buffer with limited sizes on the eNode. Buffer over flows could cause unspecified results at the eNode. When there is a race condition between Host-to-eNode and eNode-to-Host data transfer initiation, then the eNode-to-Host is given priority. But if a Host-to-eNode transfer is in progress, then the eNode will wait for the transfer to complete.