microNode Integration Specification

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microNode Integration Specification

014-0033-00 Rev. B

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Revision History

Revision	Release Date	Change Description
A	January 18, 2012	Initial release.
B	March 13, 2012	n Expanded information for regulatory considerations and certifications. n Removed errata section that is no longer relevant.

1 Overview

The purpose of this document is to provide guidelines allowing an integrator to design a Host product that utilizes the microNode and ensures that the system meets all of its technical objectives and requirements.

The following documents are referenced and provide more detail.

- **ULP Node Interface Library (UNIL) (010-0066-00)**
  Provides information about the library of portable C code provided by On-Ramp Wireless which can be integrated into a customer's existing software architecture.
- **UNIL API (010-0072-00)**
  Provides details relating to the UNIL Application Programming Interface.
- **ULP Node Host Message Specification (014-0020-00)**
  Provides details relating to Node Host messages.
- **Node FCC/IC/ETSI EMC Compliance Test Procedures (009-0021-00)**
  Describes/explains the FCC/IC/ETSI EMC compliance tests and how to use On-Ramp Wireless's configuration software for these tests.
- **NPT User Guide (010-0060-00)**
  Describes the setup, configuration, and use of a collection of utilities called Node Provisioning Tools (NPT) used for Node provisioning.

2 DC and AC Characteristics

2.1 Absolute Maximum Ratings

Operating outside of these ranges may damage the unit.

The microNode is MSL 3-rated and should be handled as an MSL 3 device per IPC/JEDEC J-STD-033 (latest revision). See section 10.3.1 for further information.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-40	85	ºC
Operating Temperature	-40	85	ºC
Input Voltage	2.2	5.5	V
Digital Interface Signals, 3.3V nominal	3.0	3.6	V

2.2 Recommended Operating Conditions

Table 2. Operating Conditions

Parameter	Min	Max	Unit
Input voltage, VBATT	2.2	5.5	V
Ambient Temperature, Ta	-40	85	ºC

The following characteristics apply across the -40°C to +85°C temperature range unless otherwise noted.

Table 3. Operating Characteristics

Description	Min	Typ	Max	Units
DC Characteristics				
Voltage – VBATT	2.2	3.6	5.5	Volt
Off Current – Note 1	0.05	0.1	2.0	µA
Deep Sleep Current - Note 1	10	20	40	µA
Idle Current – Note 1	10	15	25	mA
Receive Current – Note 1	75	85	90	mA
Transmit Current – Note 2	200	245	280	mA
Digital				
VOL – Voltage Output, Low (4mA sink)	0		0.1	V
VOH – Voltage Output High (4mA source)	Vdd-0.9		Vdd-0.1	V
Environmental				
Operating Temperature	-40		+85	°C

Description	Min	Typ	Max	Units
Storage Temp	-40		+85	°C
Humidity – non-condensing	5		95	%
Ramp Temperature (maximum rate at which operating temperature should change)			30	°C/Hr.
Receiver				
Receiver Sensitivity – Note 3	-140	-142	-144	dBm
Receiver Image Reject	38	45	50	dB
Noise Figure	3.5	5.0	6.7	dB
Input IP3 (high LNA gain mode)		-11		dBm
Maximum RF input level for specification compliance			-20	dBm
General RF Characteristics				
Frequency Range – Note 4	2402		~2482	MHz
Channel Spacing	N/A	1.99	N/A	MHz
Transmitter				
Maximum RF Conducted Power –Note 5 FCC/IC markets: ETSI markets:	 20.0 8.5	 21.3 9.5	 21.5 10.0	 dBm dBm
Carrier Rejection	-35	-40	-50	dBc
Signal Modulation		DSSS-DBPSK		
Signal Bandwidth		1.0		MHz
BT Factor		0.3		
Peak to Average Ratio		2.3		dB
Spectral bandwidth at maximum RF power: -6dB BW -20dB BW		 0.96 1.75		 MHz MHz
ACPR – Note 6			-30	dBc
Harmonics – Note 7			-43	dBm
Transmit Power Level Accuracy – Note 8			±1.5	dB
Transmitter Spurious Outputs – Note 9 30MHz to 2400MHz: 2482MHz to 8000MHz:			 < -43 < -43	 dBm dBm
VSWR Tolerance Maximum VSWR for spec compliance – Note 10: Maximum VSWR for stability.			 1.5:1 9:1	

NOTES:

1. Tested at 3.6V input.
2. Measured at 21.5 dBm TX output (Typ=50W), 3.6V, range includes VSWR ≤ 1.5:1 (Po not compensated).
3. Sensitivity at maximum spreading factor of 13 (8192) with 10% FER.

4. The upper frequency range is market dependent:
   a. FCC/IC: CH38; 2475.63 MHz.
   b. ETSI: CH40; 2479.61 MHz.
   c. Japan: CH41; 2481.60 MHz.
5. Maximum TX RF power is limited by FCC/IC grant to 21.5 dBm in these markets.
6. Spec and test method comes from FCC 15.247(d); Band Edge Emissions, 2 MHz offset.
7. At any TX power level, VSWR ≤ 3:1. Harmonics fall into FCC restricted bands.
8. Estimated sum of all contributors with VSWR ≤ 1.5:1. Normal link mode.
9. At any TX power level, VSWR ≤ 3:1. Applies to spurious, not ACPR or harmonics. Generally the largest spurious output outside the 2.40-2.48GHz band is at 2/3LO and 4/3LO.
10. Maximum VSWR for spec compliance applies at 25C only. Slightly degraded ACPR/mask and power variation can be expected at temperature extremes.

2.3 Effects of Temperature and Voltage

The microNode is based largely on Complementary Metal–Oxide–Semiconductor (CMOS) technology. The current drain of CMOS circuitry can vary substantially over Temperature. The RF circuitry and its performance also vary substantially over Temperature.

The microNode utilizes two main power domains when it is functioning:

1. **LDO Regulators that work from 2.2V up to 5.5V.**
   These are enabled when the POWER_ON signal for the microNode is active. These can act as a linear load as voltage increases from minimum to maximum – although these circuits do not normally consume much power.

2. **Switching power domains.**
   When the microNode wakes up to communicate with the Host or for networking events, its switching regulators are enabled. These buck-boost switching regulators supply the 3.3V and other logic supplies over the input range of 2.2-5.5V. The power efficiency of these regulators change dramatically over input voltage, load levels, and temperature. Nominally, the power efficiency is best at 3-4.0V. The efficiency becomes poor below 3.0V and is moderately efficient at the higher input levels.

The following graphs show the relative differences across the operating voltages and their effect on current consumption.

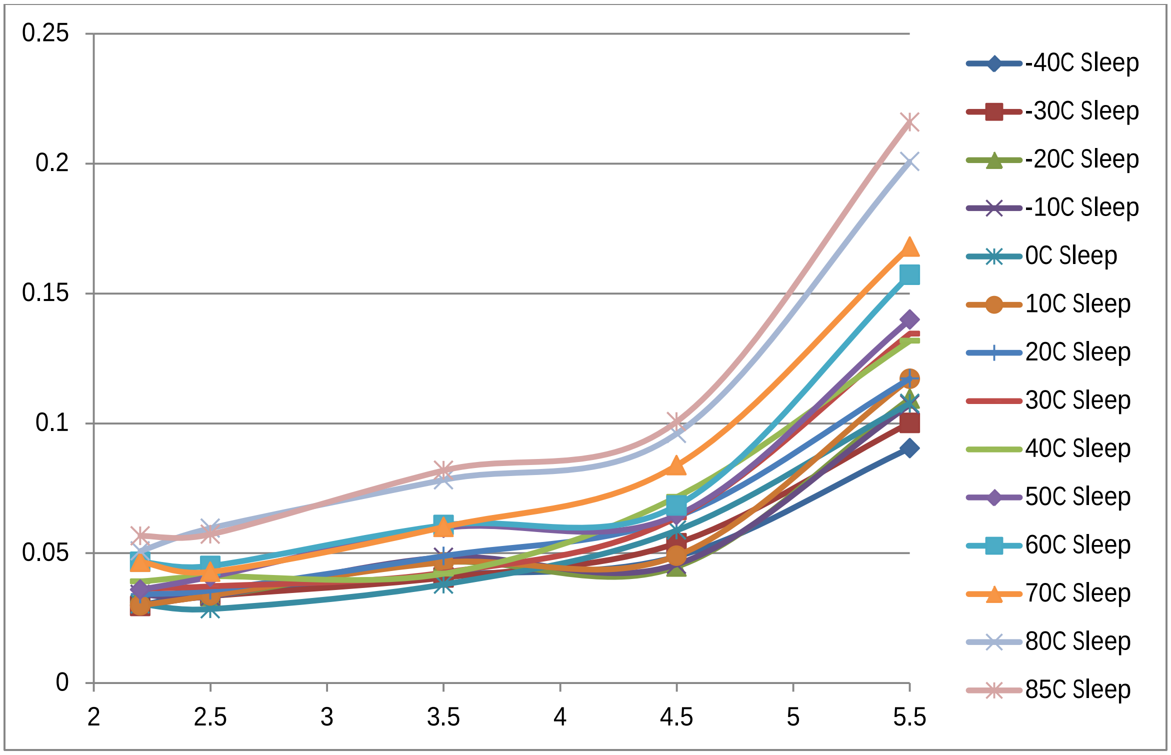


Figure 1. microNode Deep Sleep Power Consumption (mW Power vs VBATT Input)

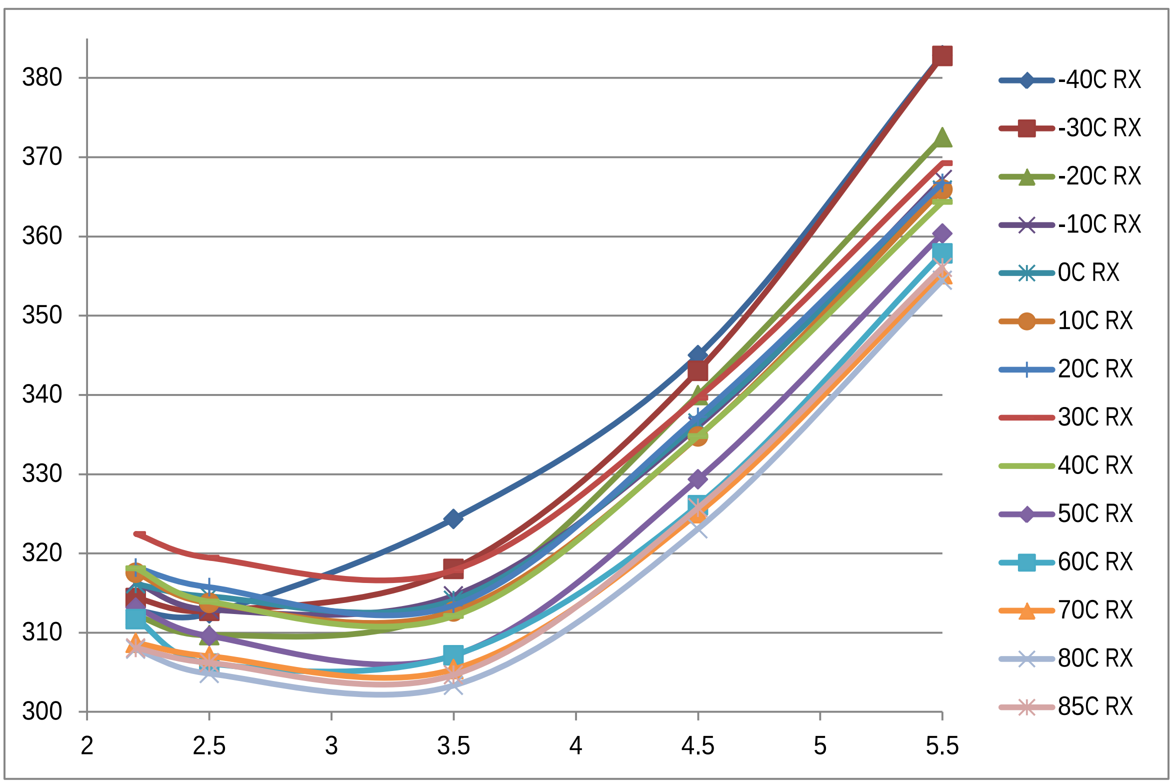


Figure 2. RX State Power Consumption (mW Power vs VBATT Input)

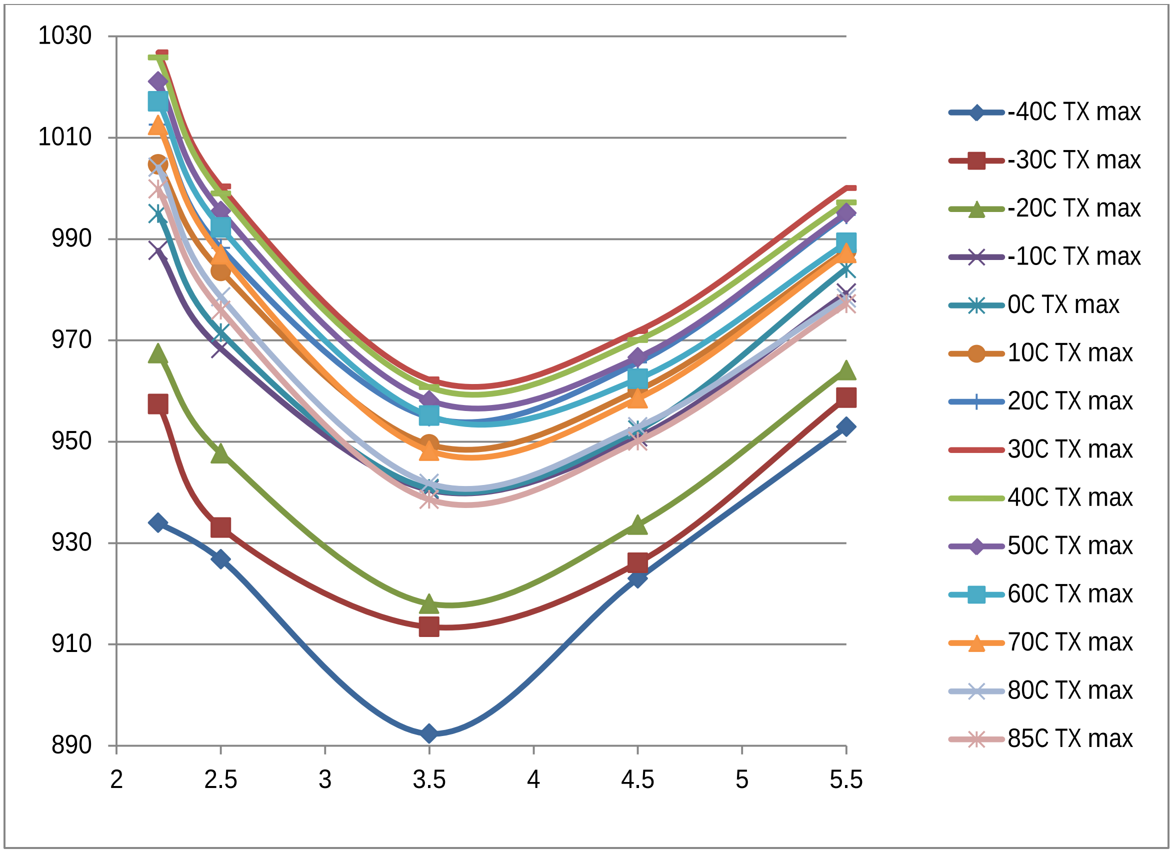


Figure 3. TX Power Consumption at 21.5 dBm (mW Power vs VBATT Input)

3 Electrical Interface

This chapter describes the electrical interface of the microNode and how the Host processor controls the microNode.

Table 4. microNode Pin Descriptions

Pin #	Pin Name	Signal Direction Relative to microNode	Signal Type	Comment
1, 2, 3, 4, 7, 10	Ground	Power	Power	Ground return. Should be low RF impedance to a solid ground plane of the Host
11,14, 17, 20, 21, 26, 30, 31, 34, 35, 37, 38, 40	Ground	Power	Power	
5, 6	VBATT	Power	Power	Input power to the microNode. It is recommended that the Host integrator allow for decoupling of the microNode by placing space for up to a 100 µF ceramic cap. This may or may not be required, depending on the Host's power supply and its impedance.
8	SRQ	Output	CMOS_O	Slave Request
9	SRDY	Output	CMOS_O	Slave Ready
12	SCLK	Input	CMOS_I	SPI Clock
13	MISO	Output	CMOS_O	SPI Master In Slave Output
15	CS	Input	CMOS_I	SPI Chip Select
16	MOSI	Input	CMOS_I	SPI Master Output Slave In
18	MRQ	Input	CMOS_I	Master Request
19	3V3	Output	CMOS_O	3.3V Switcher output
22	RESET_N	Input	OC_1	RESET input
23	USTATUS	I/O	CMOS_O, CMOS_I	USTATUS. To be used by the microNode as a GPIO. Undefined at this time. Float for now.
24	POWER_ON	Input	CMOS_A	This is used to turn ON/OFF the Internal Power supplies of the microNode.
25	ANT_SEL	Output	CMOS_O	This is used by the microNode to control its antennas for diversity.
27	UART_SIN	Input	CMOS_I	UART Serial input. Not supported at this time.

Pin #	Pin Name	Signal Direction Relative to microNode	Signal Type	Comment
28	UART_SOUT	Output	CMOS_O	UART Serial output. Not supported at this time.
29	TOUT	Output	CMOS_O	TOUT is a normally low signal that pulses high in response to specific Network Timing Events
32	RF_PAEN_EXT	Input	CMOS_I	This is used to force the PA off. It is internally pulled low. Do not connect at this time.
33	RF_TXENA	Output	CMOS_O	This signal is used to indicate status of the Power Amplifier for the microNode: Low - OFF, High - Enabled.
36	RF	RF RX/TX	50 Ohm	This is the RF input/output for the microNode. It is a 50 Ohm castellated “pin.”
39	RF_SHDN	RF Shutdown	CMOS_O	This pin indicated the status of the microNode’s RF Transceiver: Low= Shutdown, High = Active

NOTES:

1. The VDD of the internal logic of the microNode is 3.3Volt.
2. The Host is the SPI Master and the microNode is the SPI Slave.
3. OC_1

   The pin-type is unique for the RESET line. Internal to the microNode, this is a simple RC circuit that Resets to GND (0 Volts) and rises to 1.8Volts (maximum). Externally, it is required to drive this pin via an Open Collector (States: Ground=microNode Reset, or float=microNode Active). Most Host CPUs have programmable I/Os that allow setting as an output (low) and as input (tri-state or float). A pull-up is not permitted. Voltages above 1.8V can damage the Reset line of the microNode or place the microNode in a latchup state.
4. CMOS_A
   a. The CMOS_A pin is used to control two Analog Regulators and their Enable pins.
   b. The pin has hysteresis.
      - Going High (Active): V input High is 1.2V
      - Going Low (OFF): V input Low is 0.4V
   c. When the microNode is ON, this pin consumes a nominal 0.2 µA but as maximum of 2 µA over the entire temperature range.

5. VBATT
   a. The microNode operating voltage is 2.2-5.5V, which drives a buck/boost regulator (3.3Volts) internal to the microNode.
   b. The 3.3V regulator drives the RF and PA circuitry of the microNode which also drives its operating CMOS I/O voltages.

3.1 Signal Descriptions

3.1.1 VBATT

This is the main power to the microNode. This needs a low impedance source to the Host's power source. It is recommended that the Host have provision for up to a 100 µF low ESR capacitor. It is likely this capacitor is not required if low impedance design rules are followed.

3.1.2 POWER_ON

This signal controls the power-on of the LDO circuitry for the microNode. It must be shut off prior to starting the microNode power-up sequence as defined in section 4.4: Startup (Power On) Sequence. After the microNode is powered up, this signal is to remain logic high.

3.1.3 RESET_N

The microNode has a basic RC Reset circuit that should be cleared during the startup sequence for the microNode. This signal is an Open Collector style of signal that can be cleared (grounded) for Reset and allowed to float when the microNode is operational. This pin should never be exposed to a voltage greater than 1.8V.

3.1.4 MRQ

The MRQ (Master Request) is the Host's normal way of waking the microNode to initiate SPI communications. Logic "High" forces the microNode awake.

3.1.5 SRDY

SRDY (Slave Ready) is an indication from the microNode that it has fully booted its internal Firmware image, initialized its Hardware and Interfaces, and is ready for communication (arbitration) with the Host. Logic "High" indicates the microNode is ready for communications.

3.1.6 SRQ

The SRQ (Slave Request) signal is an indication from the microNode that it wants the Host's attention. When SRQ is asserted "High," the Host must read the Status registers of microNode. If SRQ is "High," SRDY will also be "High."

3.1.7 USTATUS

USTATUS is currently undefined. In software it can be either an Input or Output. Currently it is configured as an input. The Host should not use this signal.

3.1.8 SPI System

The SPI system is the generic term used for all SPI signals (MOSI, MISO, CS, SCLK) to be set up for SPI communications to occur between Host and microNode.

The microNode SPI is the Slave in the Master/Slave communications and is defined in section 4.2: SPI Mode and Timing.

3.1.9 ANT_SEL

The Antenna Select (microNode output) signal is used to control a RF T/R signal to allow Antenna Diversity. This is more fully defined in Chapter 8: Antenna Diversity.

3.1.10 UART_SIN

This UART_SIN is a microNode UART input signal. It is reserved for future use and should not be used by the Host. Leave unconnected.

3.1.11 UART_SOUT

The UART_SOUT is a UART output signal that is currently reserved. The Host should not use this pin.

3.1.12 TOUT

This signal is a Time Synchronizing signal that pulses high upon specific network timing events.

3.1.13 RF_PAEN_EXT

The RF_PAEN_EXT signal is a direct hardware signal that can be used to disable the Power Amplifier (PA) for the microNode. This signal is pulled low (100k to ground) to allow the PA to work as normal. A microNode external device can temporarily assert this signal high to de-key the PA for the microNode. The purpose of this direct control is to allow simple coexistence algorithms with other RF devices. If the external device is transmitting, its transmitter signal can disable the PA for the microNode thus avoiding a TX collision.

3.1.14 RF_TXENA

This signal is a status output of the microNode that allows other RF devices to monitor when the microNode is transmitting. In a simple RF coexistence scheme, the RF_TXENA can disable a coexisting radio's transmitter, while the microNode is transmitting. The RF_TXENA signal goes active high when transmitting.

3.1.15 RF_SHDN

This microNode output indicates status of the microNode's RF Transceiver. If low, the transceiver sleeps (no RX and no TX). Using RF_SHDN and RF_TXENA in combination, co-existing RF devices can determine the absolute state of the RF Transceiver of the microNode.

3.1.16 RF

This is the RF port (TX and RX) for the microNode. It is a nominal 50 Ohm port. For best results ensure the load termination (antenna) has a VSWR of 1.5:1 or better (return loss < -14 dB).

3.2 Environmental

3.2.1 ESD

The microNode is designed to be a truly embedded module and can almost be considered an IC. The microNode is to be placed as a direct-connect to the Host CPU. Therefore, the microNode has inherent minimal electrostatic discharge (ESD) protection on its I/O.

Table 5. ESD Information

ESD Model	Class and Minimum Voltage
HBM	Class 1C (>1000V)
MM	Class A (>100V)

The RF port does have some protection in the form of an inductor to ground, thus allowing some robustness to direct ESD strikes.

If the application is intended for harsh ESD or lightning strike scenarios it is recommended that the Integrator take extra precautions to guard against accidental resets or ESD damage.

3.2.2 Harsh Environments

The microNode employs miniature surface-mounted components in its assembly. If the target design is intended for high humidity or salt environments and intended to have a long service life, it is recommended that the designer take necessary precautions to guard against prolonged exposure to moisture and other contaminants. A sealed enclosure (IP68) or potting may be required in extreme environments.

4 SPI Interface and Sequences

4.1 SPI System Interface Overview

The SPI slave interface is currently the only supported interface for Host-to-Node communication.

NOTE: The microNode must be the only SPI slave on the bus.

The SPI slave interface provides communication with an external Host through a 7-wire interface. The Host is the SPI master and the microNode is the SPI slave. In addition to the four standard SPI signals, three additional signals are used to complement the SPI bus: MRQ, SRQ, and SRDY. The additional signals are included to support microNode state transitions and bi-directional message traffic.

The SPI signals include four that are controlled by the master and three that are controlled by the slave.

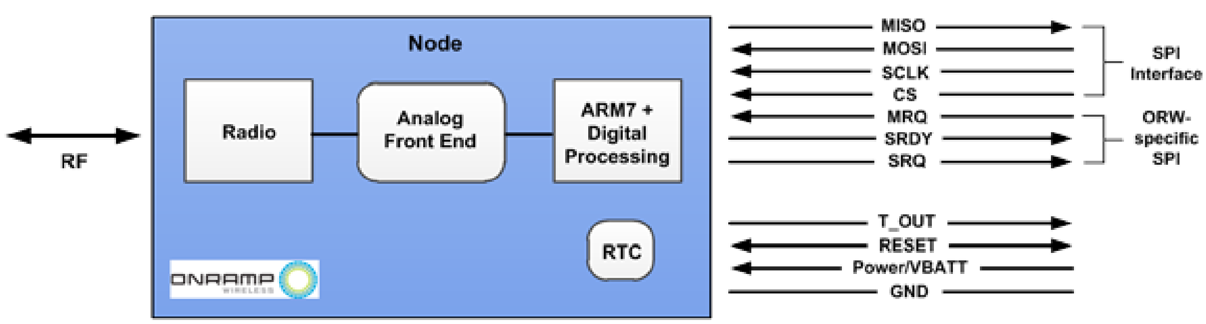
Master-controlled Signals

- MOSI
- SCLK
- CS
- MRQ

Slave-controlled Signals

- MISO
- SRQ
- SRDY

When MRQ and SRQ are low, the remaining master controlled signals (MOSI, SCLK, and CS) must be held low or tri-stated. This is to prevent these signals from back-driving the microNode slave that may be in deep sleep. When either MRQ or SRQ assert high, the master should set each of the three signals appropriately according to their standard usage. No pull-up resistors should ever be applied to any signals on the microNode.



4.2 SPI Mode and Timing

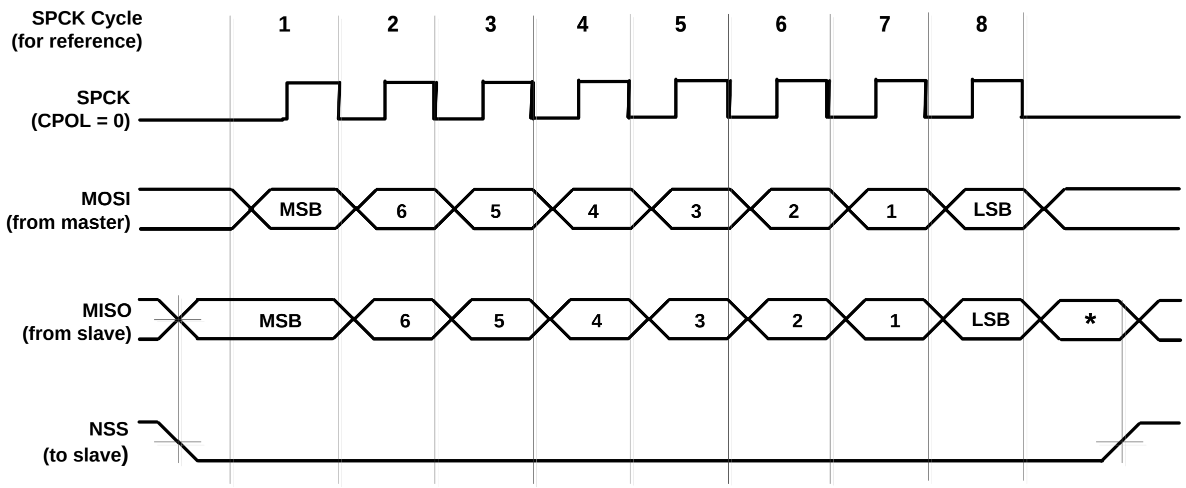


Figure 4. SPI Timing, CPOL = 0, CPHA = 0

4.3 Host Initialization

What is described here is the initialization of the Host, its operating software, and the control sequences used to drive the microNode.

Due to specific clock and memory requirements, the microNode must go through specific Initialization and Wake sequences.

NOTE: Some CPUs have internal pull-up resistors that are active after Power On Reset. Through CMOS leakage, the Host CPU can supply voltages to the microNode I/O bus prior to the Host CPU fully initializing and disabling the pull-up resistors. It must be noted that during the brief initialization period, the POWER_ON signal must be "low." Activating the POWER_ON signal with other microNode signals being pulled "high" can cause CMOS latchup within the microNode.

4.4 Startup (Power On) Sequence

During, and immediately after Power On Reset (POR), the Host has no control of its I/O power states. For instance, some CPUs have GPIO that tri-state or act as inputs during power up. Other CPU brands have programmable pull-ups on its I/O and need the Host CPU to disable those pull-ups for the Host's GPIO to work correctly with the microNode. This setup and configuration of GPIO takes a finite time during the Host boot process. This is detailed in the following figure.

Whereas the power-up sequence is described here, it is recommended the Integrator not attempt this entire startup sequence without assistance. On-Ramp Wireless offers a formal and controlled library to help with this startup and communication interface called UNIL. This is fully documented and released by On-Ramp Wireless. The UNIL tracks all details of the lower (physical) and higher (messages) layers of the Host-Node communications. For more information on UNIL see the documents referenced in chapter 1 at the beginning of this document.

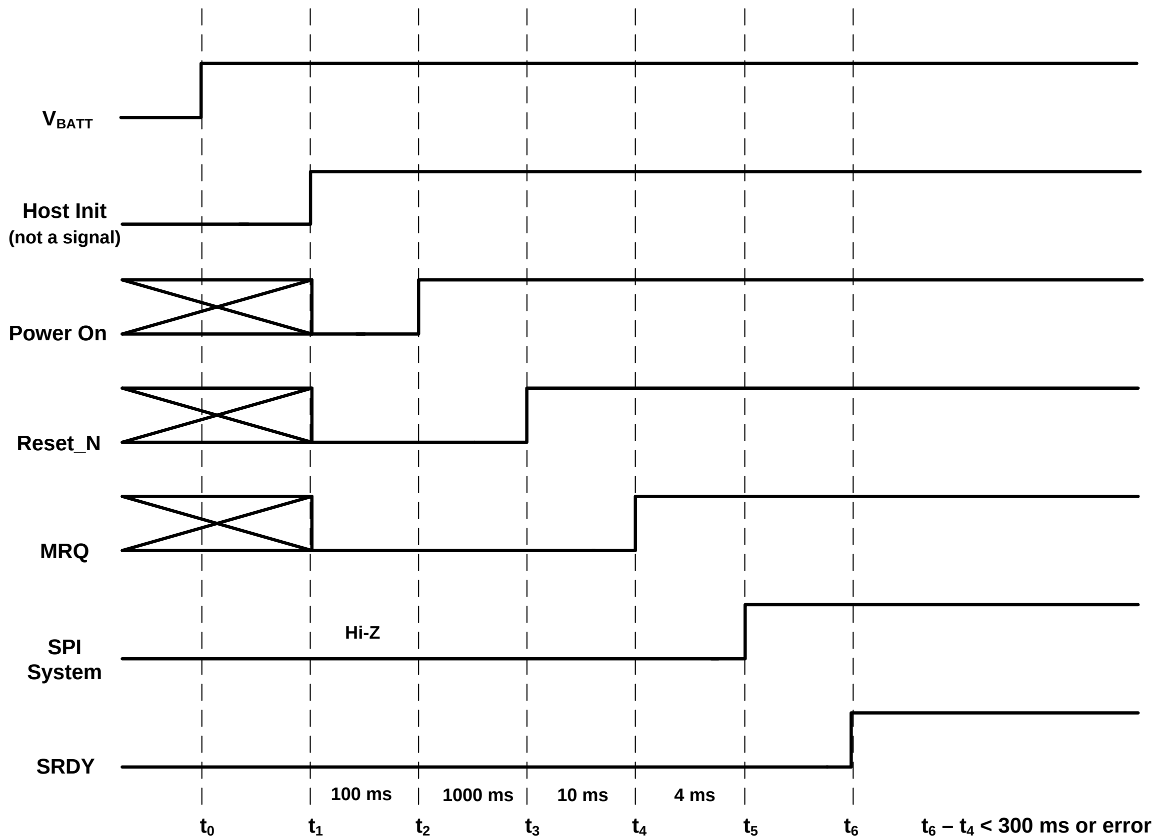


Figure 5. microNode Powerup Timing Sequence

The timing sequence shown in Figure 5 above is described below.

- **t0 à t1** This phase is where the Host's System power has been applied and the Host Software must power up and initialize the GPIO interfaces for the microNode to the required states defined at time t1. The t1 state becomes "TRUE" indicating the Host sets all the GPIO to a known and controlled state (Low).
- **t2** At t2 state, all the output signals to the microNode are set low and the Power On Signal is set high. This turns on the internal LDO regulators of the microNode to initiate a power up sequence. The time between t1-t2 is approximately 100 ms, or longer.
- **t3** t3 is when the Host releases the microNode from its Reset state. This time allows the microNode's 32 kHz to turn on and stabilize. The time between t2-t3 is 1 second, or longer.
- **t4** t4 signals the start of the Host wanting to initiate communications (arbitration) with the microNode. The Host raises MRQ to turn on various circuitry. The time between t3-t4 is 10 ms, or longer.

- **t5** After the assertion of t4, the microNode begins its "Wake sequence." The microNode must boot, initialize its operating system and hardware and when it is ready for communications it raises its SRDY signal back to the Host. At this point, communications (Arbitration) can begin.
- **t6** At this point the microNode signals its readiness by asserting the SRDY pin. The Host can now begin communications with the microNode.

4.5 Wake Sequence

The microNode can be awakened in two manners:

- MRQ assertion from the Host. The Host desires communications with the microNode and awakens the microNode by asserting the MRQ line. This is a Synchronous Wake Sequence.
- The microNode can "self-awaken" due to network events. In this case, a timer internal to the microNode "pops" and triggers the microNode to "Wake." When the microNode is awake it asserts its SRDY as a matter of course to indicate to the Host (if it needs to) that it can start communicating with the microNode while it is awake. This is an Asynchronous Wake Sequence.

4.5.1 Wake Sequence (Synchronous)

The following sequence demonstrates the timing required of the Host to awaken the microNode from a sleep state.

Assumptions:

- The microNode has been previously Powered On and Arbitrated.
- The power (VBATT) has remained stable and the microNode has not been Reset (Reset is set to tri-state/float).

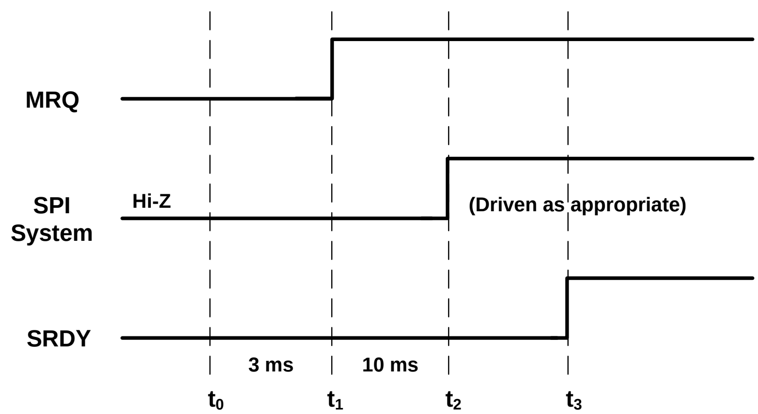


Figure 6. Host-Initiated microNode Wake Sequence – SRDY Low (Synchronous)

The timing sequence shown in Figure 6 above is described below.

- **t0** The Host desires to Wake the microNode and asserts MRQ high.
- **t0 à t1** After MRQ has gone High, the Host's SPI system and other I/O can be enabled. Asserting the MRQ has enabled the internal I/O power supply of the microNode and the Host's SPI can be enabled 4 ms after the rise of MRQ.
- **t1 à t2** After the initial assertion of MRQ, the microNode has to internally power up and initialize its systems. When it is ready to communicate it will assert its SRDY line to signal it is now ready for SPI interaction. From MRQ assertion until the microNode is ready, takes about 80 ms.
- **t3** The microNode is now ready to communicate with the Host.

4.5.2 Wake Sequence (Asynchronous)

In this scenario, the microNode is already awake due to a networking event (SRDY is already High) and the Host wants to communicate with the microNode while it is awake. The Host asserts MRQ to ensure that the microNode stays awake during its communication cycle.

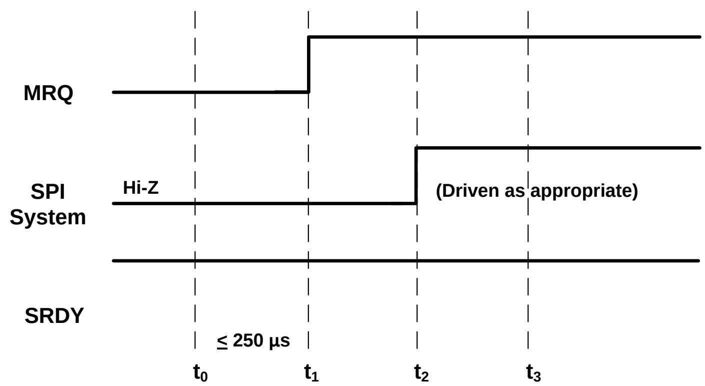


Figure 7. Host-Initiated microNode Wake Sequence – SRDY High (Asynchronous)

4.6 Host-Driven Reset Sequence

If the microNode fails to communicate (or similar), it may be necessary to Reset the microNode. The following figure shows the proper sequence to reset the device.

NOTE: Resetting the device causes it to go through a Cold Acquisition process to reacquire the network.

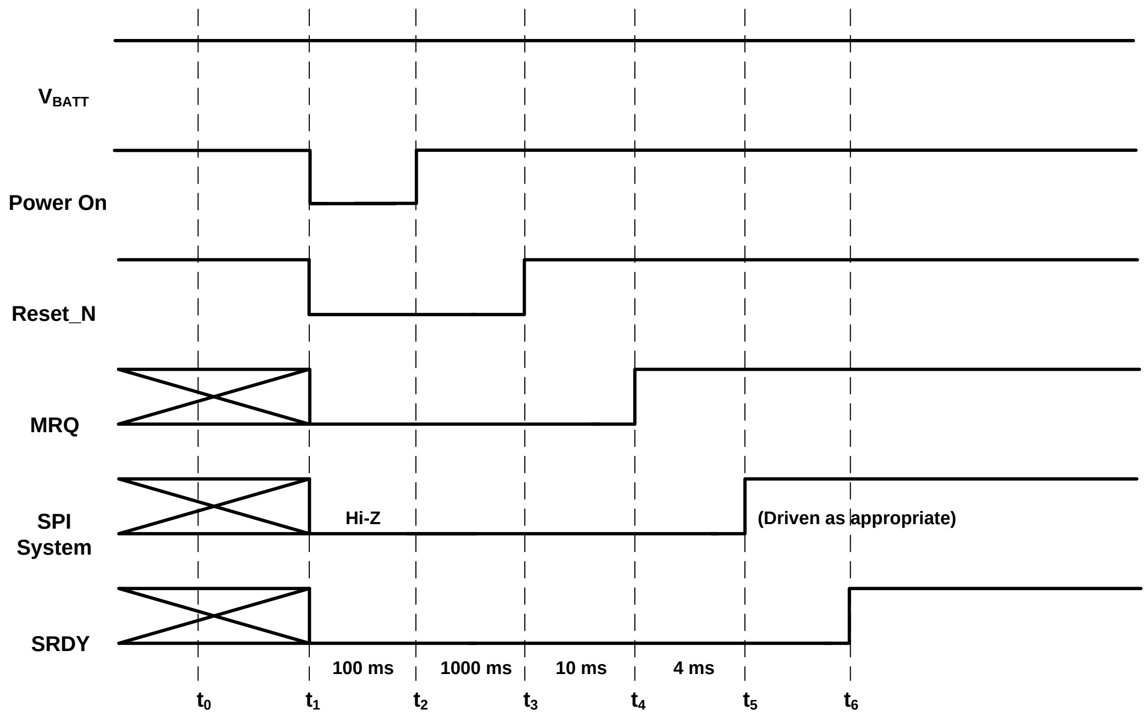


Figure 8. Host-Driven Reset Sequence

4.7 Host MRQ Release/microNode Allowed to Sleep Sequence

If the Host determines there are no more messages or SPI transactions required, it nominally de-asserts the MRQ to allow the microNode to fall back to Deep Sleep (lowest power mode). The figure below shows how this is sequenced by the Host/microNode. A small delay in de-asserting SRDY is enforced to prevent quick toggling (Waking) of the microNode.

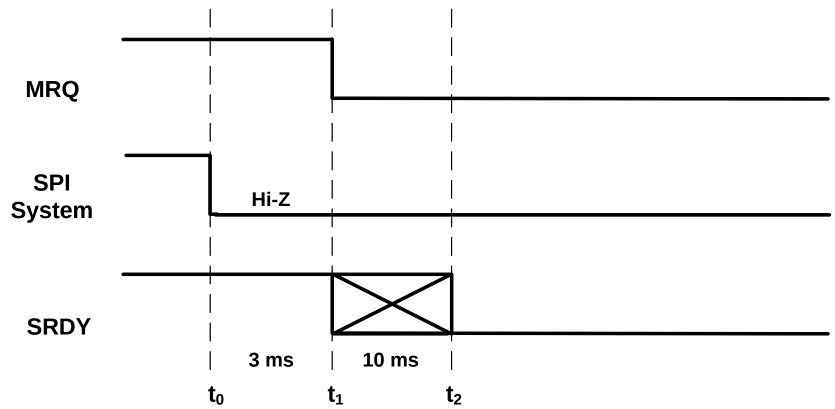


Figure 9. Host MRQ Release/microNode Allowed to Sleep Sequence

5 Power States

The microNode has a number of states it runs through during its various operating modes.

General comments:

1. The microNode accepts a wide input voltage range (2.2-5.5V).
2. The microNode has low drop out (LDO) regulators that will operate 100% of the time the microNode is powered (POWER_ON signal set high).
3. There are 3.3V/1.2V Buck/Boost Switching regulators that use the wide input range to drive key RF and Digital circuits. The 3.3V regulator is only turned on in certain active operating states of the microNode.

The microNode tries to minimize its power consumption but is largely driven by network operating states and ULP modes of operation. This document does not describe all of the modes in detail but, in general, there are two main operating modes for the microNode:

- **Continuous Mode**
  In this mode, the microNode is ON (awake) at least 50% of the time (100% of its RX cycle). The microNode starts up, searches for the network, locks on, and Joins. In this mode, the microNode nominally is either in RX or TX modes (radio is ON and in a high power consumption state), or in an Idle state where the clocks and CPU are ON but the radio is OFF (moderately low power mode). The continuous mode is usually for applications where the Host and microNode are AC-powered and system current consumption is not an issue.
- **Slotted Mode**
  This mode has the microNode falling into a Deep Sleep state – the lowest power state of the microNode. In this mode, the microNode is mostly powered down – except for a couple of low power LDO Regulators. The microNode can sleep for hours at a time if the network is configured to allow this.

The power states are described in the following sections.

5.1 Operating States

This section describes the various operating states within the operational modes.

5.1.1 Power Off State

When the microNode is totally non-functional, the Host can set the POWER_ON signal Low to deactivate the circuitry of the microNode. This should NOT be confused with Deep Sleep states where the microNode mostly sleeps yet maintains key network timers to wake up synchronously with network activity. If awakened from the Power Off state, the microNode must go through a very power-hungry search/acquisition algorithm to re-acquire the ULP network.

5.1.2 Deep Sleep State

The microNode shuts off all its power regulators except a couple low quiescent LDO regulators. These regulators keep a minimal amount of circuitry alive for tracking network timers, enable a 32 kHz clock, and some minor interface circuitry.

5.1.3 Oscillator Calibration State

When the microNode is in Deep Sleep state, it attempts to maintain accuracy of its low power 32 kHz clock to enable faster network synchronizing when it wakes up. The CPU of the microNode is not activated during this calibration state. The microNode will periodically, and briefly, Wake in a very low power mode to calibrate its 32 kHz clock to its very accurate 26 MHz clock. This is especially important when the temperature varies substantially causing the 32 kHz oscillator to drift. This is illustrated in the following figure.

This plot is an example of the microNode performing a self-calibration of its 32 kHz oscillator. The pulses represent the TCXO being turned on periodically to perform the calibration. The microNode Wakes itself from Deep Sleep, Calibrates, and then falls back to sleep. Minimal power is consumed during this self-calibration process. As can be seen, the microNode does this approximately every 900 seconds.

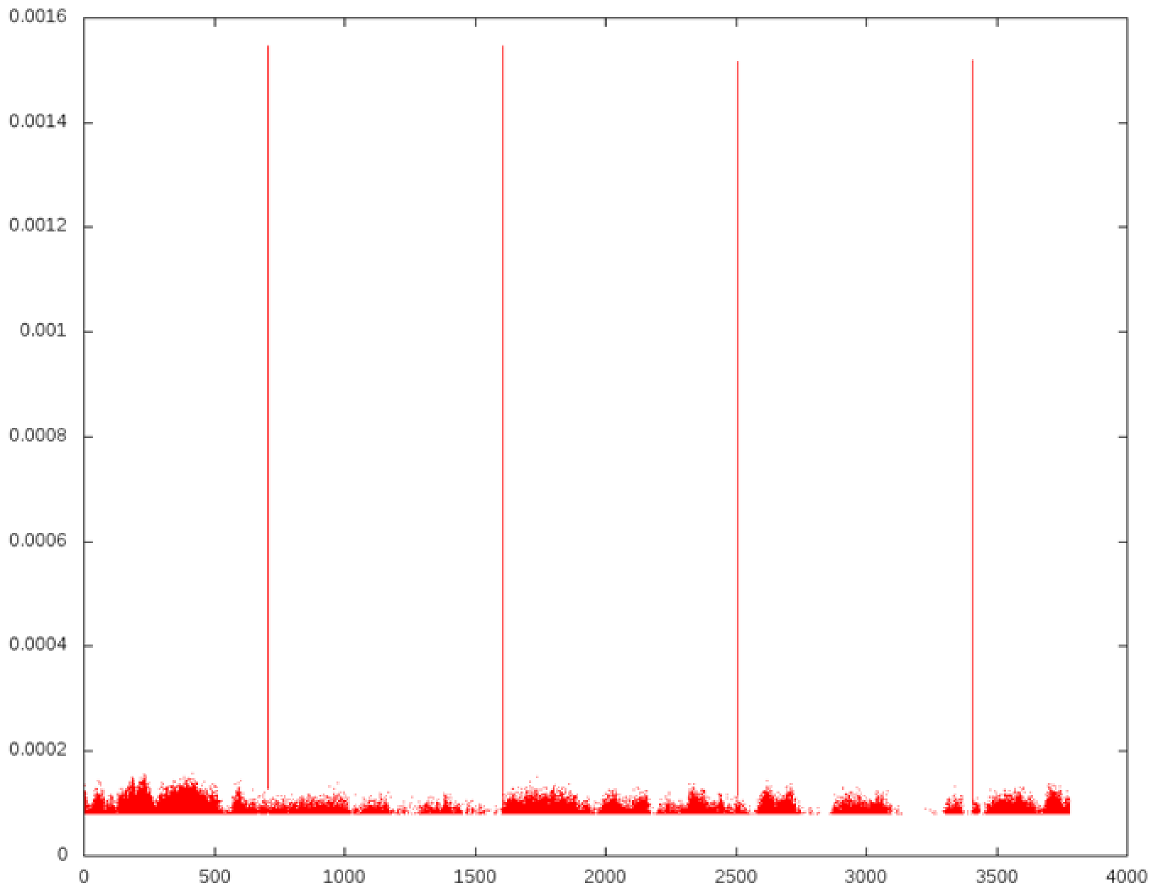


Figure 10. microNode Oscillator Calibration: Current (Amps) vs Time (Seconds)

5.1.4 Idle State

Idle state has various sub-states but generally refers to a state where the microNode is "awake" and its system clock is on, the CPU is awake, but the RF is OFF.

5.1.5 RX State

The microNode turns on all its clocks, the main CPU and the RF in an RX-only state. The RF transceiver, in RX state, consumes a moderate amount of power.

5.1.6 TX State

When the microNode transmits, it uses a variable transmit power that is correlated to its received RSSI. In this state, the microNode is likely at its highest power states, but this is somewhat dependent on RSSI. The worst case state (maximum power) is shown in Figure 11. This is at approximately 21.5 dBm output power. This is the microNode's highest power state.

5.2 System

As noted, the microNode can go through various states of Deep Sleep, Idle, RX, and TX. The plot shown in the following figure provides a representative microNode waking up and going through these states and transitions.

All ULPs are different and current consumption is affected by many factors.

- Network coverage. How much TX power does a microNode need to transmit its data?
- Temperature range
- Operating Voltage
- Continuous mode vs Slotted mode: What is the Uplink Interval?
- Amount of data in the data model
- Quality of Service (QoS) for data delivery

All of the factors indicated above must be examined carefully and plotted to understand the end result in current profiles and expected battery life projections.

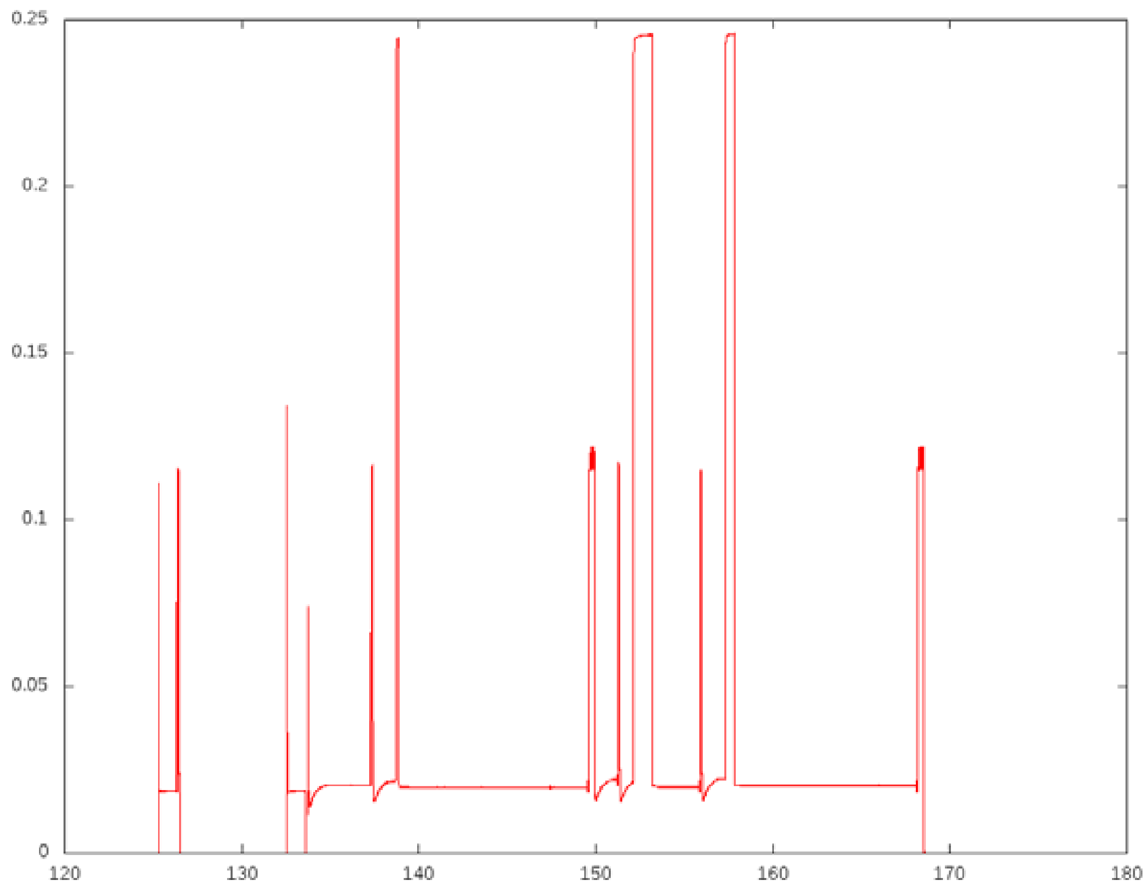


Figure 11. Representative Current Consumption During Sleep, Idle, RX, and TX; x16 Spreading Factor (Amps vs Seconds)

The plot shown in the figure above represents the nominal transitions for the microNode from Deep Sleep, Idle, and Transmit states. In this case, a TX spreading factor of 16 is used. It is important that the Host designer understand the System operating profile, operating voltages, different operating modes of the microNode and the ultimate effect on System power consumption. Of course, this is especially true if a battery powered device is being considered.

6 Messaging Protocol

The details of Host/Node messaging are typically not necessary for integrators to implement, given the functional interface provided by the *ULP Node Interface Library (UNIL) (010-0066-00)* and *UNIL API (010-0072-00)*. However, low-level understanding of the SPI protocol used may be critical in resolving Host interface issues.

For mid-level details of the messages that may be sent over this interface, refer to *ULP Node Host Message Specification (014-0020-00)*.

6.1 Arbitration

Arbitration is the process a Host uses to signal to the Node that it supports the On-Ramp Wireless bi-directional messaging protocol. The arbitration sequence is designed to reduce the probability that an arbitrary non-Host transfer sequence can mirror a valid arbitration sequence.

Arbitration consists of both Host and Node transmitting an arbitration request/reply pair. After a defined turn-around delay, both transmit a validation request/reply. The turn-around delay avoids race conditions between Host and Node and provides enough time to allow ISR execution to complete before the next SPI transfer.

If the Node does not reply to the Host request, the Host needs to wait for a turn-around delay and retry the arbitration request.

The Host must perform the arbitration sequence before any other SPI Bus communication can take place between the Host and the Node.

The Host must initiate this arbitration sequence on boot up. Additionally, the Host must perform the arbitration sequence when the Node sends to the Host an arbitration message. This can occur due to the Node going into Deep Sleep and then waking up. Since the Node requires the arbitration sequence after waking from Deep Sleep and since the Host is not aware of when the Node goes to Deep Sleep, the Host must be able to detect that the Node is requesting arbitration and the Host must then reset its Host interface state machine and perform arbitration. For more information on the Host interface SPI bus state machine, refer to section 6.3: Host Interface SPI Bus State Machine.

6.2 Message Protocol

Host-to-Node transfers use master message command pairs and Node-to-Host transfers use slave message command pairs. Both transfers use identical command sequences with only the encoding of the commands differing. The command sequence for a message transfer consists of a request/acknowledgement pair followed by a defined turn-around delay and then a message composed of a header pair and a payload.

Variable length payloads are supported by encoding the payload size in the second half of the message request. The second half of the message reply contains the available receive buffer size. If the message payload size exceeds the receive buffer size, then a new request must be made after a turn-around delay with a payload size that does not exceed the receive buffer size.

After a successful message request transfer, the Host waits a turn-around delay and then initiates the transfer with a message header command. The payload immediately follows the header and, if necessary, is zero padded to match the payload size indicated in the message request.

After the payload, the Host waits a turn-around delay before proceeding with any other further messages.

The Host interface SPI bus is a standard SPI bus (with MISO, MOSI, CS, and SCLK) with the addition of three lines (MRQ, SRQ, and SRDY). These three additional lines are used to provide the Host with the ability to wake up the Node over the SPI Bus as well as providing the Node with the ability to prompt the Host to begin a SPI Bus transaction. The Node is also exceptional in that it must be the only slave present on the SPI Bus, since MOSI, CS, and SCLK must be undriven (tri-stated) any time that MRQ is low.

Before any message is communicated over the SPI Bus, the MRQ and SRDY lines must be high. The Host guarantees this by pulling the MRQ line high and waiting for the Node to pull the SRDY line high. The Host cannot proceed with SPI Bus communication until both of these lines are high. Once MRQ and SRDY are high, the Host, being SPI Bus master, can continue with a normal SPI Bus transaction.

When the Node wishes to communicate with the Host, it pulls the SRQ line high. The Host must have the ability to detect this and start a SPI Bus transaction (by first pulling the MRQ high and waiting for SRDY to go high). A standard SPI Bus transaction is described and illustrated in Figure 14.

Message exchanges between Host and Node are shown below in Figure 12.

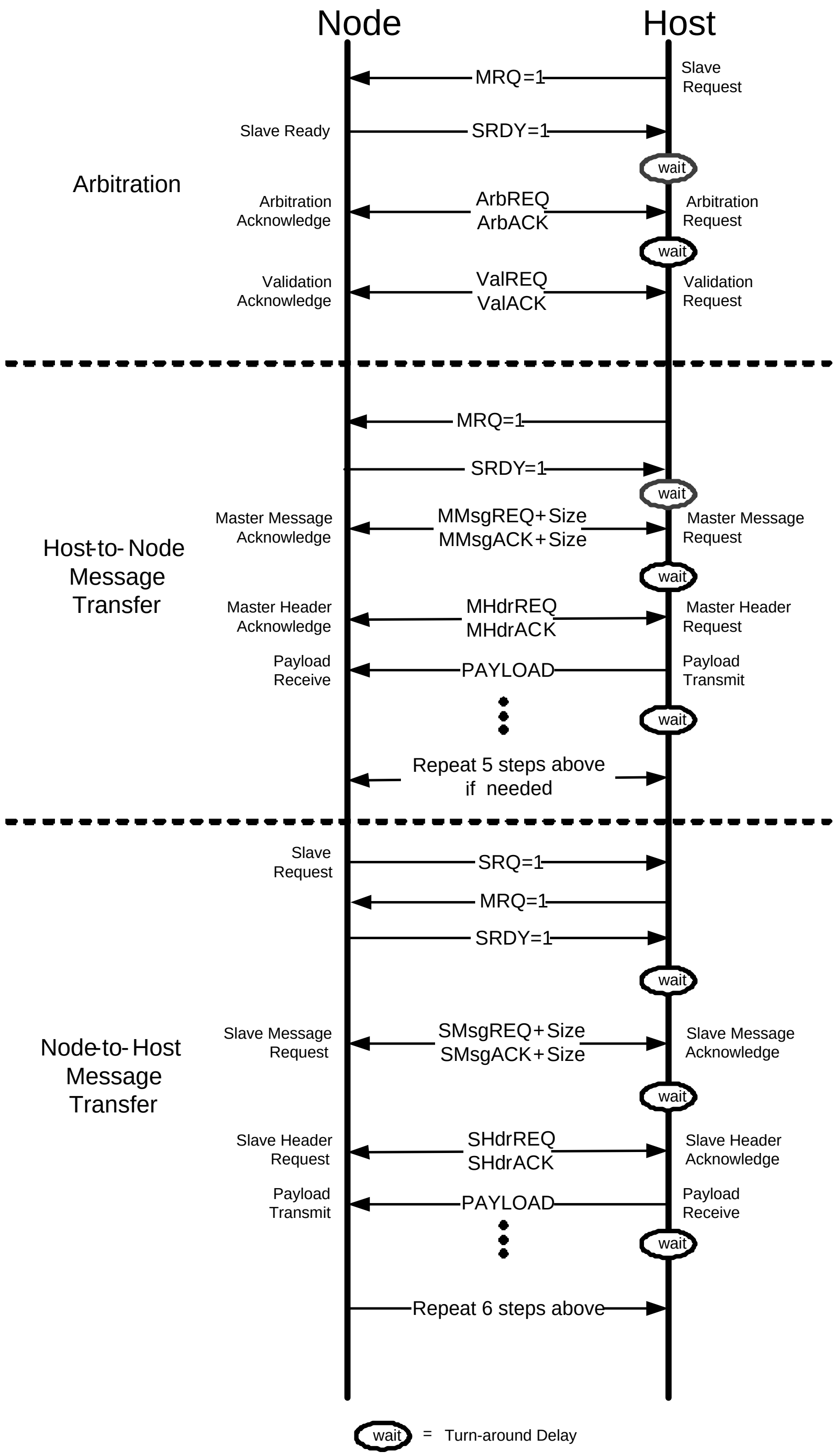


Figure 12. SPI Master and Slave Message Sequences

In each of the request/acknowledge command pairs shown, the top command is transmitted by the Host (master) and the bottom command is transmitted by the Node (slave). The wait bubbles indicate a predefined turn-around delay which provides ISR processing time and avoids race conditions between Host and Node.

6.3 Host Interface SPI Bus State Machine

This section illustrates the sequence of messages that can take place on the Host interface SPI bus. The design and implementation of the actual state machine on the Host software is up to the Host software designer. This diagram is provided to demonstrate the message sequence over the SPI Bus. Note the usage of the turn-around delay, which is required in between each step of message exchange. This delay is required by the Node and is currently defined as having a time of 200 µs.

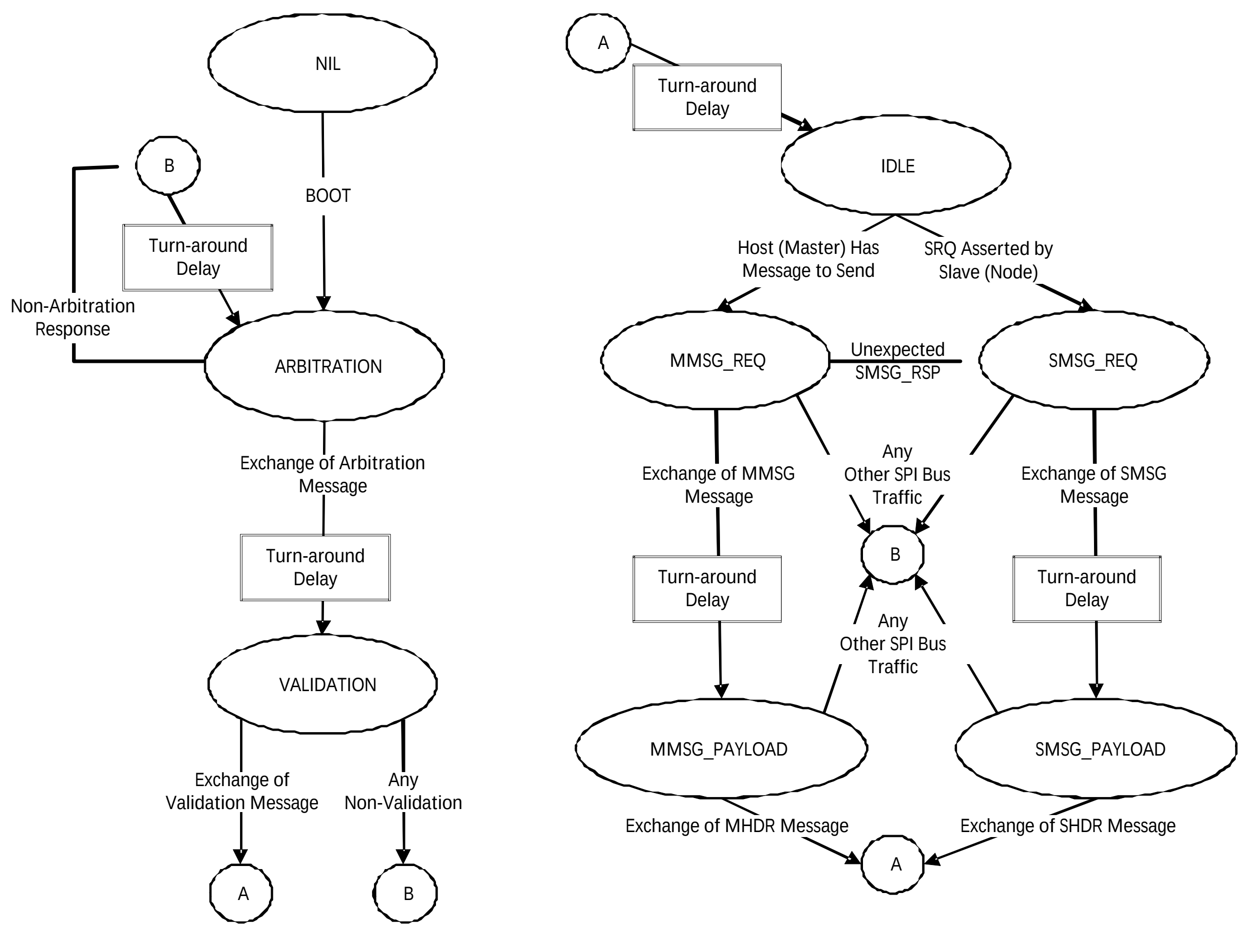


Figure 13. Host Interface SPI Bus State Machine

6.4 SPI Bus Timing Example

This section provides an example illustration of an exchange of messages first from master (Host) to slave (Node) and then from slave (Node) to master (Host). Each step in the timing sequence is described below:

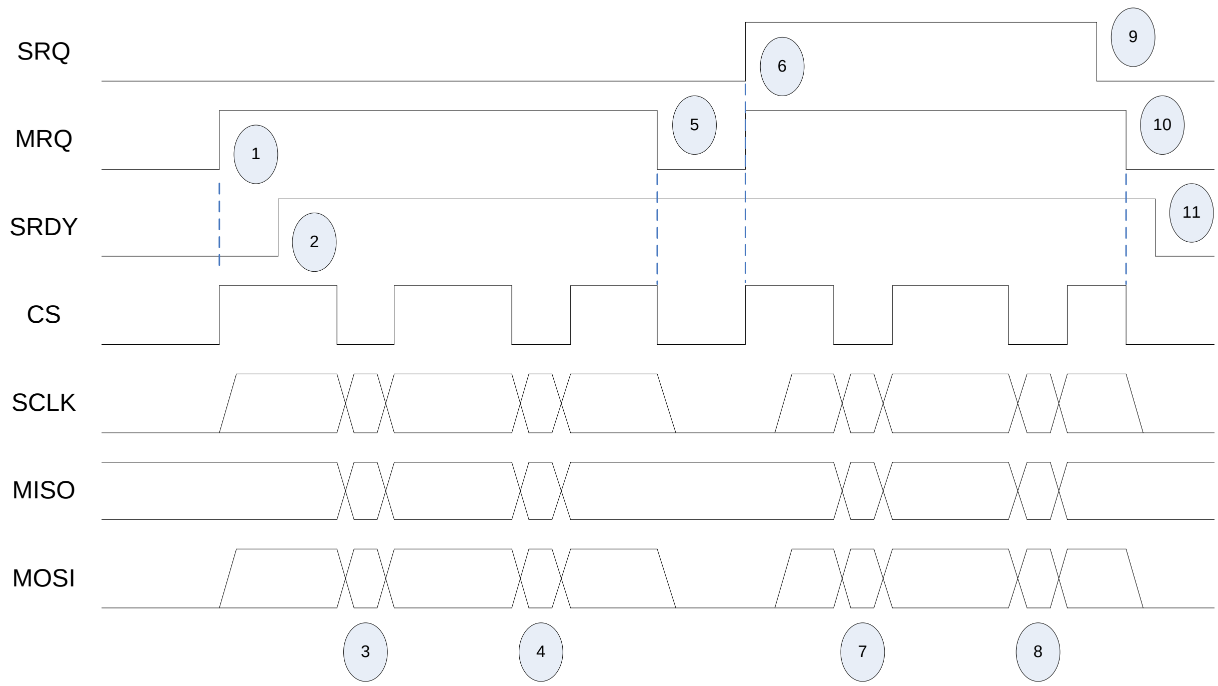


Figure 14. SPI Timing Example

Note that MRQ state transitions must respect the timing requirements shown in Figure 6, Figure 7, and Figure 9.

The following items pertain to the numbered bubbles above:

1. Host has a message that it desires to send to Node. The first thing that it does is drive MRQ and CS high.
2. The Host then waits for the Node to drive SRDY high. No SPI bus transaction with the Node can occur before this.
3. After SRDY is high, the Host can start with the SPI data transaction. This is accomplished by driving the Node CS line low and then having the Host toggle the SCLK, and MOSI lines and having the Node toggle the MISO line according to the data to be transferred. The SPI Host interface specifies that first a MMsg pair is exchanged.
4. A MHdr pair is exchanged. Note that the payload of the message is appended to the MHdr.
5. The Host detects that the transaction is complete and that it does not wish to send more messages to the Node at this time. It drives the MRQ line low. Since MRQ is low, CS, SCLK and MOSI are tri-stated.

6. At some time in the future, the Node desires to send a message to the Host. It indicates this to the Host by driving SRQ high. Since SRQ is high, the Host drives MRQ and then CS high. It then waits for SRDY to go high, which it already is.
7. The Host starts the SPI data transaction. This is accomplished by driving the Node CS line low and then having the Host toggle the SCLK, and MOSI lines and having the Node toggle the MISO line according to the data to be transferred. The SPI Host interface specifies that first a SMsg pair is exchanged.
8. A SHdr pair is exchanged. Note that the payload of the message is appended to the SHdr.
9. The Node detects that the transaction is complete and that it does not wish to send more messages to the Host at this time. It drives the SRQ line low.
10. The Host detects that SRQ has gone low and that it does not have any messages to send to the Node. It drives the MRQ line low. Since MRQ is low, CS, SCLK and MOSI are tri-stated.
11. The Node drives the SRDY line low after MRQ goes low.

6.5 Host Message SPI Example

This section provides an example Host message exchange from master (Host) to slave (Node). In this example, the Host is sending a version request message.

This example is a zoomed-in view of the example provided previously in Figure 14. This section covers what happens in step 3, which includes the two SPI exchanges initiated by the Host.

With any SPI Host interface message, first an MMsg or SMsg pair must be exchanged. This pair contains information on how big the message is (from the message originator) and how much message queue space is available (on the message destination).

The following diagram shows such an example:

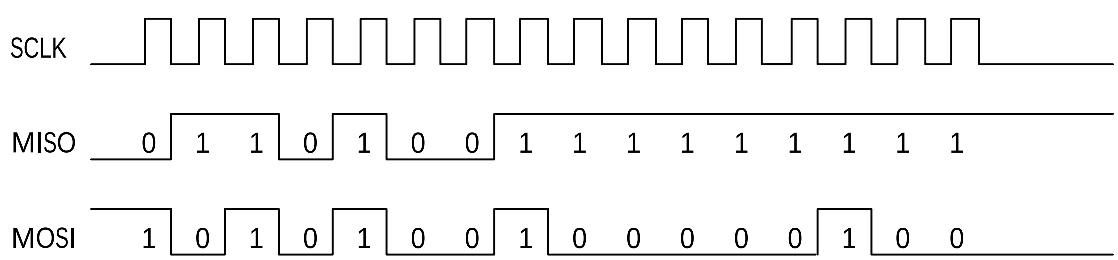


Figure 15. Host Message on SPI – MMsg Pair

The SPI clock edging is configurable with a polarity and phase. In order to communicate with the Node, the SPI clock polarity must be set to "the inactive state value of SPI clock is logic level zero" and the SPI clock phase must be set to "data is captured on the leading edge of SPI clock and changed on the following edge of SPI clock." This means that the data lines (both MISO and

MOSI) are read on the SCLK rising edge and are set or cleared on the SCLK falling edge, and is commonly referred to as CPOL=0, CPHA=0.

This illustration shows that the bit streams for MISO and MOSI are:

- MISO: 0110100111111111
- MOSI: 1010100100000100

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MMsgACK (1001)

buffer size=255 (11111111)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MMsgREQ (1001)

payload size=4 (00000100)

An MMsg pair or SMsg pair is immediately followed by the corresponding MHdr pair or SHdr pair. This is illustrated below:

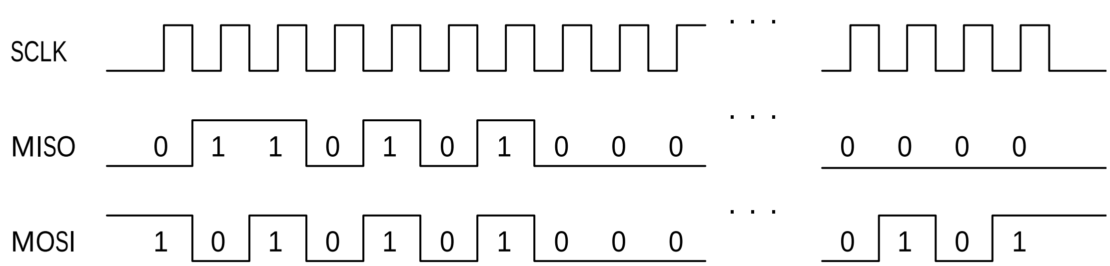


Figure 16. Host Message on SPI – MHdr Pair

For purpose of brevity, this timing diagram shows only a portion of the data exchange. The complete bit streams for MISO and MOSI are as follows:

- MISO: 011010100000000100000000000000000000000000000000000000000000000000 000000000000
- MOSI: 10101010000000010000100000000000000101010100000011110000111100001010 010110100101

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MHdrACK (1010)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MhdrREQ (1010)

Hard coded byte=1 (00000001)

Payload:

length=8 (0000100000000000)

message type=VERSION (0001010101000000)

trailing sequence (11110000111100001010010110100101)

- The payload is Little Endian. The least significant byte is transmitted over SPI first.
- All MHdr and SHdr payloads are terminated by the fixed trailing sequence 11110000111100001010010110100101.
- The example above shows a message going from master to slave, thereby having a payload in the master to slave direction appended at the end of the MhdrREQ and no payload appended at the end of the MhdrACK.

6.6 Host Message “Connect” SPI Example

This section provides an example Host message exchange of the CONNECT message from master/Host to slave/Node and subsequent response from the slave to the master.

The timing is similar to the timing illustrated in the previous section, but the data and length of data is different.

The steps involved in this exchange are as follows:

The Host desires to send the CONNECT message to the Node. As described in the previous section, this starts with an MmsgREQ/MmsgACK exchange over the SPI bus.

- MISO: 0110100111111111
- MOSI: 1010100100000110

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MMsgACK (1001)

buffer size=255 (11111111)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MmsgREQ (1001)

payload size=6 (00000110)

The MMsg exchange is followed by the MHdr exchange, which includes the payload of the CONNECT message.

- MISO: 011010100000000100000000000000000000000000000000000000000000000000000 0000000000000000000000000000000000000000000
- MOSI: 101010100000000100001100000000000011001001000000000000010000000000000 0000000000011110000111100001010010110100101

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=MHdrACK (1010)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =MhdrREQ (1010)

Hard coded byte=1 (00000001)

Payload:

length=12 (0000110000000000)

message type=CONNECT (0011001001000000)

host interface=True (00000001000000000000000000000000)

trailing sequence (11110000111100001010010110100101)

The payload of the message includes first the length, which is the number of bytes in the payload including the length and the trailing sequence.

It is followed by the message type, which in this case is 0x4032, and corresponds with CONNECT.

The CONNECT message has a 4-byte field that is a Boolean flag specifying whether or not the Node should send asynchronous SPI messages to the Host. To specify that the Node should send messages to the Host, the value of 0x00000001 is used.

It is then followed by the standard fixed trailing sequence.

This message exchange is followed by a Node-initiated message exchange for the purpose of sending an ACK of the CONNECT message to the Host. This starts with a SmsgREQ/SMsgACK exchange over the SPI bus.

- MISO: 0110101100000100
- MOSI: 1010101111111111

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=SMsgACK (1011)

buffer size=255 (11111111)

payload size=4 (00000100)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =SmsgREQ (1011)

buffer size=255 (11111111)

The SMsg exchange is followed by the SHdr exchange, which includes the payload of the ACK message.

- MISO: 01101100000000010000100000000000001100000000000011110000111100001010 010110100101
- MOSI: 10101100000000010000000000000000000000000000000000000000000000000000 000000000000

These bits indicate:

MISO: from slave to master (01)

length of message=2 (10)

opcode=SHdrACK (1100)

Hard coded byte=1 (00000001)

Payload:

length=8 (0000100000000000)

message type=ACK (0011000000000000)

trailing sequence (11110000111100001010010110100101)

MOSI: from master to slave (10)

length of message=2 (10)

opcode =ShdrREQ (1100)

Hard coded byte=1 (00000001)

Unused Extra Data (0000……0)

7 microNode Configuration

Node Provisioning Tools (NPT) are used for Node provisioning. Complete provisioning of Nodes involves three distinct utilities:

1. Node Software Upgrade Utility (sw_upgrade.py)
   This utility is used for upgrading the Node firmware.
2. Node Flash Configuration Utility (config_node.py)
   This utility is used for programming Node flash configuration parameters.
3. Node Key Provisioning Utility (provision_node_keys.py)
   This utility is used for programming Node Over-the-Air (OTA) security keys.

For details about Node Provisioning Tools, refer to the *NPT User Guide (010-0060-00).*

8 Antenna Diversity

The microNode supports Antenna Diversity for optimal System performance. In many cases, the microNode and Host system are mounted in fixed locations that often experience nulls in the RF spectrum. Antenna Diversity can help with optimization of the RX and TX paths. In marginal coverage areas, an RF null could easily disadvantage the microNode to enforce it to transmit at a higher TX Power (more current) or causes network loss and frequent rescanning to reacquire the network (again, more current). These scenarios produce customer dissatisfaction as well as increased battery drain. On-Ramp Wireless has designed numerous diversity solutions and has found the circuit in shown in the following figure to work well.

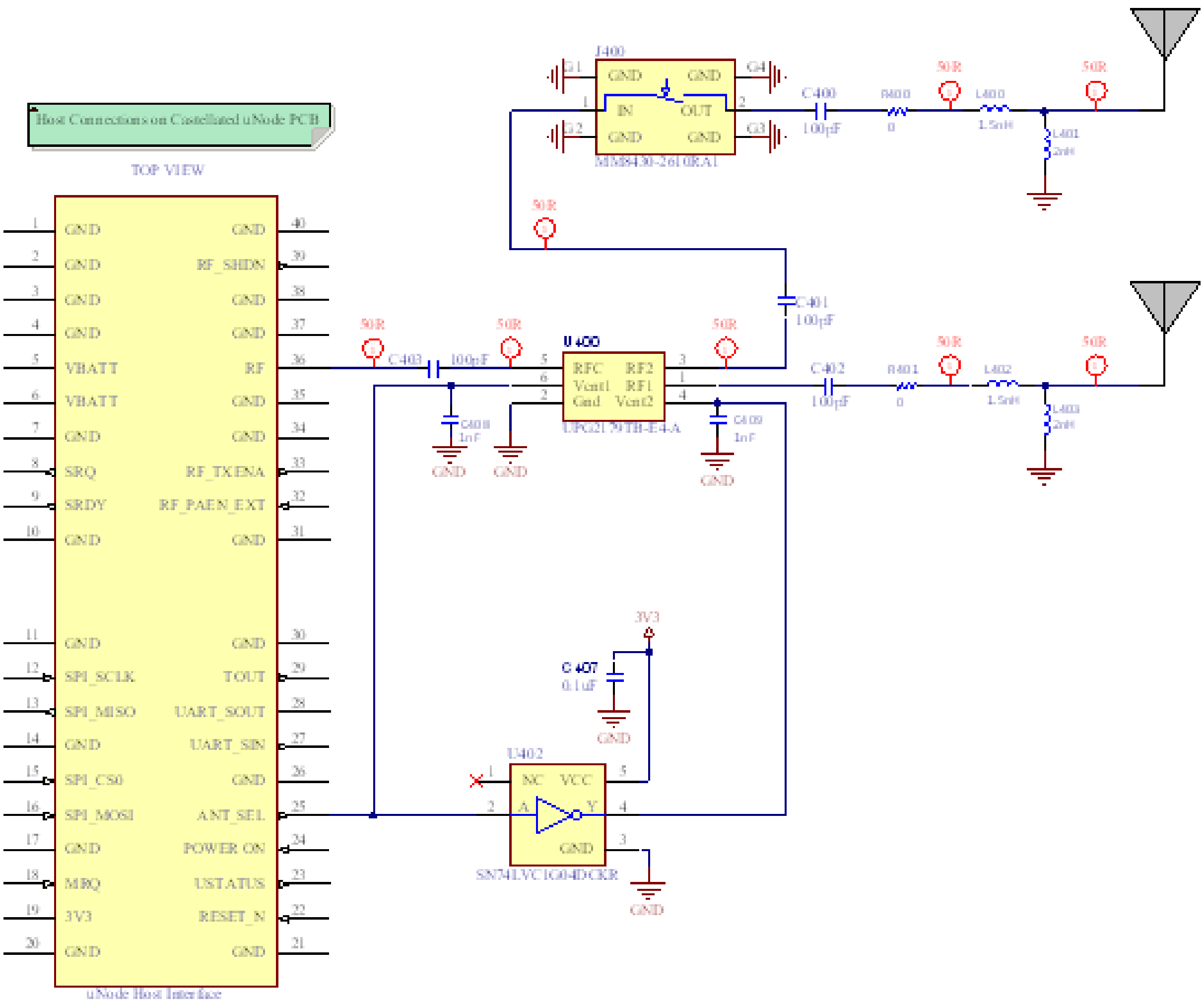


Figure 17. Antenna Diversity Circuit

8.1 Antenna Design Considerations

Good antenna design is also crucial to success. It is important to consider some pertinent issues.

- Ceramic antennas can work well but may sometimes have issues. Careful testing must be done to ensure desired gains and radiation patterns.
- The product must be researched in conjunction to the AP, its deployment, and its antenna radiation pattern. Nominally the AP will be tower or mountain mounted with a downward tilt. The microNode and System may be mounted vertically or horizontally—forcing requirements on the microNode's optimal radiation pattern.
- The antenna must be well matched and with low loss between microNode and antenna. It is important to follow the manufacturer's recommendations. The use of low tolerance ceramic capacitors and low tolerance thin film inductors are recommended. Examples include the Murata GJM series of capacitors and LQP series of inductors. If using stripline RF port feeds, care must be employed to ensure low loss and proper impedance. The antenna match may change when fully integrated into a product. Is advised to recheck the match after full integration. During tuning this may require the use of so called "RF pigtails" in an ad hoc fashion. If the Bill of Materials (BOM) cost will allow, a special connector can be implemented to support this verification/optimization.
- Metallic objects nearby to the antenna can affect radiation gains, patterns, and power match. Typically anything within about 4-5 inches can affect the match significantly particularly if the nearby metal is resonant at 2.4 GHz. A little pattern distortion usually is not of too much concern unless deep wide angular nulls in the antenna pattern results. Other types of pattern distortion can be caused by absorptive losses due to lossy dielectrics nearby the antenna, which represents real power loss dissipated as heat in the loss object. This represents power that is completely lost and not radiated in a useful direction.
- Noisy System clocks with harmonics can fall into the operating band of the microNode and can be picked up by the antennas—degrading sensitivity, or causing Electromagnetic Compatibility (EMC) regulatory failures.

8.2 Diversity Considerations

The operating frequency of the microNode is the ISM 2.4GHz band. This has a wavelength of 12.3 cm in air. For optimal null/peak diversity detection, the antennas must be separated by at least 2.5" (5cm). It is a good idea on the diversity antenna to orient it 90 degrees from the main antenna in order to improve on polarization diversity between antennas in addition to spatial de-correlation.

Practical ground plane-independent antennas are preferable to those that require the printed circuit board (PCB) copper for the antenna counterpoise. Examples of these are dipole antennas and some chip patch antennas. However these can be cost adders in certain cases. It should be noted however that some chip antennas that use the PCB for ground return have been shown to produce reasonable performance. Two examples of this are the surface mount offerings from Molex and Antenova.

- The Antenova Rufa was found to have slightly better performance but about 2x higher cost. It is low profile but consumes more “XY” space. Cost is approximately $0.70 for 10k pieces.
- The Molex 47948-0001 works well. It stands about 4 mm tall but consumes much less “XY” space. Cost is approximately $0.35.

9 Regulatory Considerations

The microNode uses a castellation for its RF port. This lowers the unit cost but also requires the System Integrator to certify the complete Host System for FCC, IC, ETSI, Japan, or other regions intended for sale into their respective markets. Whereas On-Ramp Wireless does not provide a modular certification for the module, it has gone through its own certification of the product to ensure it can be certified. The microNode was certified on an On-Ramp Wireless application platform—the “eHost.” These documents and results are available to System Integrators to ensure that the product can be certified.

Additionally, On-Ramp Wireless has prepared certification guidelines on how to use the software and system tools required for certification. Some markets (such as FCC/IC) are fairly straight forward for certification and are largely TX Spectrum-based. Other markets (such as ETSI) require a much more sophisticated FER process involving an Access Point and Quick Start System. These procedures are defined in the document entitled *Node FCC/IC/ETSI EMC Compliance Test Procedures (009-0021-00).* This document also includes hints and recommendations to help make the process as easy as possible. For more information about this document, see the list of documents referenced in Chapter 1: Overview.

9.1 Block Diagram

Some regulatory domains require a block diagram of the module for their documentation similar to that shown in the following figure.

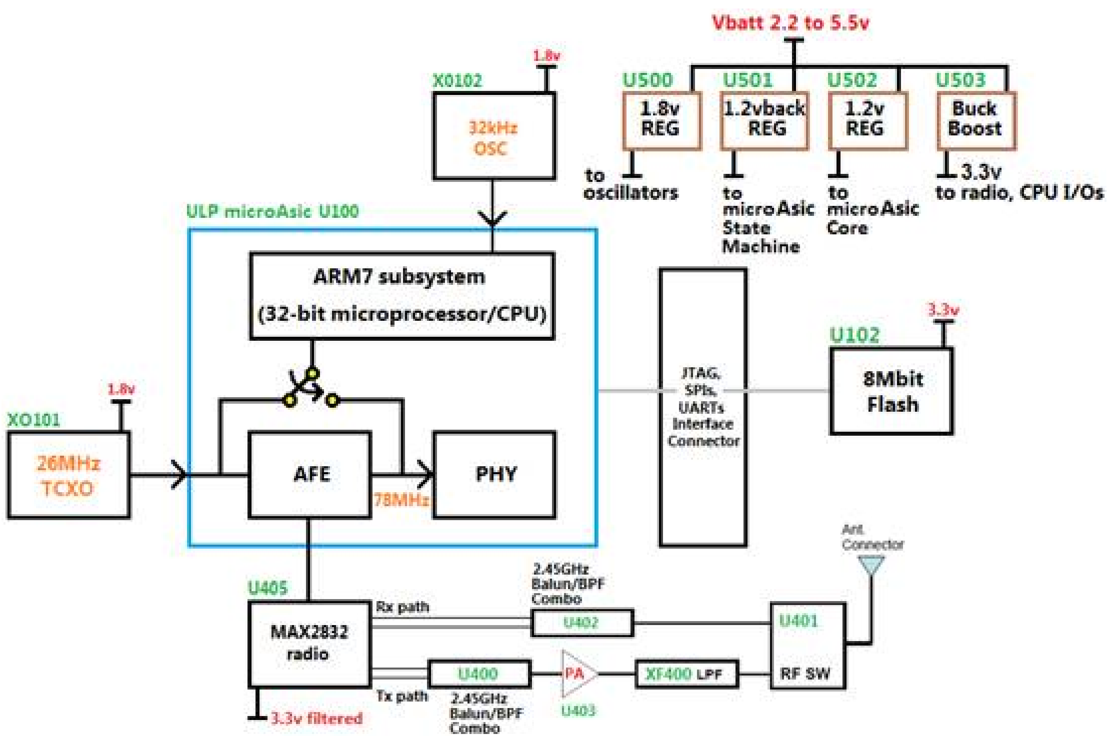


Figure 18. microNode Block Diagram

9.2 Certifications

The microNode is designed to meet regulations for world-wide use. It is certified in the United States, Canada, and Europe as a Limited Single Module. The certifications currently achieved are listed in the following table.

Table 6. microNode Certifications

Country	Certifying Agency	Certification(s)
United States	Federal Communications Commission (FCC)	n 15.207 for powerline conducted emissions. n 15.215 for RF TX bandwidth, power, conducted and radiated emissions.
Canada	Industry Canada (IC)	n RSS210e, includes FCC tests and IC-specific tests (RX radiated emissions).
Europe	European Telecommunications Standards Institute (ETSI)	n 300 440-1 and 440-2, ETSI Emissions. n 301 489-1, ETSI Immunity.

Additional details can be found in the document entitled *Node FCC/IC/ETSI EMC Compliance Test Procedures (009-0021-00)* referenced in Chapter 1: Overview.

The integrator of the final product is often required to do additional compliance tests. The integration application and market will determine specifics. The integrator is advised to consult with local experts in compliance certifications for complete information.

- **FCC/IC**
  The final product may only need Class B unintentional radiator and powerline conducted emissions tests. This should be done with the actual production antenna.
- **ETSI**
  Europe's system is a self-declaration system. There are no documents to submit or certification grants to obtain. One must have the passing test results available for all applicable requirements at any time if challenged.
- Other countries will vary.

9.3 FCC Warnings

This device complies with part 15 of the Federal Communications Commission (FCC) Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

WARNING: This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the instructions, this equipment may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Re-orient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

9.4 IC Warnings

The installer of this radio equipment must ensure that the antenna is located or pointed so that it does not emit RF field in excess of Health Canada limits for the general population. Consult Safety Code 6 which is obtainable from Health Canada's website http://www.hc-sc.gc.ca/index-eng.php.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

To reduce potential radio interference to other users, select the antenna type and its gain so that the equivalent isotropically radiated power (EIRP) is not more than that permitted for successful communication.

Canadian Two Part Warning Statement:

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

9.5 ETSI Warnings

None known.

9.6 Usage

FCC ID: XTE-ULPU100. IC: 8655A-ULPU100. This device is only authorized for use in fixed and mobile applications. To meet FCC and other national radio frequency (RF) exposure requirements, the antenna for this device must be installed to ensure a separation distance of at least 20cm (8 inches) from the antenna to a person.

9.6.1 Note to Integrators

A label showing the FCC ID and IC designators, listed above, must be affixed to the exterior of any device containing the microNode (if the microNode is not visible). The exterior label must include: *Contains FCC ID: XTE-ULPU100, IC: 8655A-ULPU100*.

9.6.2 RF Exposure Statement

The air interface supports operation on channels in the 2402 MHz – 2476 MHz range for FCC/IC regulatory domains and 2402 MHz – 2481 MHz for the ETSI regulatory domain.

Before the ULP microNode becomes operational, it must undergo a commissioning procedure, during which critical information required for operation is entered into the device and stored in non-volatile storage. It is during the initial commissioning procedure that the regulatory domain, under which the device will operate, is set. Subsequent configuration of the device during operation is checked against the commissioned regulatory domain and non-permitted channels or transmit power levels are rejected and the device will not transmit until a permissible configuration per the commissioned regulatory domain is set.

9.7 Antennas

This device has been designed to operate with a 2 dBi omni-directional antenna. It is permissible to use a different antenna as long as it is the same type (e.g., monopole/omni) and has the same or lower gain. Antenna types having a higher gain are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

10 Manufacturing Considerations

This section deals with manufacturing details such as:

- Design of Host PCB for mounting the microNode
- The manufacturing process and soldering profile
- The validation and configuration of the microNode after the assembly process.

10.1 Mechanical Outline

The microNode is a PCB module with 40 castellated pins on two sides of its perimeter. It is designed to be directly surface-mounted onto a Host PCB. All signals (including power, grounds, RF, and digital interface) are brought through the 40 castellated pins. The mechanical outline of the PCB is detailed in Appendix E: microNode Mechanical Drawing.

10.2 Host PCB Constraints

For Host layout, please refer to Appendix C: PCB Land Pattern. It is important to use the recommended land pattern as well as consider coplanarity of the Host in order to get optimal yield in manufacturing. Coplanarity is defined as the bow and twist of the microNode and Host PCBs. Careful measurements of the microNode have been made such that it meets flatness specifications such as those defined in Appendix B: Coplanarity Requirements. Some design considerations of the Host may be:

- Layout of the PCB. Are the copper planes (top, bottom, and center) similar in coverage and density? For instance, the top layer of the Host PCB will be all ground plane, yet if the bottom of the PCB is not similar it will warp during reflow.
- Is the Host board large? If so, the Host may need center support during reflow to prevent "drooping."

10.3 Solder Profile

The microNode is a module intended to be surface-mounted to the Host PCB. The Host supplies all the control lines and antenna port for the microNode. The microNode requires specific soldering profiles. The use of the Restriction of Hazardous Substances (RoHS) Directive is recommended for all soldering. The microNode itself is RoHS-compliant. For further details, refer to Appendix D: microNode Solder Profile.

10.3.1 Handling Procedures for microNode

- The microNode should be handled as an MSL 3 device per IPC/JEDEC J-STD-033 (latest revision).

- If the microNode is exposed to air for more the 168 hours prior to use, it must be baked for a minimum of 8 hours at 125°C prior to use. Refer to the IPC/JEDEC J-STD-033 (latest revision) for further information.
- Residual material (if not used within 168 hours) should be baked (as above) and resealed in a moisture barrier bag. Refer to the JEDEC standard indicated above for additional details.

10.3.2 Solder Procedures for microNode

The microNode is a RoHS-compliant device and should be soldered with lead-free solder paste and a "no-clean" process. Characterization at On-Ramp Wireless was conducted as follows: Solder type used was SAC305 AIM NC 258, with ROL0 Flux paste.

Table 7. Solder Profile Information

Rate of Rise 2°C/Sec Max	Ramp to 150°C (302°F)	Progress through 150°C – 175°C (302°F – 347°F)	To Peak Temp 230°C – 245°C (445°F – 474°F)	Time Above 217°C (425°F)	Cool Down ≤ 4°C/Sec	Profile Length Ambient to Peak
Short Profiles	≤ 60 Sec	15-45 Sec	45-75 Sec	45-60 Sec	45± 15 Sec	2.75-3.75 Min
Long Profiles	≤ 90 Sec	60 -90 Sec	45-60 Sec	45-75 Sec	45± 15 Sec	4.0-5.0 Min

NOTE: The recommended reflow profile for NC258 is provided as a guideline. Optimal profile may differ due to oven type, assembly layout, or other process variables. Contact AIM technical support if you require additional profiling assistance.

- A representative solder profile for a 10-Zone reflow oven is provided for reference.
- Representative Gerber files and an assembly drawing are provided for reference.
- The information provided is for use as a guideline. The manufacturer is responsible for their specific implementation.

The solder profile is shown in Appendix D: microNode Solder Profile.

11 Errata

The microNode uses a Channel scheme such as the following:

- Channel 1 = 2402 MHz and each successive channel is 1.99 MHz offset to that Channel 1.
- Channel 2 = 2403.99 MHz
- Channel 3 = 2405.98 MHz
- Etc.

The microNode uses a 26 MHz reference clock for processing and for the direct conversion radio. It has been found that 26 MHz harmonics can create strong tones that cause some RF sensitivity degradation on these harmonic channels.

- 93*26 MHz = 2418 MHz. This affects channel 9.
- 94*26 MHz = 2444 MHz. This affects channel 22.
- 95*26 MHz = 2470 MHz. This affects channel 35.

System integrators should NOT use these 3 channels as microNode RX sensitivity can be degraded by a nominal 3-10 dB.

Refer to On-Ramp Wireless Issues #2319 and #2616.

Appendix A Abbreviations and Terms

Abbreviation/Term	Definition
AGC	Automatic Gain Control
ALC	Automatic Level Control
AP	Access Point (this product)
API	Application Programming Interface
ASIC	Application-Specific Integrated Circuit
BOM	Bill of Materials
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
CPOL	Clock Polarity (for SPI)
CPU	Central Processing Unit
DFS	Dynamic Frequency Selection
DPLL	Digital Phase-Locked Loop
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FER	Frame Error Rate
GND	Ground
GPIO	General Purpose Input/Output
HBM	Human Body Model
IC	Industry Canada
IIP3	Input Third-Order Intercept Point
LDO	Low Drop Out
LNA	Low Noise Amplifier
LO	Local Oscillator
microNode	Second generation of the ULP wireless module that integrates with OEM sensors and communicates sensor data to an Access Point.
MISO	Master Input, Slave Output
MM	Machine Model
MOSI	Master Output, Slave Input
MRQ	Master Request
MSL	Moisture Sensitivity Level
Node	The generic term used interchangeably with eNode or microNode.
NPT	Node Provisioning Tools
OTA	Over-the-Air
PA	Power Amplifier

Abbreviation/Term	Definition
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
POR	Power On Reset
QoS	Quality of Service
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RoHS	Restriction of Hazardous Substances
RSSI	Receive Signal Strength Indicator
RT	Remote Terminal
RTC	Real Time Clock
RX	Receive/Receiver
SCLK	Serial Clock
SMT	Surface Mount Technology
SNR	Signal-to-Noise Ratio
SPI	Synchronous Peripheral Interface
SRDY	Slave Ready
SRQ	Slave Request
TX	Transmit/Transmitter
UART	Universal Asynchronous Receiver/Transmitter
ULP	Ultra-Link Processing™. On-Ramp Wireless proprietary wireless communication technology.
UNIL	ULP Node Interface Library
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator
VSWR	Voltage Standing Wave Ratio
XO	Crystal Oscillator

Appendix B Coplanarity Requirements

Per IPC-2221 Generic Standard on Printed Board Design Section 5.2.4, the maximum bow and twist shall be 0.75% for boards that use surface mount technology (SMT).

B.1 microNode Dimensions

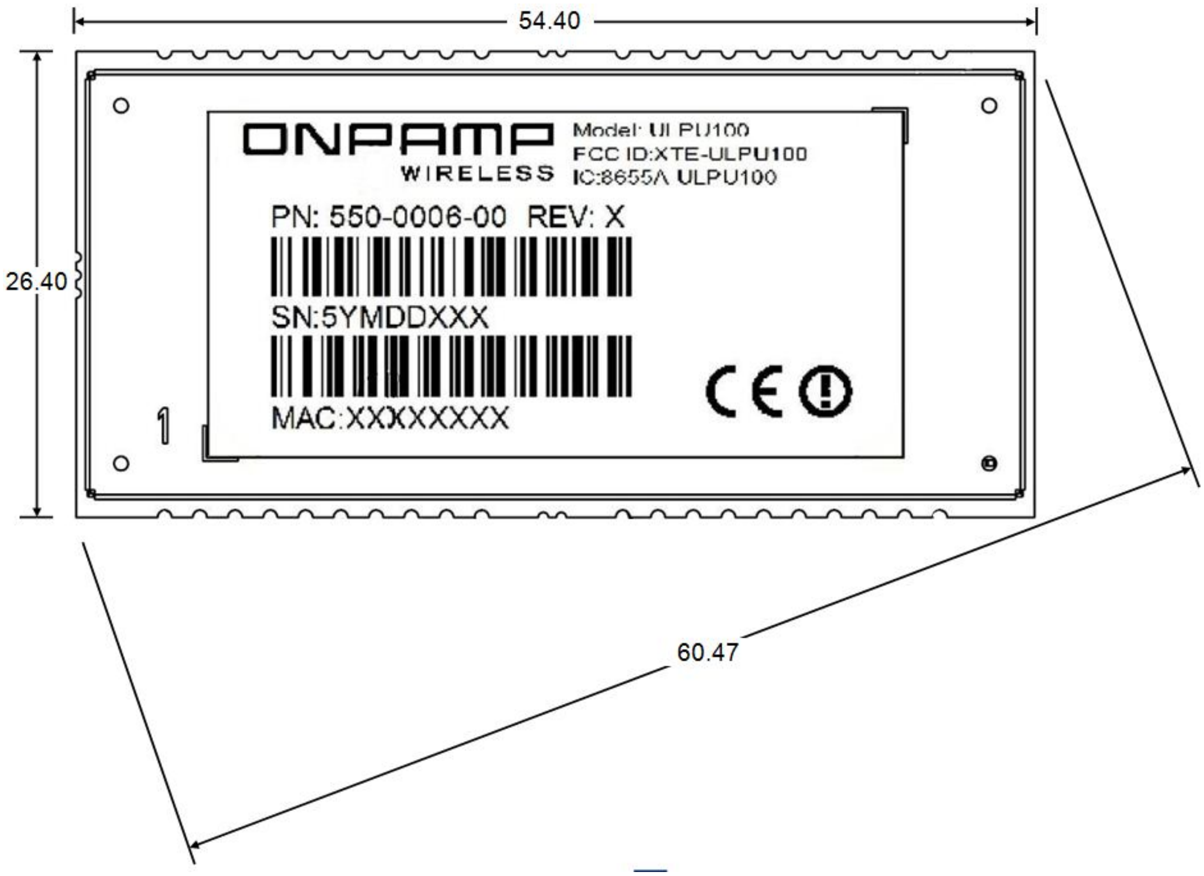


Figure 19. microNode Dimensions

- **Length Dimension**

  54.40 mm, with flatness of 0.75% = 0.408 mm Maximum.

- **Width Dimension**

  26.40 mm, with flatness of 0.75% = 0.198 mm Maximum.

- **Diagonal Dimension**

  60.47 mm, with flatness of 0.75% = 0.454 mm Maximum.

B.2 Bow Measurement

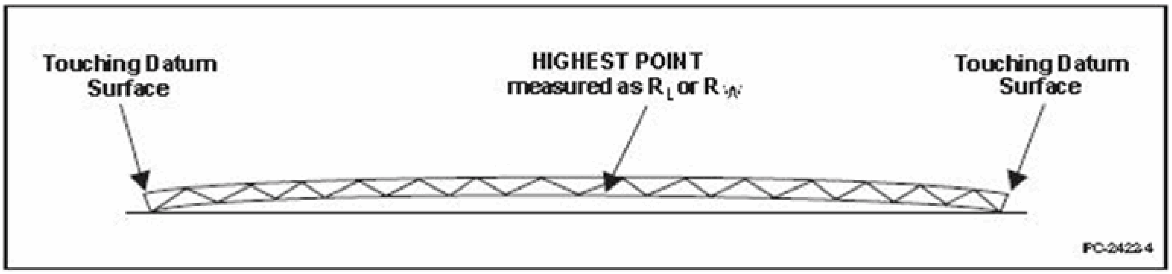


Figure 20. Bow Measurement of Length and Width Bow

$$B_L = \frac{R_L}{L} \times 100$$

R_L = Highest Measured Value (mm) over Length and L = 54.40 mm

$$B_W = \frac{R_W}{W} \times 100$$

R_W = Highest Measured Value (mm) over Width and W = 26.40 mm

B.3 Twist Measurement

$$Twist = \frac{R}{2*(D)} \times 100$$

R = Highest Measured Value (mm) over diagonal

D = Diagonal Measurement of Board = 60.47 mm

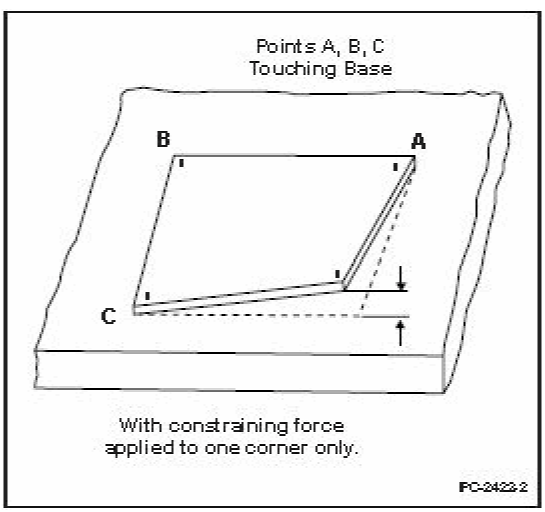


Figure 21. Twist Measurement

Appendix C PCB Land Pattern

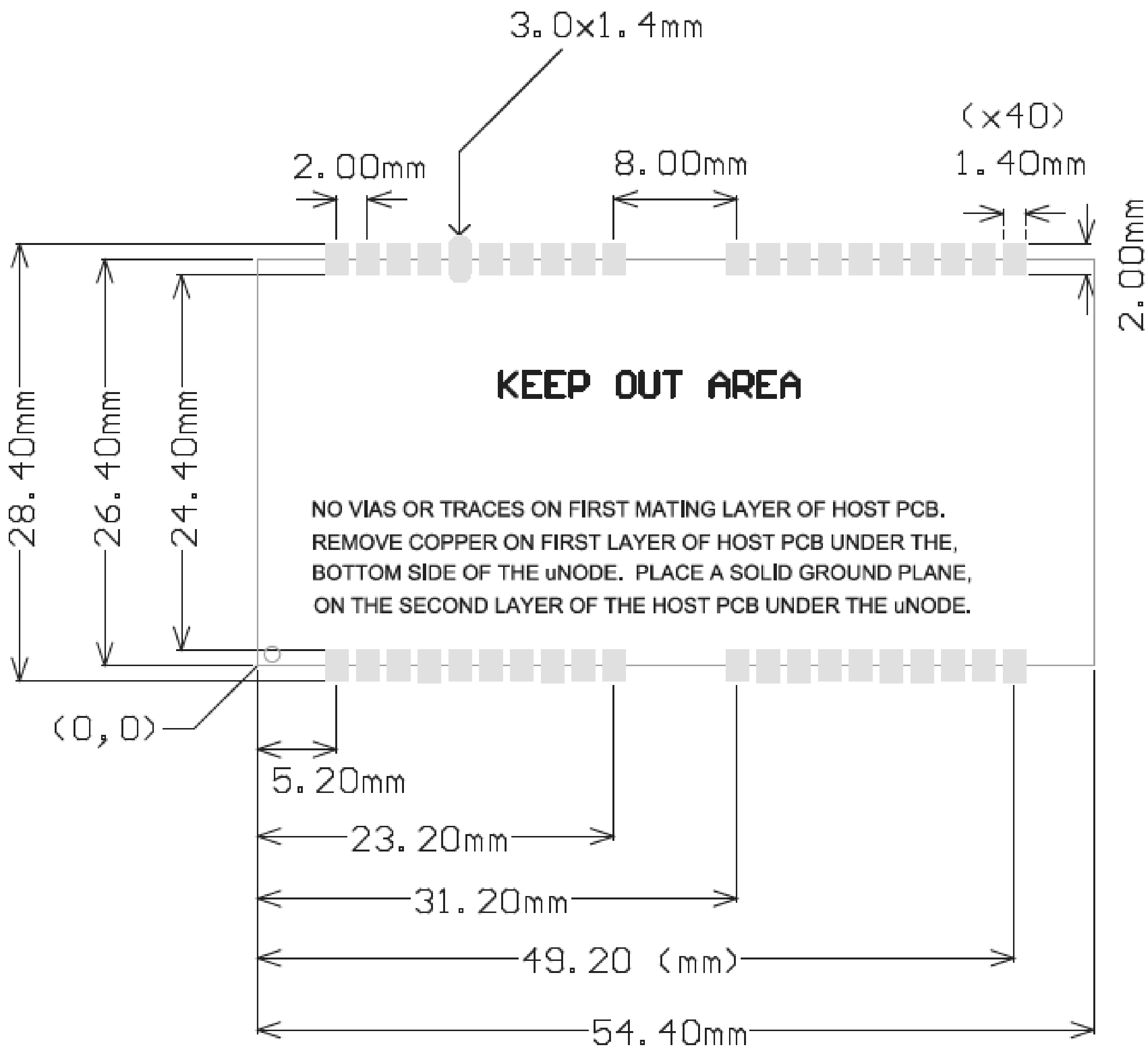


Figure 22. microNode PCB Land Pattern

Appendix D microNode Solder Profile

The following solder profile is for reference purposes only. Integrators should consult with their manufacturers to determine their specific profile.

NOTE: In the figure below, uNode is shorthand for microNode.

uNODER3 **Tue Aug 30 2011 09:17:32**

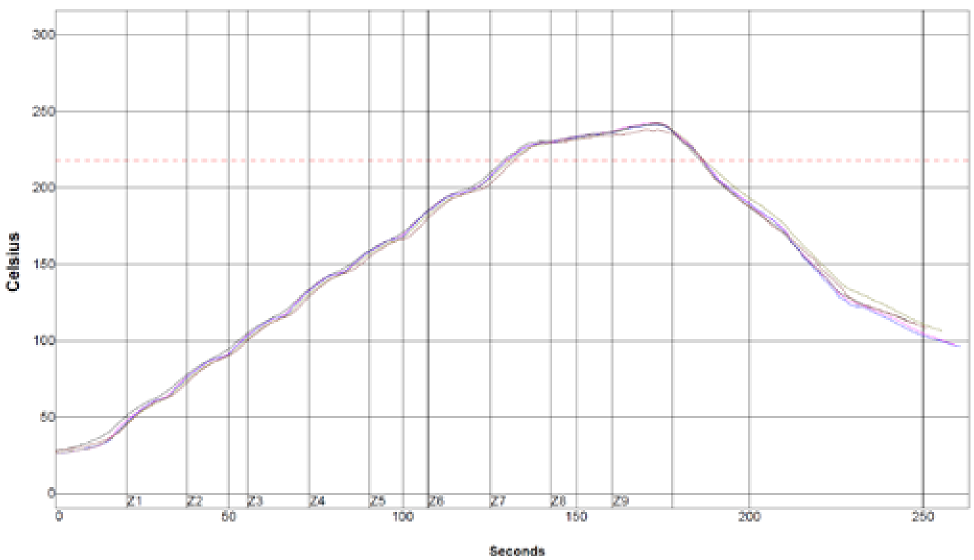
Company:
Oven Name: HELLER 1809EXL

Site:
Process Window Name: AIM NC258 NOCLEAN

Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8	9
Top	74	102	130	164	182	220	256	241	252
Bottom	74	102	130	164	182	220	256	241	252

Conveyor Speed (inch/min): 33.9



PWI= 81%	Max Rising Slope		Max Falling Slope		Reflow Time /218C		Peak Temp	
<TC2>	1.76	78%	-2.48	1%	56.33	51%	242.56	67%
<TC3>	1.79	81%	-2.60	-7%	56.51	53%	241.54	54%
<TC4>	1.71	74%	-2.27	15%	55.64	42%	242.23	63%
<TC5>	1.64	67%	-2.31	13%	56.75	57%	241.78	57%
<TC6>	1.67	70%	-2.26	16%	54.26	24%	237.82	4%
Delta	0.15		0.34		2.49		4.74	

Process Window:

Solder Paste: AIM NC258 NOCLEAN

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=0.9) (Calculate Slope over 20 Seconds)	0	2	Degrees/Second
Max Falling Slope (Calculate Slope over 20 Seconds)	-4	-1	Degrees/Second
Time Above Reflow - 218C	45	60	Seconds
Peak Temperature	230	245	Degrees Celsius

Description:

Profiled Using KIC 2000 Technology

KIC
San Diego, CA USA

Tel: +1 858 673 6050
Fax: +1 858 673 0085

www.kicthermal.com
tech@kicmail.com

Figure 23. Solder Profile

Appendix E microNode Mechanical Drawing

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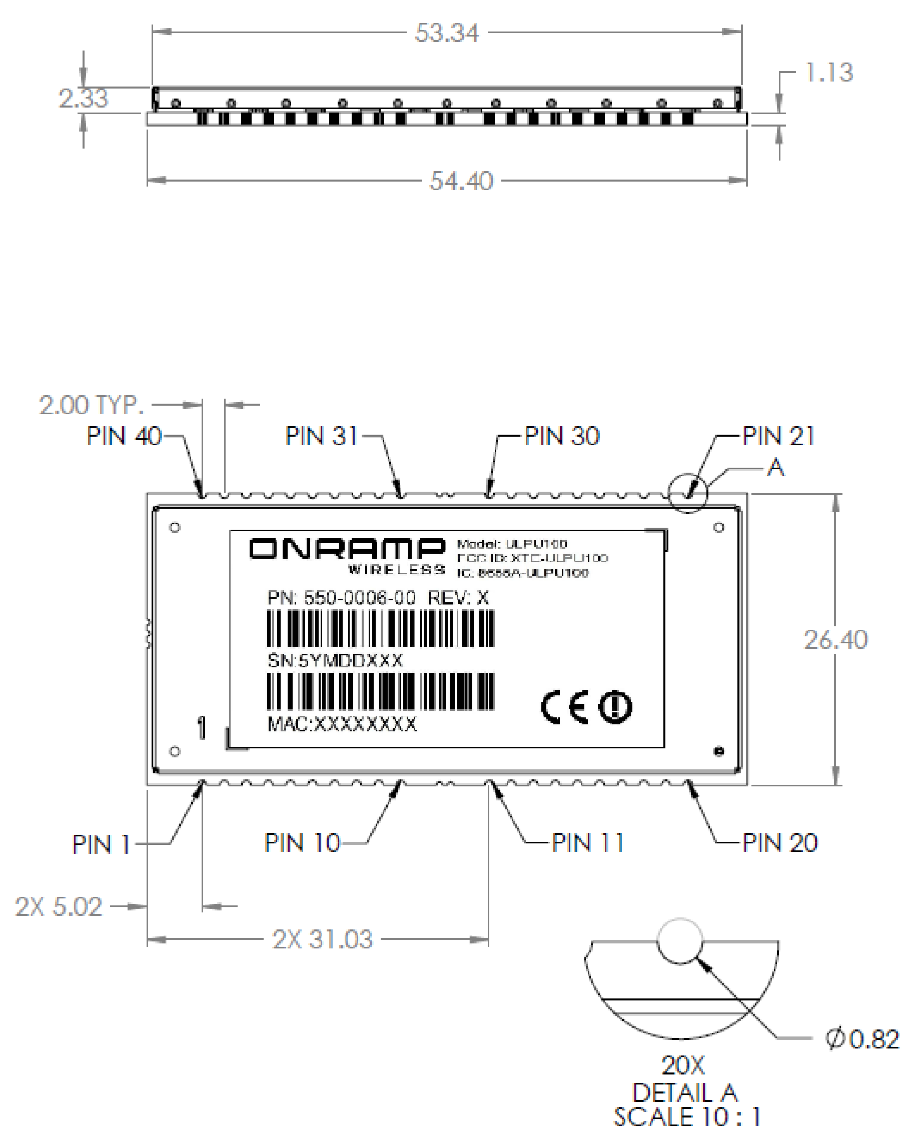
NOTES- UNLESS OTHERWISE SPECIFIED

1. PER IPC-2221 GENERIC STANDARD ON PRINTED BOARD DESIGN SECTION 5.2.4 - THE MAXIMUM BOW AND TWIST SHALL BE 0.75% FOR BOARDS THAT USE SURFACE MOUNT TECHNOLOGY.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	06/24/2011	M.U.
B	NODE PIN DESCRIPTION TABLE CHANGES AND SHIELD UPDATED	10/10/2011	M.U.
C	UPDATED SHIELD, BOARD, TABLE & ARTWORK	01/12/2012	M.U.



NODE PIN DESCRIPTION TABLE

Pin Name	uNode Pin #	Pin Description	Signal Direction Relative to UNODE
SPI-MISO	13	Master In Slave Out	Output
SPI-MOSI	16	Master Out Slave In	Input
SPI-SCLK	12	Serial Clock	Input
MRQ	18	Master Request	Input
SRDY	9	Slave Ready	Output
SRQ	8	Slave Request	Output
SPI-CS0	15	SPI Chip Select	Input
T_OUT	29	Timer Output	Output
RESET_N	22	eNode Reset	Input
RF	36	RF Port	Output, 50 Ohm
RF_SHDN	39	RF Status (ON/OFF)	Output
RF_TXENA	33	RF Status (RX/TX)	Output
RF_PAEN_EXT	32	Disable TX	Input
UART0_SOUT	28	UART TX	Output
UART0_SIN	27	UART RX	Input
ANT_SEL	25	Antenna Select	Output
POWER_ON	24	Power On	Input
USTATUS	23	GPIO	Input/Output (undefined)
VBATT1	5, 6	2.2-5.5V	Power
3V3	19	3.3V power	Output (switched)
GND	1, 2, 3, 4, 7, 10, 11, 14, 17, 20, 21, 26, 30, 31, 34, 35, 37, 38, 40		Ground

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METRIC ONLY

UNLESS OTHERWISE SPECIFIED

INTERPRET DRAWING PER ASME Y14.100-2004

ALL DIMENSIONS ARE IN MM (MILLIMETERS) AND APPLY AFTER SURFACE TREATMENT

INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009

	NAME	DATE
DRAWN	A. CASCIA	06/19/2011
CHECKED		
ENG. APPR.	D. ESPEY	06/24/2011
MFG APPR.	M.U.	06/24/2011
Q.A.		
C.M.		

ONRAMP WIRELESS
10920 VIA FRONTERA, SUITE 200, SAN DIEGO, CA 92127

TITLE: MECHANICAL DRAWING, UNODE

SIZE: B DWG. NO. 510-0028-XX REV: C

SCALE: 2:1 SHEET 1 OF 1

DO NOT SCALE DRAWING

MATERIAL

FINISH

Figure 24. microNode Mechanical Dimensions