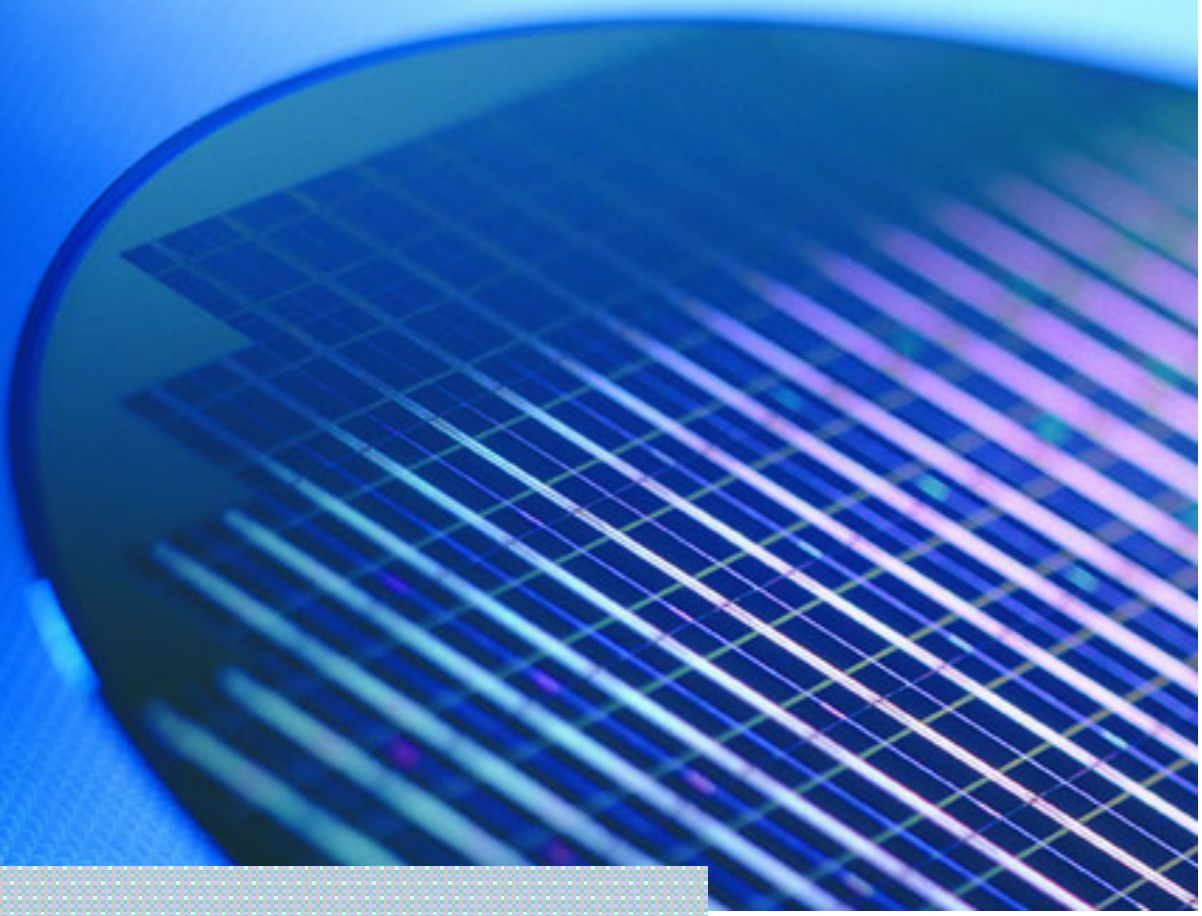
Data Sheet, DS3, June, 2003

ROK 104 001

Bluetooth™ System Module



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ROK 104 001

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	Updated Information on FCC and R&TTE Approval, Updated section 3.6.8 on Power Management 2003-June
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Preliminary Data

1 Overview

The Bluetooth 1.1 System Module ROK 104 001 is a complete FCC and R&TTE type approved product for fast implementation and cuts your time-to-market. It is a compact and cost effective radio/baseband module that can be implemented in any kind of electronic device. The module includes a baseband processor with 4 Mbit Flash memory, a radio solution, interfaces to antenna and application, supporting circuitry, together with basic Bluetooth software for signaling at HCI level (Host Controller Interface) or ECP level (Embedded Communication Platform).

The antenna filter is specially designed for applications in a GSM environment such as inside a mobile phone. The ROK104001 also has a very high threshold for high signal levels in-band, which makes it very suitable to be in an IEEE 802.11b environment.

As the ROK 104 001 is a generic product, it can be used for many different types of applications that require Bluetooth capability such as

- Computers and peripherals
- Handheld devices and accessories
- Inustrial and medical sensors
- Access points and home base stations
- Applications where short time-to-market is required

Type	Package
ROK 104 001	LGA-87

1.1 Key Features

- A small and complete class 2 Bluetooth system
- Forms full Bluetooth functionality with only the addition of an antenna
- Point to multipoint, 7 slaves for HCI firmware and 3 slaves for ECP firmware
- Power management: PARK, SNIFF & HOLD as well as system power saving
- Excellent high signal level performance in-band
- Exceptional out-band blocking in all GSM bands
- Multiple interfaces UART, PCM, bi-directional serial interface/GPIO
- Capability of embedded solutions
- Qualified to Bluetooth spec. 1.1
- FCC and R&TTE type approved
- Supports all Bluetooth profiles

1.2 Reference documents for ECP firmware

- ECI Protocol Specification
- ECI Driver User Manual
- ECI Driver Release Notes
- ECI Firmware Release Notes

These documents can be provided through your Infineon Technologies sales contact.

2 Pin Description

2.1 Pin Configuration

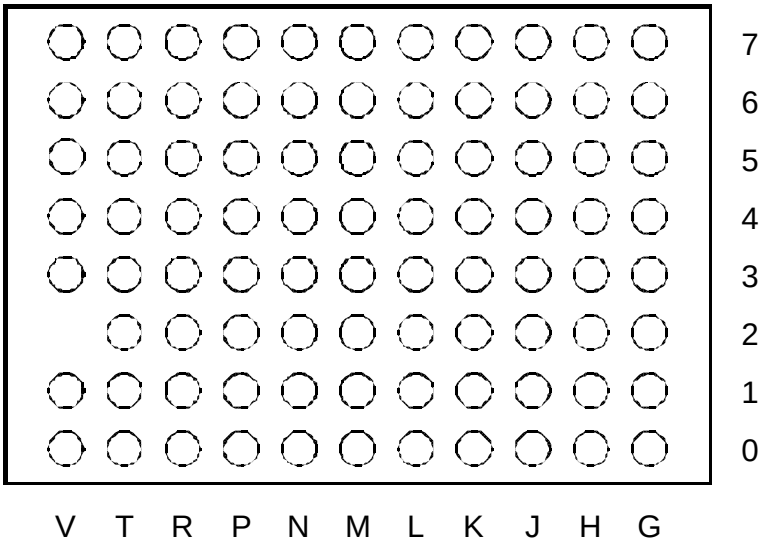


Figure 1 ROK 104 001, Bottom View

2.2 Pin Definition and Function

Table 1 Pin Definition and Function

Pin	Symbol	Type [1)]	Description
G0-2	GND	Power	Mechanical connection to ground
G3-4	N.C.		Mechanical connection - treat as no connect. Pad required.
G5-7	GND	Power	Mechanical connection to ground
H0	N.C.		Mechanical connection - treat as no connect. Pad required.
H1	GND	Power	Mechanical connection to ground
H2	D-	BD, PHY, IOP2	USB data pin (USB function is not supported)
H3	D+	BD, PHY, IOP2	USB data pin (USB function is not supported)
H4	ON	DI, Power	When tied to V_{DD}, the module is HW enabled
H5	GND	Power	Ground
H6	GND	Power	Mechanical connection to ground
H7	N.C.		Mechanical connection - treat as no connect. Pad required.
J0	N.C.		Mechanical connection - treat as no connect. Pad required.
J1	UART2Tx	DO, IOP1	Tx data from UART 2 - not supported by HCI FW
J2	UART2CTS	DIU, IOP1	Flow control signal, Clear To Send data to UART 2 - not supported by HCI FW
J3	UART1CTS	DIU, IOP2	Flow control signal, Clear To Send data to UART 1
J4	V_{DDIO}	Power	External supply rail to the input / output ports
J5	V_{DD}	Power	Supply Voltage
J6	GND	Power	Ground
J7	N.C.		Mechanical connection - treat as no connect. Pad required.
K0	N.C.		Mechanical connection - treat as no connect. Pad required.
K1-2	N.C.		Not connected
K3	UART1RTS	DO, IOP2	Flow control signal, Request To Send data from UART 1
K4	UART1Tx	DO, IOP2	Tx data from UART 1
K5	N.C.		Not connected
K6	GND	Power	Signal ground
K7	N.C.		Mechanical connection - treat as no connect. Pad required.
L0	N.C.		Mechanical connection - treat as no connect. Pad required.
L1	PCMRx	BDU, IOP2 (input default)	PCM receive data (default)
L2	PCMSYNC	BD, IOP2	PCM data sampling rate
L3	WAKEUP	DO, IOP2	Indicates that the module wants to be attached (USB function is not supported)
L4	GND	Power	Ground
L5	N.C.		Not connected

Table 1 Pin Definition and Function (cont'd)

Pin	Symbol	Type[1)]	Description
L6	GND	Power	Ground
L7	N.C.		Mechanical connection - treat as no connect. Pad required.
M0	GND	Power	Mechanical connection to ground
M1	PCMCLK	BD, IOP2	PCM clock that sets the PCM data rate
M2	EXTINT	DID, IOP1	External interrupt for embedded purposes
M3	UART1Rx	DIU, IOP2	Receive data to UART 1
M4	N.C.		Not connected
M5	PWRAVAIL	DID, IOP1	Indicates whether external power is available; used in conjunction with PWRFAIL - not supported by HCI FW
M6	N.C. - VTP4	DO	Not connected - vendor test point #4
M7	GND	Power	Mechanical connection to ground
N0	N.C.		Mechanical connection - do not connect
N1	PCMTx	BD, IOP2 (output default)	PCM transmit data (default)
N2	UART2Rx	DIU, IOP1	Receive data to UART 2 - not supported by HCI FW
N3	GPIOB5	BD, IOP2	General purpose signal #5 input / default output for embedded purposes
N4	GPIOB4	BD, IOP1	General purpose signal #4 input / default output for embedded purposes
N5	UART2RTS	DO, IOP1	Flow control signal, Request To Send data from UART 2 - not supported by HCI FW
N6	N.C. - VTP3	DI	Not connected -vendor test point #3
N7	$V_{DD\text{-}RFDIG}$	AO	Output from internal regulator connected to digital section of the radio. Shall be connected to a minimum capacitance of 2.2µF.
P0	N.C.		Mechanical connection - treat as no connect. Pad required.
P1	GPIOB3	BD, IOP1	General purpose signal #3 input / default output for embedded purposes
P2	EXTSYS WAKEUP	DI, IOP1	Can be used as an external interrupt to control the EBC - for embedded purposes
P3	SERIALCLK	BD3, IOP1	Bidirectional serial interface / GPIO clock signal
P4	DETACH	DIU, IOP2	Indicates that the USB host wants to detach the module (USB function is not supported)
P5	N.C. - VTP2	DO	Not connected - vendor test point #2
P6	GPIOB6	BD, IOP1	General purpose signal #6 input / default output for embedded purposes
P7	N.C.		Mechanical connection - treat as no connect. Pad required.
R0	N.C. - VTP5	AO	Not connected - vendor test point (VDD_DIG) #5
R1-2	GND	Power	Ground
R3	RESET	DI, IOP1	Reset signal, active low (must be fed from an open drain output)

Table 1 Pin Definition and Function (cont'd)

Pin	Symbol	Type [1)]	Description
R4	GPIOB2	BD, IOP1	General purpose signal #2 input / default output for embedded purposes
R5	PWRFAIL	DIU, IOP1	Indicates a poer fail condition; used in conjunction with PWRAVAIL - not supported by HCI FW
R6	GPIOB7	BD, IOP1	General purpose signal #7 input / default output for embedded purposes
R7	N.C.		Mechanical connection - treat as no connect. Pad required.
T0	N.C.		Mechanical connection - treat as no connect. Pad required.
T1	GND	Power	Ground
T2	ANT	BD, RF	50 Ω antenna connection
T3	GND	Power	Ground
T4	N.C.		Not connected
T5	N.C. - VTP1		Not connected - vendor test point #1
T6	SERIALDATA	BD, IOP1	Serial interface - data signal
T7	N.C.		Mechanical connection - treat as no connect. Pad required.
V0-1	GND	Power	Mechanical connection to ground
(V2)			(No pad)
V3-7	GND	Power	Mechanical connection to ground

1) AO = Analogue output pad
BD = Bi-directional pad
BDU = Bi-directional pad with pull-up
DI = Input pad
DIU = Input pad with pull-up
DID = Input pad with pull-down
DO = Digital Output
GND = V_{SS} power supply pad
IOP1 = IO group V_{DD_DIG} power supply pad
IOP2 = IO group V_{DD_IO} power supply pad
POW = Core power supply pad
PHY = USB transceiver pad shared with UART1 RI and DCD pins (USB function is not supported)
RF = Radio Frequency pad

3 Functional Description

3.1 Functional Block Diagram

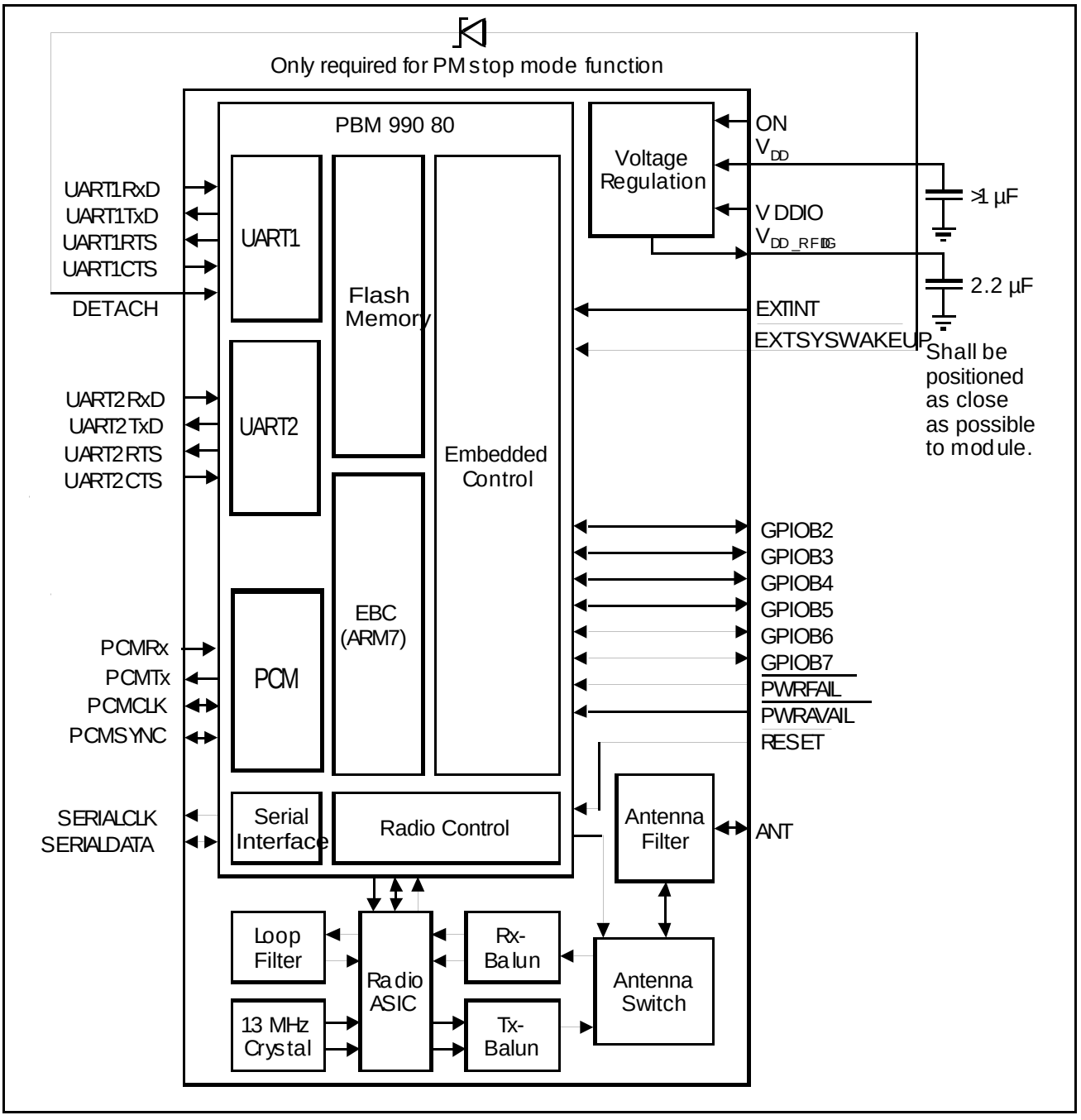


Figure 2 Block Diagram

The ROK 104 001 is a complete Bluetooth module that has been specified and designed according to the Bluetooth System v1.1. Its implementation is based on a high-

performance integrated radio IC working with the baseband controller PBM 990 80, with integrated flash memory and surrounding secondary components.

ROK 104 001 consists of three major parts; a baseband controller, firmware, and a radio. Multi slot data and voice packets are supported. Communication between the module and the host controller is carried out on UART and PCM interfaces. ROK 104001 is compliant with BT version 1.1 and is a Class 2 BT Module. ROK 104 001 is tested according to R&TTE and FCC type approval requirements.

3.2 Design Sections

ROK 104 001 has five major design sections. Figure 2 illustrates the interaction of the various sections. The functionality of each section will be briefly explained.

3.2.1 Radio

The radio functionality is achieved by an Infineon Technologies Radio IC, a short-range microwave frequency radio transceiver for Bluetooth communication links based on RFCMOS technology.

3.2.2 Baseband

The baseband functionality is achieved by using Infineon Technologies PBM 990 80, providing the baseband functionality and Flash memory. The baseband contains a Bluetooth core (EBC); an ARM 7 processor, I/O ports (PCM and UART) and RAM memory. Firmware is downloaded into the flash memory. The interfaces that are implemented on the baseband chip are UART, PCM and serial clock interface (bi-directional serial interface / GPIO).

PBM 990 80 provides the link-setup and control routines for the layers above. Furthermore, PBM 99080 also provides Bluetooth security like encryption, authentication and key management.

Please refer to the PBM 990 80 data sheet for further information regarding baseband functionallity.

3.2.3 Voltage Regulation Section

There are three inputs to the voltage regulation section (V_{DD}, V_{DD_IO}, ON). V_{DD} can be fed with 3.1 V to 4.75 V. The power regulator on the module creates 2.7 V regulated supply.

A separate power supply rail (V_{DD_IO}) is provided for the I/O ports, UART and PCM. V_{DD_IO} can either be connected to V_{DD} or to a dedicated supply rail, which is the same as the logical interface of the host.

The ON input is the only signal that is required to activate the module.

3.2.4 Crystal Oscillator

An internal crystal oscillator supplies radio IC and Baseband with a stable frequency. No external oscillator or crystal is required.

3.2.5 Flash Memory

ROK 104 001 is delivered with 4 Mbit Flash memory. Firmware (F/W), in terms of link manager and applicable upper layer stack parts, resides in the Flash and is available as image file formats.

3.3 Module HW Interfaces

3.3.1 Host Interfaces

To enable a host system to access the Bluetooth radio link, a Host Controller Interface (HCI) has been defined. The host system controls and distributes data to and from the Bluetooth Link Manager with a set of commands. These commands are carried physically on either the UART or USB interface (not supported by firmware).

3.3.1.1 UARTs

The UART implemented on the baseband is an industry standard and supports the following baud rates: 300, 600, 900, 1200, 1800, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 bits/s. 128-byte FIFOs are associated with the UART1.

Four signals will be provided for the UART interface. TxD & RxD are used for data flow, and RTS & CTS shall be used for flow control. The module is a DCE.

There are two on-chip UART interfaces, UART1 and UART2.

UART1 has 128-byte FIFOs and full modem control support and is used for data in and out transmission at bit rates up to 921 kbit/s. UART1 is setup to a DTE configuration.

UART2 has 16-byte FIFOs and is used for control and/or boot.

Start-detect and Auto-baud functionality is available for both UARTs.

Table 2 HCI Default Settings UART1, UART2

Speed	57600 bit/s
Data bit	8 bit
Stop bit	One
Parity	None
Flow	CTS/RTS

Note: These settings can be changed from the HCI level using Ericsson specific commands. For HCI and ECP firmware, UART2 is disabled since UART1 is default.

3.4 Other Interfaces

3.4.1 Serial Interface

The bi-directional serial interface / GPIO interface function is based on software using two GPIO's. The interface has a capacity of handling approximately 100 kbit/s.

A master serial I/F is available on the module. This is used to control external serial interface devices. The controls of the serial interface pins are performed by Ericsson specific HCI commands available in the FW implementation. See Application Note. This enables application in a stand-alone ROK 104 001 module to also control other devices via the serial interface.

3.4.2 General Purpose I/O

The ROK 104 001 architecture supports up to 8 General Purpose I/O's. 2 GPIO's are default, that is used as the serial interface.

3.4.3 PCM Voice Interface

Uses the standard PCM interface, which has a sample rate of 8 kHz (PCMSYNC). The PCM I/F can be set in master or slave mode (providing or receiving the PCMSYNC and PCMCLK).

PCM clock (PCMCLK) is variable between 200kHz and 2.048 MHz in slave mode. During the master mode, the PCMCLK is set at 2 MHz. PCM data can be linear PCM (13-16bit), µ-Law (8 bit) or A-Law (8 bit).

Over the air the encoding is programmable to be CVSD, A-Law or µ-Law.

The PCM line interface can act either as slave or master. When the PCM line interface is slave the frequency range of PCMCLK (in) is 200 kHz to 2.048 MHz. When the PCM line interface is master PCMCLK (out) is always 2 MHz.

Each PCM symbol on the PCMTx or PCMRx line is organized as an 8 or 16-bit sequence of bits, arriving synchronous to PCMCLK in (if the PCM line interface is slave) or PCMCLK out (if the PCM line interface is master). The symbol starts with its most significant bit arriving after a positive edge on the PCMCLK in (or out), one clock cycle after a PCMSYNC in (or out) positive transition. The symbol is then transferred by one bit each PCMCLK in (or out) clock cycle until the least significant bit is transferred. The EBC then samples the arriving bit at falling edges of PCMCLK in (or out).

The PCM symbols are transmitted bit by bit starting with the MSB, one clock cycle after a positive edge on the PCMCLK in (if the PCM line interface is slave) or PCMCLK out (if the PCM line interface is master), one clock cycle after a PCMSYNC (in or out) positive transition. The rest of the bits are then transferred by one bit each PCMCLK (in or out) cycle, and are synchronized with the rising edge of this clock.

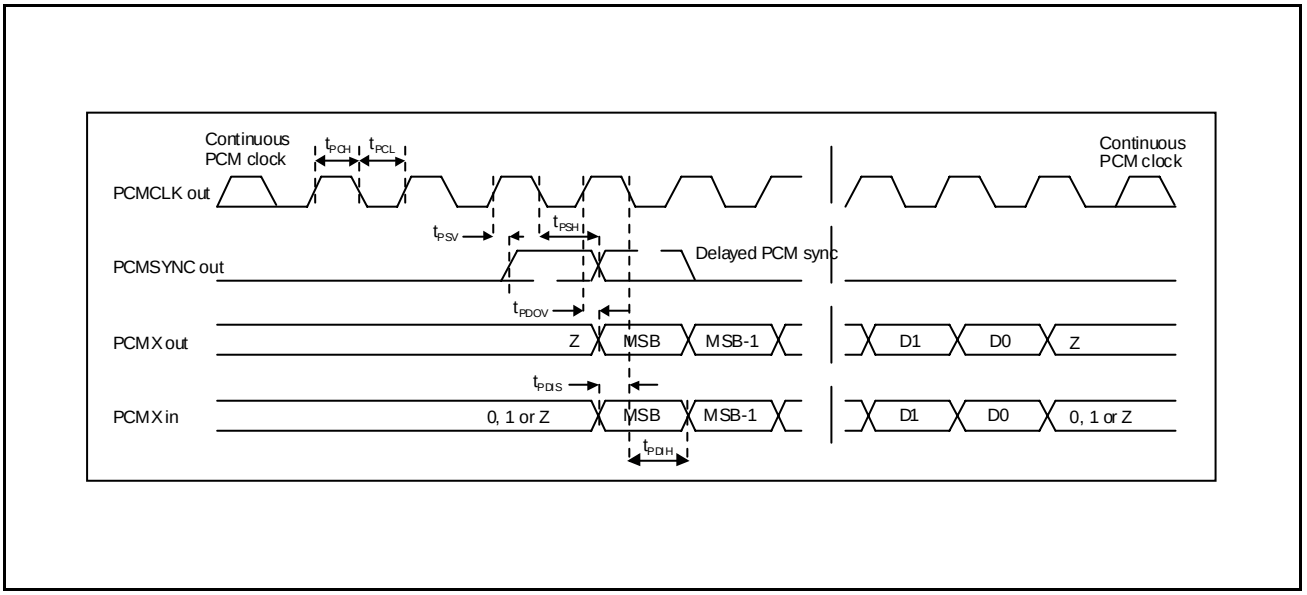


Figure 3 PCM Master Mode Timing Diagram

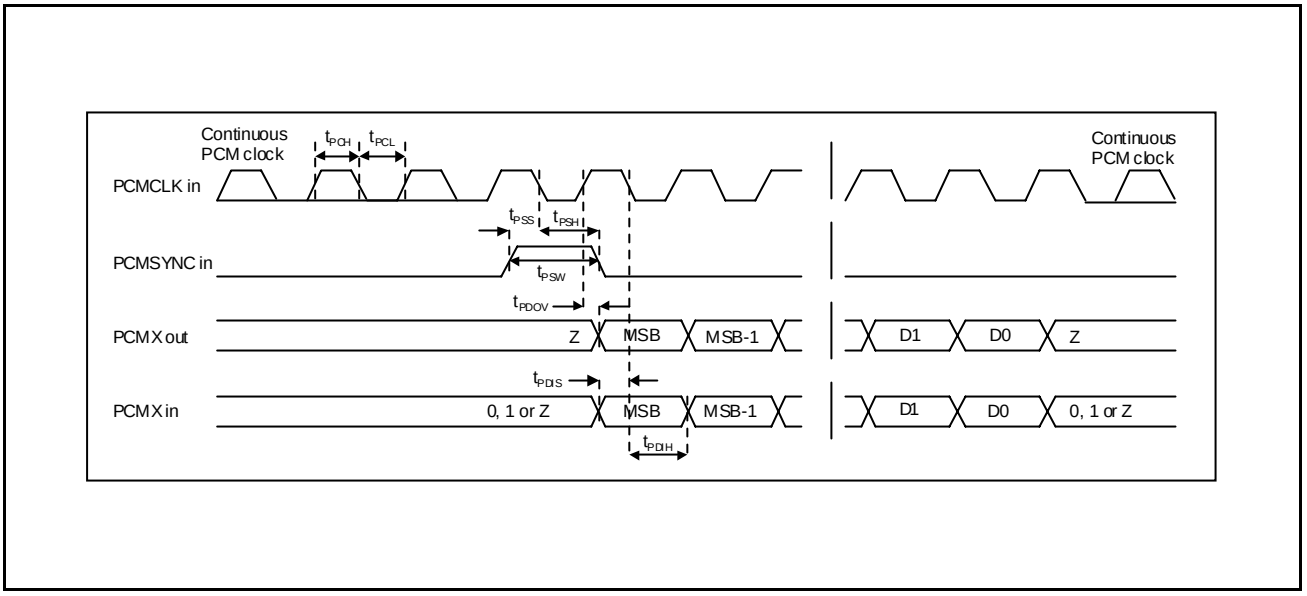


Figure 4 PCM Slave Mode Timing Diagram

3.4.4 Antenna

The ANT pin should be connected to a 50 Ω antenna interface, thereby supporting the best signal strength performance, VSWR should not be higher than 2:1. Infineon Technologies can recommend application specific antennas.

3.5 Software

The Bluetooth link is partitioned into a hardware part and a software part. The software relates to the Bluetooth protocol stack. Depending on the level of integration, there will be two different firmware models available, including hardware specific drivers for the Bluetooth core, UARTs, GPIO and bidirectional serial interface / GPIO. The level of integration follows the two main scenarios:

- LM & HCI firmware for HCI based applications, where the upper layer stack is integrated in a host processor external to the ROK 104001
- Embedded Communication Platform (ECP) where LM and upper layer Bluetooth stack resides in the ROK 104001, communicating with an external host processor through an easy to use ECI-interface (Embedded Communication Interface). For further documentation on ECP and ECI, please refer to ECI-driver documentation.

3.5.1 Firmware

The module includes firmware for the host controller interface, HCI, and the link manager, LM. The FW resides in the Flash and is available in load format (*.mfl) and in binary format (*.bin).

3.5.2 Bluetooth Module Stack

The Host Controller Interface (HCI) handles the communication by the transport layer through the UART interface with the host. The Baseband and radio provide a secure and reliable radio link for higher layers. The following sections describe the Bluetooth module stack in more detail, see also **Figure 5**. It is implemented in accordance with and complies with the Specification of the Bluetooth System v1.1.

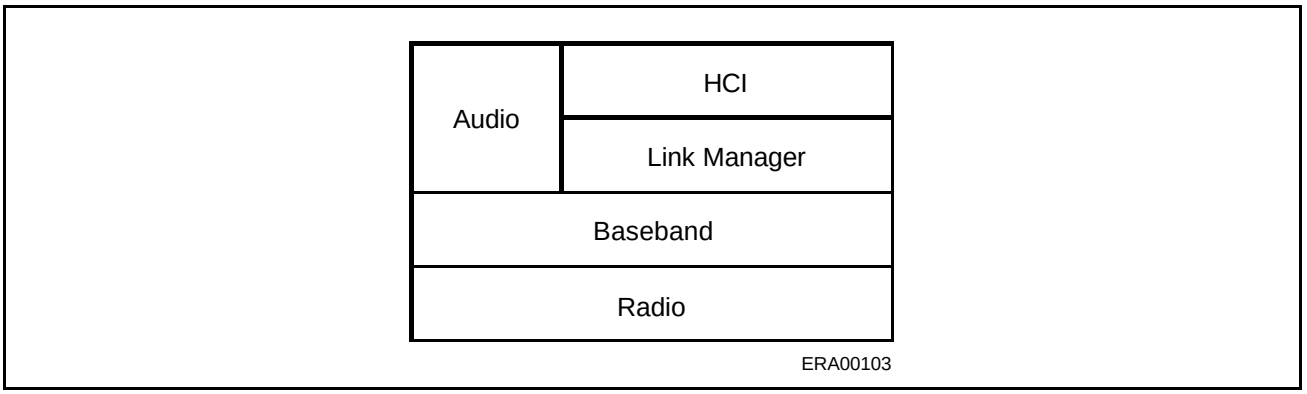


Figure 5 HW/HCI FW Parts Included in the Bluetooth Module from Infineon

3.5.3 LM & HCI Firmware

In this configuration the customer will access the LM through a Host Controller Interface (HCI) protocol distributed over UART.

3.5.4 Host Controller Interface (HCI)

The HCI provides a uniform command I/F to the Baseband and Link Manager and also to HW status registers. The HCI I/F is accessed through UART. There are three different types of HCI packets:

- HCI command packet - from host to Bluetooth module HCI
- HCI event packets - from Bluetooth module HCI to host
- HCI data packets - going both ways

It is not necessary to make use of all different commands and events for an application. If the application is aimed at a pre-specified profile, the capabilities of such a profile are necessary to adjust to - see Specification of the Bluetooth System v1.1. Profiles and Application Note

a) With the HCI UART Transport Layer on top of HCI, the module will communicate with a host through the UART I/F. The PCM I/F is also available for communicating voice.

Please refer to the Specification of the Bluetooth System v1.1 part H: 1-4 for in-depth information regarding the HCI and different transport layers.

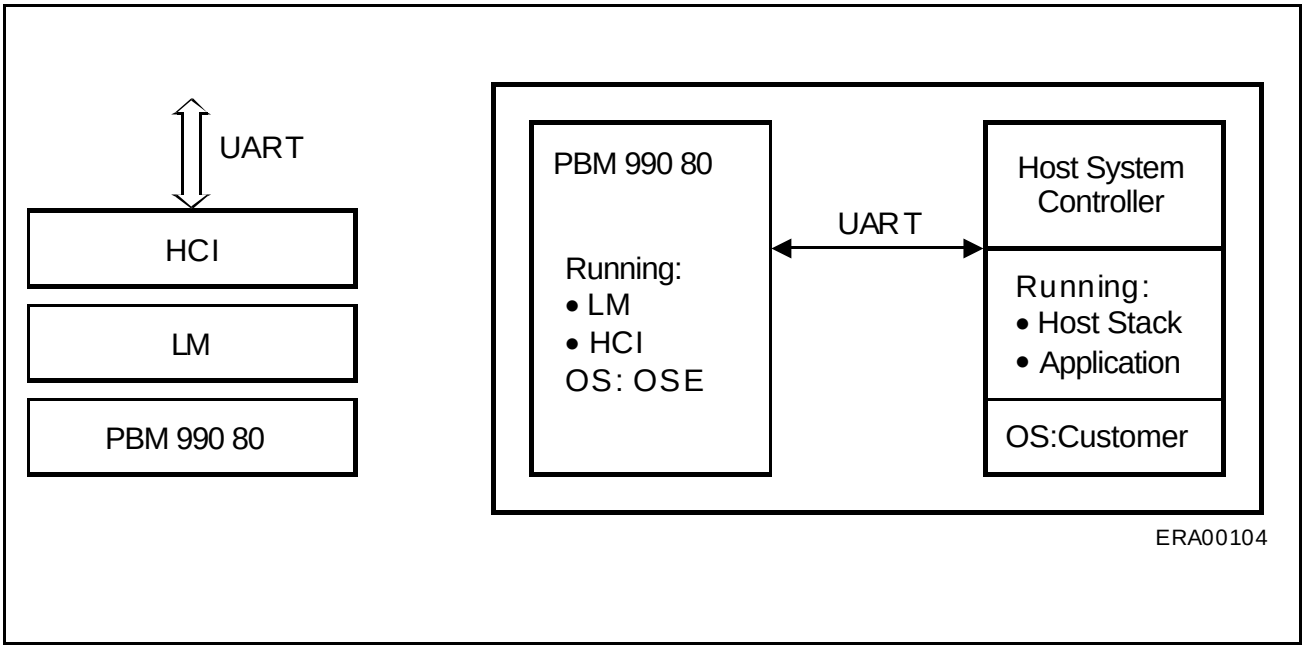


Figure 6 Host Controller Interface

3.5.5 Link Manager (LM)

The Link Manager in each Bluetooth module can communicate with another Link Manager by using the Link Manager Protocol (LMP) which is a peer to peer protocol, see **Figure 7**. The LMP messages have the highest priority and are used for link-setup, security, control and power saving modes. The receiving Link Manager filters out the message and does not need to acknowledge the message to the transmitting LM due to the reliable link provided by the Baseband and radio. LM to LM communication can take place without actions taken by the host. Discovery of features at other Bluetooth enabled devices nearby can be found and saved for later use by the host. Please refer to the Specification of the Bluetooth System v1.1 part C for in-depth information regarding the LMP.

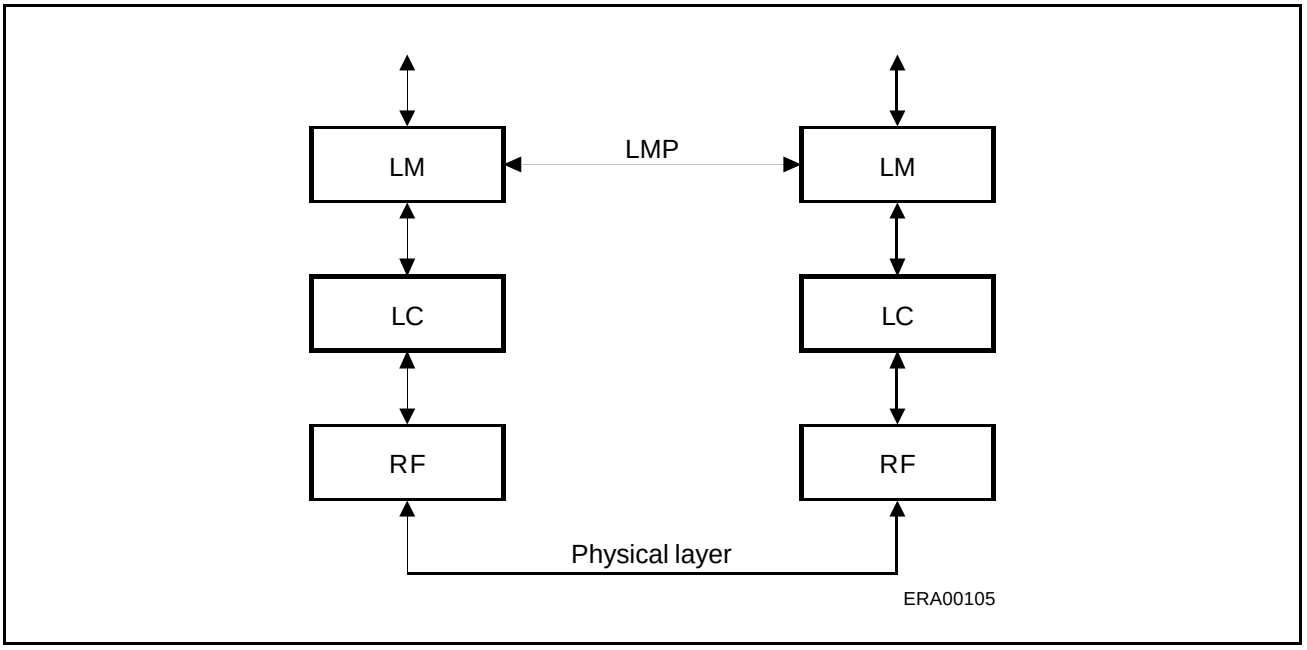


Figure 7 Link Manager

3.6 Design Guidelines

3.6.1 Power-up Sequence

There is no need for a power up sequence if V_{DD}, ON and V_{DD_IO} are tied together. A power up sequence, if used, shall be applied accordingly: GND, V_{DD_IO} supply rail, V_{DD} supply; and finally the ON signal should be applied in order to initiate the internal regulator.

The power-down sequence is similar to the power-up procedure but in the reverse format. Therefore, the disconnection of the signals shall be as follows: ON, V_{DD}, V_{DD_IO}, and finally GND.

3.6.2 RESET

The assignment of the $\overline{\text{RESET}}$ input is to generate a reset signal to ROK 104001. During power-up the reset signal is set ‘low’ so that power supply glitches are avoided. Therefore, no reset input is required after power-up.

3.6.3 Power

There are three inputs to the Voltage Management section (V_{DD}, V_{DD_IO}, ON). V_{DD} is the supply voltage that is typically 3.3 V.

A separate power supply rail (V_{DD_IO}) is provided for the I/O ports, UART and PCM. V_{DD_IO} can either be connected to V_{DD} or to a dedicated supply rail, which is the same as the logical interface of the host. The ON signal is controlling the internal regulators on or off.

An input capacitor whose capacitance is > 1 µF is required between the V_{DD} supply and ground (the amount of capacitance may be increased without limit), see **Figure 2**. This capacitor must be located as close as possible to the V_{DD} pad returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a Tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure that the capacitance will be > 1 µF over the entire operating temperature range.

3.6.4 Antenna

The antenna output routing should be 50 Ω (VSWR ≤ 2:1) all the way to the antenna in order to maintain the radio performance listed in this data sheet. For the routing underneath the module, the modules ground plane should be considered. The type approval for FCC and R&TTE have been done with an antenna gain of 1.6dBi.

3.6.5 Shielding / EMC Requirements

The module has its own RF shielding and is approved according to the standards by FCC and R&TTE. If the approval number is not visible on the outside when the module is utilised in the final product, an exterior label must state that there is a transmitter module inside the product (see Section 3.8).

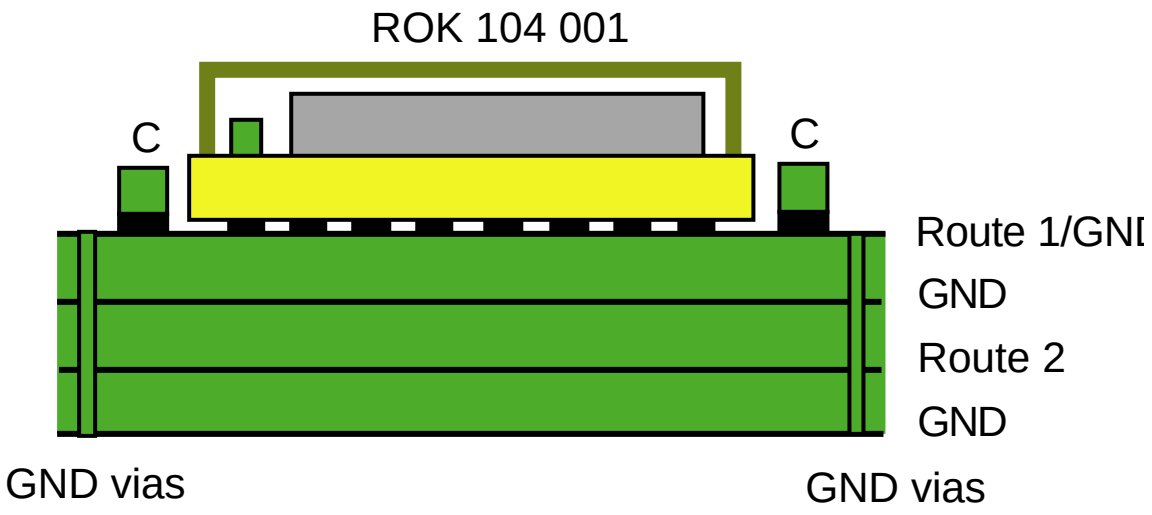


Figure 8 Side view of a recommended layout for a 4 layer PCB

Although the module has its own shielding extra precautionsregarding layout routing should be taken. It is strongly recommended that all the routing from the module shall be encapsulated between GND layers. Refer to figure 8 for an example with a 4-layer PCB.

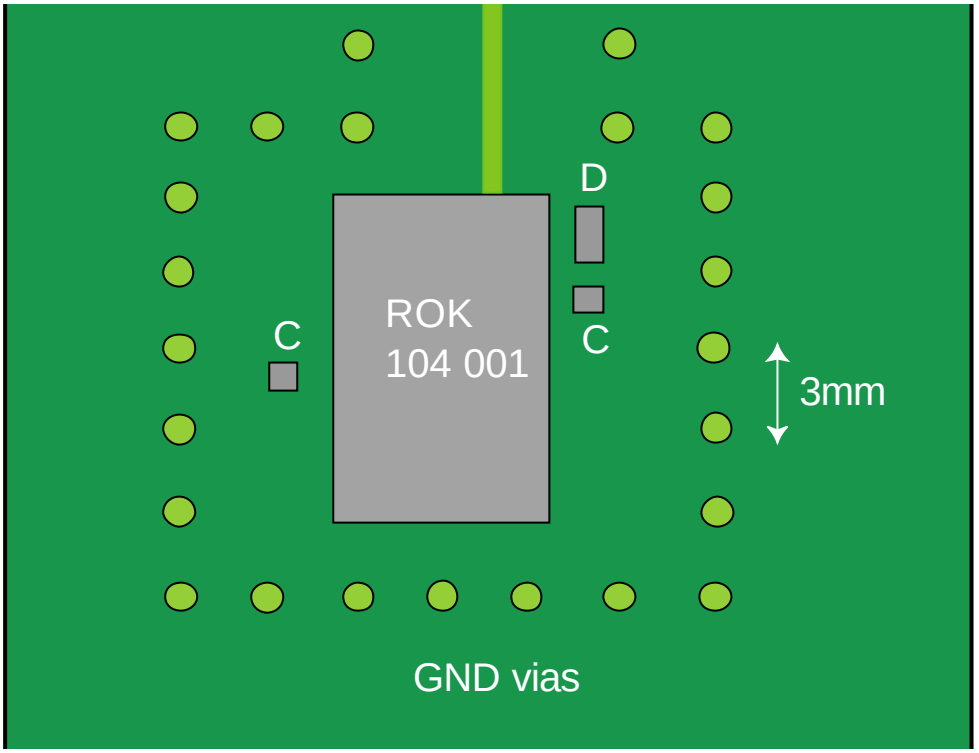


Figure 9 Top view of a recommended layout

Additionally, GND vias can be positioned around the module and its surrounding components so that any high frequency signal cannot effect any other part of the application board. This also protects the module from high frequency components that could be positioned in the near vicinity. It is recommended to have a distance of 3 mm between the earth vias. Refer to figure 9 as an example.

3.6.5.1 PCB Design Rules

As can be seen from figure10, the GND vias that surround the module should not have a large impact of the ability to route the signals to the module.

Total Thickness of PCB	1,6	3,2	mm
Via hole ø	0,3	0,6	mm
Catch Pad ø (Internal Layers)	0,7	1,2	mm
GND vias distance	3	3	mm

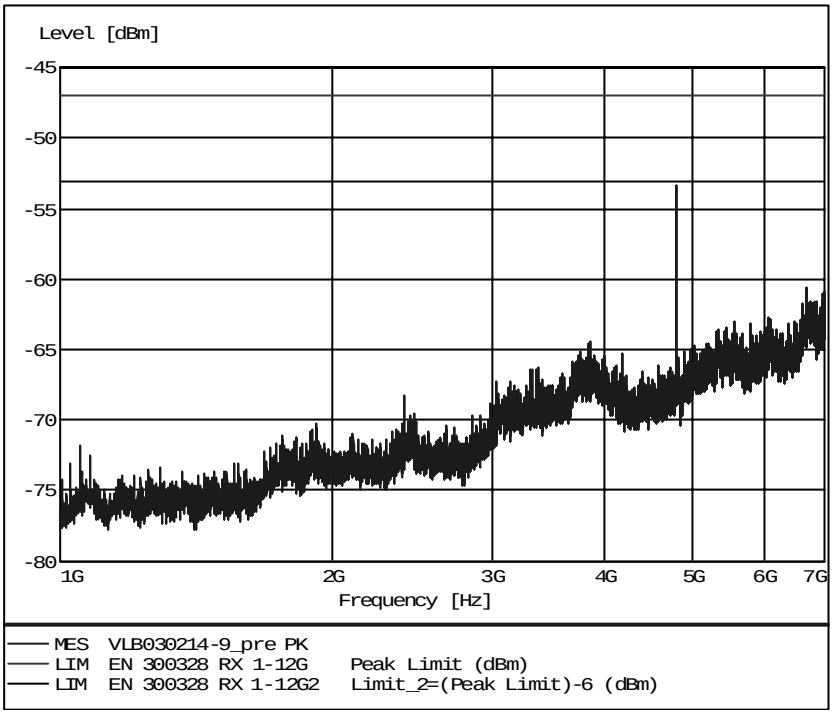
No. of possible tracks between GND vias	Maximum track width for 1.6mm thick PCB	Maximum track width for 3.2mm thick PCB	
1	767	600	um
2	460	360	um
3	329	257	um
4	256	200	um
5	209	164	um
6	177	138	um
7	153	120	um
8	135	106	um
9	121	95	um
10	110	86	um
11	100	78	um

Figure 10 Typical PCB layout design rules

3.6.5.2 Pad Size

It is recommended that the pads on the PCB should have a diameter of 0.7 - 0.9 mm. The surface finish on the PCB pads should be Nickel/Gold or a flat Tin/Lead surface or OSP (Organic Surface Protection).

3.6.5.3 Spurious Emissions Measurement



3.6.6 Ground

Ground should be distributed with very low impedance as a ground plane. Connect all GND pins to the ground plane.

3.6.7 Additional Decoupling

A capacitor whose capacitance of 2.2 µF is required between the V_{DD_RFDIG} output and ground, see block diagram **Figure 2**. This capacitor must be located as close as possible to the V_{DD_RFDIG} pad and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

3.6.8 Power Management Stop Mode

Note that from revision R2C of HCI-firmware and from R3B-revision of ECP-firmware, the Power Management stop mode is disabled by default. In order to enable this function, the 'HCI Command Store In Flash' has to be used (User ID: 131& Flash Data: 0001).

In order to utilize the power management stop mode features in the firmware; a schottky diode must be assembled between the DETACH pad and the EXTSYSWAKEUP pad,

see block diagram **Figure 2**. The cathode shall be assembled to DETACH and the anode to EXTSYSWAKEUP.

Power management stop mode is disabled by grounding the DETACH pin. A ‘high’ logical level will enable power management; a pull-up resistor is assembled on the module.

3.7 Assembly Guidelines

3.7.1 Solder Paste

The ROK 104001 module is made for surface mounting with land grid array (LGA) solder joints. To assemble the module, solder paste (eutectic Tin/Lead) must be printed at the target surface. Preferred solder paste height is 100 - 127 µm (4 - 5 mil).

3.7.2 Soldering Profile

It must be noted that the module should not be allowed to be hanging upside down in the reflow operation. This means that the module has to be assembled on the side of the PCB that is soldered last. The reflow process should be a regular surface mount soldering profile (full convection strongly preferred), the ramp-up should not be higher than 3°C/s and with a peak temperature of 210 - 225°C during 10 - 20 seconds. Max sloping rate should not be higher than 4°C/s (see example of reflow profile in **Figure 11**).

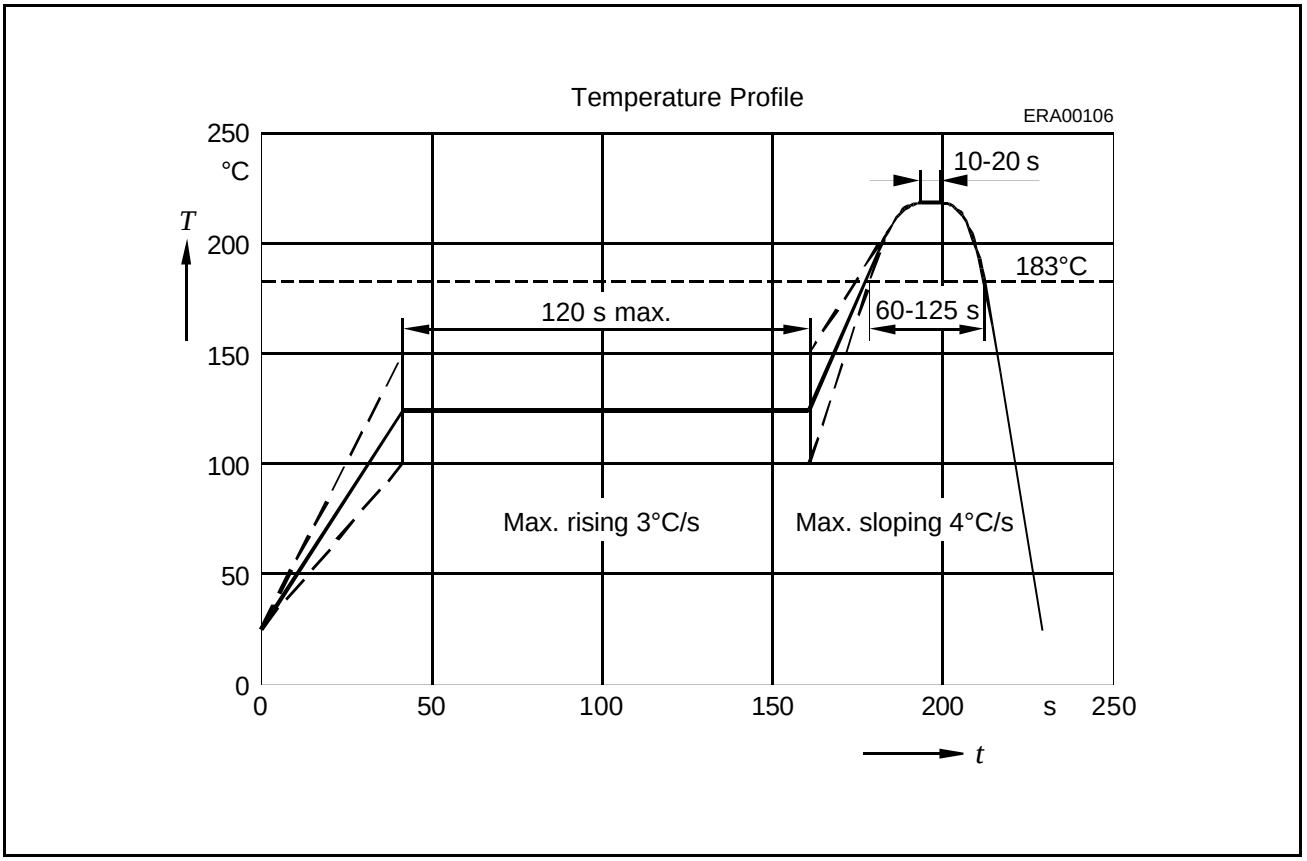


Figure 11 Eutectic SnPb-Solder Profile

3.7.3 Placement

The recommended pickup coordinates for the ROK 104001 shield is based on a nozzle with inner diameter 2 mm and outer diameter 3.17 mm. The center of the shield is the origin of coordinates, (0,0) for (x,y), giving the pickup coordinates (-1 mm,0) for (x,y).

3.7.4 Storage

Keep the component in its dry pack when not yet using the reel. After removal from the dry pack ensure that the modules are soldered onto the PCB within 48 hours.

3.8 FCC Modular Approval

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

The modular transmitter is labeled with its own FCC ID number, but, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. The exterior label can use wording such as the following: “Contains Transmitter Module FCC ID: Q23104001” or “Contains FCC ID: Q23104001”. Any similar wording that expresses the same meaning may be used.

When reusing the Modular Approval, antenna related measurements might need to be redone.The antenna used for modular approval was a max 1.6dBi half-wave antenna from gigAnt (PCB Swivel 6076019). When using an other antenna a class II permissive change will be needed.

3.9 R&TTE Approval

This device complies with the requirements in the European Union and EFTA according to the following test specifications:

EN 300 328

EN 60950 and EU standard

EN 301 489 -1/17

The R&TTE Approval for the ROK 104001-device is valid in the 19 member states of EU and EFTA. The R&TTE-organizations of respective member state must be given 4 weeks of notice before a product based on this approval is allowed to be released to market. Each state has its specific form to be filled in and submitted, for the respective R&TTE organization to respond to. In the absence of any response within four weeks, the product is allowed to be released to the market.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit
		min.	max.	
Temperature				
Storage temperature	T_{Stg}	-40	+125	°C
Maximum temperature		-40	+85	°C
Operating temperature		-20	+75	°C
Power Supply[1)]				
Supply voltage	V_{DD}	-0.3	5.25	V
Supply voltage (921k baud rate with turbo ON and ECP firmware)	V_{DD}	-0.3	4.75	V
I/O Supply voltage	V_{DD_IO}	-0.8	3.6	V
Baseband Digital I/Os				
IO voltage range	V_{IOP1}	-0.3	+2.8	V
IO voltage range	V_{IOP2}	-0.3	V_{DD_IO} + 0.3	V
Input clamp current $V_I < V_{SSIO}$ or $V_I > V_{DDIO}$	I_{IC}	-20	+20	mA
Output clamp current $V_O < V_{SSIO}$ or $V_O > V_{DDIO}$	I_{OC}	-20	+20	mA
Antenna Port				
Matching on ANT pad (VSWR)			10	NA
Input RF power - In-band - Out of band			15 15	dBm dBm

1) VDDIO supply voltage must be powered on prior to or simultaneously as the VDD supply voltage. Deviations from this power up sequence might damage the device.

4.2 DC Specifications

Table 4 DC Specifications

Unless otherwise noted, the specification applies for HCI firmware
T_{Amb} = -20 to +75°C, 3.10 < V_{DD} < 4.75 V, ON = 3.3V, VSWR ≤ 2[1)]

Parameter	Note/ Test Condition	Symbol	Values			Unit
			min.	typ.	max.	
Digital Inputs						
Low level input voltage, digital input	Guaranteed input low except ON signal	V_{IL_IOP1}	V_{SSIO} - 0.3		0.85	V
		V_{IL_IOP2}	V_{SSIO} - 0.3		0.3 x V_{DD_IO}	V
	ON signal only	V_{IL}	0		0.4	V
High level input voltage, digital input RESET#[2)]	Guaranteed input high except ON signal	V_{IH_IOP1}	1.96		2.8	V
		V_{IH_IOP}	0.7 x V_{DD_IO}		V_{DD_IO} + 0.3	V
	ON signal only	V_{IH}	1.4		VDD	V
Input pin internal pull-up resistor	(internal resistor on baseband chip)	R_{PU}	30	50	80	kΩ
Input pin internal pull-down resistor	(internal resistor on baseband chip)	R_{PD}	10	20	40	Ω
Digital Outputs						
Low level output voltage	I_{OL} = 800 µA	V_{OL}	0		V_{SSIO} + 0.1	V
High level output voltage	I_{OH} = -800 µA	V_{OH_IOP1}	2.4		2.8	V
		V_{OH_IOP2}	V_{DD_IO} - 0.1		V_{DD_IO}	V
Current Consumption						
Input leakage current, any digital input or bidirectional pin in input mode	V_I = V_{SSIO}		-1		+1	µA
	V_I = V_{DDIO}					
Output leakage current, tri-state	V_O = V_{SSIO}		-1		+1	µA
	V_O = V_{DDIO}					
HW Shutdown[3)]				65		µA

Table 4 **DC Specifications** (cont'd)
Unless otherwise noted, the specification applies for HCI firmware
T_{Amb} = -20 to +75°C, 3.10 < V_{DD} < 4.75 V, ON = 3.3V, VSWR ≤ 2[1)]

Parameter	Note/ Test Condition	Symbol	Values			Unit
			min.	typ.	max.	
Idle state with stop mode[4)]	during first 4 s.			1100		µA
	after 4 s.			270		µA
Page Scan with stop mode[5)]				3		mA
Inquiry and Page Scan with stop mode[5)]				3		mA
Hold mode[5)]	during first 4 s.			1100		µA
	after 4 s.			270		µA
Park mode[5)]				4.2		mA
Sniff mode[6)]				4.2		mA
Connection Mode[7)]	57600bps 460800bps or 921600bps with TURBO off[8)] 921600bps with TURBO on[8)]			93 100 125		mA mA mA
VDDIO supply	I_{CC_IO}			2		mA

1) Parameter errors may occur if VSWR > 2.
2) RESET# signal must be fed from an open drain output.
3) Current consumption is based upon where the 'ON' signal is low and 'VDDIO' is grounded.
4) After HCI command.
5) Inquiry and page mode current is measured during 1.28 s.
6) Sniff max & min interval: 1.28 s; Sniff attempt & Timeout: 19.375 ms.
7) Average current consumption measured during DH5 packet whilst in remote loop back configuration.
8) The HCI command turbo on has a typical throughput of 610 kbit/s but when the turbo command is off the baud rate is reduced to 510 kbit/s.

Table 5 Timing Performance

Type	Parameter/ Condition	Symbol	Values			Unit
			min.	typ.	max.	
Digital input pins requirements[1]						
All digital input and bi-directional input pins[2]	Rise time	*tr*			10	ns
	Fall time	*tr*			10	ns
Digital output pins characteristics[1]						
All digital output and bi-directional output pins[2]	Rise time C_{LOAD} = 25 pF	t_R	3.5		20	ns
	Fall time C_{LOAD} = 25 pF	t_F	3.5		15	ns
System						
Clock frequency		f_{SYS_CLK}		13.0000		MHz
Clock frequency tolerance[3]			-20		+20	ppm
Start-up time from power on				250		ms
RESET# signal duration[4]	Sink current > 1 mA			1		ms

1) Static data - All baseband input and bi-directional pins can be connected to any external driving circuit before turning on the supply, without damaging the device. However, it cannot be guaranteed that ROK 104001 does not load the external driver in this case, unless the baseband core supply voltage is completely discharged prior to this event.

2) Rise and fall times are measured between 10 % to 90 % of the V_{DDIO} level.

3) Tolerance for the system clock takes into account aging effects of the crystal.

4) RESET# signal must be fed from an open drain output.

Table 6 ACL Packets

Parameter	Condition	Values			Unit
		min.	typ.	max.	
Symmetric transfer rate	DM1 packet		108	108	kb/s
	DH1 packet		172	172	kb/s
	DM3 packet		258	258	kb/s
	DH3 packet		390	390	kb/s
	DM5 packet		286	286	kb/s
	DH5 packet		433	433	kb/s
Asymmetric transfer rate Forward mode	DM1 packet		108	108	kb/s
	DH1 packet		172	172	kb/s
	DM3 packet		387	387	kb/s
	DH3 packet		585	585	kb/s
	DM5 packet		477	477	kb/s
	DH5 packet[1)]		610	723	kb/s
Asymmetric transfer rate Reverse mode	DM1 packet		108	108	kb/s
	DH1 packet		172	172	kb/s
	DM3 packet		54	54	kb/s
	DH3 packet		86	86	kb/s
	DM5 packet		36	36	kb/s
	DH5 packet		57	57	kb/s

1) The HCI command turbo on has a typical throughput of 610 kbit/s but when the turbo command is off the baud rate is reduced to 510 kbit/s. HCI turbo on command is only valid during 921k UART baud rate.

Table 7 SCO Packets

Parameter	Condition	Values			Unit
		min.	typ.	max.	
Maximum transfer rate	HV1 packet		64.0		kb/s
	HV2 packet		64.0		kb/s
	HV3 packet		64.0		kb/s
	DV packet		57.6		kb/s

Table 8 PCM interface Requirements and Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
PCM Master mode (PCMCLK and PCMSYNC are outputs)					
PCM clock frequency	f_{PC}		2000		kHz
PCM clock high period	t_{PCH}	200			ns
PCM clock low period	t_{PCL}	200			ns
PCMSYNC pulse valid from PCMCLK rising edge	t_{PSV}			100	ns
PCMSYNC pulse hold time from PCMCLK falling edge	t_{PSH}	200			ns
PCMX data out valid from PCMCLK rising edge	t_{PDOV}			100	ns
PCMX data in setup time to PCMCLK falling edge	t_{PDIS}	100			ns
PCMX data in hold time from PCMCLK falling edge	t_{PIDH}	100			ns
PCM Slave mode (PCMCLK and PCMSYNC are inputs)					
PCM clock frequency	f_{PC}	200		2048	kHz
PCM clock high period	t_{PCH}	200			ns
PCM clock low period	t_{PCL}	200			ns
PCMSYNC setup time to PCMCLK falling edge	t_{PSS}	100			ns
PCMSYNC hold time from PCMCLK falling edge	t_{PSH}	100			ns
PCMSYNC pulse width	t_{PSW}			$1/f_{PC}$	ns
PCMX data out valid from PCMCLK rising edge	t_{PDOV}			100	ns
PCMX data in setup time to PCMCLK falling edge	t_{PDIS}	100			ns
PCMX data in hold time from PCMCLK falling edge	t_{PIDH}	100			ns

Table 9 RF Specifications

Parameter	Condition	Values			Unit
		min.	typ.	max.	
General					
Frequency range		2.402		2.480	GHz
Double sided IF bandwidth			1		MHz

Table 9 RF Specifications (cont'd)

Parameter	Condition	Values			Unit
		min.	typ.	max.	
Antenna load			50		Ω
VSWR	Rx mode		2:1		
VSWR [1]	Tx mode		2:1		
Receiver Performance					
Sensitivity level	DH1 Connection 160 kHz deviation w.r.t. BER < 0.1 %		-75	-71	dBm
Max input level		-20	+13		dBm
RSSi accuracy	P_{in} = -40 dBm	-6	0	+6	dB
	P_{in} = -60 dBm	-6	0	+6	dB
$C/I_{co\text{-}channel}$ [2) 3)]			12	14	dB
C/I_{1MHz} [2) 3)]			-3	0	dB
C/I_{2MHz} [2) 4)]			-35	-30	dB
$C/I_{>3MHz}$ [2) 4)]			-50	-30	dB
C/I_{image} [2) 4)]			-20	-9	dB
Adjacent (1 MHz) interference to inband image frequency $C/I_{image+/-1MHz}$ [2) 4)]			-30	-20	dB
Out-of-band blocking	30-1850 MHz	+5	+15		dBm
	1850-1910 MHz	+4	+15		dBm
	1911-2000 MHz	0	+9		dBm
	2001-2399 MHz	-27	-8		dBm
	2484-2999 MHz	-27	-9		dBm
	3.0-12.75 GHz	-10	+3		dBm
Intermodulation rejection [2) 5)]		-39	-30		dBm
Spurious emissions	30 MHz to 1 GHz			-57	dBm
	1 GHz to 12.75 GHz			-47	dBm
Transmitter Performance					
Frequency deviation		140	160	175	kHz
Tx power		-4	+1	+4	dBm
Initial frequency error		-75	0	75	kHz
20 dB bandwidth	with peak detector			1000	kHz

Table 9 RF Specifications (cont'd)

Parameter	Condition	Values			Unit
		min.	typ.	max.	
Tx carrier drift 2402 to 2482 MHz	1 slot (366 µs)	-25		25	kHz
	3 slots (1598 µs)	-40		40	kHz
	5 slots (2862 µs)	-40		40	kHz
Tx carrier drift 2480 to 2402 MHz	1 slot (366 µs)	-25		25	kHz
	3 slots (1598 µs)	-40		40	kHz
	5 slots (2862 µs)	-40		40	kHz
Drift rate		-20		20	kHz
Adjacent channel power	+2 MHz			-20	dBm
	-2 MHz			-20	dBm
	+3 MHz			-40	dBm
	-3 MHz			-40	dBm
	+4 MHz			-40	dBm
	-4 MHz			-40	dBm
	+13 MHz			-40	dBm
	-13 MHz			-40	dBm
Spurious emissions	30 MHz - 1 GHz			-36	dBm
	1 GHz - 12.75 GHz			-30	dBm
	1.8 GHz - 1.9 GHz			-47	dBm
	5.15 GHz - 5.3 GHz			-47	dBm

1) During the Tx mode, the VSWR specification states the limits that are acceptable before any other RF parameters are strongly affected, i.e. frequency deviation and drift.
2) Specification only valid for normal test conditions T_{AMB} = 15 - 35 C.
3) Carrier signal level of -60 dBm, interferer Bluetooth modulated.
4) Carrier signal level of -67 dBm, interferer Bluetooth modulated.
5) Carrier: -64 dBm @ 2441 MHz, 1st interferer: CW @ 2446 MHz, 2nd interferer: BT mod. @ 2451 MHz.

5 Marking

5.1 Module Marking

Each module shall be marked with the following information printed on the shield.

Table 10

Marking	Description
1: 	Infineon logotype
2: <ROK 104001/21 R1A>	Product number with suffix and revision state acc to purchase order
3: <bbbbbb>	Batch number
4: <yyww2>	Manufacturing year (yy), week (ww) and factory code (2)
5: 	Bluetooth logotype.
6: 	CE-logo.
7:**FCC ID: Q23104001**	FCC No.

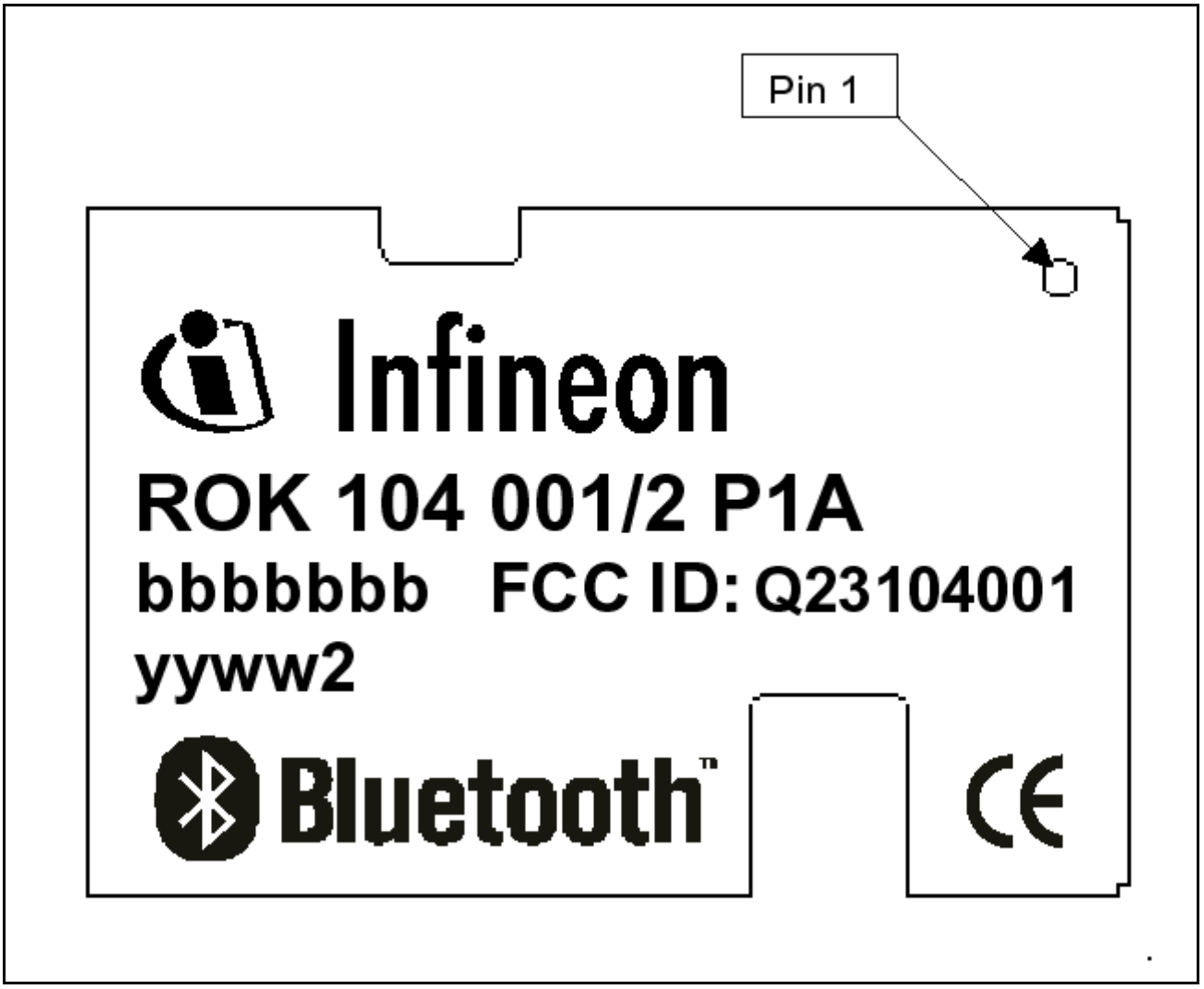


Figure 12 Module Marking

5.2 Reel Marking

The reel, reel box and dry pack has a label with the following information:

- Infineon product number with revision
- Customer product number with revision
- Quantity
- Reel-ID. (Batch No)
- Factory code
- Manufacturing date
- Country of origin
- Infineon logotype

1-6 above is also printed in BAR-code format

6 Package Outlines

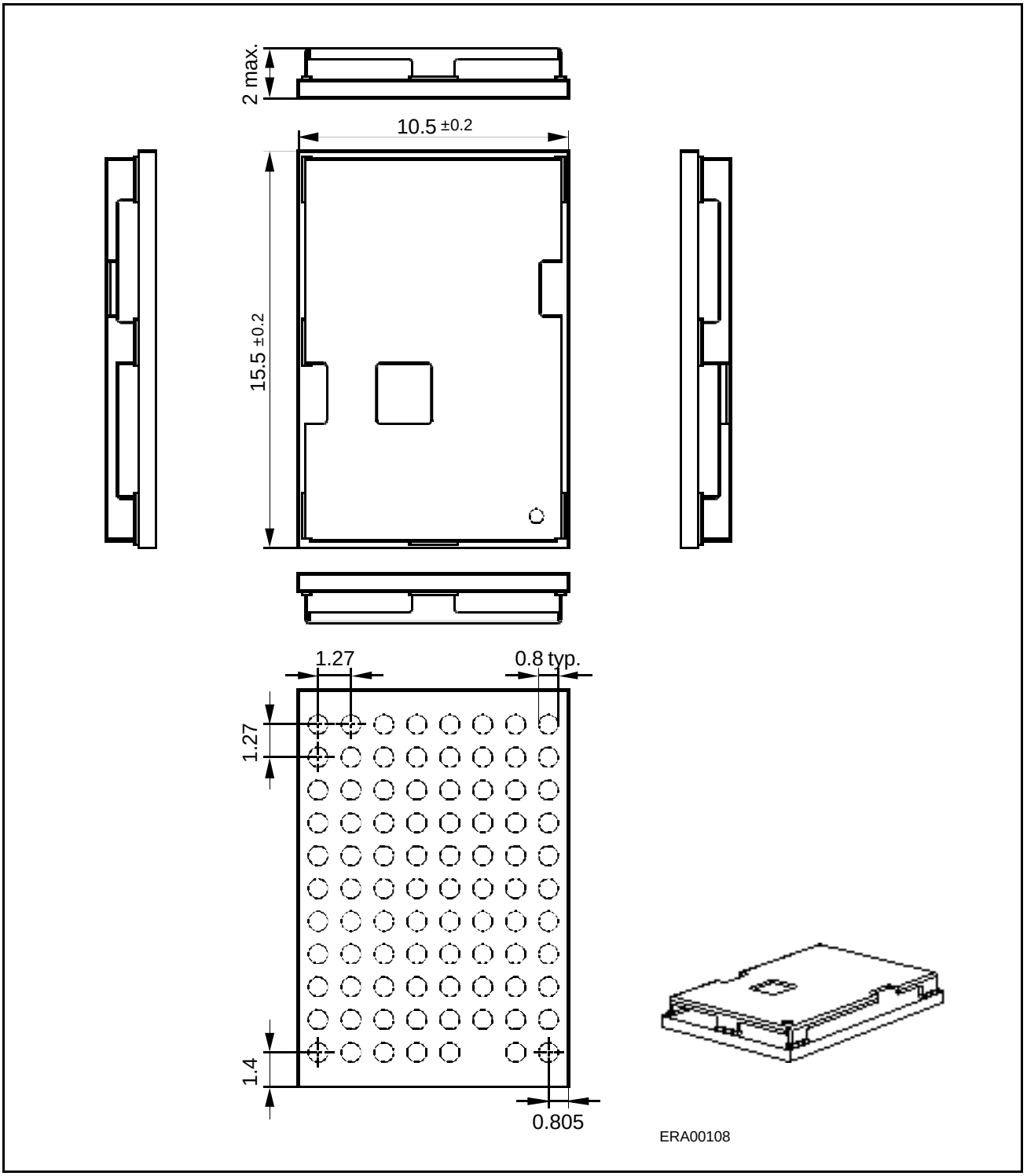


Figure 13 ROK 104 001 Mechanical Dimensions (maximum values) and Footprint, Bottom View

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

6.1 Pinout (bottom view)

Please refer to **Figure 4** for the positioning of each pad.

Table 11

7	GND	N.C.	N.C.	N.C.	VDD_RF DIG	GND	N.C.	N.C.	N.C.	N.C.	GND
6	GND	SERIAL DATA	GPIOB7	GPIOB6	N.C. - VTP3	N.C. - VTP4	GND	GND	GND	GND	GND
5	GND	N.C. - VTP1	PWRFAIL	N.C. - VTP2	UART2RTS	PWRAV AIL	N.C.	N.C.	V_{DD}	GND	GND
4	GND	N.C.	GPIOB2	DETACH	GPIOB4	N.C.	GND	UART1Tx	V_{DDIO}	ON	N.C.
3	GND	GND	RESET	SERIAL CLK	GPIOB5	UART1Rx	WAKEUP	UART1RTS	UART1CTS	D+	N.C.
2		ANT	GND	EXTSYS WAKEUP	UART2Rx	EXTINT	PCMSYNC	N.C.	UART2CTS	D-	GND
1	GND	GND	GND	GPIOB3	PCMTX	PCMCLK	PCMRx	N.C.	UART2Tx	GND	GND
0	GND	N.C.	N.C. - VTP5	N.C.	N.C.	GND	N.C.	N.C.	N.C.	N.C.	GND
	V	**T**	**R**	**P**	**N**	**M**	**L**	**K**	**J**	**H**	**G**

6.2 Footprint, Land View

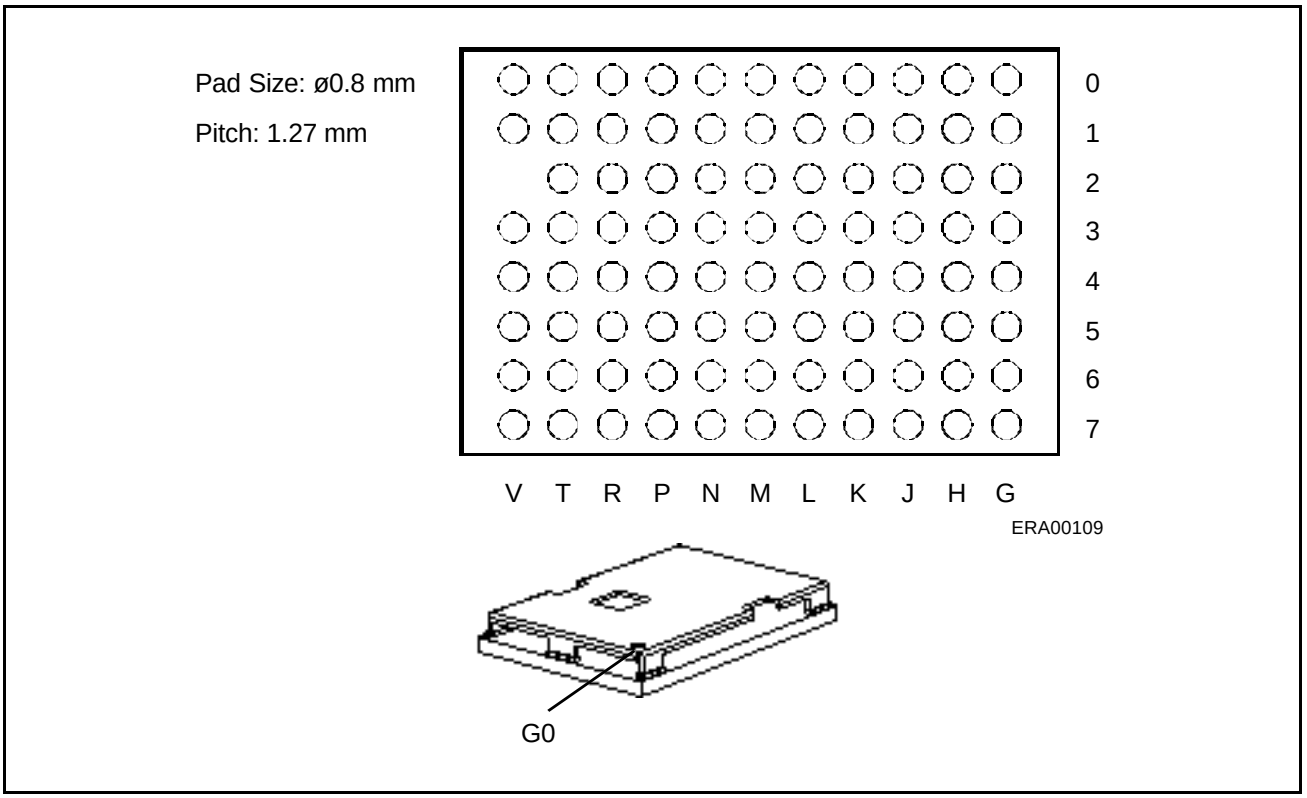


Figure 14 ROK 104 001 Mechanical Dimensions of Footprint, Land Pattern View (seen from above the component)

7 Ordering Information

Please contact Infineon Technologies for further information.

8 Packaging

The modules will be delivered in a tape & reel and dry pack, protecting them from ESD and mechanical shock.

The tape width is 24 mm and the pitch is 12 mm. The diameter of the reel is 13 inches and it contains 1500 modules.

9 Abbreviations

ASIC	- Application Specific Integrated Circuit
BER	- Bit Error Rate
CMOS	- Complementary Metal Oxide Semiconductor
DCE	- Data Circuit terminating Equipment
HCI	- Host Controller Interface
IC	- Integrated Circuit
ISM	- Industrial Scientific and Medical
LGA	- Land Grid Array
PCB	- Printed Circuit Board
PCM	- Pulse Code Modulation
Rx	- Receive
SIG	- Special Interest Group
Tx	- Transmit
UART	- Universal Asynchronous Receiver Transmitter
USB	- Universal Serial Bus