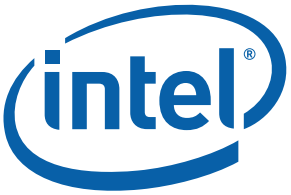

Intel® Xeon ® Processor E3-1200 Product Family and LGA 1155 Socket

Thermal / Mechanical Specifications and Design Guidelines

April 2011

Document Number: 324973-001

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Contents

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Revision History

Document Number	Description	Date
324973-001	• Initial release of the document.	April 2011

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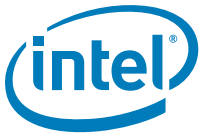

1 Introduction

This document is intended to provide guidelines for design of thermal and mechanical solution. Meanwhile thermal and mechanical specifications for the processor and associated socket are included.

The components described in this document include:

- The thermal and mechanical specifications for the following Intel® server/ workstation processors:
  - — Intel® Xeon® processor E3-1200 product family
- The LGA1155 socket and the Independent Loading Mechanism (ILM) and back plate.
- The collaboration/reference design thermal solution (heatsink) for the processors and associated retention hardware.

The Intel® Xeon® Processor E3-1200 product family has the different thermal specifications. When required for clarity this document will use:

- Intel® Xeon® processor E3-1280 (95W)
- Intel® Xeon® processor E3-1200 (80W)
- Intel® Xeon® processor E3-1200 series (95W) with integrated graphics
- Intel® Xeon® processor E3-1260L (45W)
- Intel® Xeon® processor E3-1220L (20W)

Note: When the information is applicable to all products the this document will use "processor" or "processors" to simplify the document.

1.1 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

Document	Location	Notes
Intel® Xeon® Processor E3-1200 Family Data Sheet Volume One	http://www.intel.com/Assets/PDF/datasheet/324970.pdf	
Intel® Xeon® Processor E3-1200 Family Datasheet Volume Two	http://www.intel.com/Assets/PDF/datasheet/324971.pdf	
Intel® Xeon® Processor E3-1200 Family Specification Update	http://www.intel.com/Assets/PDF/specupdate/324972.pdf	
4-Wire Pulse Width Modulation (PWM) Controlled Fans	Available at http://www.formfactors.org/	

1.2 Definition of Terms

Table 1-2. Terms and Descriptions (Sheet 1 of 2)

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
CTE	Coefficient of Thermal Expansion. The relative rate a material expands during a thermal event.
DTS	Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.
FSC	Fan Speed Control
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
ILM	Independent Loading Mechanism provides the force needed to seat the 1155-LGA land package onto the socket contacts.
PCH	Platform Controller Hub. The PCH is connected to the processor via the Direct Media Interface (DMI) and Intel® Flexible Display Interface (Intel® FDI).
LGA1155 socket	The processor mates with the system board through this surface mount, 1155-land socket.
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
Ψ_{CA}	Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as ($T_{CASE} - T_{LA}$) / Total Package Power. The heat source should always be specified for Ψ measurements.
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as ($T_{CASE} - T_S$) / Total Package Power.
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as ($T_S - T_{LA}$) / Total Package Power.
T_{CASE} or T_C	The case temperature of the processor, measured at the geometric center of the topside of the TTV IHS.

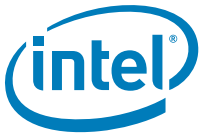

Table 1-2. Terms and Descriptions (Sheet 2 of 2)

Term	Description
T_{CASE_MAX}	The maximum case temperature as specified in a component specification.
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	Tcontrol is a static value that is below the TCC activation temperature and used as a trigger point for fan speed control. When DTS > Tcontrol, the processor must comply to the TTV thermal profile.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
Thermal Profile	Line that defines case temperature specification of the TTV at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.
TTV	Thermal Test Vehicle. A mechanically equivalent package that contains a resistive heater in the die to evaluate thermal solutions.
T_{LA}	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.

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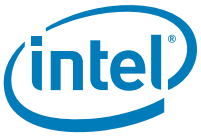


2 Package Mechanical & Storage Specifications

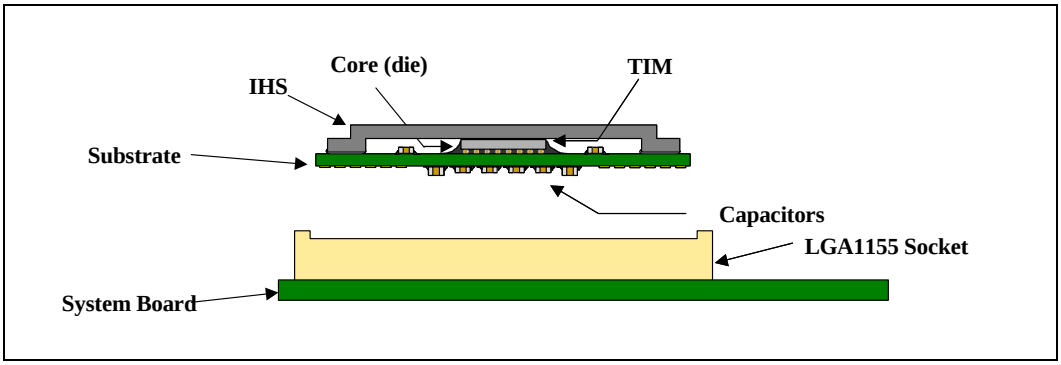
2.1 Package Mechanical Specifications

The processor is packaged in a Flip-Chip Land Grid Array package that interfaces with the motherboard via the LGA1155 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor thermal solutions, such as a heatsink. Figure 2-1 shows a sketch of the processor package components and how they are assembled together. Refer to Chapter 3 and Chapter 4 for complete details on the LGA1155 socket.

The package components shown in Figure 2-1 include the following:

1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM)
3. Processor core (die)
4. Package substrate
5. Capacitors

Figure 2-1. Processor Package Assembly Sketch



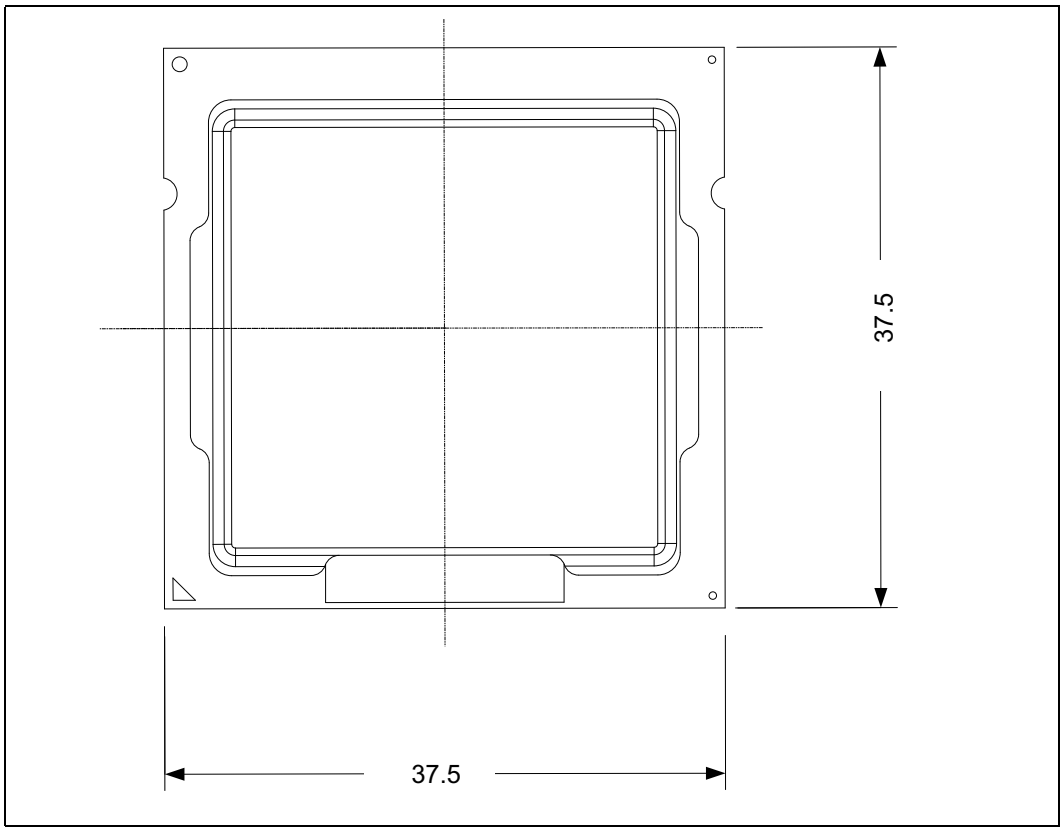
Note:
1. Socket and motherboard are included for reference and are not part of processor package.
2. For clarity the ILM not shown.

2.1.1 Package Mechanical Drawing

Figure 2-2 shows the basic package layout and dimensions. The detailed package mechanical drawings are in Appendix D. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

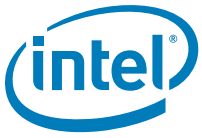
1. Package reference with tolerances (total height, length, width, and so on)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datums
6. All drawing dimensions are in mm.

Figure 2-2. Package View



2.1.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure B-3 and Figure B-4 for keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in. This keep-in zone includes solder paste and is a post reflow maximum height for the components.



2.1.3 Package Loading Specifications

Table 2-1 provides dynamic and static load specifications for the processor package. These mechanical maximum load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution.

Table 2-1. Processor Loading Specifications

Parameter	Minimum	Maximum	Notes
Static Compressive Load	-	600 N [135 lbf]	1, 2, 3
Dynamic Compressive Load	-	712 N [160 lbf]	1, 3, 4

Notes:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. Dynamic loading is defined as an 50g shock load, 2X Dynamic Acceleration Factor with a 500g maximum thermal solution.

2.1.4 Package Handling Guidelines

Table 2-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 2-2. Package Handling Guidelines

Parameter	Maximum Recommended	Notes
Shear	311 N [70 lbf]	1, 4
Tensile	111 N [25 lbf]	2, 4
Torque	3.95 N-m [35 lbf-in]	3, 4

Notes:
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization.

2.1.5 Package Insertion Specifications

The processor can be inserted into and removed from an LGA1155 socket 15 times. The socket should meet the LGA1155 socket requirements detailed in Chapter 5.

2.1.6 Processor Mass Specification

The typical mass of the processor is 21.5 g (0.76 oz). This mass [weight] includes all the components that are included in the package.

2.1.7 Processor Materials

Table 2-3 lists some of the package components and associated materials.

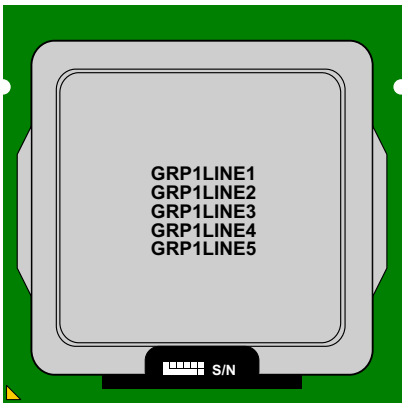
Table 2-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

2.1.8 Processor Markings

Figure 2-3 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 2-3. Processor Top-Side Markings



Sample (QDF):

GRP1LINE1: i{M}{C}YY
GRP1LINE2: INTEL CONFIDENTIAL
GRP1LINE3: QDF ES SPEED
GRP1LINE4: COUNTRY OF ORIGIN
GRP1LINE5: {FPO} {e4}

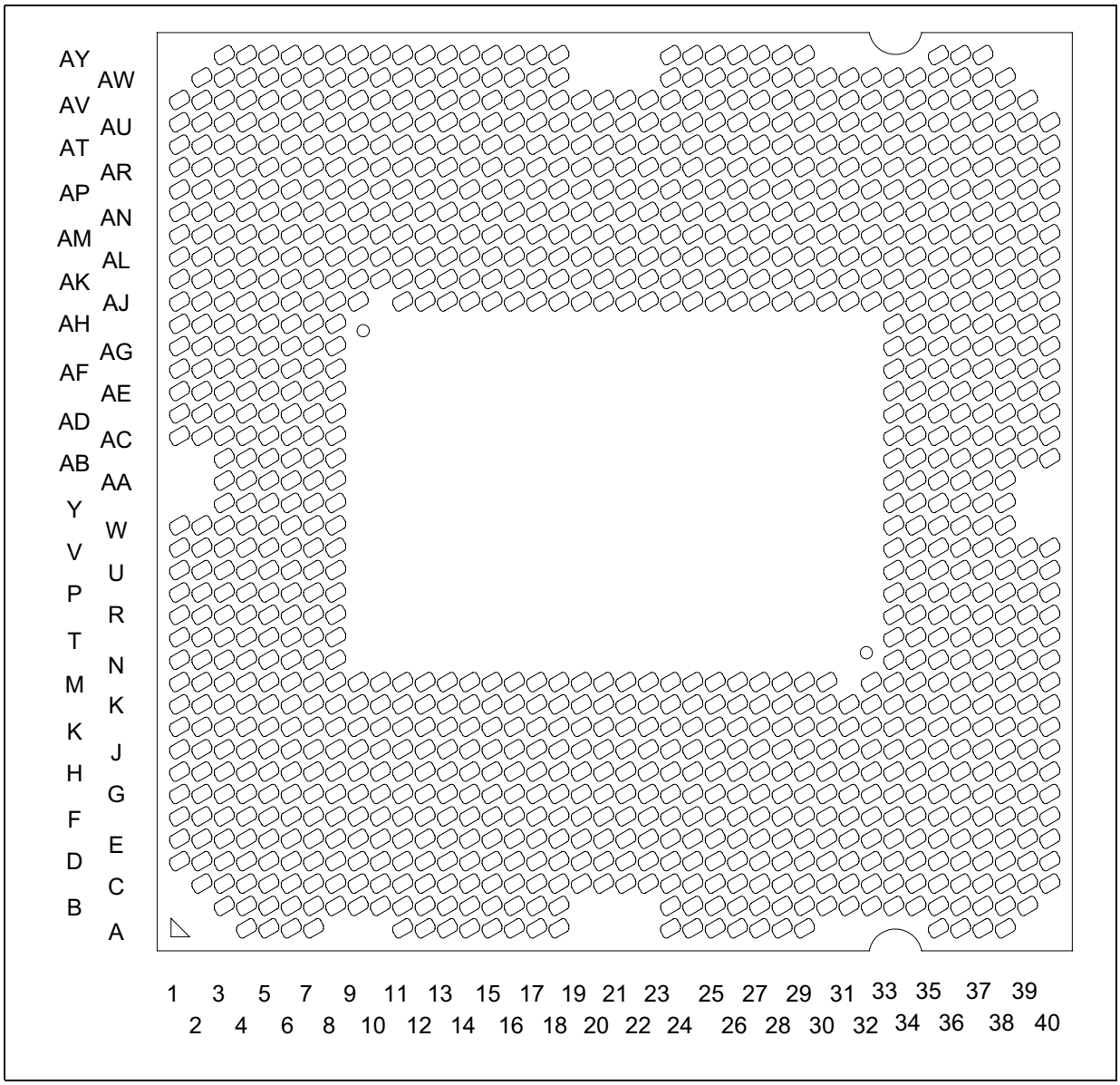
Production (SSPEC):

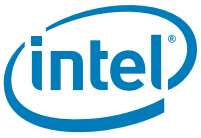
GRP1LINE1: i{M}{C}YY
GRP1LINE2: BRAND PROC#
GRP1LINE3: SSPEC SPEED
GRP1LINE4: COUNTRY OF ORIGIN
GRP1LINE5: {FPO} {e4}

2.1.9 Processor Land Coordinates

Figure 2-4 shows the bottom view of the processor package.

Figure 2-4. Processor Package Lands Coordinates





2.2 Processor Storage Specifications

Table 2-4 includes a list of the specifications for device storage in terms of maximum and minimum temperatures and relative humidity. These conditions should not be exceeded in storage or transportation.

Table 2-4. Storage Conditions

Parameter	Description	Min	Max	Notes
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.	-55 °C	125 °C	1, 2, 3
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5
$RH_{SUSTAINED\ STORAGE}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C		5, 6
$TIME_{SUSTAINED\ STORAGE}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	6 Months	6

Notes:

1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard Non-adherence may affect processor reliability.
3. $T_{ABSOLUTE\ STORAGE}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C, Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{SUSTAINED\ STORAGE}$ and customer shelf life in applicable intel box and bags.

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3 LGA1155 Socket

This chapter describes a surface mount, LGA (Land Grid Array) socket intended for the processors. The socket provides I/O, power and ground contacts. The socket contains 1155 contacts arrayed about a cavity in the center of the socket with lead-free solder balls for surface mounting on the motherboard.

The contacts are arranged in two opposing L-shaped patterns within the grid array. The grid array is 40 x 40 with 24 x 16 grid depopulation in the center of the array and selective depopulation elsewhere.

The socket must be compatible with the package (processor) and the Independent Loading Mechanism (ILM). The ILM design includes a back plate which is integral to having a uniform load on the socket solder joints. Socket loading specifications are listed in Chapter 5.

Figure 3-1. LGA1155 Socket with Pick and Place Cover

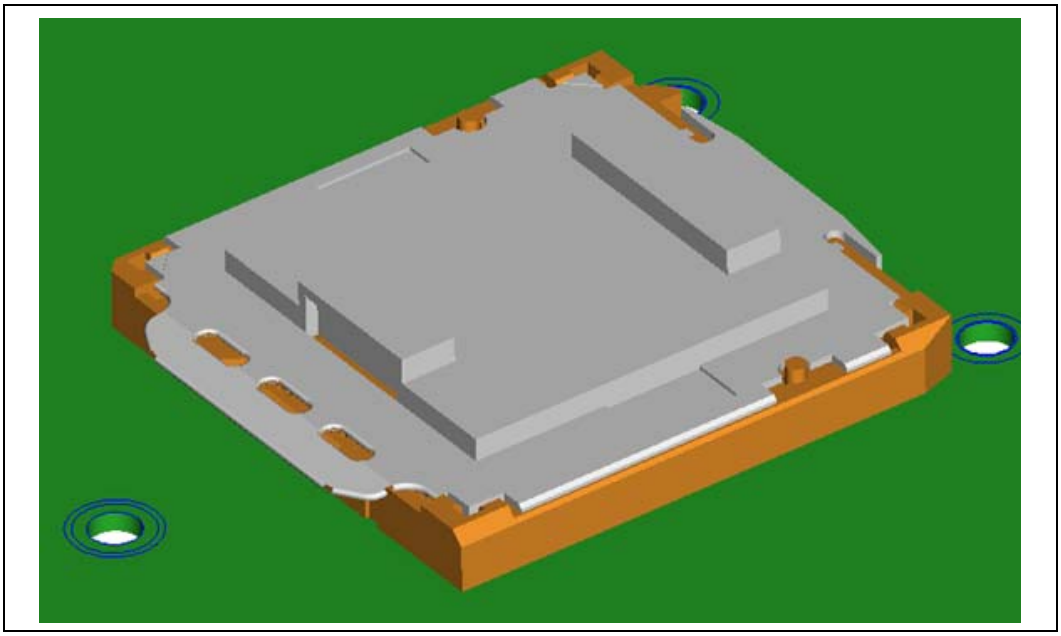
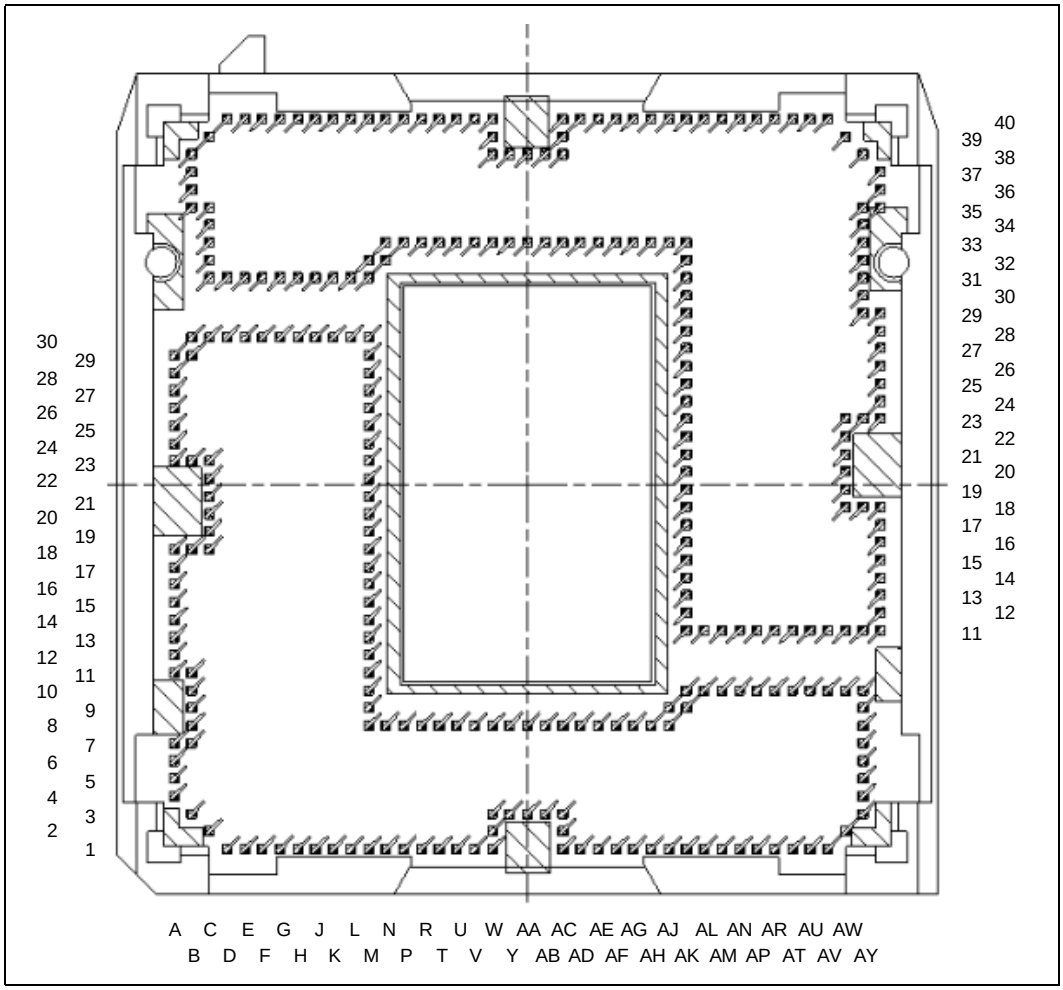


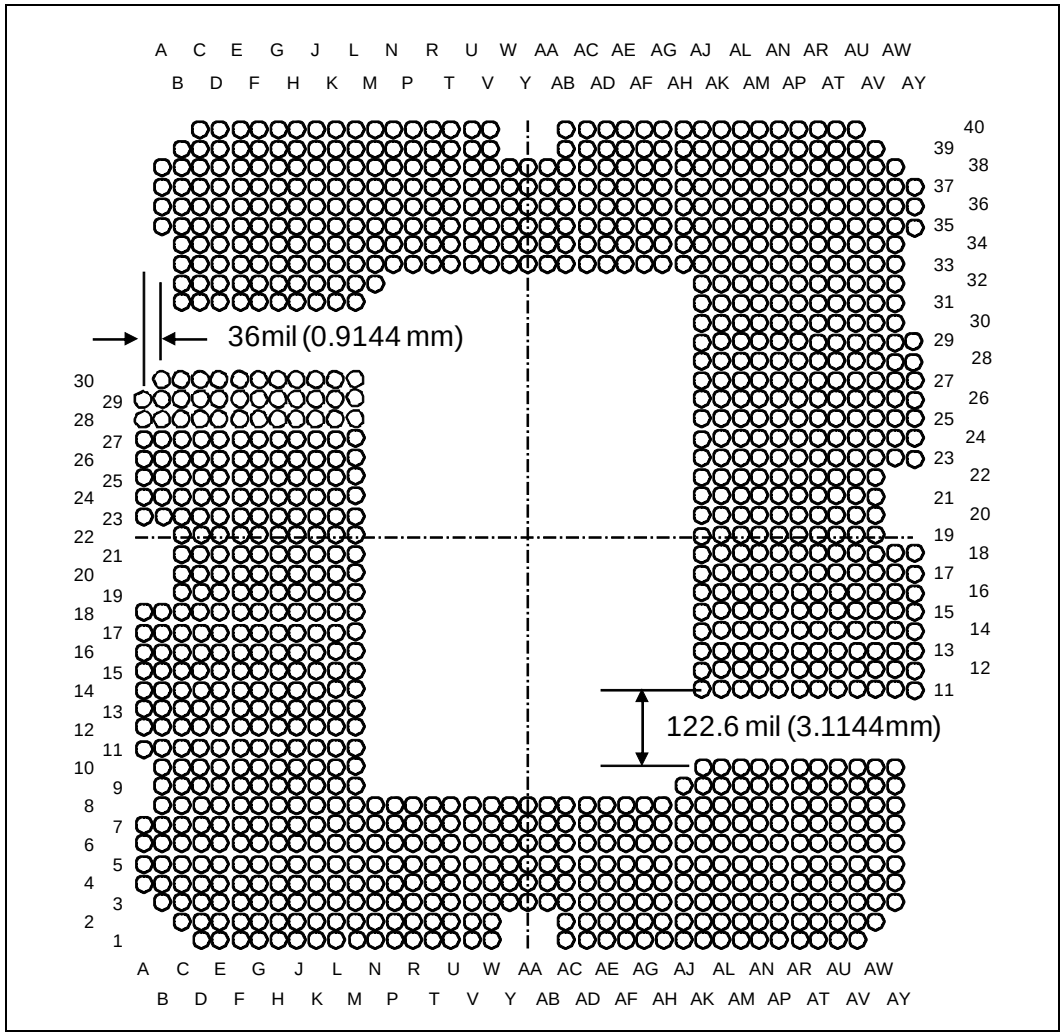
Figure 3-2. LGA1155 Socket Contact Numbering (Top View of Socket)



3.1 Board Layout

The land pattern for the LGA1155 socket is 36 mils X 36 mils (X by Y) within each of the two L-shaped sections. Note that there is no round-off (conversion) error between socket pitch (0.9144 mm) and board pitch (36 mil) as these values are equivalent. The two L-sections are offset by 0.9144 mm (36 mil) in the x direction and 3.114 mm (122.6 mil) in the y direction, see Figure 3-3. This was to achieve a common package land to PCB land offset which ensures a single PCB layout for socket designs from the multiple vendors.

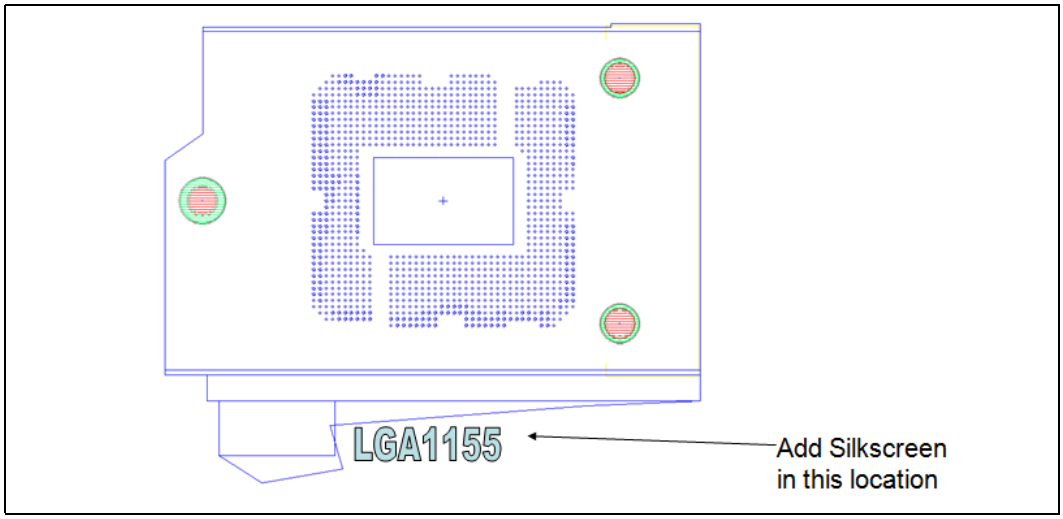
Figure 3-3. LGA1155 Socket Land Pattern (Top View of Board)



3.1.1 Suggested Silkscreen Marking for Socket Identification

Intel is recommending that customers mark the socket name approximately where shown in Figure 3-4.

Figure 3-4. Suggested Board Marking

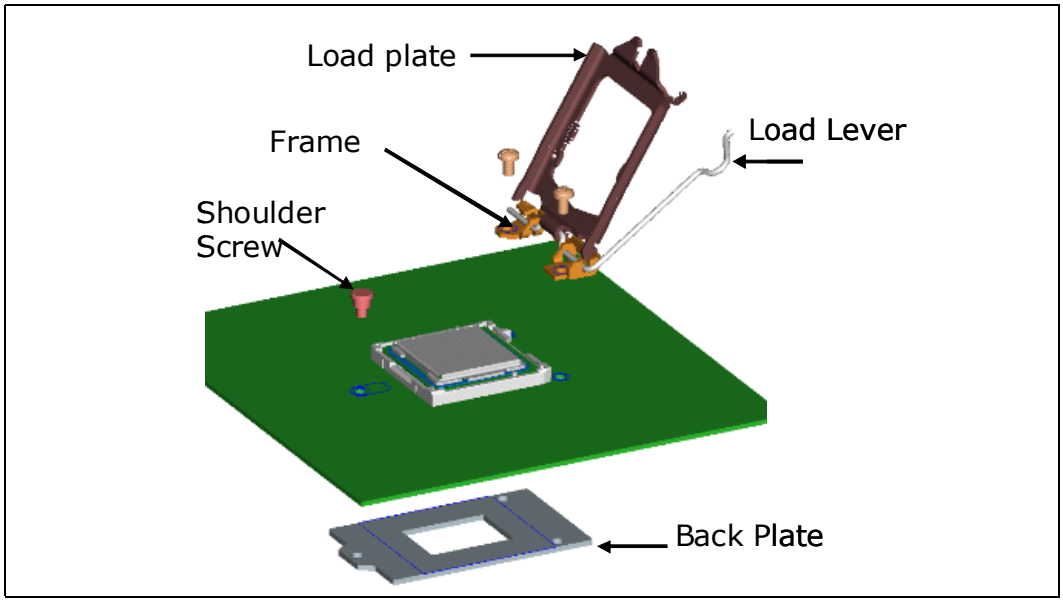


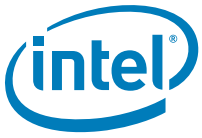
3.2 Attachment to Motherboard

The socket is attached to the motherboard by 1155 solder balls. There are no additional external methods (that is, screw, extra solder, adhesive, and so on) to attach the socket.

As indicated in Figure 3-1, the Independent Loading Mechanism (ILM) is not present during the attach (reflow) process.

Figure 3-5. Attachment to Motherboard





3.3 Socket Components

The socket has two main components, the socket body and Pick and Place (PnP) cover, and is delivered as a single integral assembly. Refer to Appendix C for detailed drawings.

3.3.1 Socket Body Housing

The housing material is thermoplastic or equivalent with UL 94 V-0 flame rating capable of withstanding 260 °C for 40 seconds which is compatible with typical reflow/rework profiles. The socket coefficient of thermal expansion (in the XY plane), and creep properties, must be such that the integrity of the socket is maintained for the conditions listed in Chapter 5.

The color of the housing will be dark as compared to the solder balls to provide the contrast needed for pick and place vision systems.

3.3.2 Solder Balls

A total of 1155 solder balls corresponding to the contacts are on the bottom of the socket for surface mounting with the motherboard. The socket solder ball has the following characteristics:

- Lead free SAC (SnAgCu) 305 solder alloy with a silver (Ag) content between 3% and 4% and a melting temperature of approximately 217 °C. The alloy is compatible with immersion silver (ImAg) and Organic Solderability Protectant (OSP) motherboard surface finishes and a SAC alloy solder paste.
- Solder ball diameter 0.6 mm ± 0.02 mm, before attaching to the socket lead.

The co-planarity (profile) and true position requirements are defined in Appendix C.

3.3.3 Contacts

Base material for the contacts is high strength copper alloy.

For the area on socket contacts where processor lands will mate, there is a 0.381 µm [15 µinches] minimum gold plating over 1.27 µm [50 µinches] minimum nickel underplate.

No contamination by solder in the contact area is allowed during solder reflow.

3.3.4 Pick and Place Cover

The cover provides a planar surface for vacuum pick up used to place components in the Surface Mount Technology (SMT) manufacturing line. The cover remains on the socket during reflow to help prevent contamination during reflow. The cover can withstand 260 °C for 40 seconds (typical reflow/rework profile) and the conditions listed in Chapter 5 without degrading.

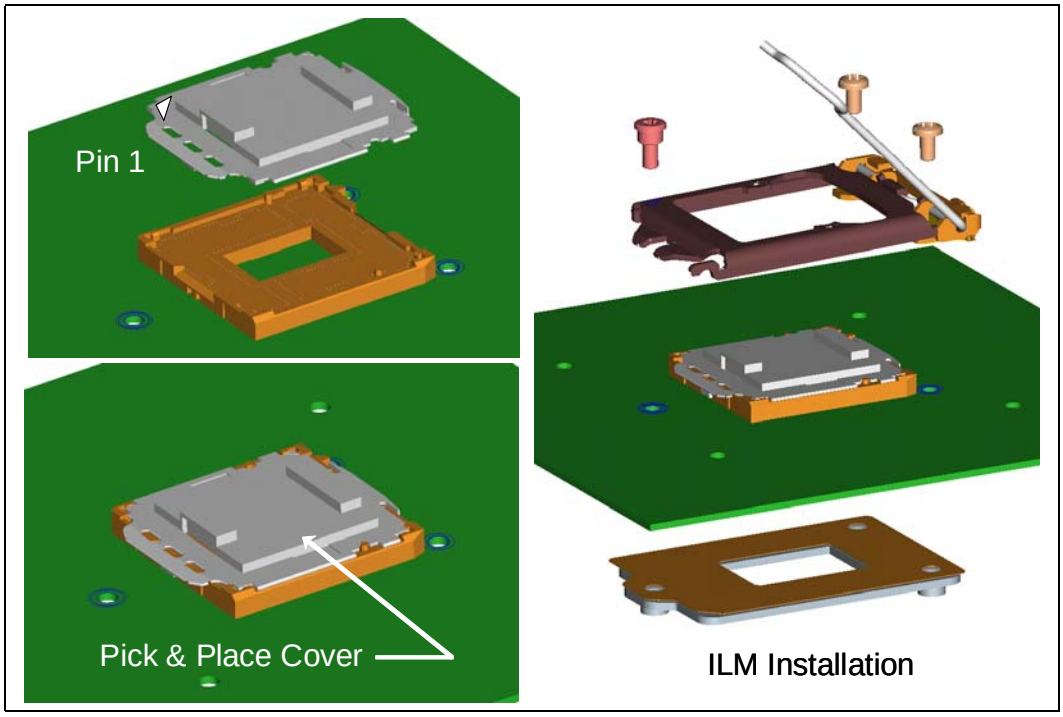
As indicated in Figure 3-6, the cover remains on the socket during ILM installation, and should remain on whenever possible to help prevent damage to the socket contacts.

Cover retention must be sufficient to support the socket weight during lifting, translation, and placement (board manufacturing), and during board and system shipping and handling. PnP Cover should only be removed with tools, to prevent the cover from falling into the contacts.

The socket vendors have a common interface on the socket body where the PnP cover attaches to the socket body. This should allow the PnP covers to be compatible between socket suppliers.

As indicated in Figure 3-6, a Pin 1 indicator on the cover provides a visual reference for proper orientation with the socket.

Figure 3-6. Pick and Place Cover



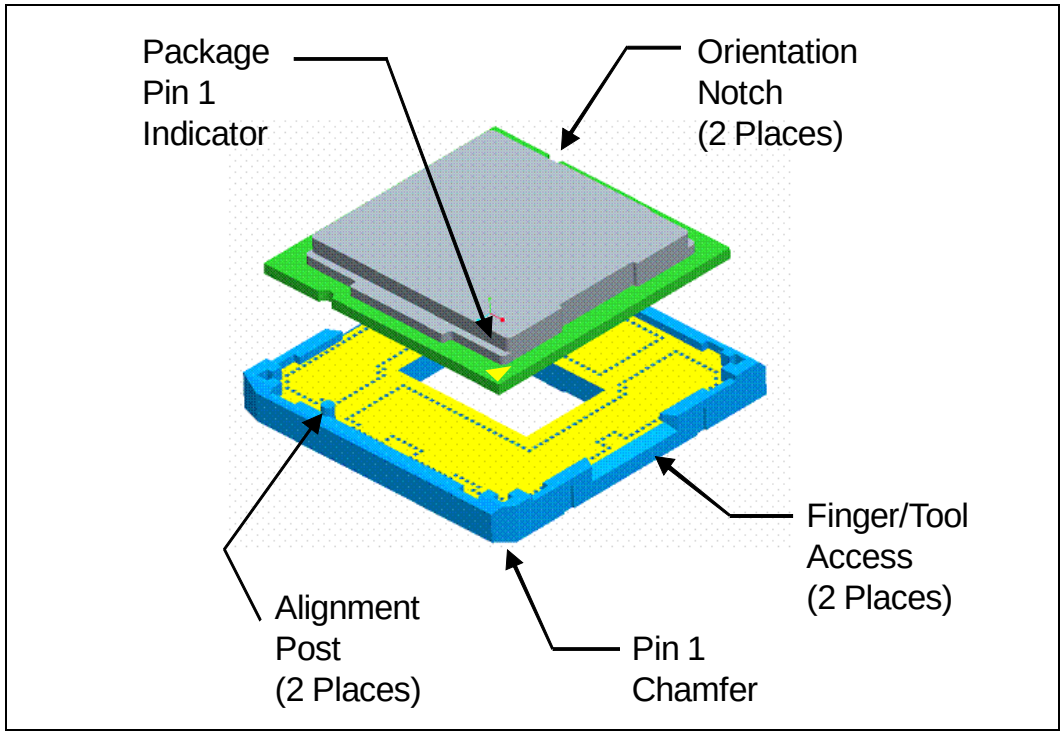
3.4 Package Installation / Removal

As indicated in Figure 3-7, access is provided to facilitate manual installation and removal of the package.

To assist in package orientation and alignment with the socket:

- The package Pin1 triangle and the socket Pin1 chamfer provide visual reference for proper orientation.
- The package substrate has orientation notches along two opposing edges of the package, offset from the centerline. The socket has two corresponding orientation posts to physically prevent mis-orientation of the package. These orientation features also provide initial rough alignment of package to socket.
- The socket has alignment walls at the four corners to provide final alignment of the package.

Figure 3-7. Package Installation / Removal Features



3.4.1 Socket Standoffs and Package Seating Plane

Standoffs on the bottom of the socket base establish the minimum socket height after solder reflow and are specified in Appendix C.

Similarly, a seating plane on the topside of the socket establishes the minimum package height. See Section 5.2 for the calculated IHS height above the motherboard.

3.5 Durability

The socket must withstand 20 cycles of processor insertion and removal. The max chain contact resistance from Table 5-4 must be met when mated in the 1st and 20th cycles.

The socket Pick and Place cover must withstand 15 cycles of insertion and removal.

3.6 Markings

There are three markings on the socket:

- LGA1155: Font type is Helvetica Bold - minimum 6 point (2.125 mm). This mark will also appear on the pick and place cap.
- Manufacturer's insignia (font size at supplier's discretion).
- Lot identification code (allows traceability of manufacturing date and location).

All markings must withstand 260 °C for 40 seconds (typical reflow/rework profile) without degrading, and must be visible after the socket is mounted on the motherboard.

LGA1155 and the manufacturer's insignia are molded or laser marked on the side wall.

3.7 Component Insertion Forces

Any actuation must meet or exceed SEMI S8-95 Safety Guidelines for Ergonomics/ Human Factors Engineering of Semiconductor Manufacturing Equipment, example Table R2-7 (Maximum Grip Forces). The socket must be designed so that it requires no force to insert the package into the socket.

3.8 Socket Size

Socket information needed for motherboard design is given in Appendix C.

This information should be used in conjunction with the reference motherboard keep-out drawings provided in Appendix B to ensure compatibility with the reference thermal mechanical components.

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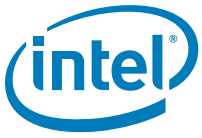


4 Independent Loading Mechanism (ILM)

The ILM has two critical functions: deliver the force to seat the processor onto the socket contacts and distribute the resulting compressive load evenly through the socket solder joints.

The mechanical design of the ILM is integral to the overall functionality of the LGA1155 socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be "build to print" from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel's detailed studies and may not incorporate critical design parameters.

Note: There is a single ILM design for the LGA1155 socket and LGA1156 socket.

4.1 Design Concept

The ILM consists of two assemblies that will be procured as a set from the enabled vendors. These two components are ILM assembly and back plate. To secure the two assemblies, two types of fasteners are required a pair (2) of standard 6-32 thread screws and a custom 6-32 thread shoulder screw. The reference design incorporates a T-20 Torx head fastener. The Torx head fastener was chosen to ensure end users do not inadvertently remove the ILM assembly and for consistency with the LGA1366 socket ILM. The Torx head fastener is also less susceptible to driver slippage. Once assembled the ILM is not required to be removed to install / remove the motherboard from a chassis.

4.1.1 ILM Assembly Design Overview

The ILM assembly consists of 4 major pieces: ILM cover, load lever, load plate and the hinge frame assembly.

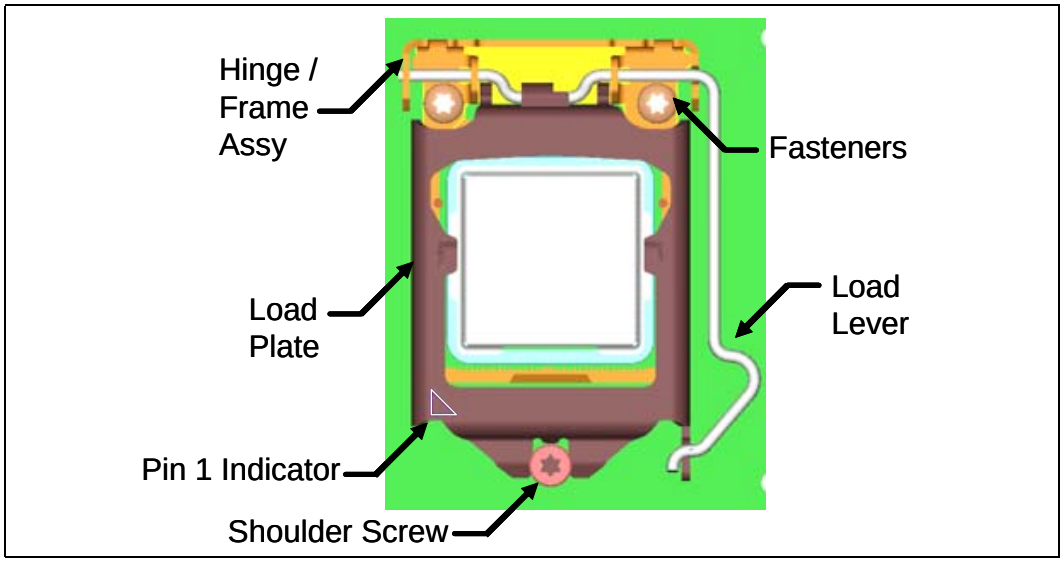
All of the pieces in the ILM assembly except the hinge frame and the screws used to attach the back plate are fabricated from stainless steel. The hinge frame is plated. The frame provides the hinge locations for the load lever and load plate. An insulator is pre-applied to the bottom surface of the hinge frame.

The ILM assembly design ensures that once assembled to the back plate the only features touching the board are the shoulder screw and the insulated hinge frame assembly. The nominal gap of the load plate to the board is ~1 mm.

When closed the load plate applies two point loads onto the IHS at the "dimpled" features shown in Figure 4-1. The reaction force from closing the load plate is transmitted to the hinge frame assembly and through the fasteners to the back plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints.

A pin 1 indicator will be marked on the ILM assembly.

Figure 4-1. ILM Assembly with Installed Processor



4.1.2 ILM Back Plate Design Overview

The back plate is a flat steel back plate with pierced and extruded features for ILM attach. A clearance hole is located at the center of the plate to allow access to test points and backside capacitors if required. An insulator is pre-applied. A notch is placed in one corner to assist in orienting the back plate during assembly.

Note: The Server ILM back plate is different from the Desktop design. Since Server secondary-side clearance of 3.0 mm [0.118 inch] is generally available for leads and backside components, so Server ILM back plate is designed with 1.8 mm thickness and 2.2 mm entire height including punch protrusion length.

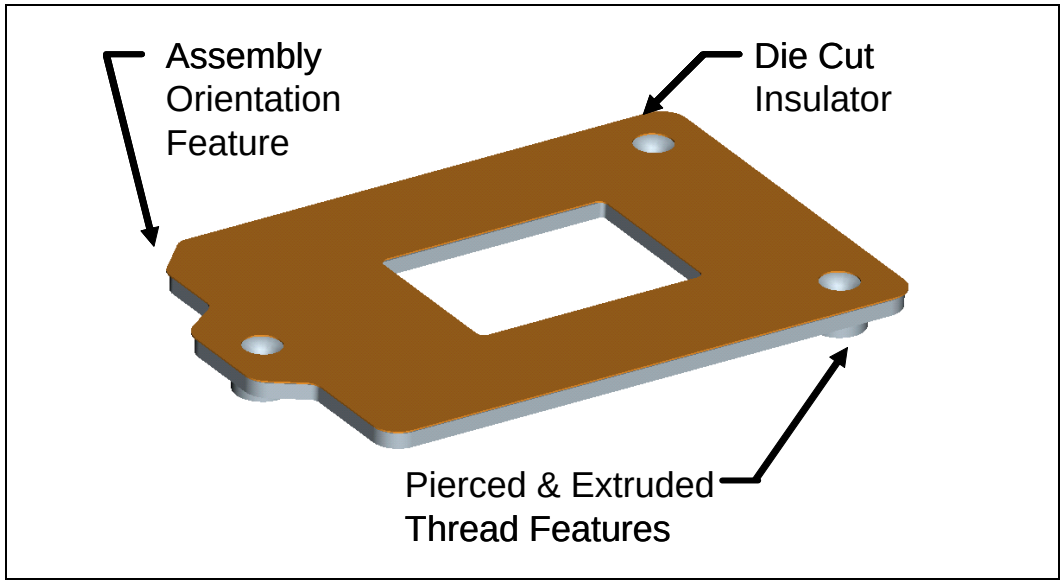
Caution: Intel does NOT recommend using the server back plate for high-volume desktop applications at this time as the server back plate test conditions cover a limited envelope. Back plates and screws are similar in appearance. To prevent mixing, different levels of differentiation between server and desktop back plate and screws have been implemented.

For ILM back plate, three levels of differentiation have been implemented:

- Unique part numbers, please refer to part numbers listed in Appendix A.
- Desktop ILM back plate to use black lettering for marking versus server ILM back plate to use yellow lettering for marking.
- Desktop ILM back plate using marking “115XDBP” versus server ILM back plate using marking “115XSBP”.

Note: When reworking a BGA component or the socket that the heatsink, battery, ILM and ILM Back Plate are removed prior to rework. The ILM back plate should also be removed when reworking through hole mounted components in a mini-wave or solder pot). The maximum temperature for the pre-applied insulator on the ILM is approximately 106 °C.

Figure 4-2. Back Plate



4.1.3 Shoulder Screw and Fasteners Design Overview

The shoulder screw is fabricated from carbonized steel rod. The shoulder height and diameter are integral to the mechanical performance of the ILM. The diameter provides alignment of the load plate. The height of the shoulder ensures the proper loading of the IHS to seat the processor on the socket contacts. The design assumes the shoulder screw has a minimum yield strength of 235 MPa.

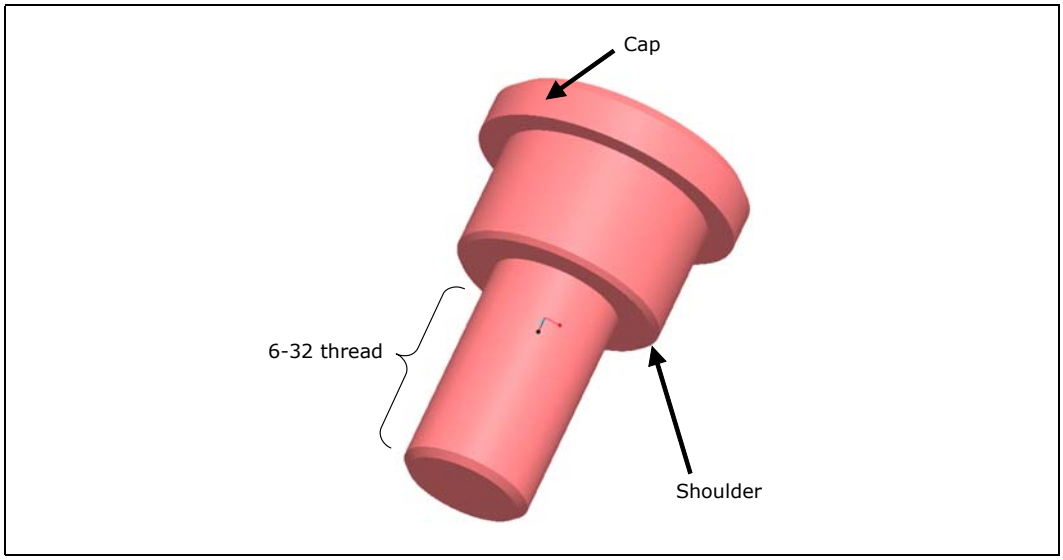
A dimensioned drawing of the shoulder screw is available for local sourcing of this component. Please refer to Figure B-18 for the custom 6-32 thread shoulder screw drawing.

The standard fasteners can be sourced locally. The design assumes this fastener has a minimum yield strength of 235 MPa. Please refer to Figure B-19 for the standard 6-32 thread fasteners drawing.

The screws for Server ILM are different from Desktop design. The length of Server ILM screws are shorter than the Desktop screw length to satisfy Server secondary-side clearance limitation. Server ILM back plate to use black nickel plated screws, whereas desktop ILM back plate to use clear plated screws. Unique part numbers, please refer to Appendix A.

Note: The reference design incorporates a T-20 Torx head fastener. The Torx head fastener was chosen to ensure end users do not inadvertently remove the ILM assembly and for consistency with the LGA1366 socket ILM.

Figure 4-3. Shoulder Screw



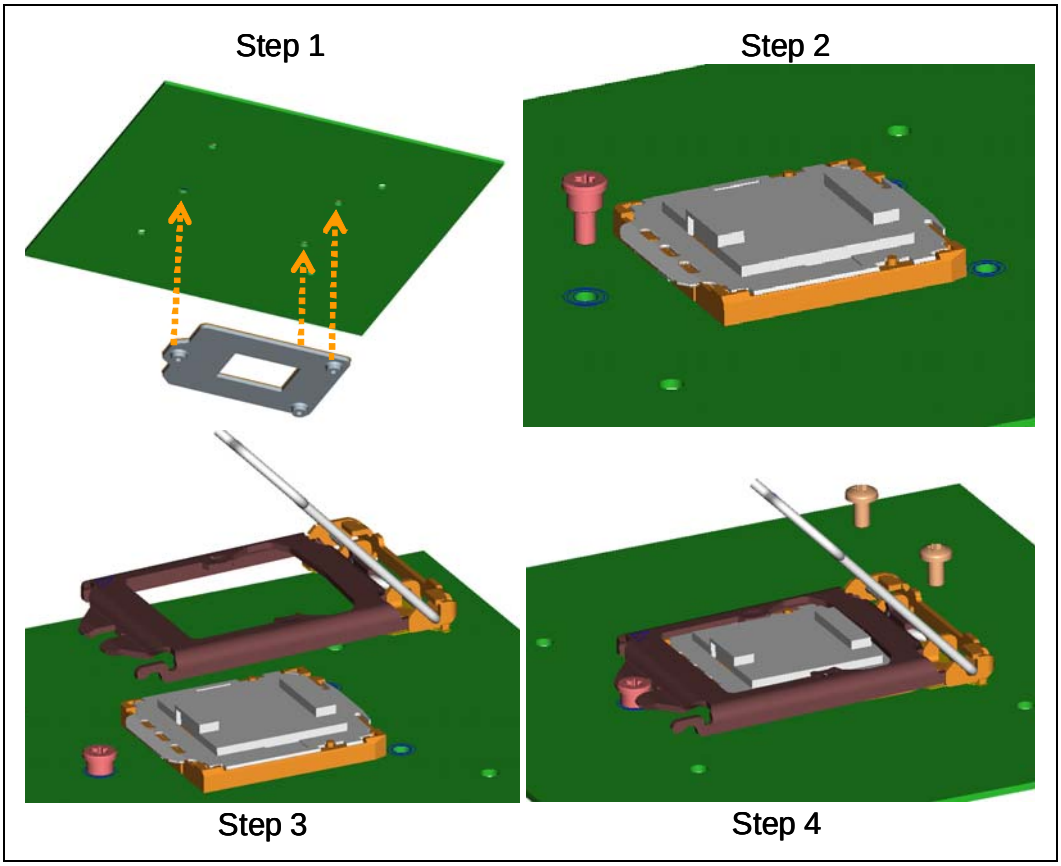
4.2 Assembly of ILM to a Motherboard

The ILM design allows a bottoms up assembly of the components to the board. See Figure 4-4 for step by step assembly sequence.

1. Place the back plate in a fixture. The motherboard is aligned with the fixture.
2. Install the shoulder screw in the single hole near Pin 1 of the socket. Torque to a minimum and recommended 8 inch-pounds, but not to exceed 10 inch-pounds.
3. Align and place the ILM assembly over the socket.
4. Install two (2) 6-32 fasteners. Torque to a minimum and recommended 8 inch-pounds, but not to exceed 10 inch-pounds.

The thread length of the shoulder screw accommodates a nominal board thicknesses of 0.062”.

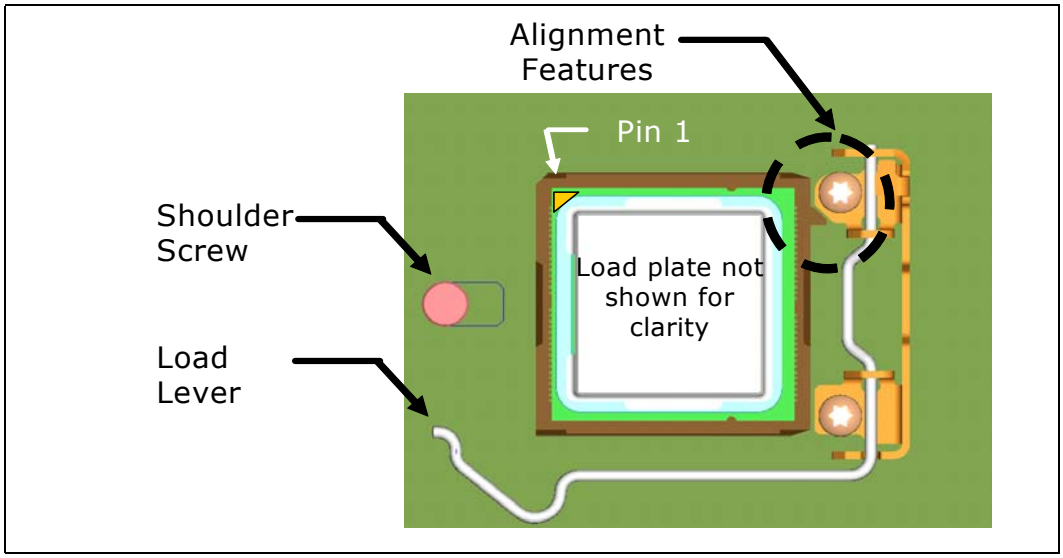
Figure 4-4. ILM Assembly



Note: Here ILM assembly shown in figure is without ILM cover preinstalled.

As indicated in Figure 4-5, the shoulder screw, socket protrusion and ILM key features prevent 180 degree rotation of ILM cover assembly with respect to socket. The result is a specific Pin 1 orientation with respect to ILM lever.

Figure 4-5. Pin1 and ILM Lever



4.3 ILM Interchangeability

ILM assembly and ILM back plate built from the Intel controlled drawings are intended to be interchangeable. Interchangeability is defined as an ILM from Vendor A will demonstrate acceptable manufacturability and reliability with a socket body from Vendor A, B or C. ILM assembly and ILM back plate from all vendors are also interchangeable.

The ILM are an integral part of the socket validation testing. ILMs from each vendor will be matrix tested with the socket bodies from each of the current vendors. The tests would include: manufacturability, bake and thermal cycling.

See Appendix A for vendor part numbers that were tested.

Note: ILMs that are not compliant to the Intel controlled ILM drawings can not be assured to be interchangeable.

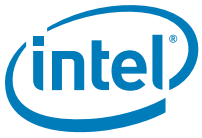
4.4 Markings

There are four markings on the ILM:

- 115XLM: Font type is Helvetica Bold - minimum 6 point (2.125 mm).
- Manufacturer's insignia (font size at supplier's discretion).
- Lot identification code (allows traceability of manufacturing date and location).
- Pin 1 indicator on the load plate.

All markings must be visible after the ILM is assembled on the motherboard.

115XLM and the manufacturer's insignia can be ink stamped or laser marked on the side wall.



4.5 ILM Cover

Intel has developed an ILM Cover that will snap onto the ILM for the LGA115x socket family. The ILM cover is intended to reduce the potential for socket contact damage from operator and customer fingers being close to the socket contacts to remove or install the pick and place cap. The ILM Cover concept is shown in Figure 4-6.

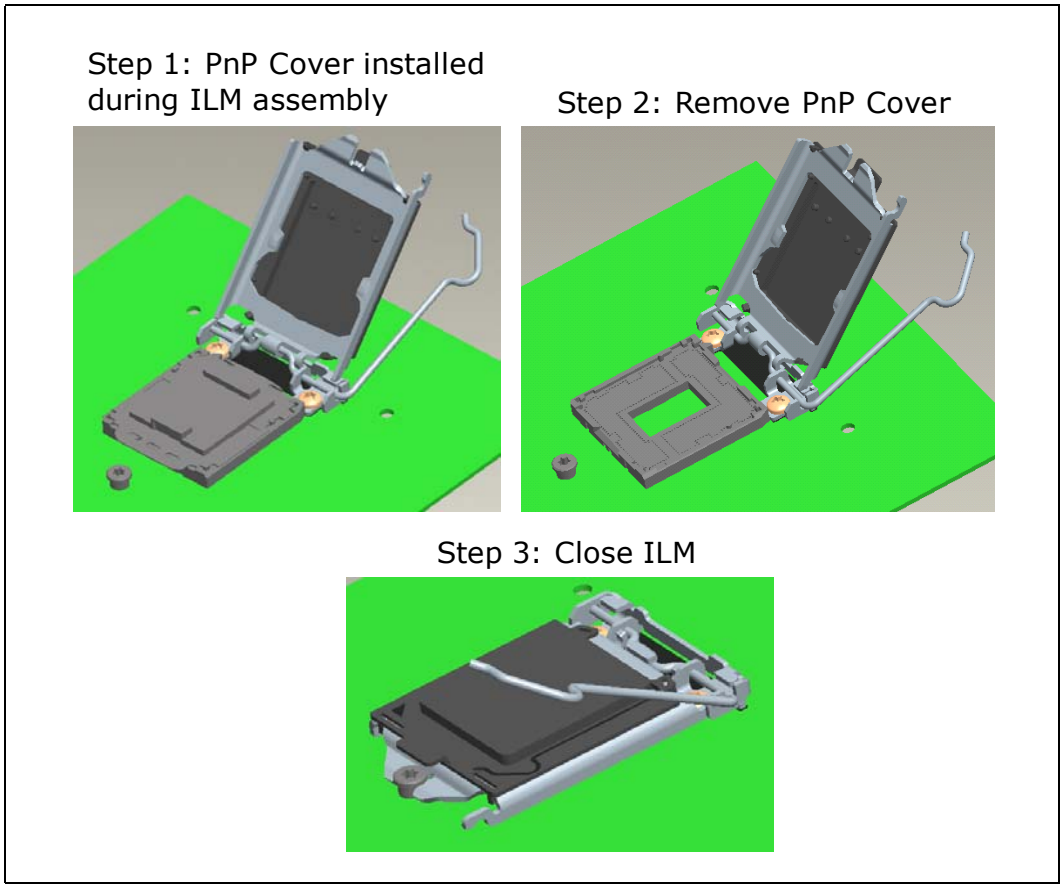
The ILM Cover is intended to be used in place of the pick and place cover once the ILM is assembled to the motherboard. The ILM will be offered with the ILM Cover pre assembled as well as offered as a discrete component.

ILM Cover features:

- Pre-assembled by the ILM vendors to the ILM load plate. It will also be offered as a discrete component.
- The ILM cover will pop off if a processor is installed in the socket, and the ILM Cover and ILM are from the same manufacturer.
- ILM Cover can be installed while the ILM is open.
- Maintain compatibility between validated ILM vendors for LGA115x socket, with the exception noted below[1].
- The ILM cover for the LGA115x socket will have a flammability rating of V-2 per UL 60950-1.

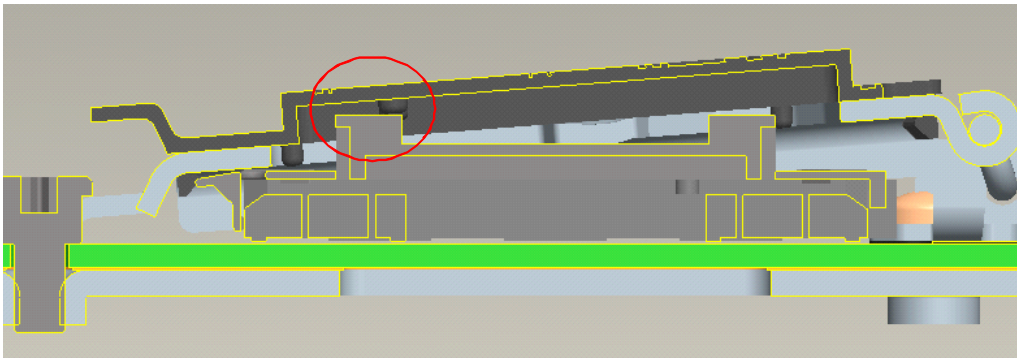
Note: The ILM Cover pop off feature is not supported if the ILM Covers are interchanged on different vendor's ILMs.

Figure 4-6. ILM Cover



As indicated in Figure 4-6, the pick and place cover should remain installed during ILM assembly to the motherboard. After assembly, the pick and place cover is removed, and the ILM mechanism (with the ILM cover installed) closed to protect the contacts. The ILM Cover is designed to pop off if the pick and place cover is accidentally left in place and the ILM closed with the ILM Cover installed. This is shown in Figure 4-7.

Figure 4-7. ILM Cover and PnP Cover Interference



As indicated in Figure 4-7, the pick and place cover cannot remain in place and used in conjunction with the ILM Cover. The ILM Cover is designed to interfere and pop off if the pick and place cover is unintentionally left in place. The ILM cover will also interfere and pop off if the ILM is closed with a processor in place in the socket.

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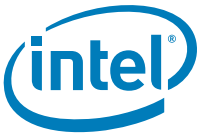
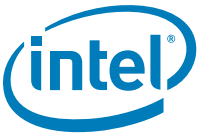




5 LGA1155 Socket and ILM Electrical, Mechanical and Environmental Specifications

This chapter describes the electrical, mechanical and environmental specifications for the LGA1155 socket and the Independent Loading Mechanism.

5.1 Component Mass

Table 5-1. Socket Component Mass

Component	Mass
Socket Body, Contacts and PnP Cover	10 g
ILM Cover	29 g
ILM Back Plate	38 g

5.2 Package / Socket Stackup Height

Table 5-2 provides the stackup height of a processor in the 1155-land LGA package and LGA1155 socket with the ILM closed and the processor fully seated in the socket.

Table 5-2. 1155-land Package and LGA1155 Socket Stackup Height

Component	Stackup Height	Note
Integrated Stackup Height (mm) From Top of Board to Top of IHS	7.781 ± 0.335 mm	2
Socket Nominal Seating Plane Height	3.4 ± 0.2 mm	1
Package Nominal Thickness (lands to top of IHS)	4.381 ± 0.269 mm	1

Notes:
1. This data is provided for information only, and should be derived from: (a) the height of the socket seating plane above the motherboard after reflow, given in Appendix C, (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances that are given in the corresponding processor data sheet.
2. The integrated stackup height value is a RSS calculation based on current and planned processors that will use the ILM design.

5.3 Loading Specifications

The socket will be tested against the conditions listed in Chapter 11 with heatsink and the ILM attached, under the loading conditions outlined in this section.

Table 5-3 provides load specifications for the LGA1155 socket with the ILM installed. The maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The socket body should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 5-3. Socket & ILM Mechanical Specifications

Parameter	Min	Max	Notes
ILM static compressive load on processor IHS	311 N [70 lbf]	600 N [135 lbf]	3, 4, 7, 8
Heatsink static compressive load	0 N [0 lbf]	222 N [50 lbf]	1, 2, 3
Total static compressive Load (ILM plus Heatsink)	311 N [70 lbf]	822 N [185 lbf]	3, 4, 7, 8
Dynamic Compressive Load (with heatsink installed)	N/A	712 N [160 lbf]	1, 3, 5, 6
Pick & Place cover insertion force	N/A	10.2 N [2.3 lbf]	-
Pick & Place cover removal force	2.2N [0.5 lbf]	7.56 N [1.7 lbf]	9
Load lever actuation force	N/A	20.9 N [4.7 lbf] in the vertical direction 10.2 N [2.3 lbf] in the lateral direction.	-
Maximum heatsink mass	N/A	500g	10

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and it's retention solution to maintain the heatsink to IHS interface. This does not imply the Intel reference TIM is validated to these limits.
3. Loading limits are for the LGA1155 socket.
4. This minimum limit defines the static compressive force required to electrically seat the processor onto the socket contacts. The minimum load is a beginning of life load.
5. Dynamic loading is defined as a load a 4.3 m/s [170 in/s] minimum velocity change average load superimposed on the static load requirement.
6. Test condition used a heatsink mass of 500 gm [1.102 lb.] with 50 g acceleration (table input) and an assumed 2X Dynamic Acceleration Factor (DAF). The dynamic portion of this specification in the product application can have flexibility in specific values. The ultimate product of mass times acceleration plus static heatsink load should not exceed this limit.
7. The maximum BOL value and must not be exceeded at any point in the product life.
8. The minimum value is a beginning of life loading requirement based on load degradation over time.
9. The maximum removal force is the flick up removal upwards thumb force (measured at 45o), not applicable to SMT operation for system assembly. Only the minimum removal force is applicable to vertical removal in SMT operation for system assembly.
10. The maximum heatsink mass includes the heatsink, screws, springs, rings and cups. This mass limit is evaluated using the heatsink attach to the PCB.

5.4 Electrical Requirements

LGA1155 socket electrical requirements are measured from the socket-seating plane of the processor to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket contact, but includes effects of adjacent contacts where indicated.

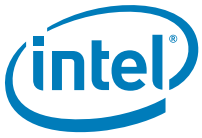


Table 5-4. Electrical Requirements for LGA1155 Socket

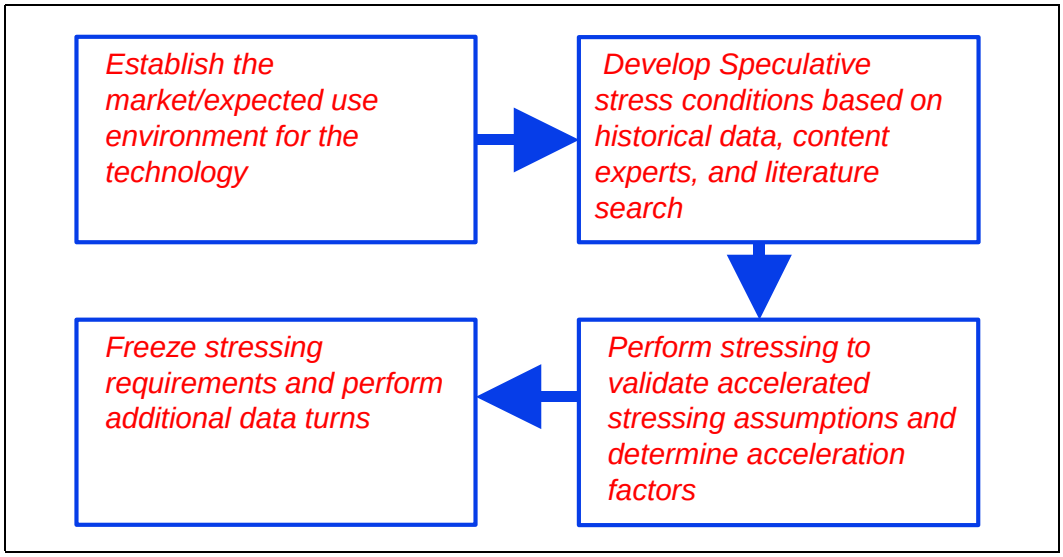
Parameter	Value	Comment
Mated loop inductance, Loop	<3.6 nH	The inductance calculated for two contacts, considering one forward conductor and one return conductor. These values must be satisfied at the worst-case height of the socket.
Socket Average Contact Resistance (EOL)	19 mOhm	The socket average contact resistance target is calculated from the following equation: sum (Ni X LLCRi) / sum (Ni) • LLCRi is the chain resistance defined as the resistance of each chain minus resistance of shorting bars divided by number of lands in the daisy chain. • Ni is the number of contacts within a chain. • I is the number of daisy chain, ranging from 1 to 119 (total number of daisy chains). The specification listed is at room temperature and has to be satisfied at all time.
Max Individual Contact Resistance (EOL)	100 mOhm	The specification listed is at room temperature and has to be satisfied at all time. **Socket Contact Resistance:** The resistance of the socket contact, solderball, and interface resistance to the interposer land; gaps included.
Bulk Resistance Increase	≤ 3 mΩ	The bulk resistance increase per contact from 25°C to 100°C.
Dielectric Withstand Voltage	360 Volts RMS	
Insulation Resistance	800 MΩ	

5.5 Environmental Requirements

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

The reliability targets in this section are based on the expected field use environment for these products. The test sequence for new sockets will be developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology can be seen in Figure 5-1.

Figure 5-1. Flow Chart of Knowledge-Based Reliability Evaluation Methodology



A detailed description of this methodology can be found at: ftp://download.intel.com/technology/itj/q32000/pdf/reliability.pdf.

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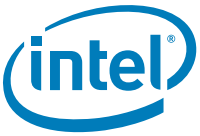


6 Thermal Specifications

The processor requires a thermal solution to maintain temperatures within its operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS).

This chapter provides data necessary for developing a complete thermal solution. For more information on a thermal solution design, please refer to Chapter 9.

6.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the Chapter 9.

The processors implement a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Digital Temperature Sensor (DTS). The DTS can be read via the Platform Environment Control Interface (PECI) as described in Chapter 7. Alternatively, when PECI is monitored by the PCH, the processor temperature can be read from the PCH via the SMBUS protocol defined in *Embedded Controller Support Provided by Platform Controller Hub (PCH)*. The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT# (see Section 6.2, Processor Thermal Features). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed only need to ensure the case temperature meets the thermal profile specifications.

A single integer change in the PECI value corresponds to approximately 1 °C change in processor temperature. Although each processors DTS is factory calibrated, the accuracy of the DTS will vary from part to part and may also vary slightly with temperature and voltage. In general, each integer change in PECI should equal a temperature change between 0.9 °C and 1.1 °C.

Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP), instead of the maximum processor power consumption. The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more details on this feature, refer to

Section 6.2. To ensure maximum flexibility for future processors, systems should be designed to the Thermal Solution Capability guidelines, even if a processor with lower power dissipation is currently planned.

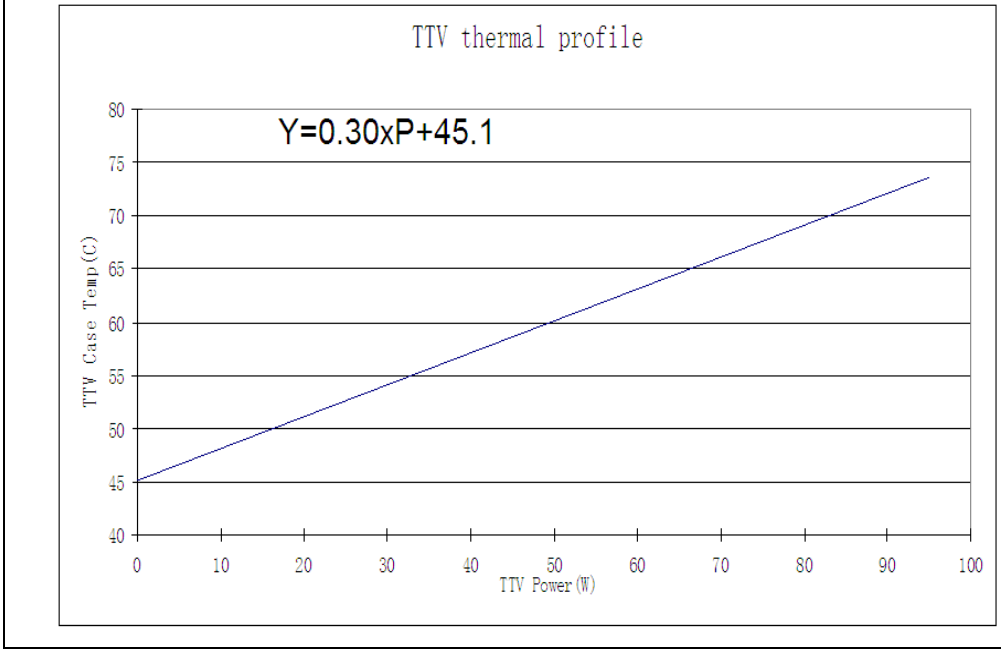
Table 6-1. Processor Thermal Specifications

Product	Guidelines[8]	Max Power Package C1E (W)[1,2,6]	Max Power Package C3 (W)[1,2,6]	Max Power Package C6 (W)[1,3,6]	TTV Thermal Design Power (W)[4,5,7]	Min TCASE (°C)	Maximum TTV TCASE (°C)
Intel® Xeon® Processor E3-1280 (95W)	2011D	28	22	5.5	95	5	Figure 6-1 &Table 6-2
Intel® Xeon® processor E3-1200 (80W)	2011D	28	22	5.5	80		Figure 6-2& Table 6-3
Intel® Xeon® processor E3-1260L (45W)	2011B	20	12	5.5	45		Figure 6-3& Table 6-4
Intel® Xeon® processor E3-1220L (20W)	2011A	18	10	5	20		Figure 6-4& Table 6-5
Intel® Xeon® processor E3-1200 (95W) with integrated graphics	2011D	28	22	5.5	95		Figure 6-5& Table 6-6

Notes:
1. The package C-state power is the worst case power in the system configured as follows:
   - Memory configured for DDR3 1333 and populated with 2 DIMM per channel.
   - DMI and PCIe links are at L1.
2. Specification at Tj of 50 °C and minimum voltage loadline.
3. Specification at Tj of 35 °C and minimum voltage loadline.
4. These values are specified at V_{CC_MAX} and V_{NOM} for all other voltage rails for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CCP} exceeds V_{CCP_MAX} at specified I_{CCP}. Please refer to the loadline specifications in the datasheet.
5. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at DTS = -1. TDP is achieved with the Memory configured for DDR3 1333 and 2 DIMMs per channel.
6. Not 100% tested. Specified by design characterization.
7. When the Multi-monitor feature is enabled (running 4 displays simultaneously) there could be corner cases with additional system thermal impact on the SA and VCCP rails ≤1.5W (maximum of 1.5W measured on 16 lane PCIe card). The integrator should perform additional thermal validation with Multi-monitor enabled to ensure thermal compliance.
8. Guidelines provide a design target for meeting all planned processor frequency requirements. For more detailed definition, please refer to latest processor Datasheet.

6.1.1 Intel® Xeon® Processor E3-1280 (95W)Thermal Profile

Figure 6-1. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1280 (95W)



Notes:
1. Please refer to Table 6-2 for discrete points that constitute the thermal profile.
2. Refer to Chapter 9 and Chapter 11 for system and environmental implementation details.

Table 6-2. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1280 (95W) (Sheet 1 of 2)

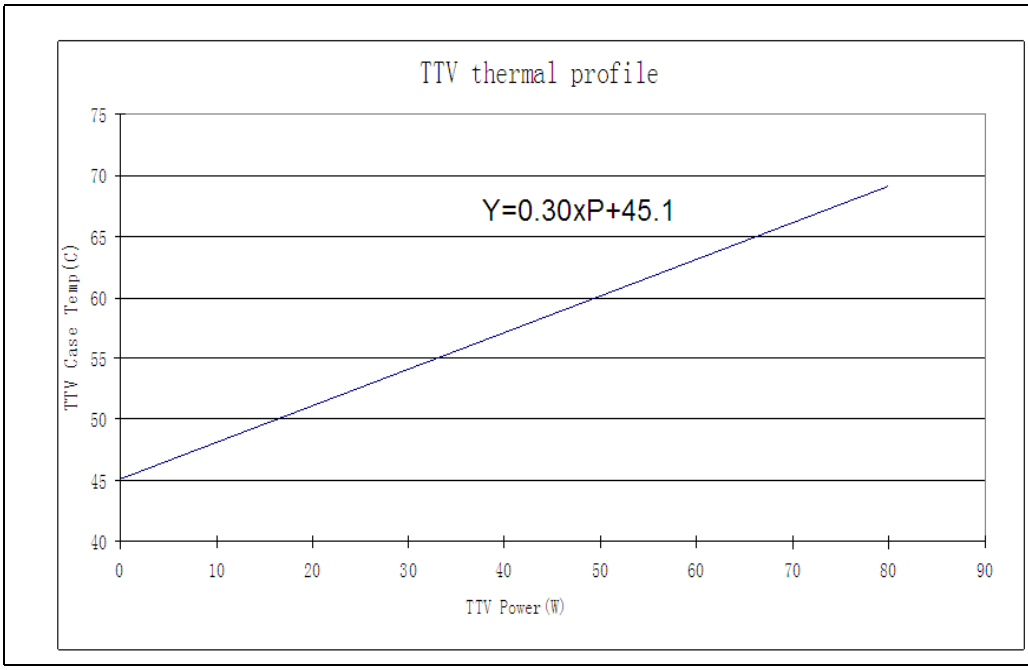
Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	45.1	50	60.1
2	45.7	52	60.7
4	46.3	54	61.3
6	46.9	56	61.9
8	47.5	58	62.5
10	48.1	60	63.1
12	48.7	62	63.7
14	49.3	64	64.3
16	49.9	66	64.9
18	50.5	68	65.5
20	51.1	70	66.1
22	51.7	72	66.7
24	52.3	74	67.3
26	52.9	76	67.9
28	53.5	78	68.5

Table 6-2. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1280 (95W) (Sheet 2 of 2)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
30	54.1	80	69.1
32	54.7	82	69.7
34	55.3	84	70.3
36	55.9	86	70.9
38	56.5	88	71.5
40	57.1	90	72.1
42	57.7	92	72.7
44	58.3	94	73.3
46	58.9	95	73.6
48	59.5		

6.1.2 Intel® Xeon® Processor E3-1200 (80W) Thermal Profile

Figure 6-2. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1200 (80W)



Notes:
1. Please refer to Table 6-3 for discrete points that constitute the thermal profile.
2. Refer to Chapter 9 and Chapter 11 for system and environmental implementation details.

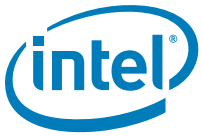
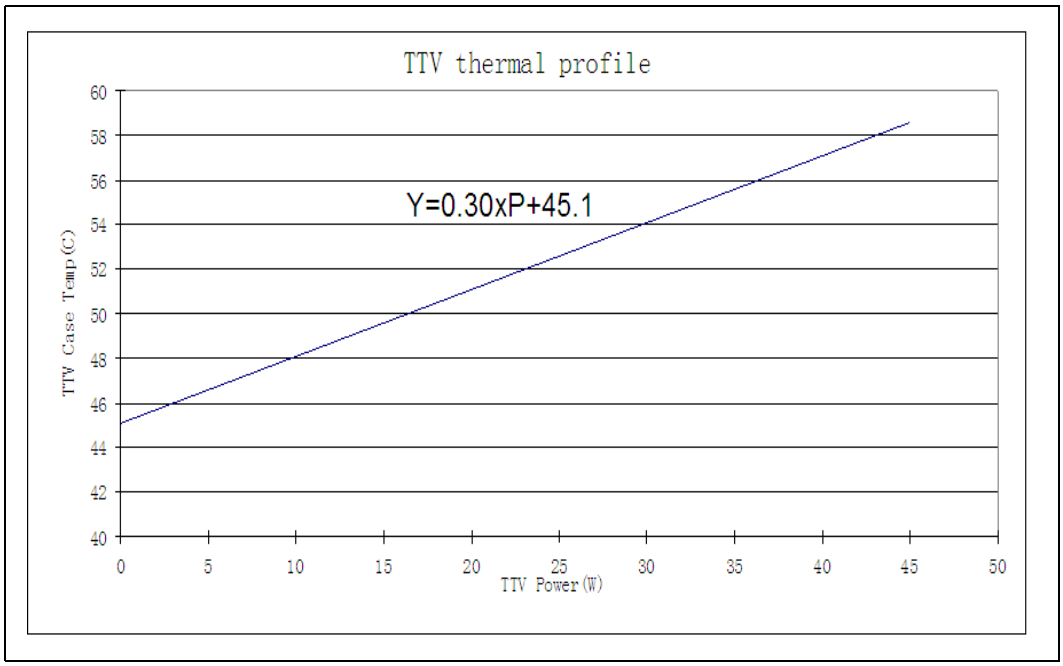


Table 6-3. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1200 (80W)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	45.1	42	57.7
2	45.7	44	58.3
4	46.3	46	58.9
6	46.9	48	59.5
8	47.5	50	60.1
10	48.1	52	60.7
12	48.7	54	61.3
14	49.3	56	61.9
16	49.9	58	62.5
18	50.5	60	63.1
20	51.1	62	63.7
22	51.7	64	64.3
24	52.3	66	64.9
26	52.9	68	65.5
28	53.5	70	66.1
30	54.1	72	66.7
32	54.7	74	67.3
34	55.3	76	67.9
36	55.9	78	68.5
38	56.5	80	69.1
40	57.1		

6.1.3 Intel® Xeon® Processor E3-1260L (45W) Thermal Profile

Figure 6-3. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1260L (45W)



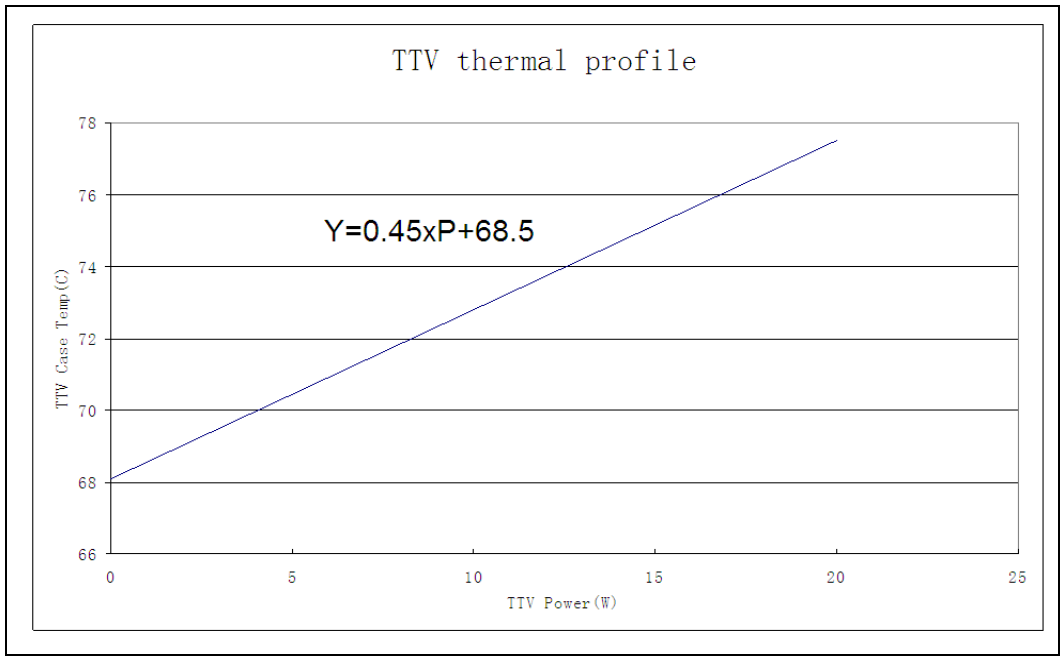
Notes:
1. Please refer to Table 6-4 for discrete points that constitute the thermal profile.
2. Refer to Chapter 9 and Chapter 11 for system and environmental implementation details.

Table 6-4. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1260L (45W)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	45.1	24	52.3
2	45.7	26	52.9
4	46.3	28	53.5
6	46.9	30	54.1
8	47.5	32	54.7
10	48.1	34	55.3
12	48.7	36	55.9
14	49.3	38	56.5
16	49.9	40	57.1
18	50.5	42	57.7
20	51.1	44	58.3
22	51.7	45	58.6

6.1.4 Intel® Xeon® Processor E3-1220L (20W) Thermal Profile

Figure 6-4. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1220L (20W)



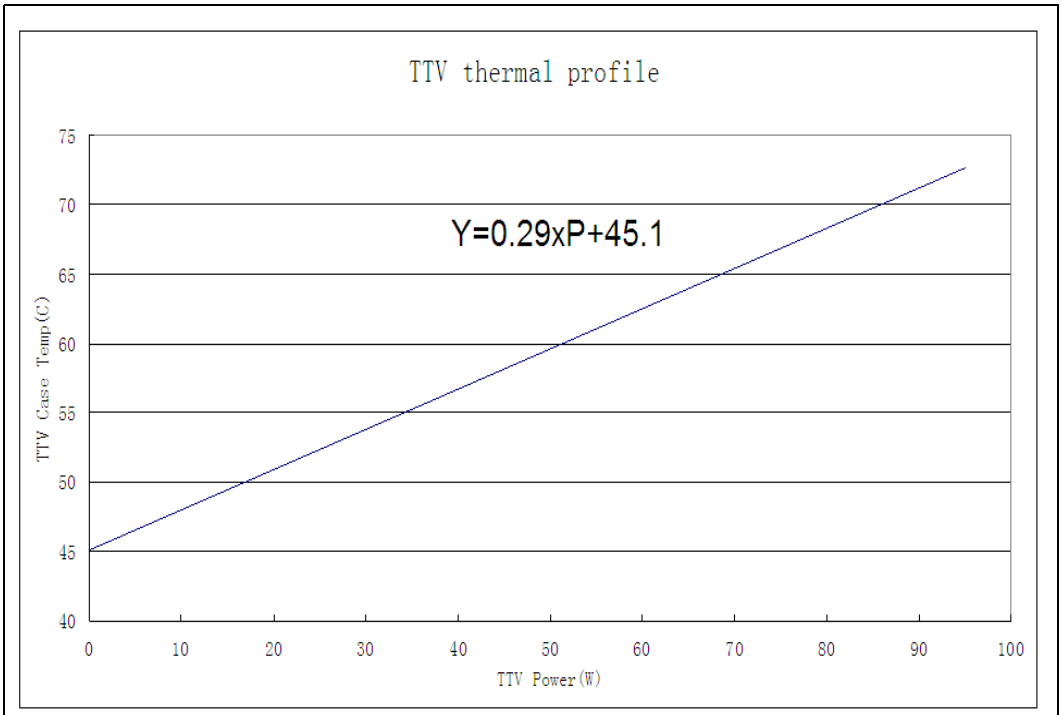
Notes:
1. Please refer to Table 6-5 for discrete points that constitute the thermal profile.
2. Refer to Chapter 9 and Chapter 11 for system and environmental implementation details.

Table 6-5. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1220L (20W)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	68.5	12	73.9
2	69.4	14	74.8
4	70.3	16	75.7
6	71.2	18	76.6
8	72.1	20	77.5
10	73.0		

6.1.5 Intel® Xeon® Processor E3-1200 (95W) with Integrated Graphics Thermal Profile

Figure 6-5. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1200 (95W) with Integrated Graphics



Notes:
1. Please refer to Table 6-6 for discrete points that constitute the thermal profile.
2. Refer to Chapter 11 for system and environmental implementation details.

Table 6-6. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1200 (95W) with Integrated Graphics (Sheet 1 of 2)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	45.1	50	59.6
2	45.7	52	60.2
4	46.3	54	60.8
6	46.8	56	61.3
8	47.4	58	61.9
10	48.0	60	62.5
12	48.6	62	63.1
14	49.2	64	63.7
16	49.7	66	64.2
18	50.3	68	64.8
20	50.9	70	65.4
22	51.5	72	66.0

Table 6-6. Thermal Test Vehicle Thermal Profile for Intel® Xeon® Processor E3-1200 (95W) with Integrated Graphics (Sheet 2 of 2)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
24	52.1	74	66.6
26	52.6	76	67.1
28	53.2	78	67.7
30	53.8	80	68.3
32	54.4	82	68.9
34	55.0	84	69.5
36	55.5	86	70.0
38	56.1	88	70.6
40	56.7	90	71.2
42	57.3	92	71.8
44	57.9	94	72.4
46	58.4	95	72.6
48	59.0		

6.1.6 Processor Specification for Operation Where Digital Thermal Sensor Exceeds $T_{CONTROL}$

During operation, when the DTS value is greater than $T_{CONTROL}$, the fan speed control algorithm must drive the fan speed to meet or exceed the target thermal solution performance (Ψ_{CA}) shown in below tables:

- Table 6-7 for the Intel® Xeon® Processor E3-1280 (95W)
- Table 6-8 for theIntel® Xeon® processor E3-1200 (80W)
- Table 6-9 for the Intel® Xeon® processor E3-1260L (45W)
- Table 6-10 for the Intel® Xeon® processor E3-1220L (20W)
- Table 6-11 for the Intel® Xeon® processor E3-1200 (95W) with integrated graphics

To get the full acoustic benefit of the DTS specification, ambient temperature monitoring is necessary.

Table 6-7. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1280 (95W) (Sheet 1 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
45.1	0.300	0.300
44.0	0.320	0.312
43.0	0.337	0.322
42.0	0.355	0.333
41.0	0.373	0.343
40.0	0.391	0.354
39.0	0.409	0.364
38.0	0.427	0.375

Table 6-7. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1280 (95W) (Sheet 2 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
37.0	0.445	0.385
36.0	0.462	0.396
35.0	0.480	0.406
34.0	0.498	0.417
33.0	0.516	0.427
32.0	0.534	0.438
31.0	0.552	0.448
30.0	0.569	0.459
29.0	0.587	0.469
28.0	0.605	0.480
27.0	0.623	0.491
26.0	0.641	0.501
25.0	0.659	0.512
24.0	0.676	0.522
23.0	0.694	0.533
22.0	0.712	0.543
21.0	0.730	0.554
20.0	0.748	0.564

Notes:
1. The ambient temperature is measured at the inlet to the processor thermal solution.
2. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.30 + (45.1 - T_{AMBIENT}) \times 0.0178$
3. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.30 + (45.1 - T_{AMBIENT}) \times 0.0105$

Table 6-8. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1200 (80W) (Sheet 1 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
45.1	0.300	0.300
44.0	0.323	0.314
43.0	0.344	0.326
42.0	0.366	0.339
41.0	0.387	0.351
40.0	0.408	0.364
39.0	0.429	0.376
38.0	0.450	0.389
37.0	0.472	0.401
36.0	0.493	0.414
35.0	0.514	0.426
34.0	0.535	0.439
33.0	0.556	0.451

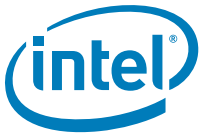


Table 6-8. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1200 (80W) (Sheet 2 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
32.0	0.578	0.464
31.0	0.599	0.476
30.0	0.620	0.489
29.0	0.641	0.501
28.0	0.662	0.514
27.0	0.683	0.526
26.0	0.705	0.539
25.0	0.726	0.551
24.0	0.747	0.564
23.0	0.768	0.576
22.0	0.789	0.589
21.0	0.811	0.601
20.0	0.832	0.614

Notes:
1. The ambient temperature is measured at the inlet to the processor thermal solution.
2. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.3 + (45.1 - T_{AMBIENT}) \times 0.0212$
3. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.3 + (45.1 - T_{AMBIENT}) \times 0.0125$

Table 6-9. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1260L (45W) (Sheet 1 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
45.1	0.300	0.300
44.0	0.341	0.324
43.0	0.379	0.347
42.0	0.417	0.369
41.0	0.454	0.391
40.0	0.492	0.413
39.0	0.530	0.436
38.0	0.567	0.458
37.0	0.605	0.480
36.0	0.643	0.502
35.0	0.680	0.524
34.0	0.718	0.547
33.0	0.756	0.569
32.0	0.793	0.591
31.0	0.831	0.613
30.0	0.869	0.636
29.0	0.906	0.658
28.0	0.944	0.680

Table 6-9. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1260L (45W) (Sheet 2 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
27.0	0.982	0.702
26.0	1.019	0.724
25.0	1.057	0.747
24.0	1.095	0.769
23.0	1.132	0.791
22.0	1.170	0.813
21.0	1.208	0.836
20.0	1.245	0.858

Notes:
1. The ambient temperature is measured at the inlet to the processor thermal solution.
2. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.3 + (45.1 - T_{AMBIENT}) \times 0.0377$
3. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.3+ (45.1 - T_{AMBIENT}) \times 0.0222$

Table 6-10. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1220L (20W) (Sheet 1 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
50.0	2.018	1.375
49.0	2.103	1.425
48.0	2.187	1.475
47.0	2.272	1.525
46.0	2.357	1.575
45.0	2.442	1.625
44.0	2.526	1.675
43.0	2.611	1.725
42.0	2.696	1.775
41.0	2.781	1.825
40.0	2.865	1.875
39.0	2.950	1.925
38.0	3.035	1.975
37.0	3.119	2.025
36.0	3.204	2.075
35.0	3.289	2.125
34.0	3.374	2.175
33.0	3.458	2.225
32.0	3.543	2.275
31.0	3.628	2.325
30.0	3.713	2.375
29.0	3.797	2.425

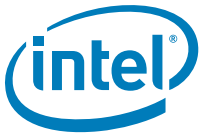


Table 6-10. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1220L (20W) (Sheet 2 of 2)

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
28.0	3.882	2.475
27.0	3.967	2.525
26.0	4.052	2.575
25.0	4.136	2.625

Notes:
1. The ambient temperature is measured at the inlet to the processor thermal solution.
2. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.45+ (68.5 - T_{AMBIENT}) \times 0.0847$
3. This column can be expressed as a function of $T_{AMBIENT}$ by the following equation:
   $Y_{CA} = 0.45 + (68.5 - T_{AMBIENT}) \times 0.05$

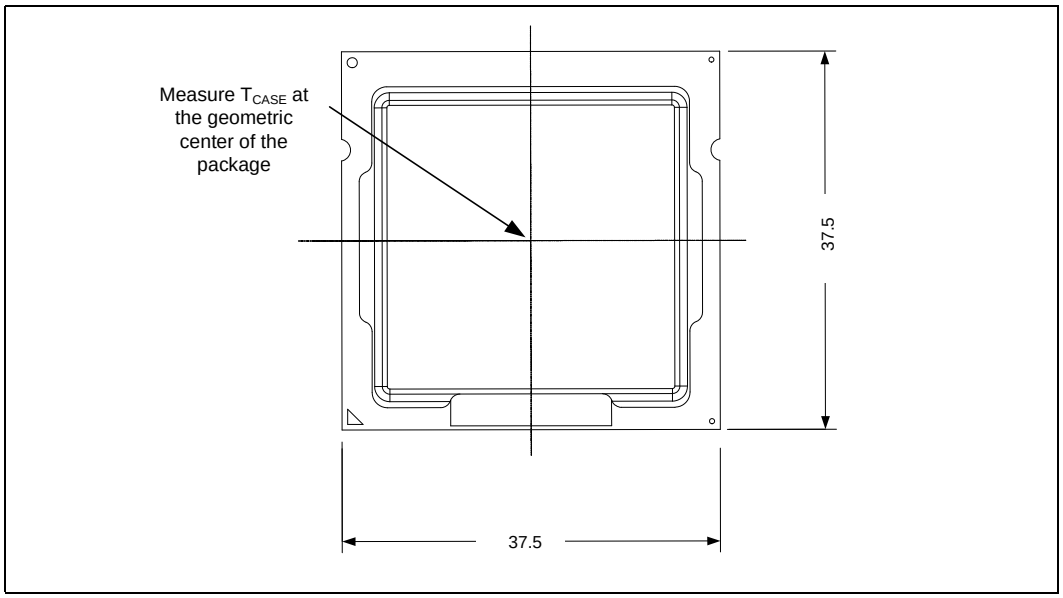
Table 6-11. Thermal Solution Performance above $T_{CONTROL}$ for the Intel® Xeon® Processor E3-1200 (95W) with Integrated Graphics

$T_{AMBIENT}$[1]	Ψ_{CA} at DTS = $T_{CONTROL}$[2]	Ψ_{CA} at DTS = -1[3]
45.1	0.290	0.289
44.0	0.310	0.301
43.0	0.328	0.312
42.0	0.346	0.322
41.0	0.364	0.333
40.0	0.383	0.343
39.0	0.401	0.354
38.0	0.419	0.364
37.0	0.437	0.375
36.0	0.455	0.385
35.0	0.473	0.396
34.0	0.491	0.406
33.0	0.510	0.417
32.0	0.528	0.427
31.0	0.546	0.438
30.0	0.564	0.448
29.0	0.582	0.459
28.0	0.600	0.469
27.0	0.618	0.480
26.0	0.637	0.491
25.0	0.655	0.501
24.0	0.673	0.512
23.0	0.691	0.522
22.0	0.709	0.533
21.0	0.727	0.543
20.0	0.746	0.554

6.1.7 Thermal Metrology

The maximum TTV case temperatures ($T_{CASE-MAX}$) can be derived from the data in the appropriate TTV thermal profile earlier in this chapter. The TTV T_{CASE} is measured at the geometric top center of the TTV integrated heat spreader (IHS). Figure 6-6 illustrates the location where T_{CASE} temperature measurements should be made. See Figure B-17 for drawing showing the thermocouple attach to the TTV package.

Figure 6-6. TTV Case Temperature (T_{CASE}) Measurement Location



Note: The following supplier can machine the groove and attach a thermocouple to the IHS. The supplier is listed below as a convenience to Intel's general customers and the list may be subject to change without notice. THERM-X OF CALIFORNIA Inc, 3200 Investment Blvd., Hayward, Ca 94545. Ernesto B Valencia +1-510-441-7566 Ext. 242 ernestov@therm-x.com. The vendor part number is XTMS1565.

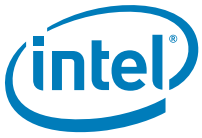
6.2 Processor Thermal Features

6.2.1 Processor Temperature

A new feature in the processors is a software readable field in the IA32_TEMPERATURE_TARGET register that contains the minimum temperature at which the TCC will be activated and PROCHOT# will be asserted. The TCC activation temperature is calibrated on a part-by-part basis and normal factory variation may result in the actual TCC activation temperature being higher than the value listed in the register. TCC activation temperatures may change based on processor stepping, frequency or manufacturing efficiencies.

6.2.2 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature provides an enhanced method for controlling the processor temperature when the processor silicon exceeds the Thermal Control Circuit (TCC) activation temperature. Adaptive Thermal Monitor uses TCC activation to reduce processor power via a combination of methods. The first method (Frequency/VID



control, similar to Thermal Monitor 2 (TM2) in previous generation processors) involves the processor reducing its operating frequency (via the core ratio multiplier) and input voltage (via the VID signals). This combination of lower frequency and VID results in a reduction of the processor power consumption. The second method (clock modulation, known as Thermal Monitor 1 or TM1 in previous generation processors) reduces power consumption by modulating (starting and stopping) the internal processor core clocks. The processor intelligently selects the appropriate TCC method to use on a dynamic basis. BIOS is not required to select a specific method (as with previous-generation processors supporting TM1 or TM2). The temperature at which Adaptive Thermal Monitor activates the Thermal Control Circuit is factory calibrated and is not user configurable. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

When the TCC activation temperature is reached, the processor will initiate TM2 in attempt to reduce its temperature. If TM2 is unable to reduce the processor temperature, then TM1 will be also be activated. TM1 and TM2 will work together (clocks will be modulated at the lowest frequency ratio) to reduce power dissipation and temperature.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a T_{CASE} that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the appropriate Thermal Mechanical Design Guidelines for information on designing a compliant thermal solution.

The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. The following sections provide more details on the different TCC mechanisms used by the processor.

6.2.2.1 Frequency / VID Control

When the Digital Temperature Sensor (DTS) reaches a value of 0 (DTS temperatures reported via PECI may not equal zero when PROCHOT# is activated, see Section 6.2.2.5 for further details), the TCC will be activated and the PROCHOT# signal will be asserted. This indicates the processors' temperature has met or exceeded the factory calibrated trip temperature and it will take action to reduce the temperature.

Upon activation of the TCC, the processor will stop the core clocks, reduce the core ratio multiplier by 1 ratio and restart the clocks. All processor activity stops during this frequency transition which occurs within 2 us. Once the clocks have been restarted at the new lower frequency, processor activity resumes while the voltage requested by the VID lines is stepped down to the minimum possible for the particular frequency. Running the processor at the lower frequency and voltage will reduce power consumption and should allow the processor to cool off. If after 1ms the processor is still too hot (the temperature has not dropped below the TCC activation point, DTS still = 0 and PROCHOT is still active), then a second frequency and voltage transition will

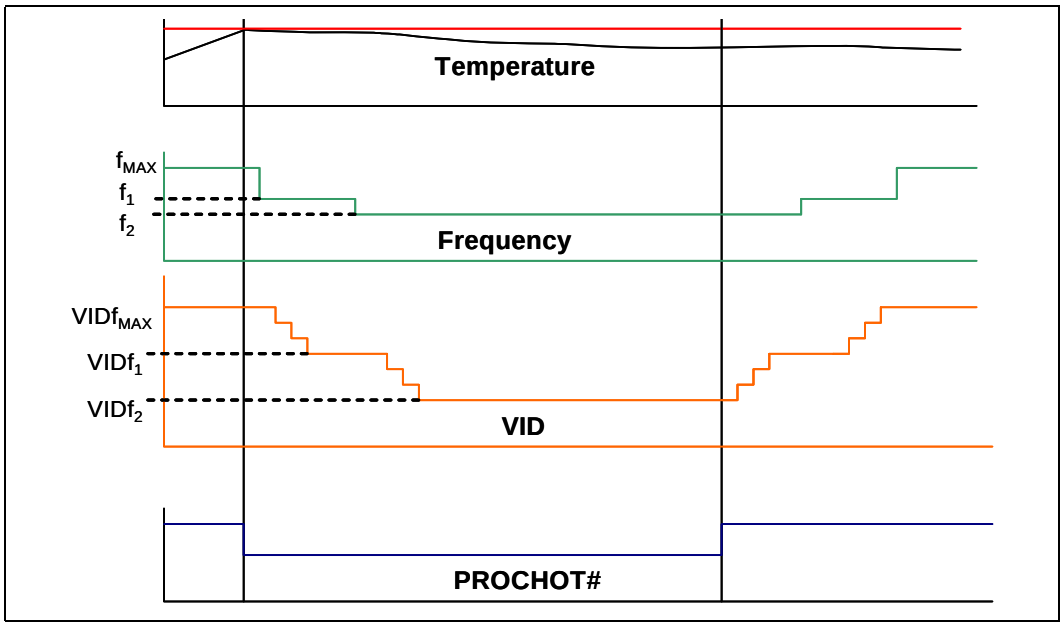
take place. This sequence of temperature checking and Frequency/VID reduction will continue until either the minimum frequency has been reached or the processor temperature has dropped below the TCC activation point.

If the processor temperature remains above the TCC activation point even after the minimum frequency has been reached, then clock modulation (described below) at that minimum frequency will be initiated.

There is no end user software or hardware mechanism to initiate this automated TCC activation behavior.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the TCC activation temperature. Once the temperature has dropped below the trip temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point via the intermediate VID/frequency points. Transition of the VID code will occur first, to insure proper operation as the frequency is increased. Refer to Figure 6-7 for an illustration of this ordering.

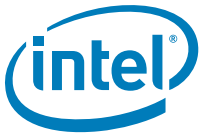
Figure 6-7. Frequency and Voltage Ordering



6.2.2.2 Clock Modulation

Clock modulation is a second method of thermal control available to the processor. Clock modulation is performed by rapidly turning the clocks off and on at a duty cycle that should reduce power dissipation by about 50% (typically a 30-50% duty cycle). Clocks often will not be off for more than 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified.

It is possible for software to initiate clock modulation with configurable duty cycles.



A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

6.2.2.3 Immediate Transition to combined TM1 and TM2

As mentioned above, when the TCC is activated the processor will sequentially step down the ratio multipliers and VIDs in an attempt to reduce the silicon temperature. If the temperature continues to increase and exceeds the TCC activation temperature by approximately 5 ºC before the lowest ratio/VID combination has been reached, then the processor will immediately transition to the combined TM1/TM2 condition. The processor will remain in this state until the temperature has dropped below the TCC activation point. Once below the TCC activation temperature, TM1 will be discontinued and TM2 will be exited by stepping up to the appropriate ratio/VID state.

6.2.2.4 Critical Temperature Flag

If TM2 is unable to reduce the processor temperature, then TM1 will be also be activated. TM1 and TM2 will then work together to reduce power dissipation and temperature. It is expected that only a catastrophic thermal solution failure would create a situation where both TM1 and TM2 are active.

If TM1 and TM2 have both been active for greater than 20ms and the processor temperature has not dropped below the TCC activation point, then the Critical Temperature Flag in the IA32_THERM_STATUS MSR will be set. This flag is an indicator of a catastrophic thermal solution failure and that the processor cannot reduce its temperature. Unless immediate action is taken to resolve the failure, the processor will probably reach the Thermtrip temperature (see Section 6.2.3 Thermtrip Signal) within a short time. In order to prevent possible permanent silicon damage, Intel recommends removing power from the processor within ½ second of the Critical Temperature Flag being set.

6.2.2.5 PROCHOT# Signal

An external signal, PROCHOT# (processor hot), is asserted when the processor core temperature has exceeded its specification. If Adaptive Thermal Monitor is enabled (note it must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted.

The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

Although the PROCHOT# signal is an output by default, it may be configured as bi-directional. When configured in bi-directional mode, it is either an output indicating the processor has exceeded its TCC activation temperature or it can be driven from an external source (such as, a voltage regulator) to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that one or more cores has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC for all cores. TCC activation when PROCHOT# is asserted by the system will result in the processor immediately

transitioning to the minimum frequency and corresponding voltage (using Freq/VID control). Clock modulation is not activated in this case. The TCC will remain active until the system de-asserts PROCHOT#.

Use of PROCHOT# in bi-directional mode can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power.

6.2.3 THERMTRIP# Signal

Regardless of whether or not Adaptive Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in the EDS). At this point, the THERMTRIP# signal will go active and stay active as described in the EDS. THERMTRIP# activation is independent of processor activity. If THERMTRIP# is asserted, processor core voltage (V_{CC}) must be removed within the timeframe defined in EDS. The temperature at which THERMTRIP# asserts is not user configurable and is not software visible.

6.3 Intel® Turbo Boost Technology

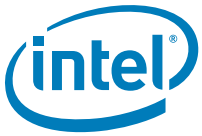
Intel® Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel® Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can utilize the thermal capacitance associated with the package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, bursty usage conditions. The turbo feature needs to be properly enabled by BIOS for the processor to operate with maximum performance. Since the turbo feature is configurable and dependent on many platform design limits outside of the processor control, the maximum performance cannot be guaranteed.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment and system design. Intel® Turbo Boost Technology may not be available on all SKUs.

6.3.1 Intel® Turbo Boost Technology Frequency

The processor’s rated frequency assumes that all execution cores are running an application at the Thermal Design Power (TDP). However, under typical operation, not all cores are active. Therefore most applications are consuming less than the TDP at the rated frequency. To take advantage of the available TDP headroom, the active cores can increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration:



- The number of cores operating in the C0 state.
- The estimated current consumption.
- The estimated power consumption.
- The temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

Note: Intel Turbo Boost Technology processor frequencies are only active if the operating system is requesting the P0 state.

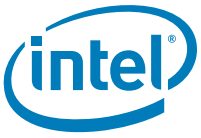
6.3.2 Intel® Turbo Boost Technology Graphics Frequency

Graphics render frequency is selected by the processor dynamically based on the graphics workload demand. The processor can optimize both processor and integrated graphics performance through managing total package power. For the integrated graphics, this could mean an increase in the render core frequency (above its base frequency) and increased graphics performance. In addition, the processor core can increase its frequency higher than it would without power sharing.

Enabling Intel® Turbo Boost Technology will maximize the performance of the processor core and the graphics render frequency within the specified package power levels. Compared with previous generation products, Intel® Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

6.4 Thermal Considerations

Intel Turbo Boost Technology allows processor cores and Processor Graphics cores to run faster than the baseline frequency. During a turbo event, the processor can exceed its TDP power for brief periods. Turbo is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery, and current specification limits. Thus, thermal solutions and platform cooling that are designed to be less than thermal design guidance may experience thermal and performance issues since more applications will tend to run at or near the maximum power limit for significant periods of time.



6.4.1 Intel® Turbo Boost Technology Power Control and Reporting

When operating in the turbo mode, the processor will monitor its own power and adjust the turbo frequency to maintain the average power within limits over a thermally significant time period. The package, processor core, and graphic core powers are estimated using architectural counters and do not rely on any input from the platform.

The behavior of turbo is dictated by the following controls that are accessible using MSR, MMIO, or PECI interfaces:

- **POWER_LIMIT_1**: TURBO_POWER_LIMIT, MSR 610h, bits 14:0. This value sets the exponentially weighted moving average power limit over a long time period. This is normally aligned to the TDP of the part and steady-state cooling capability of the thermal solution. This limit may be set lower than TDP, real-time, for specific needs, such as responding to a thermal event. If set lower than TDP, the processor may not be able to honor this limit for all workloads since this control only applies in the turbo frequency range; a very high powered application may exceed POWER_LIMIT_1, even at non-turbo frequencies. The default value is the TDP for the SKU.
- **POWER_LIMIT_1_TIME**: TURBO _POWER_LIMIT, MSR 610h, bits 23:17. This value is a time parameter that adjusts the algorithm behavior. The exponentially weighted moving average turbo algorithm will use this parameter to maintain time averaged power at or below POWER_LIMIT_1.
- **POWER_LIMIT_2**: TURBO_POWER_LIMIT, MSR 610h, bits 46:32. This value establishes the upper power limit of turbo operation above TDP, primarily for platform power supply considerations. Power may exceed this limit for up to 10 mS. The default for this limit is 1.25 x TDP.

The following considerations and limitations apply to the power monitoring feature:

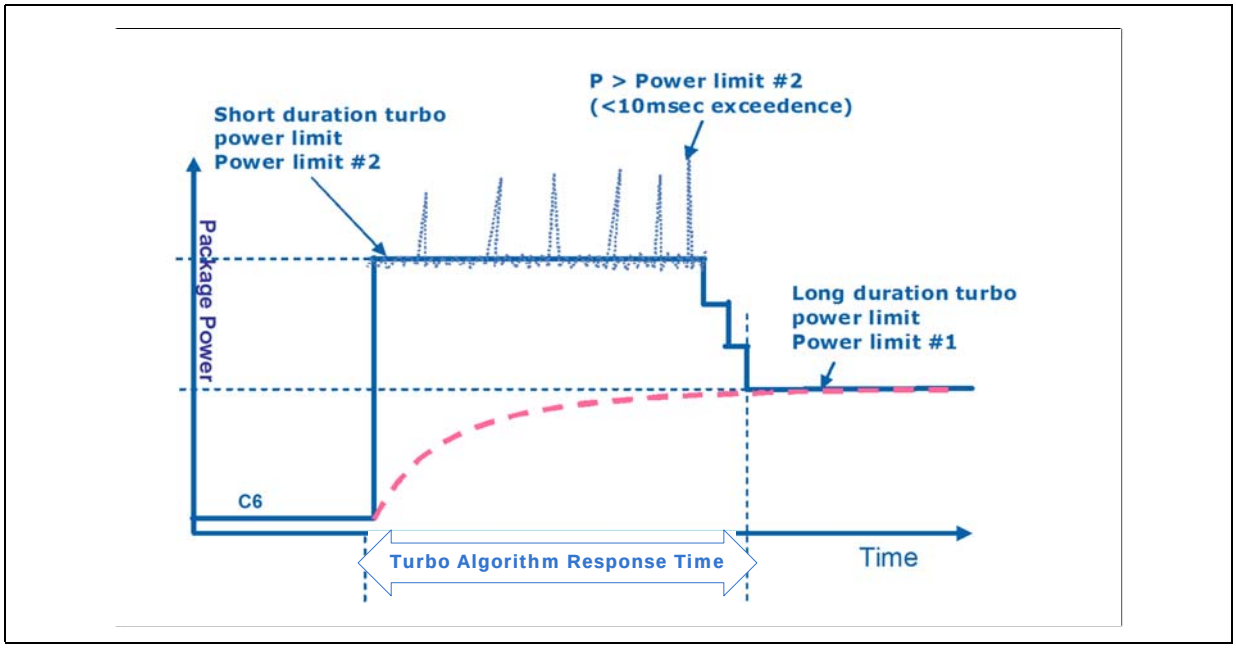
- Calibration applies to the processor family and is not conducted on a part-by-part basis. Therefore, some difference between actual and reported power may be observed.
- Power monitoring is calibrated with a variety of common, realistic workloads near Tj_max. Workloads with power characteristic markedly different from those used during the calibration process or lower temperatures may result in increased differences between actual and estimated power.
- In the event an uncharacterized workload or power “virus” application were to result in exceeding programmed power limits, the processor Thermal Control Circuitry (TCC) will protect the processor when properly enabled. Adaptive Thermal Monitor must be enabled for the processor to remain within specification.

Illustration of Intel Turbo Boost Technology power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing for customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints.

6.4.2 Package Power Control

The package power control allows for customization to implement optimal turbo within platform power delivery and package thermal solution limitations.

Figure 6-8. Package Power Control



6.4.3 Power Plane Control

The processor core and graphics core power plane controls allow for customization to implement optimal turbo within voltage regulator thermal limitations. It is possible to use these power plane controls to protect the voltage regulator from overheating due to extended high currents. Power limiting per plane cannot be guaranteed below 1 second and accuracy cannot be guaranteed in all usages. This function is similar to the package level long duration window control.

6.4.4 Turbo Time Parameter

'Turbo Time Parameter' is a mathematical parameter (units in seconds) that controls the processor turbo algorithm using an exponentially weighted moving average of energy usage. During a maximum power turbo event of about 1.25 x TDP, the processor could sustain Power_Limit_2 for up to approximately 1.5 the Turbo Time Parameter. If the power value is changed during runtime, it may take a period of time (possibly up to approximately 3 to 5 times the 'Turbo Time Parameter', depending on the magnitude of the change and other factors) for the algorithm to settle at the new control limits.

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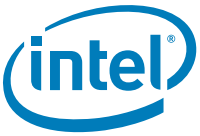

7 PECI Interface

7.1 Platform Environment Control Interface (PECI)

7.1.1 Introduction

PECI uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic '0' or logic '1'. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processors in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

The PECI bus offers:

- A wide speed range from 2 Kbps to 2 Mbps
- CRC check byte used to efficiently and atomically confirm accurate data delivery
- Synchronization at the beginning of every message minimizes device timing accuracy requirements.

For single processor temperature monitoring and fan speed control management purposes, the PECI 3.0 commands that are commonly implemented includes Ping(), GetDIB(), GetTemp(), $T_{CONTROL}$ and TjMax(TCC) read. The $T_{CONTROL}$ and TCC read command can be implemented by utilizing the RdPkgConfig() command.

7.1.1.1 Fan Speed Control with Digital Thermal Sensor

Processor fan speed control is managed by comparing DTS temperature data against the processor-specific value stored in the static variable, $T_{CONTROL}$. When the DTS temperature data is less than $T_{CONTROL}$, the fan speed control algorithm can reduce the speed of the thermal solution fan. This remains the same as with the previous guidance for fan speed control. Please refer to Section 6.1.6 for guidance where the DTS temperature data exceeds $T_{CONTROL}$.

The DTS temperature data is delivered over PECI, in response to a GetTemp() command, and reported as a relative value to TCC activation target. The temperature data reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by the PROCHOT# signal. Therefore, as the temperature approaches TCC activation, the value approaches zero degrees.

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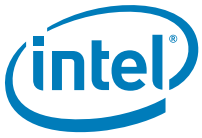


8 Sensor Based Thermal Specification Design Guidance

The sensor based thermal specification presents opportunities for the system designer to optimize the acoustics and simplify thermal validation. The sensor based specification utilizes the Digital Thermal Sensor information accessed via the PECI interface.

This chapter will review thermal solution design options, fan speed control design guidance & implementation options and suggestions on validation both with the TTV and the live die in a shipping system.

Note: A new fan speed control implementation scheme is called DTS 1.1 introduced in Section 8.4.1.

8.1 Sensor Based Specification Overview (DTS 1.0)

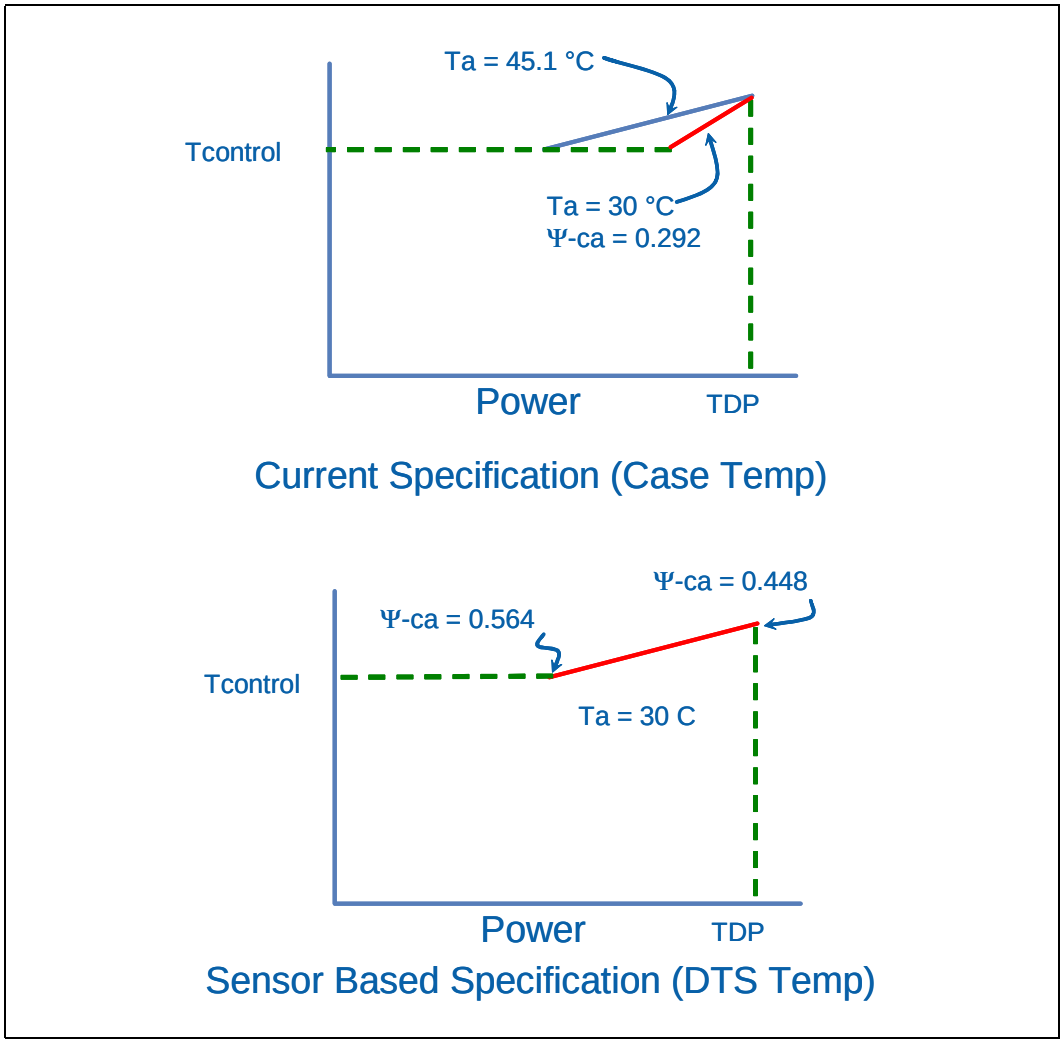
Create a thermal specification that meets the following requirements:

- Use Digital Thermal Sensor (DTS) for real-time thermal specification compliance.
- Single point of reference for thermal specification compliance over all operating conditions.
- Does not required measuring processor power and case temperature during functional system thermal validation.
- Opportunity for acoustic benefits for DTS values between $T_{CONTROL}$ and -1.

Thermal specifications based on the processor case temperature have some notable gaps to optimal acoustic design. When the ambient temperature is less than the maximum design point, the fan speed control system (FSC) will over cool the processor. The FSC has no feedback mechanism to detect this over cooling, this is shown in the top half of Figure 8-1.

The sensor based specification will allow the FSC to be operated at the maximum allowable silicon temperature or T_J for the measured ambient. This will provide optimal acoustics for operation above $T_{CONTROL}$. See lower half of Figure 8-1.

Figure 8-1. Comparison of Case Temperature vs. Sensor Based Specification



8.2 Sensor Based Thermal Specification

The sensor based thermal specification consists of two parts. The first is a thermal profile that defines the maximum TTV T_{CASE} as a function of TTV power dissipation. The thermal profile defines the boundary conditions for validation of the thermal solution.

The second part is a defined thermal solution performance (Ψ_{CA}) as a function of the DTS value as reported over the PECI bus when DTS is greater than $T_{CONTROL}$. This defines the operational limits for the processor using the TTV validated thermal solution.

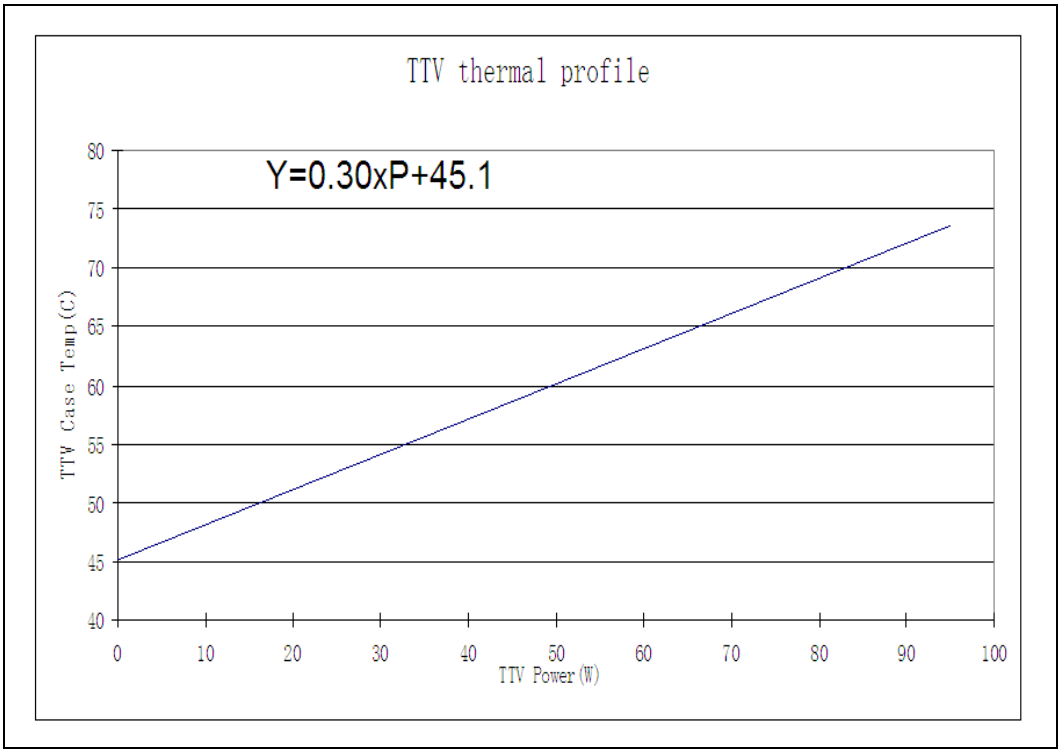
8.2.1 TTV Thermal Profile

For the sensor based specification, the only reference made to a case temperature measurement is on the TTV. Functional thermal validation will not require the user to apply a thermocouple to the processor package or measure processor power.

Note: All functional compliance testing will be based on fan speed response to the reported DTS values above $T_{CONTROL}$. As a result, no conversion of TTV T_{CASE} to processor T_{CASE} will be necessary.

A knowledge of the system boundary conditions is necessary to perform the heatsink validation. Section 8.3.1 will provide more detail on defining the boundary conditions. The TTV is placed in the socket and powered to the recommended value to simulate the TDP condition. See Figure 8-2 for an example of the Intel® Xeon® processor E3-1280 (95W) TTV thermal profile.

Figure 8-2. Intel® Xeon® Processor E3-1280 (95W) TTV Thermal Profile



Note: This graph is provided as a reference, the complete thermal specification is in Chapter 6.

8.2.2 Specification When DTS value is Greater than $T_{CONTROL}$

The product specification provides a table of Ψ_{CA} values at DTS = $T_{CONTROL}$ and DTS = -1 as a function of $T_{AMBIENT}$ (inlet to heatsink). Between these two defined points, a linear interpolation can be done for any DTS value reported by the processor.

The fan speed control algorithm has enough information using only the DTS value and $T_{AMBIENT}$ to command the thermal solution to provide just enough cooling to keep the part on the thermal profile.

In the prior thermal specifications this region, DTS values greater than $T_{CONTROL}$, was defined by the processor thermal profile. This required the user to estimate the processor power and case temperature. Neither of these two data points are accessible in real time for the fan speed control system. As a result, the designer had to assume the worst case $T_{AMBIENT}$ and drive the fans to accommodate that boundary condition.

8.3 Thermal Solution Design Process

Thermal solution design guidance for this specification is the same as with previous products. The initial design needs to take into account the target market and overall product requirements for the system. This can be broken down into several steps:

- Boundary condition definition
- Thermal design / modelling
- Thermal testing.

8.3.1 Boundary Condition Definition

Using the knowledge of the system boundary conditions (such as inlet air temperature, acoustic requirements, cost, design for manufacturing, package and socket mechanical specifications and chassis environmental test limits) the designer can make informed thermal solution design decisions.

For the thermal boundary conditions for system are as follows:

- $T_{EXTERNAL}$ = 35 °C. This is typical of a maximum system operating environment
- T_{RISE} = 5 °C.
- $T_{AMBIENT}$ = 40 °C ($T_{AMBIENT}$ = $T_{EXTERNAL}$ + T_{RISE})

Based on the system boundary conditions, the designer can select a $T_{AMBIENT}$ and Ψ_{CA} to use in thermal modelling. The assumption of a $T_{AMBIENT}$ has a significant impact on the required Ψ_{CA} needed to meet TTV $T_{CASEMAX}$ at TDP. A system that can deliver lower assumed $T_{AMBIENT}$ can utilize a design with a higher Ψ_{CA}, which can have a lower cost.

Note: If the assumed $T_{AMBIENT}$ is inappropriate for the intended system environment, the thermal solution performance may not be sufficient to meet the product requirements. The results may be excessive noise from fans having to operate at a speed higher than intended. In the worst case this can lead to performance loss with excessive activation of the Thermal Control Circuit (TCC).

8.3.2 Thermal Design and Modelling

Based on the boundary conditions, the designer can now make the design selection of the thermal solution components. The major components that can be mixed are the fan, fin geometry, heat pipe or air duct design. There are cost and acoustic trade-offs the customer can make.

To aide in the design process Intel provides TTV thermal models. Please consult your Intel Field Sales Engineer for these tools.

8.3.3 Thermal Solution Validation

8.3.3.1 Test for Compliance to the TTV Thermal Profile

This step is the same as previously suggested for prior products. The thermal solution is mounted on a test fixture with the TTV and tested at the following conditions:

- TTV is powered to the TDP condition
- Maximum airflow through heatsink
- $T_{AMBIENT}$ at the boundary condition from Section 8.3.1

The following data is collected: TTV power, TTV T_{CASE} and $T_{AMBIENT}$. and used to calculate Ψ_{CA} which is defined as:

$$\Psi_{CA} = (\text{TTV } T_{CASE} - T_{AMBIENT}) / \text{Power}$$

This testing is best conducted on a bench to eliminate as many variables as possible when assessing the thermal solution performance. The boundary condition analysis as described in Section 8.3.1 should help in making the bench test simpler to perform.

8.3.3.2 Thermal Solution Characterization for Fan Speed Control

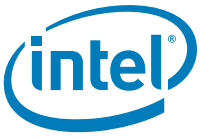
The final step in thermal solution validation is to establish the thermal solution performance,Ψ_{CA} and acoustics as a function of fan speed. This data is necessary to allow the fan speed control algorithm developer to program the device. It also is needed to asses the expected acoustic impact of the processor thermal solution in the system.

The fan speed control device may modulate the thermal solution fan speed (RPM) by one of two methods. The first and preferred is pulse width modulation (PWM) signal compliant to the 4-Wire Pulse Width Modulation (PWM) Controlled Fans specification. The alternative is varying the input voltage to the fan. As a result the characterization data needs to also correlate the RPM to PWM or voltage to the thermal solution fan. The fan speed algorithm developer needs to associate the output command from the fan speed control device with the required thermal solution performance. Regardless of which control method is used, the term RPM will be used to indicate required fan speed in the rest of this document.

8.4 Fan Speed Control (FSC) Design Process

The next step is to incorporate the thermal solution characterization data into the algorithms for the device controlling the fans.

As a reminder the requirements are:



- When the DTS value is at or below $T_{CONTROL}$, the fans can be slowed down - just as with prior processors.
- When DTS is above $T_{CONTROL}$, FSC algorithms will use knowledge of $T_{AMBIENT}$ and Ψ_{CA} vs. RPM to achieve the necessary level of cooling.

DTS 1.1 provides another option to do fan speed control without the Tambient data. Please refer to Section 8.4.1 for more details.This chapter will discuss two implementations. The first is a FSC system that is not provided the $T_{AMBIENT}$ information and a FSC system that is provided data on the current $T_{AMBIENT}$. Either method will result in a thermally compliant solution and some acoustic benefit by operating the processor closer to the thermal profile. But only the $T_{AMBIENT}$ aware FSC system can fully utilize the specification for optimized acoustic performance.

In the development of the FSC algorithm it should be noted that the $T_{AMBIENT}$ is expected to change at a significantly slower rate than the DTS value. The DTS value will be driven by the workload on the processor and the thermal solution will be required to respond to this much more rapidly than the changes in $T_{AMBIENT}$.

An additional consideration in establishing the fan speed curves is to account for the thermal interface material performance degradation over time.

8.4.1 DTS 1.1 A New Fan Speed Control Algorithm without $T_{AMBIENT}$ Data

In most system designs incorporating processor ambient inlet data in fan speed control adds design and validation complexity with a possible BOM cost impact to the system. A new fan speed control methodology is introduced to improve system acoustics without needing the processor inlet ambient information.

The DTS 1.1 implementation consists of two parts, a Ψ_{CA} requirement at $T_{CONTROL}$ and a Ψ_{CA} point at DTS = -1.

The Ψ_{CA} point at DTS = -1 defines the minimum Ψ_{CA} required at TDP considering the worst case system design Tambient design point:

$$\Psi_{CA} = (T_{CASE\_max} - T_{Ambient\ target}) / TDP$$

For example, for a 95 TDP part, the Tcase max is 72.6C and at a worst case design point of 40C local ambient this will result in

$$\Psi_{CA} = (72.6 - 40) / 95 = 0.34\ C/W$$

Similarly for a system with a design target of 45 C ambient the Ψ_{CA} at DTS = -1 needed will be 0.29 C/W.

The second point defines the thermal solution performance (Ψ_{CA}) at $T_{CONTROL}$. Figure 8-1 lists the required Ψ_{CA} for various TDP processors.

These two points define the operational limits for the processor for DTS 1.1 implementation. At $T_{CONTROL}$ the fan speed must be programed such that the resulting $\Psi_{CA}$is better than or equivalent to the required Ψ_{CA} listed in Table 8-1. Similarly the fan speed should be set at DTS = -1 such that the thermal solution performance is better than or equivalent to the Ψ_{CA}requirements **at Tambient_Max.** Based on the processor temperature, the fan speed controller must linearly change the fan speed from DTS = $T_{CONTROL}$ to DTS = -1 between these points. Figure 8-3 gives a visual description on DTS 1.1.

Figure 8-3. DTS 1.1 Definition Points

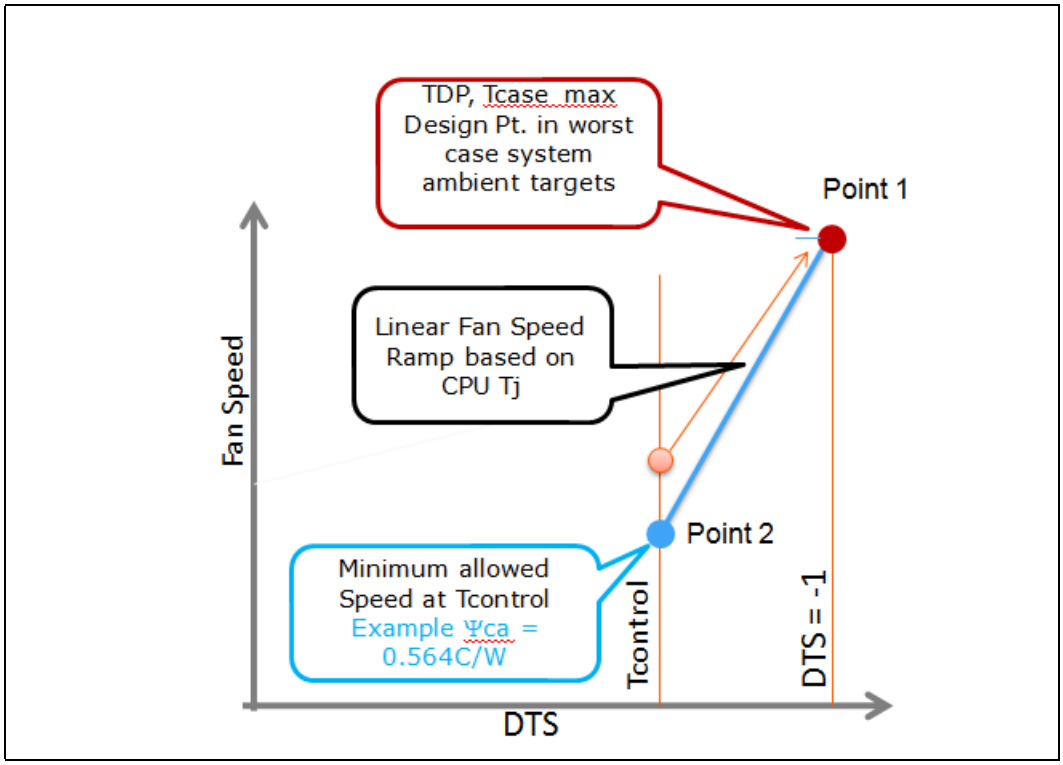


Table 8-1. DTS 1.1 Thermal Solution Performance above $T_{CONTROL}$

Processor TDP	Ψ_{CA} at DTS = $T_{CONTROL}$ [1,2]	Ψ_{CA} at DTS = -1 At System ambient_max= 40C	Ψ_{CA} at DTS = -1 At System ambient_max= 45C	Ψ_{CA} at DTS = -1 At System ambient_max= 50C
95W(no graphic)	0.569	0.354	0.300	0.248
95W(with graphic)	0.564	0.343	0.291	0.238
80W (no graphic)	0.620	0.364	0.300	0.238
45W(with graphic)	0.869	0.413	0.301	0.191
20W(no graphic)	3.713	1.875	1.625	1.375

Notes:

1. Ψ_{CA} at "DTS = $T_{control}$" is applicable to systems that has Internal Trise (Troom temperature to Processor cooling fan inlet) of less than 10 °C. In case your expected Trise is grater than 10 °C a correction factor should be used as explained below. For each 1 °C Trise above 10 °C, the correction factor CF is defined as CF= 1.7 / Processor_TDP.
2. Example, For A Chassis Trise assumption of 12 °C for a 95W TDP processor.
   CF = 1.7/95 W = 0.018/C
   For Trise > 10 C
   ΨCA at Tcontrol = Value listed in Column_2 - (Trise - 10) * CF
   ΨCA = 0564 - (12 - 10) * 0.018 =0.528 C/W
   In this case the fan speed should be set slightly higher equivalent to YCA=0.528C/W

8.5 System Validation

System validation should focus on ensuring the fan speed control algorithm is responding appropriately to the DTS values and $T_{AMBIENT}$ data in the case of DTS 1.0 as well as any other device being monitored for thermal compliance.

Since the processor thermal solution has already been validated using the TTV to the thermal specifications at the predicted $T_{AMBIENT}$, additional TTV based testing in the chassis is not necessary.

Once the heatsink has been demonstrated to meet the TTV Thermal Profile, it should be evaluated on a functional system at the boundary conditions.

In the system under test and Power/Thermal Utility Software set to dissipate the TDP workload confirm the following item:

- Verify if there is TCC activity by instrumenting the PROCHOT# signal from the processor. TCC activation in functional application testing is unlikely with a compliant thermal solution. Some very high power applications might activate TCC for short intervals this is normal.
- Verify fan speed response is within expectations - actual RPM (Ψ_{CA}) is consistent with DTS temperature and $T_{AMBIENT}$.
- Verify RPM versus PWM command (or voltage) output from the FSC device is within expectations.
- Perform sensitivity analysis to asses impact on processor thermal solution performance and acoustics for the following:
  - Other fans in the system.
  - Other thermal loads in the system.

In the same system under test, run real applications that are representative of the expected end user usage model and verify the following:

- Verify fan speed response vs. expectations as done using Power/Thermal Utility SW
- Validate system boundary condition assumptions: Trise, venting locations, other thermal loads and adjust models / design as required.

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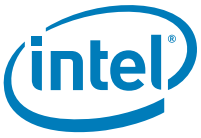
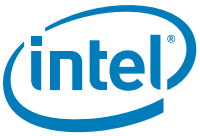




9 1U Thermal Solution

Note: The thermal mechanical solution information shown in this document represents the current state of the data and may be subject to modification.The information represents design targets, not commitments by Intel.

This section describes the overall requirements for enabled thermal solutions designed to cool the Intel® Xeon® Processor E3-1200 product family including critical to function dimensions, operating environment and validation criteria in 1U server system. Intel has developed two different collaboration/reference 1U thermal solutions to meet the cooling needs in this document.

9.1 Performance Targets

Table 9-1 provides boundary conditions and performance targets for a 1U heatsink to cool processor in 1U server. These values are used to provide guidance for heatsink design.

Table 9-1. Boundary Conditions and Performance Targets

Processor	Altitude	Thermal Design Power	T_{LA}	Ψ_{ca}[2]	Air Flow[3]	Pressure Drop[4]
Intel® Xeon® processor E3-1280 (95W)	Sea Level	95W	40.0°C	0.353°C/W	15CFM	0.383
Intel® Xeon® processor E3-1200 (80W)	Sea Level	80W	40.8°C	0.353°C/W	15CFM	0.383
Intel® Xeon® processor E3-1260L (45W)	Sea Level	45W	42.7°C	0.353°C/W	15CFM	0.383
Intel® Xeon® processor E3-1220L (20W)	Sea Level	20W	67.0°C	0.527°C/W	10CFM	0.123

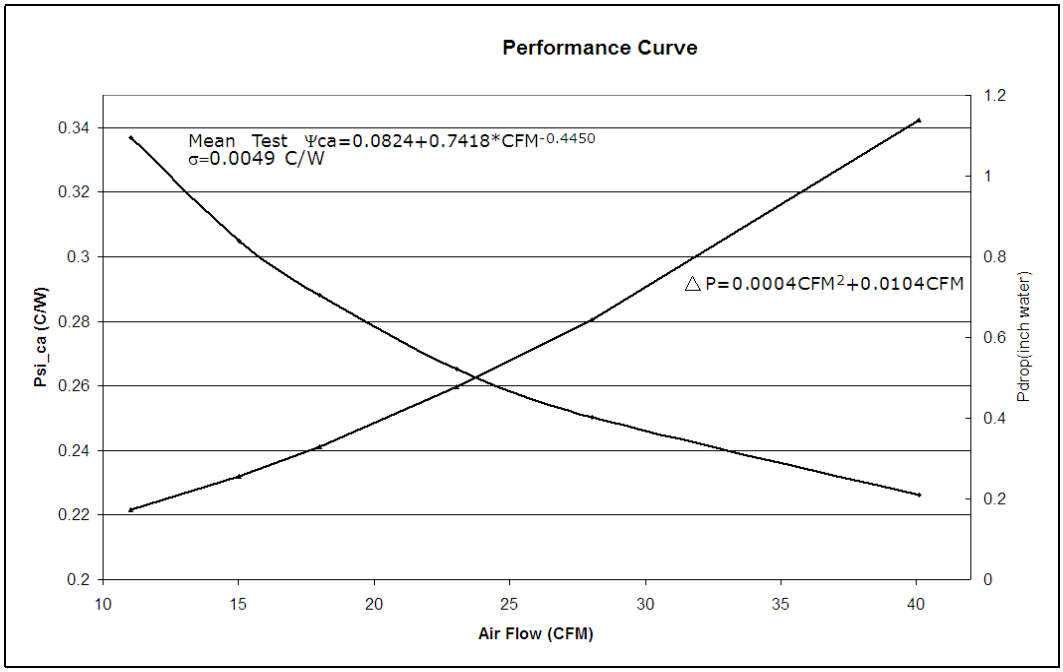
Notes:
1. The values in Table 9-1 are from preliminary design review.
2. Max target (mean + 3 sigma) for thermal characterization parameter.
3. Airflow through the heatsink fins with zero bypass.
4. Max target for pressure drop (dP) measured in inches H_2O.

9.2 1U Collaboration Heatsink

9.2.1 Heatsink Performance

For 1U collaboration heatsink, see Appendix B for detailed drawings. Figure 9-1 shows $\Psi_{CA}$and pressure drop for the 1U collaboration heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

Figure 9-1. 1U Collaboration Heatsink Performance Curves



Collaboration thermal solution Ψca (mean+3sigma) is computed to 0.319°C/W at the airflow of 15 CFM. As the Table 9-1 shown when T_{LA} is 40 °C, equation representing thermal solution of this heatsink is calculated as:

$$Y=0.319*X+40$$

where,

Y = Processor T_{CASE} Value (°C)

X = Processor Power Value (W)

Table 9-2 shows thermal solution performance is compliant with Intel® Xeon® processor E3-1280 (95W) TTV thermal profile specification. At the TDP (95W) with local ambient of 40°C, there is a 3.3°C margin.

Figure 9-2. 1U Collaboration Heatsink Performance Curves

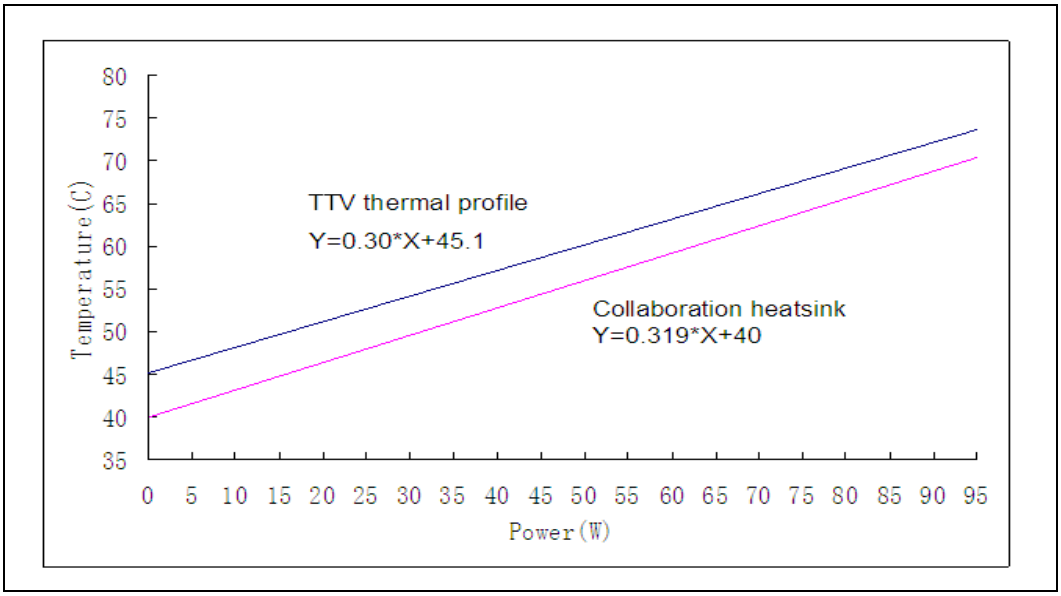


Table 9-2. Comparison between TTV Thermal Profile and Thermal Solution Performance for Intel® Xeon® Processor E3-1280 (95W) (Sheet 1 of 2)

Power (W)	TTV T_{CASE_MAX} (°C)	Thermal Solution T_{CASE_MAX} (°C)	Power (W)	TTV T_{CASE_MAX} (°C)	Thermal Solution T_{CASE_MAX} (°C)
0	45.1	40.0	50	60.1	56.0
2	45.7	40.6	52	60.7	56.6
4	46.3	41.3	54	61.3	57.2
6	46.9	41.9	56	61.9	57.9
8	47.5	42.6	58	62.5	58.5
10	48.1	43.2	60	63.1	59.1
12	48.7	43.8	62	63.7	59.8
14	49.3	44.5	64	64.3	60.4
16	49.9	45.1	66	64.9	61.1
18	50.5	45.7	68	65.5	61.7
20	51.1	46.4	70	66.1	62.3
22	51.7	47.0	72	66.7	63.0
24	52.3	47.7	74	67.3	63.6
26	52.9	48.3	76	67.9	64.2
28	53.5	48.9	78	68.5	64.9
30	54.1	49.6	80	69.1	65.5
32	54.7	50.2	82	69.7	66.2
34	55.3	50.8	84	70.3	66.8

Table 9-2. Comparison between TTV Thermal Profile and Thermal Solution Performance for Intel® Xeon® Processor E3-1280 (95W) (Sheet 2 of 2)

Power (W)	TTV T_{CASE_MAX} (°C)	Thermal Solution T_{CASE_MAX} (°C)	Power (W)	TTV T_{CASE_MAX} (°C)	Thermal Solution T_{CASE_MAX} (°C)
36	55.9	51.5	86	70.9	67.4
38	56.5	52.1	88	71.5	68.1
40	57.1	52.8	90	72.1	68.7
42	57.7	53.4	92	72.7	69.3
44	58.3	54.0	94	73.3	70.0
46	58.9	54.7	95	73.6	70.3
48	59.5	55.3			

9.2.2 Thermal Solution

The collaboration thermal solution consists of two assemblies: heatsink assembly & back plate.

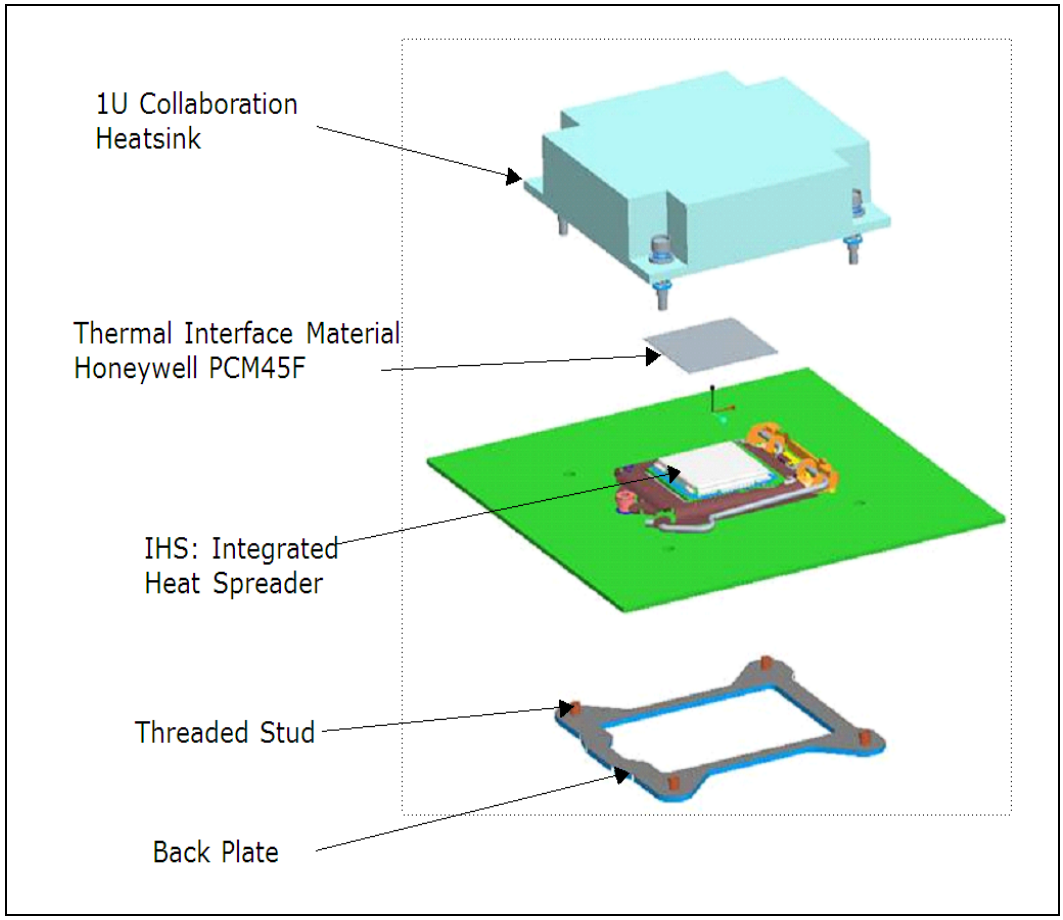
Heatsink is designed with the Aluminum base and Aluminum stack fin, which volumetrically is 95x95x24.85 mm. The heatpipe technology is used in the heatsink to improve thermal conduction.

Heatsink back plate is a 1.8 mm thick flat steel plate with threaded studs for heatsink attach. A clearance hole is located at the center of the heatsink backplate to accommodate the ILM back plate. An insulator is pre-applied.

Note: Heatsink back plate herein is only applicable to 1U server. Desktop has a specific heatsink back plate for its form factor.

9.2.3 Assembly

Figure 9-3. 1U Collaboration Heatsink Assembly



The assembly process for the 1U collaboration heatsink with application of thermal interface material begins with placing back plate in a fixture. The motherboard is aligned with fixture.

Next is to place the heatsink such that the heatsink fins are parallel to system airflow. While lowering the heatsink onto the IHS, align the four captive screws of the heatsink to the four holes of motherboard.

Using a #2 Phillips driver, torque the four captive screws to 8 inch-pounds.

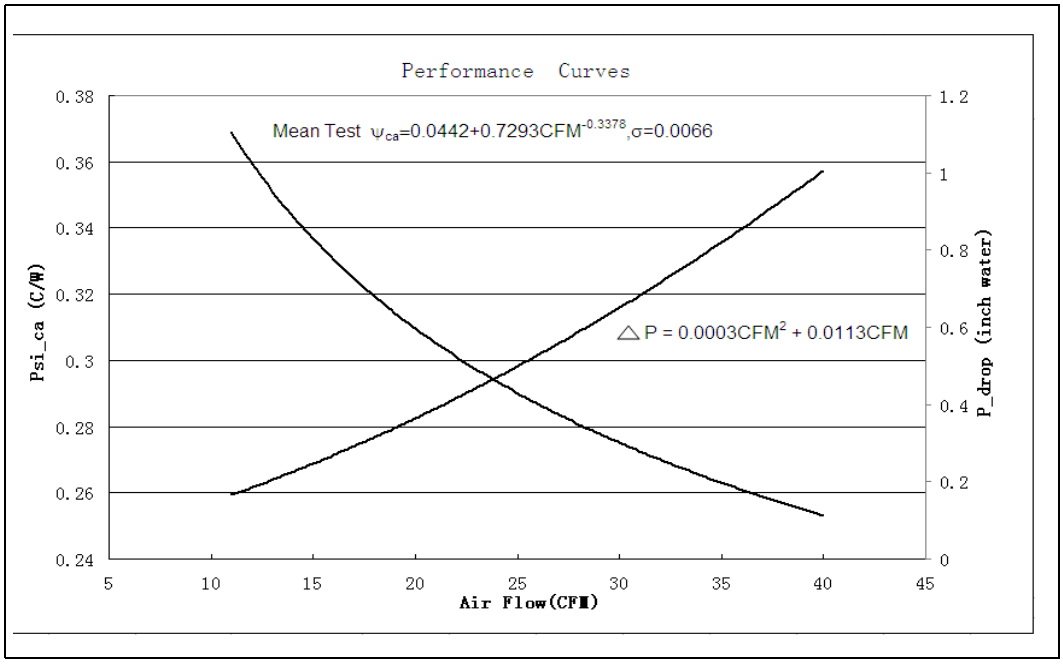
This assembly process is designed to produce a static load compliant with the minimum preload requirement (26.7 lbf) for the selected TIM and to not exceed the package design limit (50 lbf).

9.3 1U Reference Heatsink

9.3.1 Heatsink Performance

For 1U reference heatsink, see Appendix B for detailed drawings. Figure 9-4 shows $\Psi_{CA}$and pressure drop for the 1U reference heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

Figure 9-4. 1U Reference Heatsink Performance Curves



This 1U Reference thermal solution Ψca(mean+3sigma) is computed to 0.353°C/W at the airflow of 15.5 CFM, which just meets Intel® Xeon® processor E3-1280 (95W) TTV thermal profile specification when T_{LA} is 40 °C.

9.3.2 Thermal Solution

The reference thermal solution consists of two assemblies: heatsink assembly & back plate.

Heatsink is designed with extruded Aluminum, which volumetrically is 95x95x24.85 mm with total 43 fins. Please refer to Appendix B for detailed drawings.

Heatsink back plate is a 1.8 mm thick flat steel plate with threaded studs for heatsink attach. A clearance hole is located at the center of the heatsink backplate to accommodate the ILM back plate. An insulator is pre-applied.

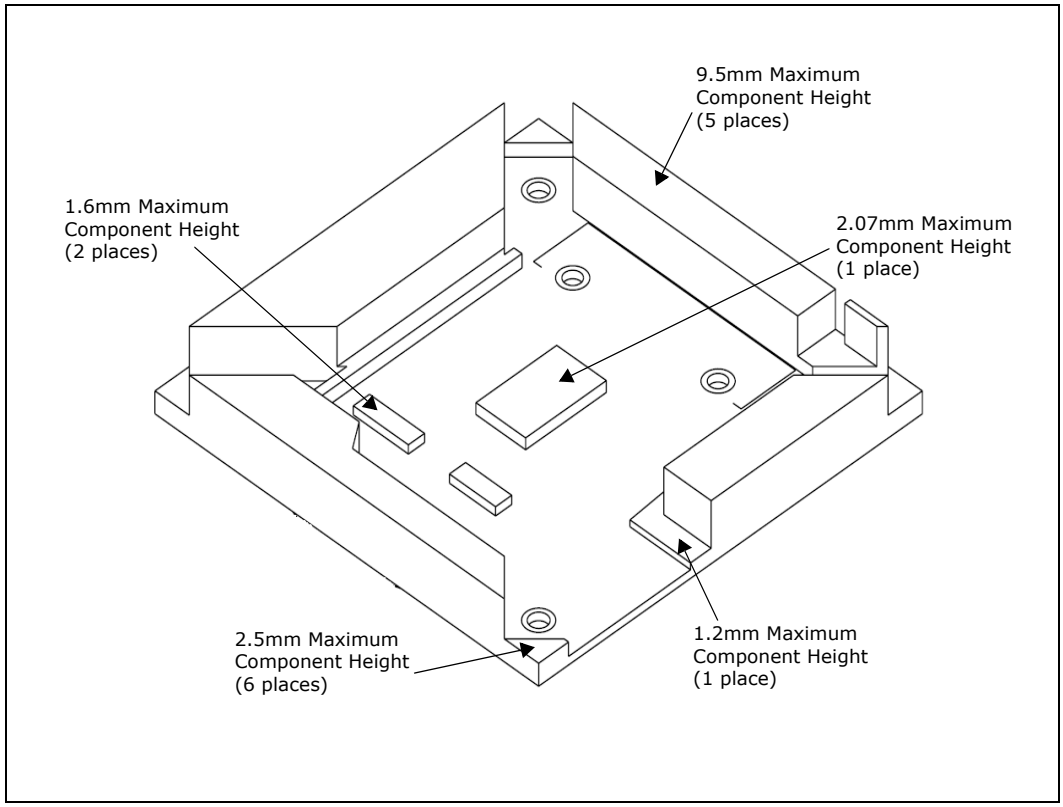
Note: Heatsink back plate herein is only applicable to 1U server. Desktop has a specific heatsink back plate for its form factor.

9.3.3 Assembly

The assembly process is same as the way described in Section 9.2.3, please refer to it for more details.

9.4 Geometric Envelope for 1U Thermal Mechanical Design

Figure 9-5. KOZ 3-D Model (Top) in 1U Server



9.5 Thermal Interface Material

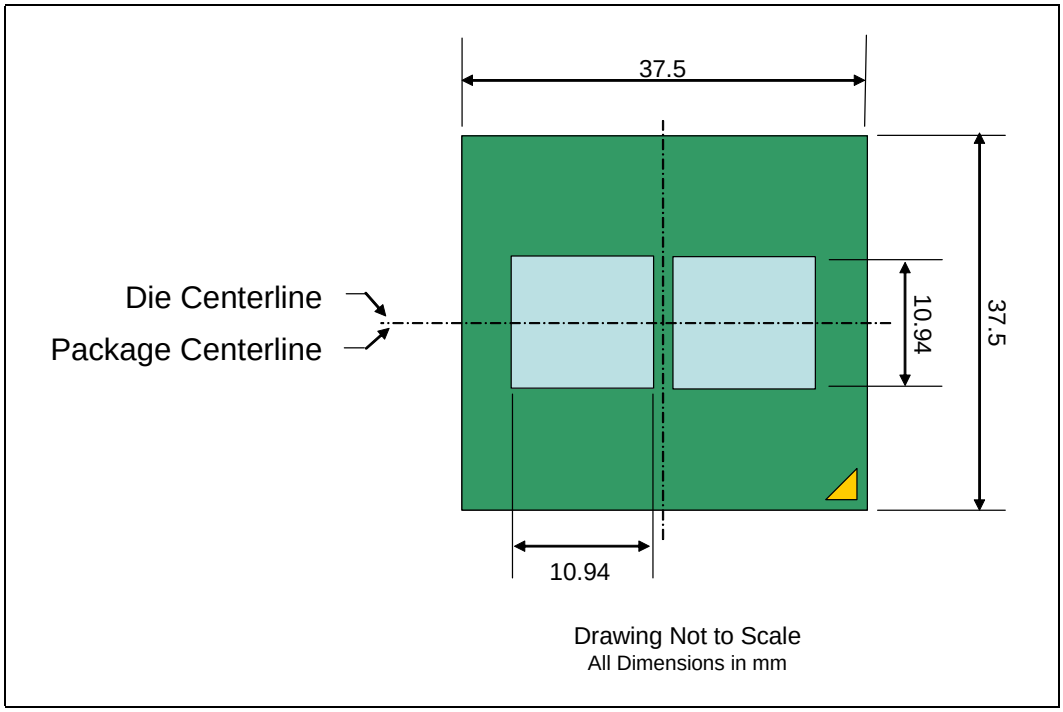
A thermal interface material (TIM) provides conductivity between the IHS and heatsink. The collaboration thermal solution uses Honeywell PCM45F, which pad size is 35x35 mm.

TIM should be verified to be within its recommended shelf life before use. Surfaces should be free of foreign materials prior to application of TIM.

9.6 Heat Pipe Thermal Consideration

The following drawing shows the orientation and position of the 1155-land LGA Package TTV die, this is the same package layout as used in the 1156-land LGA Package TTV. The TTV die is sized and positioned similar to the production die.

Figure 9-6. TTV Die Size and Orientation



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10 Active Tower Thermal Solution

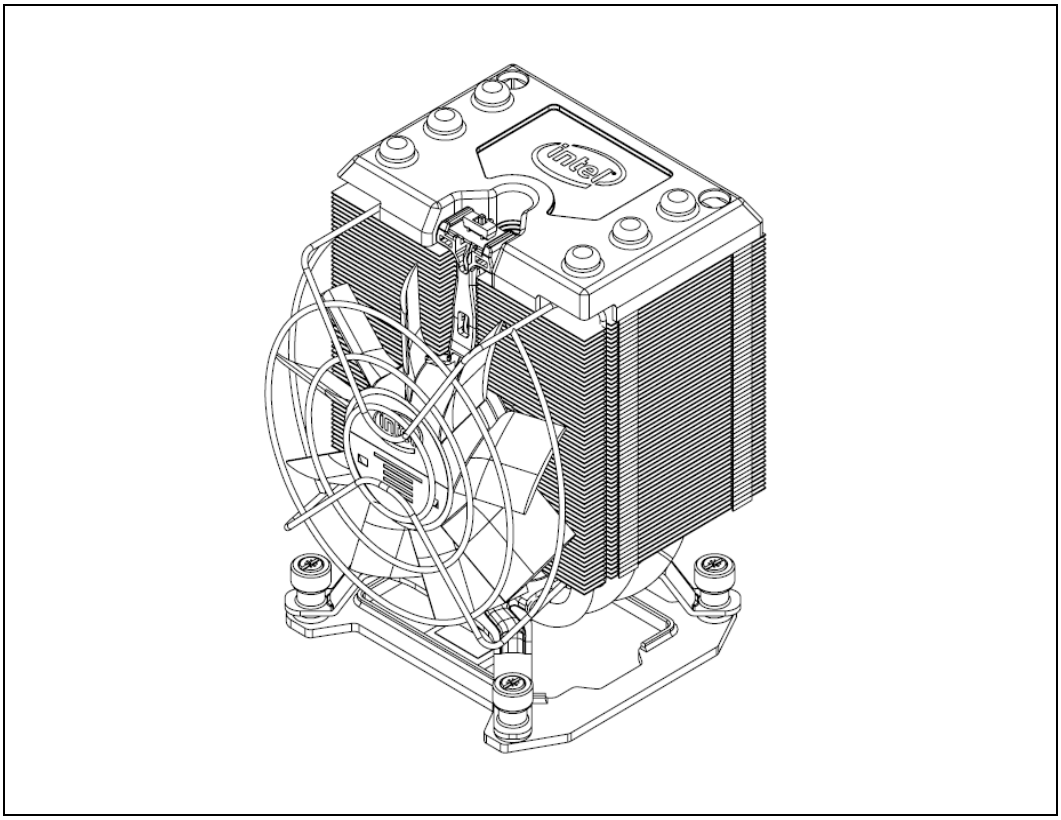
10.1 Introduction

This active tower thermal solution is intended for system integrators who build systems from baseboards and standard components. This chapter documents baseboard and system requirements for the cooling solution. It is particularly important for OEMs that manufacture baseboards for system integrators.

Note: Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets]. Figure 10-1 shows a mechanical representation of the active tower thermal solution.

Note: Drawings in this chapter reflect only the specifications on this active tower thermal solution. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designers' responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platforms and chassis. Refer to the desktop processor thermal mechanical design guide for further guidance on keep in and keep out zones.

Figure 10-1. Mechanical Representation of the Solution



10.2 Mechanical Specifications

10.2.1 Cooling Solution Dimensions

This section documents the mechanical specifications. Figure 10-1 shows a mechanical representation of the solution.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the processor with assembled thermal solution are shown in Figure 10-2 (Side View), and Figure 10-3 (Top View). The airspace requirements for this active tower heatsink must also be incorporated into new baseboard and system designs. Note that some figures have centerlines shown (marked with alphabetic designations) to clarify relative dimensioning.

Figure 10-2. Physical Space Requirements for the Solution (side view)

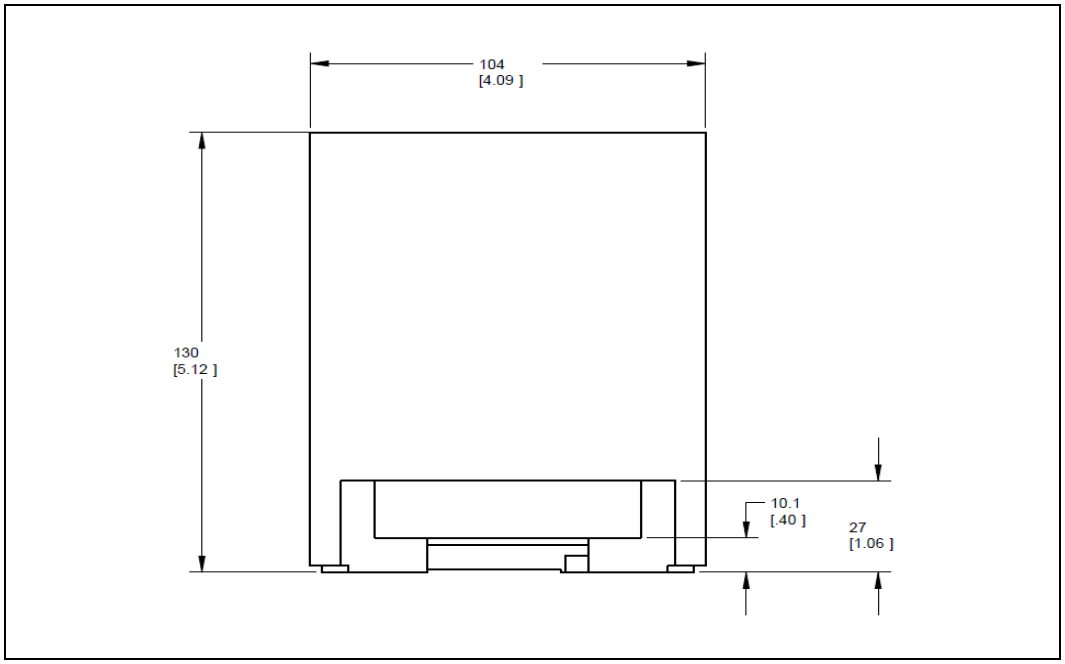
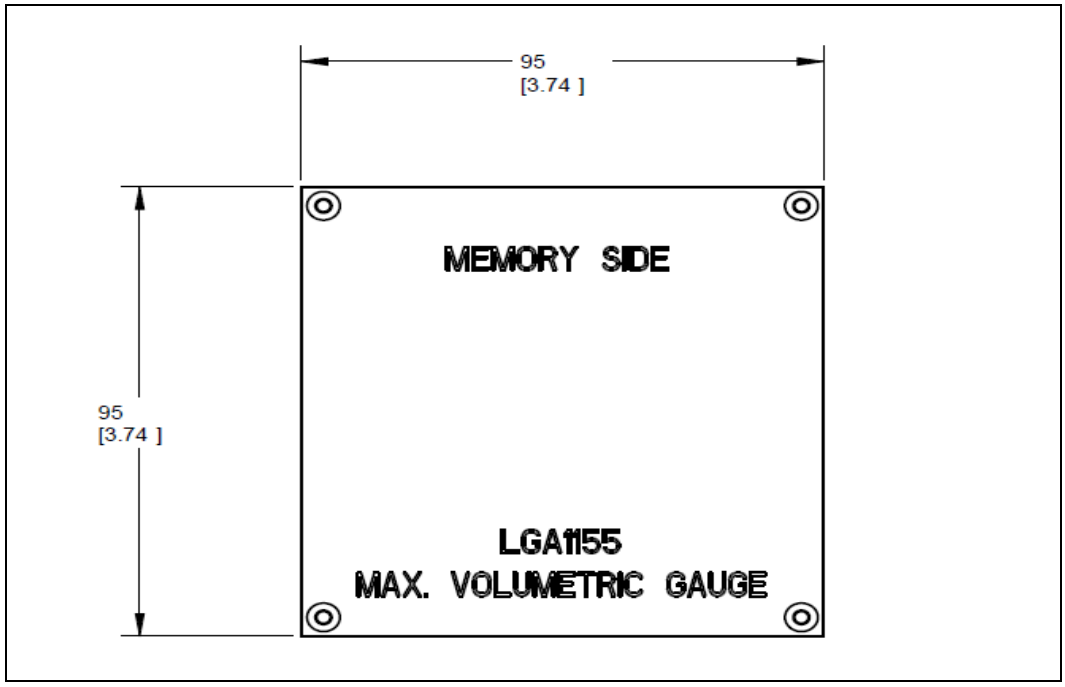


Figure 10-3. Physical Space Requirements for the Solution (top view)



Note: Diagram does not show the attached hardware for the clip design and is provided only as a mechanical representation.

10.2.2 Retention Mechanism and Heatsink Attach Clip Assembly

The thermal solution requires a heatsink attach clip assembly, to secure the processor and fan heatsink in the baseboard socket.

10.3 Electrical Requirements

10.3.1 Active Tower Heatsink Power Supply

The active tower heatsink requires a +12 V power supply. A fan power cable will be with solution to draw power from a power header on the baseboard. The power cable connector and pinout are shown in Figure 10-4. Baseboards must provide a matched power header to support this. Table 10-1 contains specifications for the input and output signals at the heatsink connector.

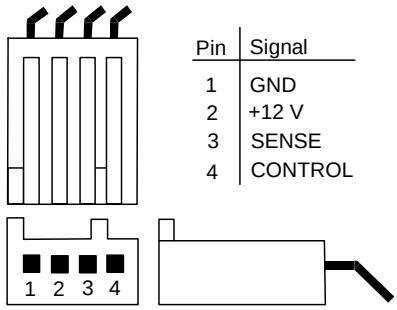
The active tower heatsink outputs a SENSE signal, which is an open- collector output that pulses at a rate of 2 pulses per fan revolution. A baseboard pull-up resistor provides VOH to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The fan heatsink receives a PWM signal from the motherboard from the 4th pin of the connector labeled as CONTROL.

The active tower heatsink requires a constant +12 V supplied to pin 2 and does not support variable voltage control or 3-pin PWM control.

The power header on the baseboard must be positioned to allow the fan power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 10-5 shows the location of the fan power connector relative to the processor socket. The baseboard power header should be positioned within 110 mm [4.33 inches] from the center of the processor socket.

Figure 10-4. Fan Power Cable Connector Description



Straight square pin, 4-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pitch, 0.025" square pin width.

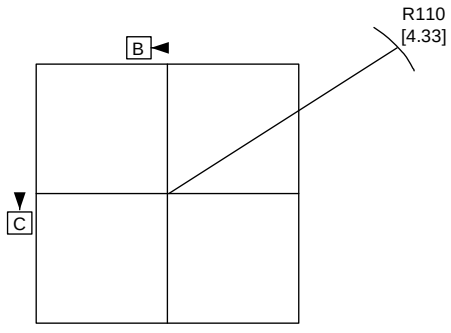
Match with straight pin, friction lock header on mainboard.

Table 10-1. Fan Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12V: 12 volt fan power supply	9.0	12.0	13.8	V	—
IC: • Maximum fan steady-state current draw • Maximum fan start-up current draw	 — —	 1.2 3.0	 — —	 A A	—
SENSE: SENSE frequency	—	2	—	pulses per fan revolution	1
CONTROL	21	25	28	kHz	2, 3

Notes:
1. Baseboard should pull this pin up to 5V with a resistor.
2. Open drain type, pulse width modulated.
3. Fan will have pull-up resistor for this signal to maximum of 5.25 V.

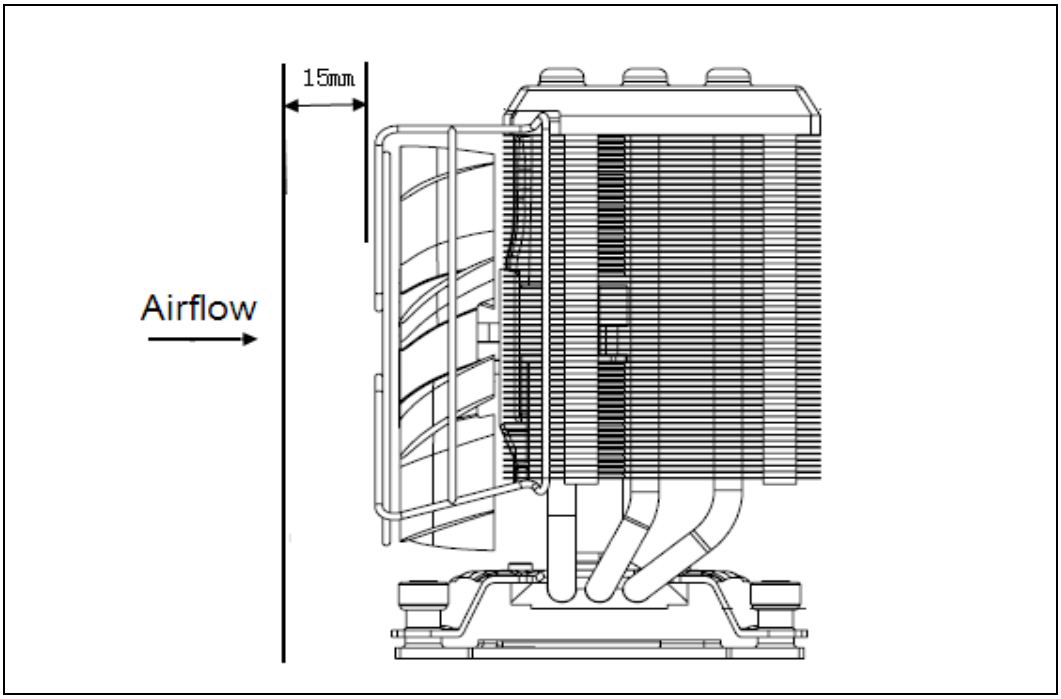
Figure 10-5. Baseboard Power Header Placement Relative to Processor Socket



10.4 Cooling Requirements

The processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 6 of this document. The active tower heatsink is able to keep the processor temperature within the specifications (see Table 6-1) in chassis that provide good thermal management. For fan heatsink to operate properly, it is critical that the airflow provided to the heatsink is unimpeded. Airflow of the fan heatsink is into the front of fan and straight out of the heatsink rear side. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 10-6 illustrate an acceptable front airspace clearance for the fan heatsink which is recommended to at least 15 mm or larger. The air temperature entering the fan should be kept below 40 ºC. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

Figure 10-6. Active Tower Heatsink Airspace Keepout Requirements (side view)



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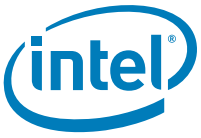
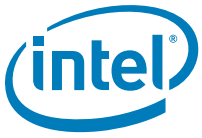




11 Thermal Solution Quality and Reliability Requirements

11.1 Reference Heatsink Thermal Verification

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. The Intel reference thermal solution will be evaluated to the boundary conditions in Chapter 5.

The test results, for a number of samples, are reported in terms of a worst-case mean + 3σ value for thermal characterization parameter using the TTV.

11.2 Mechanical Environmental Testing

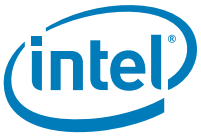
Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 11-1.

The Intel reference heatsinks will be tested in an assembled to the LGA1155 socket and mechanical test package. Details of the Environmental Requirements, and associated stress tests, can be found in Table 11-1 are based on speculative use condition assumptions, and are provided as examples only.

Table 11-1. Use Conditions (Board Level)

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	3 drops each for + and - directions in each of 3 perpendicular axes (that is, total 18 drops) Profile: 50 g, Trapezoidal waveform, 4.3 m/s [170 in/s] minimum velocity change	Visual Check and Electrical Functional Test
Random Vibration	Duration: 10 min/axis, 3 axes Frequency Range: 5 Hz to 500 Hz 5 Hz @ 0.01 g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up) 20 Hz to 500 Hz @ 0.02 g^2/Hz (flat) Power Spectral Density (PSD) Profile: 3.13 g RMS	Visual Check and Electrical Functional Test
Thermal Cycling	–25°C to +100°C;Ramp rate ~ 8C/minute; Cycle time:~30 minutes per cycle for 500 cycles.	Visual Check and Thermal Performance Test

Notes:
1. It is recommended that the above tests be performed on a sample size of at least ten assemblies from multiple lots of material.
2. Additional pass/fail criteria may be added at the discretion of the user.



11.2.1 Recommended Test Sequence

Each test sequence should start with components (that is, baseboard, heatsink assembly, and so on) that have not been previously submitted to any reliability testing.

Prior to the mechanical shock & vibration test, the units under test should be preconditioned for 72 hours at 45 ºC. The purpose is to account for load relaxation during burn-in stage.

The test sequence should always start with a visual inspection after assembly, and BIOS/Processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/Processor/memory test.

11.2.2 Post-Test Pass Criteria

The post-test pass criteria are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flatly against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

11.2.3 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. *Intel PC Diags* is an example of software that can be utilized for this test.

11.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (such as polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Material used shall not have deformation or degradation in a temperature life test.

Any plastic component exceeding 25 grams should be recyclable per the European Blue Angel recycling standards.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

RoHS compliant: Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.

Note: RoHS implementation details are not fully defined and may change.

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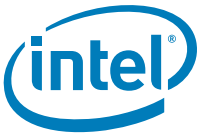

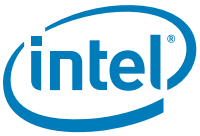

A Component Suppliers

Note: The part numbers listed below identifies the reference components. End-users are responsible for the verification of the Intel enabled component offerings with the supplier. These vendors and devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. Customers are responsible for thermal, mechanical, and environmental validation of these solutions. This list and/or these devices may be subject to change without notice.

Table A-1. Collaboration Heatsink Enabled Components-1U Server

Item	Intel PN	AVC
1U Collaboration heatsink Assembly	E49069-001	SQ41900001
1U Reference Heatsink Assembly	E95498-001	SQ00S00001
Heatsink Back Plate Assembly	E49060-001	P209000071

Table A-2. Reference Heatsink - Workstation

Item	Intel PN	Delta	Foxconn	Nidec
DHA-A Heatsink Assembly (Active)	E41759-002	DTC-DAA07	1A01C7T00-DHA_XA02	F90T12MS1Z7-64A01A1
DHX-B Socket H Compatible Xtreme Edition	E88216-001	n/a	1A01GQ110-DHX	n/a

Table A-3. Reference Heatsink Components- Workstation

Item	Intel PN	AVC	ITW
DHA-A Heatsink Clip	E36830-001	A208000389	n/a
DHA-A Fastener	E49060-001	n/a	Base: C33389 Cap: C33390

Table A-4. LGA1155 Socket and ILM Components (Sheet 1 of 2)

Item	Intel PN	Foxconn	Molex	Tyco	Lotes
LGA1155 Socket	E52846-002	PE115527-4041-01F	475962032	2069570-1	N/A
LGA115x ILM without cover	E36142-002	PT44L61-6401	475969911	2013882-3	ACA-ZIF-078-Y02
LGA115x ILM with cover	G11449-001	PT44L81-6401	475968711	2013882-5	ACA-ZIF-078-Y17

Table A-4. LGA1155 Socket and ILM Components (Sheet 2 of 2)

Item	Intel PN	Foxconn	Molex	Tyco	Lotes
LGA115x ILM cover only	G12451-001	012-1000-5377	475973003	1-2134503-1	ACA-ZIF-127-P01
LGA115x ILM Back Plate (with screws)	E36143-002	PT44P19-6401	475969930	2069838-2	DCA-HSK-144-Y09
1U ILM Back Plate (with Screws)	E66807-001	PT44P18-6401	N/A	N/A	DCA-HSK-157-Y03

Table A-5. Supplier Contact Information

Supplier	Contact	Phone	Email
AVC (Asia Vital Components Co., Ltd.)	Kai Chang	+86 755 3366 8888 x63588	kai_chang@avc.com.tw
Delta	William Bradshaw	+1 510 668-5570 +86 136 8623 1080	WBradshaw@delta-corp.com
Foxconn	Julia Jiang (for socket and ILM) Ray Wang (for heatsink)	+1 408 919 6178 +1 512 670 2638	juliaj@foxconn.com ray.wang@foxconn.com
ITW Fastex	Chak Chakir	+1 512 989 7771	Chak.chakir@itweba.com
Lotes Co., Ltd.	Windy Wong	+1 604 721 1259	windy@lotestech.com
Molex	Carol Liang	+86 21 504 80889 x3301	carol.liang@molex.com
Nidec	Karl Mattson	+1 360 666 2445	karl.mattson@nidec.com
Tyco	Billy Hsieh	+81 44 844 8292	billy.hsieh@tycoelectronics.com

The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.

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B Mechanical Drawings

Table B-1 lists the mechanical drawings included in this appendix.

Table B-1. Mechanical Drawing List

Drawing Description	Figure Number
Socket / Heatsink / ILM Keepout Zone Primary Side for 1U (Top)	Figure B-1
Socket / Heatsink / ILM Keepout Zone Secondary Side for 1U (Bottom)	Figure B-2
Socket / Processor / ILM Keepout Zone Primary Side for 1U (Top)	Figure B-3
Socket / Processor / ILM Keepout Zone Secondary Side for 1U (Bottom)	Figure B-4
1U Collaboration Heatsink Assembly	Figure B-5
1U Collaboration Heatsink	Figure B-6
1U Reference Heatsink Assembly	Figure B-7
1U Reference Heatsink	Figure B-8
1U Heatsink Screw	Figure B-9
Heatsink Compression Spring	Figure B-10
Heatsink Load Cup	Figure B-11
Heatsink Retaining Ring	Figure B-12
Heatsink Backplate Assembly	Figure B-13
Heatsink Backplate	Figure B-14
Heatsink Backplate Insulator	Figure B-15
Heatsink Backplate Stud	Figure B-16
Thermocouple Attach Drawing	Figure B-17
1U ILM Shoulder Screw	Figure B-18
1U ILM Standard 6-32 Thread Fastener	Figure B-19

Figure B-1. Socket / Heatsink / ILM Keepout Zone Primary Side for 1U (Top)

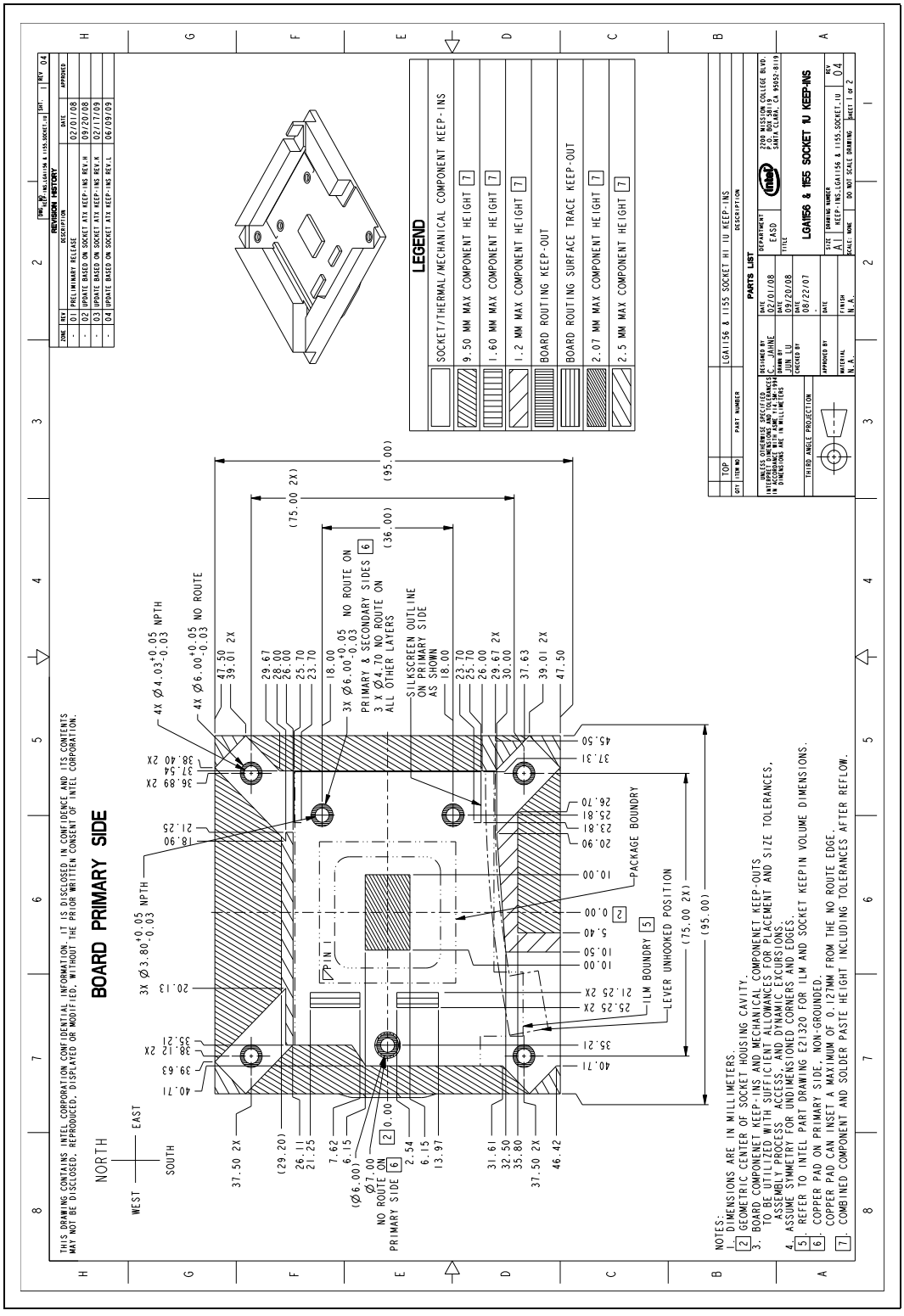


Figure B-2. Socket / Heatsink / ILM Keepout Zone Secondary Side for 1U (Bottom)

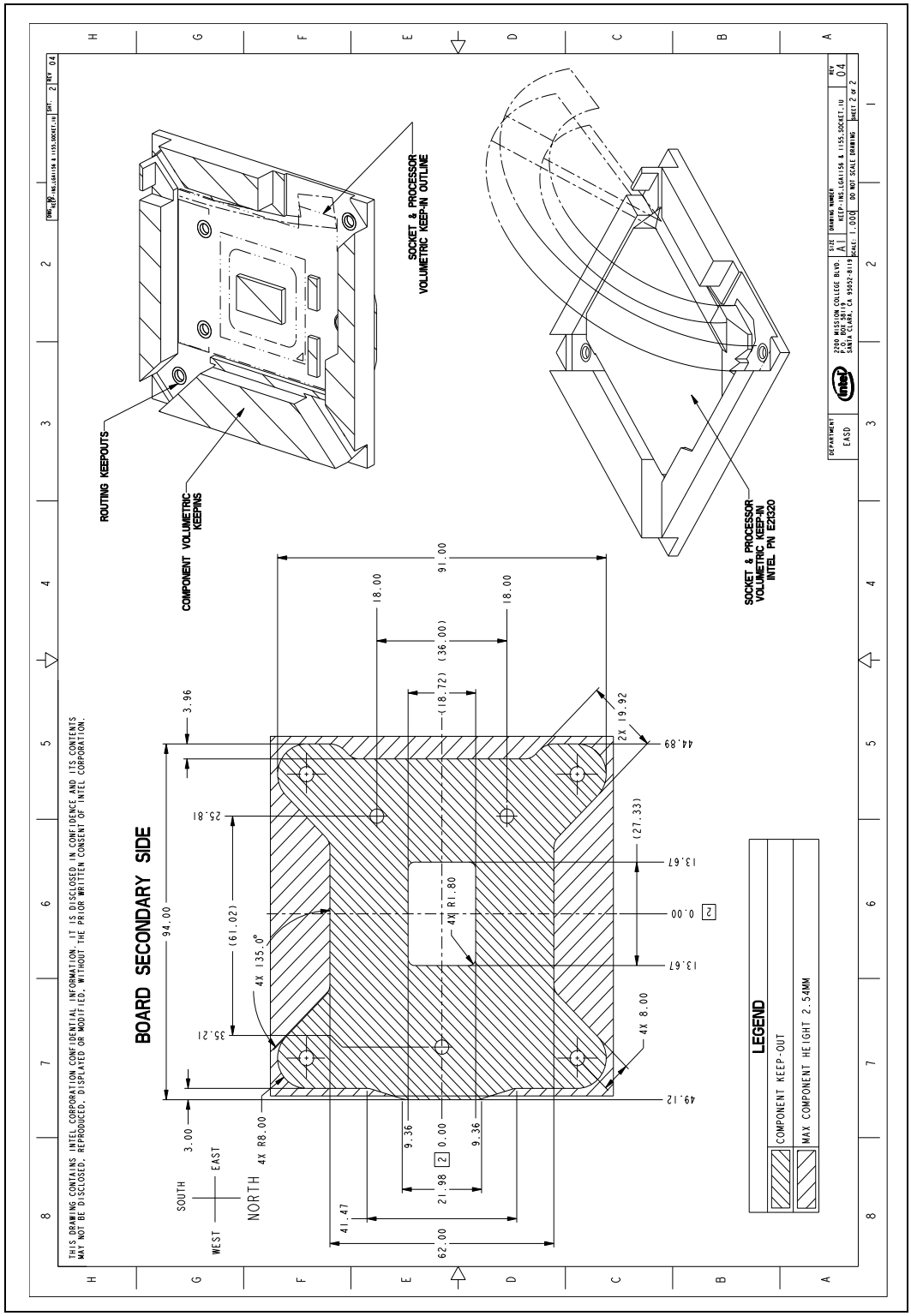


Figure B-3. Socket / Processor / ILM Keepout Zone Primary Side for 1U (Top)

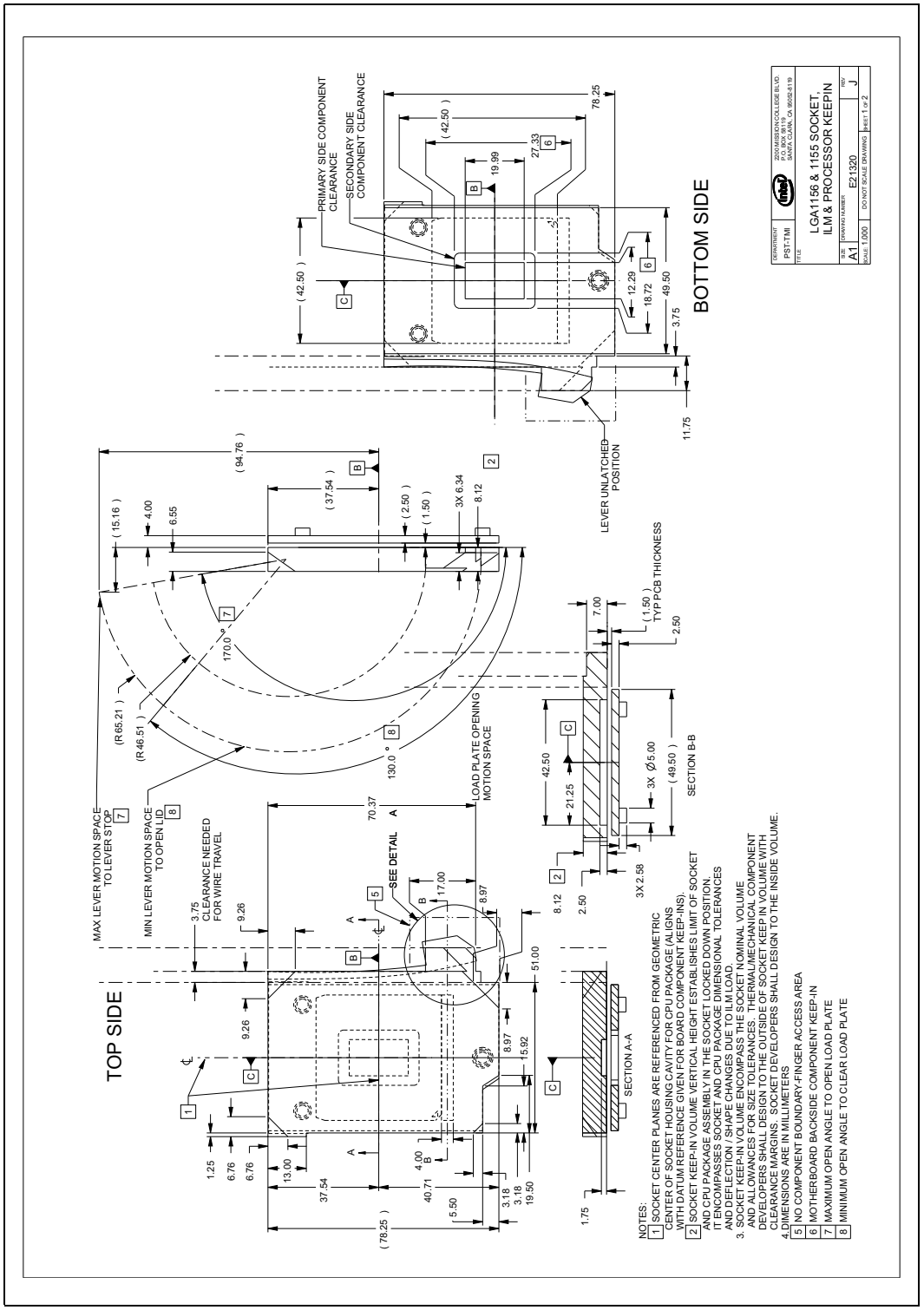


Figure B-4. Socket / Processor / ILM Keepout Zone Secondary Side for 1U (Bottom)

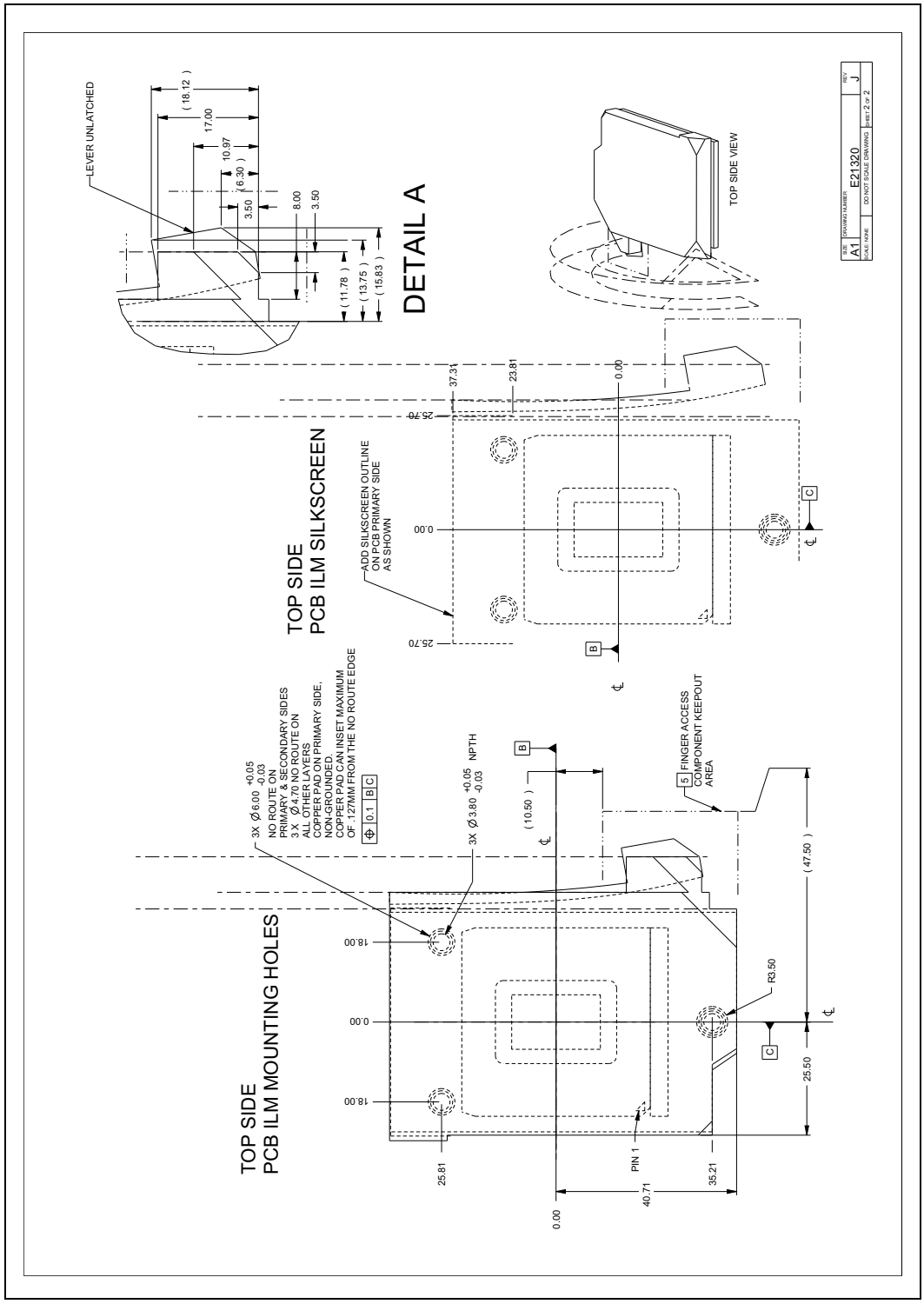


Figure B-5. 1U Collaboration Heatsink Assembly

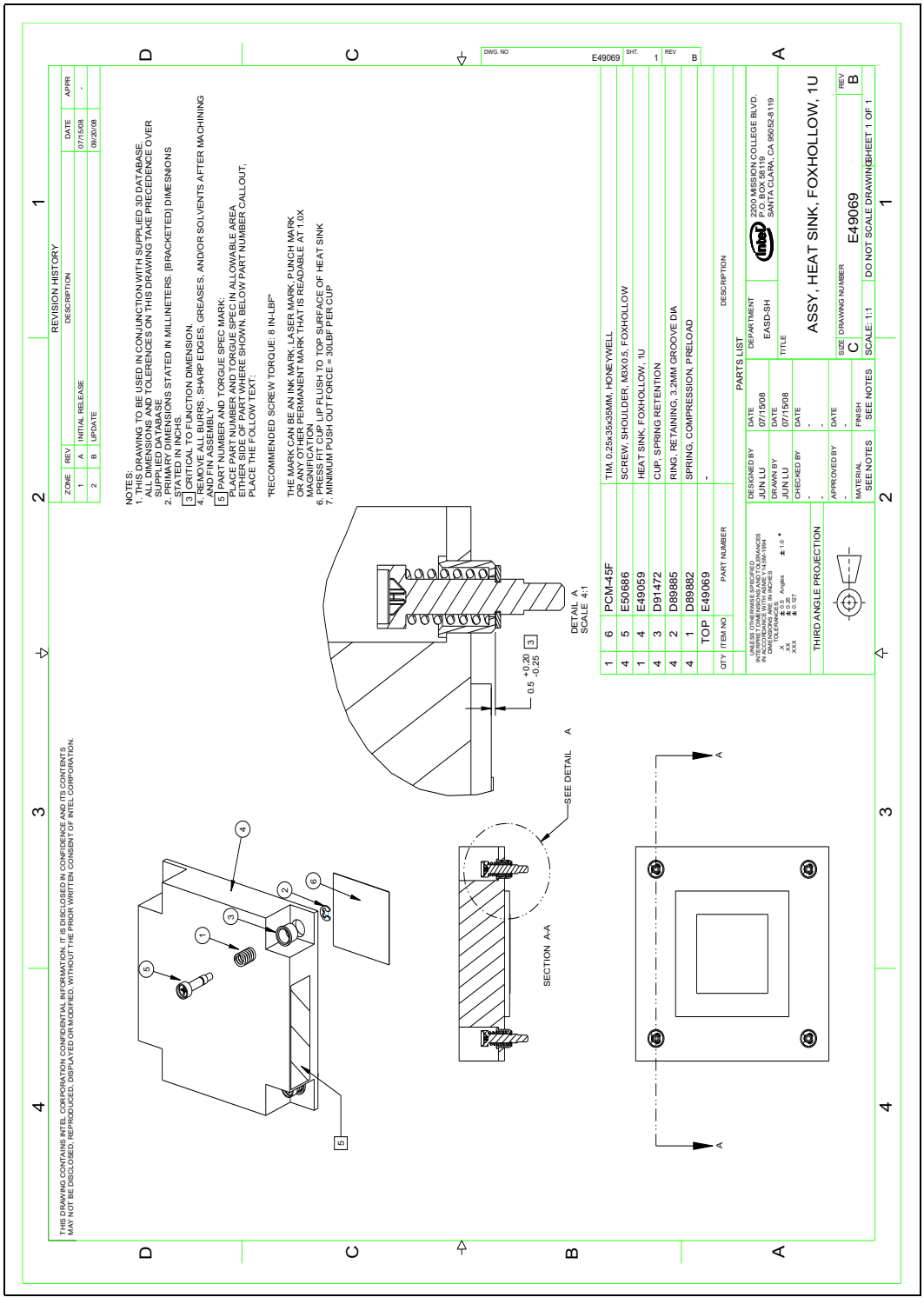


Figure B-6. 1U Collaboration Heatsink

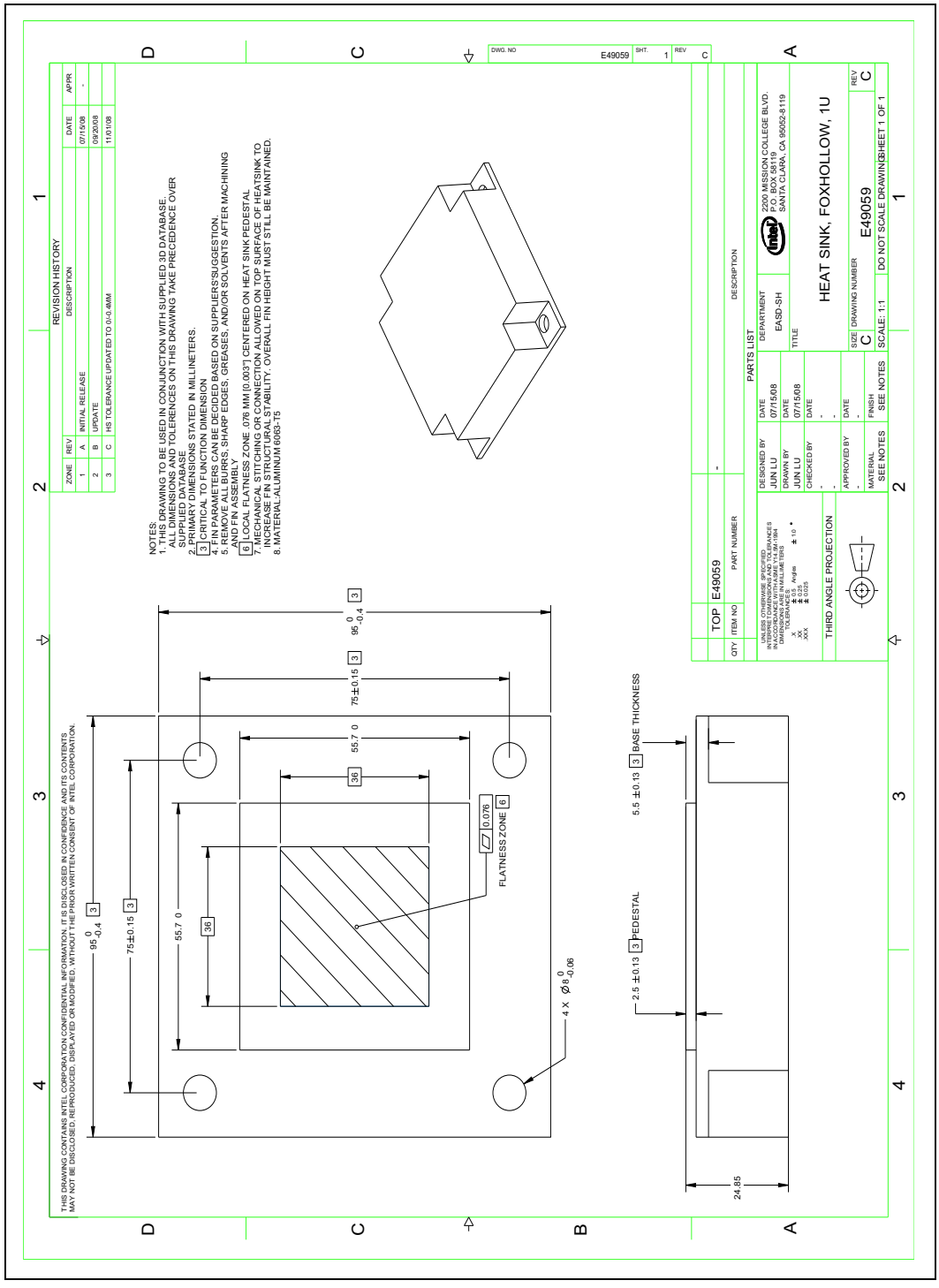


Figure B-7. 1U Reference Heatsink Assembly

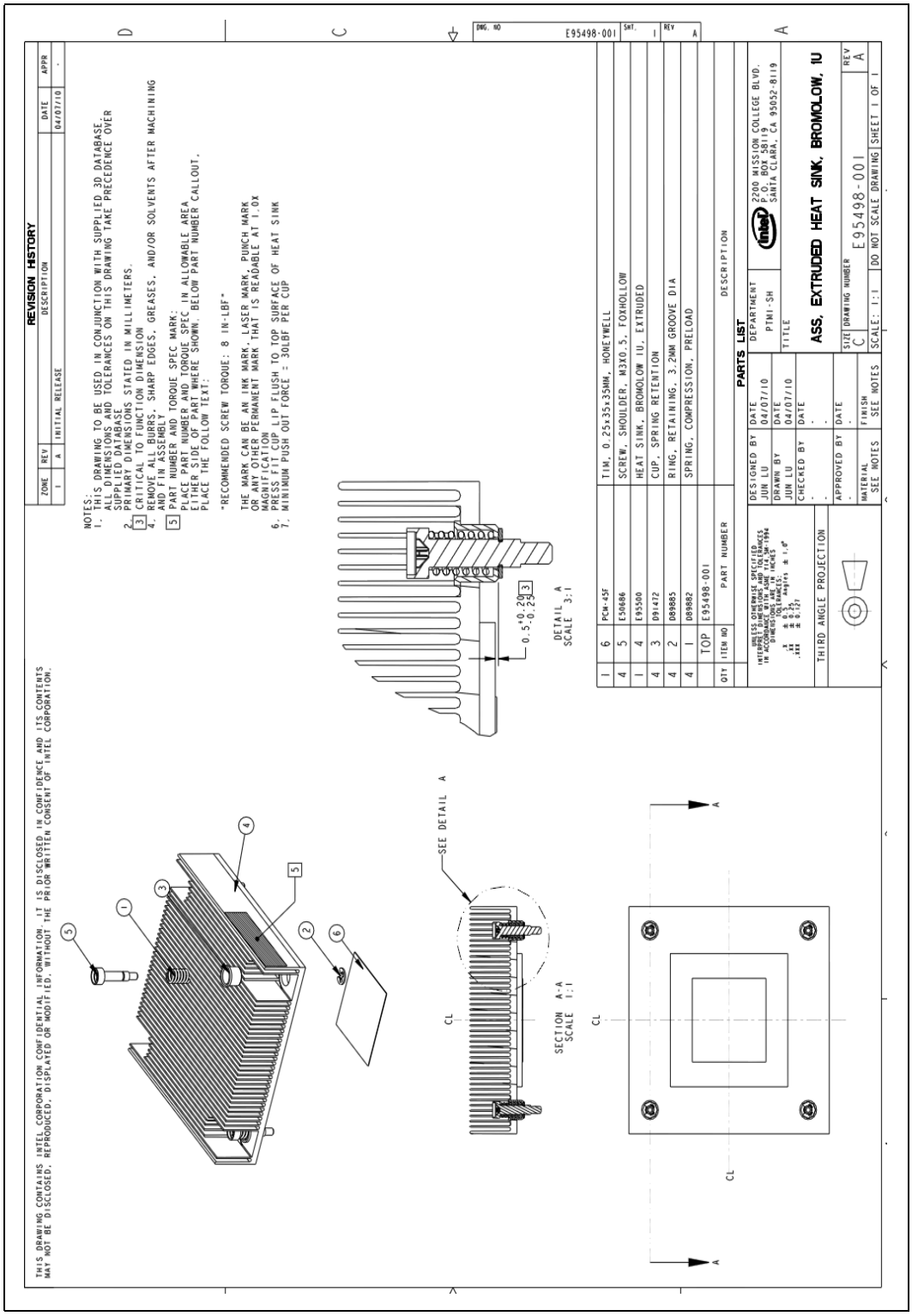


Figure B-8. 1U Reference Heatsink

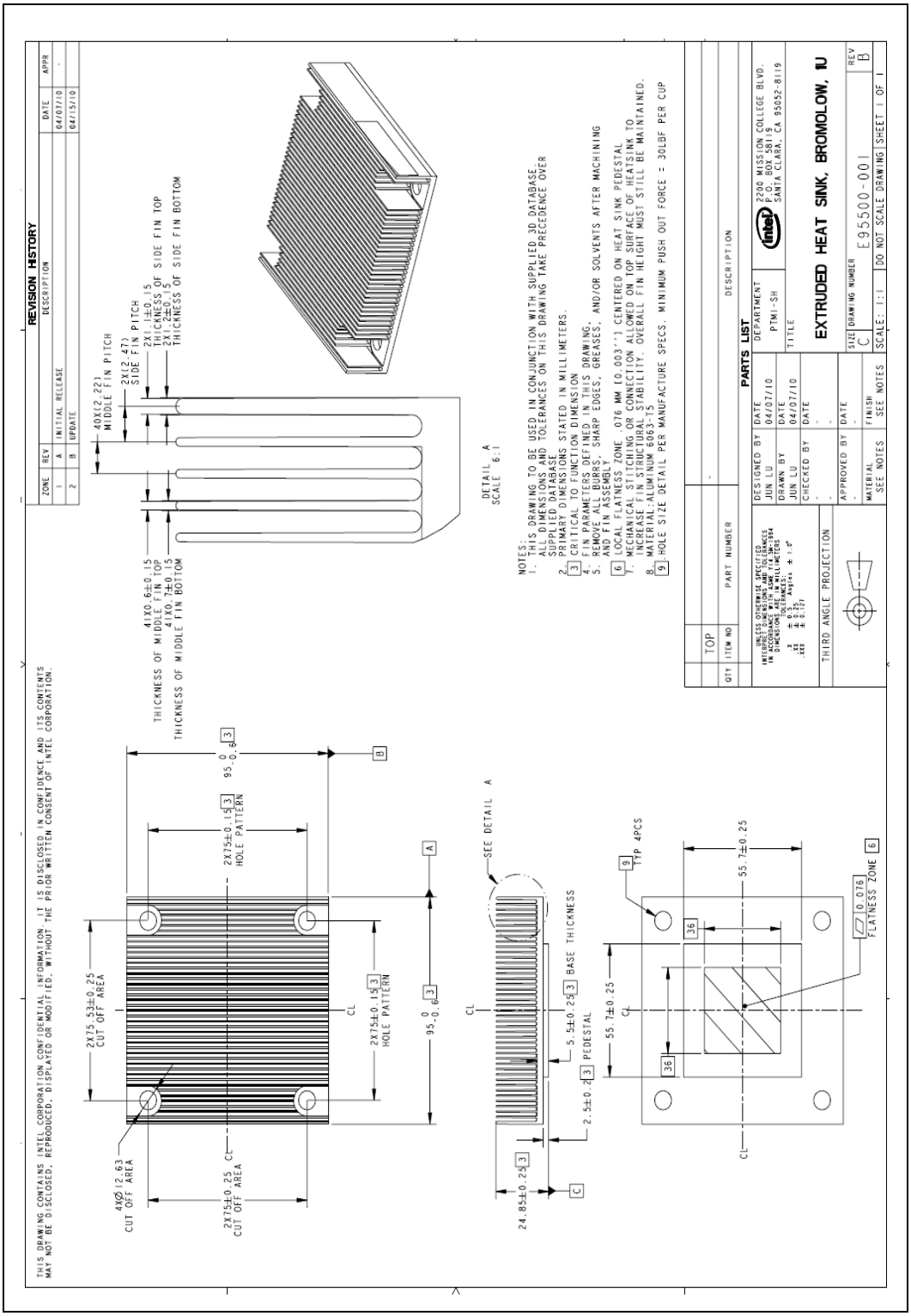


Figure B-9. 1U Heatsink Screw

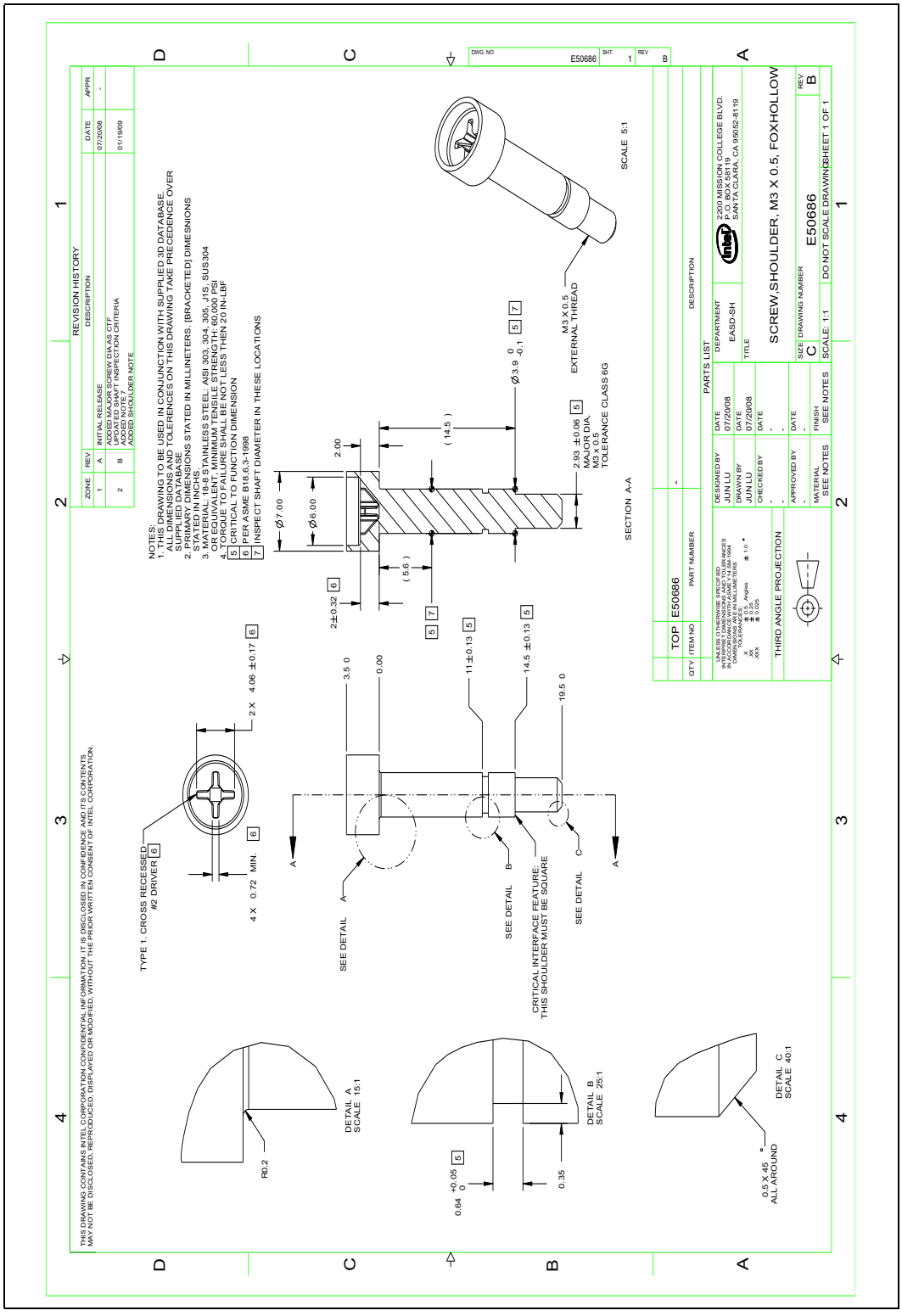


Figure B-10. Heatsink Compression Spring

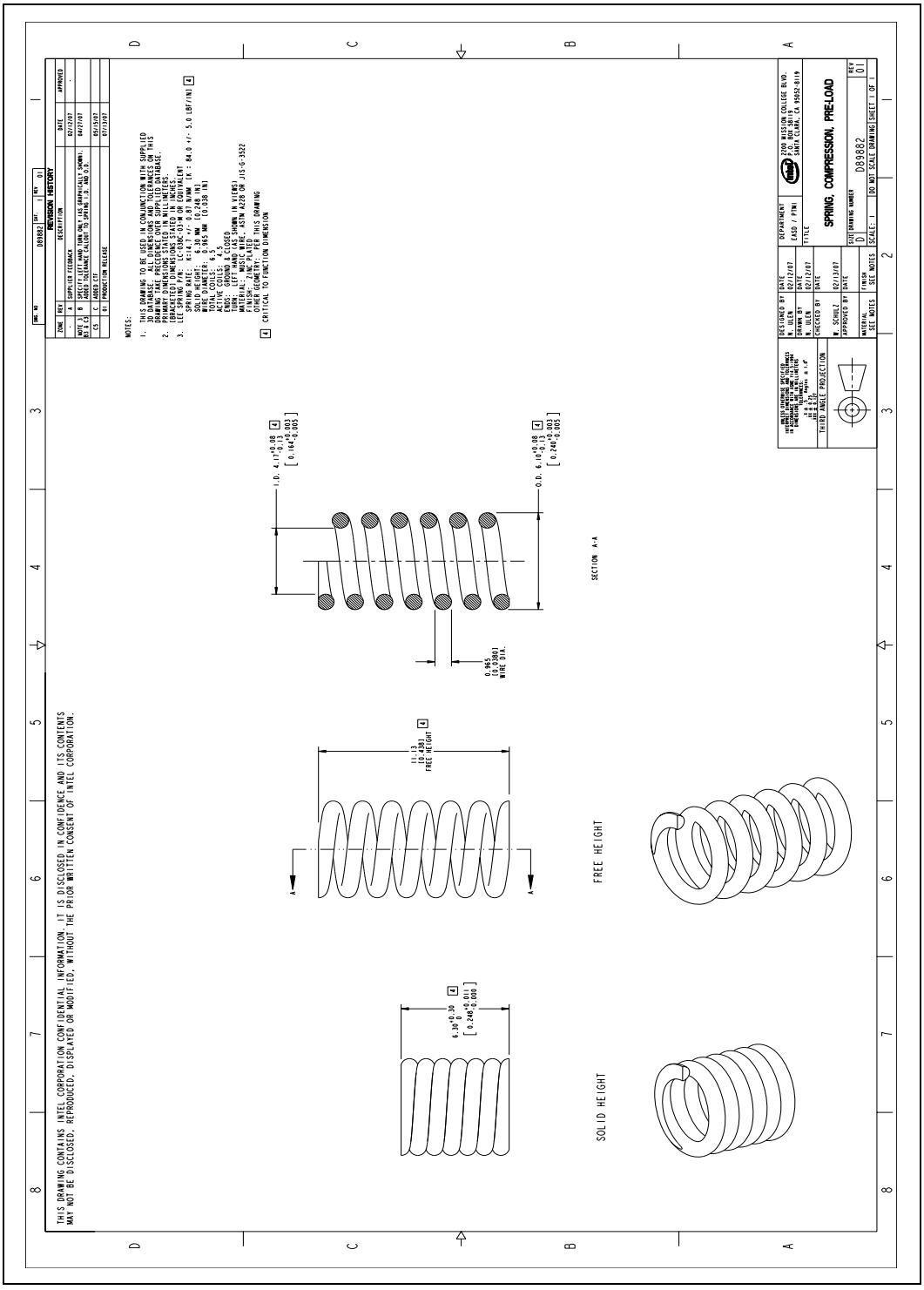


Figure B-11. Heatsink Load Cup

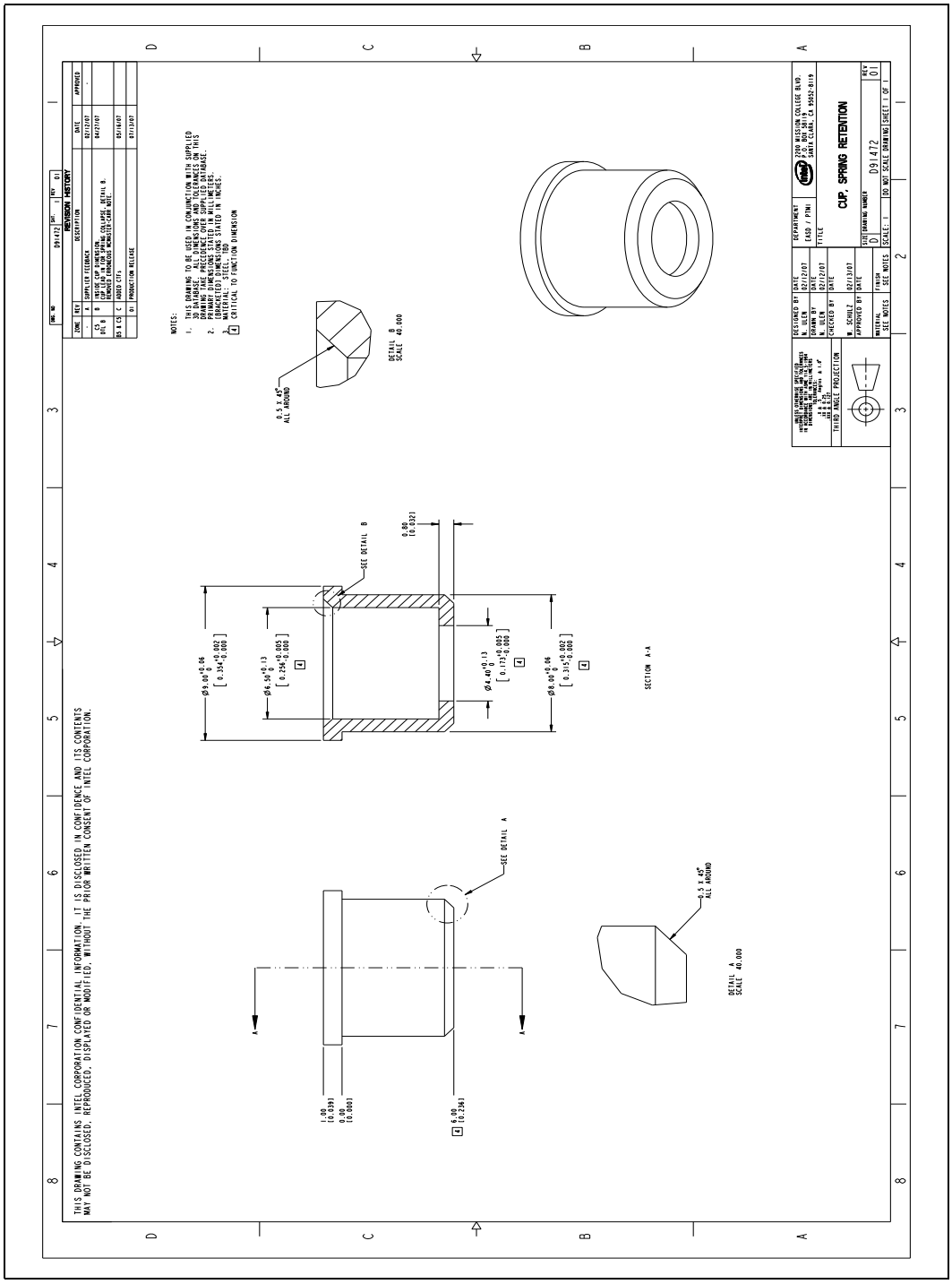


Figure B-12. Heatsink Retaining Ring

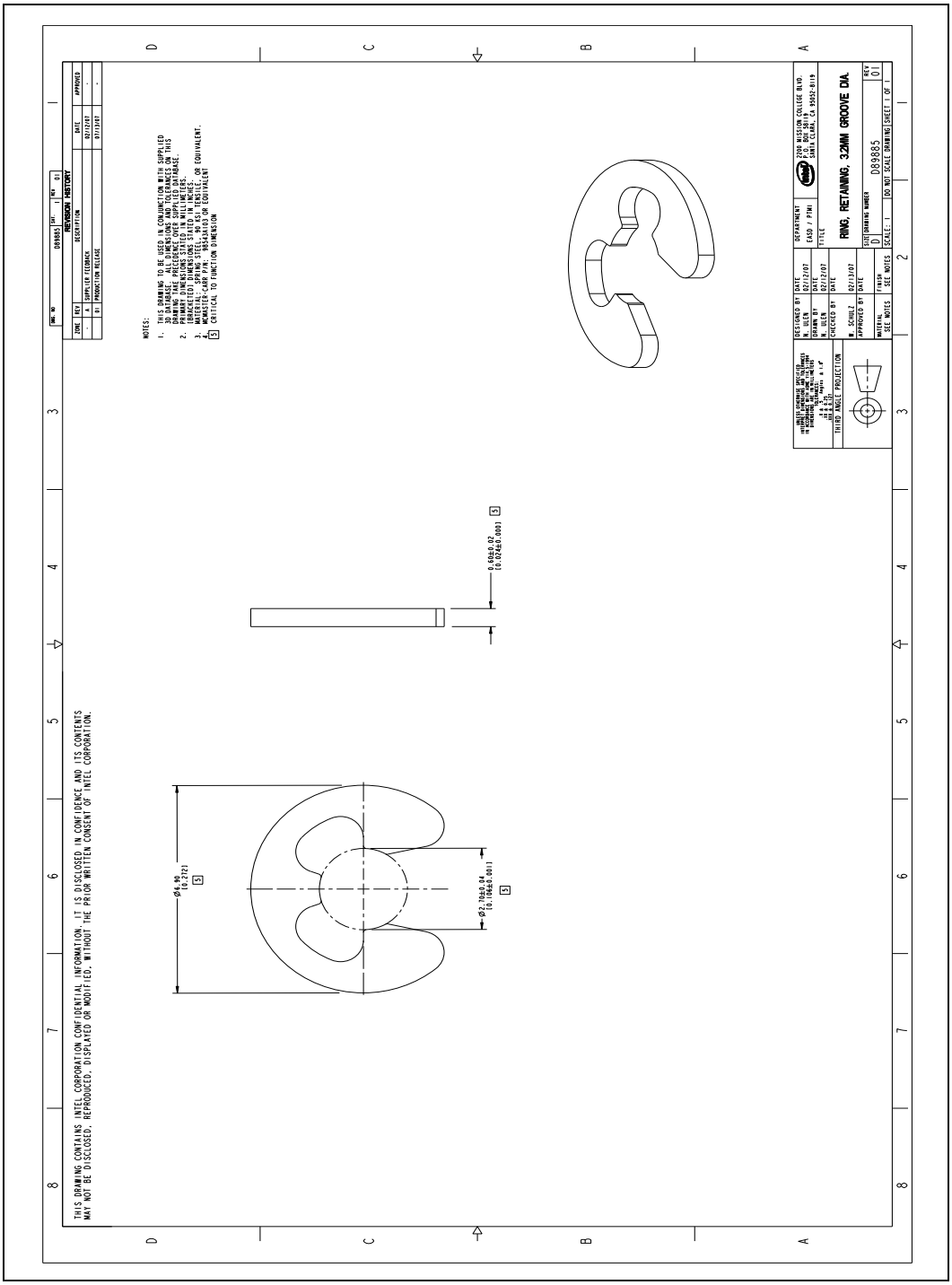


Figure B-13. Heatsink Backplate Assembly

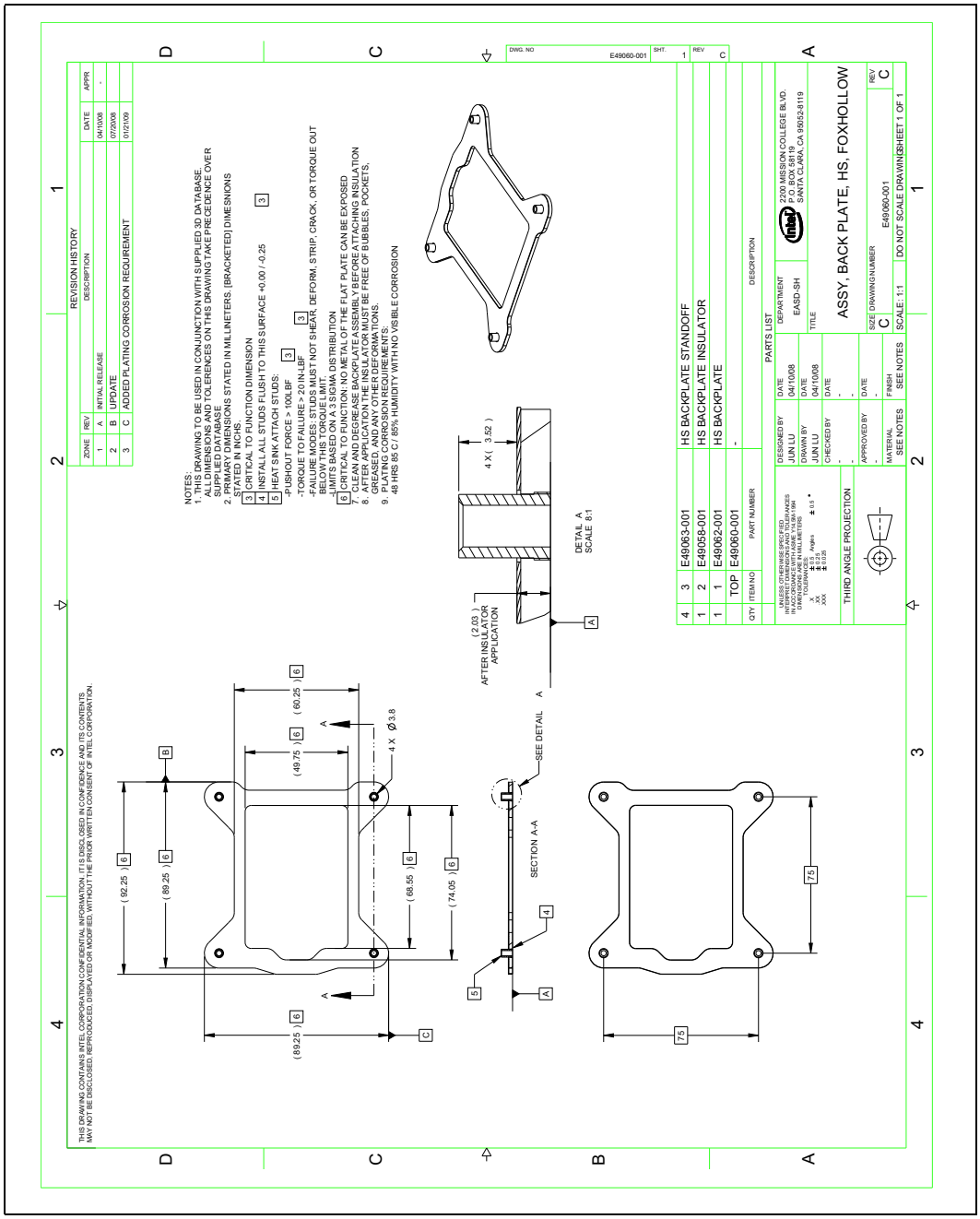


Figure B-14. Heatsink Backplate

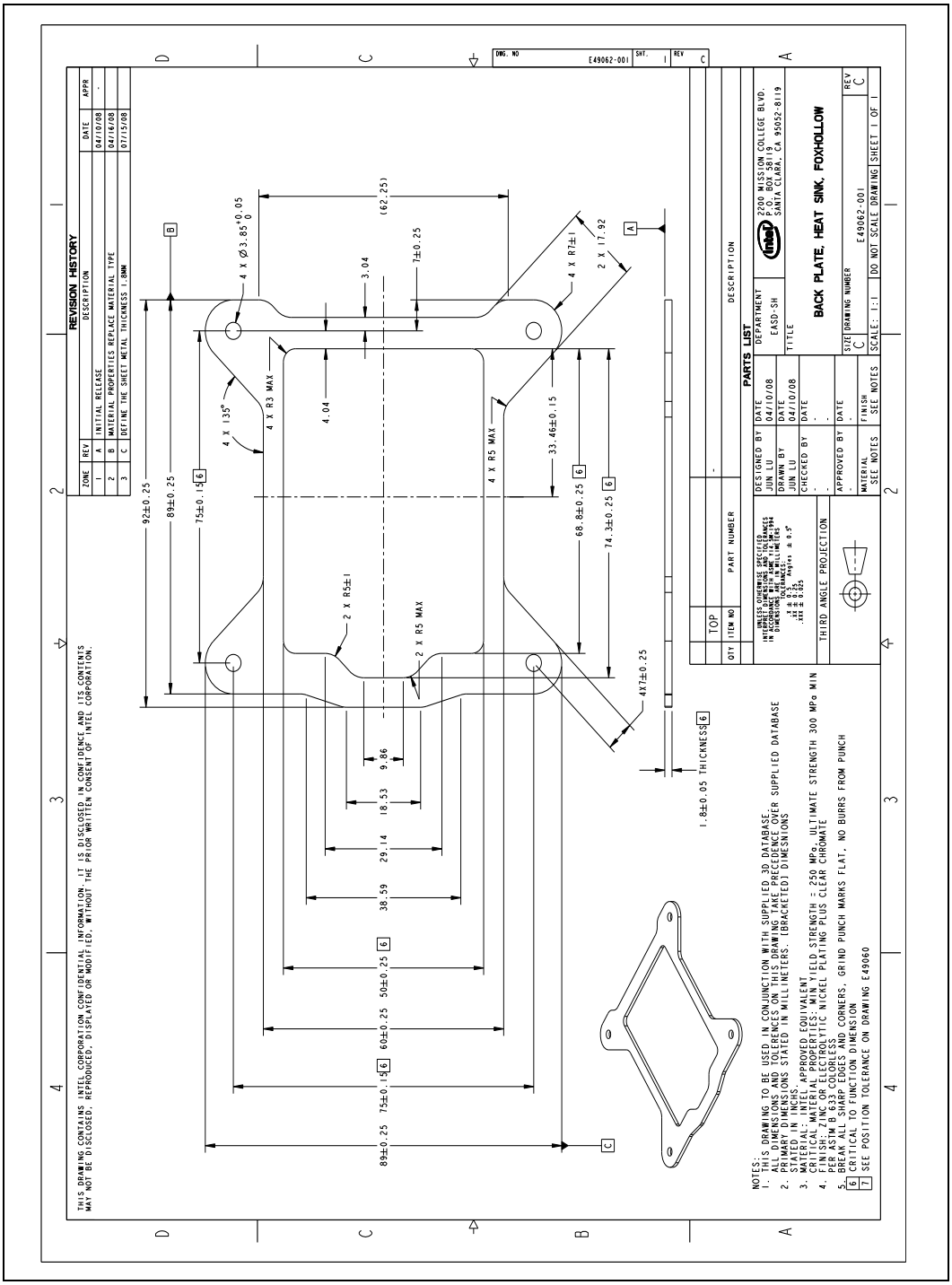


Figure B-15. Heatsink Backplate Insulator

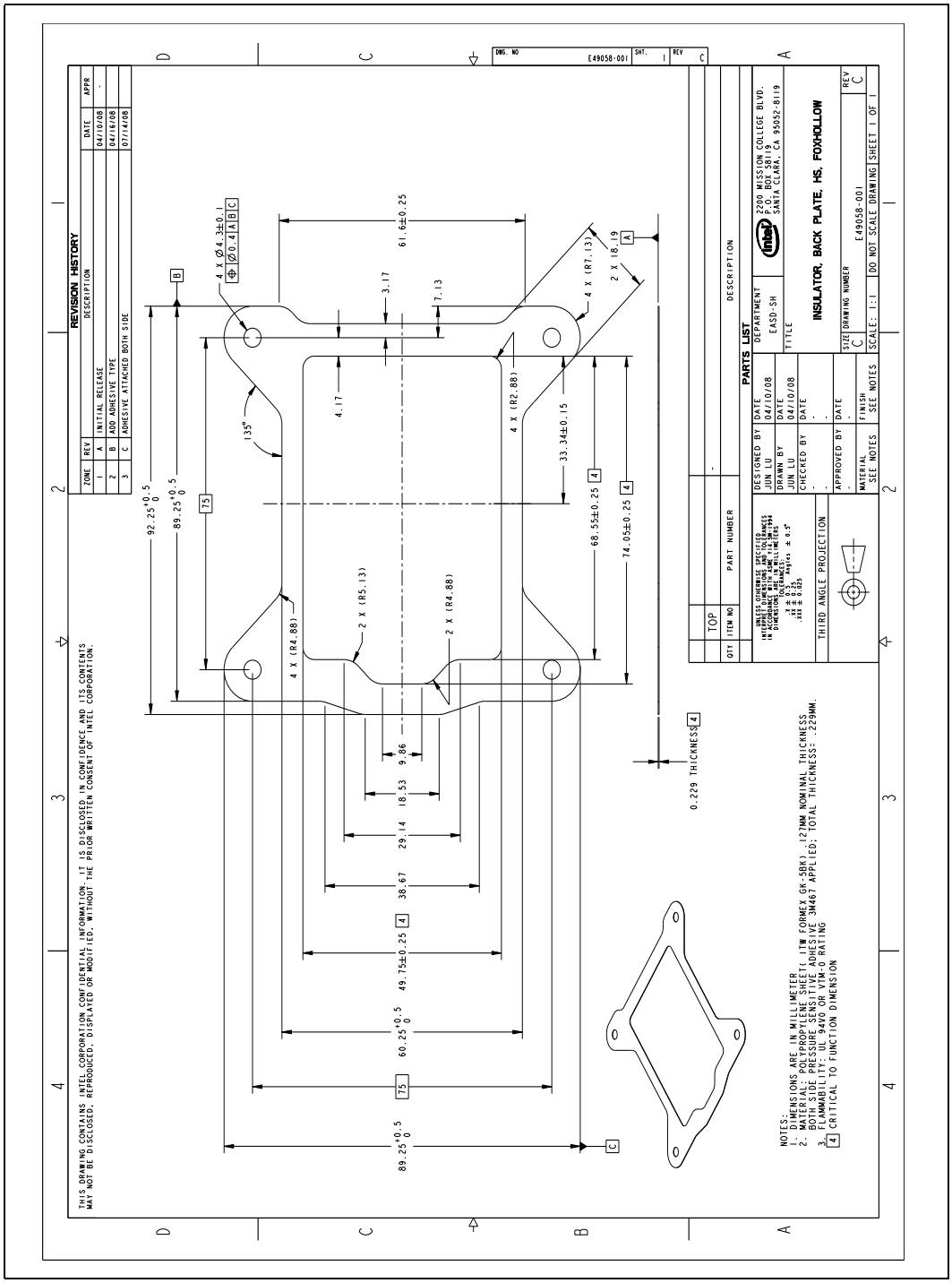


Figure B-16. Heatsink Backplate Stud

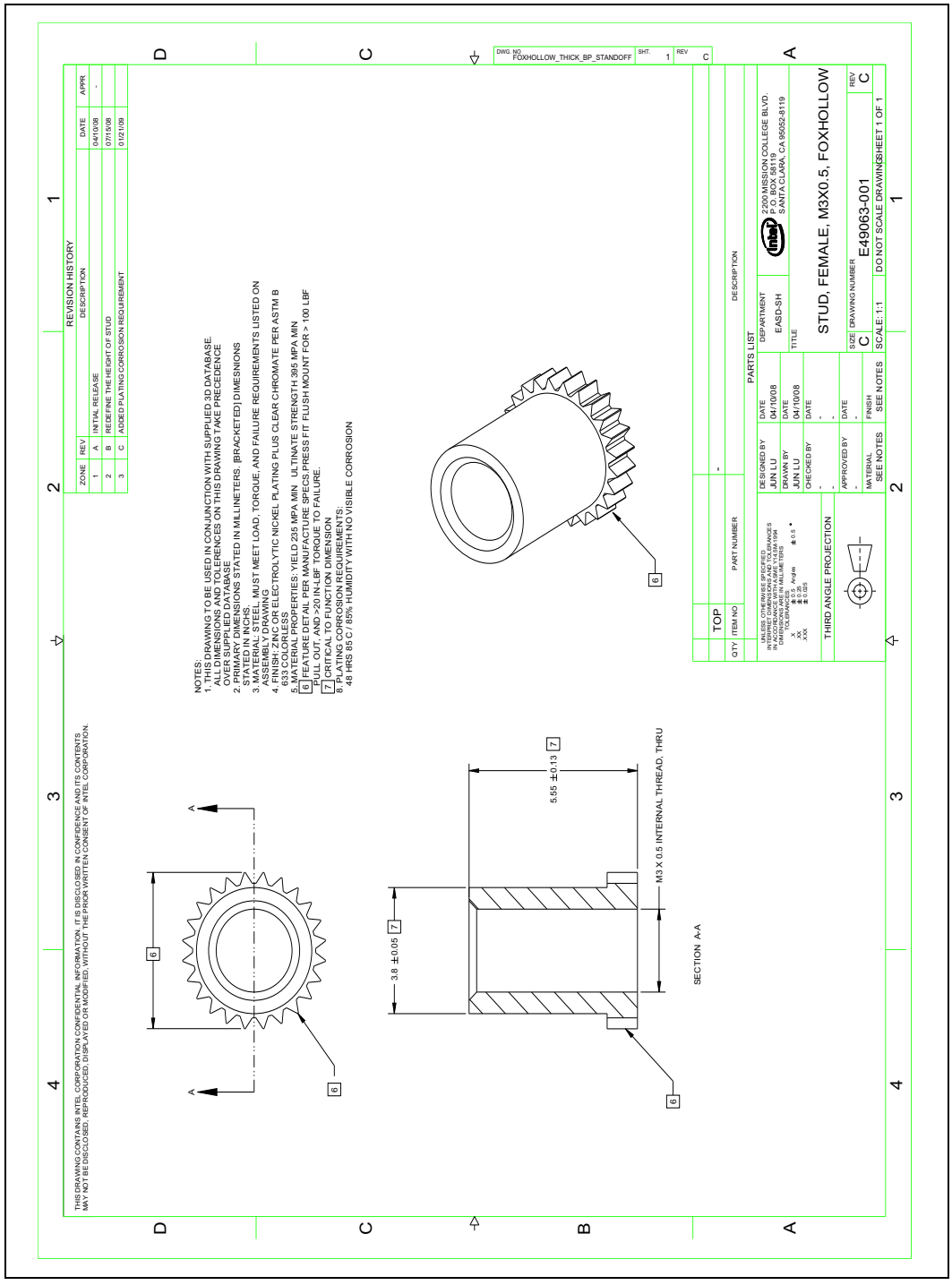


Figure B-17. Thermocouple Attach Drawing

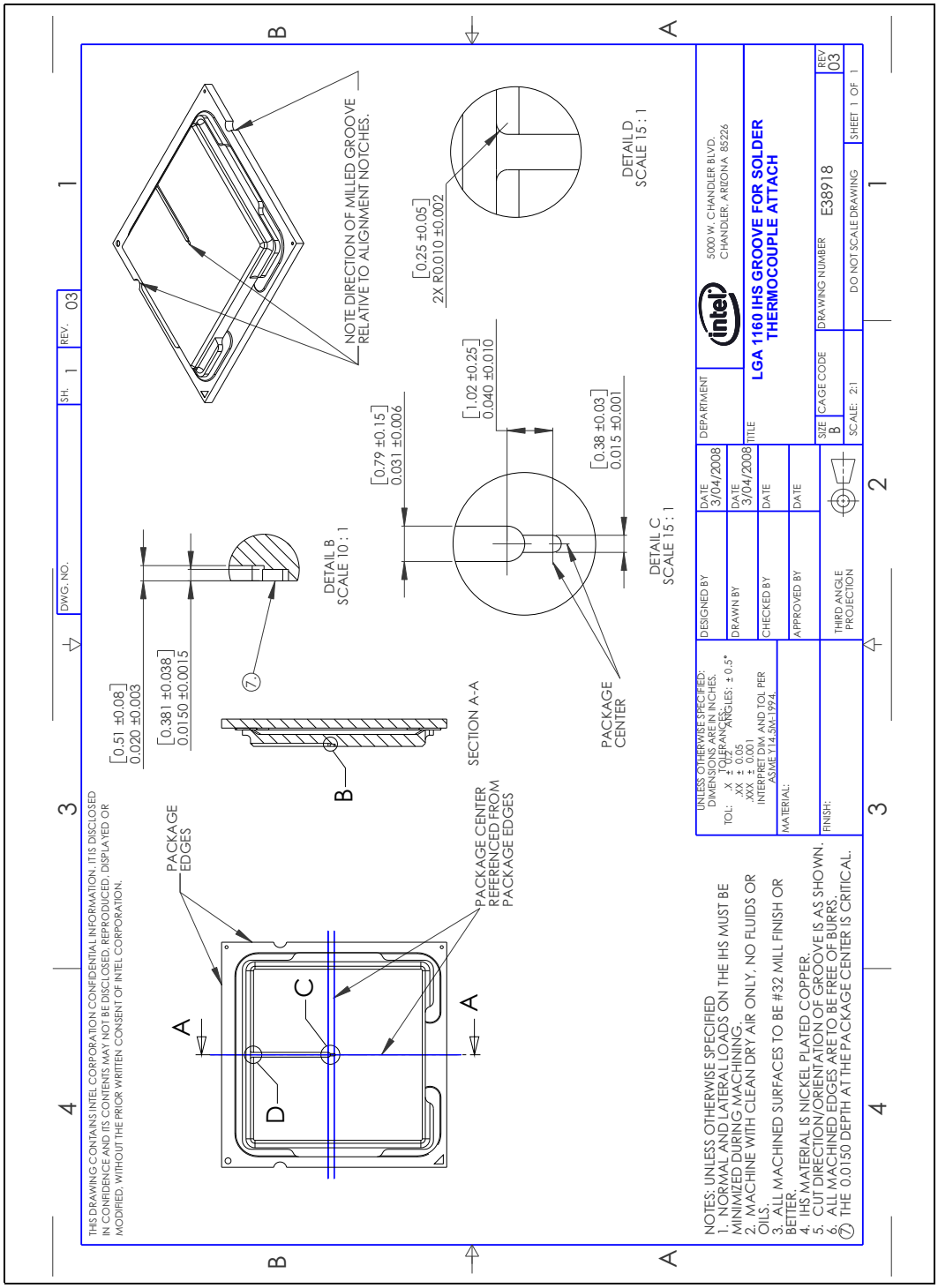


Figure B-18. 1U ILM Shoulder Screw

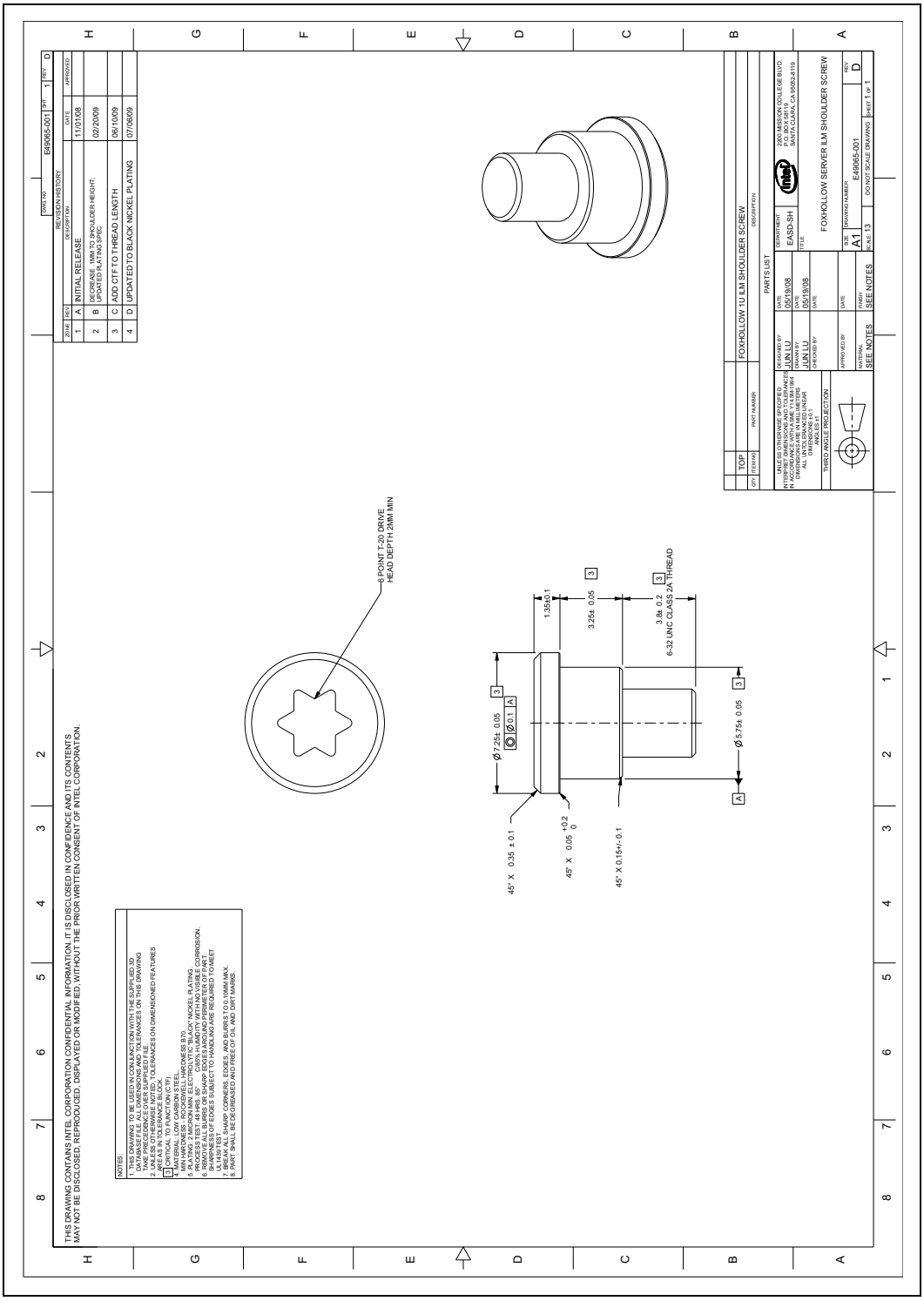
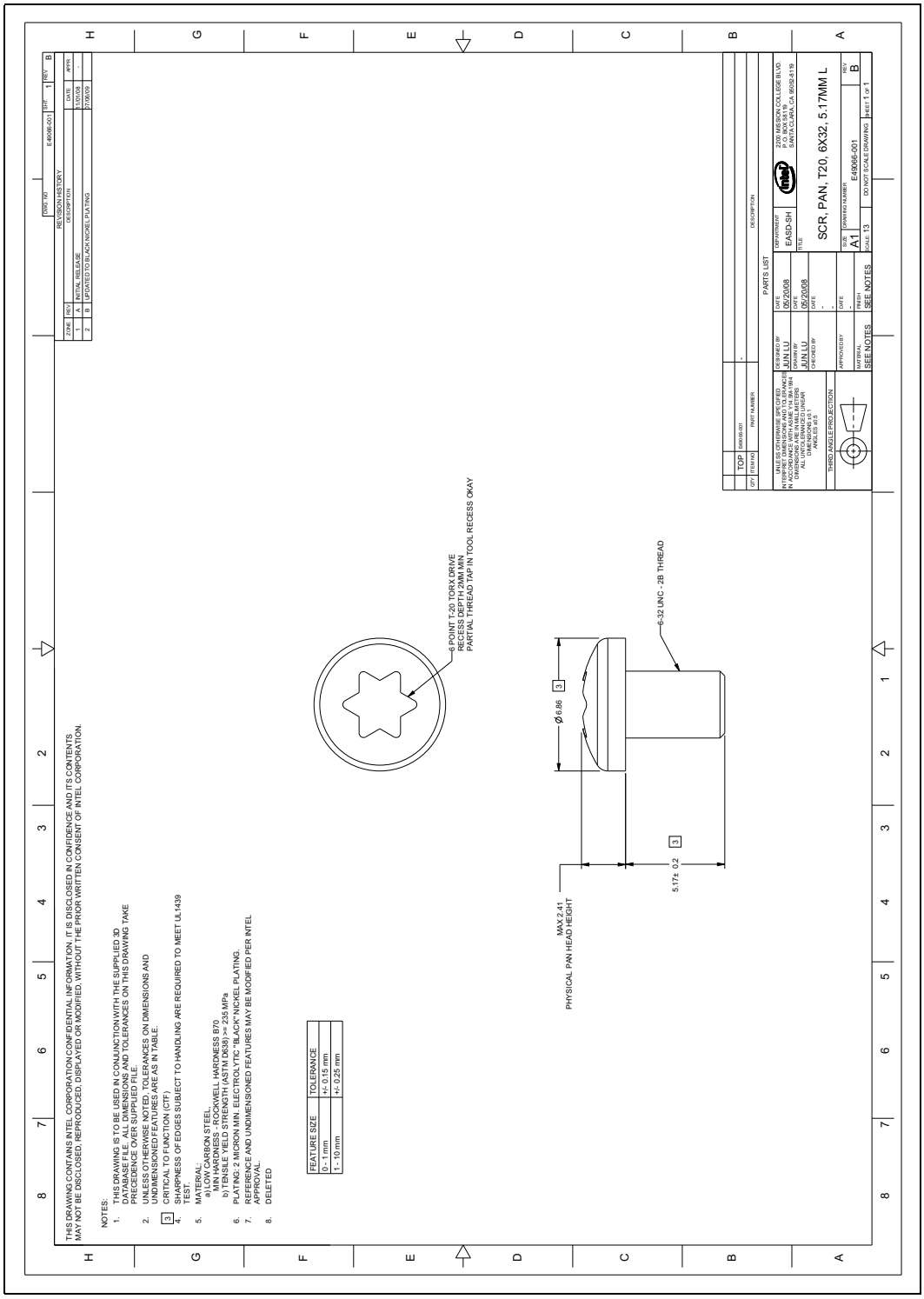


Figure B-19. 1U ILM Standard 6-32 Thread Fastener



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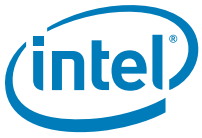


C Socket Mechanical Drawings

Table C-1 lists the mechanical drawings included in this appendix.

Table C-1. Mechanical Drawing List

Drawing Description	Figure Number
"Socket Mechanical Drawing (Sheet 1 of 4)"	Figure C-1
"Socket Mechanical Drawing (Sheet 2 of 4)"	Figure C-2
"Socket Mechanical Drawing (Sheet 3 of 4)"	Figure C-3
"Socket Mechanical Drawing (Sheet 4 of 4)"	Figure C-4

Figure C-1. Socket Mechanical Drawing (Sheet 1 of 4)

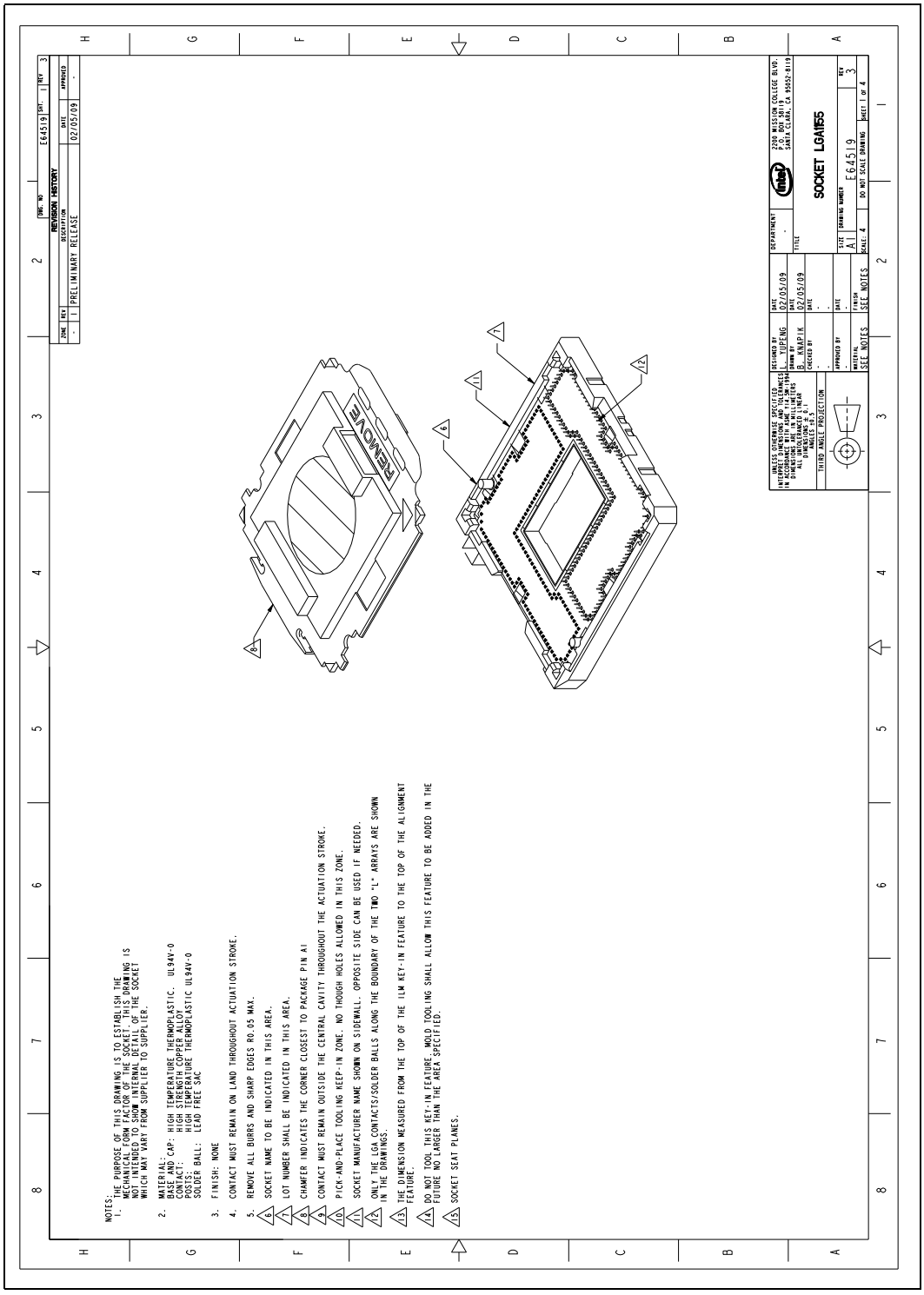


Figure C-2. Socket Mechanical Drawing (Sheet 2 of 4)

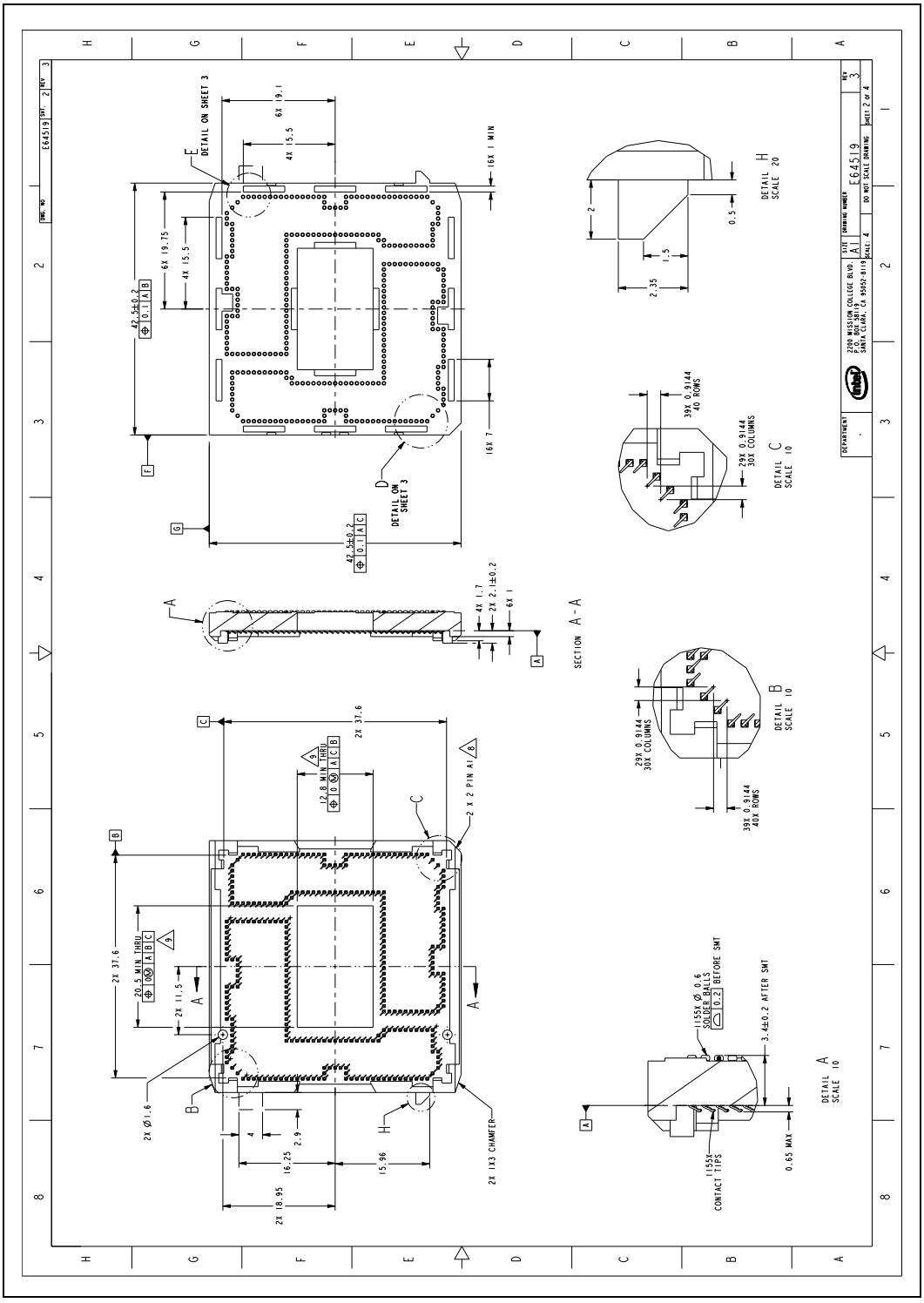


Figure C-3. Socket Mechanical Drawing (Sheet 3 of 4)

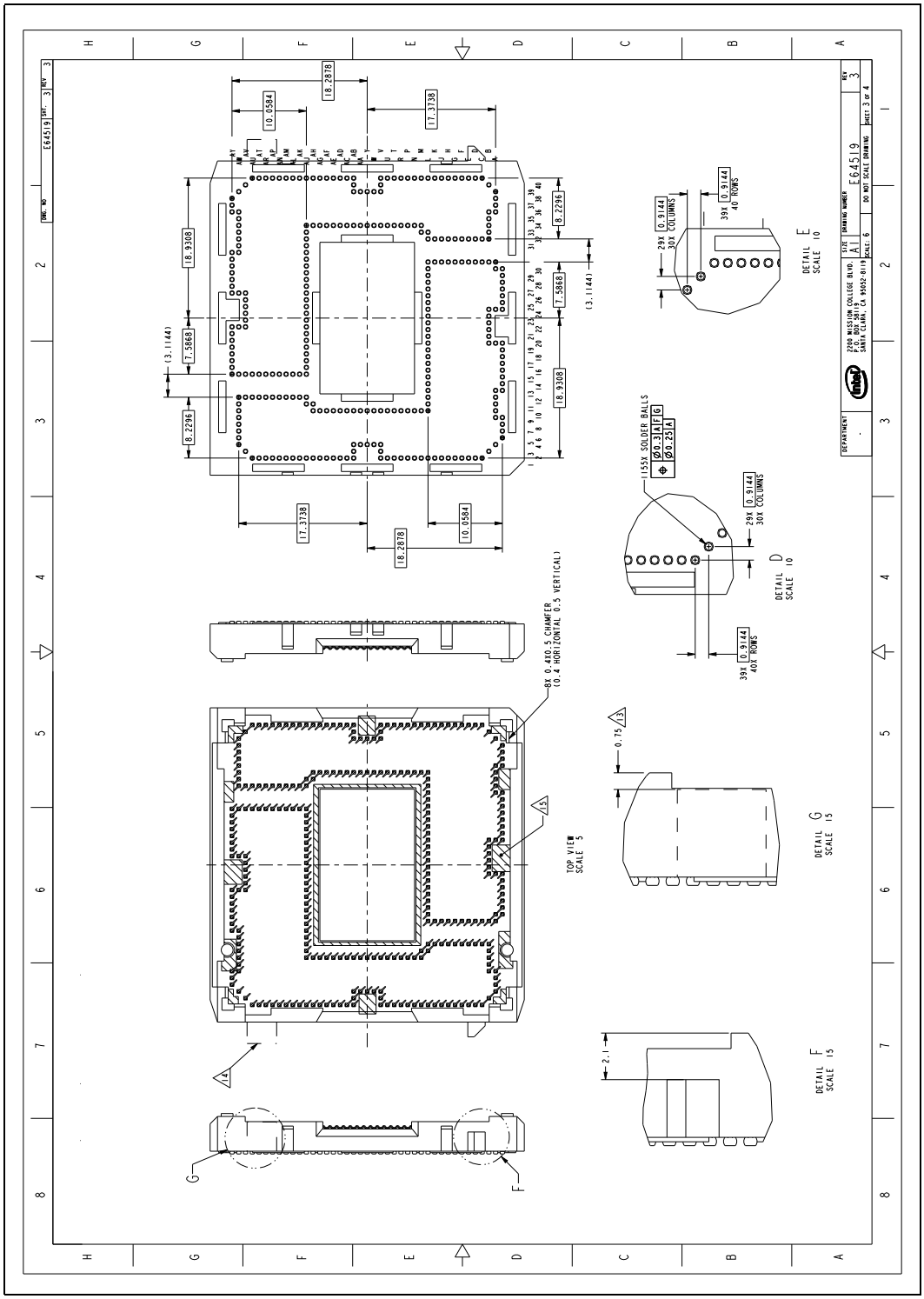
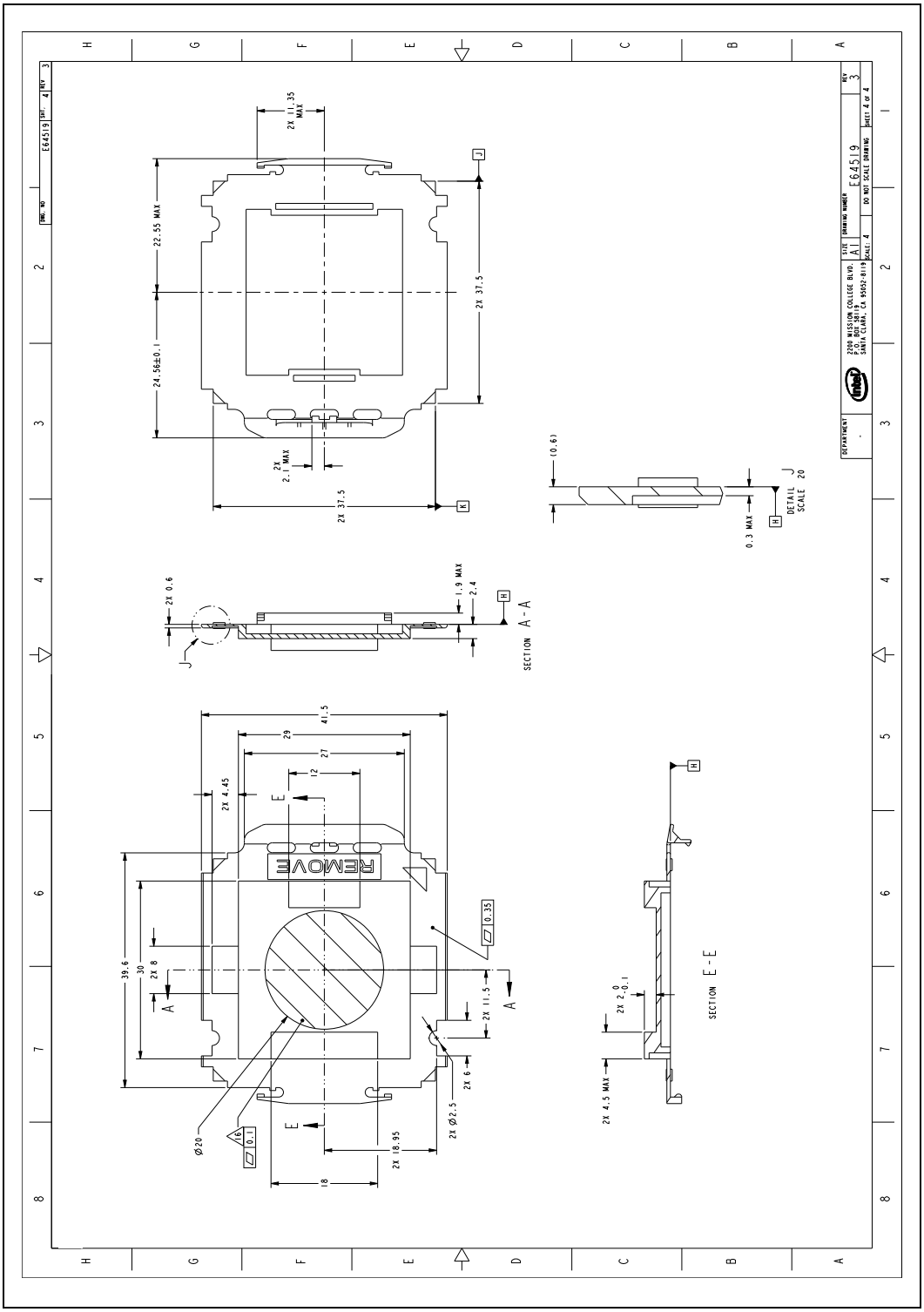


Figure C-4. Socket Mechanical Drawing (Sheet 4 of 4)



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D Package Mechanical Drawings

Table D-1 lists the mechanical drawings included in this appendix.

Table D-1. Mechanical Drawing List

Drawing Description	Figure Number
"Processor Package Drawing (Sheet 1 of 2)"	Figure D-1
"Processor Package Drawing (Sheet 2of 2)"	Figure D-2

Figure D-1. Processor Package Drawing (Sheet 1 of 2)

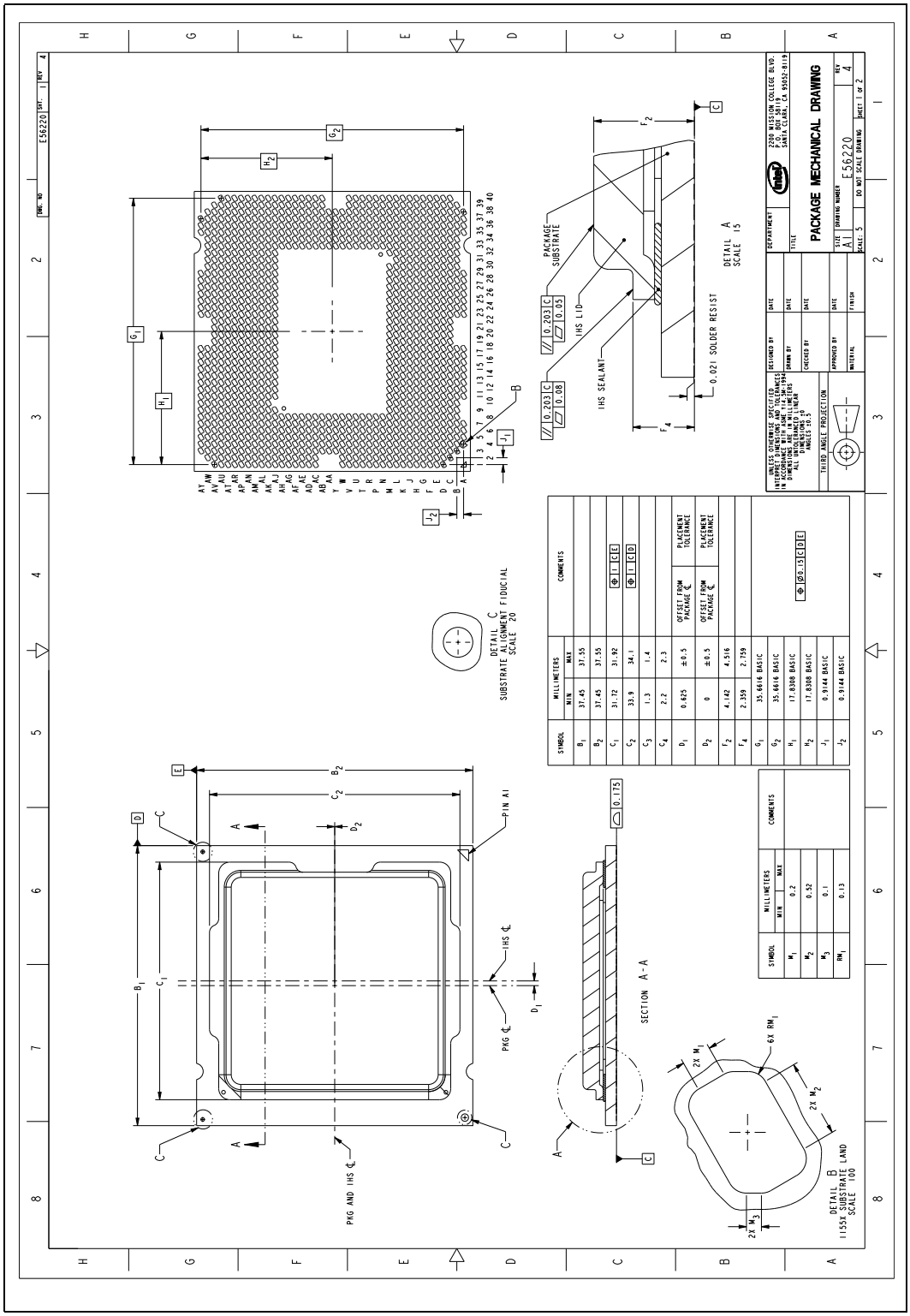
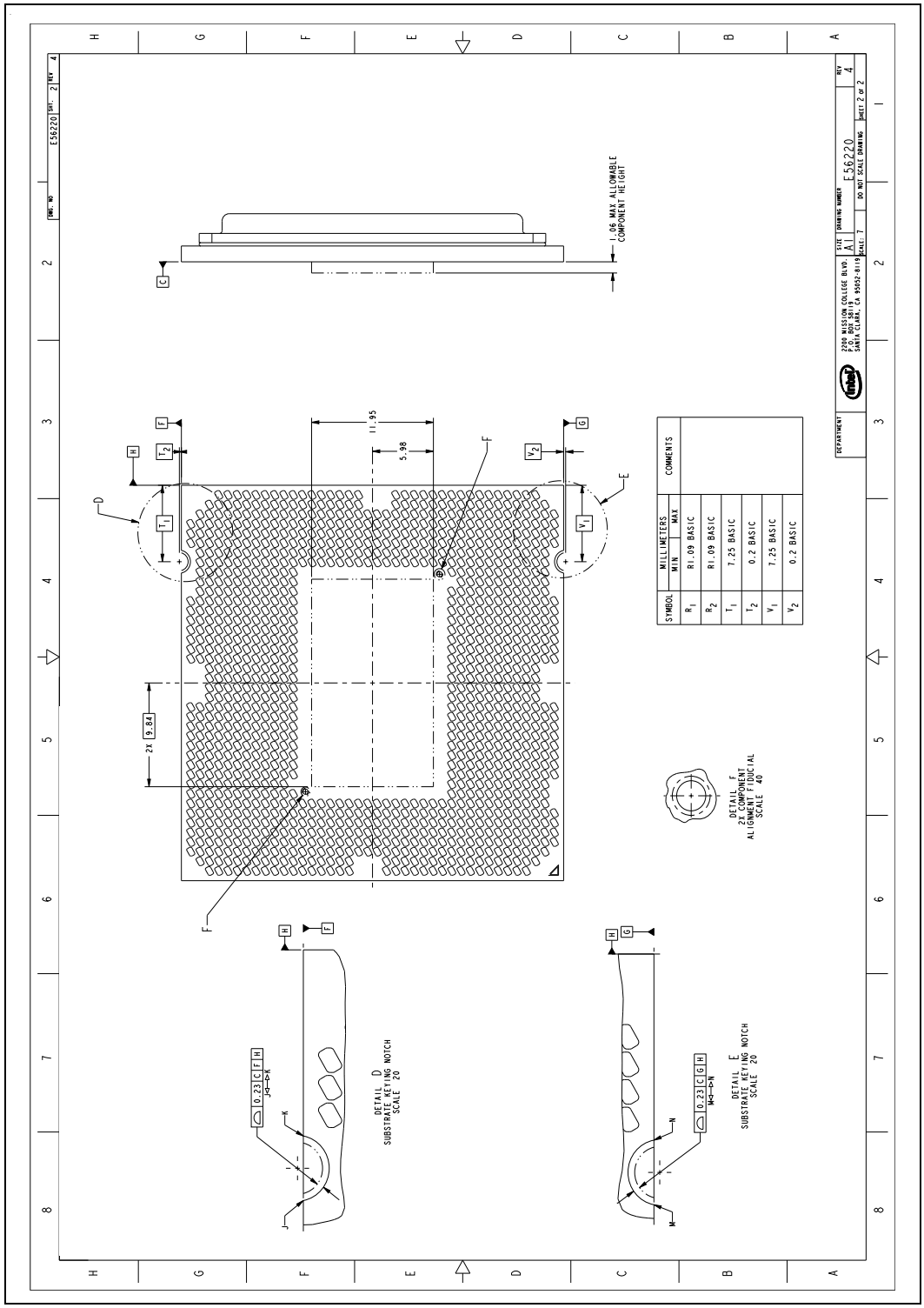


Figure D-2. Processor Package Drawing (Sheet 2of 2)



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