ABSTRACT

This document is hardware manual for LEO2-B Platform board. Contents of this document are descriptions of each blocks and usage directions. It is recommended to peruse this manual before operating LEO2-B Platform

HISTORY

Rev	Status	Date	Author	Contents

KEY WORDS

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1. Introduction

1.1 Scope

This document intends to describe the brief architecture and usage of the LEO2-B Platform board. LEO2-B Platform board is designed for LTE User Equipment test and verification.

1.2 Terminology

ADC	Analog to Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
AHB	Advanced High-performance Bus
DAC	Digital to Analog Converter
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
EPI	External Perallel Interface
ETM	Embedded Trace Macro-cell
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
UE	User Equipment
UART	Universal Asynchronous Receiver/Transmitter
SDIO	Secure Digital Input Output
USB	Universal Serial Bus
VGA	Variable Gain Amplifier
ZDB	Zero Delay BufferAMBA

1.3 Trademark List

ARM926EJ-S are registered trademarks of ARM Ltd.

1.4 Special Mark

The following table defines special marks used in this manual.

Mark Definition

2. Features and top level diagram

2.1 Features

- ARM926EJ-S (max 333MHz)
- AMBA 2.0 (max 166MHz)
- 7 Virtex4 FX140 FPGA for Modem algorithm
- RF interface (2 Receivers and 1 Transmitter)
- Application interface
- 512Mb DDR SDRAM, 1Gb NAND Flash
- USB 2.0 High speed device
- 100 Ethernet port
- 1 Serial ports (up to 115 K baud)
- JTAG and ETM Debug port

2.2 Photograph of the LEO2-B platform board

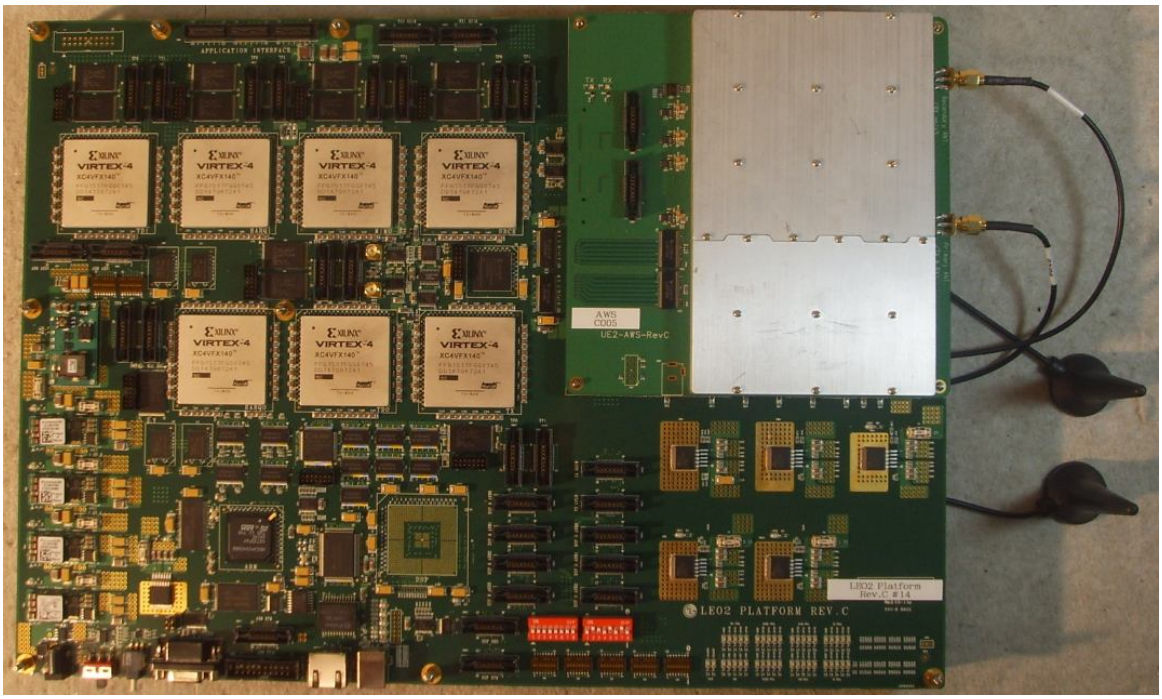

Figure 1. Photograph of LEO2-B platform

- Mechanical size of platform board is 420 (W) x 300 (H) mm

2.3 Top level block diagram

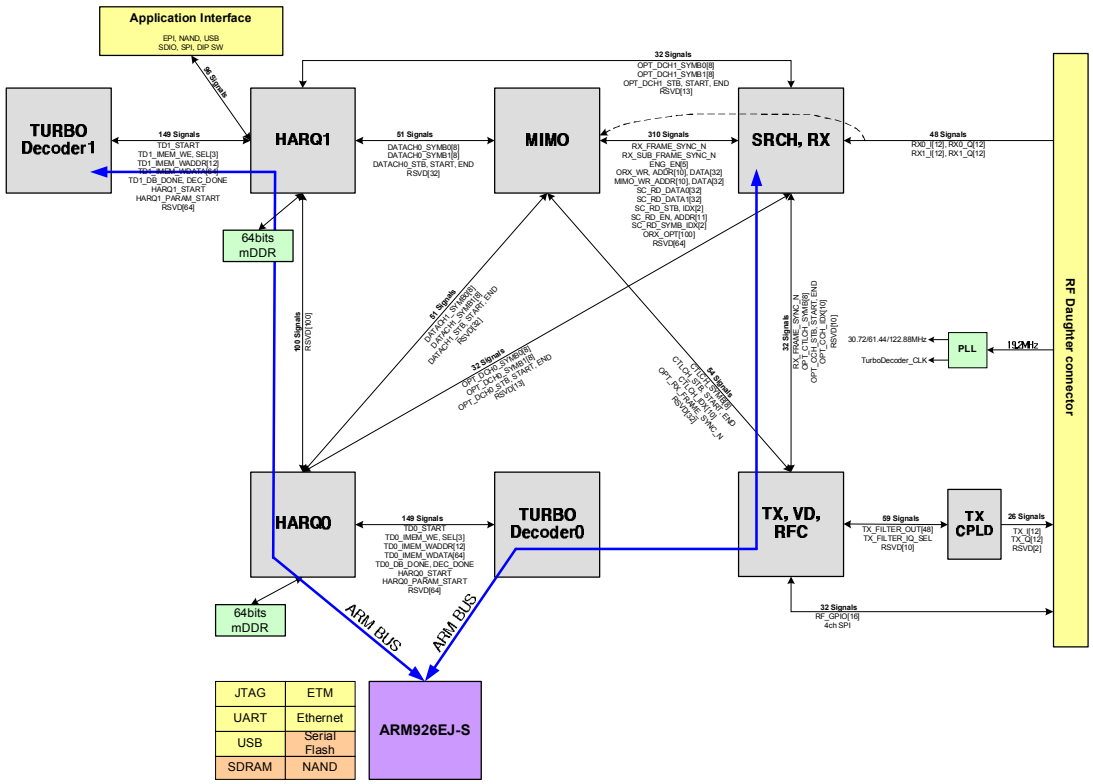

Figure 2. Top level block diagram

2.4 Placement map

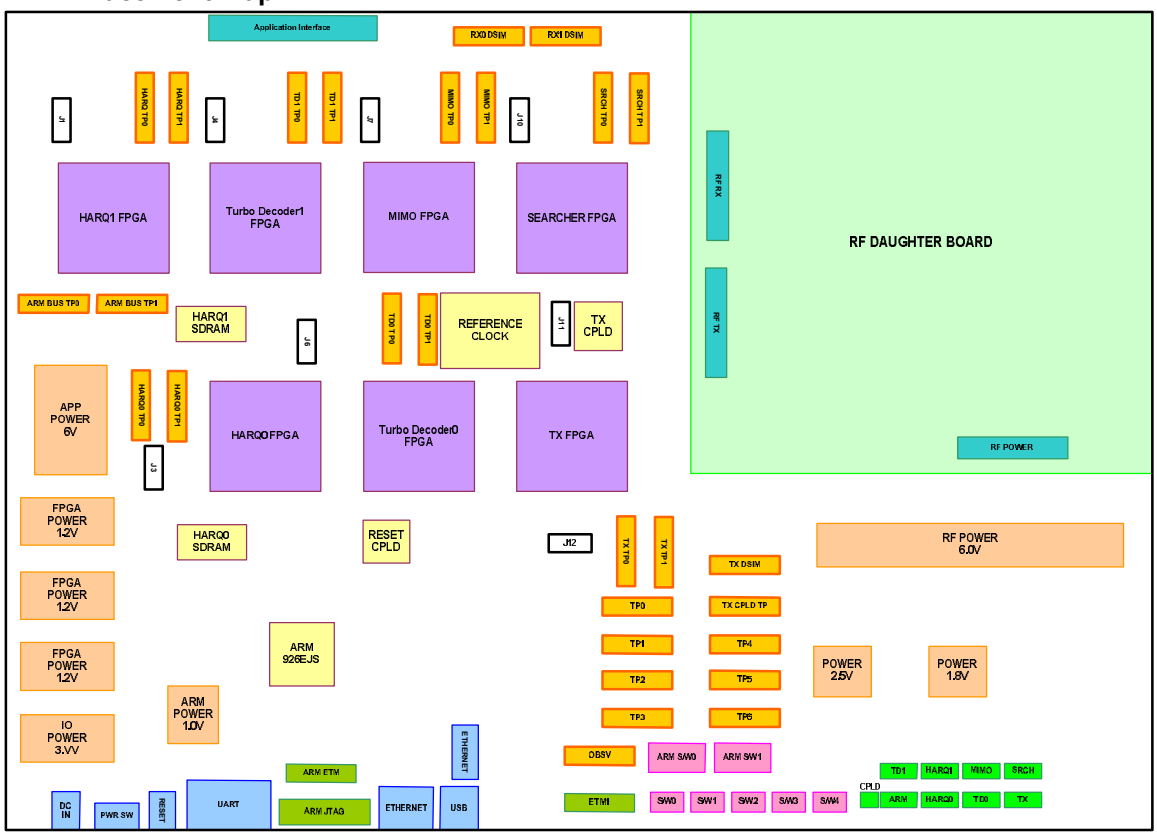

Figure 3. Placement map of the LEO2-B

3. Block description

3.1 FPGA subsystem

The LEO2-B Platform supports 7 FPGAs (xilinx virtex4 FX140, 1517pin package) for LTE UE modem algorithm. Functionality of each FPGA is

- TX FPGA : Transmit block, Viterbi decoder, RF board control
- SRCH FPGA : Receiver block
- MISO FPGA : Receiver block and MISO
- HARQ 0/1 FPGA : Hybrid ARQ block
- Turbo Decoder 0/1 FPGA : Decoder block

Signal connection of FPGAs is

- ARM926 bus signal is connected to commonly all FPGAs, except MISO FPGA.
- 32 common reserved signals are connected commonly.
- 64 test signals of each FPGA are connected to MICTOR probing header.
- 4 GPIO LEDs of each FPGAs
- Detailed signals are described on block diagram.

FPGA configure bitstream is stored in platform flash. The maximum configuration bitstream size of virtex4 FX140 is 47,856,896. Bitstream is stored in 2 serial daisy chained memories; capacity is 32Mb and 16Mb. Proper binary image should be fused on each platform memories. Xilinx Platform cable connection for image fusing are J12 (TX FPGA), J10 (SRCH FPGA), J7 (MISO FPGA), J3 (HARQ0 FPGA), J4 (HARQ1 FPGA), J6 (Turbo Decoder 0 FPGA) and J1 (Turbo Decoder1 FPGA), which are placed beside of each FPGAs.

3.2 ARM subsystem

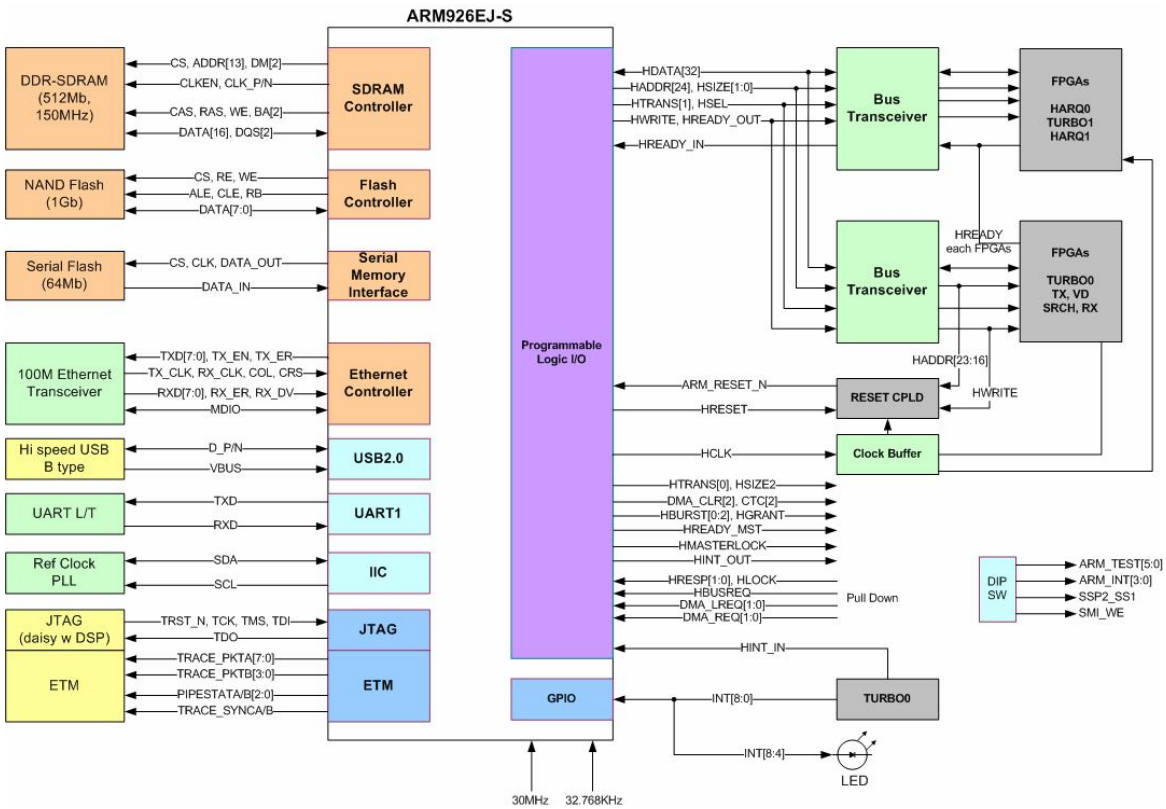

Figure 4. ARM processor block

The ARM processor is used to control the LTE UE modem logic. The processor has ARM926EJ-S core and peripheral controllers.

ARM Processor

- ARM926EJ-S core max. 333MHz, 16KB-I/D cache, configurable TMC-I/D size, MMU, TLB, JTAG and ETM trace module (multiplexed interfaces).
- 32KByte Rom (code customizable) 8KByte common SRAM.
- High performance linked list 8 channels DMA.
- Ethernet MII, management interface
- USB2.0 High speed device
- Ext. memory interface : 16bit DDR1@200MHz
- Flash interface: 8bits NAND and Serial.
- 10 independent Timers with programmable prescaler.
- RTC - WDOG - SYSCTR - MISC internal control registers.
- JTAG (IEEE1149.1) interface.
- Current clock frequency setting : ARM Core 300MHz, Bus 150MHz, SDRAM 150MHz

Memory

The memory capacity and speed grade, that is on this board, are

- SDRAM : 512Mbits, 16bits data access, DDR @ 150MHz
- NAND Flash : 1Gbits, 8bits parallel, code stored.
- Serial Flash : 64Mbits, boot loader stored.

External Interface

The LEO2-B Platform supports external interface for diagnostic monitoring and user data transfer.

- High speed USB2.0
- 100Mbps Ethernet

Interrupt

9 interrupt inputs are from interrupt handler in Turbo decoder0 FPGA.

3.3 Debugger Interface

The LEO2-B platform support debugging interface, JTAG and ETM, for ARM926

ARM926 core

- JTAG : CON12
- ETM9 : CON11

3.4 RF Interface

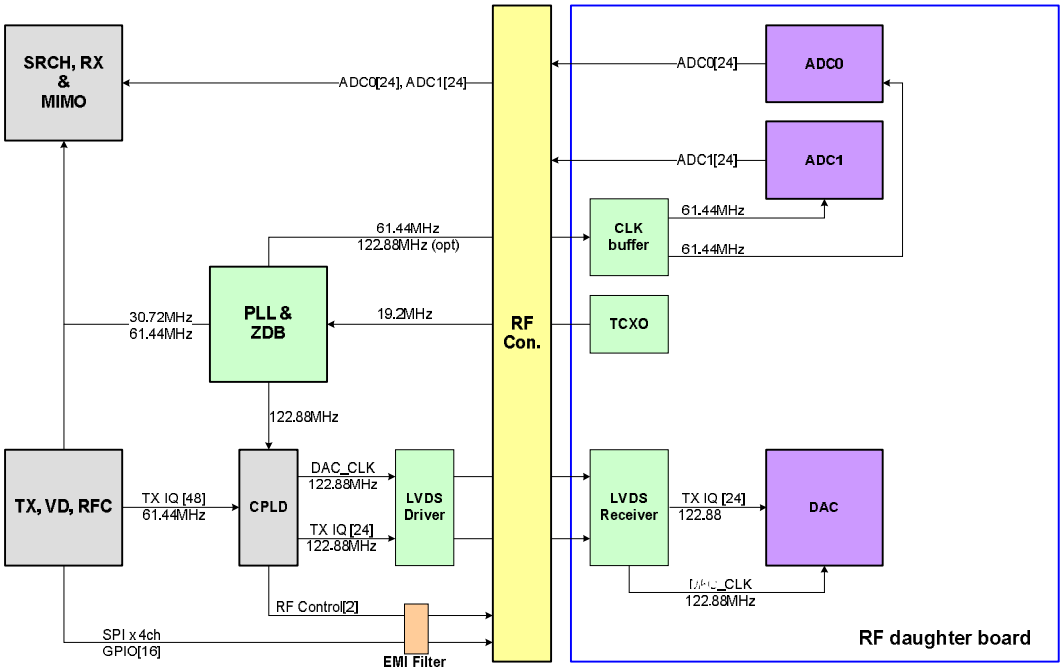

Figure 5. RF interface on LEO2-B platform board

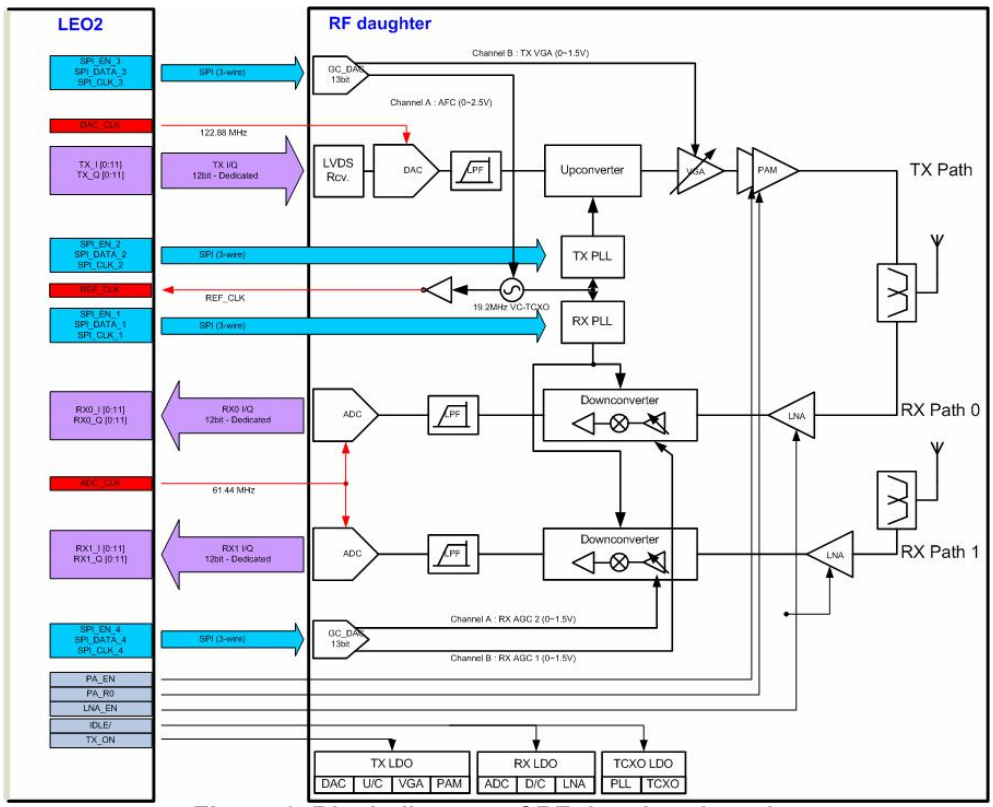

Figure 6. Block diagram of RF daughter board

The LEO2-B Platform supports RF daughter board interface to verify and test LTE UE modem algorithm. The baseband IQ signals are transmitted and received on FPGAs, Transmit part is on TX FPGA and Receive part is on SRCH, MISO FPGA. The bit resolution of IQ signal is 12bits. The sampling frequencies are 122.88MHz for DAC and 61.44MHz for ADC. The transmit signal and sampling clock are delivered through LVDS, because of it's over 100MHz data rate.

The RF control signals, GPIO and SPIs, are generated on TX FPGA.

RF daughter board consist in following blocks

- 2 antenna ports : 1 Tx and 2 Rx
- 14bits TX DAC, 14bits RX ADC
- TX synthesizer, RX synthesizer
- Modulator, Demodulator, VGA,
- Power amp, LNA and passive RF devices
- 3 x 120pin connector

3.5 Reference Clock

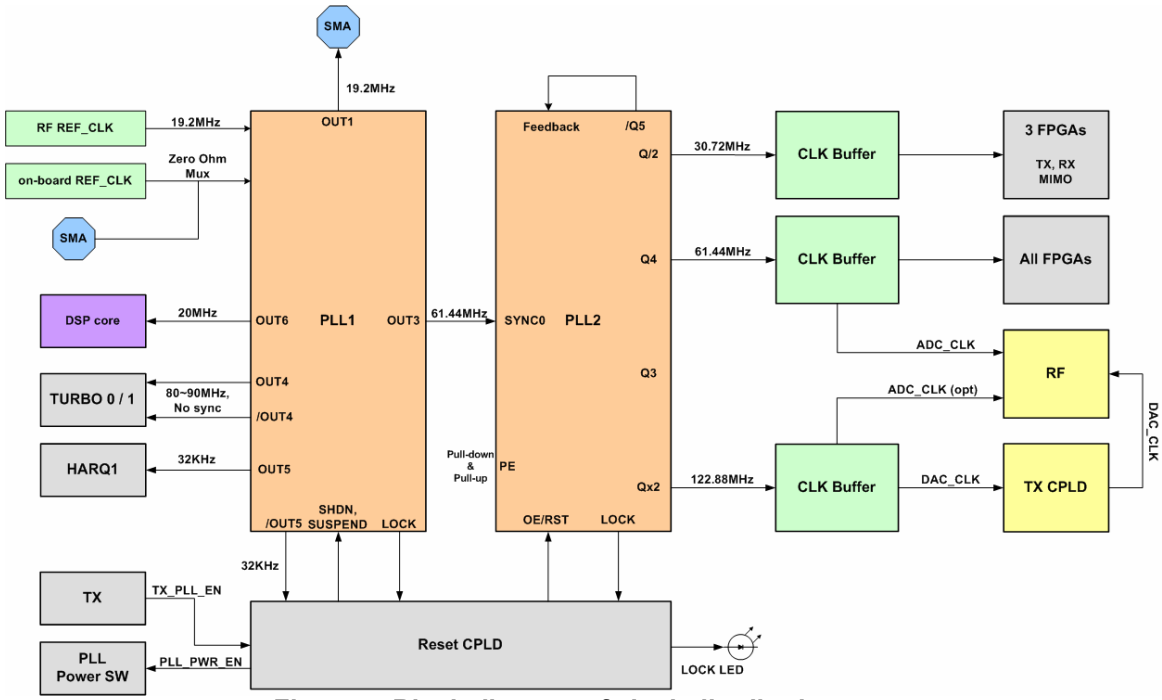

Figure 7. Block diagram of clock distribution

The 19.2MHz reference clock for LEO2-B platform board is supplied from TCXO in RF daughter board. From this ref. clock, all needed clock source for LTE UE modem is synthesized by PLLs. The PLLs generated clock frequencies 30.72, 61.44, 122.88MHz, and 32KHz.

All PLL output clocks are supplied to FPGAs and other blocks. The clock skews on each FPGA input pad is very low <1nsec.

There is additional reference clock oscillator on LEO2-B platform board for without RF daughter board test situations. This clock path selection is controlled by the 7pin on SW6. ('1' on-board, '0' RF daughter board oscillator)

3.6 Reset

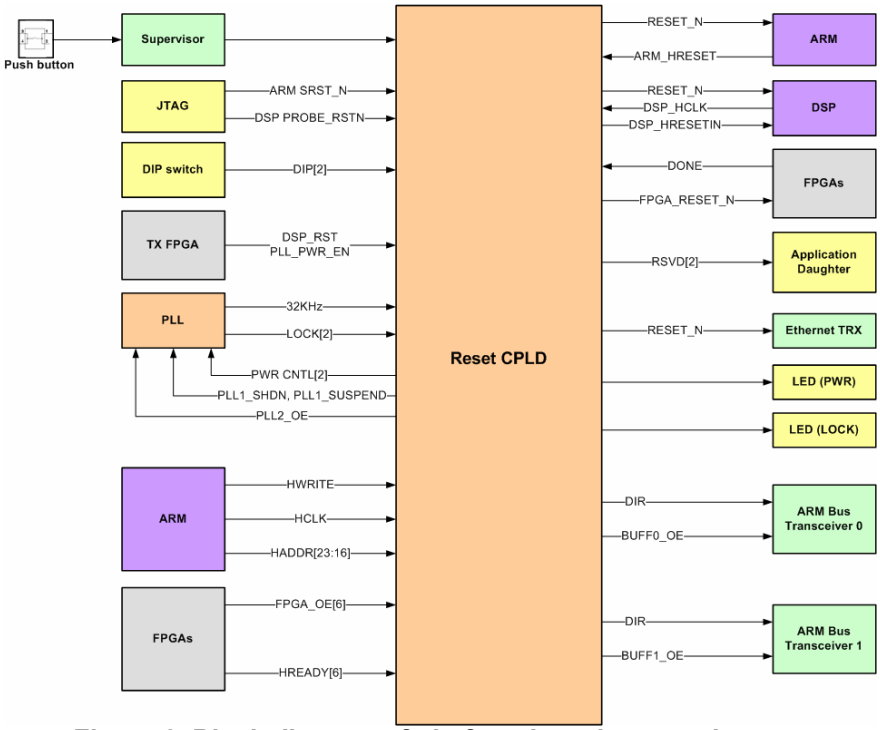

Figure 8. Block diagram of platform board reset scheme

The reset CPLD manages whole system reset scheme for ARM, Ethernet transceiver and each FPGA reset. In the lower left lower corner of the platform board, a manual reset switch is provided.

3.7 Application interface

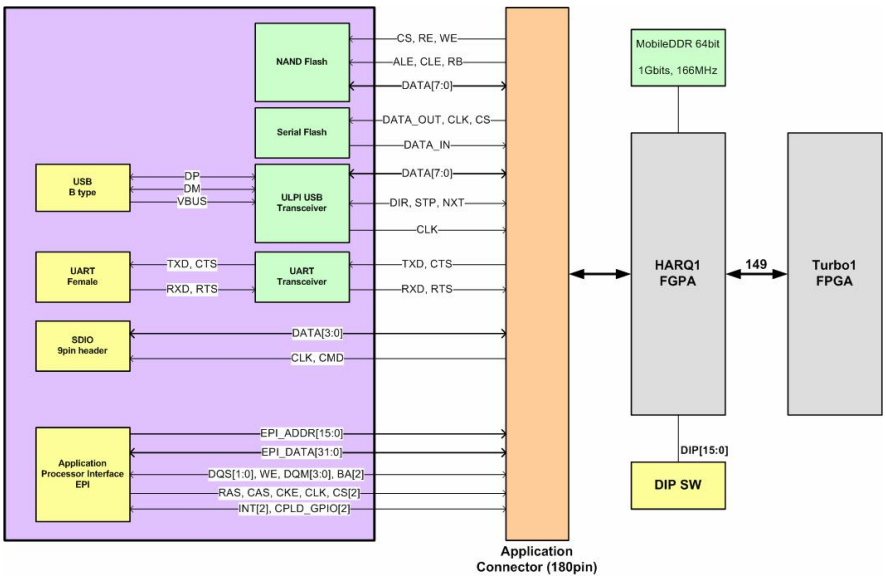

Figure 9. Block diagram of application interface

The LEO2-B platform supports a interface for external connection to application side. 3 kinds of interfaces are supported, EPI, SDIO and USB. Application side will be designed as a platform board at next phase.

3.8 Power Supplies

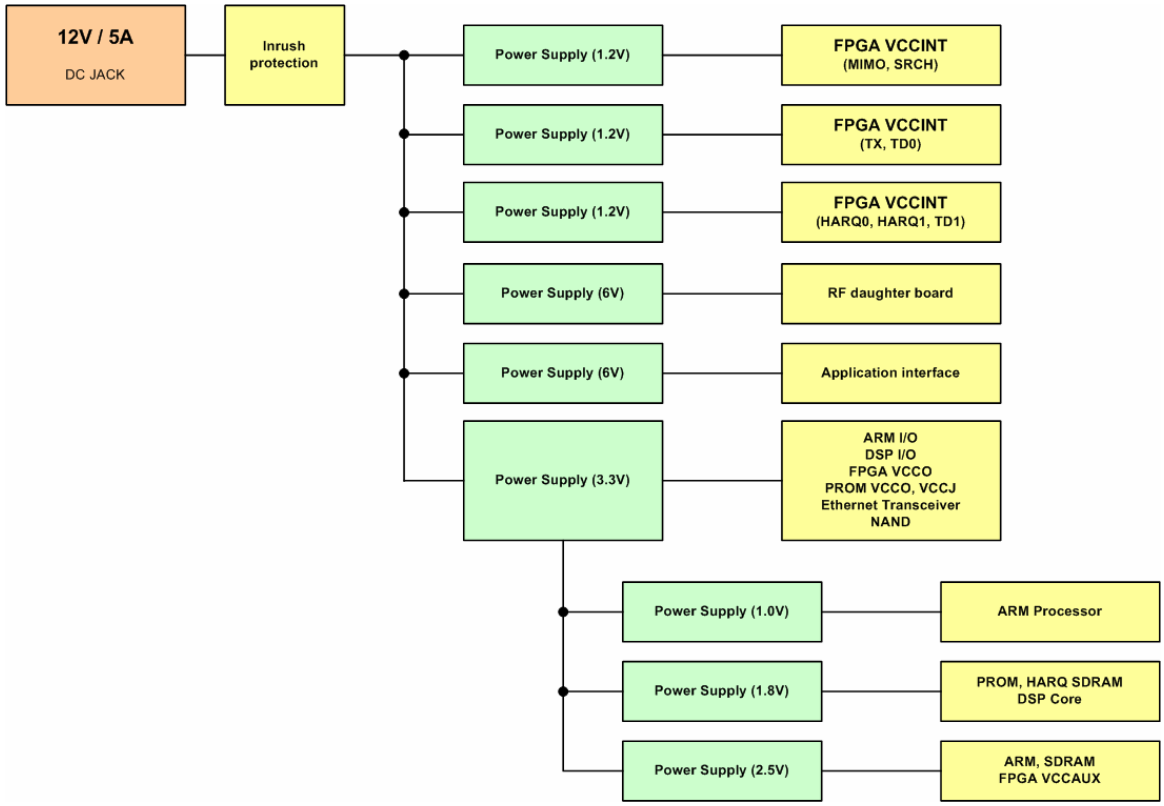

Figure 10. Block diagram of power supplies

External power supplied from DC input jack on the platform board. **To proper operation, external AC to DC power supply should be 12V and >5A.** All needed power sources of platform board are supplied from DC-DC converters and LDOs devices.

4. DIP switch, LED and logic probing connector

4.1 ARM Processor debugging configuration switch setting

Two DIP switches (SW3, SW6) are used to ARM processor configurations and platform board settings. Each control signals are assigned according to *Table 1.* "Switch on" represents "logic low", "switch off" represents "logic high" as other platform boards.

LEO2-B Platform default DIP switch settings are *Table 1.*

Remark: Setting the DIP switch in a wrong way may cause unexpected behavior that can also damage the board since that all the production tests are intended to run in a different environment.

SW3	Pin No.	Name	Description	Default
	1	ARM_INT(0)	ARM Processor interrupt input "on" : assert interrupt "off" : deassert interrupt	OFF
	2	ARM_INT(1)		
	3	ARM_INT(2)		
	4	ARM_INT(3)		
	5	DIPSW_CPLD(0)	Test signal input to reset CPLD "on" : low signal to CPLD	OFF

	6	DIPSW_CPLD(1)	"off" : high signal to CPLD	1
	7	SSP2_SS1	ARM processor booting device selection 'on' Boot from USB 'off' Boot NAND flash	OFF
	8	SMI_WE	Write enable signal of serial flash "on" : write protected "off" : write enabled	OFF
SW6	Pin No.	Name	Description	Default
	1	ARM_TEST(0)	ARM Processor configuration	OFF
	2	ARM_TEST(1)		ON
	3	ARM_TEST(2)		ON
	4	ARM_TEST(3)		OFF
	5	ARM_TEST(4)		ON
	6	ARM_TEST(5)		OFF
	7	CLK_SEL	Reference clock selection 'on' Reference clock from RF daughter 'off' on board reference clock	ON
	8			OFF

Table 1. ARM processor setting DIP switches

4.2 General purpose LED indication

There are several LEDs are present on the board. Their meanings are described in *Table 4-3.* LED turn on represent signal is high or status is good.

LED1	1.2V power OK	LED2	1.2V power OK	LED3	1.2V power OK
LED4	3.3V power OK	LED5	DC IN OK	LED6	1.0V power OK
LED7	Ethernet duplex	LED8	Ethernet link 1000	LED9	Ethernet link 100
LED10	Ethernet link 10	LED11	Ethernet activity		
LED13	2.5V power OK	LED14	All FPGA done	LED15	PLL Lock
LED16	Turbo Dec1 FPGA done	LED17	ARM INT(4)	LED18	TD1 GPIO(0)
LED19	ARM INT(5)	LED20	TD1 GPIO(1)	LED21	ARM INT(6)
LED22	TD1 GPIO(2)	LED23	ARM INT(7)	LED24	TD1 GPIO(3)
LED25	ARM INT(8)	LED26	HARQ1 FPGA Done	LED27	HARQ0 FPGA Done
LED28	HARQ1 GPIO(0)	LED29	HARQ0 GPIO(0)	LED30	HARQ1 GPIO(1)
LED31	HARQ0 GPIO(1)	LED32	1.8V power OK	LED33	HARQ1 GPIO(2)
LED34	HARQ0 GPIO(2)	LED35	HARQ1 GPIO(3)	LED36	HARQ0 GPIO(3)
LED37	MISO FPGA done	LED38	TD0 FPGA Done	LED39	MISO GPIO(0)
LED40	TD0 GPIO(0)	LED41	MISO GPIO(1)	LED42	TD0 GPIO(1)
LED43	MISO GPIO(2)	LED44	TD0 GPIO(2)	LED45	MISO GPIO(3)
LED46	TD0 GPIO(3)	LED47	SRCH FPGA Done	LED48	TX FPGA Done

LED49	SRCH GPIO(0)	LED50	TX GPIO(0)	LED51	SRCH GPIO(1)
LED52	TX GPIO(1)	LED53	SRCH GPIO(2)	LED54	TX GPIO(2)
LED55	SRCH GPIO(3)	LED56	TX GPIO(3)	LED57	RF power OK

Table 2. LED signal mapping

4.3 Logic probing connector

All of the logic analyzer probing headers are MICTOR connector type, agilent E5346A logic analyzer probing adaptor is needed to signal monitoring. Refer to LEO2-B schematic for detailed signal mappings.

5 Description of Smart antenna and beam forming modes if applicable

1) SFBC(Space Frequency Block Code) mode : Transmit diversity mode
   Easily speaking, SFBC which eNB sends same data through 2 antennas means Tx diversity.
2) SM(Spatial multiplexing) mode
   SM which eNB sends different data through 2 antennas helps high data Rate.

   Our LTE UE supports upper 2cases functionality.
   That is, we support smart antenna and beam forming in wide meaning.

6. Reference

[1]

Notice

OEM integrators and installers are instructed that the phrase. This device contains

	Warning: Exposure to Radio Frequency Radiation The radiated output power of this device is far below the FCC radio frequency exposure limits. Nevertheless, the device should be used in such a manner that the potential for human contact during normal operation is minimized. In order to avoid the possibility of exceeding the FCC radio frequency exposure limits, human proximity to the antenna should not be less than 20cm during normal operation. The gain of the antenna for 3GPP-Band4(1710~1755MHz) must not exceed _-4_ dBi. The antenna(s) used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.