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Title LEO3 RF (AWS) Hardware Manual			Type Manual

ABSTRACT

This document is a hardware RF board manual for LTE user equipment platform. Contents of this document are the description of each blocks and usage directions. It is recommended to peruse this manual before operating RF Board.

HISTORY

Rev	Status	Date	Author	Contents

KEY WORDS

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1 Introduction

1.1 Scope

This RF board is intended for radio frequency part of LTE user equipment platform to develop and verify LTE user equipment modem. This RF board is connected to 3rd version of LTE user equipment platform (LEO3) as the form of daughter board. This document intends to describe the brief architecture and usages of the board designed as RF part of LEO3 platform.

1.2 Terminology

ADC	Analog to Digital Converter
AFC	Automatic Frequency Compensation
DAC	Digital to Analog Converter
LO	Local Oscillator
LTE	Long Term Evolution
LVDS	Low-Voltage Differential Signaling
MISO	Multi-In Single-Out
PA	Power Amplifier
RF	Radio Frequency
SAW	Surface Acoustic Wave
UE	User Equipment
VGA	Variable Gain Amplifier

2 Features and Photograph

2.1 Features

- Supporting RF band: UMTS BAND-4(AWS)
  - Transmitting Frequency band: 1,710~1,755 MHz (45MHz)
  - Receiving Frequency band: 2,110~2,155 MHz (45MHz)
- 2-Receive path and 1-Transmit path (MISO)
- +6V dc main power supply
- 19.2 MHz reference clock
- Transceiver
  - Two chips transceiver solution by Infineon SMARTiLTE ICs(PMB_LTE_v093)
  - Triple-band operation
  - Three programmable LTE RF bandwidths: 5,10,20MHz
  - Supply voltage rage from 2.7 ~ 3.0V
  - Optional 2nd supply voltage from 1.71 ~ 3.0V
  - On-chip LDO
  - Different power-down modes
  - 3-wire bus programmable
- 10-bit ADC and DAC support
  - 61.44 MHz for AD conversion
  - 122.88 MHz for DA conversion
- Additional 16-bit HKDAC for Tx VGC and AFC

2.2 Photograph of the LEO3 RF board

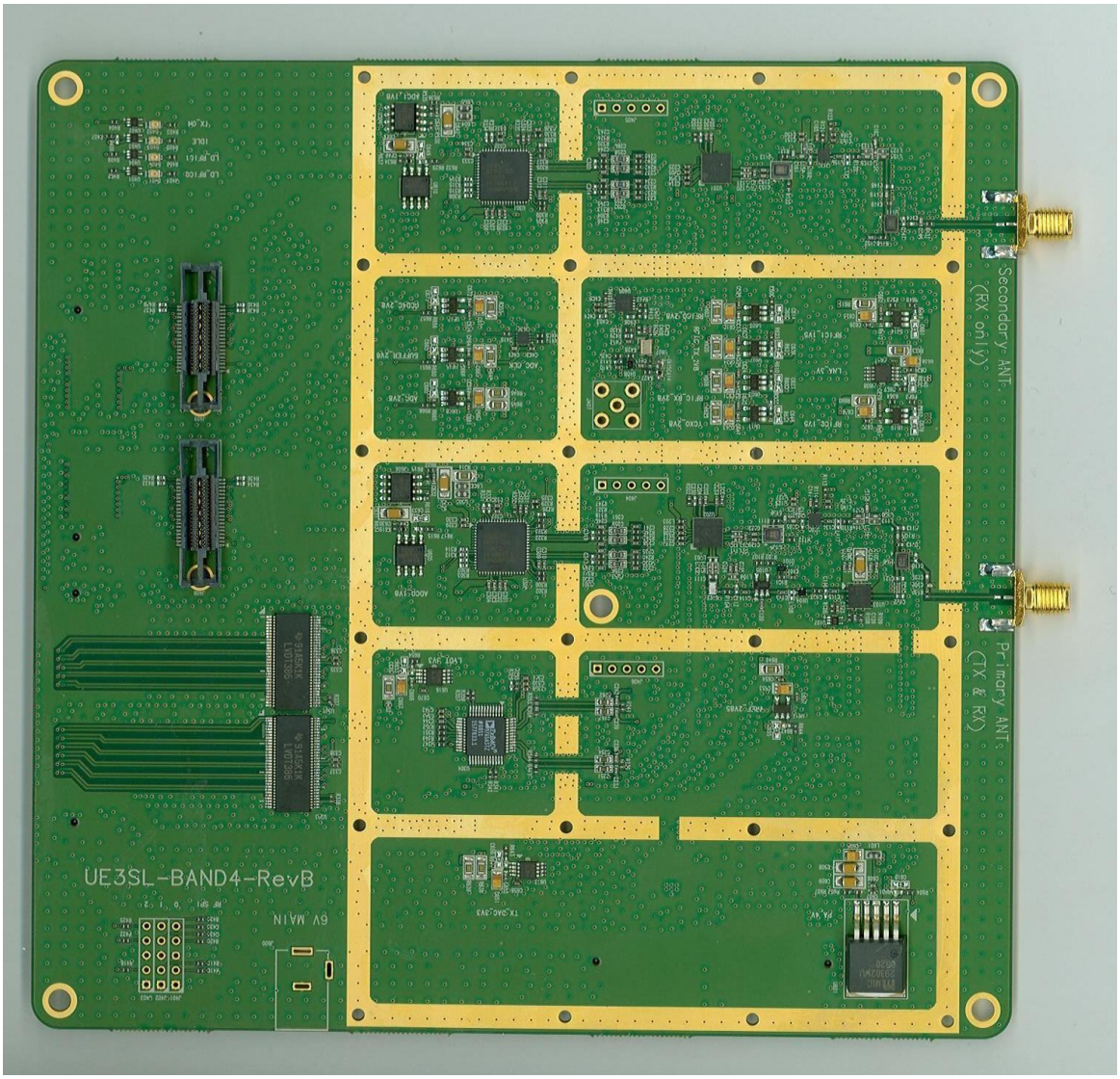

Figure 1: Photograph of LEO3 RF

- Mechanical size of board is 170 (W) X 170 (H) mm

3 Block Diagram and Description

3.1 Block Diagram (AWS)

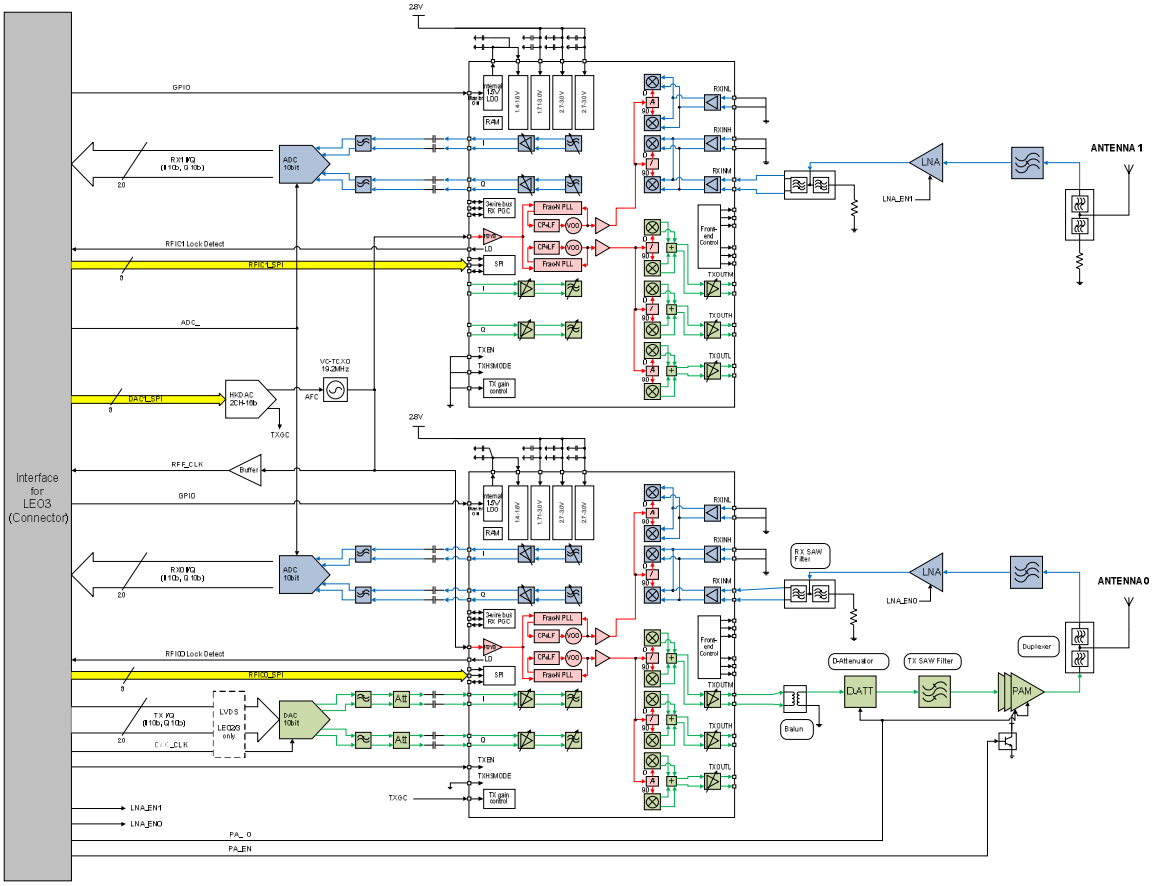

Figure 2: RF Block Diagram (For RX/TX)

3.2 Block Description

3.2.1 RX Blocks

Two receive paths, RX0 path and RX1 path, are designed for MISO technology to increase the receiving data throughput. Both of receiving paths have the same structure and consist of the following transceivers and anything else analog devices.

LNA

- This LNA is used for each receiving path
- LNA has the fixed 20dB gain at range of WCDMA Band4

Transceiver (Rx section)

- LNA2 with three programmable gain steps
- Complete analog baseband path without external components
- Three programmable baseband channel filter bandwidths
- Separate RX PGC 3-wire bus operation possible
- Performance
  - RX Total Gain : 2~80dB
  - Gain step: 1dB

- Gain switching time: under 6 us
- LNA2 Gain: 0/-6/-12 dB
- Gain deviation: +/-3 dB
- NFDSB:12dB – 42dB
- IP1dB: -15dBm

- Support frequency:
  - **Band4: 2,110MHz ~ 2,155MHz**

ADC

- Dual 10-bit, 150MSPS analog-to-digital converter
- 10-bit dedicated for each I/Q data
- A/D clock speed: 61.44MHz
- Two's complement data formatting
- Internal fixed reference mode (the input span is 2 Vp-p)

RX LO

- RX PLL settling time: 320us (initial)
- RX PLL setting time: 150us (handover)
- VCO's +frac-N PLL's +loop filters on chip
- Receive PLL

The principle is exactly the same as for TX, but the frequency offset is now

1633iMHz (instead of 1404 MHz) for all bands but band VII,

Again the result is accommodated in a 13-bit word in the RX PLL Divider Register.

For band VII the offset is 2300 MHz.

3.2.2 TX Blocks

In transmit path, it is connected to a duplexer linked to ANT0. The transmitting data from LEO3 platform is the dedicated 12-bit digital signals for each I/Q via DAC. And its signaling uses LVDS system for high speed data transmitting. Refer to the block diagram at section 2.3. The transmit data pass through the following devices.

Level Translator

- High speed data level conversion, LVDS-to-CMOS

DAC

- Dual 10-bit, 125MSPS digital-to-analog converter
- 10-bit dedicated for each I/Q data
- D/A clock speed: 122.88MHz
- Offset binary data formatting

Transceiver (Tx section)

- RF VGA's with >85dB gain range
- Three programmable baseband filter bandwidths
- Performance
  - POUTmax: 3~7dBm
  - POUTmin: -77dBm
  - TXGC range:0.5V ~ 2.2V
  - Gain switching time:10usec
  - NTX: -136dBm/Hz
  - Carrier suppression:26dB
- Support frequency:
  - **Band4: 1,710MHz ~ 1,755MHz**

Digital Attenuator

- Single 10 dB Step
- Control voltage: -8.5V≤Vc≤+8V

- Low Loss: 0.3 dB @ 900 MHz
- Low Cost SOT-25 Package

Power Amplifier

- Operating frequency: 1,710 ~ 1,785MHz
- Max output power: 28.5dBm

TX LO

- TX PLL settling time: 325us(initial)
- TX PLL settling ime: 150us (Handover)
- VCO's+frac-N PLL's+loop filters on chip

For bands I, II, III, IV and IX the desired frequency is programmed by setting the distance, in multiples of 100 kHz, from the fixed frequency offset of 1404 MHz. The result is accommodated in a 13-bit word in the TX PLL Divider Register.

For bands V, VI and VIII, the programmed frequency must be twice the wanted frequency.

For Band VII the fixed offset is 2250 MHz.

3.2.3 Common Blocks

VCTCXO

- AFC supported by the external gain control voltage
- Generating reference clock for transceiver 1st and 2nd respectively
- Generating baseband clocks as the reference clock source

16-bit HKDAC for AFC and Tx VGC control

- Dual channel 16-bit DAC
- Programmable by 3 wire serial interface, SPI
- Its analog output voltage level functions the following:
  1) AFC support
  2) VGA gain control at transmit path

4 Interface

The RF board for interfacing with LEO3 platform has 3 units of high speed 120pin connector. One of them has the role for main power supply, 6V. The others make the interface between RF to baseband (LEO3 platform) such as data transmitting and receiving, programming the SPI device, transmitting control signals, supplying A/D or D/A clock, monitoring the status and etc.

4.1 Power supply

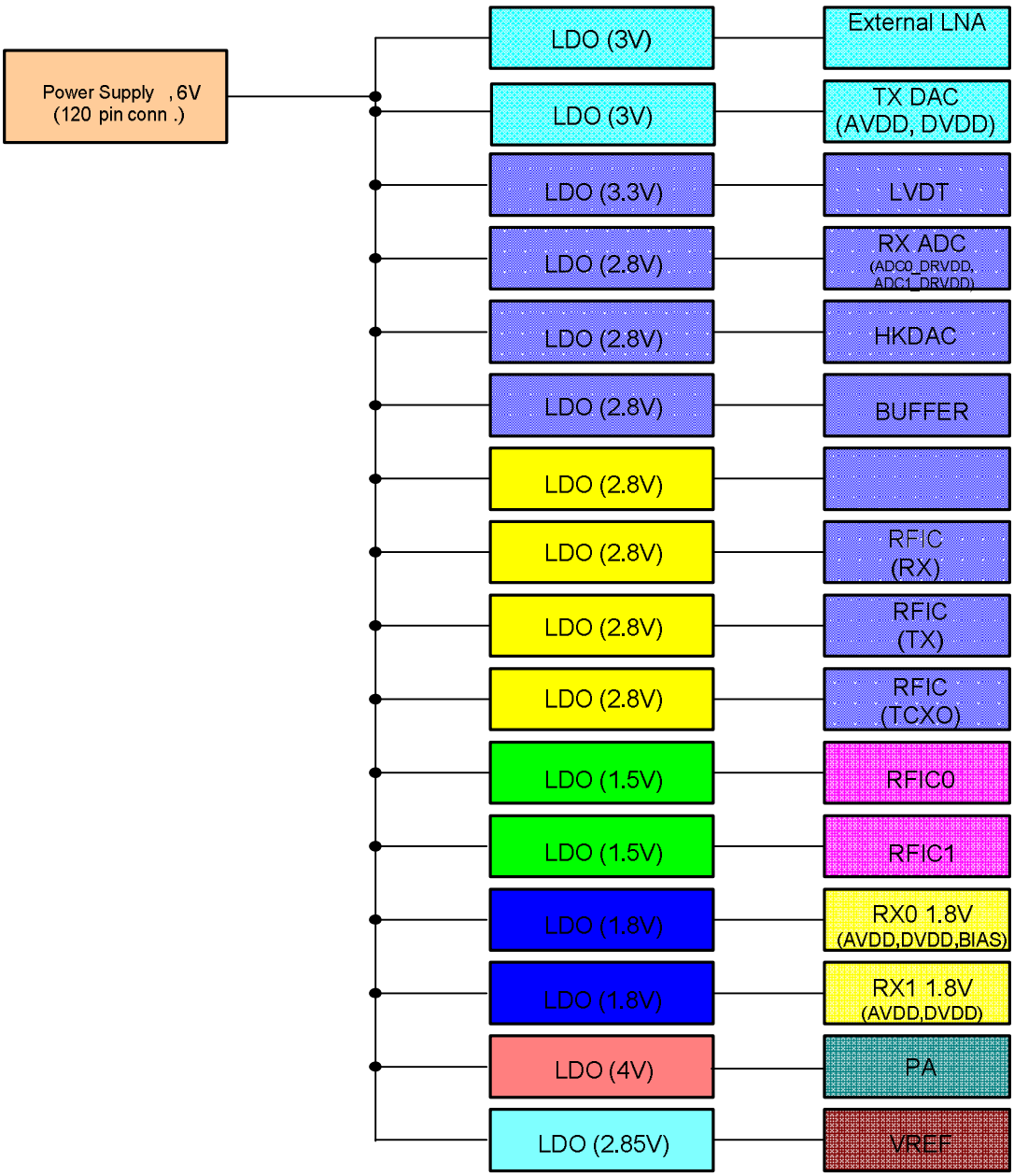

Figure 3: Diagrams of Power supply

4.2 Digital I/Q Data & Sampling Cock

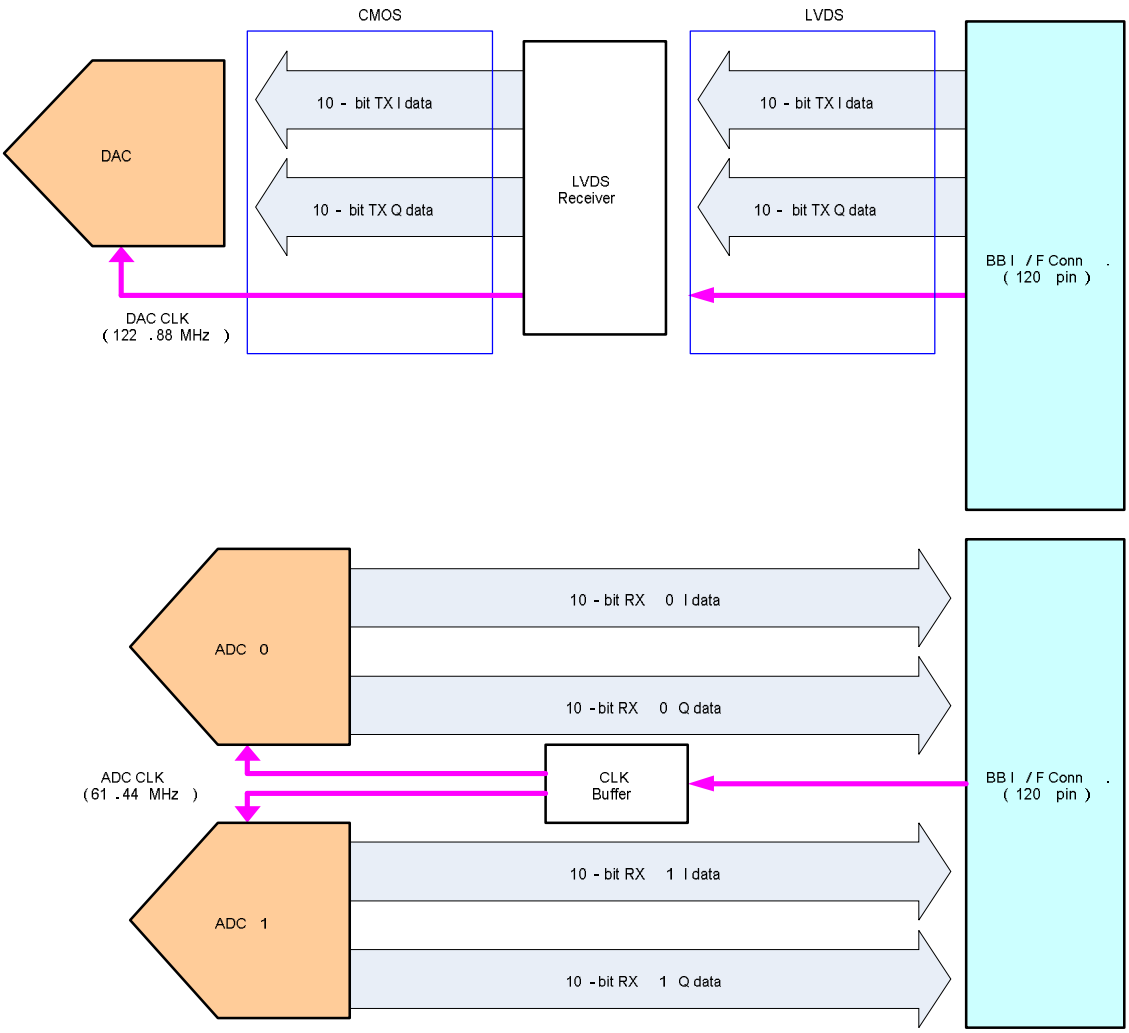

Figure 4: Diagrams of Data & Clock Signal Interface

4.3 SPI

There are 3 programmable devices on RF board by using 3 wire SPI interface. 3 units SPI blocks exist on the interface with baseband platform. They are listed at Table 1 (Also refer to block diagram at Figure 5).

At this list, 1st transceiver and 2nd transceiver consist of each SPI0 and SPI1. Also 16-bit HKDAC has the dedicated by SPI2. It can be possible by using a dedicated chip select signal for each device with LLDM software. When selecting one of them, a dedicated chip select signal enables its device to program.

SPI Device	1st Transceiver	2nd Transceiver	16bit-HKDAC
SPI block	SPI0	SPI1	SPI2
SPI data bit	-	-	16

Table 1: List of SPI programmable devices

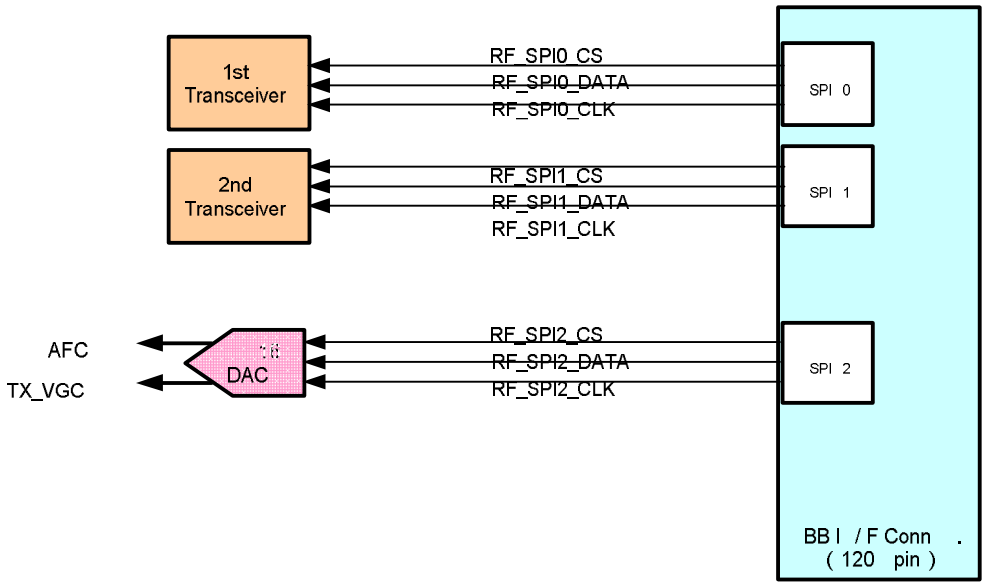

Figure 5: Diagram of SPI interface

4.4 Control signals (GPIO's)

For control the RF blocks, the control signals from LEO3 platform are connected as the below.

- BS(1)_IDLE: Enables the LDOs and LED for a self-Indicator
- TX_ON: Enables the LDOs at transmit path and transmit block at 1st Transceiver (Including turns on LED for a self-indicator)
- PA_R0 : Controls the power mode of transmitter block (Including D-attenuator)
- PA_EN : Enables PA
- LNA_EN0: Enables the LNA of antenna0 path (At the 1st transceiver)
- LNA_EN1: Enables the LNA of antenna1 path (At the 2nd transceiver)
- TCXO_ON: Enables the LDO for source clock (VC-TCXO)
- GPIO_SLEEPB(0): Enables the 1st transceiver (Via Master on signal)
- GPIO_SLEEPB(1): Enables the 2nd transceiver (Via Master on signal)

4.5 LEDs

To indicate PLL lock status of 1st transceiver(LD_RFIC0) and 2nd transceiver(LD_RFIC1), two LEDs (D401, D404) are present on the board. When locked at the frequency by setting the SPI from LEO3, LD output of each Transceiver turns on this LED.

Anything else, there are two more LEDs(D4032 D403) for TX_ON and IDLE.

4.6 Logic probing header

The type of logic probing header is MICTOR connector. For each receive path, 20-bit dedicated I/Q data is mapped to this (J408, J409). When using this logic probing, agilent E5346A logic analyzer probing adaptor is needed to signal monitoring. The following figure is captured from the schematic.

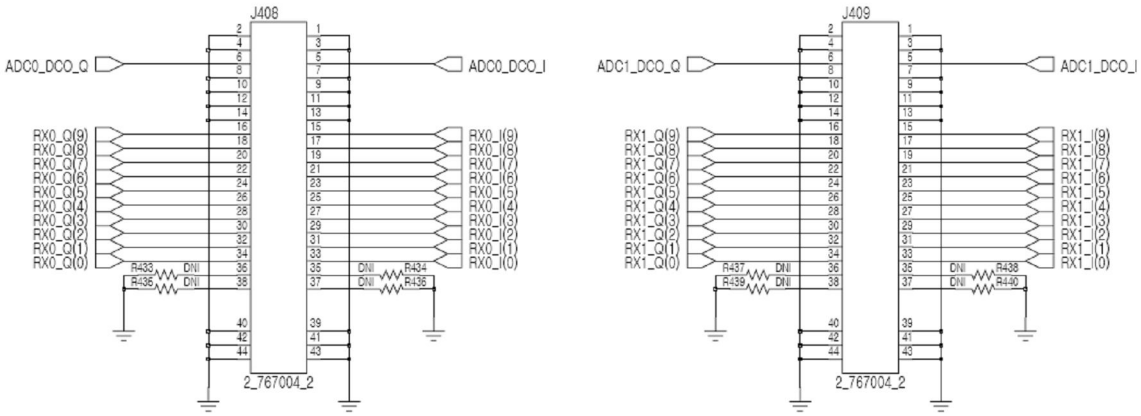

Figure 6: RX I/Q data probing Interface

5 Placement Map

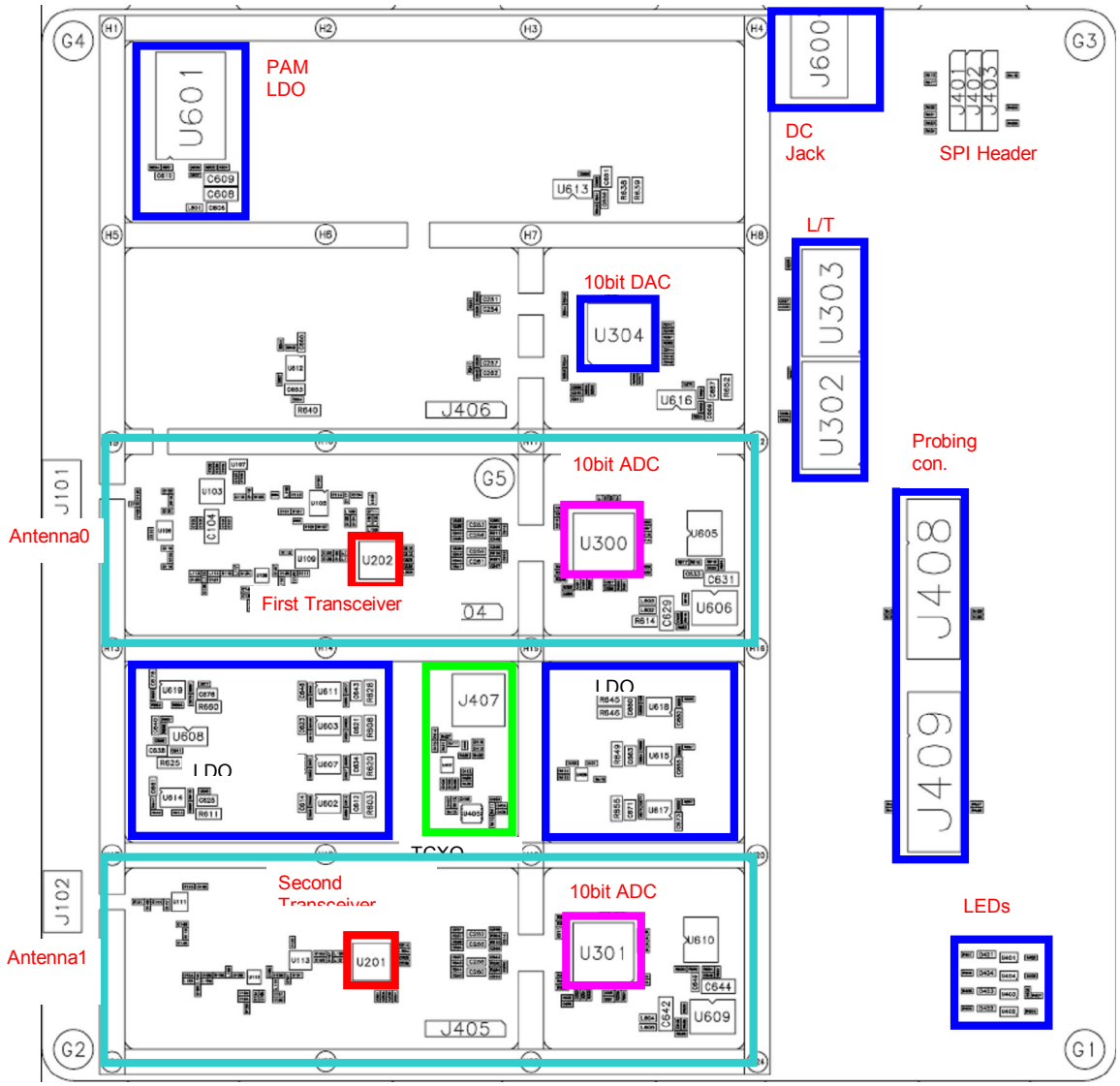

Figure 7: Top placement map of LEO3 RF (AWS)

Notice

OEM integrators and installers are instructed that the phrase. This device contains

	Warning: Exposure to Radio Frequency Radiation The radiated output power of this device is far below the FCC radio frequency exposure limits. Nevertheless, the device should be used in such a manner that the potential for human contact during normal operation is minimized. In order to avoid the possibility of exceeding the FCC radio frequency exposure limits, human proximity to the antenna should not be less than 20cm during normal operation. The gain of the antenna for 3GPP-Band4(1710~1755MHz) must not exceed _-4_ dBi. The antenna(s) used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.