# ATTACHMENT E.

## - User Manual -

| LG Electronics | Updated | File<br>BAND13 RF board manual | Rev. |
|---|---|---|---|
| Written by | Reviewed by | Granted by | Managed by |
| Title<br>LEO3 RF (Band13) Hardware Manual | | | Type<br>Manual |


**ABSTRACT**

This document is a hardware RF board manual for LTE user equipment platform. Contents of this document are the description of each blocks and usage directions. It is recommended to peruse this manual before operating RF Board.


**HISTORY**

| Rev | Status | Date | Author | Contents |
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**KEY WORDS**


LG Electronics

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# 1 Introduction

## 1.1 Scope

This RF board is intended for radio frequency part of LTE user equipment platform to develop and verify LTE user equipment modem. This RF board is connected to 3rd version of LTE user equipment platform (LEO3) as the form of daughter board. This document intends to describe the brief architecture and usages of the board designed as RF part of LEO3 platform.

## 1.2 Terminology

| | |
|---|---|
| ADC | Analog to Digital Converter |
| AFC | Automatic Frequency Compensation |
| DAC | Digital to Analog Converter |
| LO | Local Oscillator |
| LTE | Long Term Evolution |
| LVDS | Low-Voltage Differential Signaling |
| MISO | Multi-In Single-Out |
| PA | Power Amplifier |
| RF | Radio Frequency |
| SAW | Surface Acoustic Wave |
| UE | User Equipment |
| VGA | Variable Gain Amplifier |

# 2 Features and Photograph

## 2.1 Features

- Supporting RF band: BAND-13
  - Transmitting Frequency band: 777 ~ 787 MHz (10MHz)
  - Receiving Frequency band: 746 ~ 756 MHz (10MHz)
- 2-Receive path and 1-Transmit path (MISO)
- +6V dc main power supply
- 19.2 MHz reference clock
- Transceiver
  - Two chips transceiver solution by Infineon SMARTiLTE ICs(PMB_LTE_v093)
  - Triple-band operation
  - Three programmable LTE RF bandwidths: 5,10,20MHz
  - Supply voltage rage from 2.7 ~ 3.0V
  - Optional 2nd supply voltage from 1.71 ~ 3.0V
  - On-chip LDO
  - Different power-down modes
  - 3-wire bus programmable
- 10-bit ADC and DAC support
  - 61.44 MHz for AD conversion
  - 122.88 MHz for DA conversion
- Additional 16-bit HKDAC for Tx VGC and AFC

## 2.2 Photograph of the LEO3 RF board

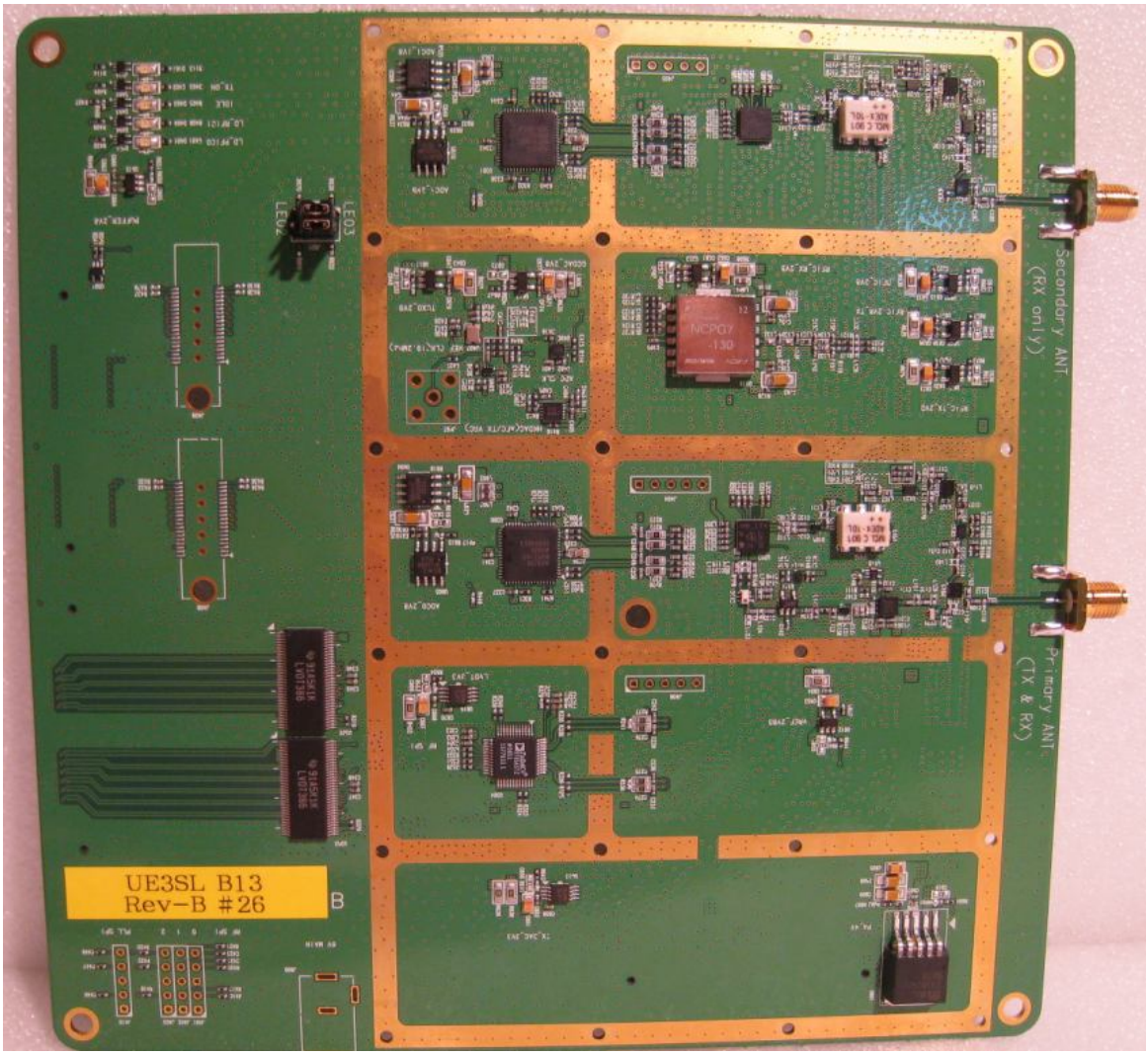


**Figure 1: Photograph of LEO3 RF**

- Mechanical size of board is 170 (W) X 170 (H) mm

# 3 Block Diagram and Description

## 3.1 Block Diagram

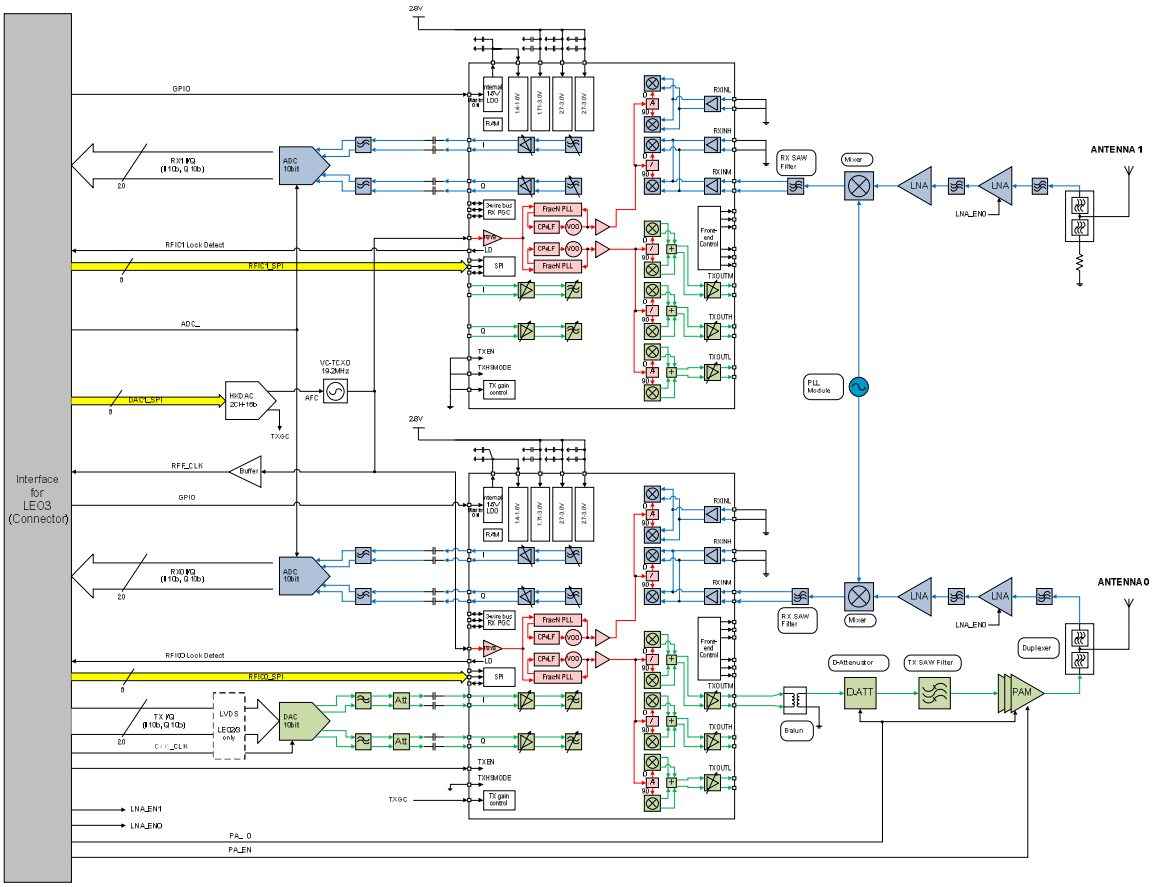


**Figure 2: RF Block Diagram (For RX/TX)**

## 3.2 Block Description

### 3.2.1 RX Blocks

Two receive paths, RX0 path and RX1 path, are designed for MISO technology to increase the receiving data throughput. Both of receiving paths have the same structure and consist of the following transceivers and anything else analog devices.

LNA
- This LNA is used for each receiving path
- LNA has the fixed 14dB gain at range of Band13

Transceiver (RX section)
- LNA2 with three programmable gain steps
- Complete analog baseband path without external components
- Three programmable baseband channel filter bandwidths
- Separate RX PGC 3-wire bus operation possible
- Performance
  - RX Total Gain : 2~80dB
  - Gain step: 1dB

- Gain switching time: under 6 us
- LNA2 Gain: 0/-6/-12 dB
- Gain deviation: +/-3 dB
- NFDSB:12dB – 42dB
- IP1dB: -15dBm

ADC
- Dual 10-bit, 150MSPS analog-to-digital converter
- 10-bit dedicated for each I/Q data
- A/D clock speed: 61.44MHz
- Two's complement data formatting
- Internal fixed reference mode (the input span is 2 Vp-p)

RX PLL
- A Module type consisting of PLL and VCO
- Programmalbe by 3 wire serial interface, SPI

### 3.2.2 TX Blocks

In transmit path, it is connected to a duplexer linked to ANT0. The transmitting data from LEO3 platform is the dedicated 10-bit digital signals for each I/Q via DAC. And its signaling uses LVDS system for high speed data transmitting. Refer to the block diagram at section 2.3. The transmit data pass through the following devices.

Level Translator
- High speed data level conversion, LVDS-to-CMOS

DAC
- Dual 10-bit, 125MSPS digital-to-analog converter
- 10-bit dedicated for each I/Q data
- D/A clock speed: 122.88MHz
- Offset binary data formatting

Transceiver (TX section)
- RF VGA's with >85dB gain range
- Three programmable baseband filter bandwidths
- Performance
  - POUTmax: 3~7dBm
  - POUTmin: -77dBm
  - TXGC range:0.5V ~ 2.2V
  - Gain switching time:10usec
  - NTX: -136dBm/Hz
  - Carrier suppression:26dB

Digital Attenuator
- Single 10 dB Step
- Control voltage: -8.5V≤Vc≤+8V
- Low Loss: 0.3 dB @ 900 MHz

Power Amplifier
- Operating frequency: 1,710 ~ 1,785MHz
- Max output power: 28.5dBm

### 3.2.3 Common Blocks

VCTCXO
- AFC supported by the external gain control voltage
- Generating reference clock for transceiver 1st and 2nd respectively
- Generating reference clock for RX PLL
- Generating baseband clocks as the reference clock source

16-bit HKDAC for AFC and TX VGC control
- Dual channel 16-bit DAC
- Programmable by 3 wire serial interface, SPI
- Its analog output voltage level functions the following:
  1) AFC support
  2) VGA gain control at transmit path

## 4 Interface

The RF board for interfacing with LEO3 platform has 3 units of high speed 120pin connector. One of them has the role for main power supply, 6V. The others make the interface between RF to baseband (LEO3 platform) such as data transmitting and receiving, programming the SPI device, transmitting control signals, supplying A/D or D/A clock, monitoring the status and etc.

### 4.1 Power supply

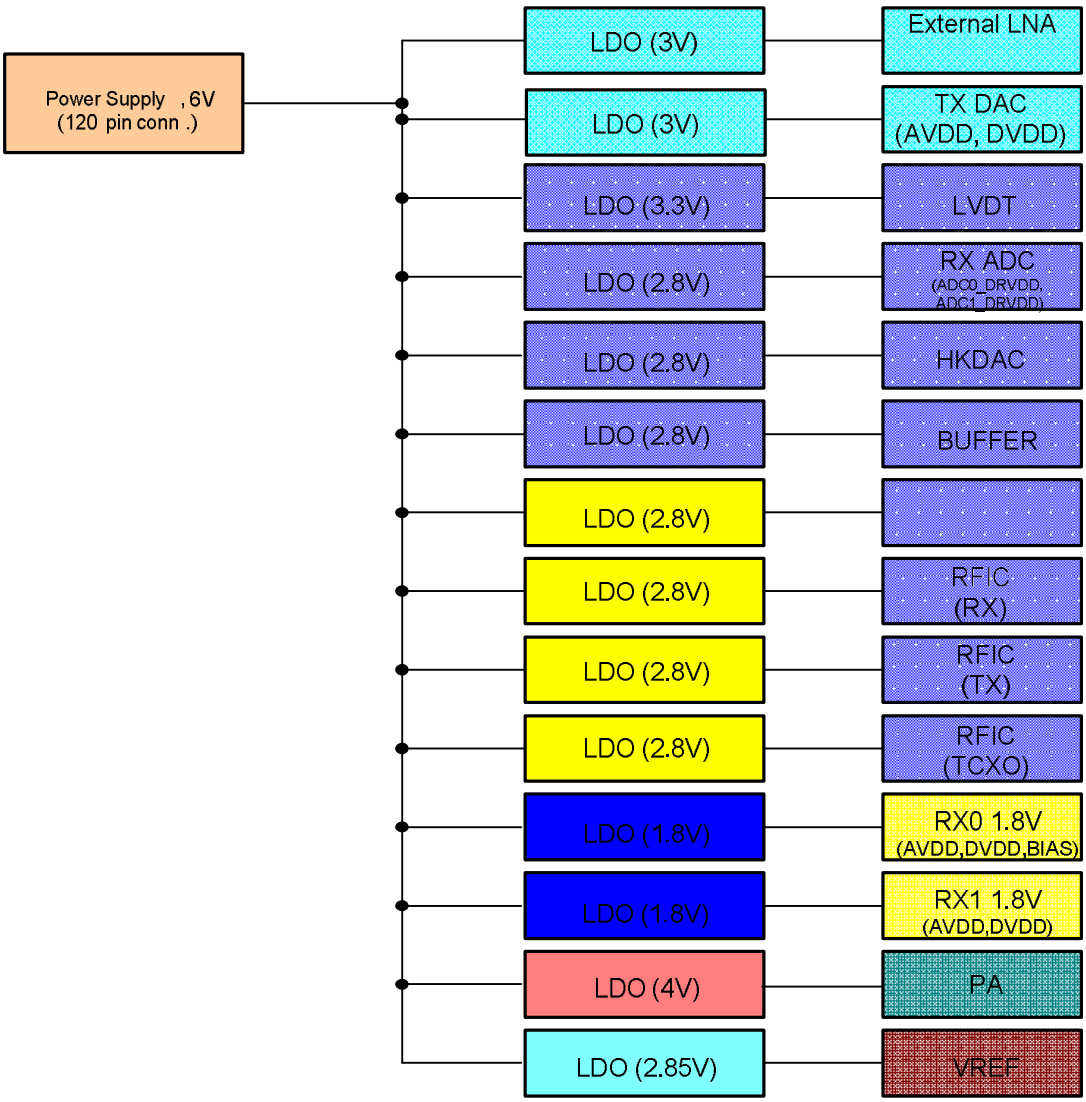


**Figure 3: Diagrams of Power supply**

## 4.2 Digital I/Q Data & Sampling Cock

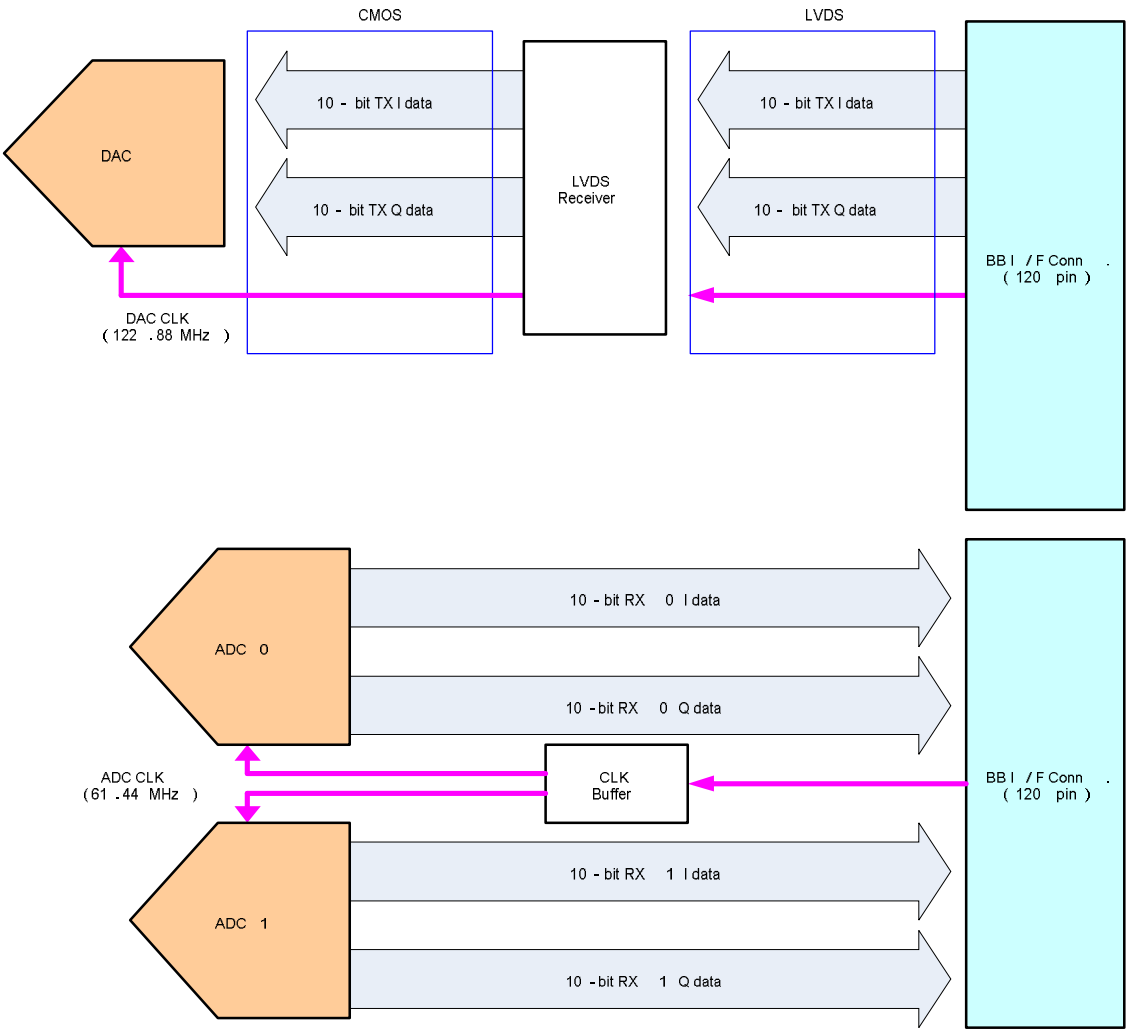


**Figure 4: Diagrams of Data & Clock Signal Interface**

## 4.3 SPI

There are 3 programmable devices on RF board by using 3 wire SPI interface. 3 units SPI blocks exist on the interface with baseband platform. They are listed at Table 1 (Also refer to block diagram at Figure 5).

At this list, 1st transceiver and 2nd transceiver consist of each SPI0 and SPI1. Also 16-bit HKDAC has the dedicated by SPI2. It can be possible by using a dedicated chip select signal for each device with LLDM software. When selecting one of them, a dedicated chip select signal enables its device to program.

| SPI Device | 1st Transceiver | 2nd Transceiver | 16bit-HKDAC |
|---|---|---|---|
| SPI block | SPI0 | SPI1 | SPI2 |
| SPI data bit | - | - | 16 |

**Table 1: List of SPI programmable devices**

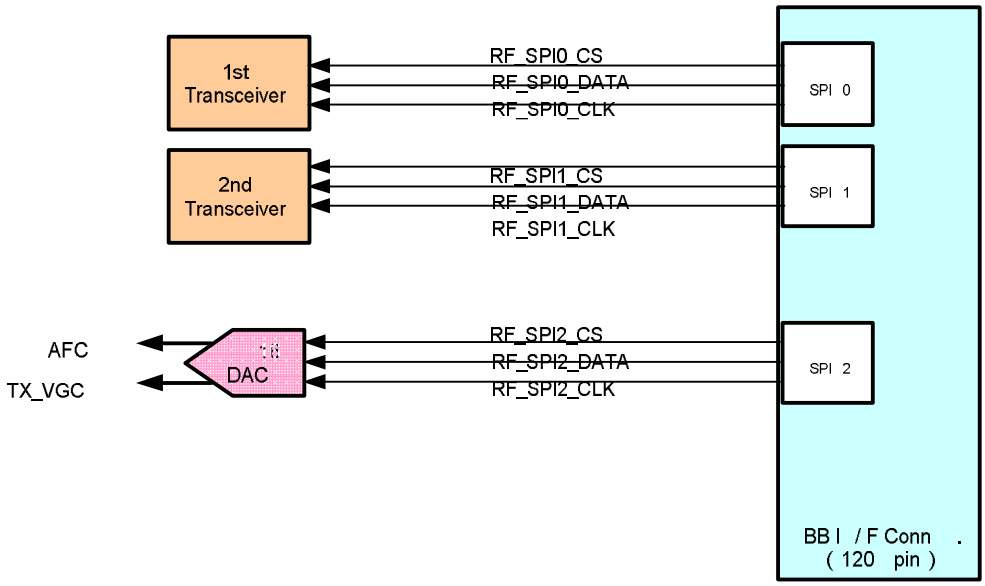


**Figure 5: Diagram of SPI interface**

## 4.4 Control signals (GPIO's)

For control the RF blocks, the control signals from LEO3 platform are connected as the below.

- BS(1)_IDLE: Enables the LDOs and LED for a self-Indicator
- TX_ON: Enables the LDOs at transmit path and transmit block at 1st Transceiver (Including turns on LED for a self-indicator)
- PA_R0 : Controls the power mode of transmitter block (Including D-attenuator)
- PA_EN : Enables PA
- LNA_EN0: Enables the LNA of antenna0 path (At the 1st transceiver)
- LNA_EN1: Enables the LNA of antenna1 path (At the 2nd transceiver)
- TCXO_ON: Enables the LDO for source clock (VC-TCXO)
- GPIO_SLEEPB(0): Enables the 1st transceiver (Via Master on signal)
- GPIO_SLEEPB(1): Enables the 2nd transceiver (Via Master on signal)

## 4.5 LEDs

To indicate PLL lock status of 1st transceiver(LD_RFIC0), 2nd transceiver(LD_RFIC1) and RX PLL, three LEDs are present on the board. When locked at the frequency by setting the SPI from LEO3, LD output of each Transceiver and RX PLL turns on these LEDs.

Anything else, there are two more LEDs(D4032 D403) for TX_ON and IDLE.

## 5 Placement Map

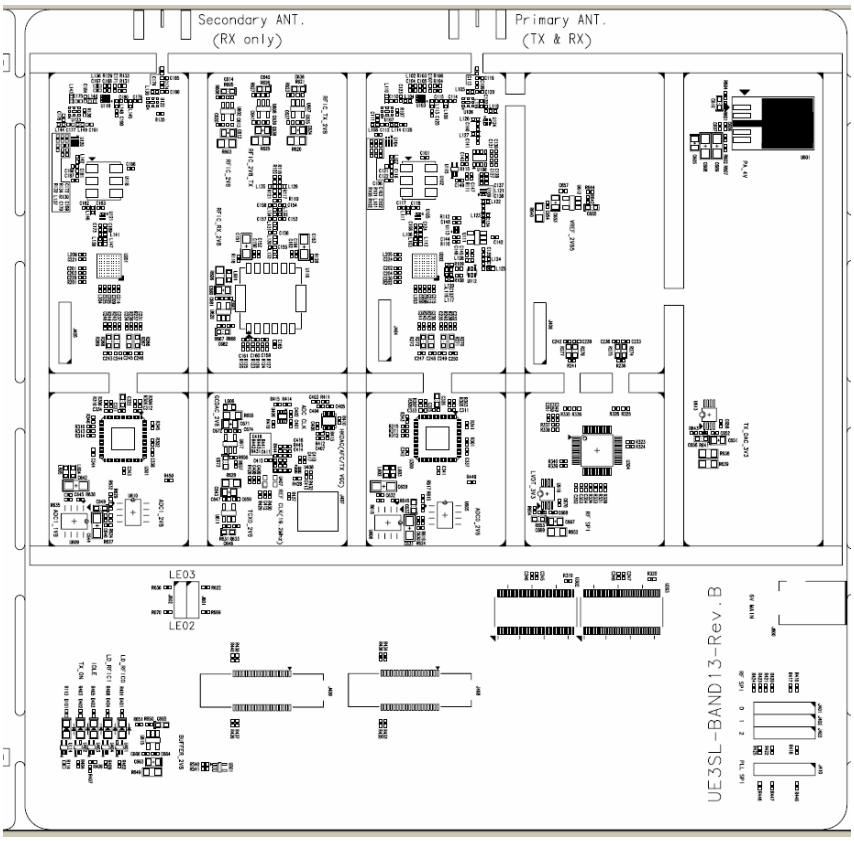


**Figure 6: Top placement map of LEO3 RF (Band13)**

Notice

OEM integrators and installers are instructed that the phrase. This device contains

| | |
|---|---|
|  | Warning: Exposure to Radio Frequency Radiation The radiated output power of this device is far below the FCC radio frequency exposure limits. Nevertheless, the device should be used in such a manner that the potential for human contact during normal operation is minimized. In order to avoid the possibility of exceeding the FCC radio frequency exposure limits, human proximity to the antenna should not be less than 20cm during normal operation. The gain of the antenna for 3GPP-Band13(777~787MHz) must not exceed ~~-2.3~~ dBi.<br><br>The antenna(s) used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. |

## ABSTRACT

## HISTORY

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## KEY WORDS

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# 1 Introduction

## 1.1 Scope

This document describes briefly the board level operations, key features and the environment of the LEO3 Platform Rev.A / Rev.B. The purpose of this platform is the verification of LG LTE ASIC, namely 'L1000', and the evaluation of LG UE system performance.

The further details about the characteristics and functions of L1000 are available on other documents.

LEO3 platform consists of a core board, a main board, an RF board and application boards. For the core board, two types of 'MOC-D' and 'MDC-D' are available on the LEO3 platform.

With the 'MOC-D' board, it is possible to implement and perform the functionalities of 'Mobile Platform' with additional application boards. In case of there being no application boards, also is it possible to implement and perform the functionalities of 'Data Card' with USB cables.

With the 'MDC-D' board, it is possible to implement and perform the functionalities of 'Data Card' the same as 'MOC-D' without application boards. And is it possible to probe and capture the signals (raw data) out of the modem part with the external DSP Bus I/F and Ethernet MAC.

But it will be focused on MOC-D only without application board in this document.

Although this platform is built with some boards, it will be described on the baseband board without application and RF board.

## 1.2 Terms and Definitions

LTE: Long Term Evolution
M-DDR: Mobile DDR
MOC-D: Modem Only Core - D
MDC-D: Modem and DSP Core – D
GMII: Gigabit Media Independent Interace
DM: Diagnostic Monitoring

# 2 Key Features and Pictures of the Platform

## 2.1 Key Features

### 2.1.1 L1000

- ARM1136JF-S with 307.2MHz core clock
- 32kB I-Cache/ 32kB D-Cache
- 32kB I-TCM/ 16kB D-TCM
- 64kB SRAM
- 128kB Boot ROM
- 16-channel DMA with 64bit AHB interface
- 64bit/32bit AHB interface with 153.6MHz
- 32bit M-DDR SDRAM controller with 153.6MHz (up to 2Gb)
- 8bits NAND Flash controller
- 2 port USB 2.0 HS device controller (Host interface/DM interface)
- 20-GPIOs with interrupt capability
- 1-channel I2C
- 1-channel UART
- 3-channel 4wire SPIs for RF control
- 1-channel general 3wire SPI
- 1-channel general 4wire SPI
- 19.2MHz reference clock
- 48MHz clock for USB/UART/I2C/Timer
- 122.88MHz DAC / 61.44MHz ADC clock
- 32.768kHz RTC clock
- 1 Tx antenna interface with 10bit I/Q
- 2 Rx antenna interface with 10bit I/Q
- External hardwire boot configuration

- Debugger port (JTAG + ETM11)

2.1.2 Memory
- MCP with 2Gb 8bit NAND flash / DDR333 1Gb 32bit M-DDR
- 64Mb Serial NOR flash (4wire SPI)

2.1.3 Other peripherals
- PMIC for evaluation and feasibility check
- 2-USB connectors
- LVDS drivers for 10bit I/Q Tx signal and DAC clock
- Application board interface (unavailable in this document)
- 1-channel SIM connector
- 1-channel 4bit SDIO connector (only available for MDC-D core board)
- JTAG/ETM 11 debug ports for ARM (ETM clock with 76.8MHz)
- JTAG debug port for DSP (only available for MDC-D core board)
- 1-Gigabit Ethernet (GMII mode) connector for DSP (only available for MDC-D core board)
- RF interface with connector (bottom side)
- Reset switch for global hardware reset
- 15 LEDs and 2 DIP-switches for debug
- 5 LEDs for Ethernet mode monitor (only available for MDC-D core board)
- 8 LEDs for DSP GPIO (only available for MDC-D core board)
- 2 DIP-switches for boot configuration setting

## 2.2 Pictures and Placement of the Platform

2.2.1 Pictures of LEO3 Platform

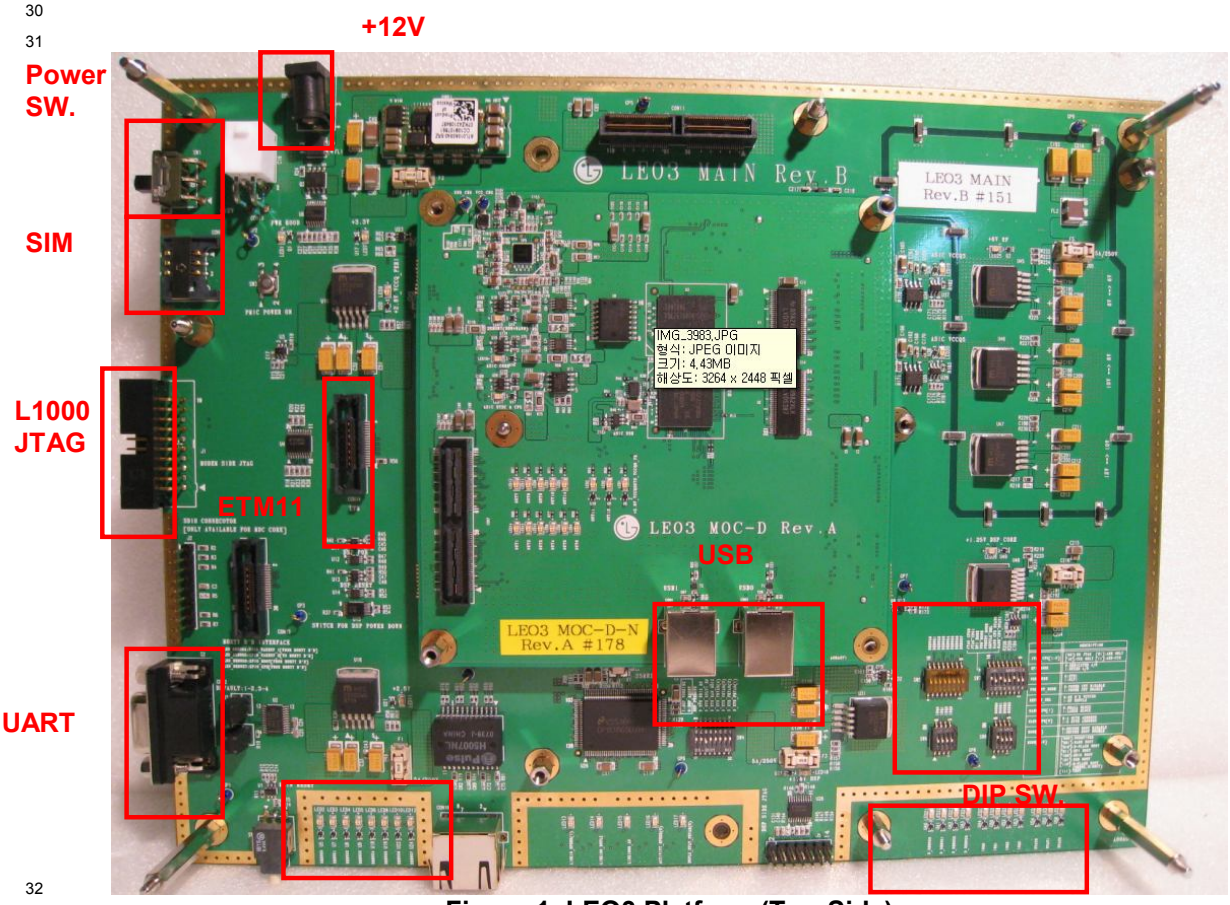


**Figure 1. LEO3 Platform (Top Side)**

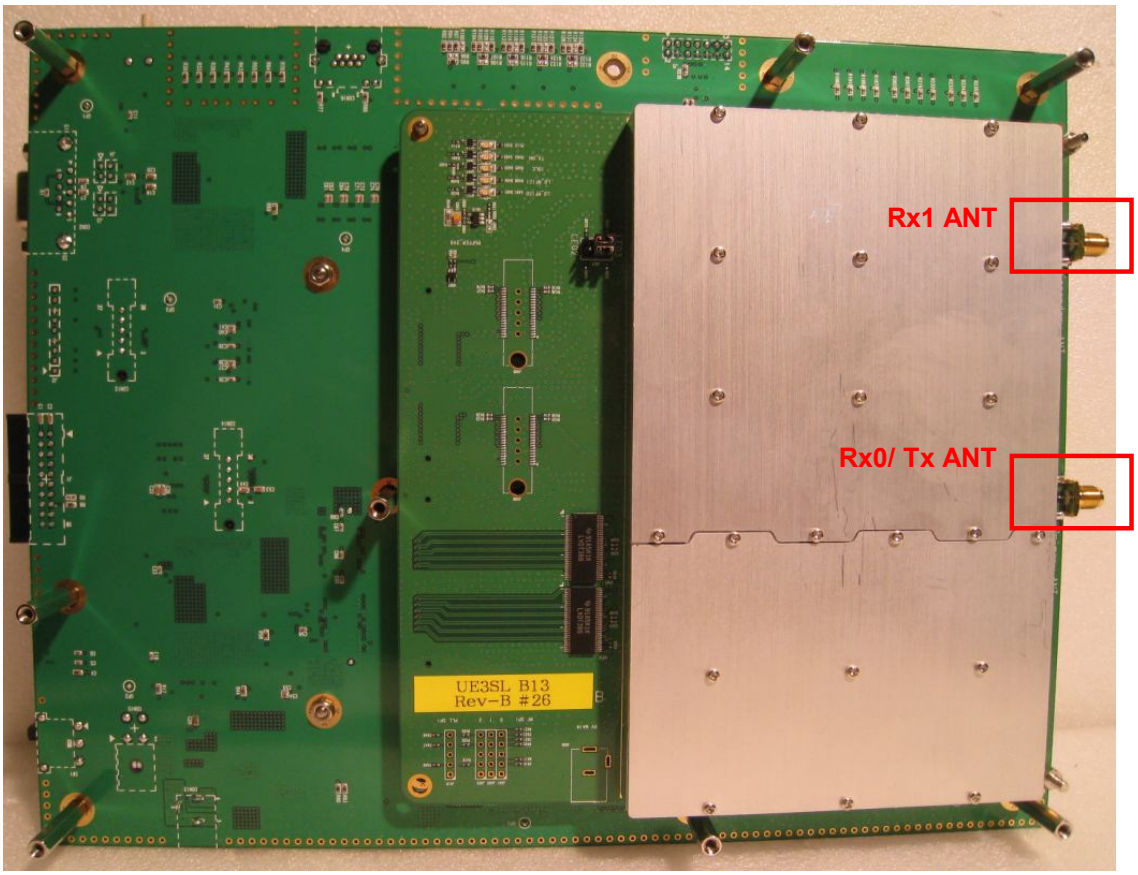


**Figure 2. LEO3 Platform (Bottom Side)**

### 2.2.2 Placement Map

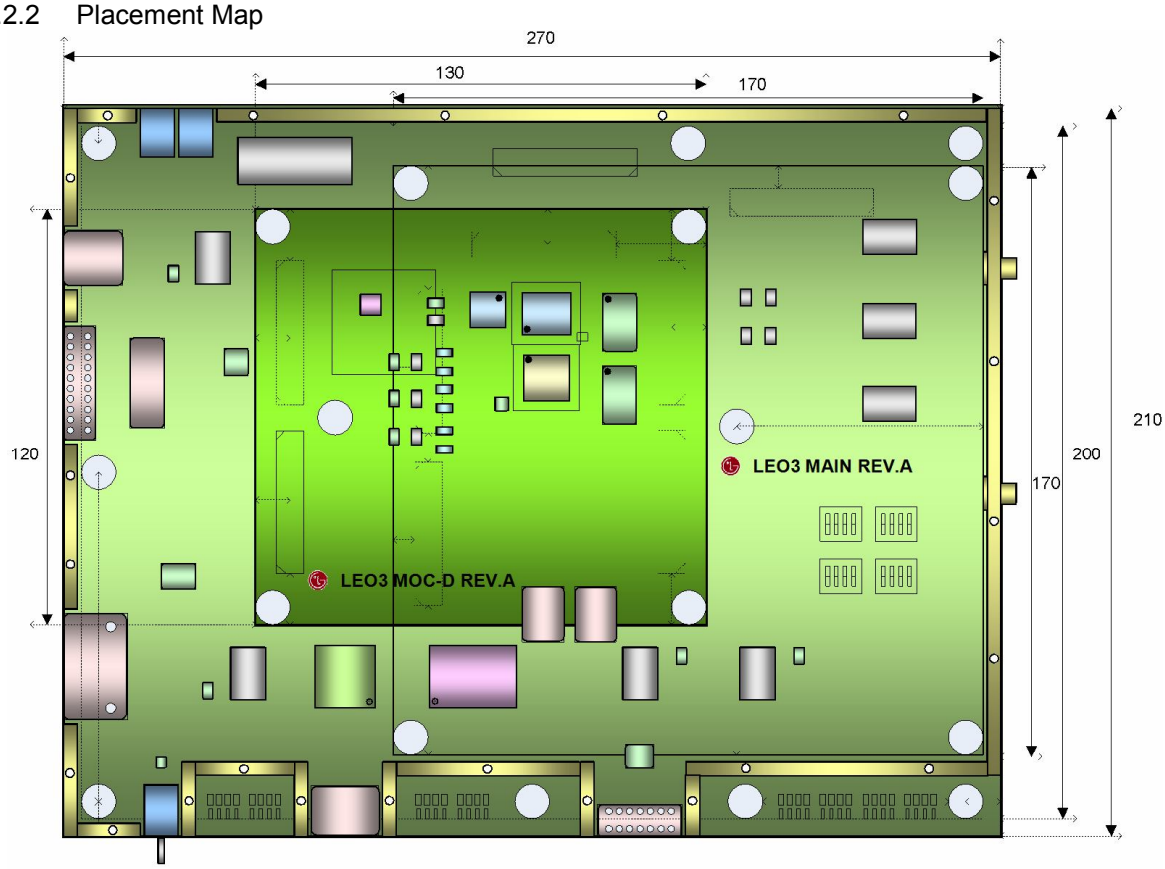


**Figure 3. LEO3 Platform Board Layout**

# 3 Power Supplies

## 3.1 Main Board Power

Main external power is supplied from DC input jack on the upper left corner of the baseband platform board. The regular input voltage is 12V. For this platform, an external power adaptor 'CLG-60-12' from Mean Well is provided with maximum current rating of 5A**.**

## 3.2 RF Board Power

The RF board power is supplied from the mian board RF connector.

The regular RF board input voltage is 6V, which is regulated from the main board power so an additional power supply for RF board is not required.

## 3.3 L1000

- Core Power - +1.2V
- Memory controller / Flash controller power - +1.8V
- I/O Power - +2.8V
- USB Power - +3.3V

## 3.4 Other Peripherals

- L1000 I/O power - +2.8V
- LVDS driver Power - +3.3V
- Reset Power - +2.8V
- SIM L/T Output Power - +1.8V / +3.0V
- Ethernet Transceiver Analog Power - +1.8V / +2.5V (only available for MDC-D core board)
- Ethernet I/O Power - +3.3V (only available for MDC-D core board)
- DSP Core Power - +1.25V (only available for MDC-D core board)
- DSP Memory Controller Power - +1.8V (only available for MDC-D core board)

# 4 Switch Setting

Configuration and control settings are done by 5-DIP switches (SW4, SW5, SW6, SW7, SW8) and 2 jumpers (J3, J4). The assignments of each signal and their descriptions are in the following tables.

| SW7 | | | |
|---|---|---|---|
| **No.** | **Name** | **Default** | **Description** |
| **1** | JTAG_CFG(0) | ON | JTAG_CFG[1:0]<br>[OFF:OFF] No JTAG<br>[OFF:ON] ARM Only<br>[ON:OFF] CC5 Only<br>[ON:ON] ARM-CC5<br>*ON: High, OFF: Low |
| **2** | JTAG_CFG(1) | OFF | |
| **3** | EPI_MODE | ON | [OFF] Dedicated Address/Data EPI I/O<br>[ON] Muxed Address/Data EPI I/O<br>*ON: HIgh, OFF: Low |
| **4** | USB_MODE | OFF | [OFF] UTMI mode<br>[ON] ULPI mode<br>*ON: High OFF: Low |
| **5** | PWR_CUT_MODE | OFF | [OFF] Power cut disable<br>[ON] Power cut enable<br>*ON: High, OFF: Low |
| **6** | REFCLK_SEL | OFF | [OFF] On-board VCTCXO 19.2MHz<br>[ON] RF board 19.2MHz<br>*ON: High, OFF: Low (Rev.A)<br>*ON: Low, OFF: High (Rev.B) |
| **7** | NAND_CFG(0) | OFF | [ON] 4byte address<br>[OFF] 5byte address<br>*ON: Low, OFF: High |
| **8** | NAND_CFG(1) | OFF | [ON] Small block (1page: 512byte + 16byte)<br>[OFF] Large block (1page 2048byte +64byte)<br>*ON: Low, OFF: High |
| **SW8** | | | |
| **No.** | **Name** | **Default** | **Description** |
| **1** | MODE(0) | ON | MODE[2:0]<br>[OFF:OFF:OFF] Undefined<br>[OFF:OFF:ON] NAND boot<br>[OFF:ON:OFF] Serial Flash boot<br>[OFF:ON:ON] EPI boot<br>[ON:OFF:OFF] SDIO boot<br>[ON:OFF:ON] USB boot<br>[ON:ON:OFF] Serial Flash boot (for debug)<br>[ON:ON:ON] Test<br>*ON: High, OFF: Low |
| **2** | MODE(1) | OFF | |
| **3** | MDOE(2) | OFF | |
| **4** | MODE(3) | OFF | [OFF] Secure Boot disable<br>[ON] Secure Boot enable<br>*ON: High OFF: Low |

**Table 1. DIP switch setting for L1000 boot configuration**

| SW6 | | | |
|---|---|---|---|
| **No.** | **Name** | **Default** | **Description** |
| **1** | IRQ(0) | OFF | [OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **2** | IRQ(1) | OFF | [OFF] High level (Rev.A), Low level (Rev.B)<br>[ON] Low level (Rev.A), High level (Rev.B)<br>*ON: High, OFF: Low (Rev.A)<br>*ON: Low, OFF: High (Rev.B) |
| **3** | IRQ(2) | OFF | [OFF] High level<br>[ON] Low level<br>*ON: Low, OFF: High |
| **4** | IRQ(3) | OFF | [OFF] High level<br>[ON] Low level<br>*ON: Low, OFF: High |

**Table 2. DIP switch setting for manual IRQ generation**

*** Caution) Please, be careful to switch 'ON" for the SW5. Switching 'ON' should be done only when the corresponding GPIO directions have defined as 'Input'. Otherwise (if defined as 'Output'), it would be possible for the L1000 to have a damage.**

| SW5 | | | |
|---|---|---|---|
| **No.** | **Name** | **Default** | **Description** |
| **1** | LED_DEBUG(0) | OFF | Corresponding to GPIO(0) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **2** | LED_DEBUG(1) | OFF | Corresponding to GPIO(1) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **3** | LED_DEBUG(2) | OFF | Corresponding to GPIO(2) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **4** | LED_DEBUG(3) | OFF | Corresponding to GPIO(3) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **5** | LED_DEBUG(4) | OFF | Corresponding to GPIO(4) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **6** | LED_DEBUG(5) | OFF | Corresponding to GPIO(5) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **7** | LED_DEBUG(6) | OFF | Corresponding to GPIO(6) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |
| **8** | LED_DEBUG(7) | OFF | Corresponding to GPIO(7) of L1000<br>[OFF] Low level<br>[ON] High level<br>*ON: High, OFF: Low |

**Table 3. DIP switch setting for LED_DEBUG**

*** SW4 is not available for MOC-D core board**

| SW4 | | | |
|---|---|---|---|
| **No.** | **Name** | **Default** | **Description** |
| **1** | D_PHYAD(1) | OFF | D_PHYAD[4:1]<br>[OFF] Ethernet PHY address value 1<br>[ON] Ethernet PHY address value 0<br>*ON: Low, OFF: High |
| **2** | D_PHYAD(2) | OFF | |
| **3** | D_PHYAD(3) | OFF | |
| **4** | D_PHYAD(4) | OFF | |
| **5** | D_ETH_MAN_MDIX | OFF | [OFF] Cross-over line mode<br>[ON] Straight lien mode<br>*ON: Low, OFF: High |
| **6** | D_ETH_MULTI_EN | ON | [OFF]: Multiple node (master)<br>[ON]: Single node (slave)<br>*ON: Low, OFF: High |
| **7** | D_ETH_MDIX_EN | OFF | [OFF]: Enable auto MDIX<br>[ON]: Disable auto MDIX (set by D_ETH_MAN_MDIX)<br>*ON: Low, OFF: High |
| **8** | DSP_PWRDOWN | OFF | [OFF]: DSP clock / reset enable<br>[ON]: DSP clock / reset disable<br>*ON: Low, OFF: High |

**Table 4. DIP switch setting for Ethernet PHY**

| Jumper No. | Name | Default | Description |
|---|---|---|---|
| **J3** | UART_CTS/<br>UART_RTS | 1-2 connection<br>3-4 connection | [1-2, 3-4] for the cross UART cable<br>[1-3, 2-4] for the straight UART cable |
| **J4** | UART_RXD/<br>UART_TXD | 1-2 connection<br>3-4 connection | [1-2, 3-4] for the cross UART cable<br>[1-3, 2-4] for the straight UART cable |

**Table 5. Jumper setting for UART signal connection**

## 5 LED Monitor

In the platform board, 15 LEDs are provided for the L1000 debug monitoring such as crash debug, timing check, interrupt flag, status of L1000 etc.

The definition of monitor is not given yet for each LED explicitly. (TBD)

The LEDs for LED_DEBUG[0:7] and the LEDs for IRQ[0:3] are located lower left-hand corner of the main board.

The LEDs for STATUS[0:2] are located lower right-hand corner of the main board.

All of them are indicated with white silkscreen printing on the main board respectively.

## 6 Image Downloading

If the other boot modes than ‘JTAG Boot’ such as ‘NAND Flash Boot’, ‘NOR Flash Boot’ are to be used, they require the related image downloading into NAND flash or NOR flash.

For further information about the image downloading including the other boot load with USB or SDIO, refer to other related documents.