Description of Functional Blocks

RBFS-C921A BT Ass'y Module

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1. RF Receiver Block

1.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-ROM WLCSP to exceed the Bluetooth requirements for co-channel and adjacent channel rejection. For EDR, an ADC is used to digitise the IF received signal.

1.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

1.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

2. RF Transmitter Block

2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm. This allows Bluetooth Main Chipset to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA. But Our Module support Class2 type

2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation or any other customer specific application.

3. RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.0 + EDR specification.

4. Power Control and Regulation

Bluetooth Module contains two linear regulators. The high-voltage regulator generates a 1.8V output which is used to power the IO circuits. A low drop out low-voltage regulator is used to generate the 1.5V core supply from the 1.8V IO supply.

5. Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency. Bluetooth Module(U1) included crystal unit.

6. USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. Bluetooth Module(U1) acts as a USB peripheral, responding to requests from a master host controller such as a PC.

7. 802.11 Co-Existence Interface

Dedicated hardware is provided to implement a variety of 802.11 (Wi-Fi) co-existence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. The details of some methods are proprietary (e.g., Intel WCS). Contact CSR for details.

8. Memory Interface

The SDRAM is a quad-bank DRAM that operates at 1.8V or 2.5V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

The Nor Flash devices are 512K x16 CMOS Multi-Purpose Flash (MPF) manufactured with high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The Flash write (Program or Erase) with a 3.0-3.6V power supply. The Flash write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pinouts for x16 memories.

9. RISC DSP Processor

This is designed as a System On a Chip : system controller and decoder controller for multi‐format digital audio player with access of various storage such as USB, SD/MMC card, NOR flash and etc. The independent dual 32‐bit RISC processors provide optimum performance and code density for the combination of control code and signal processing required for digital audio decoding, file system management and system control.

The integrates programmable and approved ARM7TDMI™ as a system controller for advanced multi‐format digital audio (MP3/WMA/Ogg) decoding, low power dedicated hardwired CDROM decoder, On‐chip SRAM and ROM, versatile audio interfaces of USB 1.1 host/device, SD/MMC card, and large number of GPIO (General Purpose Input Output) ports. In addition, SRS (WOW), MP3 encoding and WMA encoding features are available as system solutions. By utilizing advanced 0.13 micron technology.

RECORD OF CHANGES

Revision No.	Date	Description
A	Feb. 2009	Initial Release

Contact for Support

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FCC compliance Information

This device complies with part 15 of FCC Rules. Operation is subject to the following two conditions:
1. This device may not cause harmful interference received.
2. This device must accept any interference received. Including interference that may cause undesired operation.

FCC WARNING

This equipment may generate or use radio frequency energy. Changes or modifications to this equipment may cause harmful interference unless the modifications are expressly approved in the instruction manual. The user could lose the authority to operate this equipment if an unauthorized change or modification is made.

To satisfy FCC exterior labeling requirements, the following text must be placed on the exterior Of the end product.

Contains Transmitter Module FCC ID: BEJRBFS-C921A

CAUTION: This device and it's antenna(s) must not be co-located or operated in conjunction with any other antenna or transmitter. End users cannot modify this transmitter device. Any Unauthorized modification could void the user's authority to operate this device.