DTT250M – 250W Digital Television Transmitter

GENERAL DESCRIPTION

INTRODUCTION

This manual describes the LARCAN model DTT250M VHF Digital Television Transmitter.

LARCAN all-solid-state 250W VHF transmitters are designed to operate conservatively at 250W average DTV power with superb performance, reliability and operating economy.

The transmitter and exciter or translator chassis are packaged in a single 19" cabinet. The simplicity of design, the deployment of all modular and other subassemblies, and the use of standard readily available components, enhances serviceability.

Important transmitter parameters are monitored, and can be displayed on the meter built into the amplifier. Additionally, all meter readings are made available as DC signals for telemetry by remote control systems. The DTT250M, like all other LARCAN transmitting equipment, is suitable for automatic or remote-control operation.

AMPLIFIER CHAIN

The RF output of the exciter is fed to a conservatively designed broadband solid-state amplifier. This amplifier requires no tuning or adjustment within its band of operation. Simplicity of operation, reduced maintenance costs and increased reliability are a few of the major benefits derived from this modular amplifier. This module is operated well below its maximum ratings.

The amplifier chain consists of three stages of amplification.

The preamplifier stage is a high gain, broadband, thin-film integrated circuit amplifier operating class A.

The IPA stage consists of a pair of push-pull FETs in a single case, operating in class AB as a linear amplifier. This amplifier uses the identical dual FET device that is used by the PA module.

The final amplifier stage consists of six push-pull FET amplifiers that operate in class AB, in three groups of two in quadrature, and are combined in quadrature and then in a 3-way combiner. The amplifier module is rated for 250 watts average ATSC output. The module is provided with soft-start, VSWR protection, and a monitor port.

The amplifier output is fed to the bandpass filter and the directional coupler, which provides a small sample of forward and reflected output power for AGC and VSWR supervisory functions. The transmitter output then passes to the antenna system.

TRANSMITTER CONTROL

The control circuitry in this solid state transmitter is simple. Interlocking consists of the enabling circuitry necessary to ensure that any external patch panel link operation, or RF switching, can only be done with RF turned off.

All control wiring of the transmitter passes through a control circuit board (prefix 5B), and facilities are provided on this board for telemetry, status, and control connections to and from a remote control system. These are available on 15 contact D-shell connector J5.

For local operation, simply place the LOC-REM switch in the LOC position. For remote control operation the LOC-REM switch must be in the REM position. This places +12V on Remote Enable J5-5.

The Remote Enable +12V appears as an arming signal at J5-5, and the momentary connection of this +12V to J5-13 turns the transmitter ON, and momentary connection of the +12V to J5-8 turns the transmitter OFF.

The transmitter control and interlock wiring is also brought out on J3, which is provided with a terminal block style of connector interface. Remote Enable, Remote On, Remote Off, and External Interlocks 1 and 2 are all brought out on J3 for connection as required.

A thermostat is provided in the PA heatsink to open the interlock chain should an unlikely overheating condition occur.

CONTENTS

1 BANDPASS FILTER

Drawing References: Figure 1 and Figure 4.

The LARCAN bandpass filter implementation consists of a cascaded series of coupled helical resonators. A helical resonator is essentially a self supporting high Q coil (the helix) mounted inside a metallic shield enclosure. One end of the coil is solidly connected to the shield enclosure and the other end is open circuited except for a small trimmer capacitance to ground. The dimensions of the coil are critical as to frequency of operation; the assembly behaves as though it were a quarter wave coaxial transmission line resonator. Several sizes of coils and enclosures are necessary to cover the desired frequency ranges. Figure 4 indicates the generic assembly of a coupled helical resonator bandpass filter.

The referenced drawing in Figure 4 is a low band filter, but the high band unit is laid out identically and appears almost the same, except the high band helixes have fewer turns of coarser winding pitch, and their shield enclosure dimensions are somewhat smaller.

The desired response shape is presented as Figure 1, and the filter electrical equivalents are presented as Figure 2. When we examine the assembly, and take capacitances into account, the equivalent circuit of a helical resonator becomes simply a parallel resonant LC tank circuit having low (trimmer) capacitance and relatively high inductance. Adjustment of the trimmer produces a change of capacitance, and the trimmer's moveable slug is shaped to appear as a shorted turn, which alters the inductance of the helix.

Matching from and to 50 ohm transmission lines is accomplished with taps on the input and output helixes.

Coupling between sections is electrically a bridged T network of capacitors, and is made up of the small capacitance between the free ends of the coils, controllable by the amount of capacitance to ground that is introduced by the coupling adjustment screws; the coupling is maximum when the screws are backed out fully from the enclosure. Shielding partitions placed inside the enclosure between helixes, produce fixed area apertures which affect the coupling capacitance between helixes. Helix #3 in Figure 4 has taller partitions on both sides of it, giving lower capacitance and less coupling than the others.

For system use, the tuning and coupling is adjusted for a flat topped response with steep sides, and the desired shape is such that f_V - 4.5 MHz and f_V + 9.0 MHz are both 30 dB down, but the carriers must be f_V < 0.6 dB and f_A < 0.7 dB departure from flatness. Input and output return loss must be 20 dB or better over the full 6 MHz bandwidth. These sweep curves are shown below as Figure 1A.

There are nine screw adjustments and two I/O matching (with soldering iron) adjustments that need to be made simultaneously. Factory adjustment is never attempted without the aid of a network analyzer, and for this reason we say the unit is not user-adjustable.

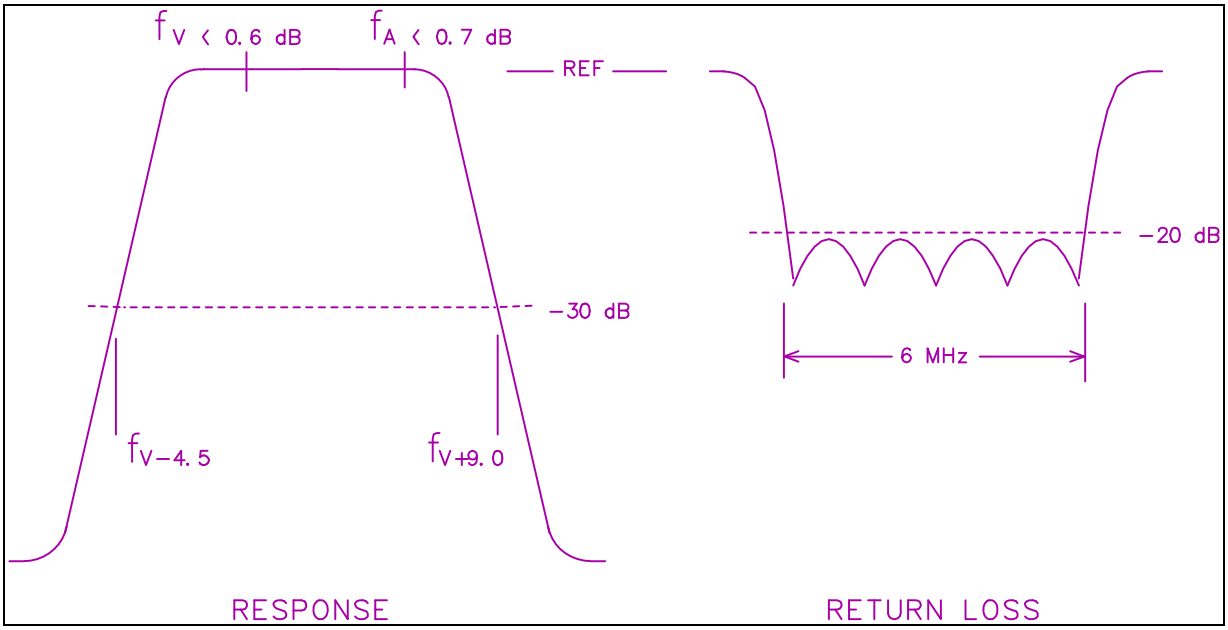

Figure 1 5-Pole Bandpass Filter Curves

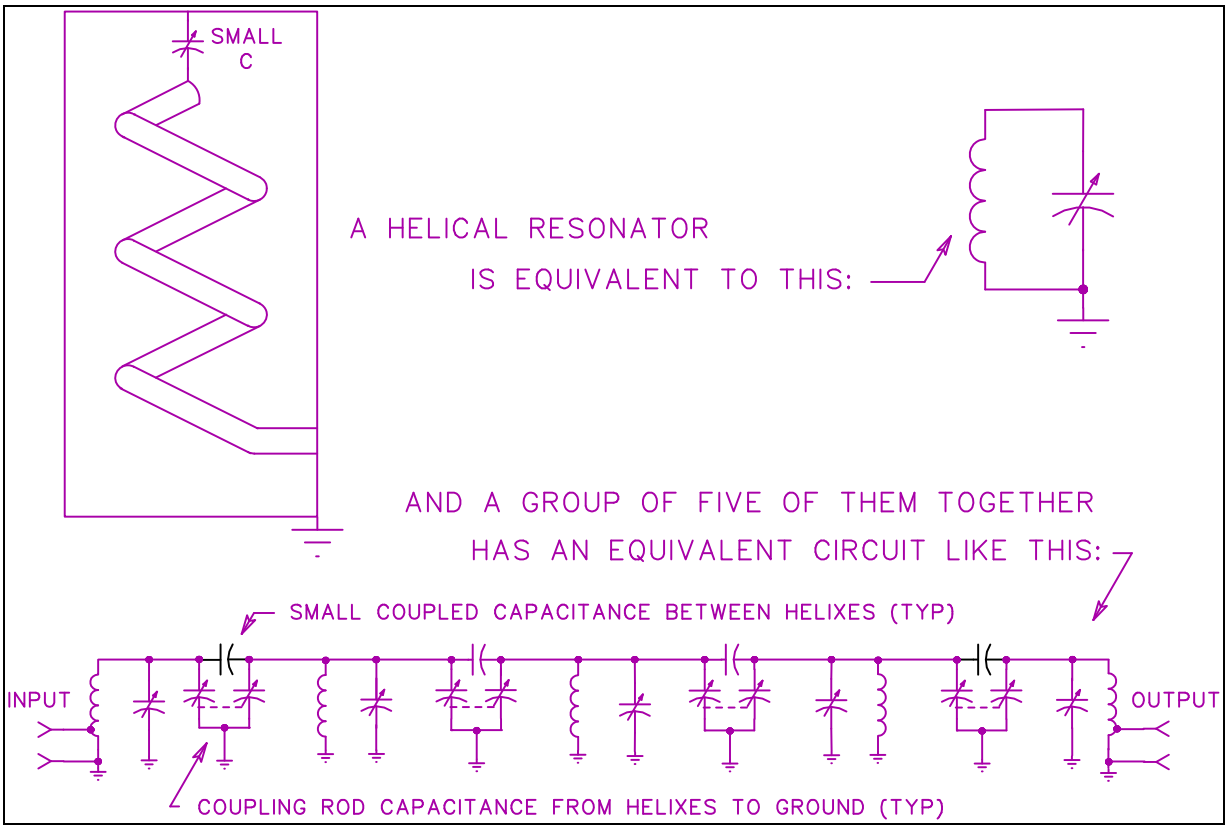

Figure 2 5-Pole Bandpass Filter Used in the TTS1000B

2 RF DIRECTIONAL COUPLER

A directional coupler is based on the principles of inductive (magnetic) coupling and capacitive coupling.

In the LARCAN quad directional coupler implementation as shown in Figure 3 (schematic equivalent) and Figure 5 (assembly), the RF to be sampled passes through a microstrip transmission line that is connected between the transmitter output filter at J3 and the antenna system at J4. The magnetic field surrounding the hot conductor of this transmission line induces a small RF current flow in other conductors situated parallel to it. One end of each sampling conductor is terminated by a resistor to ground. Sometimes small capacitors are connected across these resistors to provide a termination that remains resistive over the band. The other end of each sampling conductor connects to an external load, usually a 50 Ω input of something such as an RF detector for AGC, the station demodulator, or an RF detector for VSWR sensing.

If the sampling system as described in the forgoing paragraph were dependent only on magnetic coupling and absolutely no capacitance were present, the external loads would be driven with RF samples regardless of the direction they came from. Omnidirectionality is not wanted; our objective is that the system should be directional, that is, a signal coming from the transmitter should be seen by the "forward" ports, and a signal reflected back from the antenna should be seen by the "reflected" ports, but at the same time as little as possible of the forward signal from the transmitter should be seen on these reflected ports.

The desired directivity is achieved by the capacitance between the main line and each sampling line. The presence of this capacitance changes the relative phase of the RF signal seen in the sampling line such that *the capacitively coupled signal adds to the inductively coupled signal at the end of the line nearest the signal source, and subtracts from it at the other end, thus the sample becomes directive.*

This capacitance is trimmed by small "gimmick" capacitors designated L1 through L4. They are in reality short pieces of Teflon sleeved magnet wire which, although they may possess a fraction of a nanohenry of inductance, are mainly small capacitors which are factory adjusted by bending the wire to control the amount of coupling capacitance between the transmission line and the sampling loop concerned. The position of the capacitor along the loop does not seem to matter.

Terminations are provided at the subtractive ends of each of the four sampling lines.

In the enclosure shown in Figure 5, J3 and J4 are the filter and antenna ports respectively, and J1, J5 are "forward" samples which are maximum amplitude for signals incident on J3; while J2, J6 are "reflected" samples which are maximum amplitude for signals incident on J4.

Different coupling values are obtained from the spacing of conductors; the nearer the spacing, the greater the coupling. Coupling is also greater according to frequency, and rises at a rate of about 6dB per octave. In the boards shown in Figure 5, the J1 and J2 signals will be about 10dB greater amplitude (about 36dB below the generator level at 70 MHz on low band or 200 MHz on high band) than the signals sampled from J5 and J6 (about -46dB). Generally for system purposes the reflected signal sample to the VSWR supervisory system should be taken from the J2 connector because it has greater coupling and we need to measure a much smaller signal in a detector having finite small-signal sensitivity. System forward signals can be taken from J1 for the AGC detector, and J5 for the system monitoring demodulator.

A network analyzer and extremely accurate terminations are required for setting up the directional coupler. The adjustments are made to the trimming capacitances L1 through L4, and the capacitors in parallel with resistors R1 through R4. Our target is directivity of 30dB or better on each sampling port, and coupling (forward direction) for J1 and J2 about 36dB down, J5 and J6 about 46dB down.

No user adjustments are possible or recommended. Very little can go wrong with the directional coupler other than from the antenna being hit by lightning, and inspection is all that is recommended, nothing more.

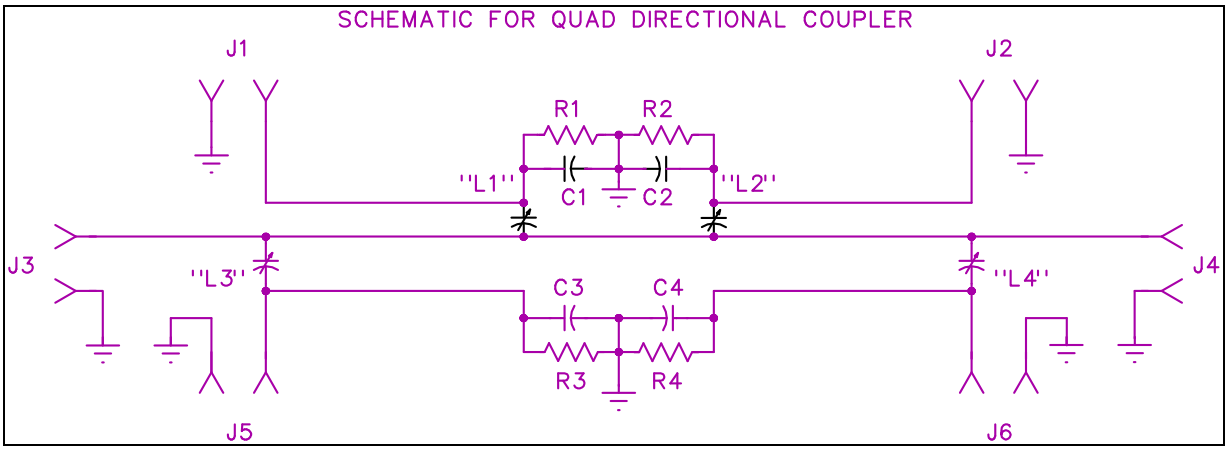

Figure 3 Quad Directional Coupler Equivalent Schematic

POWER AMPLIFIER LOW BAND

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Functional Description

The Power Amplifier module consists of a six-way power splitter, six FET amplifiers, a six-way power combiner, a VSWR protection board, and power & I/O connectors. Two full-size heatsinks provide the cooling for the active devices. It is designed for 1.5 kW sync peak power output in Low Band 54 - 88 MHz Analog television systems, and provides power gain of approximately 20 dB, with 1.5 kW peak sync visual or 900 W aural output. The module can provide upwards of 250W of average digital power when used with appropriate predistortion. It is fully hot-pluggable, incorporating protective circuitry for excess VSWR power cutback.

6-Way Splitter/Input Board

Part number: 40D1474G1/40D1474G2
References: Figure 3 and Figure 4.

The 6-Way power splitter receives its RF input signal from the drive stage and provides six input signals to integral input matching networks for the six FET amplifiers. The incoming signal is first split in three by a 3-way Wilkinson splitter, and the three resultant signals are split again by three 2-way Wilkinson splitters to provide the six outputs required. Terminations for the 3-way splitter are provided by R109, R110, and R111, with reactive trimming by L109, L110, and L111; and for the two-way splitters, terminations are R101, R103 and R105, with reactive trimming by C106, C116, and C126. Impedance match is provided by C145, C142, C138, C144, C145, C139, and C140 which make the path from the 50 Ω input to the six quarter- wave matching sections, into a low-pass π network. C148 provides input matching for the transition from the input connector to the input transmission line.

A built-in detector (CR102 and C147) is fed from a directional coupler on the input transmission line, to provide a sample of the input signal for module gain monitoring. R117 and R118 terminate the directional coupler.

FET RF Amplifiers

References: Figure 3, Figure 4, Figure 5, Figure 6.

Each of the six amplifiers in the module consists of two, source grounded N-channel, insulated gate Field Effect Transistors (FETs) packaged in a single case, operating class AB in a push-pull configuration. Because these FETs are "enhancement mode" devices, they require positive gate-to-source bias voltage on each gate to cause source-drain conduction. A quiescent Class AB idling bias current is set independently for each half. The gate voltage required to produce this idling current may vary between 2 V and 5 V according to the device specification sheet, and the idling current used. FET gate threshold voltages also are temperature sensitive, so thermal compensation is provided by R9, RT1, and R10, RT2. Bias current is set to 500mA per half of the device for analog operation and 750mA per half for digital operation.

Gate bias is supplied from an adjustable voltage divider from the +39 V regulated bias rail. Resistors R1, R2, R3, R4 provide gate bias for one half of the amplifier; R5, R6, R7, R8 provide bias for the other half.

The RF input signal is applied to balun T1 to provide two signals 180˚ out-of-phase. These signals are stepped down to match the low input impedance of the FET device through a π-network consisting of C1, C2, C3, L1, L2, C4, and the device CG-S. The gate input impedance at the operating frequency is low compared with the values of R3 and R6, which have little or no effect at RF.

R3 and R6 provide a DC path for bias, and provide loading at lower frequencies where gate impedance is high, in order to assist in maintaining amplifier stability. The choice of C6 and C7 values, and the series inductance of board traces, also ensures effective bypassing at critical frequencies of interest.

The output matching π-network, consisting of inductors L3 thru L8, and capacitances C13 thru C16, transforms the very low output impedance of the FET, to 12.5 Ω. The two antiphase output signals are finally combined in balun T2, L9. Jumpers placed across parts of L7 and L8, plus the changed values of C13, C14, C15 and C16, configures the system for channels 5 & 6 operation.

DC is applied to the FET drains through L3, L4 for the Q1A half, and L5, L6 for the Q1B half. L3 and L6 are short sections of microstrip line which transform the impedances of L4 and L5 to higher values as seen by the FET. RF and lower frequencies are bypassed with paralleled C5, C9, C10 for one half of the amplifier, and C8, C11, C12 for the other half. These groups of capacitors are selected in value and for their internal equivalent series inductances so that they will be an effective bypass at critical frequencies of interest, including video, to assist in maintaining stability.

Note that fuses are provided for the voltage supplied to the FET drain connections. The intent of these fuses is to protect the surrounding circuitry in the event of a device failure. The normal failure mode of active devices such as these is short-circuit, and the fuse will blow in this case, isolating the defective device from the rest of the module and transmitter power supply, allowing the remaining devices to keep operating normally. A blown fuse can serve as a valuable troubleshooting aid, when trying to identify failed devices.

6-Way Combiner/Output Board

Part number: 40D1472G1/40D1472G2
References: Figure 6 and Figure 3.

The six amplifier outputs are applied to three 2-way Wilkinson combiners and phase delayed to correct the quadrature condition imposed by the input splitter board. The three outputs of these Wilkinson combiners are again combined by a 3-way Wilkinson combiner into a single 50 ohm output. Terminations for the Wilkinson networks are similar to those provided on the Input board described above, and consist of R100, C105, R102, C115, R104, C125 for the 2-ways; and R106, L106, R107, L107, and R108, L108 for the 3-way combiner. An output matching π network is formed by C131 thru C134, C136, C137, and C141, along with the series inductance of the board trace.

A directional coupler feeds a BNC connector on the module front panel, and can be used for output monitoring. The bi-directional coupler provides DC samples corresponding to both forward and reflected power to the VSWR protection board for monitoring module gain and VSWR protection. Terminations for these coupler line sections are provided by R113, R114, and R115; the RF samples for VSWR monitoring are detected by CR100, C143, and R112 for "forward" and by CR101, C146, and R116 for "reflected".

VSWR Control Board

Part number: 20B1549G1
References: Figure 7 and Figure 8.

The VSWR control board performs a number of functions: it provides regulated bias voltages to the FET power amplifier stages, it provides hot-plug-in capability to protect the amplifier module when plugged into an

operating transmitter, it provides protection to the FETs against over-dissipation due to high VSWR, and it monitors the module RF power gain.

If the module is plugged into a powered transmitter using several modules running in parallel, the power supply connections are first made through the longer contacts of the module's DC power connector and into VSWR board J1 pin 8. This allows the electrolytic bypass capacitors of all amplifiers to charge through current limiting resistor R5, preventing overstress of all amplifier fuses due to charge current of the bypass capacitors. When the module is fully seated, the high current contacts are connected and the module can operate normally.

In normal operation the power supply enters J1 via pin 2, and is regulated to +39 VDC by series resistor R10 and zener diode VR1. Regulator U1 provides constant B+ voltage for op-amps U2, U3, U4, and the comparator reference voltages. When the module is first turned on (or plugged in) and U1 begins regulating, the charging current of C7 turns on Q1 which pulls the bias line low for a brief period of time. This provides a slow start for the module after DC power is applied.

The overall RF system of the transmitter provides overall VSWR protection via the external RF detector boards discussed in other sections of this manual, but VSWR sensing is also provided in the module for its own safety. In the transmitters utilising modules in parallel, one or more failed or disconnected modules or a fault in the six-way combiner or subsequent 3 dB coupler, may cause a module output mismatch.

To the module, any mismatch which appears as reflected power is detected and sensed at pin 11 of J1 to comparator circuit U2B.

R21 sets the level at which VSWR protection begins. If the level of detected reflected power on pin 5 of U2B exceeds the control voltage set on pin 6, the output on pin 7 will go high. R22, C10, and CR1 provide a fast attack, slow release control voltage to Q2 when a high VSWR condition suddenly occurs. This will turn on Q2 which turns on Q4 which quickly reduces the bias applied to the power amplifier FETs; this reduced bias also reduces their gain and therefore their RF output and keeps the amplifier at safe levels.
When a module is plugged into an operating transmitter, the slow start circuitry consisting of C7 and Q1 will initially keep the module turned off. Power from the other modules working into the combiner will enter the module and be detected by the reflected power detector. This would prevent the module from ever operating properly, unless the VSWR circuit is momentarily over-ridden.

The circuit of U4 produces a pulse approximately 2 seconds after power is applied to the module. At power-up, pin 2 of U4 will be pulled high by C11. R26 charges this capacitor, and when the pin 2 voltage goes below the voltage on pin 3, the output of U4 will go high. A pulse whose duration is controlled by C9 and R18 will then be applied to pin 3 of U2A. U3B detects that the module is not producing forward power and that the reverse power is high. Under these conditions the output of U2A goes high, turning on Q3, momentarily disabling VSWR protection, and allowing the module to come on.

DC samples corresponding to forward power into and out of the module are applied to U3A pins 2 and 3 respectively. When pin 3 voltage is higher than that of pin 2, corresponding to "RF gain is okay" the comparator output U3A pin 1 is high, causing the green LED on the front panel of the module to light. The comparison threshold (ie. module gain is ok) is set by adjustment of R4.

Adjustment of bias voltage to establish proper quiescent FET bias current

Important: 50 Ω input and output terminations are necessary to achieve consistent results and prevent damage to the devices when testing modules. Supplemental cooling is not required when performing bias adjustments or low power sweep of the PA modules.

POWER AMPLIFIER LOW BAND

- Remove all fuses from the module to be tested. (There are 12 fuses in total).
- Adjust all bias pots to maximum resistance, for minimum bias voltage. (Again, there are 12).
- Use a clip lead to short the junction of C7, R6, R7 and R10 to ground. This shuts off side B of the amplifier so it will not interfere with measurement of bias current from side A.
- Terminate the RF input and output into a 50 Ω load.
- Apply +50VDC from the front panel test point on the transmitter, through an ammeter, to the positive copper bus bar, and its negative to chassis. Caution: Observe polarity!
- Check the voltage on the bias terminals, it should be 39 V ±2 V. (The bias terminals are connected together via insulated bus wire).
- Read the current drawn by the VSWR board and bias regulator. Next, install a fuse in side A (nearest the panel) of amplifier #1; adjust the corresponding bias pot for a 500 mA increase in the power supply current; this increase corresponds to an idling bias current of 0.5 A (750mA for digital operation). Remove the fuse. Remove the side B bias short and place it on side A at the junction of C6, R2, R3 and R9. Place the fuse in side B. Adjust the side B bias pot for the proper current.
- Move the fuse to the remaining fuse holders, one at a time, and adjust each companion bias potentiometer in the same manner for the proper bias current.
- Install remaining fuses and remove the bias short after all bias adjustments have been made.

Low power sweep of amplifiers

Note: Low power sweep of PA modules should not be required under normal circumstances – even when replacing FET devices. There are no tuning adjustments on these modules.

- Ensure that terminations are in place in the test setup. All modules require 50 Ω source and load impedances to prevent damage and for consistent results during testing.
- Connect the module to a sweep system, typically as shown in Figure 1. The sweep generator should be adjusted to give a linear sweep from about 45 to 75 MHz, or from 65 to 95 MHz, to sweep the part of Low Band that the module is intended for, with a small amount of out-of-band signal on both ends. Ensure that a coaxial 20 dB attenuator pad is connected to the RF output of the amplifier, in order to prevent possible damage to the sweep comparator.
- Connect the lab power supply +50 V to the positive supply bus bar, and the negative to the chassis of the amplifier. The current should be limited to 7 or 8 A for this test. Caution: observe polarity!
- With the power supply switched on, the current drawn should be not more than the bias current for all the devices together - about 6 amperes (12 x 0.5 A) for the PA module.
- The swept in-band frequency response, for Low Band modules, should be essentially flat within ±1 dB as shown in Figure 1, with gain approximately 20 ±1 dB.

POWER AMPLIFIER LOW BAND

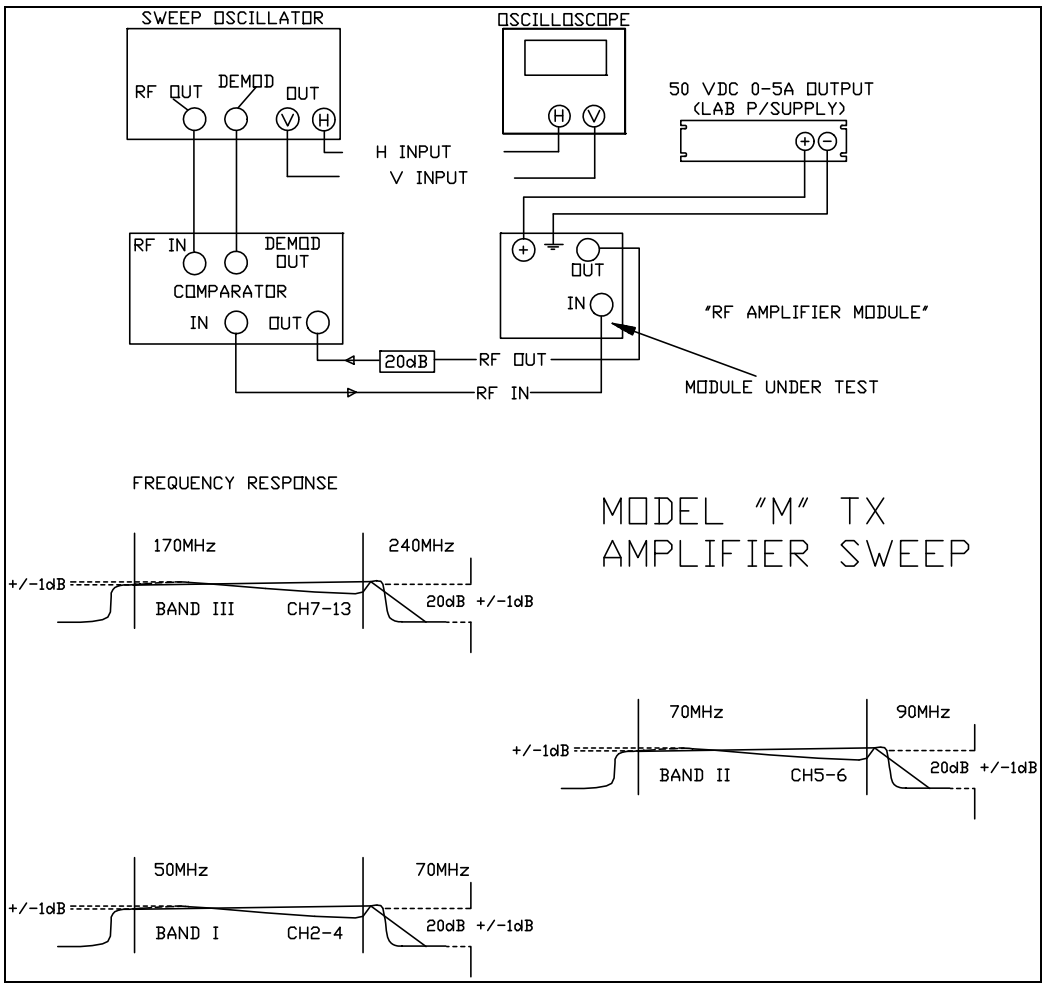


Figure 1 Module sweep Setup

Green LED Sensitivity Adjustment

One of the functions of the VSWR board is to monitor the overall gain of the PA module. This VSWR board is located at the rear of the module, adjacent to the output RF connector. For the locations of the components on the board, please refer to Figure 7.

Verify that all the PA modules are in good working order, and then proceed as follows:

- With all modules running at normal operating power, place AGC/MANUAL switch into the MANUAL position and adjust the exciter output power until the transmitter output power reads 110%.
- Remove the module to be set up, and remove the two front fuses from it, in order to simulate a single FET package failure. Replace this "crippled" module in the transmitter, and apply a nominal 50% APL staircase video signal to the transmitter (analog transmitters).
- The green LED should now be extinguished; if it is not, remove the module and adjust potentiometer (R4) on the VSWR board clockwise, replace the module and try again, repeating until the LED is barely extinguished when the module is re-powered.
- Replace the fuses so the module is again fully operational, and verify that the green LED is now fully lighted when the module is replaced in the transmitter and re-powered.

  - It is recommended that R4 be adjusted one half turn at a time, to establish a known reference point.
- Place the AGC/MANUAL switch in the AGC position, and with the RAISE/LOWER switch, readjust the transmitter output power to 100%.
- Similarly, the aural amplifier may be adjusted in the same manner, but being an FM signal the modulation of the carrier is not critical.

POWER AMPLIFIER 1.5KW HIGH BAND 40D1493G3

CONTENTS

Functional Description

Drawing references: Figure 2 through Figure 7

The Power Amplifier module consists of a six-way power splitter, six 250 W FET amplifiers, a six-way power combiner, a VSWR protection board, and power & I/O connectors. Two full-size heatsinks provide the cooling for the active devices. It is designed for 1.5 kW sync peak power output in High Band 174 - 230 MHz Analog television systems, and provides power gain of approximately 15 - 16 dB, with 1.5 kW peak sync visual or 900 W aural output. The module can provide upwards of 250W of average digital power when used with appropriate predistortion. It is fully hot-pluggable, incorporating protective circuitry for excess VSWR power cutback.

6-Way Splitter/Input Board

Part number: 40D1496G1
Drawing References: Figure 3 and Figure 4

The Six-Way power splitter receives its RF input signal from the drive stage and provides six input signals to integral input matching networks for the six FET amplifiers. The incoming signal is first split in three by a three-way Wilkinson splitter and the three resultant signals are split again by three two-way Wilkinson splitters to provide the six outputs required. Terminations for the three-way splitter are provided by R109, R110, and R111, and for the two-way splitters, terminations are R101, R103 and R105. C115 provides input matching for the transition from the input connector to the input transmission line.

A built-in detector (CR102 and C147) is fed from a directional coupler on the input transmission line, to provide a sample of the input signal for module gain monitoring. R113 and R117 terminate the directional coupler,

FET RF Amplifiers

Drawing References: Figure 3 through Figure 6

Each of the six amplifiers in the module consists of two, source grounded N-channel, insulated gate Field Effect Transistors (FETs) packaged in a single case, operating class AB in a push-pull configuration. Because these FETs are "enhancement mode" devices, they require positive gate-to-source bias voltage on each gate to cause source-drain conduction. A quiescent Class AB idling bias current is set independently for each half. The gate voltage required to produce this idling current may vary between 2 V and 5 V according to the device specification sheet, and the idling current used. FET gate threshold voltages also are temperature sensitive, so thermal compensation is provided by R9, RT1, and R10, RT2. Bias current is set to 500mA per half of the device for analog operation and 750mA per half for digital operation.

Gate bias is supplied from an adjustable voltage divider from the +39 V regulated bias rail. Resistors R1, R2, R3, R4 provide gate bias for one half of the amplifier; R5, R6, R7, R8 provide bias for the other half.

The input RF is applied to balun T1/L1 to provide two signal outputs 180˚ out of phase. These signals are stepped down to match the low input impedance of the device through a dual section, twin π network consisting of C1, C2, L2, L3, C7, and the device CG-S. The gate impedance at the operating frequency is much lower than R3 and R6, so these resistors have no effect at RF.

R3 and R6 provide a DC path for bias, and provide loading at lower frequencies in order to assist in maintaining amplifier stability. The choice of C4 and C5 values, and their internal equivalent series inductances, also ensures effective bypassing at all frequencies.

The output matching π network, consisting of inductors L5 through L10, and capacitances C12 through C16, tunes out the FET drain capacitance and transforms the very low output impedance of the FET to 12.5 ohms. The two 180˚ antiphase output signals are combined in balun T2, L11.

DC is applied to the drains through L4, L5 for the "A" half, and L6, L7 for the "B" half. L5 and L6 are also short sections of microstrip transmission line which transform the apparent RF impedances of L4 and L7 to higher values as seen by the FET. RF and lower frequencies are bypassed with C3, C8, C9, C6, C10, C11.

These groups of capacitors are selected in value and for their internal equivalent series inductances so that they will be an effective bypass at all frequencies of interest including video, to assist in maintaining stability. Towards this objective of stability, in addition to resonating with the device drain-to-drain capacitance at RF, inductor L9 places a heavy load on the FET output at low frequencies, where it behaves as a dead short.

Note that fuses are provided for the voltage supplied to the FET drain connections. The intent of these fuses is to protect the surrounding circuitry in the event of a device failure. The normal failure mode of active devices such as these is short-circuit, and the fuse will blow in this case, isolating the defective device from the rest of the module and transmitter power supply, allowing the remaining devices to keep operating normally. A blown fuse can serve as a valuable troubleshooting aid, when trying to identify failed devices.

6-Way Combiner/Output Board

Part number: 40D1468G1
Drawing References: Figure 3 and Figure 6

The six amplifier outputs are applied to three two-way Wilkinson combiners and phase delayed to correct the quadrature condition imposed by the input splitter board. The three outputs of these Wilkinson combiners are then combined by a three-way Wilkinson combiner into one 50 ohm, output. Terminations for the Wilkinson networks consist of R100, R102, and R104 for the three two-way; and R106, R107, R108 for the three-way combiner, which also requires reactive trimming from L100 thru L102 in order that the matching network can accommodate the bandwidth from channel 7 through 13.

A directional coupler feeds a BNC connector on the module front panel and can be used for output monitoring. The bi-directional coupler provides DC samples proportional to forward and reflected power to the VSWR protection board for monitoring module gain and VSWR protection. Terminations for these coupler line sections are provided by R114, R115, and R118; the RF samples for VSWR monitoring are detected by CR100, C112, and R112 for "forward" and by CR101, C113, and R116 for the "reflected" direction.

VSWR Control Board G1

Part number: 20B1549G1
Refs: 20B1594 & 30C1418 (Figure 6).

The VSWR control board performs a number of functions: it provides regulated bias voltages to the FET power amplifier stages, it provides hot-plug-in capability to protect the amplifier module when plugged into an

operating transmitter, it provides protection to the FETs against over-dissipation due to high VSWR, and it monitors the module RF power gain.

If the module is plugged into a powered transmitter using several modules running in parallel, the power supply connections are first made through the longer contacts of the module's DC power connector and into VSWR board J1 pin 8. This allows the electrolytic bypass capacitors of all amplifiers to charge through current limiting resistor R5, preventing overstress of all amplifier fuses due to charge current of the bypass capacitors. When the module is fully seated, the high current contacts are connected and the module can operate normally.

In normal operation the power supply enters J1 via pin 2, and is regulated to +39 VDC by series resistor R10 and zener diode VR1. Regulator U1 provides constant B+ voltage for op-amps U2, U3, U4, and the comparator reference voltages. When the module is first turned on (or plugged in) and U1 begins regulating, the charging current of C7 turns on Q1 which pulls the bias line low for a brief period of time. This provides a slow start for the module after DC power is applied.

The overall RF system of the transmitter provides overall VSWR protection via the external RF detector boards discussed in other sections of this manual, but VSWR sensing is also provided in the module for its own safety.

In the transmitters utilising modules in parallel, one or more failed or disconnected modules or a fault in the six-way combiner or subsequent 3 dB coupler, may cause a module output mismatch.

To the module, any mismatch which appears as reflected power is detected and sensed at pin 11 of J1 to comparator circuit U2B.

R21 sets the level at which VSWR protection begins. If the level of detected reflected power on pin 5 of U2B exceeds the control voltage set on pin 6, the output on pin 7 will go high. R22, C10, and CR1 provide a fast attack, slow release control voltage to Q2 when a high VSWR condition suddenly occurs. This will turn on Q2 which turns on Q4 which quickly reduces the bias applied to the power amplifier FETs; this reduced bias also reduces their gain and therefore their RF output and keeps the amplifier at safe levels.

When a module is plugged into an operating transmitter, the slow start circuitry consisting of C7 and Q1 will initially keep the module turned off. Power from the other modules working into the combiner will enter the module and be detected by the reflected power detector. This would prevent the module from ever operating properly, unless the VSWR circuit is momentarily over-ridden.

The circuit of U4 produces a pulse approximately 2 seconds after power is applied to the module. At power-up, pin 2 of U4 will be pulled high by C11. R26 charges this capacitor, and when the pin 2 voltage goes below the voltage on pin 3, the output of U4 will go high. A pulse whose duration is controlled by C9 and R18 will then be applied to pin 3 of U2A. U3B detects that the module is not producing forward power and that the reverse power is high. Under these conditions the output of U2A goes high, turning on Q3, momentarily disabling VSWR protection, and allowing the module to come on.

DC samples corresponding to forward power into and out of the module are applied to U3A pins 2 and 3 respectively. When pin 3 voltage is higher than that of pin 2, corresponding to "RF gain is okay" the comparator output U3A pin 1 is high, causing the green LED on the front panel of the module to light. The comparison threshold (ie. module gain is ok) is set by adjustment of R4.

POWER AMPLIFIER 1.5KW HIGH BAND 40D1493G3

Adjustment of bias voltage to establish proper quiescent FET bias current

Important: 50 Ω input and output terminations are necessary to achieve consistent results and prevent damage to the devices when testing modules. Supplemental cooling is not required when performing bias adjustments or low power sweep of the PA modules.

- Remove all fuses from the module to be tested. (There are 12 fuses in total).
- Adjust all bias pots to maximum resistance, for minimum bias voltage. (Again, there are 12).
- Use a clip lead to short the junction of C5, R6, and R7 to ground. This shuts off side B of the amplifier so it will not interfere (through L9) with measurement of quiescent current from side A.
- Terminate the RF input and output into a 50 Ω load.
- Apply +50VDC from the front panel test point on the transmitter, through an ammeter, to the positive copper bus bar, and its negative to chassis. Caution: Observe polarity!
- Check the voltage on the bias terminals, it should be 39 V ±2 V. (The bias terminals are connected together via insulated bus wire).
- Read the current drawn by the VSWR board and bias regulator. Next, install a fuse in side A (nearest the panel) of amplifier #1; adjust the corresponding bias pot for a 500 mA increase in the power supply current; this increase corresponds to an idling bias current of 0.5 A (750mA for digital operation). Remove the fuse. Remove the side B bias short and place it on side A at the junction of C6, R2, R3 and R9. Place the fuse in side B. Adjust the side B bias pot for the proper current.
- Move the fuse to the remaining fuse holders, one at a time, and adjust each companion bias potentiometer in the same manner for the proper bias current.
- Install remaining fuses and remove the bias short after all bias adjustments have been made.

Low power sweep of amplifiers

Note: Low power sweep of PA modules should not be required under normal circumstances – even when replacing FET devices. There are no tuning adjustments on these modules.

- Ensure that terminations are in place in the test setup. All modules require 50 Ω source and load impedances to prevent damage and for consistent results during testing.
- Connect the module to a sweep system, typically as shown in Figure 1. The sweep generator should be adjusted to give a linear sweep from 160 to 240 MHz so that all of High Band or Band III is swept, with a small amount of out-of-band signal on both ends.
- Connect the lab power supply +50 V to the positive supply bus bar, and the negative to the chassis of the amplifier. The current should be limited to 7 or 8 A for this test. Caution: observe polarity!
- With the power supply switched on, the current drawn should be not more than the bias current for all the devices together - about 6 amperes (12 x 0.5 A) for the PA module.
- The swept in-band frequency response, for High Band modules, should be essentially flat within ±1 dB as shown in Figure 1, with gain approximately 15 to 16dB.

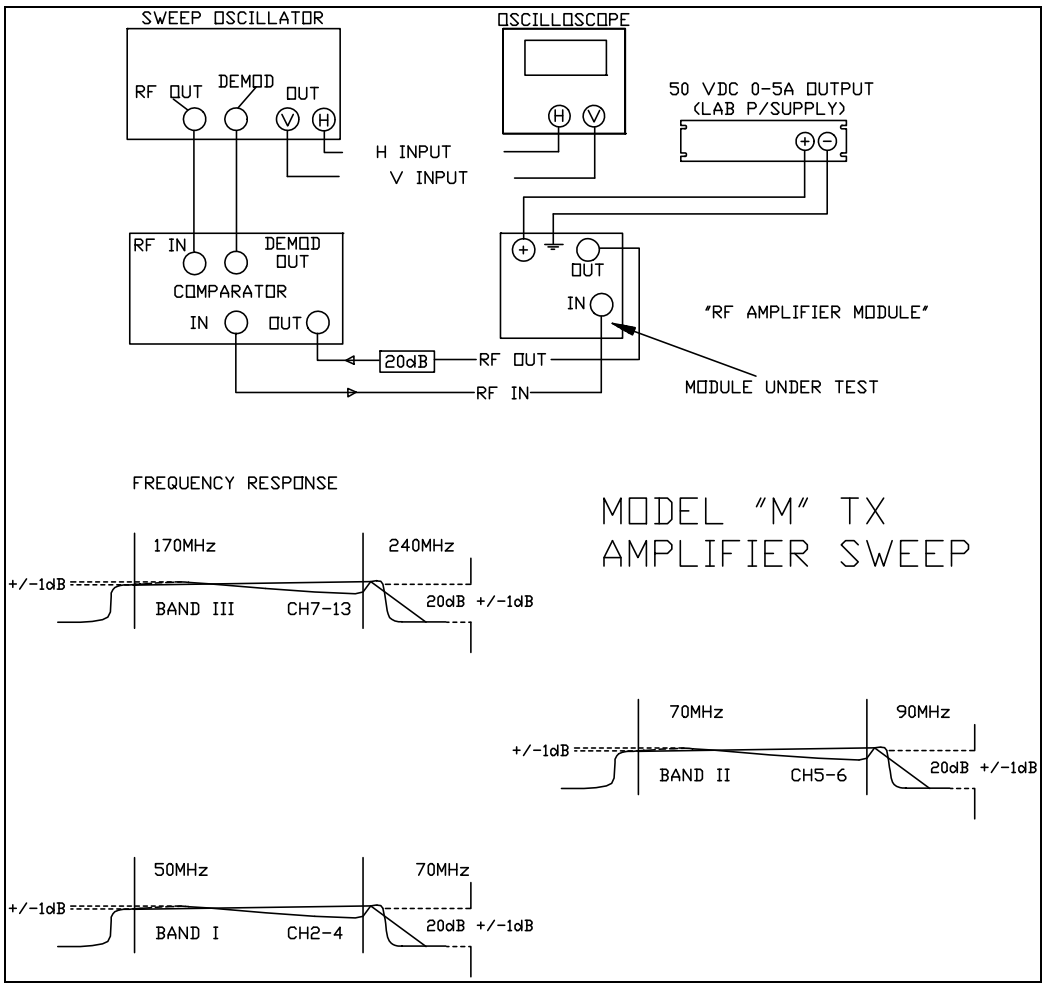


Figure 1 Module Sweep Setup

Green LED Sensitivity Adjustment

One of the functions of the VSWR board is to monitor the overall gain of the PA module. This VSWR board is located at the rear of the module, adjacent to the output RF connector.

Verify that all the PA modules are in good working order, and then proceed as follows:

- With all modules running at normal operating power, place AGC/MANUAL switch into the MANUAL position and adjust the exciter output power until the transmitter output power reads 110%.
- Remove the module to be set up, and remove the two front fuses from it, in order to simulate a single FET package failure. Replace this "crippled" module in the transmitter, and apply a nominal 50% APL staircase video signal to the transmitter (analog transmitters).
- The green LED should now be extinguished; if it is not, remove the module and adjust potentiometer (R4) on the VSWR board clockwise, replace the module and try again, repeating until the LED is barely extinguished when the module is re-powered.
- Replace the fuses so the module is again fully operational, and verify that the green LED is now fully lighted when the module is replaced in the transmitter and re-powered.

  - It is recommended that R4 be adjusted one half turn at a time, to establish a known reference point.
- Place the AGC/MANUAL switch in the AGC position, and with the RAISE/LOWER switch, readjust the transmitter output power to 100%.
- Similarly, the aural amplifier may be adjusted in the same manner, but being an FM signal the modulation of the carrier is not critical.

Intermediate Power Amplifier

30C1892G1 - G2 - G3:
Figures 1, 2, and 7.

The 30C1892 Intermediate Power Amplifier basically consists of a fan-cooled heatsink and three circuit boards. These boards are the Preamplifier board, the Amplifier Input board, and the Amplifier Output board. This subassembly is equipped with shielding covers and is mounted on a standard 19" panel. Figure 1 shows the basic construction of the IPA assembly, although the drawing was originally made for a system using an additional AGC module shown as item 50 on the drawing. AGC in the TTS1000B transmitter is implemented in the exciter instead, so item 50 is not used and non-existent in the present system.

A directional coupler (shown in Figure 12) is also mounted on the panel and provides a metering DC signal corresponding to the output RF from the Intermediate Power Amplifier.

Figures 2 and 7 for Low Band and High Band respectively, illustrate the arrangement of boards on the amplifier heatsink. Drawing 30C1474 is for our 250 watt RF power amplifier, derated for IPA service.

Cooling for the IPA heatsink is provided by a small (approx 100 cfm) axial flow Rotron™ fan which is mounted on a bracket situated so that the fan blows air on the finned portion of the heatsink.

RF Preamplifier

10A1453G2 (Low Band) and 10A1453G3 (High Band):
Figures 3 and 8.

This preamplifier design originally was used in the two IPAs of the aural/sound section of a dual RF chain transmitter which operates two single RF chains in quadrature and therefore requires phase and gain control of the input to each chain. It therefore has components in place for adjustment of RF gain and phase to enable setting up these paralleled transmitters. In a single chain transmitter such as the TTS1000B, no requirement exists for control of RF phase nor consequently its components, but our design standardization results in lower overall expense being incurred by simply leaving the components on the PC board.

The following discussion deals with the phasing components because they are a part of the signal path through the preamplifier, but functionally they are inconsequential except for technical interest.

The RF input signal from the exciter is fed via J1 into a quadrature hybrid U1 configured as a phase shifter, which is able to produce a phase shift in excess of 90° between its pin 1 (input) and pin 6 (output). A valuable property of a quadrature hybrid network connected as shown in Figures 3 and 8, is that it can introduce a variable phase delay that depends on the value of capacitance at its 0° and 90° ports. These ports (U1 pins 2 and 5) each see a pair of variable capacitance diodes CR1, CR2 and CR3, CR4. The capacitance of these diodes depends on the amount of reverse bias voltage applied to them from the arm of R2. In all transmitters, R2 is adjustable from the front panel and is marked PHASE.

In the Low Band unit, the output of the hybrid is then fed via an attenuator R5 (marked GAIN) to amplifier U2 which is output to terminal J2. C12 and the lead inductance of U2 perform output matching to 50 Ω. The gain of U2 is spec'd as 18 dB and there are a few dB of losses, so the effective gain of the Low Band preamp board is about 12 to 14 dB when R5 is turned up to its maximum output position.

In the High Band unit, the output of the hybrid is also fed via an attenuator R5 (GAIN) but this time to an additional preamplifier stage U4, whose output appears at the input of U2, which feeds terminal J2. The spec'd gain of type MWA330 in the U4 position is 6 dB, and type MHW6185 or CA2885 (U2) is 18 dB. A few dB of losses exist on the board, so the effective gain of the High Band preamp board 10A1453G3 with R5 at maximum is about 18 to 20 dB. (High Band preamps 10A1453G1 in higher powered externally diplexed transmitter aural service, use a type MWA130 as U4. Specified gain is about 12 dB, but substitution of U4 in the internally diplexed systems is not recommended due to overall linearity considerations).

At the output of U2, a match to 50 Ω is provided by C12 and the device lead inductance, which together create a matching network in boards where a type CA2885 device is used; conversely a type MHW6185 device will drive 50 Ω directly therefore no special output matching is necessary, and C12 is not present.

Most LARCAN exciters produce their best linearity at or near their maximum rated output levels, and often the overall system gain is sufficient to result in overdrive of later stages of the transmitter. The transmitter or translator lineup may therefore include an in-line attenuator in the RF chain ahead of the IPA module, in order to prevent overdrive from certain models of exciter-modulator.

U3 is a voltage regulator providing B+ to the amplifier, and biasing for the varactor diodes.

RF isolation is provided by inductors L1 and L2 while capacitors C1 and C2 act as DC blockers.

SRF 3943-2 Intermediate Power Amplifier:

Figures 4, 5, 6, 9, 10, and 11.

The Intermediate Power Amplifier (IPA) in both the Low Band and High Band versions, is configured in push-pull, using dual N-channel enhancement mode Field Effect RF power transistors which are operated in class AB. The IPA circuit is very similar to the circuit of a single amplifier of the 1.5 kW PA module described in another Section of this manual.

The Low Band and High Band versions of the IPA differ slightly due to the frequency ranges to be covered.

Low Band IPA Circuit Description

The IPA consists of two, source grounded N-channel, insulated gate Field Effect Transistors (FETs) packaged in a single case, operating class AB in a push-pull configuration. The original schematic indicates a type MRF-151-G as the dual FET used; actually we now use a "selected MRF-151-G to tightly controlled specifications" which is proprietary to LARCAN and designated type SRF 3943-2. The

MRF-151-G could be used as a replacement in case of dire emergency, but there are no guarantees as to its performance.

Because these FETs are "enhancement mode N-channel" devices, they require positive gate-to-source bias voltage on each gate to cause source-drain conduction. The quiescent Class AB idling bias current is set at 0.6 ampere for each half. The gate voltage required to produce this idling current may vary between 2 V and 5 V according to the device specification sheet, and typically is 3 to 4 V. FET gate threshold voltages also are temperature sensitive, so thermal compensation is provided by RT1 and RT2.

Gate bias is supplied out of adjustable voltage dividers from +20 V regulated bias sources CR1 and CR2. Current limiting to these zener diodes is provided through R1 and R8. Resistors R9, R2, R3, R4, and RT1 provide gate bias for the "A" half of the amplifier; R10, R7, R6, R5, and RT2 provide bias for the "B" half.

The RF input signal arriving in J1 is applied to balun T1 to provide two signals 180° out-of-phase. These antiphase signals are stepped down to match the low input impedance of the FET through a π-network consisting of C1, C2, C3, L1, L2, C4, and the device input capacitance, and then applied to the gates. The capacitance value of C4 is changed for operation on channels 5 & 6. The gate input impedance at the operating frequency is low compared with the values of R3 and R6, which have little or no effect at RF.

R3 and R6 provide a DC path for bias, and provide loading at lower frequencies where gate impedance is high, in order to assist in maintaining amplifier stability. The choice of C6, C7, C20, and C21 values, their series inductances, and that of board traces, also ensures effective bypassing at critical frequencies.

The output matching π-network, consisting of inductors L3 thru L8, and capacitances C13 thru C16, transforms the very low output impedance of the FET, upwards to a standard 50 Ω. The two antiphase output signals are finally combined in balun T2, L9. Jumpers placed across parts of L7 and L8, plus the changed values of C13, C14, C15 and C16, configures the system for channels 5 & 6 operation.

DC is applied to the FET drains through L3, L4 for the Q1A half, and L5, L6 for the Q1B half. L3 and L6 are short sections of microstrip line which transform the apparent RF impedances of L4 and L5 to higher values as seen by the FET. RF and lower frequencies are bypassed with paralleled C9, C10, and C17 for the "A" half of the amplifier, and C11, C12, and C18 for the "B" half. These groups of capacitors are selected in value and for their internal equivalent series inductances so that they will be an effective bypass at critical frequencies of interest, including video, to assist in maintaining stability. The connections for C20 and C21 also assist in stability due to their return paths through the ground plane of the output board. This connection provides a small amount of negative feedback as a primitive means of neutralizing the amplifier.

The RF output leaves the board from J2.

LB IPA Setup Procedures

1.Set up a 50 V power supply, current limited to a little more than 1.2 amps.

2.Turn both bias potentiometers to their maximum resistance position. Remove both fuses.

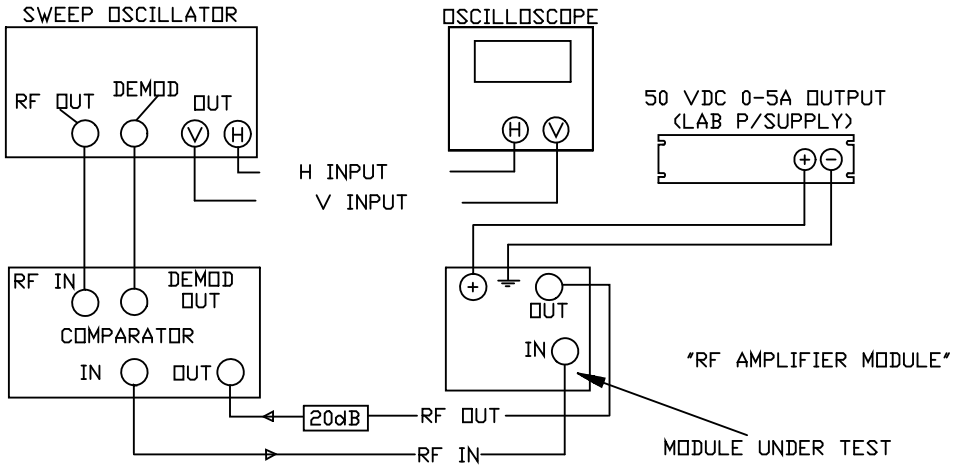
3. SRF 3943-2 Intermediate Power Amplifier: LB Setup, continued.

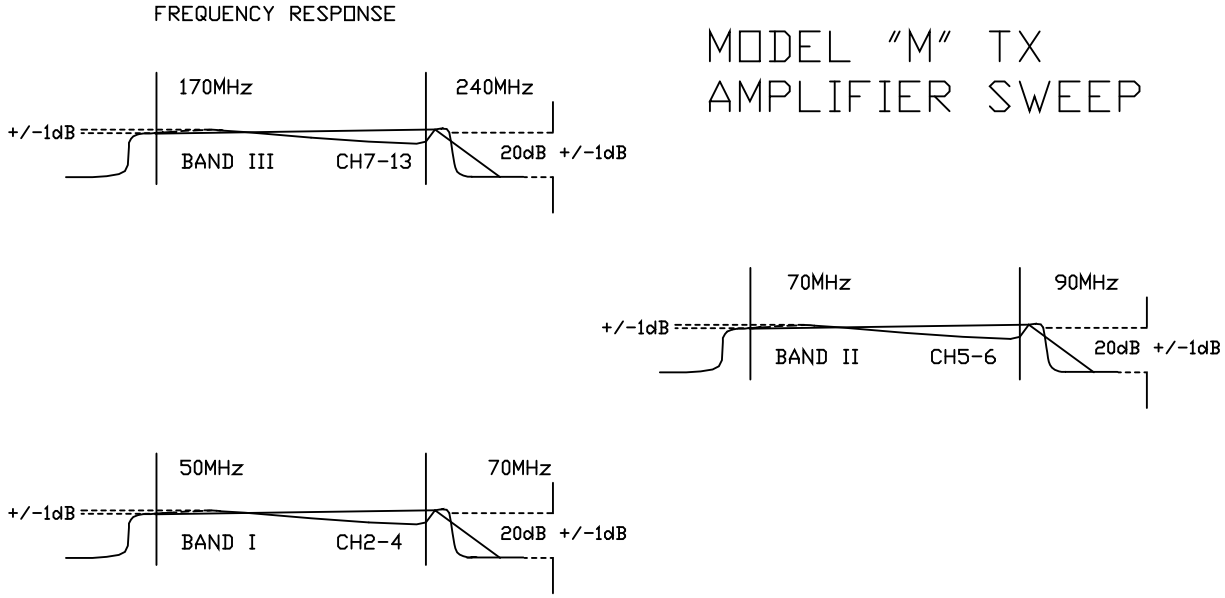
3.Apply the 50 V supply to one transistor at a time (one half package) and adjust the corresponding bias resistor for 600 mA drain current. These settings are a starting value, which will be readjusted during system test, for minimum intermods and FM noise.

4.Connect a 30 dB, 20 W attenuator to the output of the amplifier. This will absorb amplifier output and protect the sweep detector. Use it instead of the 20 dB pad shown in the diagram below.

5.Reinstall fuses and apply B+ to both supply connections of the amplifier module.

6.Apply a low level sweep to the amplifier and measure the DC input current (not more than 1.2 amps) and gain. Gain of the amplifier alone should be about 20 to 24 dB, and with the preamp (R5 at maximum) the combined gain should be between 32 and 38 dB. Flatness over the band should be better than 1 dB, as shown in the following diagram. Curves for chs 2-4 and 5,6 are correct:





1 Sweep setup and response for IPA alone, without preamp.

High Band IPA Circuit Description

The IPA consists of two, source grounded N-channel, insulated gate Field Effect Transistors (FETs) packaged in a single case, and operating in a push-pull configuration in class AB. These N-channel FETs are "enhancement mode" devices, so require a positive gate-to-source bias voltage on each gate to cause source-drain conduction. Quiescent Class AB idling bias current is set at 0.6 ampere for each half.

The gate voltage required to produce this idling current may vary between 2 and 5 V due to variances among FETs, and typically is 3 to 4 V. Gate voltages also are temperature sensitive, so temperature compensation is provided by RT1 and RT2.

Gate bias is supplied out of adjustable voltage dividers from +20 V regulated bias sources CR1 and CR2. Current limiting to these zener diodes is provided through R2 and R8. Resistors R9, R1, R3, R4, and RT1 provide gate bias for the "A" half of the amplifier; R10, R7, R5, R6, and RT2 provide bias for the "B" half.

The input RF arriving in J1 is applied to balun T1, L1 to provide two signal outputs 180° out of phase. These signals are stepped down to match the low input impedance of the device through a dual section, twin π network consisting of C1, C2, L2, L3, C3, and the device input capacitance, and then applied to the gates. The gate impedance at the operating frequency is much lower than R3 and R5, so these resistors have little or no effect at RF.

R3 and R5 provide a DC path for bias, and provide loading at lower frequencies in order to assist in maintaining amplifier stability. The choice of C2 and C6 values, and their internal equivalent series inductances, also ensures effective bypassing at critical frequencies.

The output matching π network, consisting of inductors L5 thru L10, and capacitances C12 thru C16, tunes out the FET drain capacitance and transforms the very low output impedance of the FET, upwards to a standard 50 ohms. The two 180° antiphase output signals are finally combined in balun T2, L11.

DC is applied to the drains through L4, L5 for the "A" half, and L6, L7 for the "B" half. L5 and L6 are also short sections of microstrip transmission line which transform the apparent RF impedances of L4 and L7 to higher values seen by the FET. RF and lower frequencies are bypassed with C1, C10, C11, and C8, C9, C7.

These groups of capacitors are selected in value and for their internal equivalent series inductances so that they will be an effective bypass at all frequencies of interest including video, to assist in maintaining stability. Towards this objective of stability, in addition to resonating with the device drain-to-drain capacitance at RF, inductor L9 places a heavy load on the FET output at low frequencies, where it behaves as a dead short.

HB IPA Set Up Procedures

1.Set up a 50 V power supply, current limited to a little more than 1.2 A.

2.Turn both bias potentiometers to their maximum resistance for minimum bias. Short C6 with a clip lead. This zero-biases the "B" half so it does not interfere (via L9) with the "A" half being adjusted.

3.Apply the supply to the B+ terminals and adjust R1 bias-adjust potentiometer for 600 mA drain current on side "A". Turn off the supply, change the clip lead to short C2 instead of C6, turn on the supply again, and adjust R7 bias-adjust potentiometer for 600 mA drain current on side "B".

These will be the starting points; the bias current settings and L9 will be readjusted during system test, for minimum intermods and FM noise. Disconnect the clip lead after adjusting bias currents.

4.Connect a 30 dB 20 W attenuator to the output of the amplifier.

5.Apply B+ to both supply connections of the amplifier.

6.Apply a low level sweep to the module and measure the DC input current (about 1.2 amps) and gain. Amplifier gain by itself should be 15 to 17 dB, and with preamp included and R5 at maximum, overall gain should be between 33 and 37 dB. Sweep response should be flat within 1 dB over the band as shown in the sweep diagram from page 4, repeated below. Note that the sweep curves are applicable to the push-pull FET amplifier only and the preamp is not included.

CONTENTS

Control and Metering Panel

40D1985G1

Transmitter control and monitoring is performed by the Control and Metering Panel. This 19" wide, 3 unit (5$\frac{3}{4}$") panel serves primarily as a mechanical mounting for the transmitter's control switches, status indicator lights, and a multifunction meter. It also is the mounting for the control circuit board described below, and for an output metering circuit board.

The transmitter control panel features as seen from the front, are:

- A panel meter calibrated 0-125 percent, and a 0-100 linear scale;
- The meter input selector switch for forward and reflected power, IPA output level, and AGC voltage;
- Pushbuttons for ON, OFF, REMOTE/LOCAL, AGC ON/OFF, TX RESET;
- A screwdriver adjusted potentiometer for the desired AGC level, hence transmitter output power;
- Five LEDs providing indications (from left to right) when lighted:
    - EXT 1 interlock is closed,
    - the output amplifier TEMP thermostat is cool,
    - EXT 2 interlock is closed.
    - VSWR L/O when lighted means three major VSWR events have occurred during a short time and the transmitter is now off the air, and
    - VSWR C/B lights up during a VSWR event that is sufficient to cause the transmitter power output to decrease, or even to momentarily turn off the transmitter.

The transmitter is provided with a VSWR cutback function that either reduces its power output to save it from harm in the event of gradual occurrences such as antenna ice build-up, or momentarily takes it off the air from random events.

Three VSWR events occurring rapidly in a short time will cause the VSWR Lockout mode to turn the transmitter off until it is reset. Random VSWR events normally do not cause lockout unless the reflection is sustained, causing repeated momentary tripping and ultimate lockout. Antenna or line damage occasionally can be a factor, but usually ice accumulation on the antenna causes sustained high VSWR.

Transmitter Control Circuit board Assembly

30C1829G1

See Figure 1 and Figure 2.

There are seven connectors on the Control circuit board. These connectors perform the following functions:

- J1 interconnects with J3 of the Metering board via a 34-wire ribbon cable.
- J2 connects elsewhere in the transmitter, such as the exciter and the PA, and to the meter.
- J3 connects to the external interlocks, and any special local controls for TX off and on functions.
- J4 interconnects with J4 of the Metering board for the AGC potentiometer and switch wiring.
- J5 is a 15-contact D-shell connector provided for user remote control system.

- J6 interconnects with J5 of the Metering board for the AGC, VSWR cutback, and VSWR shutdown signals.
- J7 is the connection to the AGC feedback input of the exciter.

The transmitter interlock chain begins with the +12V at K1-7. When K1 is set ON by energizing its coil K1-1, contacts 7 and 12 close and contacts 7 and 10 open, turning off the LED inside the OFF button S4. The +12V from closed contact 7-12 lights the LED inside the ON button S3 and lights the opto-diode in U3D, which provides a logical active low out of its pin 10 for a remote control status interface. This status signal simply tells the remote control through J5-6 that the transmitter was instructed to be ON, nothing more.

The +12V from contact 7-12 also comes out of the board on J3-5, which is one side of the EXT 1 interlock. EXT 1 in larger transmitters is often used with a fire alarm system to stop all blowers, and in lower power transmitters it is still worthwhile that a normally closed fire alarm contact be connected to EXT 1 because the fan(s) in the transmitter could cause enough air currents in the transmitter room to fan the flames.

When the EXT 1 interlock is closed and the +12V appears on J3-4, the +12V is now at DS5 (marked EXT 1) and the opto-diode of U3C which both light up to say EXT 1 is closed. The active low from U3C pin 11 informs the remote control via J5-14 that EXT 1 interlock is closed.

The +12V now is applied to J2-8 which connects to a normally closed contact in a thermostat that responds to the temperature of the RF power amplifier. If a cooling fan should stop and the amplifier should overheat, this contact will open and prevent the +12V from appearing at J2-3. This of course breaks the chain and removes the 12V from the solenoid of the power supply contactor.

Assuming the thermostat is cool, DS4 and the opto-diode in U3B are lighted, confirming TEMP is okay. The logical active low out of U3B pin 14 informs the remote control of this fact through J5-7.

Next stop for the +12V is a normally closed VSWR lockout relay contact connected via J1-5 and J1-9 from the Metering Board (Prefix 5A, K2). This relay operates and the interlock chain is opened, if for some reason the transmitter has seen a large amount of reflected power and the Metering Board VSWR supervisory circuit has repeatedly tried and retried to keep the transmitter on and finally decided "Enough!" The VSWR lockout relay can be reset from RESET button S6, or by the VOR Enable and/or Remote ON via jumpers E1, E3.

Assuming the VSWR is low and 5A-K2 contacts are closed, the +12V next appears at J3-3, which is EXT 2 interlock. This is the place where RF patch panel link contacts or coaxial switch auxiliary contacts, and/or dummy load thermostat contacts would be connected so that the transmitter can only be ON when valid RF paths are present, consequently the EXT 2 path from J3-3 to J3-7 will be intact.

Finally, when the interlock chain is complete, the +12V is applied to the solenoid of the power supply primary contactor through J2-10, and the cooling fans and power supply are all turned on. The DS3 LED marked EXT 2 is lighted, as is the opto-diode in U3A. The output active low from U3A at pin 15 informs the remote control via J5-15 that the EXT 2 interlock is intact.

The interlocked +12V is also available at J3-6 so it can be used for special on-site control functions.

The transmitter control circuit permits the transmitter always to be turned OFF. Any +12V applied to the K1 Reset coil at pin 6 will cause the +12V to be removed from the interlock chain discussed above, and diverted instead to the LED inside the OFF button S4. The fact that turn off is possible regardless of the position of the REMOTE/LOCAL switch, is a valuable safety feature provided in all LARCAN transmitters.

The transmitter AGC system is based on an RF attenuator located near the output stage of the exciter, and this is controlled by DC voltage supplied from RF detectors which sample the RF output from the transmitter. If the

output rises, the DC voltage increases, and this increases the amount of attenuation, thus the output is maintained at a constant level. The AGC processing is done by analog op-amp circuits in the Metering Board, but the initial threshold setting is done in the Control board from AGC switch S5 and AGC potentiometer R9. These simply provide an adjustable reference bias voltage to the AGC circuit, which adjusts the power output inversely according to this bias voltage. When S5 is open (the LED in S5 is off and AGC is Disabled), R9 rises to the +12V rail of the Metering Board and the AGC processing stage inverts this high voltage so its output and thus the AGC voltage is very low, resulting in maximum exciter output. Exciter output is preadjusted with AGC off, to make 110% transmitter power.

In the event of a VSWR that exceeds a preset amount, the AGC voltage becomes modified a little to reduce the transmitter output by an amount proportional to the reflected signal. This "VSWR Cutback" permits the transmitter to remain on the air at reduced power if the antenna should gradually accumulate a layer of ice. If the reflected power should exceed a much larger amount causing repeated momentary tripping off air and the VSWR supervisory circuit attempts to restore transmitter operation but cannot and then locks out, then the AGC voltage is cut down even more. This is called "VSWR Shutdown."

The AGC voltage and modifications to it from VSWR, are summed in U2A which is basically a buffer amplifier that also provides a telemetry output to the remote control system through J5-3.

R15 sets the calibration of the meter when it reads from the AGC position of the meter selector switch S1.

R1 sets the calibration of the meter when it reads the IPA output level from the IPA position of S1.

Forward and Reflected meter calibration is done with potentiometers on the Metering Board.

Contents:

RF Metering & AGC Board

20B1299G3:
Figures 1 and 2.

This board serves several functions: AGC, VSWR supervision, forward & reflected power metering, and telemetry. Except for their functions and input names, metering boards have identical RF detectors. For this reason, Detector #1 for "Forward" will be described, and #2 for "Reflected" will be referenced by its component numbers inside parentheses ( ).

RF Detectors:

The #1 Forward (#2 Reflected) RF power sample is applied to J1 (J2) and is terminated by R2 (R4). A small amount of forward bias is applied to CR1 (CR2) via R1 and R5 (R3, R6) to overcome the threshold voltage of the diode and enhance its detection linearity at low signal levels. The opposing connection of CR1 (CR2) diode junction and Q1 (Q2) emitter-base junction provides temperature compensation.

Q1 (Q2) buffer amplifier provides a low impedance source to drive the trap C3, C4, and L1 (C5, C6, L2), through R9 (R10). This trap is broadly resonant to 4.3 MHz, and significantly attenuates 3.58 MHz NTSC color subcarrier as well as any 4.5 MHz intercarrier that may be generated in CR1 or CR2 due to the presence of visual and aural RF signals together in the system. Removal of these subcarrier components before the signal is peak detected, enables the circuit to be responsive to sync peak power only (for visual) or just CW (aural) power, and relatively immune to undesired carriers.

CR3 (CR4) is a peak detector with a time constant set by C7 and R11 (C8, R12). The signal from this peak detector is fed to op-amp U1 (U2) pin 5. The gain of this stage is 2x (4x), and its output on pin 7 feeds telemetry and metering signals to the outside world. In the board used as Prefix 5A in the 1 kW transmitter, pin 7 also feeds voltages for AGC (VSWR supervision) to the pin 3 second half of U1 (U2). These op-amps are used in the main AGC and VSWR functions of the transmitter.

U1 (U2) output pin 7 zero-offset voltage is controlled by R18 (R20). This pot should be set with no RF input, so that while you watch the voltage on TP1 (TP2) as you are setting the pot, you will observe the decrease of the voltage towards zero. When it ceases decreasing, stop adjusting. Expect about 20 mV offset voltage when the op-amp output is almost touching ground. If the pot is turned beyond this point, the output stage of the op-amp will be driven into saturation thus unable to respond to low power levels.

The output of U1-7 (U2-7) drives the RF power meter through R32 (R30) which set the meter deflection with a known RF signal. U1-7 (U2-7) drives the telemetry buffer U4 through R29 (R47) which are adjusted to calibrate the telemetry to a standard voltage with a known RF signal. Forward calibration is done with full rated power and a forward RF sample from the probe section applied to J1. R29 is adjusted for 3.0 VDC delivered to J3-6, and R32 is adjusted for a 100% reading on the forward power meter position.

For Reflected calibration, the same forward RF sample is then applied through a 16 dB pad to J2, and R47 is adjusted for 1.5 VDC at J3-10, and R30 is set for a 2.5% reading on the Reflected Power meter. Because of the extra 16 dB, the calibration automatically gets a x40 multiplier, so the actual reading of the meter is 2.5% on a full scale of 12.5%. The first scale mark of the meter is then 0.5%. If you were to substitute a 10 dB pad for the 16 dB and adjust R36 and R49 to get the VSWR supervision levels out of the way, you would see a meter deflection of 100% which corresponds to actual 10% reflected power, and a telemetry output voltage of 3.0 VDC. It is simply the insertion of the pad and the subsequent calibration, that provides the meter multiplier scale factor.

When you are setting up the adjustments on this board, disable the AGC, and set the exciter level for 100% RF output from the transmitter. This is especially true for the reflected or VSWR settings, because these are done at a forced RF level that is high enough that the AGC system will be driven into cutback mode which is what will need to be set up because it affects the exciter output.

AGC and VSWR supervision:

The output from U1 (U2) pin 7 is also applied to a second op-amp U1 (U2) pin 3. If the detected level at U1 pin 3 rises above the level set by the AGC pot (on the Control board) at U1 pin 2, the output on pin 1 will rise. This AGC output is applied via J5-1 to a final buffer amplifier (U2A on the Control board) and from there to a PIN attenuator in the exciter, thereby reducing the transmitter power accordingly.

The reflected power detector CR2, Q2, CR4, U2 is similar in operation to the forward power detector CR1, Q1, CR3, U1. If the reflected power rises to a value higher than a calibrated value of 17 to 18 dB below the forward power level, then pin 3 of U2 rises above the voltage on pin 2 that is set by the adjustment of R36, U2 pin 1 will go higher, which applies a drive cutback signal via J5-2 to U2A in the Control board and from there to the PIN attenuator in the exciter. At the same time, U3 pins 3 and 6 are also driven more positive.

When the voltage on U3-3 exceeds the voltage on U3-2 that is determined by trip threshold control R42, U3-1 goes HIGH, to output a status signal HIGH through buffer Q4, and to energize VSWR trip relay K1 thru buffer Q3. The base of Q3 in some transmitters may have a time delay R61, C21 added, to avoid false VSWR tripping after power failure and restoration. The component parts for this "fix" may be soldered to the back of the board in Rev 4 and earlier.

If the reflected power increases still further, the voltage on U3-6 rises past the voltage threshold set by R49 on U3-5, then U3-7 will switch LOW, which triggers the "555" timer U5. This IC will produce an output pulse at U5 pin 3 of approximately one second duration. This pulse is also applied to the PIN attenuator to temporarily remove RF drive. Restoration of the transmitter should normally happen

after one or two occurrences. The third occurrence within a predetermined time (C20, R51) should cause lockout.

If enough VSWR events within a short time, or one sustained occurrence, causes U5 to produce three pulses in rapid succession, C20 acquires a sufficient charge thru R51 to raise the voltage of pin 5 of comparator U6 higher than its reference voltage on pin 6, then Q5 will be driven HIGH which energizes relay K2, thus locking out the transmitter.

When +12V regulated power is taken from the companion exciter, regulator VR1 is not needed nor used.

RF Metering Board Test and Calibration:

Forward Power Meter Calibration - Zero Adjust

With no RF input connected, measure the DC voltage at U1-7 (or TP1) and adjust R18 until the output voltage at U1-7 (TP1) drops to a minimum, approximately 10 to 20 mVDC. A DC coupled scope will make the adjustment easier to see; the objective is to place the U1 output as near the op-amp ground rail as possible without the op-amp going into saturation. Turning the pot farther will decrease the sensitivity of the system for small signals. Once this minimum voltage has been reached, do not re-adjust R18.

Reflect Power Meter Calibration - Zero Adjust

With no RF input connected, measure the DC voltage at U2-7 (or TP2) and adjust R20 for a minimum, which should be approximately 20 mVDC. Once this minimum voltage has been reached, do not re-adjust R20. This adjustment is done in precisely the same way as in step a) above.

Forward Power calibration and Telemetry

Turn off the AGC and set the exciter RF output for the transmitter to run at rated peak sync (or at maximum licensed power, whichever is less; call this "Full Power"), then adjust R29 for a telemetry output reading of 3.0 VDC measured at U4 pin 7 or J3-6.

Reflected Power calibration and VSWR Trip Settings

With the transmitter still at "full power", disconnect the RF input cable from J1 and connect it instead to the reflected power input J2 via a 16 dB pad. Adjust R30 so that the reflected power meter upper scale reads 25. This now corresponds to an actual reflected power of 1/40 (2.5%).

Adjust R47 so that the telemetry output at U4 pin 1 reads 1.5 VDC. This is the voltage that corresponds to 2.5% power. Full scale 10% power will be 3.0 VDC. We are reading a front-panel meter whose scale is calibrated to a square law so it displays power, and we want the corresponding voltage. In the event that the circuit cannot deliver 1.5 VDC, go for 1.0 VDC instead. The telemetry voltage corresponding to 10% power level will then be 2.0 VDC. Most remote control systems can accommodate this.

Adjust R36 to cut back the output of the transmitter until the reflected power meter upper scale now reads 20 (2.0%). This is about 17 to 18 dB below the full forward power output of the transmitter.

With the 16 dB pad still in circuit, adjust R42 until K1 energizes, and the "VSWR C/B" indicator LED on the Control Panel lights up.

Replace the 16 dB pad with a 10 dB pad, and adjust R49 slowly until U3-7 goes LOW, causing U5 to pulse. After three pulses (visible on the meter), lock out and a red "VSWR L/O" indication on the Control Panel should occur. Check that RESET is possible using the RESET button S6 on the Control Panel.