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TECHNICAL MANUAL
1KW UHF INTERNALLY DIPLEXED TV TRANSMITTER
MX1000U SERIES

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INTRODUCTION

This manual describes the LARCAN model MX1000U, internally diplexed UHF television transmitter.

LARCAN all-solid-state 1 kW UHF transmitters are designed to operate conservatively at 1 kW peak sync visual/vision RF power and 100W average aural/sound single carrier RF power, with superb performance, reliability and operating economy. The MX1000U transmitter accepts an on-channel internally diplexed (in a 10:1 ratio vis to aur/snd) composite driving signal of 10 mW peak visual RF, as input to its RF chain.

The 1 kW transmitter is self-contained within a single 19" cabinet with an integral cooling fan and filtered rear door air intake. The simplicity of design, the employment of modular subassemblies, and the use of standard readily available components, also enhances serviceability.

Important transmitter parameters are monitored, and can be displayed on the meters built into the transmitter control panel. Additionally, telemetry readings are made available as DC signals for monitoring by remote control systems. The MX1000U, like all other LARCAN transmitting equipment, is suitable for unattended remote-control operation.

AMPLIFIER CHAIN (REFER TO FIGURE 1)

The Aural signal of the transmitter is diplexed (at IF) with the visual/vision signal within the exciter (hence the term "internally diplexed), and is amplified in common with the visual signal in the above amplifier chain (hence the term common amplification).

The internally diplexed composite RF output of the exciter/translator is fed to a 4-way active splitter. The 4 outputs of the splitter are fed to conservatively designed broadband solid-state amplifiers. The outputs from the four PA modules are combined for the total transmitter output power. These amplifiers require no tuning or adjustment. Phasing for the four PA modules is done at the splitter level. Internal cable lengths and precise production tolerances allow for a very small adjustment range for phasing. Simplicity of operation, reduced maintenance costs and increased reliability are a few of the major benefits derived from this modular amplifier design. The modules are operated well below their maximum ratings.

Each RF power amplifier (PA module) is fully modular within itself and each module has a gain equivalent to the entire gain of the transmitter (see Figure 2). Each PA module has it's own preamplifier, Intermediate PA, Driver and PA section. The front end preamplifier on the PA module monitors and provides soft startup, overdrive and VSWR protection for the module itself (independent of the transmitter protection). The output stage of the module consists of three amplifier "pallets" each consisting of two push-pull LDMOS FET amplifiers that operate in class AB, and are combined in quadrature. The outputs of these pallets are further combined in a 3-way combiner. The amplifier module is rated for 350 watts, and in the present four PA module system is operated at a total transmitter power of 1 kW sync peak + 100 watts aural/sound. The module is provided with a test jack for monitoring.

The amplifier output is fed to the bandpass filter and a directional coupler, which provides a small sample of forward and reflected output power for metering, AGC and VSWR supervisory functions. An additional sample is available for monitoring and transmitter setup. The transmitter output then passes to the antenna system.

TRANSMITTER CONTROL

The control circuitry in this solid state transmitter is straightforward and simple. The use of latching type relays ensures that the transmitter state (on/off, or trip status) is “remembered” under power failure conditions. Interlocking is provided for loss of airflow and for over temperature conditions. An additional interlock connection point is provided for interlocking the transmitter to an external patch panel.

Facilities are provided on the control board for telemetry, status, and control connections to and from a remote control system. These are available on 25 pin D-sub connector.

For remote control operation, simply press the REMOTE switch (LED illuminated). This places +12V on Remote Enable line and allows the transmitter to be turned on and off via remote control. In this mode the transmitter cannot be turned on locally but for safety purposes, the transmitter can always be turned off locally while in REMOTE.

The Remote Enable +12V appears as an arming signal at J5-5. A momentary connection of this +12V to J5-13 turns the transmitter ON, and momentary connection of the +12V to J5-8; turns the transmitter OFF.

Control circuit power for the transmitter is supplied by two redundant power supplies wired in parallel. The failure of either power supply will not affect the operation of the transmitter.

The transmitter's power supply consists of two ferro-resonant transformers each with dual secondary windings. Each transformer secondary feeds a rectifier/filter and linear regulator combination. The regulator modules are located inside the rear door of the transmitter and can be removed for servicing by first disconnecting the two cables and then unplugging the module. This can be done without turning off the transmitter.

A two pole fused disconnect or breaker is required for transmitter connection from line-to-line. The transmitter is wired per Figure 5.

- Press the OFF button on the control panel. Pull out the regulators so they are no longer mating with their respective AC power connectors. Turn on the power supply breakers. Press the ON button. Looking into the back of the transmitter DS6 and DS7 on the AC distribution board should be illuminated (refer to figure 3). If the blower comes on and DS6 and DS7do not, then the AC Distribution board needs to be bench tested.

- Press the OFF button again. Install the regulators but disconnect the cables that mate at the top of each regulator (connecting the regulators to the PAs). Turn on the transmitter. Measure the voltage on the output connectors of the regulators. The voltage should be 28V (±0.5V) for each regulator. Note: Since the regulators have no load, when the transmitter is subsequently turned off it will take a while for the voltage to decay down to zero.

- Turn off the transmitter. Reconnect the cables to the regulators. Turn the RF drive level down as far as it will go at the appropriate OUTPUT LEVEL/RF OUTPUT adjustment on the exciter. Alternatively, disconnect the drive from the output of the exciter. Turn on the transmitter. Using a clamp-on current meter, measure the current going from the regulators to the PA's. Measure the current going through the +28V supply cables and not the return cables (some of the ground current may return through the transmitter chassis as opposed to the return wires, causing the current reading to be lower than it actually is). The 28V supply cables are the two lower wires in the cable assembly (Figure 4). These are accessible by pushing back the protective covering on the cable. The front panel current meter (the digital LCD meter) can now be calibrated for each PA module. (Remember that the modules are numbered 1-4 from left to right across the front of the transmitter. This will be reversed when looking into the rear of the cabinet.) The corresponding adjustment pot on the control panel (PC board 20C2065G1) is listed below.

PA1	Pot R221	PA2	Pot R225
PA3	Pot R229	PA4	Pot R223

  These adjustments can be accessed by opening the hinged control panel on the front of the transmitter.

- Disable the AGC using the front panel AGC Enable switch. Note: the AGC is disabled when the LED on the enable switch is off. Increase the output power from the exciter until 100%

operating power in achieved. Use a thru-line type Wattmeter to measure the transmitter power. Select FWD on the analog meter select switch and adjust R164 on the control board until the forward power meter (analog meter) reads 100%.

- To calibrate the aural power, refer to the RF detector board description and setup procedure.
- Calibration of the reflected power metering and the VSWR cutback and trip is detailed next. Note, this setup was done at the factory initially, and should not be adjusted unless absolutely necessary. Conditions that would warrant this adjustment include the replacement of the RF detector assembly or the control PC board.
- Turn R130 fully CW and R138, and R128 fully CCW
- The Reflected power meter reading corresponds to 10X the actual power reflected. That is, when the reflected power meter reads 100%, this means 10% of the output power is being reflected (ie: there is a VSWR of 1.9:1 at the transmitter output). (10dB match). To calibrate the meter for this level, the forward sample port that feeds the RF detector circuitry for metering is fed through a 10dB attenuator back to the reflected power input on the RF detector board. To do this, disconnect the cable at the forward port of the output directional couple and connect Reflected power sample cable through a 10dB pad to the forward power port. This simulates having a 10dB mismatch on the output of the transmitter. Note: AGC must be disabled during this procedure. Adjust R117 until a 100% reading is achieved on the RFL power setting of the analog meter.
- Change the attenuation from 10dB to 16db of the forward power into the reflected port on the metering board. Adjust R138 so that the power just starts to cutback slightly
- Adjust R130 so that the VSWR CUTBACK LED just turns on.
- Change the attenuation to 13dB. The cutback circuit should cut the power way back. Adjust R128 so that the transmitter trips and locks out with VSWR.
- Now change the attenuation to 14 dB of forward power into the reflected port on the metering board. Adjust R128 so that the transmitter does not trip and lockout with VSWR. You may have to press reset, adjust the pot, press reset, adjust the pot, etc. Then repeat the previous step to verify that the transmitter still trips with 13 dB of reflected power.
- Reconnect the forward and reflected sample cables to the directional coupler as they were before. Verify that the AGC buttons can raise and lower the power levels.

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1. INTRODUCTION

RF Power levels throughout the transmitter are sampled in directional couplers, and the resulting RF samples are detected and appropriately processed to provide DC outputs corresponding to the amplitude of the desired parameter of the input signal. These DC outputs contribute to the AGC/VSWR supervision of the transmitter as well as the front panel metering.

The 41D1607G1 and 41D1607G3 dual RF detectors are designed for measuring forward visual/vision signal, forward aural/sound signal and reflected combined visual and aural signal. Group 1 is for NTSC and group 3 is for PAL. The circuitry provides DC outputs corresponding to the instantaneous visual/vision forward and reflected RF levels at the back porch (blanking level) of the modulated signal, so that the DC output remains proportionally constant regardless of the video signals to the transmitter. Two virtually identical detector circuits reside on a single board for visual forward and reflected metering. Detection sensitivity of the circuitry for reflected visual/vision power is approximately 10 dB greater than for the visual/vision forward RF detector circuit. Group 1, (for NTSC) and group 3, (for PAL) differ only in their colour subcarrier frequency, consequently in a few component values.

The aural/sound metering circuit takes a sample of detected video signal from forward port and provides DC level proportional to the amplitude of the aural carrier. The sample of this DC level is used to compensate visual forward reading affected by presence of the aural carrier at the forward port. The reflected port does not have this compensation circuit so in reality reflected reading is combined visual and aural power.

The 41D1607G2 and 41D1607G4 dual RF detectors are similar, but have identical detection sensitivities for each circuit. They are designed for use in parallel amplifier systems. Group 2 is for NTSC and group 4 is for PAL; again, these differ only in colour subcarrier frequencies. The two ports J2 and J3 are not identical. J2 has aural metering circuit and compensation circuit for the presence of aural carrier at J2 port. J3 will measure combined visual and aural power unless special trap is used to reject aural carrier

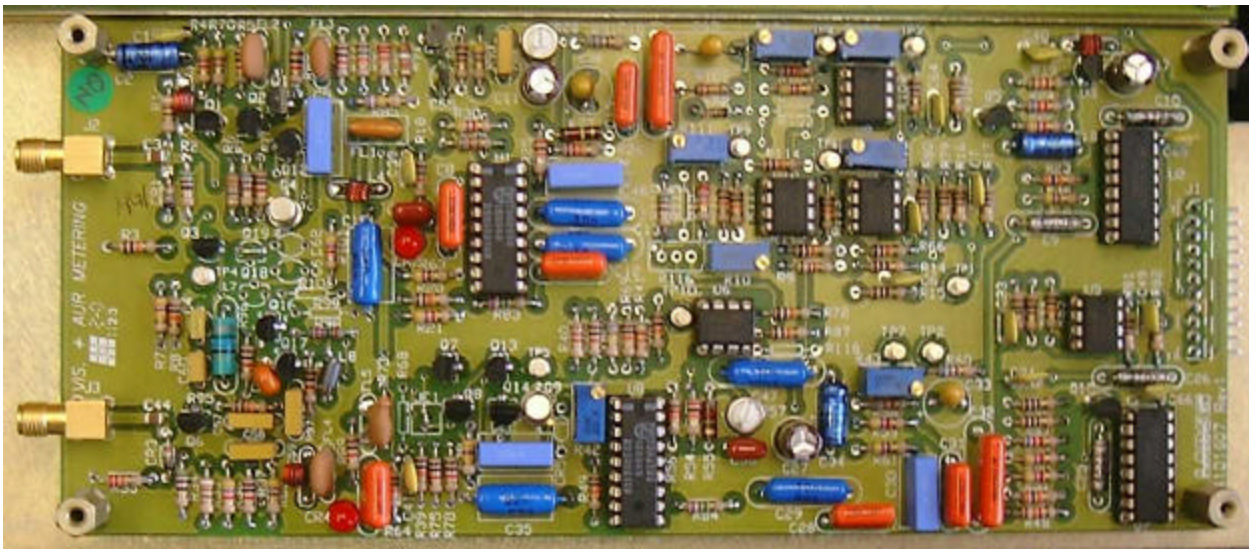

Figure 1: RF Detector Board

2. CIRCUIT DESCRIPTION

Drawing references: 41D1607 sheet 1 (Figure 3), and 41D1607S sheet 1 (Figure 4).

The visual/aural RF Detector board is fitted with two RF detectors, which respond to RF samples fed from RF directional couplers mounted on transmission lines in the amplifier cabinets and/or on external probe sections. The modulation envelope blanking level is measured because it remains constant, regardless of the picture content of the transmission. Measurement sampling occurs during the back porch.

Both sections of the board are almost identically configured, except for the component numbering, system gains and the function names given in schematic Figure 2. Because the same discussion applies to both circuits, we will describe the first one only, but refer to the second one during the description by enclosing the relevant component numbers in parentheses ( ).

VISUAL FORWARD AND COMBINED REFLECTED CIRCUIT DESCRIPTION

(REFER TO 41D1607S SHEET 1)
The RF sample is applied to input J2 (J3) and is terminated by R2 (R34). CR1 (CR3) and Q1 (Q6) form an envelope detector. CR1 (CR3) is forward biased slightly by R1 (R33) and R3 (R35) to overcome CR1 (CR3) conduction threshold voltage, thereby improving detection linearity. Q1 (Q6) is forward biased by R3 (R35) as well, and when RF is applied, Q1(Q6) is driven in the direction of turn off during each positive-going half cycle, thus causing its emitter voltage to become more positive, and in effect forming a linear envelope detector.

C50 (C51) utilizes the lead inductances of CR1 (CR3) and Q1(Q6) to form a Tee network, which provides a matching section that improves the UHF signal transfer between the devices.

Q1(Q6) and CR1 (CR3) have similar temperature coefficients, and the opposing connection of the two in this back-to-back configuration, provides temperature compensation.

Finally, Q1(Q6) serves as a low impedance video source to drive the colour traps FL2, FL4 and aural traps FL1, FL3 which remove the colour subcarrier burst and aural carrier from the back porch. Subsequent downstream sampling circuits monitor the blanking level, therefore require a clean back

porch. The detected video signal is phase split by Q2 (Q7) to produce two 180° out of phase signals. The inverted video signal, after being buffered by Q11(Q13), is fed to input pin 11 of sync separator Ul (U8).

Ul (U8), pin 7 is an open collector "mute" output, which switches off when adequate horizontal sync pulses matching the setting of R28 (R57) are present, lighting CR2 (CR4) the "sync ok" LED. If a TV sync signal is not detected, pin 7 collector goes low, and CR2 (CR4) is turned off. When sync is detected, the sync output at pin 9 delivers a positive-going composite sync pulse, which turns on Q5 (Q10) whose collector then goes low. If no sync is detected by Ul (U8), its pin 9 remains LOW, and Q5 (Q10) remains off.

After the pin 9 pulse has finished, Q5 (Q10) turns off and its collector output goes high. This low-to-high transition activates blanking multivibrator U2 (U7), and an active low pulse is fed to Q3 (Q8), turning it on.

Q4, C5, and U4A (Q9, C22, and U6B) form a sample-and-hold circuit that samples the signal originating from the emitter of Q2 (Q7) and which is buffered by Q12 (Q14). Sampling occurs during the back porch, and holds during the subsequent horizontal line. This DC sample is amplified in U4A (U6B).

Because a "single supply" op-amp is used at U4 (U6), the output seen on TP9 (TP10) will contain a small DC offset which must be minimized because low level signals are near ground/earth potential. With no RF input, this offset voltage is adjusted by potentiometer R10 (R42) as near as possible to zero. A residual voltage offset of 10 to 20 millivolts can be expected.

Outputs from unity gain op-amps U4A, U4B(U5A, U5B) drive the forward (reflected) power metering circuits, and provide telemetry and AGC (VSWR) signals.

Bench test calibration consists of adjusting the level to U4A (U5A) on R13 (R43) with calibrated, properly modulated input: The forward input at J2 should be 200 mW in 50Ω, (J3 Reflected input 20 mW for both the 41Dl607G1 ,3 boards, or for 41D1607G2,4 boards the J3 Combined input 200 mW), and the voltage observed at TP1 (TP2) should read 4.0 volts DC for full scale calibration.

AURAL FORWARD METERING

A sample of the signal detected by CR1 from J2 is buffered by Ql and high-pass filtered by R90, C55 and the input impedance of Q15. R92 and R91 set the base bias for Q15 while R93 and R94 set the gain of the stage to approximately 4.7 for the 4.5 MHz (5.5 MHz) aural intercarrier signal. The wideband visual/aural signal drives FL1, an aural bandpass filter. This filter is chosen to match the broadcast standard used. C59 couples the filtered aural signal to common emitter amplifier Q17 which is direct coupled to common base amplifier Q16. The bias for these stages is set by resistors R95, R96, R97. C57 and C58 provide bypassing. Q16 is a current amplifier with L7 as the collector load and C60 provides frequency compensation.

The aural signal is then fed to a peak voltage detector consisting of CR6, C63 and R102. U9A provides DC amplification of the detected signal. Amplifier gain is set by potentiometer R104 such that the DC level at TP8 is in the range of 7VDC. This provides enough "safety" range for the signal not to saturate yet enough level to reliably give a 4VDC calibration at TP3.

3. TEST AND CALIBRATION

TEST EQUIPMENT FOR BOARD TESTS ON THE BENCH:

RF Detector test fixture, comprising a 12 volt DC power supply, suitable connectors for the board to be tested, a signal generator, a modulator, and an amplifier good for 200 milliwatts output. An exciter will suffice for the generator and modulator, but its output is good for a maximum +10 dBm (10 mW) therefore

requires an external amplifier, and the exciter aural output may be used as an unmodulated source if required (A LARCAN exciter visual/vision section can not deliver unmodulated RF).

TEST PROCEDURE

TEST EQUIPMENT REQUIRED
- 12 V power supply
- UHF preamplifier (approx 200mWo/p).
- Video Generator.
- Modulator.
- UHFUpconverter.
- Oscilloscope.
- Spectrum Analyzer.
- VHF / UHF Two Way Splitter.

For test setup, see Figure 2.

1. Connect board under test to power supply. Apply ground on pin 7 & 8 of J2 and apply +12v (± 0.2 V) to pins 3 & 4. Do not apply RF to J2 and J3 yet.
2. Adjust R111 max CW.
3. Adjust R10 to get a min voltage at Ul0-1 (TP9).
4. Check the voltage between U10-2 and U10-3. It should be no more than 10 mV.
5. Adjust R42 to get a minimum voltage at U6-7 (TP10).
6. Check the voltage between U6-6 and U6-5. It should be no more than 10 mV.
7. Set R104 in mid position.
8. Apply staircase modulated RF signal from UHF upconverter to J2 and J3 through splitter according to Table 1. The signal should include aural carrier 10 dB lower than visual sync peak. Check this level on the spectrum analyzer. Note: *Make sure* to *set spectrum analyzer resolution RBW to 300 kHz to see sync peak level.*

Assembly Group	G1/G3		G2/G4	
Connector	J2	J3	J2	J3
Visual Peak Signal [dBm]	23	13	20	20

TABLE 1.

9 Adjust R104 for 7.5 ± 0.5 V at TP8.
10 Adjust R107 for 4V at TP3.
11 Adjust R28 so that CR2 lights up.
12 Adjust R57 so that CR4 lights up.
13 Using the oscilloscope, check that there are positive 12V pulses at TP4 and TP5.
14 Check DC voltage at TP9.
15 V_{TP9} should be within 4.5V to 9.5V.
16 Check DC voltage at TP10.
17 V_{TP1O} should be within 4.5V to 9.5V.
18 Turn off the aural carrier.
19 Adjust R13for4VatTP1.
20 Turn on the aural carrier.
21 Adjust R111 for4V at TPl.
22 Repeat steps 12 and 13 until voltage at TP1 stays the same with and without aural carrier.
23 Adjust R43 for 4 V at TP2 with aural carrier on.

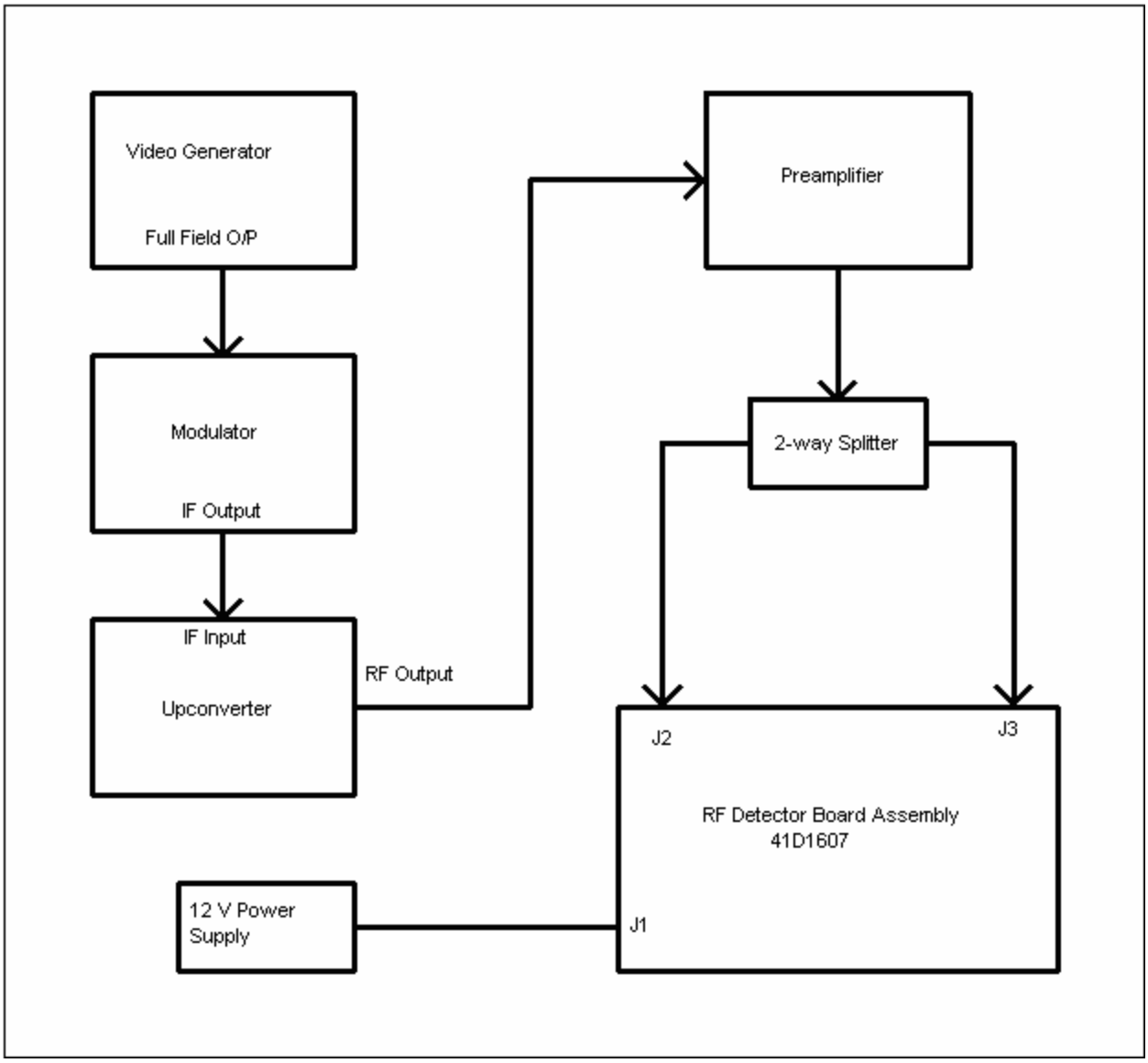

Figure 2. Test Setup For Visual + Aural RF Detector Assembly.

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1. INTRODUCTION

The PA module for the MX1000 is a high gain linear amplifier. Each PA module includes its own preamplifier, intermediate amplifier, driver amplifier and power amplifiers. The gain of the module is equal to the gain of the entire transmitter. Every PA module has its own on-board protection against overdrive, excessive VSWR and over temperature. A single LED on the front panel indicates the status of the module. Any fault will cause this LED to turn off.

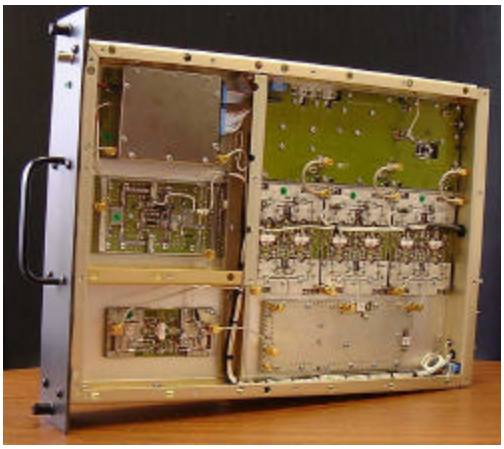


Figure 1: PA Module, MX1000

2. CIRCUIT DESCRIPTION

FRONT END PREAMP.

The RF input to the module is via J1. U1 provides the amplification of the signal for this stage. This IC is an 18dB gain broadband hybrid amplifier. The output of this stage to the following amplifier (IPA) stage is through J2. A directional coupler HY1 provides a sample of the input power for a detector CR1, C2 through C4 and buffer amplifier U6B and associated components. A PIN attenuator circuit consisting of CR2, CR3, R8 through R13 and C5 and C6 provides the means for controlling the signal gain through the front-end stage. A higher voltage applied to this attenuator through L1 results in less attenuation through the PIN attenuator and hence, more gain through the preamp unit. A further coupler HY2 provides an output sample to a detector and buffer circuit (CR4 and U6C). The maximum gain of the front-end preamplifier is approximately 8dB, however, in practice, the gain is adjusted to compensate for gain differences in other stages such that the gain of each PA module is the same.

The three-way combiner circuit for the PA module incorporates a bi-directional coupler with detectors for forward and reflected power on the module. These detected voltage samples for forward and reflected power are fed into the front-end preamp through J4-7 and 14. Comparator circuitry is used to detect either overdrive conditions or VSWR conditions. Since the circuitry is identical for both forward and reflected, a circuit description will be given for the forward power circuit only.

U3D is configured as a comparator with the reference voltage being provided by the voltage divider consisting of R44, 45, 46. *Note: this level is preset. Values for this voltage divider should not be*

modified. Doing so without prior authorization from factory service personnel will void any warranty. When the detected voltage rises above the preset level, the output of the comparator U3D goes high, and forces transistor Q1 to the "on" state through diode CR7. Other inputs to Q1 include the reflected (VSWR) signal, an external mute signal and a power-up delay circuit consisting of U5D configured as a comparator along with R47 through R50 and C20. The action of turning on Q1 causes the voltage on the PIN attenuator, preset by R25, to be shunted through the transistor, thus increasing the attenuation of the PIN attenuator.

Additional circuitry on the front-end preamplifier also drives the logic for the Green LED on the front panel of the PA module. Output samples from each of the power amplifier pallets are monitored and compared with preset voltages through comparators U2C, U2D and U3C. A failure of the output of any one of these pallets will cause the output of U5A to drop and the LED (connected to J6) to be extinguished. Note: this applies if the input RF signal is removed and thus results in no output from the module (as well as in the case of an overdrive situation or VSWR cutback situation).

There are buffered signals for the various stages on the PA module that are brought to the front-end preamp and routed through to the interface board on the rear of the PA module. These signals are present on the 25 pin connector (intended as an on-site troubleshooting port). In the MX 1000 application, these signals are present but most are not monitored by the transmitter's control circuitry.

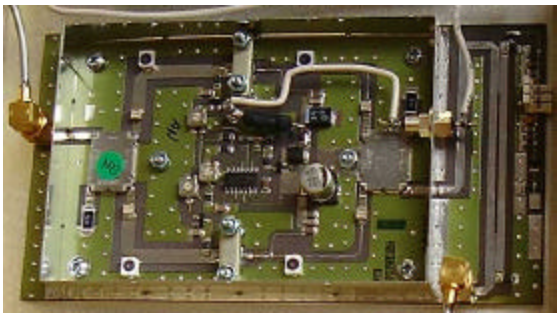


Figure 2: IPA Module

IPA MODULE

The intermediate amplifier consists of two FET amplifiers, type MRF181 paralleled in RF phase quadrature, and operated in class A. Amplifier static bias control and over-current protection is provided by an industry-standard type µA723 regulator IC, U1. The overall gain of the Intermediate Amplifier is a nominal 15 dB over the band.

The input signal is split evenly by quadrature hybrid splitter HY1. Each FET gate is matched with the equivalent of an L network followed by a π network. Capacitors C100 and C110 provide DC blocking of the gate voltage. A couple of low impedance microstripline sections along with adjustable capacitor (C101 or C111) to ground and the gate capacitance of the FET form the L-C-L-C matching network for the input circuit. This matching arrangement is good for operation from 470 through 860 MHz, adjustable capacitors C101 and/or C111 provides for a flat frequency response over the range.

The output circuit is similar except it uses narrower (higher impedance) microstriplines because the drain impedance of the FET is higher. The output matching network is adjustable with variable capacitor C103 or C113. Again, this capacitor is adjusted only to provide flat response over the 470 to 860 MHz range. An output coupling capacitor C104 or C114 completes the match to 50 ohms; two amplifier outputs are combined in a quadrature hybrid HY2.

Bias to the gates of the FETs passes through R100 or R110 from balance controls RV100 or RV110. The bias regulator Ul uses an µA723 (MC1723CD) to provide approximately 6½ volts to the gate bias controls RV100 & RV110. Voltage divider R5, R6 provides the inverting input of the regulator error amplifier with a sample of the output voltage, and the wiper of RV3 provides the non inverting input with its reference signal which is an adjustable fraction of the 7.15 V built-in reference of the µA723. The adjustment of RV3 therefore should be able to give an output within the range from zero to approximately 9 volts. R4, C2, C1, R3, and C4 provide frequency-compensation and maintain regulator stability.

Drain current of the two FETs is sampled by the voltage drop across R7. When this voltage exceeds approximately 0.5V at normal operating temperature (about 1.5 amps total FET current), Q3 begins conduction and feeds voltage to pin 2 of the regulator to start its current foldback/limiter circuit. The regulator reduces its output voltage, which in turn reduces the bias on the FETs, they decrease their drain currents, reducing the voltage drop across R7 and over-current protection is achieved. CR1 protects Q3 emitter-base junction from current inrush to C3 and C107 charging during start-up.

PALLET

The following description applies to the driver amplifier as well as the circuitry used in each of the three sub-modules comprising the final PA stage of the PA module. The difference being that the driver consists of a single device amplifier (called a "half-pallet") while the final stage are based on dual FET amplifiers with an integral 3dB hybrid combiner. Referring to the schematic diagrams (figures 14 and 16) one will notice that even the component numbering is similar. The following description is for the dual FET version of the amplifier (refer to fig 16).

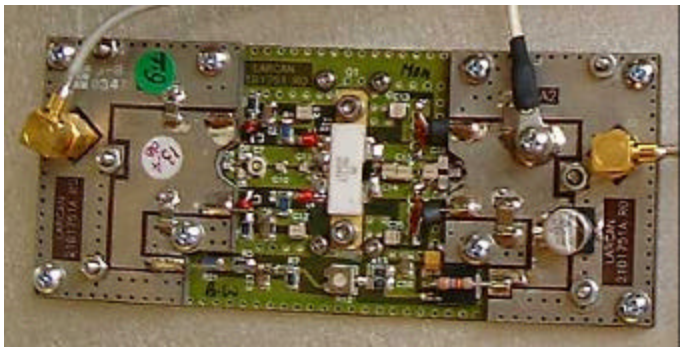


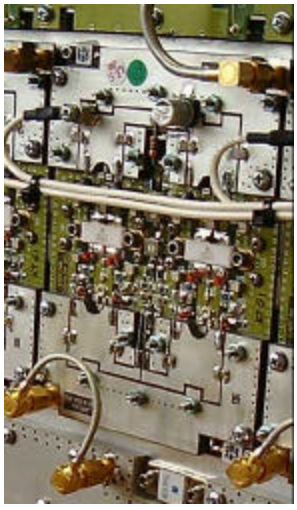
Figure 4: Driver

The stripline balun developed at LARCAN is a practical implementation of the coaxial cable based solution on a broadside-coupled horizontal stripline structure. It is made up of three printed circuit boards of high dielectric material bolted together. Using this structure, very tight coupling can be achieved, thus emulating the properties of a coaxial transmission line balun. With this arrangement, the characteristic impedance and degree of coupling can be controlled through geometric dimensions. This circuit is the subject of a patent application.

The amplifier pallet (full-pallet) couplers also include hybrid 3dB couplers as part of the multi-layer stripline circuit. The resultant output of the coupler assembly is two pairs of equal and opposite phase signals 90 degrees out of phase (that is, a set of signals at 0° and 180°, and a set of signals at 90° and 270°).

Transistors Q1 and Q2 are Lateral N-Channel Broadband Push-Pull Power MOSFETs. One side of the amplifier is described.

Components C6 through C11 and C52 along with the associated printed circuit traces form the matching network to the gate of the push pull transistor Q1. L2 and R2 along with L3 and R3 are low frequency parasitic arrestors. Similarly, C14 through C15 and C53 along with associated stripline traces provide output matching on the drain of the device. C6, C8, C16 and C18 also provide DC blocking of the supply and bias voltage. C7 is factory adjusted for a flat frequency response from 470 to 860 MHz.



DC power enters the module through a screw terminal connection and is fed to the main circuit board through a series of jumpers. 28V is fed to the drains of the FETs via L5 and L6 with bypass capacitors C13, C25, C20, C22 and C28. Bias for the devices is via L1/L4 with bypass capacitors C1, C2, C5 and C12. The bias voltage is adjusted via R12 and R11, from a regulated source provided by Ul. R12 sets the overall bias and R11

provides adjustment for balance between Q1 and Q2. Thermistors R21 and R22 provide thermal stability for the bias.

MODULE INTERFACE BOARD.

This PC board is located on the rear of each PA module. The RF input and DC input to the module enters via this interface board. Four fuses are located on this board. Three fuses are in line with the 3 output PA pallets and one with the front end, IPA and driver modules. These fuses serve to protect the circuitry from damage in the event of a device failing in the short circuit condition. This is part of the “soft failure" mechanism of the PA modules. Because the normal failure mode of a transistor is a short circuit, and we desire to keep the rest of the PA module functioning in the event of a failure, the fuse effectively disconnects the failed circuit from the regulator, allowing it to supply the rest of the module.
The interface board performs a number of other signal routing functions. Various signals from the different stages of the module are routed through this board to connectors. In the case of the MX1000, many of these signals are not routed any further, but are present on the connector (J3).

3-WAY SPLITTER

The three-way splitter is a stripline implementations of a 1.76dB hybrid/3 dB hybrid combination. It is a mechanical structure consisting of 3 PC boards sandwiched together to form the stripline structure. The middle layer board thickness along with the trace locations determine to the largest extent the coupling. J4 feeds a 1.76dB splitter. The input power to this splitter is divided 1/3 – 2/3 between the two outputs. The 1/3 output is fed to J3 and the 2/3 output is fed to a further 3dB hybrid coupler. The two outputs of this coupler are fed to J1 and J2. The termination load for the reject port of the 1.76dB splitter is at the far end of the board from J4 and the termination load for the 3dB coupler is located at the edge of the board between J2 and J3. J5 is connected to a directional coupler on the input to the splitter and is not used in this configuration.

3-WAY COMBINER

The three-way combiner is essentially the mirror of the 3-way splitter. J1 and J2 are coupled to the inputs of a 3 dB hybrid coupler. The output of this combiner is fed to the input of a 4.77dB hybrid coupler along with the input from J3. The output of this coupler appears at J4. R6 serves as the balance load for the 3dB coupler while R7 serves as the balance load for the 4.77 dB coupler. Each of the inputs to this combiner have a directional coupler and detector circuit that feeds a DC sample of the output of each pallet to the sensing circuitry on the front-end module. As well, a directional coupler on the output of the combiner has detectors for both the forward and reflected power samples of the output. All the information fed back to the front-end appears at J11. Additionally, a second directional coupler provides an RF sample that is fed to a front panel test point via J5.

3. TESTING AND TROUBLESHOOTING

Basic troubleshooting of a PA module is as follows. The front panel LED is extinguished if one or more output amplifier pallet levels are lower than nominal preset level. As mentioned earlier, if the drive is removed from the module(s), the output of the amplifiers also satisfy this condition and thus the LED will be off. In this case, there is nothing wrong with the amplifier. Therefore, if all the LEDs are off, the first place to look is at the output of the exciter.

If a fault condition exists (LED off) on a single module, the first place to check is the PA module interconnect board where all the fuses are installed. A blown fuse will most often indicate a defective amplifier pallet. Most times, this will be the problem and replacing the defective amplifier and fuse will rectify the problem. If, however, there are no blown fuses, there are other areas to check.

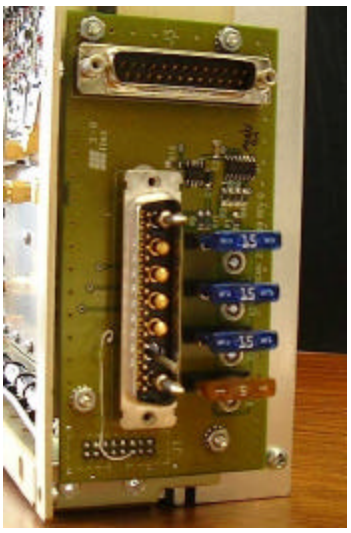


Figure 6: Fuses

The front panel current meter will give an indication of the current drawn by the modules in comparison to one another both under drive conditions and under static bias conditions. Check the current under drive conditions for overdrive situations and under static bias conditions (no drive) for amplifier stage failure.

Check for potential connector problems causing either no drive to a module (input connector) or VSWR (output connector) problems. Also, if you suspect an over temperature condition, be extremely careful when pulling out a module as the heatsink may be too hot to hold onto comfortably.

The following procedures are essentially the same procedures used during factory testing. Basically, if there is no suspected problem with a particular stage, we would recommend not performing these procedures.

FRONT-END PREAMP

- Short Pin J4-10 to ground (this can be accomplished by placing a small jumper across J4-10 and J4-8). This simulates a good thermal switch.
- Connect a +28V power supply to E1 and ground.
- Apply a 0dBm (1mW) RF input to the amplifier.
- Turn R25 fully clockwise. The preamp should have minimum gain (approx. 7dB). Adjusting R25 from one extreme to the other should vary the gain 4dB.
- Check RF output telemetry. There should be 1.5V ±0.5V at J3-12.
- Check the RF input telemetry. There should be 1.0 ±0.2 V at J3-13.
- Check the RF attenuator voltage telemetry. There should be 5.4V ±0.2V at J3-1
- Check Thermal switch status indication. J3-4 should be 0V.
- Remove the jumper from J4-10 to J4-8. (This simulates the thermal switch opening). The voltage at J3-4 should be high (4 Volts ±0.5V) and J3-1 should be 0V.
- Replace the jumper across J4-10 and J4-8.
- RF Mute check: Connect a variable supply, to J3-2. Gradually increase the voltage until the gain drops by 30dB or more. The applied voltage should be approximately 2.5 volts.
- Reflected Power Cutback check: Connect the variable supply to J4-9. Increase the voltage gradually until the gain drops by 30dB or more. The voltage should be approximately 4.0Volts ±0.2V. This same voltage should also be present at J3-14. J3-6 should be 4.0 volts.
- Overdrive Cutback check: Connect the variable supply to J3-7. Increase the voltage until the gain drops by 30dB or more. The voltage should be 7 volts ±0.5V. The voltage at J3-11 should be the same and the voltage at J3-7 should be 4.0 volts.
- Set the adjustable supply to 2 volts. Connect this voltage to J4-1, J4-3 and J4-5 simultaneously. J2-6 and J3-5 should be high. Disconnecting any one or more of J4-1,3 or 5 should cause both J2-6 and J3-5 to go low (0V).

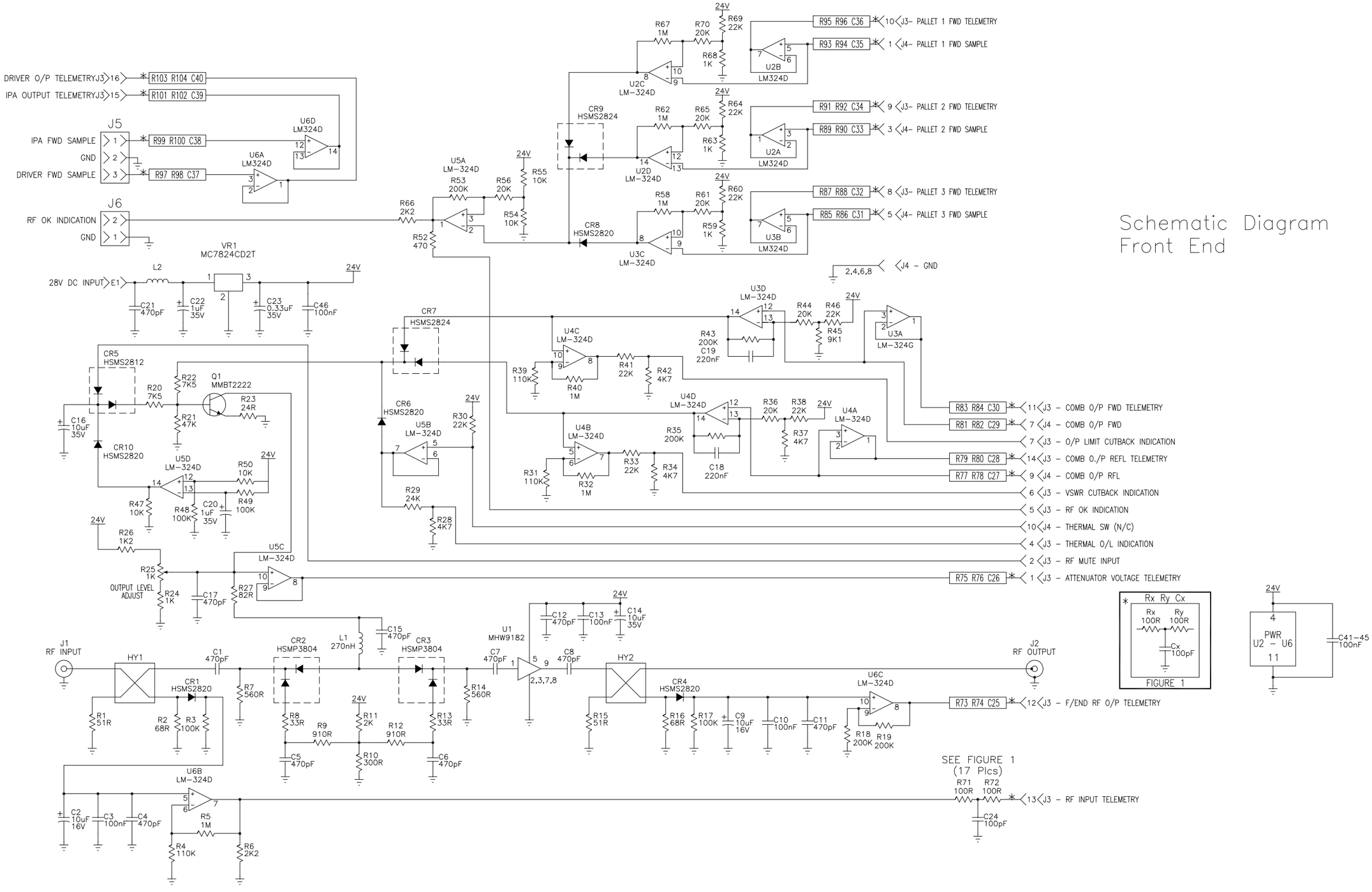
INTERMEDIATE AMPLIFIER (IPA) BENCH TEST PROCEDURE:

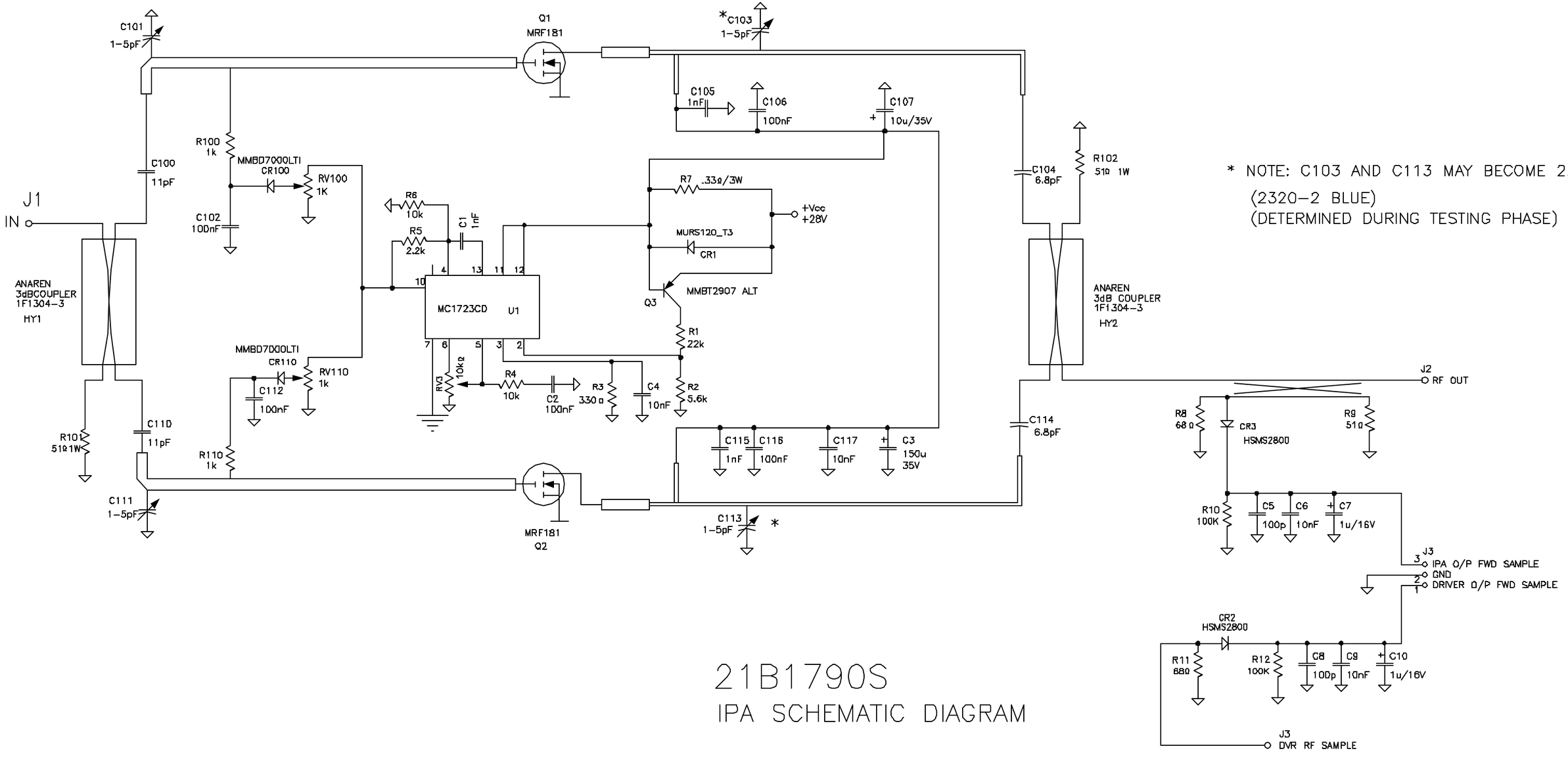
This amplifier must be mounted on a properly sized heatsink for testing.

- Connect a suitable load to the output of the IPA.
- On the IPA under test, set RV200 fully clockwise and set RV110 fully counter-clockwise.
- Set variable power supply to 28.0 volts and set its current limit to 1 ampere.
- Apply the +28V to the feedthrough capacitor of the IPA shield box.
- Adjust RV3 to achieve 6.5 ±0.2 volts at the junction of R5 and RV100.
- Adjust RV200 to achieve total current draw of 500 ±20 mA.
- Check that the junction of R100 and CR100 measures between 3.5 and 5.5 volts.
- Adjust RV110 to raise total current draw to 1000 ±50 mA.
- Check that the junction of R110 and CR110 measures between 3.5 and 5.5 volts.
- Increase the power supply current limiting to 2.2 Amps.

- Increase RV3 clockwise slowly and check that the maximum current limits itself at 1.6 ±0.1 Amp but do not allow current to go above 2 amps while performing this test.
- Reset RV3 to achieve 6.5 ±0.2 volts measured at the junction of R5 and RV100.
- Check balance of the two transistors with a voltmeter connected between the hot sides of C105 and C115; difference voltage should be less than 3 mV.
- Apply RF drive (max. +18dBm to IPA) and adjust C101, C103, C111, and C113 for minimum frequency response ripple and flat response. Gain should be a minimum of 15 dB with maximum variation less than 0.5 dB over the frequency range 470 MHz through 860 MHz (Note: IPA output will then be about +33dBm or 2 Watts, so make sure you properly protect your test equipment).
- If roll off at the higher frequencies prevents meeting this gain-bandwidth specification, it may be necessary to replace either C103 or C113 or both with a higher value; use variable capacitor made by Johanson, part # 16E2320-2, which is 2.5 to 10pF.

Schematic Diagram
Front End





* NOTE: C103 AND C113 MAY BECOME 2.5-10pf
(2320-2 BLUE)
(DETERMINED DURING TESTING PHASE)

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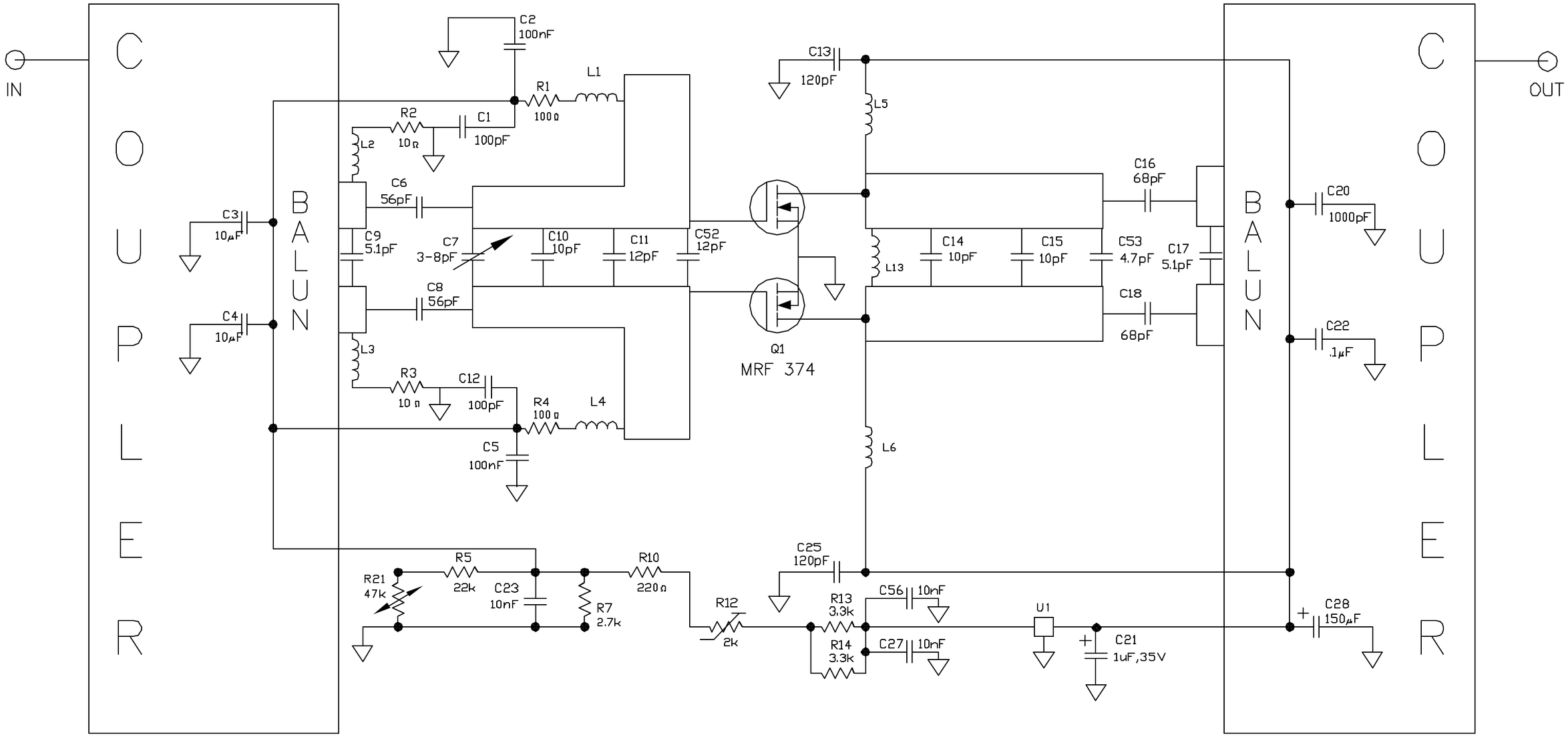
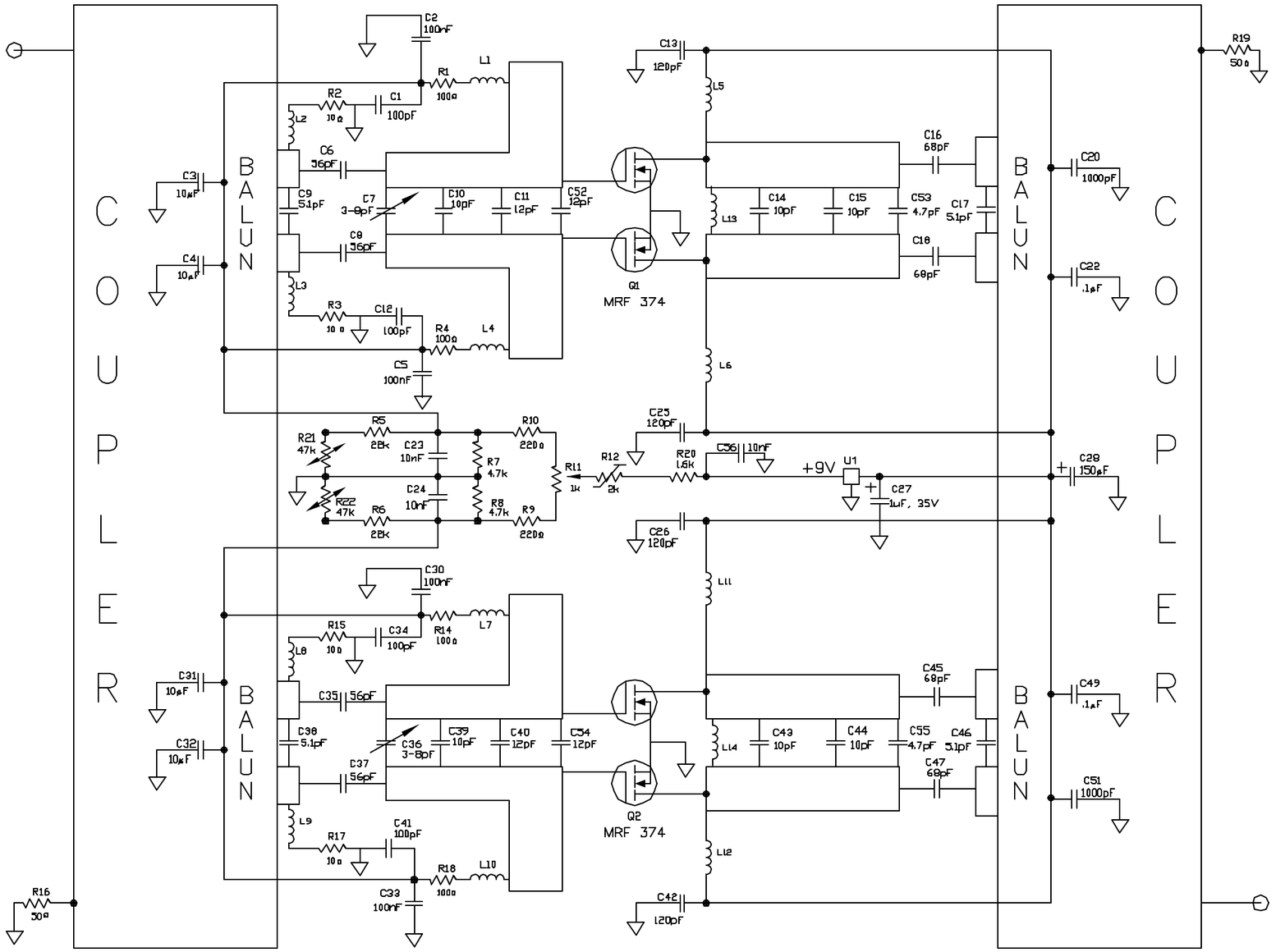
IPA SCHEMATIC DIAGRAM



21B1751S

SCHEM—HALF PALLET



LAST
C 56
R 22
L 14
Q 2

MISSING
C 19
C 21
C 29
C 48
C 50
R 13

21B1639S
SCHEM– PALLET AMPLIFIER

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LIST OF FIGURES

1. INTRODUCTION

The following description, while described as the module housing for the transmitter, in essence, comprises the additional assemblies and circuits that are not included in the other assemblies described in this manual. They include such assemblies as the Blower, the 4-way combiner and reject load assemblies for the overall output, the various interface circuitry and the protection circuitry. The “housing” is basically the assembly that brings all these items together.

2. BLOWER REPLACEMENT

The Blower is located on the top of the module housing. It is accessible through the top of the transmitter. The blower is a backward curved motorized impeller. The motors have no adjustments and need no maintenance. The blower motor bearing life should be on the order of 100,000 hours. Should the blower fail for any reason, the replacement is relatively simple. The entire blower and motor assembly can be removed through the top of the cabinet.

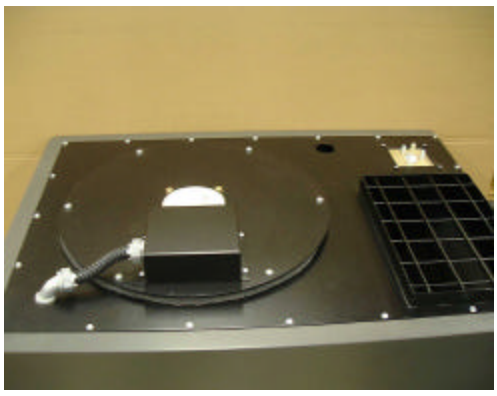


Figure 1: Roof of Transmitter

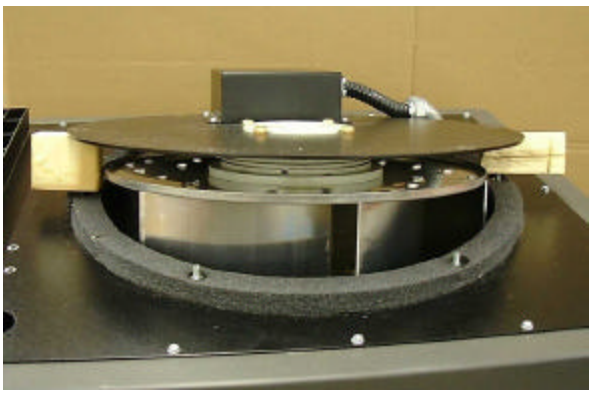


Figure 2: Access to Blower

3. COMBINER AND REJECT LOAD

The 4-way combiner used in the transmitter is basically a combination of three 3dB hybrid couplers. Two couplers form the first level of combining and a third combines the outputs of the first two for the final output. These combiners require balancing loads, or reject loads. The loads

are located in the module housing on an assembly similar to the module assembly. The Reject load assembly is within the cooling air plenum and comprises all three reject loads for the combiners. This reject load assembly is not removable when the transmitter is under power and as such incorporates SMA connectors and is held in place additionally by screws through the rear of the module housing. A sample of the input to each of the loads is provided on the front panel of the reject load assembly. These samples can be used for setting up of the 4-way splitter. Phase and gain of each power amplifier signal path can be adjusted to minimize the power in these reject loads.

4. THERMAL SWITCH AND AIR SWITCH

THERMAL SWITCH

The thermal switch is located on the air duct between the module housing and the blower. It can be accessed by opening up the control panel. The thermal switch, through its mounting on the air duct essentially monitors the outgoing air temperature of the module housing. The metal in the duct itself serves to 'average' the temperature in the duct. It is connected to the TEMP interlock circuitry in the control electronics.

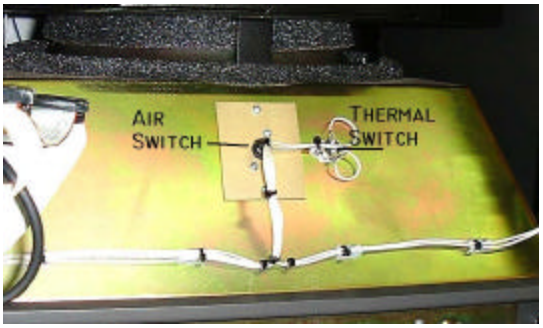


Figure 3: Thermal Switch/Air Switch Location

AIR SWITCH

The Airflow switch consists of a power resistor mounted back to back with a thermal switch. The air that flows through the transmitter flows across this assembly, cooling the resistor. If the airflow is compromised, the resistor is not cooled properly and thus heats up. At a certain temperature, the thermal switch will open, shutting off the power supplies and thus protecting them from damage. ***The thermal switch mounted on the resistor should not be confused with the transmitter thermal protection.***

The air switch is designed to detect the presence of air flow throughout the normal operating temperature range of the transmitter and in fact operates, under normal conditions at a much higher temperature than the maximum operating temperature of the transmitter itself. The sole purpose is to detect the presence of air flow, and in the case of reduced, or no air flow, the resistor/thermal switch combination overheats and shuts off the supplies. **WARNING: AC VOLTAGE IS PRESENT ON THE AIR SWITCH RESISTOR. DO NOT REMOVE THIS ASSEMBLY WITHOUT FIRST DISCONNECTING AC FROM THE TRANSMITTER.**

TABLE OF CONTENTS

1. INTRODUCTION

The 4-way splitter provides four evenly balanced, equal amplitude, properly phased signals to each of the PA modules in the transmitter. The intention is to provide the ability to fine match the phasing and gain of the amplifiers such that they combine with the minimum of reject power. It has been found that normal production tolerances do not cause wide variations in phasing between amplifiers and thus the control over the output phase is limited to a relatively narrow range. At different channels, some touch-up of phasing might be desireable in order to finely balance the PAs, although, it is not absolutely necessary.

2. CIRCUIT DESCRIPTION

The RF enters this splitter via J5 and is applied to a PIN attenuator circuit comprised of CR1 and CR2 and associated circuitry. The attenuator voltage to this circuit is applied through L1 via buffer amplifier/ inverter Q1. A higher voltage at E2 results in more attenuation through the PIN attenuator. E2 is fed from the transmitters AGC/VSWR circuitry.

The signal at the output of the PIN attenuator is fed to a hybrid 3dB coupler HY1. The two outputs from HY1 are fed to two more hybrids HY2 and HY3. The result is four outputs, equal in amplitude but differing in phase. Each of the four signals is then passed through a phasing network and a further PIN attenuator for the purpose of balancing the transmitter phase and gain overall. All four balancing circuits are identical therefore only the circuit that supplies PA1 will be described.

The phasing adjustment is accomplished by using two varactor diodes CR100 and CR101, connected to the output ports of a 3dB hybrid coupler HY4. If the impedance of these pure reactances is kept equal, the signal is reflected back through to the isolation port of the hybrid with a change in phase and minimal loss. The reverse bias on the varactor diodes is controlled through R101 and R102/R103. Attenuation adjustment is controlled by varying the bias across CR102 via R108 through R111. This has the effect of shunting some signal to ground. R110 controls the coarse level adjustment and R109 controls the fine adjustment. U1 is a signal buffer amplifier. The signal is then passed through a final coupler which provides a sample to a detector circuit and to the output connector J1.

3 TEST AND TROUBLESHOOTING

GENERAL

Because the splitter, in its normal operation provides the phasing and balance for the modules in the transmitter, often times, if the balance between modules is incorrect, the splitter is the first suspected problem area. One must be very careful troubleshooting under these conditions. What may be suspected as a gain or phase imbalance can simply be a problem with a PA module. In addition, in the field it may be difficult to quantify phase relationships between signals without a network analyzer. As mentioned elsewhere in this manual, the transmitter has been delivered to site in a fully functioning condition. As designed, the phasing controls in the splitter circuitry will allow up to approximately 30 degrees of phase

shift. The bulk of the phase relationship between the signal is developed within the hybrid splitters themselves. Additionally, the gain controls on the splitter is only for fine matching of the module outputs.

TROUBLESHOOTING

If trouble is suspected with the splitter unit itself, the following checks may be done to pinpoint the cause of failure.

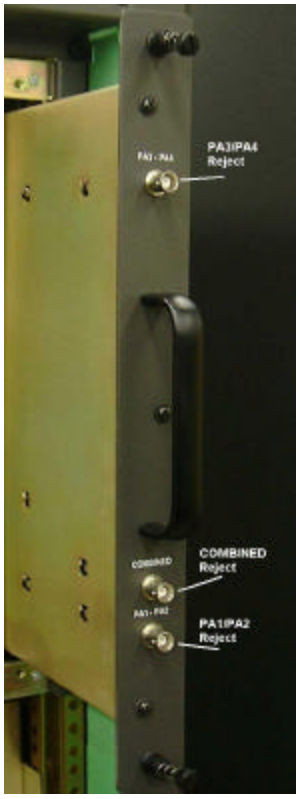
- Turn off the transmitter
- With +12V connected to E1, verify that there is +8V (±0.1V) at pin 3 of VR1.
- Disconnect the AGC signal to E2.
- With signal applied at the input use a spectrum analyzer, to verify that there is signal at each of the four output ports. Note; if one of the output ports is significantly lower (10dB) than the rest, this may indicate a problem in that particular circuitry.
- With a variable supply connected to E2, verify that the output levels of each port drop at least 30dB with a voltage of 3.0 Volts.

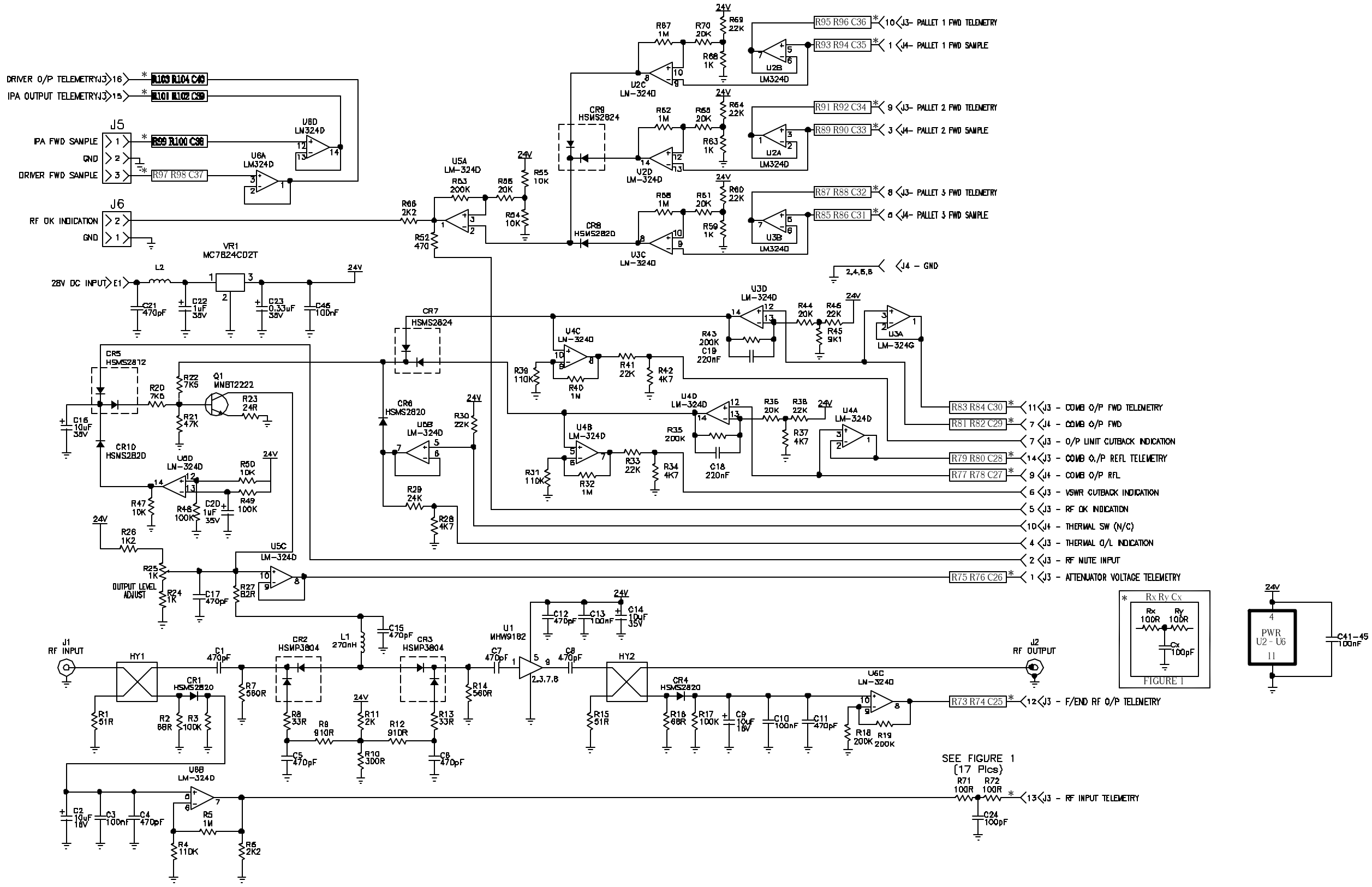
SPLITTER SETUP

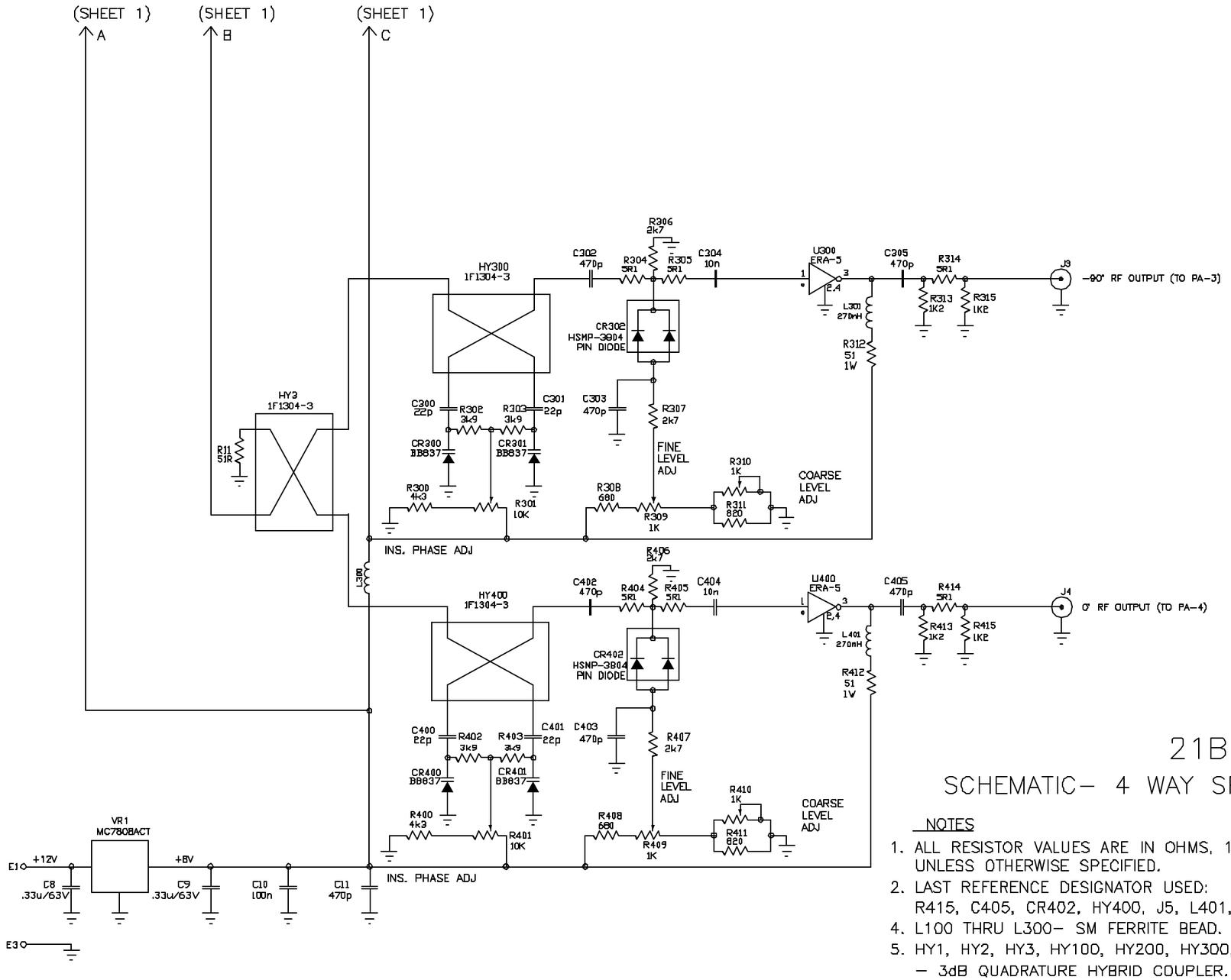
Fine balancing of the splitter outputs is accomplished with the transmitter operating at full power. Refer to Figure 1 below. Firstly, the phasing and gain balance must be done between the inner level of combining, that is between PA1 and PA2 and between PA3 and PA4. Then, carefully, the phasing must be done between the PA1/PA2 combination and the PA3/PA4 combination.

The simplest way to balance the phase and gains is to monitor the reject load power. On the front of the reject load assembly, there are various sample ports for such purpose. The relative phasing and gain is adjusted to minimize the signal level at these ports.

- Balance all four PA output levels. This is best done with a spectrum analyzer connected to each sample port in turn and adjusting R110, R210, R310 and R410 to adjust the level of its respective PA module output.
- With the transmitter operating at full power, connect a spectrum analyzer to reject load sample port for PA1/PA2. See figure 3.
- Adjust either R101 or R201 (one or the other, not both) to minimize the measured signal at this sample port.
- Connect the spectrum analyzer to reject load sample port for PA3/PA4.
- Adjust either R301 or R401 (one or the other, not both) to minimize the measured signal at this sample port.
- Connect the spectrum analyzer to the transmitter overall reject load sample port.
- Carefully adjust phase adjustment pots R101 AND R201 together to minimize the measured signal at this sample port (alternately R301/R401 pair can be adjusted instead).
- Repeat the above steps to further reduce reject levels. Note: do not use the gain adjustments to attempt to minimize reject load power.




DRIVER O/P TELEMETRY J3 16
IPA OUTPUT TELEMETRY J3 15
J5
IPA FWD SAMPLE
GND
DRIVER FWD SAMPLE
J6
RF OK INDICATION
GND
R103 R104 C40
R101 R102 C39
R99 R100 C38
R97 R98 C37
U6D LM324D
U6A LM324D
VR1 MC7824CD2T
28V DC INPUT E1
L2
C21 470pF
C22 1uF 35V
C23 0.33uF 35V
C45 100nF
24V
CR5 HSMS2812
CR10 HSMS2820
Q1 MMBT2222
R20 7K5
R22 7K5
R23 24R
R21 47K
C16 10uF 35V
U5D LM-324D
R50 10K
R47 10K
R48 100K
C20 1uF 35V
R49 100K
R26 1K2
R25 1K
OUTPUT LEVEL ADJUST
R24 1K
C17 470pF
U5C LM-324D
R27 82R
U5A LM-324D
R53 200K
R55 10K
R54 10K
R56 2K2
R52 470
CR7 HSMS2824
CR6 HSMS2820
U6B LM-324D
R30 22K
R29 24K
R28 4K7
CR9 HSMS2824
CR8 HSMS2820
U2C LM-324D
U2D LM-324D
U3C LM-324D
R67 1M
R70 20K
R69 22K
R68 1K
R62 1M
R65 20K
R64 22K
R63 1K
R58 1M
R61 20K
R60 22K
R59 1K
U2B LM324D
U2A LM324D
U3B LM324D
R95 R96 C36
R93 R94 C35
R91 R92 C34
R89 R90 C33
R87 R88 C32
R85 R86 C31
10 J3- PALLET 1 FWD TELEMETRY
1 J4- PALLET 1 FWD SAMPLE
9 J3- PALLET 2 FWD TELEMETRY
3 J4- PALLET 2 FWD SAMPLE
8 J3- PALLET 3 FWD TELEMETRY
6 J4- PALLET 3 FWD SAMPLE
2,4,6,8 J4 - GND
U3D LM-324D
U4C LM-324D
U4D LM-324D
U4B LM-324D
U3A LM-324G
U4A LM-324D
R44 20K
R45 22K
R45 9K1
R43 200K
C19 220nF
R39 110K
R40 1M
R41 22K
R42 4K7
R36 20K
R38 22K
R37 4K7
R35 200K
C18 220nF
R31 110K
R32 1M
R33 22K
R34 4K7
R83 R84 C30
R81 R82 C29
R79 R80 C28
R77 R78 C27
11 J3 - COMB O/P FWD TELEMETRY
7 J4 - COMB O/P FWD
7 J3 - O/P LIMIT CUTBACK INDICATION
14 J3 - COMB O/P REFL TELEMETRY
9 J4 - COMB O/P REFL
6 J3 - VSWR CUTBACK INDICATION
5 J3 - RF OK INDICATION
10 J4 - THERMAL SW (N/C)
4 J3 - THERMAL O/L INDICATION
2 J3 - RF MUTE INPUT
R75 R76 C26
1 J3 - ATTENUATOR VOLTAGE TELEMETRY
J1 RF INPUT
HY1
CR1 HSMS2820
CR2 HSMP3804
CR3 HSMP3804
L1 270nH
C1 470pF
C15 470pF
R1 51R
R2 68R
R3 100K
R7 560R
R8 33R
R8 910R
R11 2K
R12 910R
R13 33R
R14 560R
R10 300R
C5 470pF
C6 470pF
U1 MHW9182
2,3,7,8
C7 470pF
C8 4.7pF
C12 470pF
C13 100nF
C14 10uF 35V
HY2
CR4 HSMS2820
R15 51R
R16 68R
R17 100K
C9 10uF 16V
C10 100nF
C11 470pF
U6C LM-324D
R18 200K
R19 200K
J2 RF OUTPUT
R73 R74 C25
12 J3 - F/END RF O/P TELEMETRY
U6B LM-324D
C2 10uF 16V
C3 100nF
C4 470pF
R5 1M
R4 110K
R6 2K2
SEE FIGURE 1 (17 Plcs)
R71 100R
R72 100R
C24 100pF
13 J3 - RF INPUT TELEMETRY
Rx Ry Cx
Rx 100R
Ry 100R
Cx 100pF
FIGURE 1
PWR U2 - U6
C41-45 100nF



21B1779S2

SCHEMATIC– 4 WAY SPLITTER

NOTES

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%, UNLESS OTHERWISE SPECIFIED.
2. LAST REFERENCE DESIGNATOR USED: R415, C405, CR402, HY400, J5, L401, VR1
4. L100 THRU L300– SM FERRITE BEAD.
5. HY1, HY2, HY3, HY100, HY200, HY300, HY400 – – 3dB QUADRATURE HYBRID COUPLER.

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1. INTRODUCTION

MX1000 POWER SUPPLY

The MX1000 power supply consists of two transformers, each with dual (isolated) secondary windings. Each power amplifier module is fed from a 60A linear voltage regulator. The output voltage of each regulator is 28 Vdc. The input of the regulator assembly fed from the secondary of the ferro-resonant transformer secondary winding is 35 Vac. The AC power to the transformers is supplied via a contactor on the AC distribution board. This contactor is controlled through the transmitter's control board, ensuring that all interlock and overload conditions are observed.

LINEAR REGULATOR

The 60A linear voltage regulator is a 'generic' term for the entire plug-in assembly that performs more than simply a regulation function. In essence, the Linear regulator assembly is an independent power supply (less the transformer), performing rectification, regulation and self protection. Assembly is accessible through the rear of the transmitter and can be removed from service without turning off the transmitter. (*For the purposes of description in this text, the 'front' of the linear regulator will be designated as the end with the handle, which is in actuality, located at the rear of the transmitter*). Obviously, removing a regulator will disable the associated power amplifier and result in a lower output power. The AC input to the regulator is fed through the rear of the regulator and the control, status and telemetry connections as well as the DC output fed to the PA is located at the front of the module.

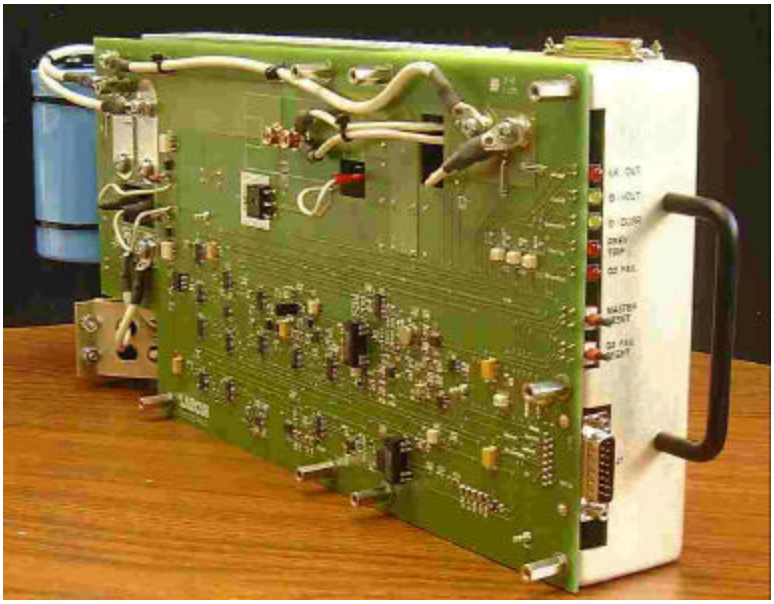


Figure 1: Linear Regulator Assy.

2. CIRCUIT DESCRIPTION

The linear regulator assembly incorporates the following circuitry:

- A semiconductor-controlled rectifier bridge, the input filter capacitor and power resistors (Q1, C1 and R63, R64 respectively). This circuitry is shown in block A on the schematic diagram.
- The Voltage Regulator itself (block B).
- The control circuitry (block C,D,E,F,G)which provides a few different functions including over-current protection, over-voltage protection and power-on and reset functions.

RECTIFICATION

Refer to block 'A' on the schematic diagram 40D1680S.

Rectification of the AC from the transformer secondary winding is performed by a semiconductor-controlled bridge (SCR) rectifier, Q1. Capacitor C1 performs the filtering function. The advantage of using a semi-controlled rectifier bridge instead of a conventional rectifier bridge is significant. In normal operating conditions the bridge is constantly on because the opto-coupled triacs, U33 and U34 are active. Thus Q1 behaves as a conventional rectifier bridge. In the case of serious damage to the regulator unit the control can isolate the transformer secondary from the rest of the transmitter by turning off the bridge (turning on U32). The power resistors R63, R64 are bleeder resistors, to safely discharge filter capacitor C1, when the unit is pulled out of the transmitter.

REGULATION CIRCUITRY

Refer to block 'B' on Schematic Diagram 40D1680S.

The voltage regulator circuitry consists of a low current linear voltage regulator, U1 utilizing an external high power pass transistor, giving the regulator the required current capability for this application. The combination of pnp transistor Q3 and npn power transistor Q2, creates the equivalent of a high power npn pass transistor.

OR gate U25d activates, as required by the various overload commands from the control circuitry, The output of this gate is applied to the internal shut down circuitry of U1-2. The command for over-voltage shutdown is applied through U25d-12 and the command for over-current is applied through U25d-13.

The output voltage setting for this regulator is provided by R18, R19 and R20. Additional regulator output filtering is provided by C8 through C12

CONTROL CIRCUITRY

Control Circuit Operation

a. Over-current.
Whenever an over-current or short-circuit condition occurs the control circuit will shut down the output of the regulator, wait for 3 seconds and try to restart. A fault is indicated by two LEDs lighting up, a red LED (previous trip) which latches on showing that a trip has been recorded and counted and a yellow LED (over-current) which is on for the 3 second shutdown duration only. After three trips a red LED (lockout) will come on until a reset command is received, resetting all counters and restarting the cycle.

b. Over-voltage
The operation of the overvoltage protection circuitry is much the same

Figure 2: Front Panel Indicators

as that of the overcurrent circuitry with a couple of exceptions. One of the common causes of failure in a series linear regulator is the short circuit of the series pass transistor. Once the pass transistor has shorted, there is no way to shut down the regulator output (to prevent over-voltage damage to the power amplifiers), hence the SCR bridge that effectively disconnects the entire regulator from the transformer secondary. When the over-voltage protection circuitry detects an over-voltage condition the circuit shuts down the output of the regulator for 3 seconds and then tries to restart the regulator. The fault is shown by two LEDs lighting up, the red LED (previous trip) which latches on showing that a trip has been recorded and counted and a yellow LED (over-voltage) which is on for the 3 second shutdown duration only. After three trips a red LED (lockout) will come on until a reset command is received, resetting all counters and restarting the cycle. In the event that the series pass transistor short circuits, turning off the regulator IC will have no effect. In this case, additional control circuitry will shut down the rectifier bridge isolating the regulator. A red LED (Q2 short-circuit) comes on. A local reset switch for this circuitry is available for restarting the regulator (if the pass transistor is indeed short circuited the circuitry will again shut down the regulator showing the same fault condition). In this case the regulator must be serviced and Q2 replaced. Until the necessary steps are taken to do this, the damaged regulator is safely isolated from the rest of the transmitter.

c. Power ON Reset and Master Reset

The regulator assembly utilizes control voltages supplied by the transmitter control power supplies. These are supplied via a connector on the front of the regulator module. In the event that these 'auxiliary' voltages are removed from the circuit the regulator control circuit shuts down the rectifier bridge, isolating the regulator. This situation could occur if either the auxiliary power supply fails or if the 15 pin control connector is disconnected leaving the unit without the auxiliary voltages. When the voltages are reapplied, the circuitry sends a power-on reset pulse, setting all counters and protection circuits back to original conditions. The same effect occurs when the master reset switch is pressed and released.

Over-current protection (refer to block C on schematic diagram 41D1680S)

Along with current transducer S1, block C on the schematic contains the over-current protection. The current information from S1 is amplified and compared to a threshold determined by the setting of R51. When the current information reaches the threshold level, the output of comparator U6 goes high (0 to 10V). U3 is a buffer amplifier that is used to distribute the over-current status to various other circuits within the regulator (see table)

Pin (U3)	Output function
pin 10	front panel status LED (over-current) and via inverter U20d to over-current event counter U14a.
pin 2	activates the OR gate U25d shuting down the regulator.
pin 4	starts the timing circuitry (see block E).
pin 6	activates the locking circuitry.

Whenever an over-current event happens, the comparator output toggles (U6-6) and the positive level through U3 (pin 6) is transferred through the closed contacts of K1 to the gate of Q7. Q7 turns on and R35, R41 and R43 form a voltage divider latching U6 into the 'tripped' state. When a reset command is issued relay K1 is activated, the gate of Q7 discharged and the circuit comes back to its original state.

Over-Voltage Protection (refer to Block D on Schematic diagram 41D1680S)

Over-voltage condition is sensed by U4. This is a programmable voltage sensor. The threshold over-voltage reference is set by the voltage divider consisting of R5, R21 and R22 (the threshold is set by the following formula: V= 2.6 [1+ (R5+R21)/ R22]). An over-voltage condition causes

the output of U8 (pin8) to go high. This triggers flip-flop U10a. Once set, the flip-flop output (pin 6) stays high until a reset pulse clears the flip-flop. The output of the flip-flop activates a yellow LED (over-voltage indicator CR5), the over-voltage counter, U14b, the 'trip recorded' circuit of U29b and the regulator shutdown circuitry of U25d.

The over-voltage circuitry is reset by U12 as follows: Once the over-voltage disappears, the output of U4 returns to zero, pin 5 of AND gate U2b becomes logic 1. The signal at pin 4 of this gate is connected to the output of U10a (already set to logic 1). After a delay determined by the timing circuitry (see block E), pin 3 of U2b goes high triggering U12 and resetting U10a. The regulator will restart. If the fault is still present the over-voltage trip will re-occur and event counters will allow three overloads before the lock out circuitry shuts the regulator down.

In the event that the regulator is unable to shut down the output due to pass transistor short circuit, the over-voltage shutdown circuitry will shut down the regulator but it will have no effect on the output voltage. The output of U4 cannot return to zero in this case and pin 13 of U2a is high (via inverter U20e) instead of pin 5 of U2b. After the timing circuitry delay, pin 1 of AND gate U2a is set high, thus causing its output to go high. The output of flip-flop U10b is set and stays high until reset via S2 (Q2 FAIL RESET). The output of U10b (pin 10) activates solid state relay U32 . This removes drive from U33 and U34, turning OFF the bridge. The regulator circuitry is now fully isolated from the secondary of the transformer and the rest of the transmitter.

Timing and Counting Circuitry (refer to Block E on Schematic diagram 41D1680S)

When overloads occur OR gate U25C triggers timer IC U26. This OR gate is triggered on pin 10 in the case of over-voltage trips and on pin 9 in the case of over-current trips. Once triggered the timer releases a train of pulses to counter U28b. AND gates U30a, U30b and U31a monitor the outputs of the counter and when all outputs are high U31a triggers the internal reset circuitry to restart the regulator.

If the overload event was an over-current, U31d enables timer IC U16 (see block G). This IC issues a pulse activating Q4, opto-coupler U15 and relay K1. The relay discharges the gate of MOSFET Q7, releasing the over-current protection. Since relays are inherently slow devices, opto-coupler U15 holds the shutdown pin of the regulator U1 high during the reset period. This prevents serious over-current conditions on the output of the regulator from causing damage during this transition period when the over-current protection circuit is resetting.

If the overload event was an over-voltage the output of U31a removes the shutdown condition from AND gates U2a/U2b allowing the regulator to return to operation.

Each of the inputs to U25c are driven by an AND gate (U30d and U30c). These gates form part of the three-shot lock-out circuitry. Binary counter U14a counts three over-current events and U14b counts three over-voltage events. As long as the number of trips is less than three the outputs of U31c and U31b are logic 0, the outputs of inverters U27e and U27d are logic 1 and over-current or over-voltage trips are transmitted through the AND gates U30d/U30c. Once either of the event counters reaches a count of three, the output of AND gate U31c or U31b goes high and the internal reset circuitry is disabled . When the overload count reaches three LED CR8 (lockout) turns on. A master reset is required to restart the regulator circuitry in this case.

Power-On and Master Reset Circuit (refer to Block F on Schematic diagram 41D1680S)

Whenever the control power supply from the transmitter (+ 12v) is disconnected and reconnected to the circuitry, a power-up master reset is initiated. Q5 is activated after a delay given by capacitors C36-C39 and divider R78, R74. K2 triggers the timer U18 which issues a mater reset pulse. K2 can also be activated directly by pressing and releasing the master reset switch SW1 on the regulator.

Additionally, the main control board of transmitter can issues a reset command on pin 1 of connector J1 (operator pressing tx front panel reset button). This external reset command will only have an effect only if an overload trip has been recorded and is disregarded otherwise. In this case U19 activates relay K2.

3. TESTING AND TROUBLESHOOTING

With the exception of replacing the pass transistor in this circuit, repair of the circuitry on these units in the field is not recommended. Any adjustments provided on the module are for factory settings only. Modification of these settings should not be attempted in the field as damage to other sections of the transmitter may occur.

To remove a regulator module, first unplug the control cable (ribbon cable). This shuts off the regulator. Then unplug the DC cable that feeds the PA module and pull the module out of the housing. Support the bottom of the regulator as the slide mechanism is shorter than the regulator itself and the regulator may drop suddenly, potentially damaging the AC input connector.

NOTES
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%, UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
3. ALL DIODES ARE , UNLESS OTHERWISE SPECIFIED.
4. LAST REFERENCE DESIGNATOR USED: R79, C50, CR12, K2, L34, D7, J2, VR1, S1, SW2.
5. NOT USED: R56, Q6, C2, C3, C17, C34.

A
B
C
D
E
F
G

+5v
R10 91R
R1 91R
R2 100R
U34 MOC3041S
U33 MOC3041S
U32 AQV251A
CR1
CR2
R3 75R 35W
R4 75R 35W
R6 1K 1.6W
R7 1K 1.6W
Vin 32V
AC1
AC2
Q1 M5010012F
GND
C1 82000uF
R63 220,35W
R64 220,35W
R27 200R
U27b MC74AC04D
U27a MC74AC04D
Q2 KSD24510
Q3 TIP36
R15 1K
R16 1K
R18 18K
R19 10K
R20 6K2
U1 MC1723CD
R11 510R
C5 150pF
R13 1K
R14 510R
C4 0.1uF
CR3 1SMB5925BT3
CR4 1SMB5937BT3
C6 10uF
C7 4700uF/50V
C8 4700uF/50V
C9 4700uF/50V
C10 4700uF/50V
C11 4700uF/50V
C12 4700uF/50V
R12 510R
U25d MC74AC32D
S1 LA55-P CURR. TRANSDUCER
+12V -12V
R5 2K
JP1
R21 9K1
R22 1K
C13 1uF 35V
C14 1uF
U4 MC3423D
R23 5K1
R24 5K1
U5 MOC212S
R25 1K
U10a MC74HC109D
U20b
U20C MC74AC04D
C47 820pF
CR5
R26 300R
U22 MOC212S
GND J2-X
CURRENT DIF. VOLTAGE TEL J1-7
Vout 28V J2-X
OVERVOLTAGE J1-11
R75 51K
R76 51K
U20d
U20a MC74AC04D
C46 820pF
R29 51K
U3 MC14050BD
R34 10K
R35 300R
Q7 2NT002LT1
C50 330nF
R39 5K1
U9 LF351D
R40 5K1
R42 2K4
U7 LF351D
R46 1K
R45 3K
R47 24R
R41 510R
R43 510R
R44 1K
U6 LM319H
C18 100nF
R36 150R
R30 51K
R32 51K
R31 51K
K1 836C-1J
R79 100R
C21 330pF
R37 5K1
C20 100nF
R38 200R
R49 10K
R50 10K
VR1
R54 4K7
R48 10K
U8 LF351D
R51 10K
R52 5K6
R53 3K
C19 100nF
U20e MC74AC04D
U12 MC74AC32D
TP1
U17C MC74AC32D
U20f MC74AC04D
CR6
R33 300R
U23 MOC212S
OVERCURRENT J1-5
CURRENT TEL J1-10
+12V J1-4
C42 10uF
U2A MC74AC11D
U2B
U10b MC74HC109D
CR7
R9 300R
U11 MOC212S
TRANS. SHORTCIRC J1-4
S2
TRANS. SH. RESET
R25 1K
R57 20K
R58 20K
C22 1uF
C23 1uF
C27 330nF
R59 10K
U12 LM555CM
C24 100nF
CR10 MMBZ5232BLT1
R60 180K
C25 1uF
C26 1uF
C15 100nF
U26 LM555CM
R28 150K
C16 1uF
U30d MC74AC08D
U25c MC74AC04D
U30c MC74AC08D
U27f MC74AC04D
U28b MC74HC393ADR
U30a
U30b MC74AC08D
U31a 74AC08
U27e MC74AC04D
U27d
C49 10uF
R61 1K
U29a MC74HC109D
U31c MC74AC08D
U14a MC74HC393AD
C44 100nF
C48 10uF
C33 1uF
U29b MC74HC109D
U31b MC74AC08D
U14b MC74HC393AD
U25b MC74AC32D
U27C MC74AC04D
U25a MC74AC32D
U17a MC74AC32D
U17d
U31d MC74AC08D
U17b MC74AC32D
C28 330nF
C29 100nF
R65 51K
R66 100K
C30 1uF
C31 1uF
U16 LM555CM
CR11 MMBZ5232BLT1
U15 MOC212S
R17 1K
Q4 2NT002LT1
U18 LM555CM
R68 10K
C35 330nF
R69 100R
CR12
R67 180K
C32 1uF
K2
SW1
Q5 2NT002LT1
C36 1uF
C37 1uF
C38 1uF
C39 1uF
R78 51K
R70 100R
R55 100R
U19 AQV251A
R71 200R
R74 51K
U2C MC74AC11D
R72 1K
R73 1K5
U21 MOC212S
R62 300R
RESET J1-1
5V J1-6
GND J1-2
GND J1-9
-12V J1-3
C41 10uF
C40 10uF
LOCKOUT J1-12
CR8
R8 300R
U24 MOC212S
R77 300R
CR9

41D1680S
SCH. – LIN. REGULATOR

TABLE OF CONTENTS

1. INTRODUCTION

In order to minimize the amount of wiring in the transmitter, a single circuit board was used to distribute the AC power and various DC control voltages throughout the transmitter. The circuit board is mounted on the AC circuit breakers behind the circuit breaker panel. On later models of the MX1000, the control power supplies are also mounted on this panel.

2. CIRCUIT DESCRIPTION

The AC from the mains terminal block is distributed to the various power supplies and the blower via this board and the breakers. The control power supplies receive their AC power via fuses Fl through F4 on J8 and J9. The three control voltages from these supplies come into the board on J8 and J9 as well. Each of the voltages is monitored by voltage monitor ICs U3, U4, and U5. If one of the voltages fail, the PS1 FAIL or PS2 FAIL LED will illuminate. In addition, these control supply failure signals are routed to the transmitter control board.

Each of the control voltages from the control power supplies is diode-ORed. Note that a single control power supply can power the transmitter on it's own. Dual supplies are provided only for redundancy.

The AC to the transmitter blower and to the two power supplies is routed through circuit breakers CB1 through CB3. The BLOWER ON command is applied to this board on J8-39 from the tx control board. An emergency interlock is provided for interlocking the transmitter to a building fire alarm system. This interlock disables the transmitter blower as well as the power supplies (not the control power supplies). The connections to this interlock are on J7. The interlock can be bypassed via JP1. K6 controls the AC to the contactor relay K3 which provides AC to the blower at J2-2 and J2-3. The AC that supplies the blower, also supplies power to the airflow switch.

The voltage applied to the blower also arms the power supply contactors K1 and K2.

The TX-ON command is applied through J8-37 from the transmitter control board. This signal energizes K4 and voltage is applied to the power supply contactor coils of K1 and K2 via the step start thermal interlock circuits and the breaker auxiliary contacts.

The AC to the power supplies is applied through a step-start circuit to minimize the inrush currents associated with the ferroresonant power supplies. This step start circuitry consists of a resistor in series with the transformer that is shorted out after a predetermined delay period. A solid state relay is used to short the resistors allowing full supply voltage to be applied to the power supplies. In the event of a failure in this timing circuit there is a thermal cutout switch mounted on the step start resistors. These thermals will remove the power to the power supply contactor coils, thus removing power from the supply.

The step start timing circuit for one power supply will be described, the second circuit is identical. When AC is applied to the surge The step start timing circuit for one power supplyresistors, AC is applied to opto isolator U2-3 (U2-4). This opto-isolator applies voltage to the timing circuit consisting of R5 and C5

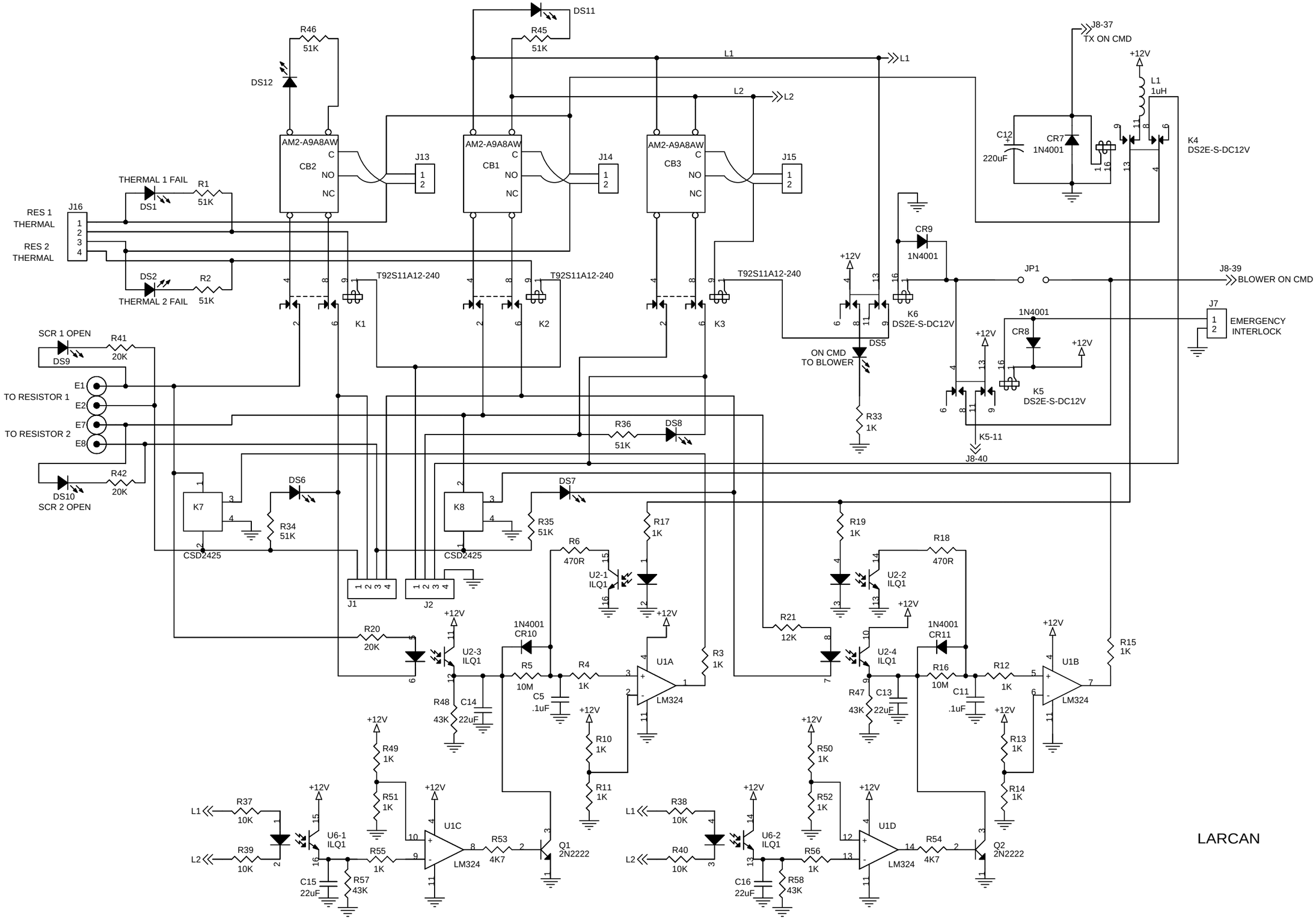
(R16/C11). When the voltage across the capacitor reaches a predetermined level as set by the voltage divider R10/R11 (R13/R14), the output of comparator UlA (UlB) goes high causing the solid state relay K7 (K5) to turn on, shorting out the surge limiting resistors.

3. TESTING AND TROUBLESHOOTING

This board is essentially an interconnect circuit for the transmitter and, as such there are not many circuits on the board to require service.

Much of the troubleshooting that can be done with this circuit is detailed in the installation section of this manual. The troubleshooting can be done by simply observing which LEDs are illuminated and determining where the problem lies. Refer to figure for the location of the LEDs and to the schematic diagram (figure) for their function.

DS 11 and DS12 indicate the presence of AC on the inputs to the circuit breakers CB1 through CB3. DS5 indicates the presence of a blower command. DS8 indicates that the blower contactor K3 is closed. DS6 and DS7 indicate that power supply contactors (K1 and K2 respectively) are closed. DS9 and DS10 are illuminated during the startup inrush limiting period, indicating essentially that the inrush resistors are in circuit. Note that these resistors are provided to limit the inrush caused by the magnetizing current of the ferroresonant transformers and protect the contactors from damage due to these high currents as well as prevent inadvertent breaker trips. Should the inrush circuitry fail to function properly, leaving these resistors in circuit and dissipating power, the thermal cutouts mounted on the surface of the resistors will open, causing the contactors to open. DS1 and DS2 indicate this thermal cutout condition should it occur.


DS11
R45
51K
R46
51K
DS12
L1
L2
J8-37
TX ON CMD
+12V
L1
1uH
C12
220uF
CR7
1N4001
K4
DS2E-S-DC12V
AM2-A9A8AW
CB2
CB1
CB3
C
NO
NC
J13
J14
J15
THERMAL 1 FAIL
R1
51K
DS1
RES 1
THERMAL
RES 2
THERMAL
J16
DS2
R2
51K
THERMAL 2 FAIL
T92S11A12-240
K1
K2
K3
CR9
1N4001
K6
DS2E-S-DC12V
JP1
J8-39
BLOWER ON CMD
J7
EMERGENCY
INTERLOCK
1N4001
CR8
K5
DS2E-S-DC12V
ON CMD
TO BLOWER
DS5
R33
1K
K5-11
J8-40
SCR 1 OPEN
R41
20K
DS9
E1
E2
E7
E8
TO RESISTOR 1
TO RESISTOR 2
R36
51K
DS8
R42
20K
DS10
SCR 2 OPEN
K7
K8
CSD2425
DS6
DS7
R34
51K
R35
51K
J1
J2
R6
470R
U2-1
ILQ1
R17
1K
R19
1K
R18
470R
U2-2
ILQ1
R21
12K
R20
20K
U2-3
ILQ1
1N4001
CR10
R5
10M
C5
.1uF
R4
1K
U1A
LM324
R3
1K
R48
43K
C14
22uF
R10
1K
R11
1K
U2-4
ILQ1
1N4001
CR11
R16
10M
C13
22uF
R47
43K
C11
.1uF
R12
1K
U1B
LM324
R15
1K
R13
1K
R14
1K
R49
1K
R51
1K
R37
10K
R39
10K
U6-1
ILQ1
U1C
LM324
R53
4K7
Q1
2N2222
R55
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R40
10K
U6-2
ILQ1
U1D
LM324
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1K
C16
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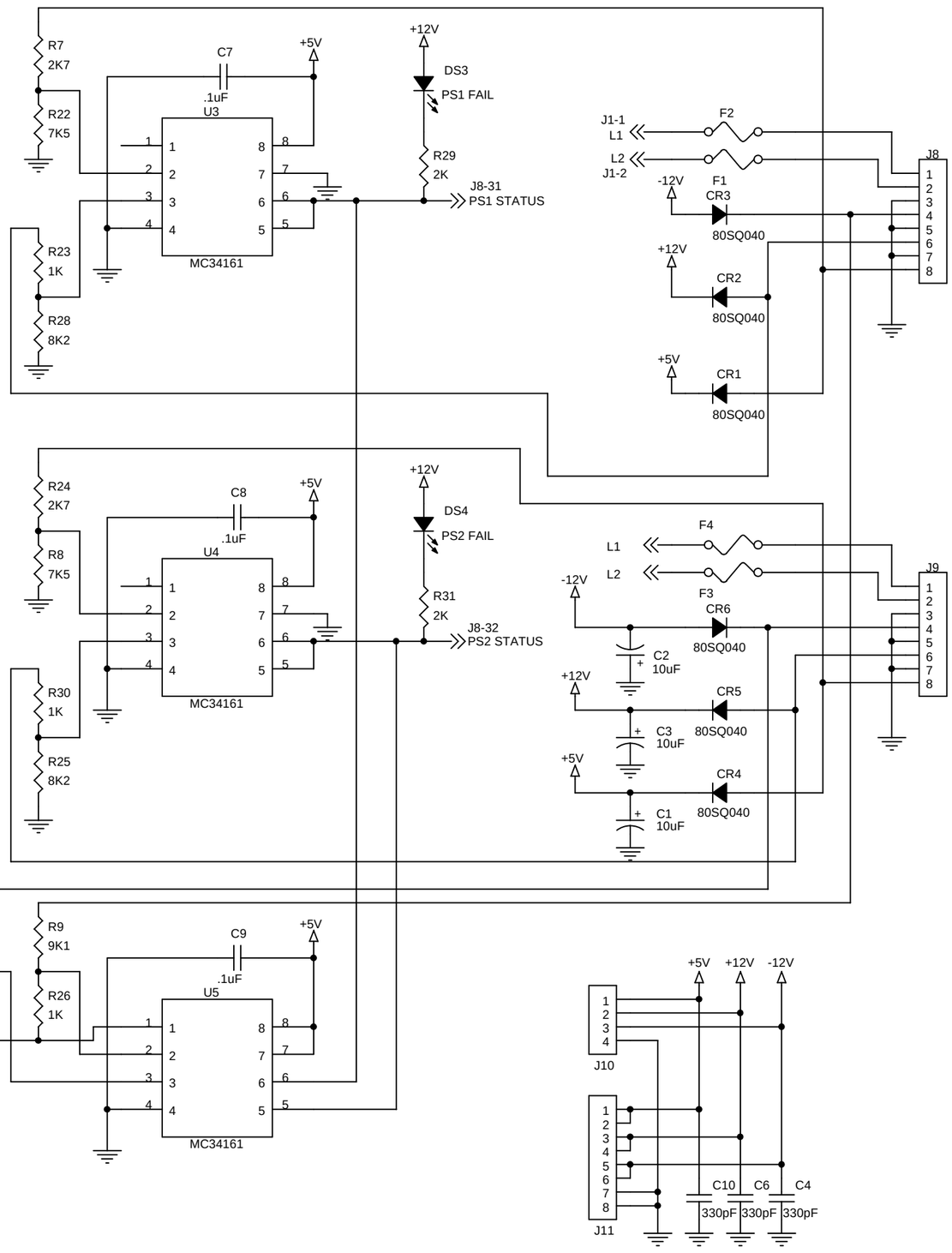
R58
43K
L1
L2
+12V

LARCAN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2K7
R22
7K5
C7
.1uF
+5V
U3
MC34161
R23
1K
R28
8K2
+12V
DS3
PS1 FAIL
R29
2K
J8-31
PS1 STATUS
J1-1
L1
L2
J1-2
F2
-12V
F1
CR3
80SQ040
+12V
CR2
80SQ040
+5V
CR1
80SQ040
J8
R24
2K7
R8
7K5
C8
.1uF
+5V
U4
MC34161
R30
1K
R25
8K2
+12V
DS4
PS2 FAIL
R31
2K
J8-32
PS2 STATUS
F4
L1
L2
F3
J9
-12V
CR6
80SQ040
C2
10uF
+12V
CR5
80SQ040
C3
10uF
+5V
CR4
80SQ040
C1
10uF
R27
9K1
R32
1K
R9
9K1
R26
1K
C9
.1uF
+5V
U5
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C6
C4
330pF
330pF
330pF

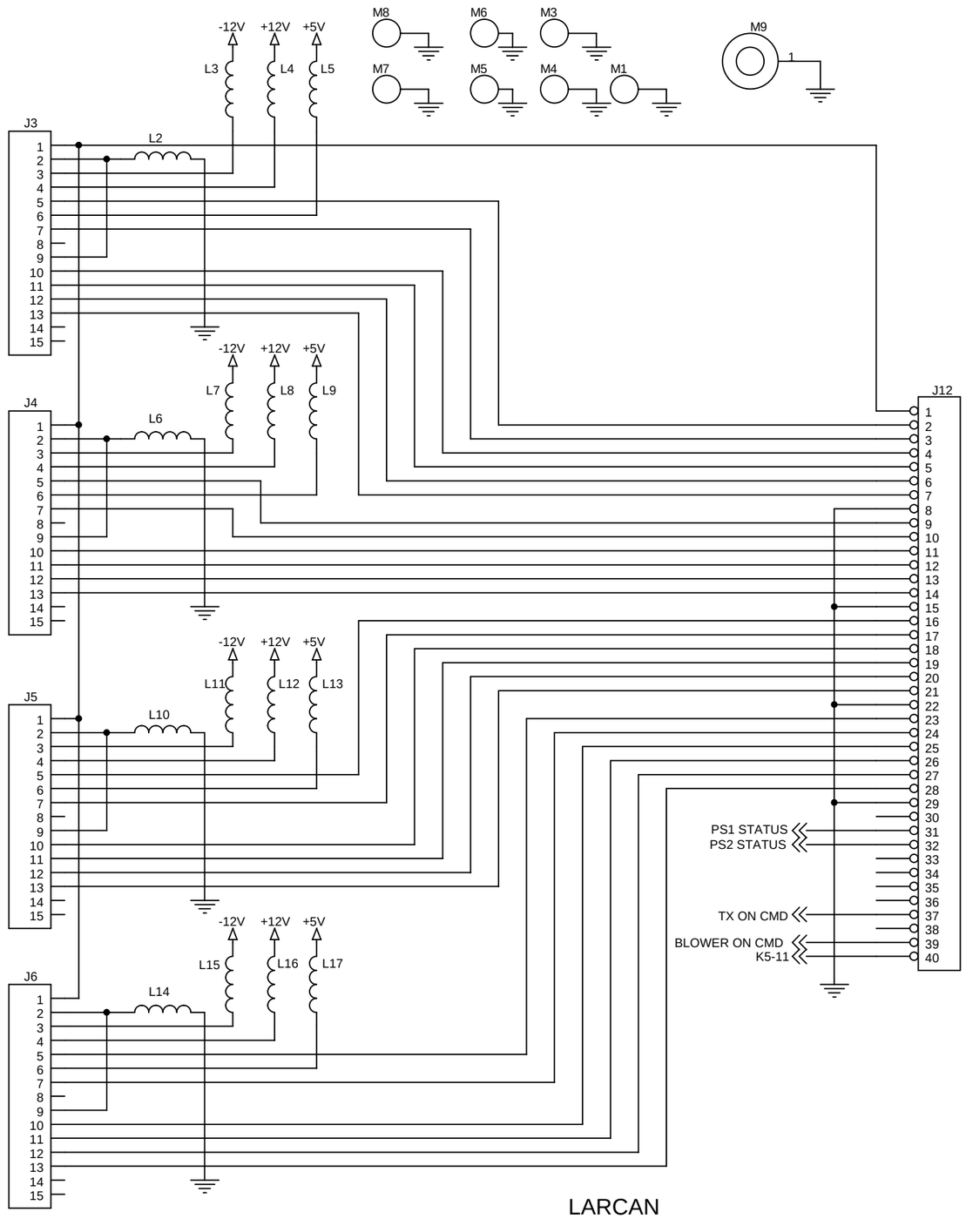

M8
M6
M3
M7
M5
M4
M1
M9
1
-12V
+12V
+5V
L3
L4
L5
J3
L2
L7
L8
L9
J4
L6
L11
L12
L13
J5
L10
L15
L16
L17
J6
L14
J12
PS1 STATUS
PS2 STATUS
TX ON CMD
BLOWER ON CMD
K5-11
LARCAN

TABLE OF CONTENTS

1. INTRODUCTION

The MX1000 control system is completely self contained on a hinged panel at the front of the transmitter. From this panel, the user can turn the transmitter on and off, raise and lower the output power, and monitor all critical parameters and status. The interface for remote control of the transmitter is also provided from this panel.

The control system handles all the interlocking control, protects the transmitter against excessive VSWR and displays power supply status. Meters are provided for monitoring output power, reflected power, P/S currents and AGC voltage.

Figure 1 Front Panel

2. CIRCUIT DESCRIPTION

GENERAL

The circuitry is generally divided into various functional sections. Each section performs different functions and is typically shown on a separate sheet of the schematic. The circuit board used in

the MX1000 was designed for dual uses. On the MX1000, this board is configured to control a single transmitter. In another configuration (internally referred to as Group-2), this board controls dual PA/Power supply cabinets.

ON/OFF CONTROL AND INTERLOCK FUNCTIONS (PAGE 1 OF THE SCHEMATIC).

The ON/OFF state of the transmitter is determined by the state of the latching relay K6. Note that OFF switch S11 is connected such that it is always enabled (this is a built in safety feature of the transmitter: pressing S11 at any time, even if the transmitter is in remote mode will latch K6 into the OFF state). The ON switch S12 is only enabled when the LOCAL/REMOTE switch Sl0 (shown in LOCAL mode) is placed in the LOCAL position. If S10 is in REMOTE mode, the remote inputs are enabled and can turn on and off the transmitter.

Interlock connections to the control board are on J2. The signals from the interlock circuitry in the transmitter are opto-isolated (U21, U22 and U24A) for circuit protection. Interlocks include the airflow in the cabinet and the air temperature in the exhaust duct as well as another 'External' interlock that can be connected to patch panel or coax switch interlocking circuits. The outputs of the opto-isolators are fed to AND gates U19B and U19C. If an interlock opens or fails in any way, these gates will remove the drive from the base of transistors Ul 7A and B. These transistors buffer the ON command from K6 to turn on the power supplies.

Interlock failure also latches the associated latching relay (K3, K4, K7, K8, or K9). These relays remain latched until a reset command is issued. If an interlock is opened and then restored, the latching relay remains latched. This ensures that a "history" or record of the interlock failure is retained. On early versions of the transmitter, this would cause the interlock LED to remain off until the reset was given. Later versions of the control circuit included a circuit that would cause the LEDs to blink on and off after the interlock was restored but before the reset was pressed. A blinking LED indicates that the interlock was opened but subsequently restored.

Note that the command to turn on the blower is sent directly from relay K6 and is not included in the interlock circuitry.

METERING DISPLAY CIRCUITRY (PAGE 2 AND 3 OF THE SCHEMATIC)

The circuitry shown on pages 2 and 3 of the schematic is identical in function. The two sets of circuitry simply drive different meters. The metering circuit on the control board serves to route the selected signal (coming from various points within the transmitter) to the front panel display meter. As both metering circuits are the same, only the circuitry on page 2 of the schematic will be described.

A debounce IC is used as a latching circuit for the meter selection switches. The debounce ICs U6 and U7 (MC14490) use an oscillator to debounce the switch inputs. Capacitor C31 is connected between to pins 7 and 9 of U7 and determines the frequency of oscillation. Buffer inverter U42A is used to connect the oscillator output of U7 to pin 7 of U6. When a switch is pressed, R33 is temporarily removed from the circuit allowing the oscillator to oscillate and the debounce IC debounces the switch inputs. When the switch is released, R33 is grounded, causing the oscillations to stop. At the point the oscillation is stopped, the output of the debounce IC latches. The outputs remain latched in the last known state until the debounce oscillator is functioning (user presses a selector switch). The outputs of U6 and U7 drive the selector inputs of CMOS analog switch ICs U3 and U4. The output of these analog switches drive the digital panel meter via buffer amplifier U9C and calibration pot R217.

The schematic shown on page 3 is identical in design to that of page 2, except for the obvious component designation changes and that the buffer amplifier output drives the analog power meter. This meter is current driven, so the adjustment pot R219 adjusts the current being fed through the meter, as opposed to the voltage being fed to the meter.

AGC AND VSWR PROTECTION (PAGE 4 OF THE SCHEMATIC).

The AGC circuitry is designed to maintain the power of the transmitter at a particular power level, however the AGC circuit is also used to generate cutback protection in the event of excessive output VSWR.

Output power is sampled and detected by the RF detector board and fed to the AGC circuitry J8. U35A buffers the voltage and feeds the metering display circuitry through calibration pot R164. U35B is configured as a comparator, using the voltage from NOVPOT U43 as a reference voltage against the sampled output voltage. The output of U35B feeds the AGC output via buffer amplifier U35C. AGC enable switch S23 is shown in the "disable" position. In this position, the AGC voltage is grounded through forward biased transistor U33D, thus disabling the ACG part of the circuit.

U43 is a solid state Non Volatile Digital Potentiometer. The IC has an internal pulse counter and internal switching logic and the solid state equivalent of a stepping motor to connect the taps in an internal string of resistors, one at a time to its "wiper" terminal. Programmable non-volatile memory is provided within the device to maintain its last setting and restore that setting during power-up. U41 is configured as a clock pulse generator providing the required clock signal to U43. VR1 is a safety device that disables the raise/lower circuitry from operation during power fail or power-up conditions. This prevents inadvertent transmitter power changes. The output of VR1 feeds AND gate U38A. Pressing the RAISE (S20) or LOWER (S17) switch causes the other input to U38A to go high. This has the effect of starting the clock generator, U41, and placing a low on pin 7 of U43. If the RAISE switch was pressed, pin 2 of U43 is low as well, causing the "wiper" pin (pin5) of U43 to rise in voltage. If the LOWER switch was pressed, pin2 of U43 stays low, causing pin 5 of U43 to lower in voltage.

AGC SYSTEM OPERATION

The function of the Automatic Gain Control system is to keep the transmitter operating at 100% over varying environmental conditions. The intent of this system is not to compensate for device failures, or excessive loss in output systems due to mismatch or poor tuning. Power FETs have some inherent change in gain over operating temperature and this is the reason for the AGC system. Generally, the AGC is set up with 10 - 15% headroom. Typically, this is done by disabling AGC, setting the exciter for a tx output power of 115%, then, with the AGC enabled, lowering (or raising) the power for a nominal 100% output. Of course, this can only be done (properly) with a healthy transmitter, at normal operating temperature. The AGC control sends a voltage to a variable attenuator located in the 4-way splitter module. This voltage is varied, depending on the gain of the PA modules, to keep the transmitter output constant.

The detected sample of the reflected power is fed to comparator U29B. This signal is compared to a factory set threshold level determined by resistor combination R142, R146,R138 and R125. As the reflected power increases to this preset level, the output voltage from U29B will increase. The output of U29B feeds buffer amplifier U35C and thus overrides the AGC voltage, causing the transmitter power to drop. In addition, op-amp U29C compares the output voltage from U29B to a factory preset level as determined by R137/R13O. As the output of U29B increases due to VSWR, U29C will turn on the CUTBACK LED D56 on the front panel display.

The forward power telemetry is also sent to op-amp U28B where it is amplified by a factor of two and then passed through a pot. The output from the pot is then sent to op-amp U28C. However, if the output of the pot is too low, diode CR28 will pass a voltage of approximately 2.7V to the input of the diode. The other input of op-amp U28C receives the reflected power telemetry. Now, when pot R128 is set properly, if the reflected power telemetry reaches the same voltage as the forward telemetry from pot R128, then you have high VSWR and the transmitter should be shut off. The transmitter will be shut off because the output of op-amp U28C will cause relay K11 to trip. When K11 trips, it sends a "VSWR OUT TRIP" indication to and gate U19A which causes the transmitter to turn off. It will also cause K10 to trip, and stay tripped until a reset command is

issued, causing the VSWR trip led to record the VSWR trip. Now, once K11 trips, the input capacitor to U31 A will start to charge. When it passes +5V, relay K11 will be set back to it's original state and the transmitter will turn on again. In this way, a momentary VSWR will cause the transmitter to trip off and then restart. However, each time relay K11 trips, the monostable IC U30B sends a pulse to slightly charge capacitor C92. If the transmitter trips 3 times in succession, capacitor C92 will have charged past the voltage present on the negative input of U31B, which is provided by the voltage divider of R150 and R154. Should this happen, op-amp U31B will cause relay K5 to trip. This will turn off the transmitter until a reset command is issued.

INTERCONNECTION WITH THE TRANSMITTER (PAGE 5 OF THE SCHEMATIC)

Information from the various modules within the transmitter are fed to the control board via J3. Table 1 details the signals and pins.

Table 1

1	Reset Command	All Regulators
2	Over Current Status	Regulator 1
4	Current Telemetry	Regulator 1
5	Over Voltage Status	Regulator 1
6	Lockout Status	Regulator 1
9	Over Current Status	Regulator 2
11	Current Telemetry	Regulator 2
12	Over Voltage Status	Regulator 2
13	Lockout Status	Regulator 2
16	Over Current Status	Regulator 3
18	Current Telemetry	Regulator 3
19	Over Voltage Status	Regulator 3
20	Lockout Status	Regulator 3
23	Over Current Status	Regulator 4
25	Current Telemetry	Regulator 4
26	Over Voltage Status	Regulator 4
27	Lockout Status	Regulator 4

The lockout information from the regulators is an open collector signal, these signals are bused together to a “collective” lockout indication. The trip information is connected together in a similar manner. Diode CR32 connects the trip and the lockout lines so that either a trip or a lockout of the regulators will cause opto U31A to turn on U16B, causing the REGULATORS OK LED to turn off. In addition, relay K1 will latch, causing the REGULATOR TRIP LED to turn on. K1 is also connected to remote interface J5 which will indicate that a regulator tripped. If a regulator trips, and then locks out, the REGULATORS OK LED will be off. However the REGULATOR TRIP LED will blink, indicating the lockout. U8 is configured as an oscillator that controls the ‘blinking’ of the LEDs The clock signal from U8-3 passes through U5A only if a regulator has locked out. This signal then alternately turns U16A on and off.

The current telemetry signals from the regulators are used for front panel metering and also telemetry. These voltages pass through calibration pots R221, R225, R229 and R233. From here they are buffered by op amp U2 and sent to both the remote control interface and to the analog switches that send the signals to the meters.

Note: In the case of parallel 1kW cabinets, the information from the second amplifier cabinet is returned to the control board via J4.Pl

REMOTE CONTROL (PAGE 6 OF THE SCHEMATIC)

This page illustrates the routing of the remote control interface. Connector J11 is a 25 pin D-shell connector that comprises the majority of the remote control interface connection. Remote control connections are detailed in Table 2. When the front panel REMOTE switch is pressed, a remote

arming voltage is present and the grounding of a remote control input will result in that command being issued. A remote reset command on J11-5 will cause the opto U24 to send a reset command. This reset is split into an active low and an active high reset by transistors U20 B and D.

Connectors J12, J13, J14, and J15 bring information from the PA's to the remote interface. On those connectors pin 3 brings the cutback voltage, and pin 5 brings a RF OK indication. The cutback voltage is buffered by op amps U10A, B ,C,D while the RF OK indication is isolated by opto isolators U11A, U11B, U12A, U12B.

Table 2

Pin	Signal	Function
1	PA 1 Current	Telemetry
2	PA 2 Current	Telemetry
3	PA 3 Current	Telemetry
4	PA 4 Current	Telemetry
5	Reset	Command
6	ON	Command
7	OFF	Command
8	AGC Raise	Command
9	PA 1 Cutback	Telemetry
10	PA 2 Cutback	Telemetry
11	PA 3 Cutback	Telemetry
12	PA 4 Cutback	Telemetry
13	Reflected Power	Telemetry
14	Vis. Fwd. Power	Telemetry
15	Aur. Fwd. Power	Telemetry
16	AGC Lower	Command
17	PA 1 RF OK	Status
18	PA 2 RF OK	Status
19	PA 3 RF OK	Status
20	PA 4 RF OK	Status
21	Ext Interlock	Status
22	Temperature Interlock	Status
23	Air Flow Interlock	Status
24	Cab. 2 Temp. Interlock**	Status
25	Cab. 2 Air Flow Interlock**	Status

3. TESTING AND TROUBLESHOOTING

For the most part, there is very little servicing that can be done to this circuit in the field. The circuitry uses surface mount technology (SMT) and can be very difficult to service with conventional tools. There are adjustments that are preset at the factory and do not require readjustment under normal circumstances in the field. The following tests are in essence, functional tests that can be performed to determine it the circuitry is indeed working properly. In the event that the circuitry is not functioning the way it should, it is suggested that firstly, a visual inspection be done for obvious problems, secondly, that wiring into and from the circuit board be inspected and finally, that the circuit board be removed and replaced. For these tests, if the board functionality is tested in the transmitter, it is recommended that the breakers for the blower, and power supplies be left off.

METERING SWITCHES

- Ensure that JP1 and JP2 are installed. *Note: on the MX1000 version of this board, some switches are not installed. These are for the dual cabinet version of the controller.*

- On power-up the LEDs on the VIS switch for POWER METERING should be lit as should the LED on the PA1 switch for METERING.
- When a switch button is pressed the corresponding LED should illuminate.
- Select the VIS metering function on the POWER METERING section. Connect a variable power supply set to 4 volts to J8-9. Adjust R164 for a reading of 100% on the power meter. R219 may need adjustment in order to get the correct deflection on the meter.
- Select the RFL metering function. Using the variable supply, apply 4 volts to J8-6. Adjust R117 for a reading of 100% on the meter.
- Select the AUR metering function. Connect the variable supply to J8-11. Note that the board has no adjustment for the meter deflection in this function. In the transmitter calibration of this function is done on the RF detector board. There should be meter to deflection for 4 volts input.
- Select the AGC metering function. Press the OFF switch. Measure the voltage on the BNC connector J16. Adjust R217 so that the voltage measured at the BNC connector appears on the LCD display (±0.1 volts).
- Select the PA1 metering function. Apply a voltage between 1 and 2 volts to J3-4 and verify that there is a meter reading. Note: a voltage higher than 2 volts will cause a reading of "1" on the screen indicating an over-range condition.
- Select the PA2 metering function. Apply a voltage between 1 and 2 volts to J3-4 and verify that there is a meter reading.
- Select the PA3 metering function. Apply a voltage between 1 and 2 volts to J3-4 and verify that there is a meter reading.
- Select the PA4 metering function. Apply a voltage between 1 and 2 volts to J3-4 and verify that there is a meter reading.

INTERLOCKS

- Install jumpers across:

  J2-1 and J2-2
  J2-3 and J2-4
  J2-5 and J2-6

- Press the reset button. The EXTERNAL, TEMP, and AIR LEDs should all be illuminated.
- Remove the jumper across J2-1/J2-2. The EXTERNAL LED should extinguish. Re-install the jumper. The LED should stay off until RESET is pressed. While the Led is on you should see ground on J11-21, while the led is off, J11-21 will be floating.
- Remove the jumper across J2-3 and J2-4. The TEMP led should turn off. Re-install that jumper. The Led should stay off until you press reset. While the Led is on you should see ground on J11-22, while the led is off, J11-22 will be floating.
- Remove the jumper across J2-5 and J2-6. The AIR led should turn off. Re-install that jumper. The Led should stay off until you press reset. While the Led is on you should see ground on J11-23, while the led is off, J11-23 will be floating.
- Again remove the jumper across J2-5 and J2-6. The AIR led should turn off. Re-install the jumper. Put the board in remote (push in the remote button so the led on the switch is turned on) and by grounding J11-5 you should be able to turn on the LED again.

CONTROL

In Remote mode, the local ON button (on the tx front panel) will not work. The OFF button will still work. This is a built-in safety feature of the transmitter.

- Verify that the REMOTE switch is in the Local, or 'out' position. The corresponding LED should be off. The transmitter controller is in 'Local' control mode.
- Press the ON switch and verify that its corresponding LED is illuminated. Press the OFF switch and verify that its LED is illuminated and the ON LED is extinguished.

- Press the REMOTE switch to set the control into 'Remote' mode. The LED on the REMOTE switch should be illuminated. Press the OFF switch. The OFF LED will illuminate. Verify that when the ON switch is pressed, there is no change in state.
- Set the control back to 'remote' mode.
- Ground J11-7, and verify that the OFF LED turns on.
- Ground J11-6 and verify that the ON LED turns on and the OFF LED is extinguished.
- Verify that with the control in 'local' mode that the above two steps have no effect on the transmitter on/off state.
- Press RESET. Verify that the REG OK LED is illuminated and the REG TRIP LED is extinguished.
- Verify that by grounding J3-2 (or any one of J3 pins 2,5,9,12,16,19,23,26), the REG TRIP LED illuminates and REG OK LED turns off. The REG TRIP LED will only turn off when RESET is pressed and there is no ground on J3-2 any of the other pins noted above.
- Ground J3-6 (lockout). The REG TRIP LED should now blink. The LED will blink as long as J3-6 is grounded (Any one of J3 pins 6, 13, 20, 27).

REMOTE STATUS AND TELEMETRY INTERFACE

- Using a variable power supply set at approximately 4 volts, the voltage applied at pins listed in the first column will be buffered and appear at the pin on the second column.

J12-2	J11-9
J13-2	J11-10
J14-2	J11-11
J15-2	J11-12

- Grounding the pin listed in the first column, will result in a grounded pin in the second column

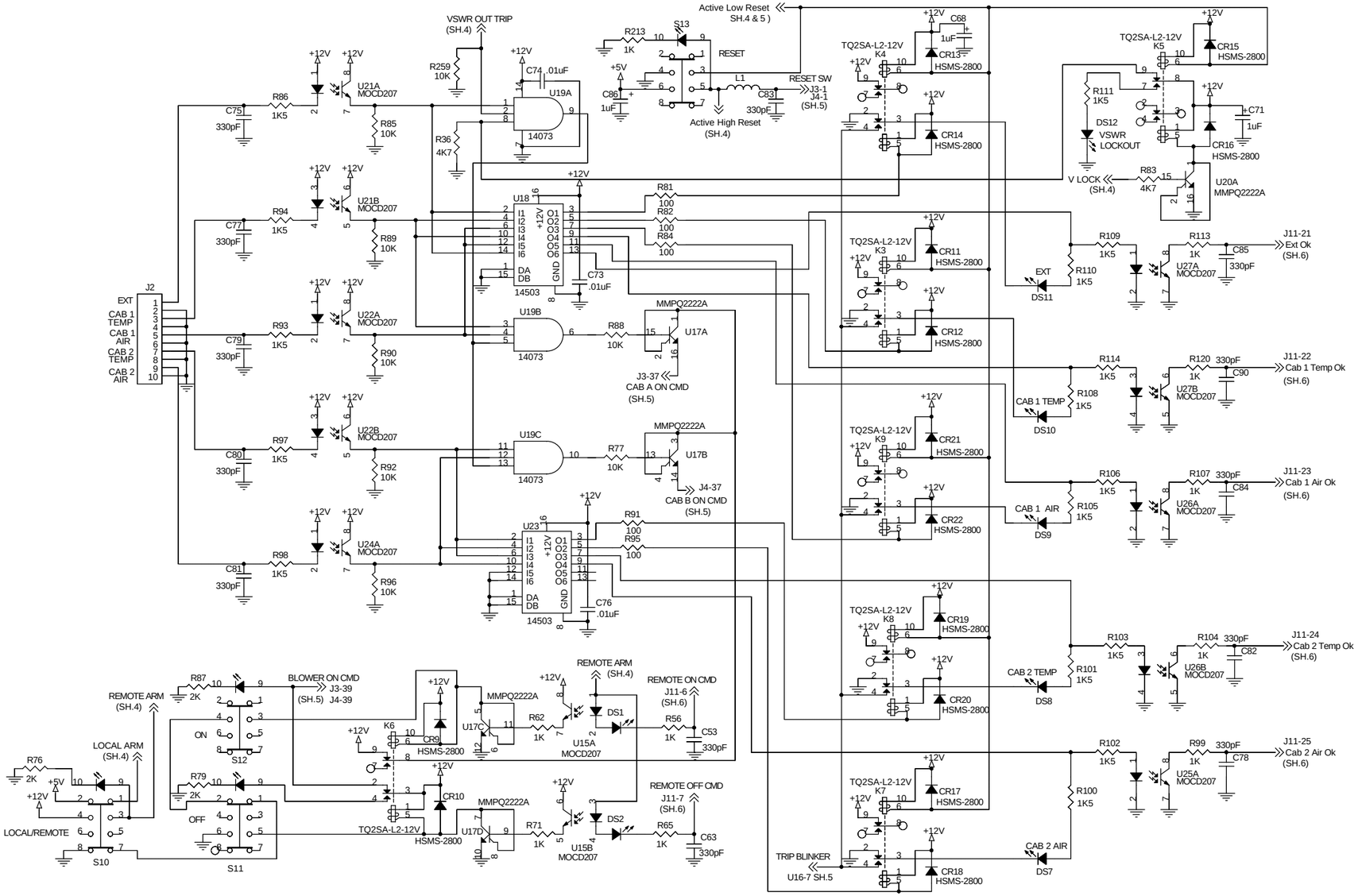
J12-5	J11-17
J13-5	J11-18
J14-5	J11-19
J15-5	J11-20

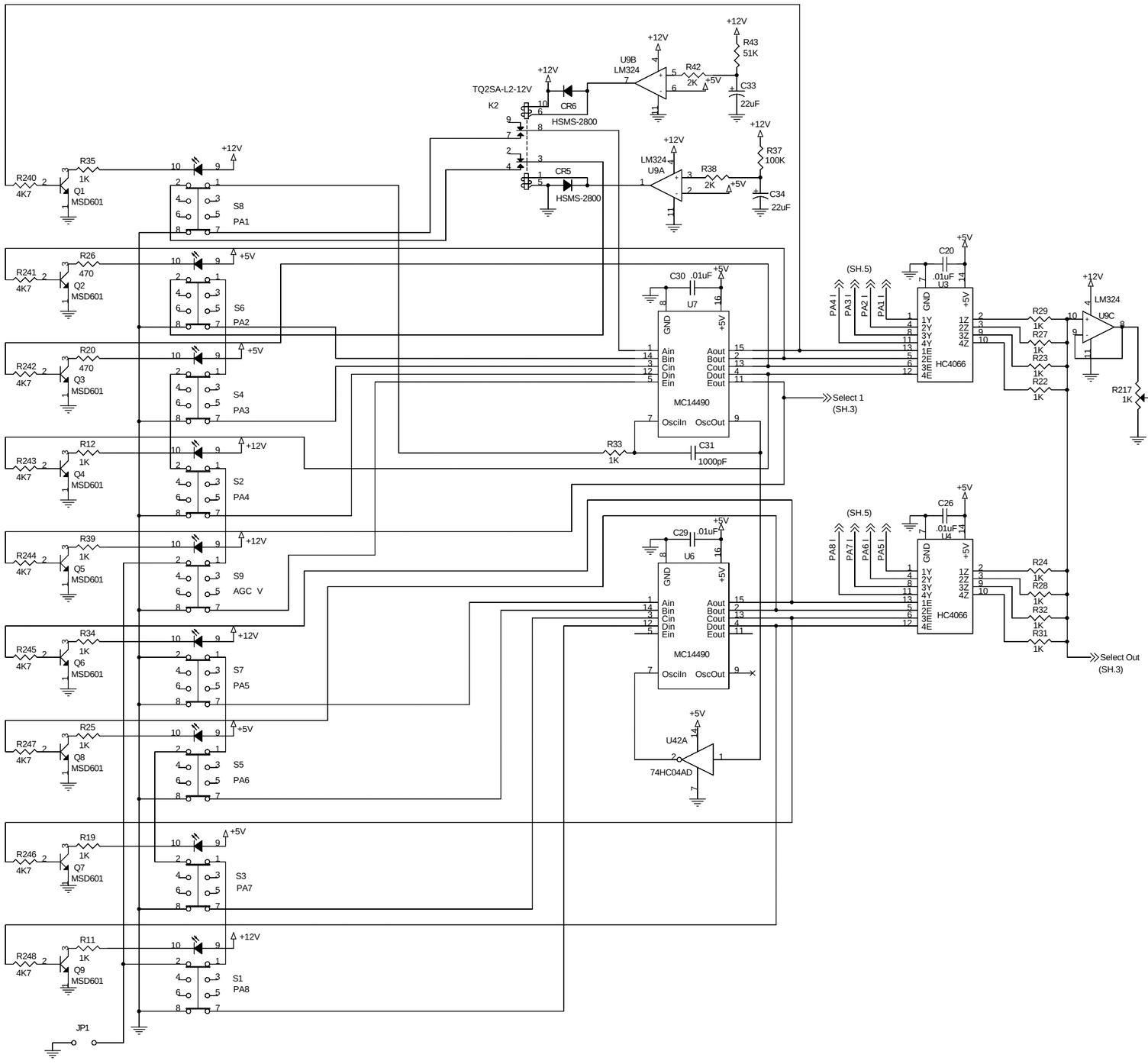
- Apply a voltage (~4 volts) to J8-11. The same voltage should appear at J11-15.
- Apply a voltage to J8-9. Adjust R164 for the same reading at J11-14.
- Apply a voltage to J8-6. Adjust R117 so for the same reading at J11-13.

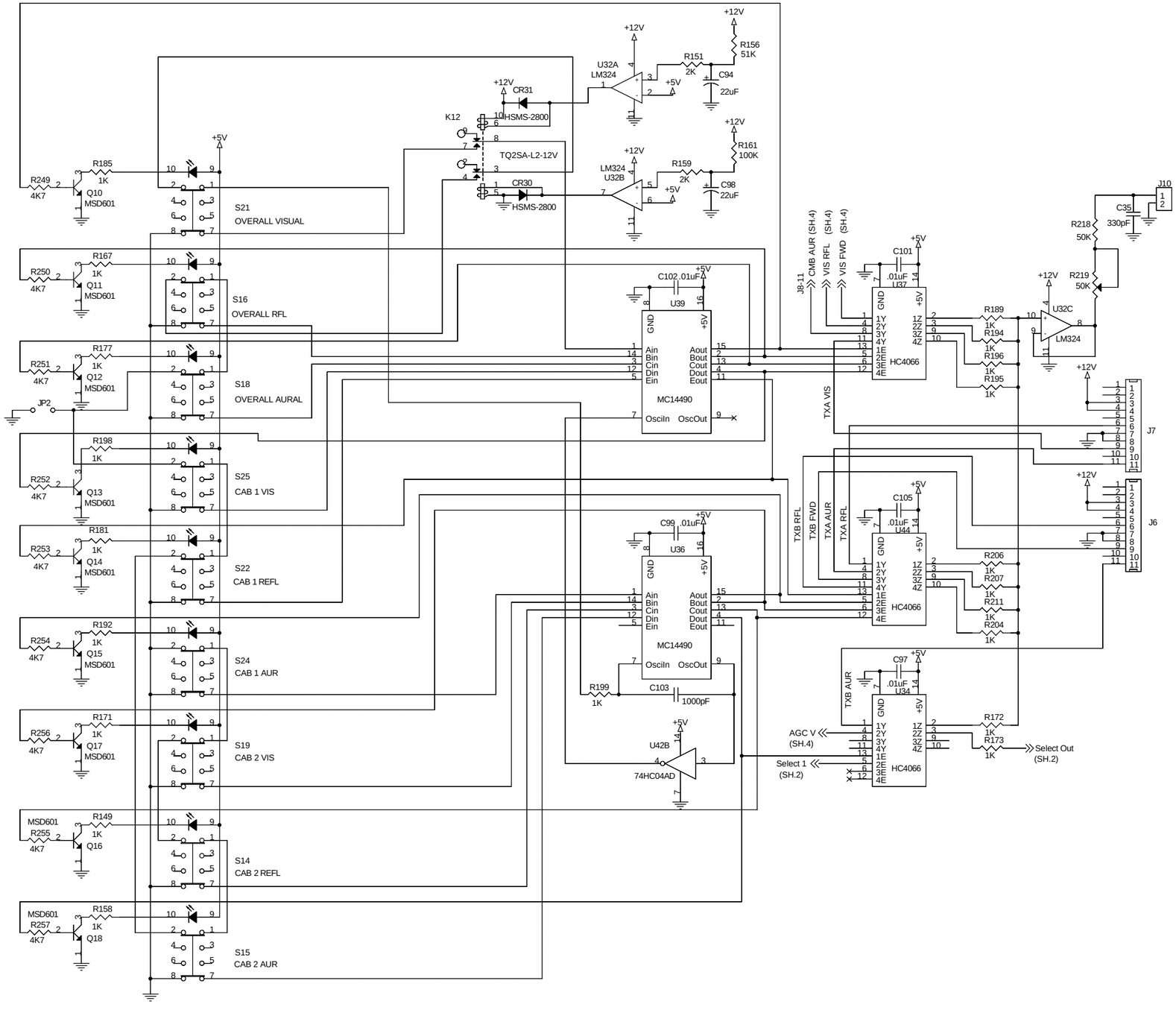
AGC CIRCUITRY

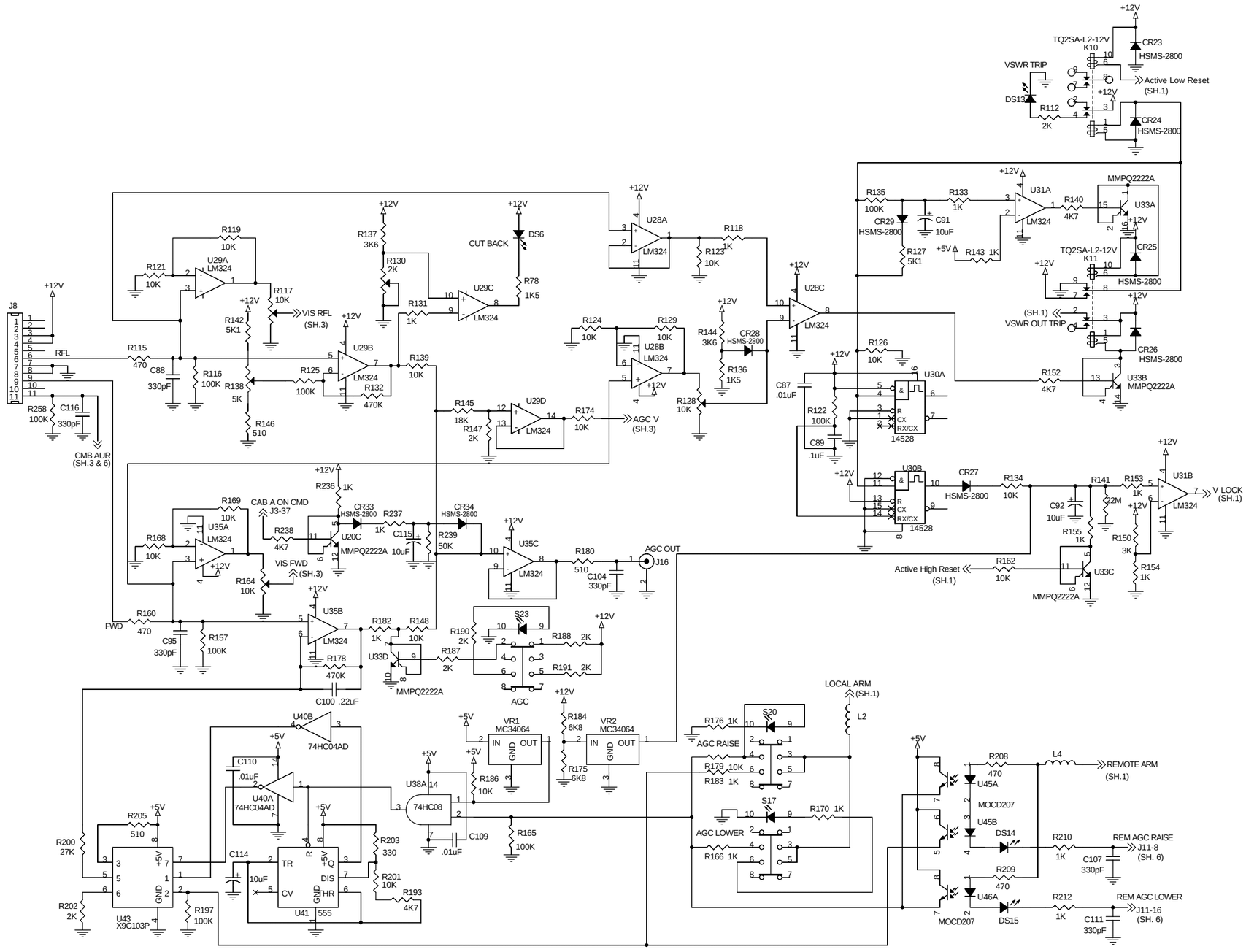
- Install jumpers across J2-7,8 and across J2-9,10.
- Press the ON switch.
- Apply +5V to J8-9. Do not apply any voltage to any other pins on that connector.
- Push the ACG ENABLE switch. The LED on the switch should illuminate indicating AGC control is enabled.
- Measure the voltage on the AGC connector J16.
- With the transmitter in local control mode, alternately pressing the AGC RAISE and LOWER buttons you should be able to lower and raise the voltage on J16 (note: RAISE will actually decrease the voltage and vice versa).
- Set the control to remote mode. The AGC RAISE and LOWER switches will no longer vary the voltage on J16. By alternately grounding pins J11-8 and J11-16 you should be able to lower and raise the voltage on connector J16 (remotely).
- Press the OFF switch.
- The voltage on J16 should be substantially higher (approximately 8 volts or higher).
- Press the ON switch.
- Remove the voltage on J8-9. Apply +5V to J8-6.
- Monitor the voltage at J16. Adjust R138 for approximately 1 volt at J16.

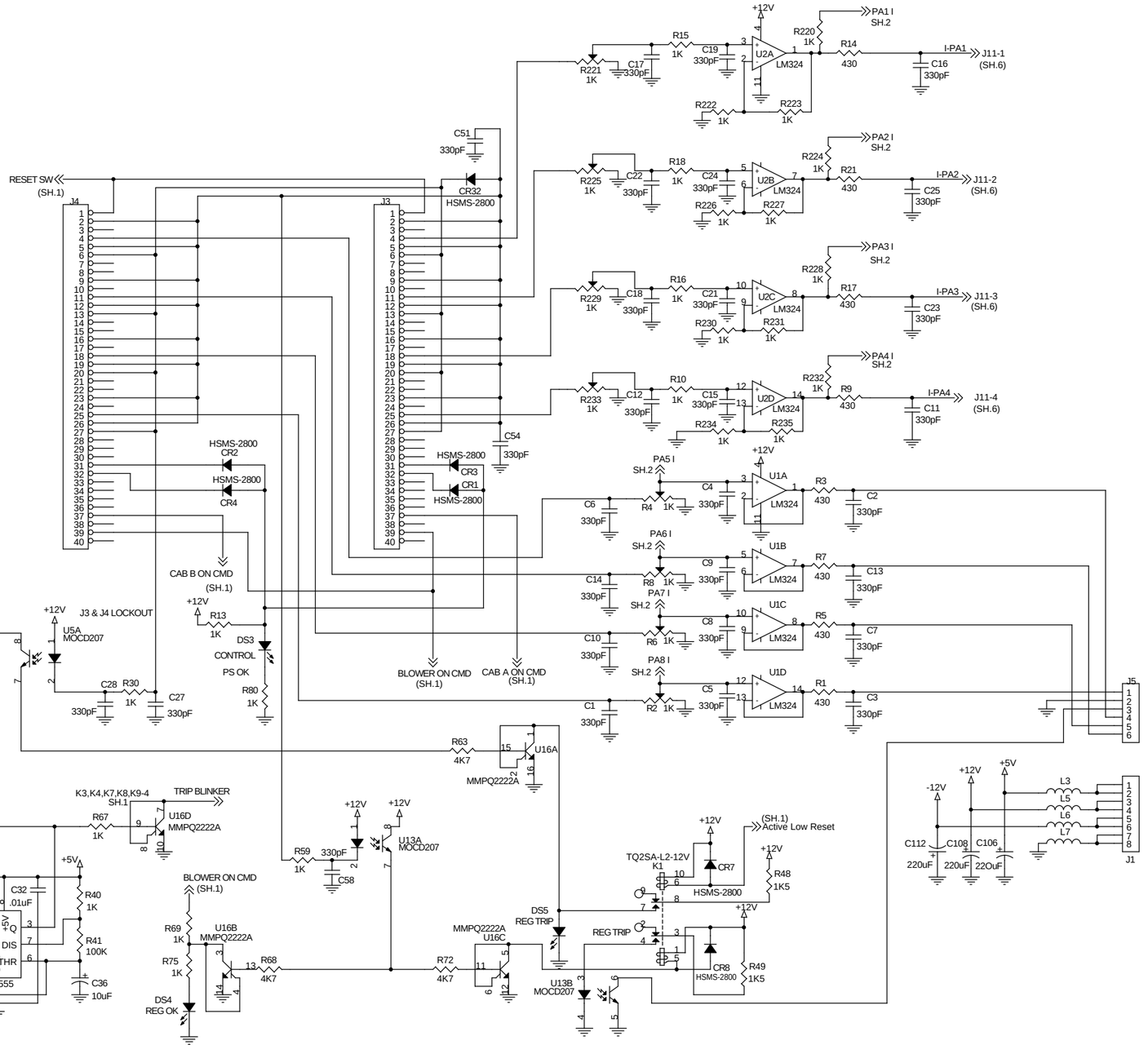
- Adjust R137 and verify that DS6 can be turned on and off by this adjustment.
- Apply +4V to J8-9. Adjust R128 for 4.0 Volts at U28-9.
- Apply +4V to J8-6. The VSWR TRIP LED should illuminate and the VSWR L/O LED will illuminate after a few seconds.
- Remove the voltage from J8-6. Press RESET to clear the VSWR TRIP and VSWR L/O LEDs.
- Briefly touching +4V to J8-6 and removing it 3 times within a few seconds will cause theVSWR L/O LED to come on and stay on until RESET is pressed.

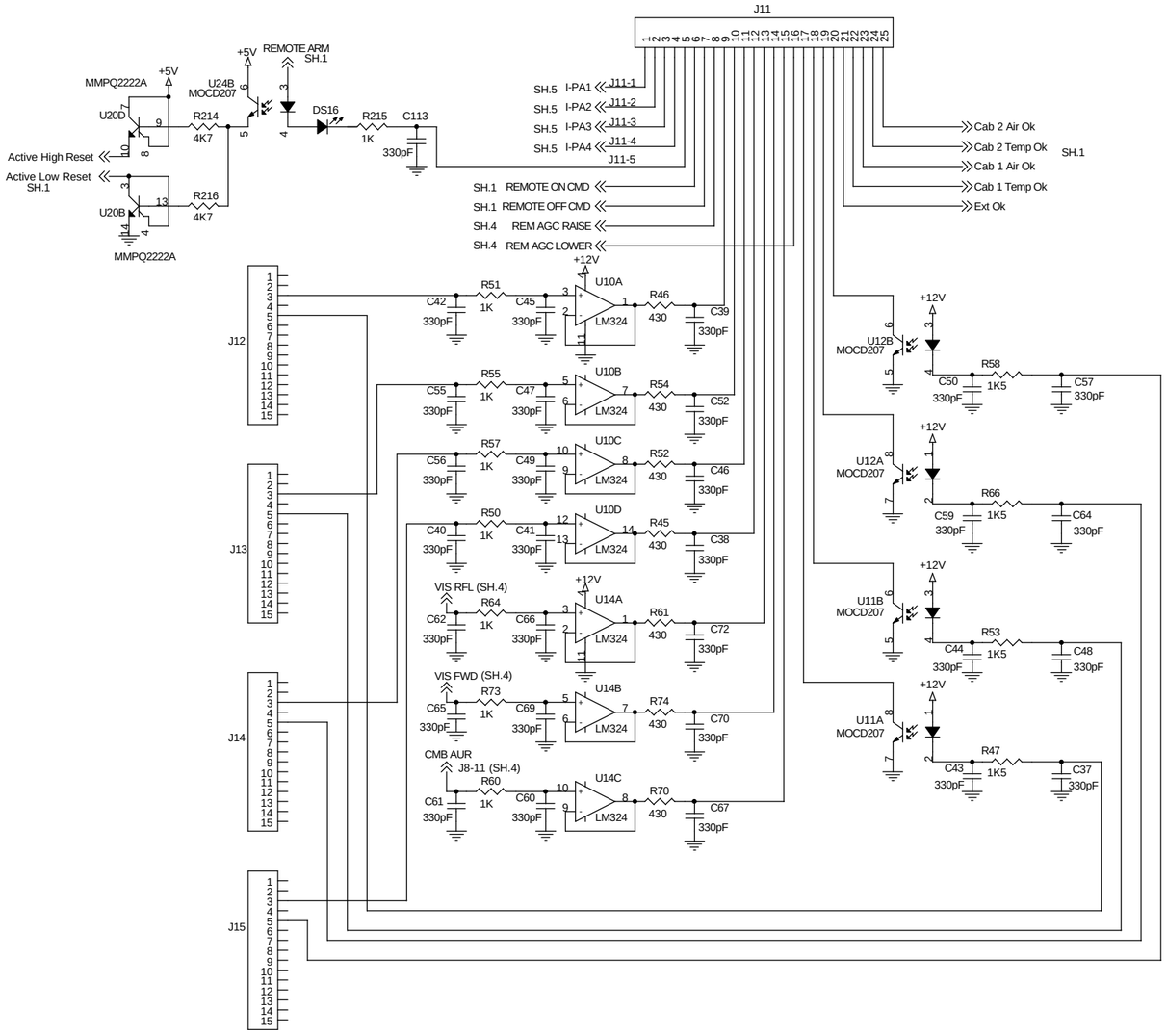

VSWR OUT TRIP
(SH.4)
Active Low Reset
SH.4 & 5)
Active High Reset
(SH.4)
RESET
RESET SW
J3-1
J4-1
(SH.5)
J2
EXT
CAB 1 TEMP
CAB 1 AIR
CAB 2 TEMP
CAB 2 AIR
U21A MOCD207
U21B MOCD207
U22A MOCD207
U22B MOCD207
U24A MOCD207
U19A
U19B
U19C
14073
U18
U23
14503
TQ2SA-L2-12V
K4
K3
K9
K8
K7
CR13 HSMS-2800
CR14 HSMS-2800
CR11 HSMS-2800
CR12 HSMS-2800
CR21 HSMS-2800
CR22 HSMS-2800
CR19 HSMS-2800
CR20 HSMS-2800
CR17 HSMS-2800
CR18 HSMS-2800
CR15 HSMS-2800
CR16 HSMS-2800
CR9 HSMS-2800
CR10 HSMS-2800
DS12 VSWR LOCKOUT
DS11
DS10
DS9
DS8
DS7
DS1
DS2
U20A MMPQ2222A
U17A
U17B
U17C
U17D
U15A MOCD207
U15B MOCD207
U27A MOCD207
U27B MOCD207
U26A MOCD207
U26B MOCD207
U25A MOCD207
V LOCK
(SH.4)
J3-37
CAB A ON CMD
(SH.5)
J4-37
CAB B ON CMD
(SH.5)
J11-21
Ext Ok
(SH.6)
J11-22
Cab 1 Temp Ok
(SH.6)
J11-23
Cab 1 Air Ok
(SH.6)
J11-24
Cab 2 Temp Ok
(SH.6)
J11-25
Cab 2 Air Ok
(SH.6)
TRIP BLINKER
U16-7 SH.5
REMOTE ARM
(SH.4)
BLOWER ON CMD
(SH.5)
J3-39
J4-39
REMOTE ON CMD
J11-6
(SH.6)
REMOTE OFF CMD
J11-7
(SH.6)
LOCAL ARM
(SH.4)
LOCAL/REMOTE
S10
S11
S12
S13
ON
OFF
R213 1K
R259 10K
R36 4K7
R86 1K5
R85 10K
R94 1K5
R89 10K
R93 1K5
R90 10K
R97 1K5
R92 10K
R98 1K5
R96 10K
R81 100
R82 100
R84 100
R91 100
R95 100
R88 10K
R77 10K
R87 2K
R79 2K
R76 2K
R62 1K
R56 1K
R71 1K
R65 1K
R111 1K5
R109 1K5
R110 1K5
R114 1K5
R108 1K5
R106 1K5
R105 1K5
R102 1K5
R100 1K5
R103 1K5
R101 1K5
R83 4K7
R113 1K
R120 1K
R107 1K
R104 1K
R99 1K
C74 .01uF
C73 .01uF
C76 .01uF
C68 1uF
C86 1uF
C83 330pF
C79 330pF
C77 330pF
C80 330pF
C81 330pF
C71 1uF
C85 330pF
C90 330pF
C84 330pF
C82 330pF
C78 330pF
C53 330pF
C63 330pF
+12V
+5V


+12V
R43
51K
U9B
LM324
R42
2K
+5V
C33
22uF
TQ2SA-L2-12V
K2
CR6
HSMS-2800
CR5
HSMS-2800
LM324
U9A
R38
2K
R37
100K
C34
22uF
R35
1K
R240
4K7
Q1
MSD601
S8
PA1
R26
470
R241
4K7
Q2
MSD601
S6
PA2
R20
470
R242
4K7
Q3
MSD601
S4
PA3
R12
1K
R243
4K7
Q4
MSD601
S2
PA4
R39
1K
R244
4K7
Q5
MSD601
S9
AGC V
R34
1K
R245
4K7
Q6
MSD601
S7
PA5
R25
1K
R247
4K7
Q8
MSD601
S5
PA6
R19
1K
R246
4K7
Q7
MSD601
S3
PA7
R11
1K
R248
4K7
Q9
MSD601
S1
PA8
JP1
C30 .01uF
U7
MC14490
Ain
Bin
Cin
Din
Ein
Aout
Bout
Cout
Dout
Eout
GND
OsciIn
OscOut
R33
1K
C31
1000pF
Select 1
(SH.3)
C29 .01uF
U6
U42A
74HC04AD
(SH.5)
PA4 I
PA3 I
PA2 I
PA1 I
C20
.01uF
U3
HC4066
1Y
2Y
3Y
4Y
1E
2E
3E
4E
1Z
2Z
3Z
4Z
R29
1K
R27
1K
R23
1K
R22
1K
LM324
U9C
R217
1K
C93
.1uF
330pF
C96
J9
C26
.01uF
U4
PA8 I
PA7 I
PA6 I
PA5 I
R24
1K
R28
1K
R32
1K
R31
1K
Select Out
(SH.3)


+12V
R156
51K
U32A
LM324
R151
2K
C94
22uF
+5V
CR31
HSMS-2800
K12
TQ2SA-L2-12V
CR30
HSMS-2800
R161
100K
LM324
U32B
R159
2K
C98
22uF
R185
1K
R249
4K7
Q10
MSD601
S21
OVERALL VISUAL
R167
1K
R250
4K7
Q11
MSD601
S16
OVERALL RFL
R177
1K
R251
4K7
Q12
MSD601
S18
OVERALL AURAL
JP2
R198
1K
R252
4K7
Q13
MSD601
S25
CAB 1 VIS
R181
1K
R253
4K7
Q14
MSD601
S22
CAB 1 REFL
R192
1K
R254
4K7
Q15
MSD601
S24
CAB 1 AUR
R171
1K
R256
4K7
Q17
MSD601
S19
CAB 2 VIS
MSD601
R149
1K
R255
4K7
Q16
S14
CAB 2 REFL
MSD601
R158
1K
R257
4K7
Q18
S15
CAB 2 AUR
C102 .01uF
U39
MC14490
OsciIn
OscOut
Ain
Bin
Cin
Din
Ein
Aout
Bout
Cout
Dout
Eout
GND
C99 .01uF
U36
R199
1K
C103
1000pF
U42B
74HC04AD
J8-11
CMB AUR (SH.4)
VIS RFL (SH.4)
VIS FWD (SH.4)
C101
.01uF
U37
HC4066
TXA VIS
R189
1K
R194
1K
R196
1K
R195
1K
U32C
LM324
R218
50K
R219
50K
C35
330pF
J10
J7
J6
TXB RFL
TXB FWD
TXA AUR
TXA RFL
C105
.01uF
U44
R206
1K
R207
1K
R211
1K
R204
1K
C97
.01uF
U34
TXB AUR
R172
1K
R173
1K
AGC V
(SH.4)
Select 1
(SH.2)
Select Out
(SH.2)


J8
RFL
CMB AUR
(SH.3 & 6)
R258 100K
C116 330pF
R115 470
C88 330pF
R116 100K
R119 10K
U29A LM324
R121 10K
R117 10K
VIS RFL
(SH.3)
R142 5K1
R138 5K
R146 510
U29B LM324
R125 100K
R132 470K
R139 10K
R137 3K6
R130 2K
R131 1K
U29C LM324
CUT BACK
DS6
R78 1K5
U28A LM324
R118 1K
R123 10K
U28C LM324
R124 10K
R129 10K
U28B LM324
R144 3K6
CR28 HSMS-2800
R136 1K5
R128 10K
R145 18K
R147 2K
U29D LM324
R174 10K
AGC V
(SH.3)
R135 100K
CR29 HSMS-2800
C91 10uF
R133 1K
U31A LM324
R140 4K7
MMPQ2222A
U33A
R127 5K1
+5V
R143 1K
TQ2SA-L2-12V
K11
CR25 HSMS-2800
(SH.1)
VSWR OUT TRIP
CR26 HSMS-2800
R126 10K
R152 4K7
U33B MMPQ2222A
C87 .01uF
U30A
R122 100K
C89 .1uF
14528
TQ2SA-L2-12V
K10
CR23 HSMS-2800
VSWR TRIP
DS13
R112 2K
Active Low Reset
(SH.1)
CR24 HSMS-2800
U30B
CR27 HSMS-2800
R134 10K
R141 22M
R153 1K
U31B LM324
V LOCK
(SH.1)
C92 10uF
R155 1K
R150 3K
R154 1K
U33C MMPQ2222A
Active High Reset
(SH.1)
R162 10K
R236 1K
R169 10K
CAB A ON CMD
J3-37
CR33 HSMS-2800
R237 1K
CR34 HSMS-2800
R238 4K7
U20C MMPQ2222A
C115 10uF
R239 50K
U35C LM324
R180 510
C104 330pF
AGC OUT
J16
R168 10K
U35A LM324
R164 10K
VIS FWD
(SH.3)
R160 470
FWD
C95 330pF
R157 100K
U35B LM324
R182 1K
R148 10K
U33D MMPQ2222A
R178 470K
C100 .22uF
S23
R190 2K
R188 2K
R187 2K
R191 2K
AGC
R184 6K8
VR2 MC34064
R175 6K8
VR1 MC34064
R186 10K
U38A 74HC08
C109 .01uF
R165 100K
U40B 74HC04AD
U40A 74HC04AD
C110 .01uF
R205 510
R200 27K
R202 2K
U43 X9C103P
R197 100K
C114 10uF
U41 555
R203 330
R201 10K
R193 4K7
LOCAL ARM
(SH.1)
L2
S20
R176 1K
AGC RAISE
R179 10K
R183 1K
S17
AGC LOWER
R166 1K
R170 1K
L4
R208 470
U45A MOCD207
U45B
REMOTE ARM
(SH.1)
R210 1K
DS14
REM AGC RAISE
J11-8
(SH. 6)
C107 330pF
R209 470
U46A MOCD207
DS15
R212 1K
REM AGC LOWER
J11-16
(SH. 6)
C111 330pF


RESET SW
(SH.1)
J4
J3
C51
330pF
CR32
HSMS-2800
C54
330pF
HSMS-2800
CR3
HSMS-2800
CR1
HSMS-2800
CR2
HSMS-2800
CR4
CAB B ON CMD
(SH.1)
BLOWER ON CMD
(SH.1)
CAB A ON CMD
(SH.1)
+12V
J3 & J4 LOCKOUT
U5A
MOCD207
C28
330pF
R30
1K
C27
330pF
+12V
R13
1K
DS3
CONTROL
PS OK
R80
1K
+12V
R221
1K
C17
330pF
R15
1K
C19
330pF
U2A
LM324
R220
1K
PA1 I
SH.2
R14
430
I-PA1
J11-1
(SH.6)
C16
330pF
R222
1K
R223
1K
+12V
R225
1K
C22
330pF
R18
1K
C24
330pF
U2B
LM324
R224
1K
PA2 I
SH.2
R21
430
I-PA2
J11-2
(SH.6)
C25
330pF
R226
1K
R227
1K
+12V
R229
1K
C18
330pF
R16
1K
C21
330pF
U2C
LM324
R228
1K
PA3 I
SH.2
R17
430
I-PA3
J11-3
(SH.6)
C23
330pF
R230
1K
R231
1K
+12V
R233
1K
C12
330pF
R10
1K
C15
330pF
U2D
LM324
R232
1K
PA4 I
SH.2
R9
430
I-PA4
J11-4
(SH.6)
C11
330pF
R234
1K
R235
1K
+12V
PA5 I
SH.2
C6
330pF
R4
1K
C4
330pF
U1A
LM324
R3
430
C2
330pF
PA6 I
SH.2
C14
330pF
R8
1K
C9
330pF
U1B
LM324
R7
430
C13
330pF
PA7 I
SH.2
C10
330pF
R6
1K
C8
330pF
U1C
LM324
R5
430
C7
330pF
PA8 I
SH.2
C1
330pF
R2
1K
C5
330pF
U1D
LM324
R1
430
C3
330pF
J5
R63
4K7
U16A
MMPQ2222A
K3,K4,K7,K8,K9-4
SH.1
TRIP BLINKER
R67
1K
U16D
MMPQ2222A
+12V
+12V
R59
1K
330pF
C58
U13A
MOCD207
+12V
(SH.1)
Active Low Reset
TQ2SA-L2-12V
K1
CR7
HSMS-2800
+12V
R48
1K5
+5V
C32
.01uF
R40
1K
R41
100K
C36
10uF
U8
555
TR
+5V
DIS
THR
CV
GND
BLOWER ON CMD
(SH.1)
R69
1K
R75
1K
U16B
MMPQ2222A
R68
4K7
DS4
REG OK
R72
4K7
MMPQ2222A
U16C
DS5
REG TRIP
REG TRIP
+12V
CR8
HSMS-2800
R49
1K5
U13B
MOCD207
-12V
+12V
+5V
L3
L5
L6
L7
C112
220uF
C108
220uF
C106
22OuF
J1


J11
SH.5 I-PA1 J11-1
SH.5 I-PA2 J11-2
SH.5 I-PA3 J11-3
SH.5 I-PA4 J11-4
J11-5
Cab 2 Air Ok
Cab 2 Temp Ok
Cab 1 Air Ok
Cab 1 Temp Ok
Ext Ok
SH.1
SH.1 REMOTE ON CMD
SH.1 REMOTE OFF CMD
SH.4 REM AGC RAISE
SH.4 REM AGC LOWER
+5V
REMOTE ARM SH.1
MMPQ2222A
U20D
U24B MOCD207
R214 4K7
DS16
R215 1K
C113 330pF
Active High Reset
Active Low Reset SH.1
U20B
R216 4K7
MMPQ2222A
+12V
U10A
U10B
U10C
U10D
U14A
U14B
U14C
LM324
R51 1K
R55 1K
R57 1K
R50 1K
R64 1K
R73 1K
R60 1K
R46 430
R54 430
R52 430
R45 430
R61 430
R74 430
R70 430
C42 330pF
C45 330pF
C55 330pF
C47 330pF
C56 330pF
C49 330pF
C40 330pF
C41 330pF
C62 330pF
C66 330pF
C65 330pF
C69 330pF
C61 330pF
C60 330pF
C39 330pF
C52 330pF
C46 330pF
C38 330pF
C72 330pF
C70 330pF
C67 330pF
VIS RFL (SH.4)
VIS FWD (SH.4)
CMB AUR
J8-11 (SH.4)
J12
J13
J14
J15
U12B MOCD207
U12A MOCD207
U11B MOCD207
U11A MOCD207
R58 1K5
R66 1K5
R53 1K5
R47 1K5
C50 330pF
C59 330pF
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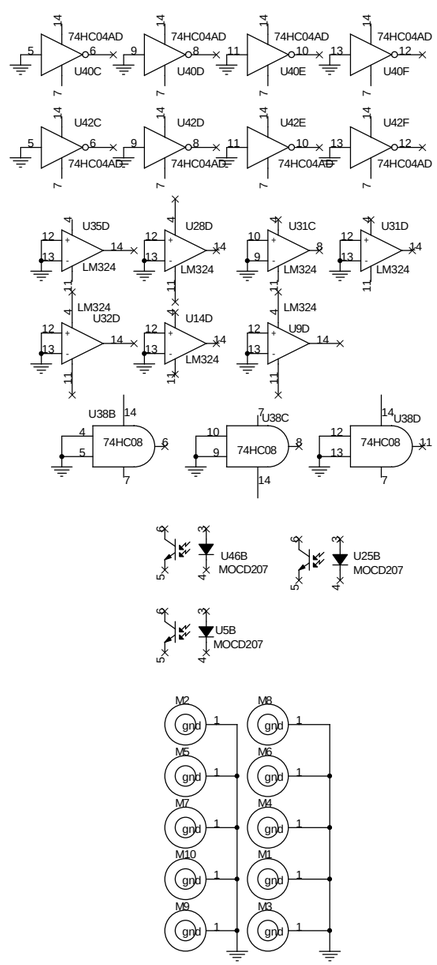
C43 330pF
C57 330pF
C64 330pF
C48 330pF
C37 330pF


74HC04AD
U40C
U40D
U40E
U40F
U42C
U42D
U42E
U42F
LM324
U35D
U28D
U31C
U31D
U32D
U14D
U9D
U38B 74HC08
U38C 74HC08
U38D 74HC08
U46B MOCD207
U25B MOCD207
U5B MOCD207
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M8
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M9
M3
gnd

TABLE OF CONTENTS

1. INTRODUCTION

The bandpass filter is a three-pole filter, the center frequency of each pole being determined by an adjustable line capable of being screwed into or out of the cavity. Two lines are available:

- 470-600 MHz range; and
- 600-800 MHz range.

The input and output coupling are controlled by the area of variable loops in the cavities. As these are pushed further into the cavity, the effective area increases, resulting in more magnetic lines within the cavity being intercepted and thereby tighter coupling. The intercavity coupling is controlled by the depth of the capacitive probes within each cavity

The use of both capacitive and magnetic coupling results in a bandpass that is symmetrical in off-channel rejection. The bandpass filter is normally aligned to be slightly overcoupled. This results in a suppression of the out-of-band ±4.5 MHz products of approximately 14 dB. The overall insertion loss of this section is approximately 0.5 dB.

2. OUTPUT ALIGNMENT

REQUIRED EQUIPMENT:

The following test equipment is required to align the output of the XLS1000 transmitter:

- 0-1,000 MHz Sweep Generator (Wavetek 1080 or equivalent);
- X-Y Oscilloscope (Hitachi V-212 or equivalent);
- 50 Ω detector (TTC 8520-301 or equivalent);
- Wiltron return loss bridge 62NF50;
- 7/8"-N adaptor (Andrew 2260B or equivalent);
- HN female-to-N female adaptor;
- 50 Ω load (Microlab TA6MN or equivalent);
- 50 Ω coaxial cables for connections.

Note that the first four Items can be replaced by an appropriate network analyzer and its associated accessories.

PROCEDURE

1. Set the sweep generator to the channel of operation.
2. Sweep width should be adjusted to 2 MHz/division.
3. A reference-setting sweep should be sent directly into the detector set for seven divisions of deflection on the scope.
4. Connect the equipment as shown in Figure 1.
5. Set L102, L104 and L106 for an approximate on-channel bandpass.

Note: During each of the following steps, fine tune these adjustments to maintain the best possible bandpass.

6. Set L103 and L105 for minimum insertion loss.
7. Flatten the response using L101 and L107.
8. Set L201 and L202 for the out-of-band ± difference beats.

Note: Notch filters L201 and/or L202 may or may not be present. If both filters are present, try each notch on both sides as one combination may have less adverse effects on the bandpass than the other.

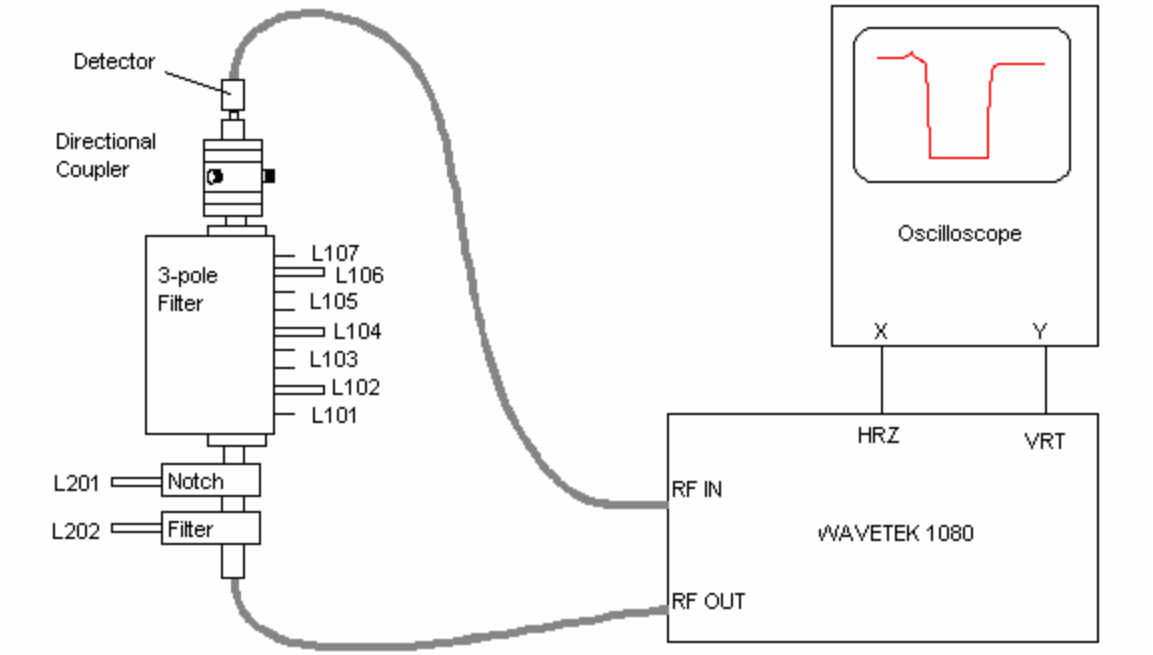

Figure 1. Sweep Alignment Test Set-up

9. Re-flatten the response using L101 and L102.
10. Set width of filter using L103 and L105. The width should be equal to the aural-to-visual difference of +0.5 MHz (total of 5 MHz for NTSC in North America). Ideally, waveshape should appear as shown in Figure 2.

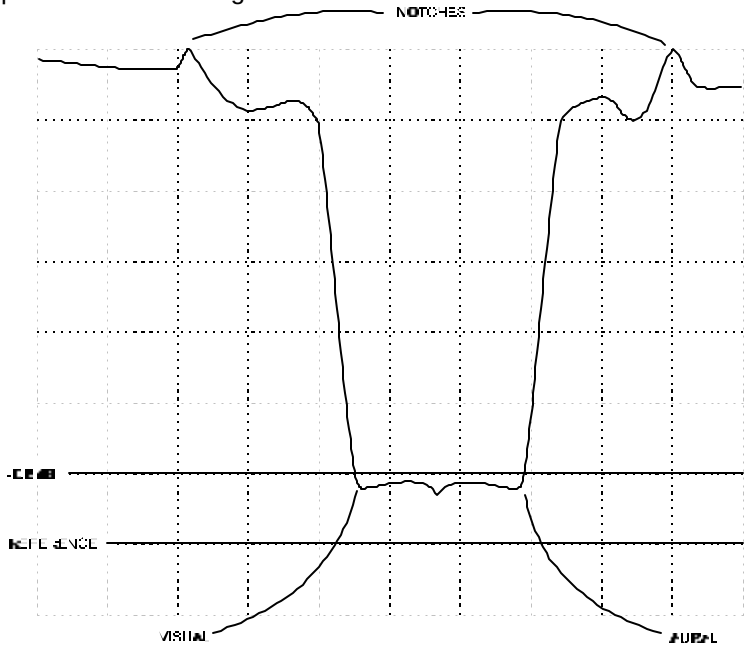

Figure 2. Ideal NTSC Response

11. Adjusting L105 and L107 interactively with each other, tune for proper bandwidth and best out-of-band rejection.
12. Adjusting L103 and L101 interactively with each other, tune for proper bandwidth and best out-of-band rejection.

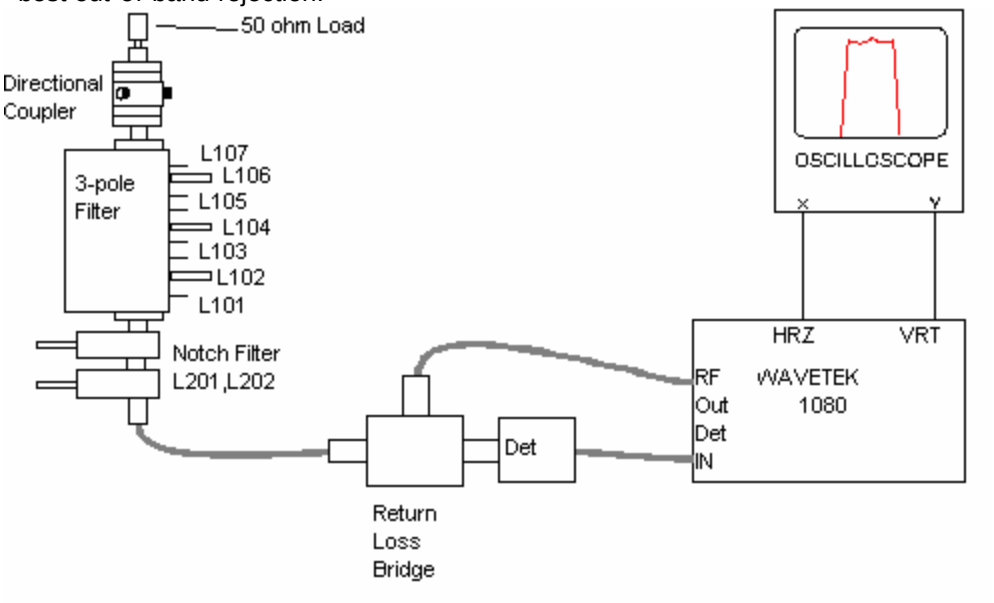

Figure 3. Return Loss Set-up

13. Configure the equipment for return loss measurements, as shown in Figure 3.
14. Return loss should be 30 dB at carriers (Reference Figure 4).

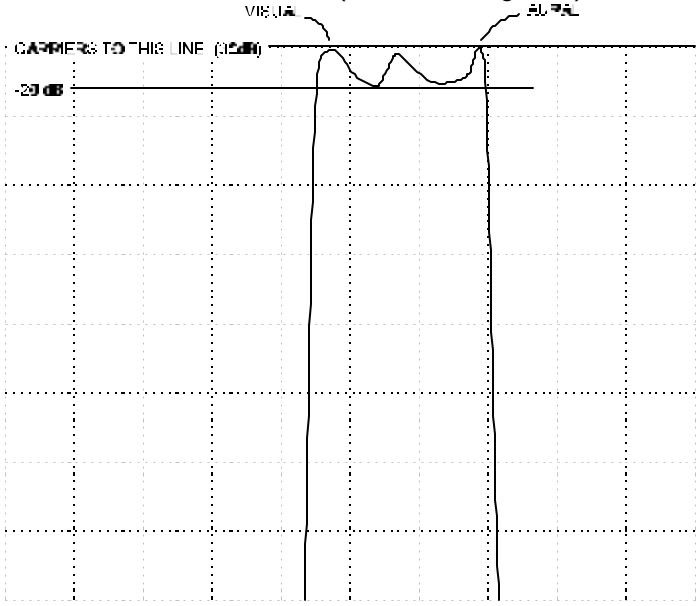

Figure 4. Ideal Return Loss

15. Readjust the filter slightly as needed to obtain proper response.

Note: During this test, the Wavetek 1080 should be set to maximum output.

16. Reconnect the equipment as in Figure 1 and repeat the sweep setup to compare response to the NTSC ideal in Figure 2.

17. If the response is acceptable (less than 0.8 dB loss), return to the return loss setup and lock down all adjustments on the bandpass filter.
18. Notches should be locked down after performing the final fine adjustment with a television signal.

3. OUTPUT CHANNELING INFORMATION

BPF Lines 3 ea.

- 470-600 MHz Part Number 6920-6008
- 600-806 MHz Part Number 6920-6009

Notch Filter Line Discs 2 ea.

- 470-506 MHz Part Number 1314-2016-4
- 506-570 MHz Part Number 1314-2016-3
- 570-690 MHz Part Number 1314-2016-2
- 690-806 MHz No disks used