CONTENTS

FIGURES

1 POWER AMPLIFIER HEATSINK ASSEMBLY

The MXi Power Amplifier Heatsink Assembly 41D2272G1 consists of a fan-cooled heatsink and ten printed circuit board sub-assemblies. The first module is a pre-amplifier, known as the Front-End Module. This first stage is operated in Class A mode. Next is the Driver pallet, which is biased so as to pre-correct for the non-linearity in the final amplifier stage. The next stage is a five-way splitter that splits the RF power so it can be fed to the PA pallets. The final amplifier stage is the PA pallets. After the pallets is the five-way combiner which combines the output power from the PA pallets. The last sub-assembly on the heatsink is the directional coupler which detects the forward and reflected power and provides samples to the control board and a RF test point on the rear panel. Also mounted on the heatsink is a thermal switch, which protects the amplifiers from over-temperature conditions such as the absent of cooling or amplifier over dissipation. This heatsink assembly is mounted in the Amplifier Chassis Assembly 41D2270G1 or G2. Descriptions of each stage are detailed in the following pages.

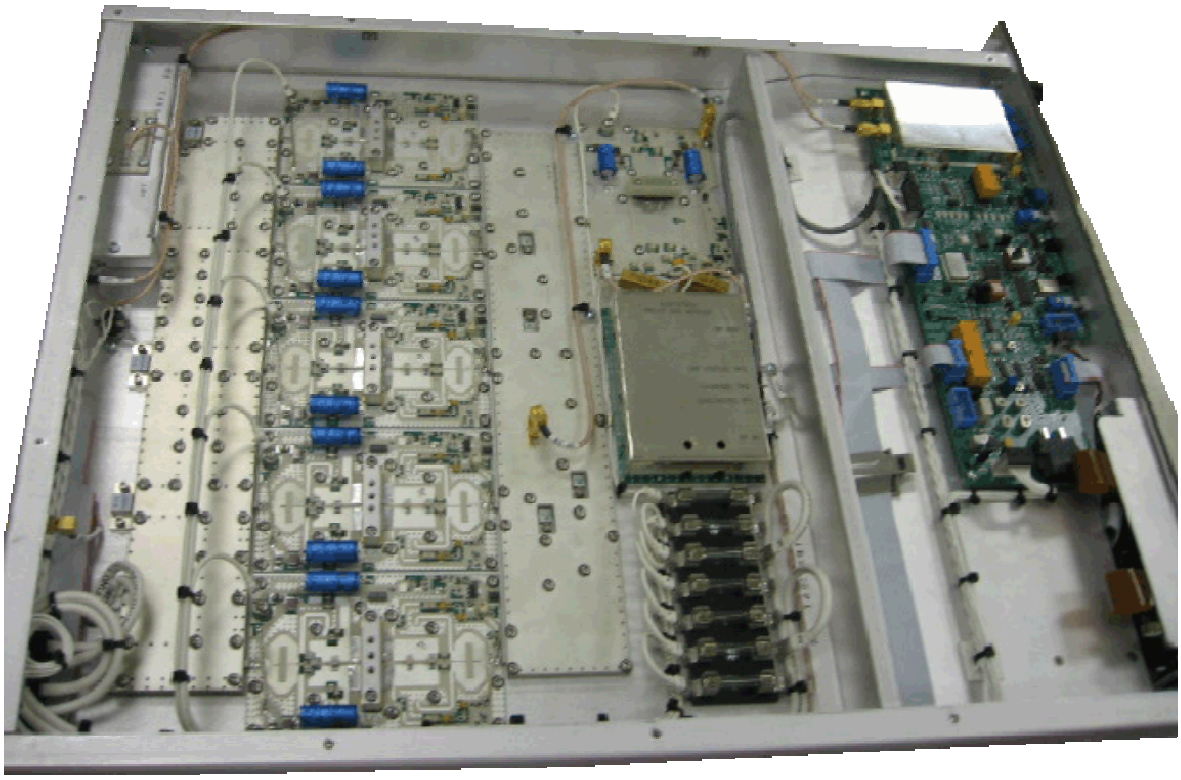


Figure 1 MXi Sub-Assemblies

The above picture illustrates the arrangement of the sub-assemblies on the amplifier heatsink assembly. From right to left are the Front-End and Driver modules. Centered and towards the back are the Splitter, PA modules and the Combiner. At the very back is the Directional Coupler. Strategically installed on the heatsink, is a thermal switch which protects the amplifier from over temperature conditions.

Cooling for the heatsink is provided by a fan array assembly consisting of four 4-inch axial flow +12VDC muffin fans. This array is situated near the front section of the MXi housing underneath the MXi Amplifier Controller PC board. The fans blow air into the finned portion of the heatsink, which exhausts through the rear.

2 FRONT END MODULE ASSEMBLY 21B1473G7

Drawing Reference: Figure 2 and Figure 3

The front end module performs several distinctive functions. Firstly, it serves as a pre-amplifier, which boosts the signal from the up-converter by approximately 9dB. This module also contains a phase shift circuit and a variable attenuator; both adjustments are available and set to maximum and do not need to be adjusted in the MXi amplifier. These circuits are only used for adjusting phase and gain balance between two paralleled amplifiers.

The RF signal is fed to the amplifier through hybrid HY1 and attenuator P-AT1. Refer to Figure 3.

HY1, along with associated components CR1, CR2, C1 through C6, R1, R2 and RV1 act as a phase shifter. P-AT1 is a variable attenuator. The attenuation is controlled by RV2. Typically, RV2 is adjusted for minimum attenuation (fully clockwise) during the bench testing of the module. Once this is done, RV2 is not adjusted again.

U1 is a hybrid linear amplifier with a nominal gain of 17.5dB. The typical operating point of the amplifier in this application is well below the 1 Watt rating of the hybrid.

The power to the Front-End module (+32VDC) comes in at TP2.

The control voltage at TP1 comes from the AGC and VSWR cutback circuit in controller board. This voltage corresponds to the output power of the final amplifier. If the AGC circuit is enabled and the output power tries to increase, TP1 voltage increases, thus maintaining the output at the pre-set level. Similarly, if the reflected power increases past the VSWR cutback setting, TP1 increases and the output power is reduced.

The higher the voltage at TP1, the higher the attenuation in the module, therefore, lower the overall output power.

RF STATUS (TP3) and as mentioned above the PHASING control (RV1) and GAIN control (RV2) are other features of this module which are not applicable to this amplifier.

3 DRIVER MODULE 21B2708G3

Drawing references: Figure 4 and Figure 5.

The Driver Pallet is located in the front of the Power Amplifier. It is the second component in the signal flow of the Power Amplifier Module after the VSWR PC Board.

The design of the Driver Module 21B2708G3 is based on the device MRF6V3090N. It is a Lateral N-channel Enhancement-Mode Power MOSFET capable of 90W (rated power). However, for this application and the desired linear performance, its output to the final stage is significantly below this.

Components C1 through C6, along with the associated printed circuit traces, form the matching network to the gate of the push-pull transistor Q1. Similarly C7 through C14, along with associated stripline traces provide output matching on the drain of the device. C15, C16, C19 and C20 provide the DC blocking of the supply. The rest of the capacitors provide DC blocking of the bias voltage.

DC power enters the module through a screw terminal connection and is fed to the drain of the device via L1 and L2 with bypass capacitors. Bias for the devices is provided via combination of resistors, capacitors and stripline traces.

The bias circuit provides two functions; precision gate bias setting and external shutdown.

The bias voltage is adjusted using R11 from a regulated source provided by U1. Thermistor R18 provides thermal stability for the bias.

The source of the bias voltage is a reference IC, U1, which has its ground reference terminal connected to the collector of Q5. Q5 is biased using R10 and R16 to provide thermal compensation.

When no Shutdown (5V) is applied at R7, the precision reference is active and provides 6.2VDC to the level adjustment circuit R21, R11 and R17. When R11 has been set to achieve 1.4A bias current to the pallet, a bias voltage of approximately 2.6 to 2.7VDC is applied to the gates of the FETs

4 PA PALLET ASSEMBLY 21B2729G1

Drawing references: Figure 6 and Figure 7.

The Power Amplifier pallet is a FET amplifier assembly containing a stripline balun system. The baluns are used for impedance matching and coupling signals at the input and output of the pallet. It is a practical implementation of the coaxial-based solution on a broadside-coupled horizontal stripline structure.

The amplifier circuit is based on the Laterally Double-Diffused MOSFET Q1. Capacitors C1, C2, C3 and C4 along with the associated printed circuit traces, form the matching network to the gates of Q1. Similarly, C5 through C14 along with associated stripline traces provide output matching on the drain of the device. C22, C23, C26, C27, C28, C29 provide DC blocking of the supply. The rest of the capacitors provide DC blocking for bias voltage.

DC power +50VDC enters the module through a screw terminal connection VDD. This DC voltage is fed to the drains of the device via L1 and L2 with bypass capacitors. Bias for the devices is provided via combination of resistors, capacitors and stripline traces.

The bias circuit is located on the 21B2729 board at the input side of the pallet. It provides two functions; precision gate bias setting and external shutdown. The pallet's shutdown function is used in certain applications where the pallet is used as a driver amplifier.

The bias voltage is adjusted using R11 from a regulated source provided by U1. Thermistor R18 provides thermal stability for the bias.

The source of the bias voltage is a reference IC, U1, which has its ground reference terminal connected to the collector of Q5. Q5 is biased using R10 and R16 to provide thermal compensation.

When no Shutdown (5V) is applied at R7, the precision reference is active and provides 6.2VDC to the level adjustment circuit R21, R11 and R17. When R11 has been set to achieve 1.4A bias current to the pallet, a bias voltage of approximately 2.6 to 2.7VDC is applied to the gates of the FETs.

5 FIVE-WAY SPLITTER/FIVE-WAY COMBINER

Drawing reference: Figure 8 to Figure 11

The splitter utilizes a combination of hybrid 4-port quadrature (90° phase difference) couplers that require terminations on the 4th port. The termination maintains isolation between the two output ports of the individual hybrids. The input section is a 2.22dB hybrid which feeds a 3dB hybrid from one output port and a 1.76dB hybrid from the other port. One output of the 1.76dB hybrid further feeds another 3dB hybrid.

The splitter provides five equal amplitude signals to the pallet amplifier inputs with the proper phase relationship so that the combiner (a reverse image of the splitter) will provide a single output at the desired connector. Any phase and / or amplitude differences will result in increased dissipation in the combiner isolation terminations and a corresponding reduction in output power.

The five-way splitter and five-way combiner cover the entire UHF television band (470-860MHz). The combiner can have in excess of 1.5dB unbalance at some frequencies and still combine the signals with less than 0.1dB loss to the reject loads.

The splitter and combiner are constructed using a stacked arrangement of three separate PCBs. All of the stripline traces are found on the middle PCB and each hybrid coupler is formed using broadside coupled lines on opposite sides of the middle board. The two outside PCBs support the ground planes required above and below the stripline. Cutouts are made in the upper and lower ground plane PCBs to allow access to the connection points on the middle layer. Direct connections are made using short lengths of bus wire soldered between the combiner inputs and each amplifier pallet output. These short connections minimize the phase errors and reflections that can occur with many cable interfaces.

6 DIRECTIONAL COUPLER 21B2746G1

Drawing reference: Figure 12 and Figure 13

At the rear of the heatsink and fed by the output of the combiner is a directional coupler which is constructed from edge coupled transmission lines. This is also a 4 port device similar to the 3dB couplers, except the coupling is much weaker (-40dB nominal in this case). The input and output port of the directional coupler is the main output 50Ω transmission line, while the other two ports are the ends of the coupled line. The coupled line is simply a second 50Ω transmission line laying parallel and spaced some distance away from the main line. The coupled port closest to the amplifier output connector is terminated by a 51Ω resistor and the other coupled port is directly connected to the centre pin of the 'RF-TP' (RF Test Point) BNC connector located on the rear panel of the amplifier. The primary function of this directional coupler is to provide a low power RF sample of the forward power appearing at the amplifier combined output. The nominal coupling is given as -40dB, but the coupling does vary with frequency from about -43dB at 470MHz to about -38dB at 860MHz.

7 BENCH TEST PROCEDURES

The following procedures are test instructions for the amplifier modules comprising the MXi amplifier.

7.1 FRONT-END MODULE, *21B1473G7*, BENCH TEST PROCEDURE

- Connect +28V to TP2. Limit the power supply current 0.5A. Check that the current consumption is about 0.30A.
- Apply a 0dBm (1mW) RF input to the amplifier.
- Turn RV2 fully clockwise. The Front-End module should have a gain of about 11dB. Adjusting RV2 from one extreme to the other should vary the gain by 20dB. Set RV2 fully clockwise after checking the range (maximum Gain)
- Set phasing adjustment, RV1, fully clockwise (Phasing not required in this model).
- RF Mute Check: Connect a variable power supply to TP1. Gradually increase the voltage until the gain drops by 20dB or more. The applied voltage should be about 7.0 volts in this condition.
- Telemetry (not used on all models): Monitor TP3. Note that the voltage on TP3 decreases to 0.0V when RF output has been muted.

7.2 DRIVER PALLET, *21B2708G3*, BENCH TEST PROCEDURE

- BIAS SETTING: Connect a 50-Ohm load to the output of the Driver pallet.
  - Before applying +50V to the module, adjust R11 fully counter-clockwise (CCW). Limit the power supply current to 1.0A.
  - Apply +50V to the B+ terminal. Monitor the Drain current and adjust R11 clockwise (CW) for a current of **0.35A ± 0.05A**.
  - Proceed to the next step if a network analyzer or similar equipment is available.
- RF SWEEP: Check that the gain of the Driver pallet, in the frequency range of 470MHz to 806 MHz. is between 20 to 22dB.

7.3 PA PALLET 21B2729G1 BENCH TEST PROCEDURE

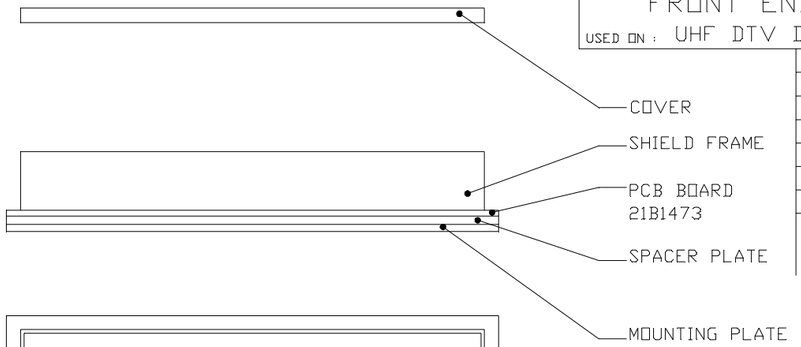
- BIAS SETTING: Connect a 50-Ohm load to the output of the PA pallet.
  - Before applying +50V to the module, adjust R11 fully counter-clockwise (CCW). Limit the power supply current to 2.0A.
  - Apply +50V to the B+ terminal. Monitor the Drain current and adjust R11 clockwise (CW) for a current of **1.45A ± 0.05A**.
  - Proceed to the next step if a network analyzer or similar equipment is available
- RF SWEEP: Check that the Gain of the PA pallet, in the frequency range of 470MHz to 806MHz, is between 20 to 22 dB.

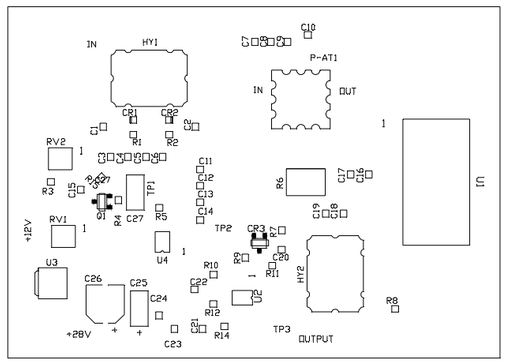
LARCAN	DWG NO.	SHT 1 OF 1	REV 5.1

TITLE: FRONT END

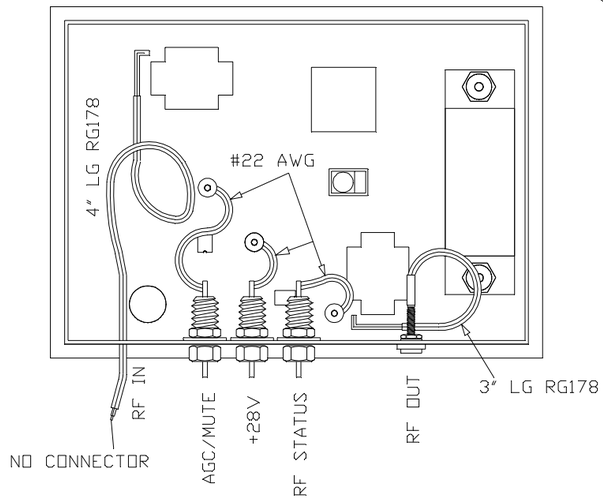
USED ON : UHF DTV DRIVER

	REVISIONS	APPR
1	RN 98-160, MAY 98 H.D	S.H.
2	RN 98-162, JUNE 98 D.S.	S.H.
3	RN 99-243, APR 27,RM, ADDED C27	
4	RN 99-438, SEPT 17 H.D.	S.H.
5	RN03-130 4 APR. 03 HV	L.C.
5.1	RN03-308 25 AUG. 03 SS	





UHF S.S. FRONT END PCB 21B1473 REV.3
ASSEMBLY G1



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DWG NO.	SHT 1 OF 1	REV 5.1
DRAWN BY : H.DRAPPEL		CHKD BY : S.HAIDAU
NEXT ASSY:	DATE: 02:MAR:98	SCALE : 1/1
DO NOT SCALE DWG.	SAVED AS :1B147301rev5.1	

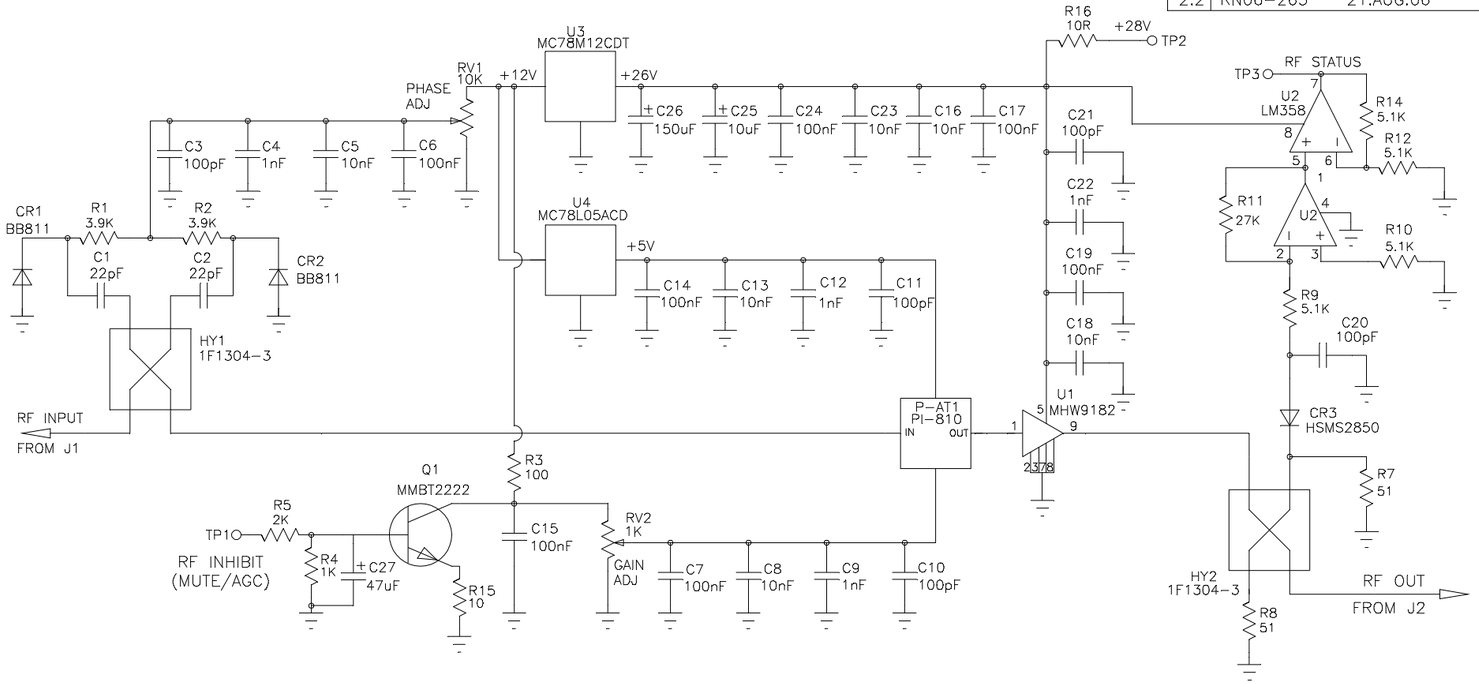
Figure 2 21B1473 MXi Front End UHF DTV Driver Assembly

LARCAN	DWG NO.	SHT 1 OF 1 11A1354S1	REV 2.2

TITLE SCHEMATIC –UHF/DTV FRONT END

USED ON : UHF/DTV

	REVISIONS	APPR
1	RN99–243 27APR99 RM ADDED C27	AS
2	RN99–412 26AUG99 RM ADDED R15;C27 FROM 10 TO 47uF	AS
2.1	RN00–264 26SEP00 D.S	AS
2.2	RN06–263 21.AUG.06 D.L.	



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DWG NO.	SHT 1 OF 1 11A1354S1	REV 2.2
DRAWN BY : DANIELA S.	CHKD BY : S.H.	
NEXT ASSY: 21B1473		
DO NOT SCALE DWG.	SAVED AS : 1A1354S1R2_2	DATE: 18:JUN:98 SCALE : NONE

Figure 3 11A1354 MXi Front End UHF DTV Driver Schematic

TOLERANCES	
UNLESS OTHERWISE SPECIFIED	
3 DECIMAL PLACES	±.005
2 DECIMAL PLACES	±.010
FRACTIONS	±1/64
ANGLES	±1°
MACHINE FINISH	63

ALL DIMENSIONS ARE IN INCHES UNLESS NOTED OTHERWISE

LARCAN

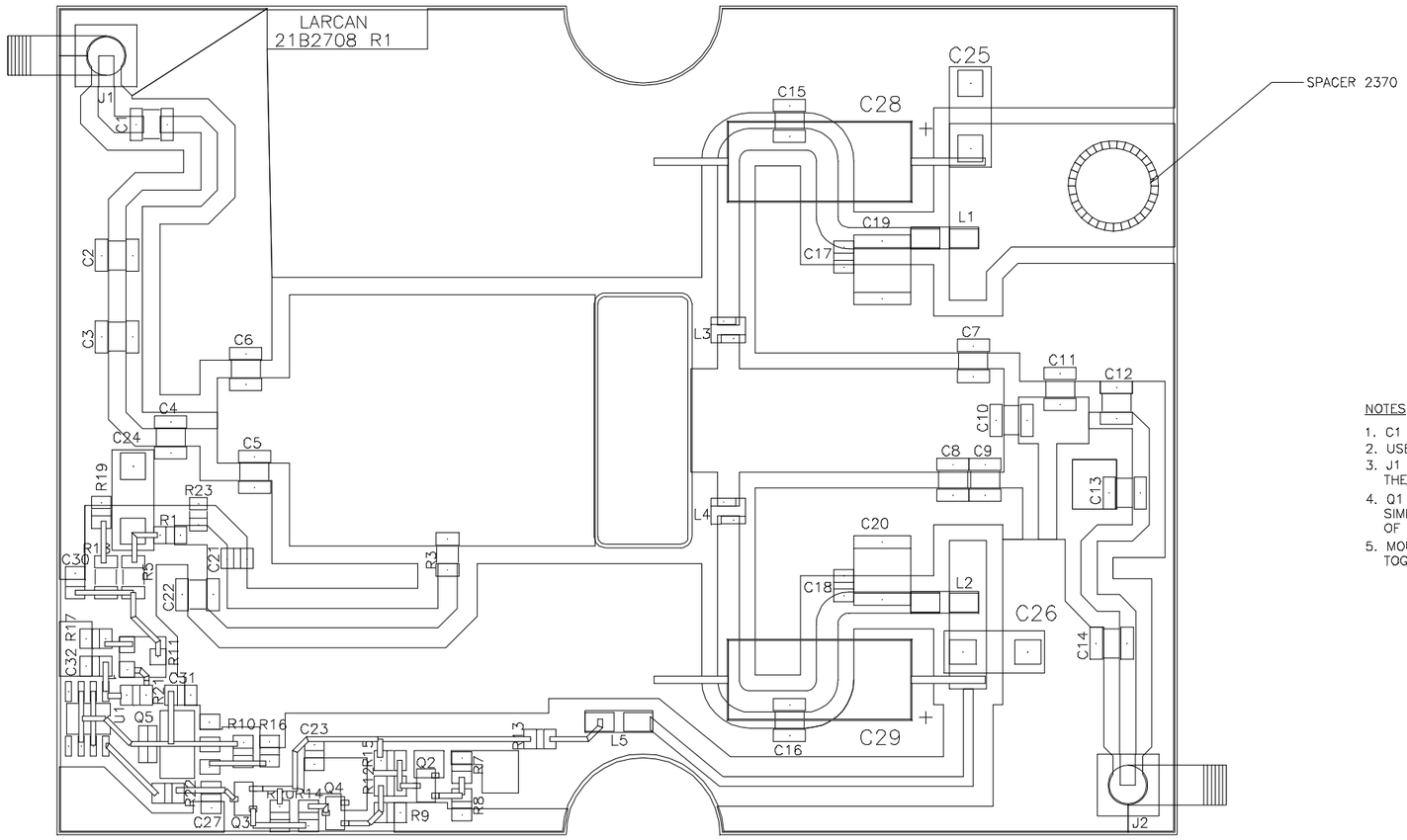
DWG NO.	SHT 1 OF 1	REV
	21B2708A1	1.1

TITLE

PALLET AMPLIFIER

USED ON :

	REVISIONS	APPR
0	RN09-218 18 NOV 09 DS	AS
1	RN11-038 28 JAN 11 DS	AS
1.1	RN11-089 6 APR11 DCB	



SCALE : 2/1

NOTES

1. C1 – MOUNT ON SIDE EDGE.
2. USE OVEN TEMPERATURE AS FOR PCB 21B2705.
3. J1 AND J2 SHOULD BE SPACED SLIGHTLY OFF THE BOARD SO AS NOT TO SHORT OUR CONNECTOR
4. Q1 SHOULD HAVE A THIN LAYER OF RT7203U00000 OR SIMILAR THERMAL COMPOUND APPLIED TO THE UNDERSIDE OF DEVICE
5. MOUNTING SCREWS FOR Q1 TO BE TORQUED AT 3 INCH LBS TOGETHER WITH CLAMP

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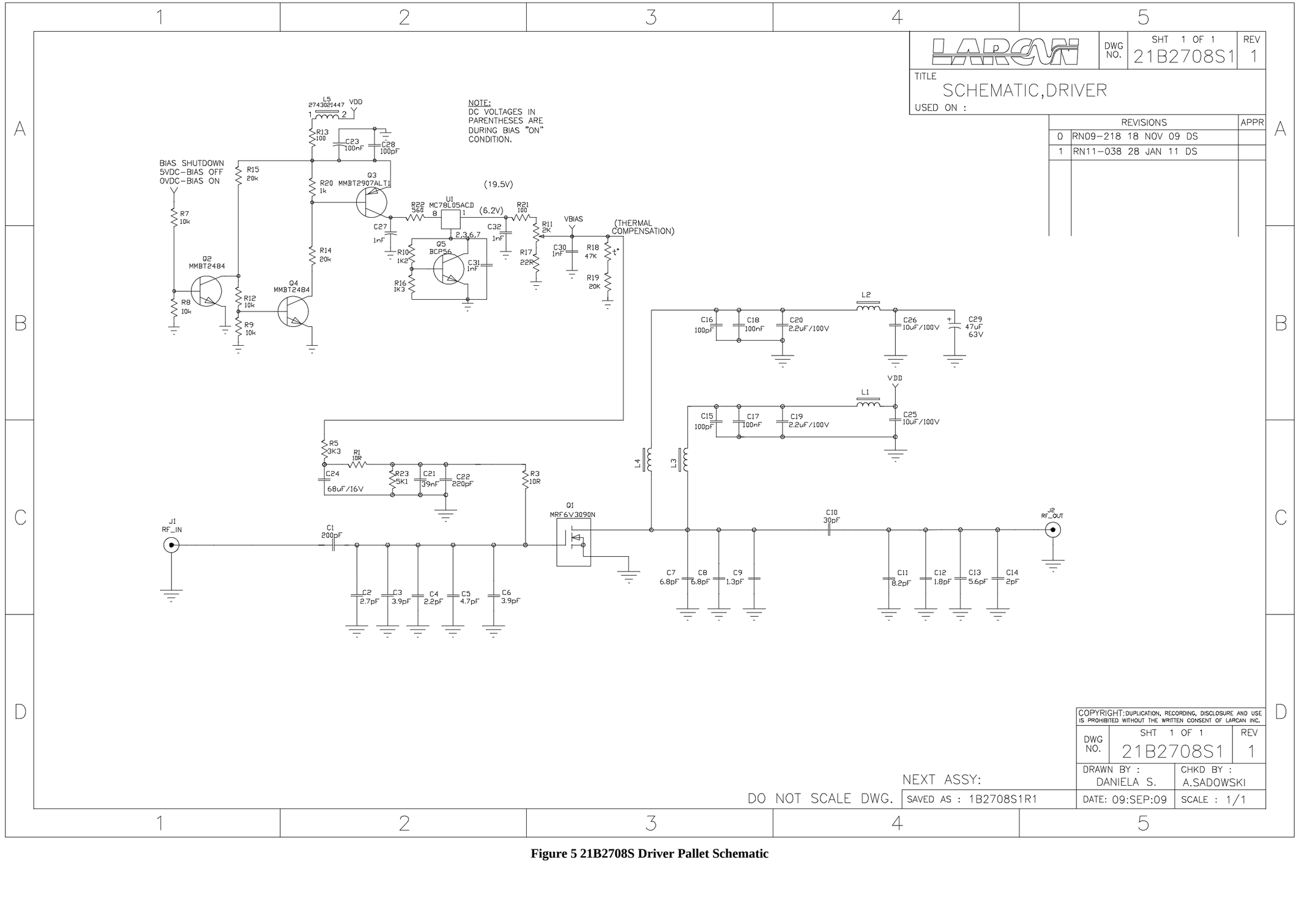
DWG NO.	SHT 1 OF 1	REV
	21B2708A1	1.1
DRAWN BY : DANIELA S.		CHKD BY : A.SADOWSKI
DATE: 18:NOV:09		SCALE : 2/1

NEXT ASSY:

DO NOT SCALE DWG. SAVED AS : 1B2708A1R1.1

Figure 4 21B2708S Driver Pallet Assembly



LARCAN

DWG NO.	SHT 1 OF 1	REV
	21B2708S1	1

TITLE
SCHEMATIC,DRIVER

USED ON :

REVISIONS		APPR
0	RN09–218 18 NOV 09 DS	
1	RN11–038 28 JAN 11 DS	

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DWG NO.	SHT 1 OF 1	REV
	21B2708S1	1
DRAWN BY : DANIELA S.		CHKD BY : A.SADOWSKI
DO NOT SCALE DWG.	SAVED AS : 1B2708S1R1	DATE: 09:SEP:09
NEXT ASSY:		SCALE : 1/1

Figure 5 21B2708S Driver Pallet Schematic

TOLERANCES	
UNLESS OTHERWISE SPECIFIED	
3 DECIMAL PLACES	±.005
2 DECIMAL PLACES	±.010
FRACTIONS	±1/64
ANGLES	±1°
MACHINE FINISH	63

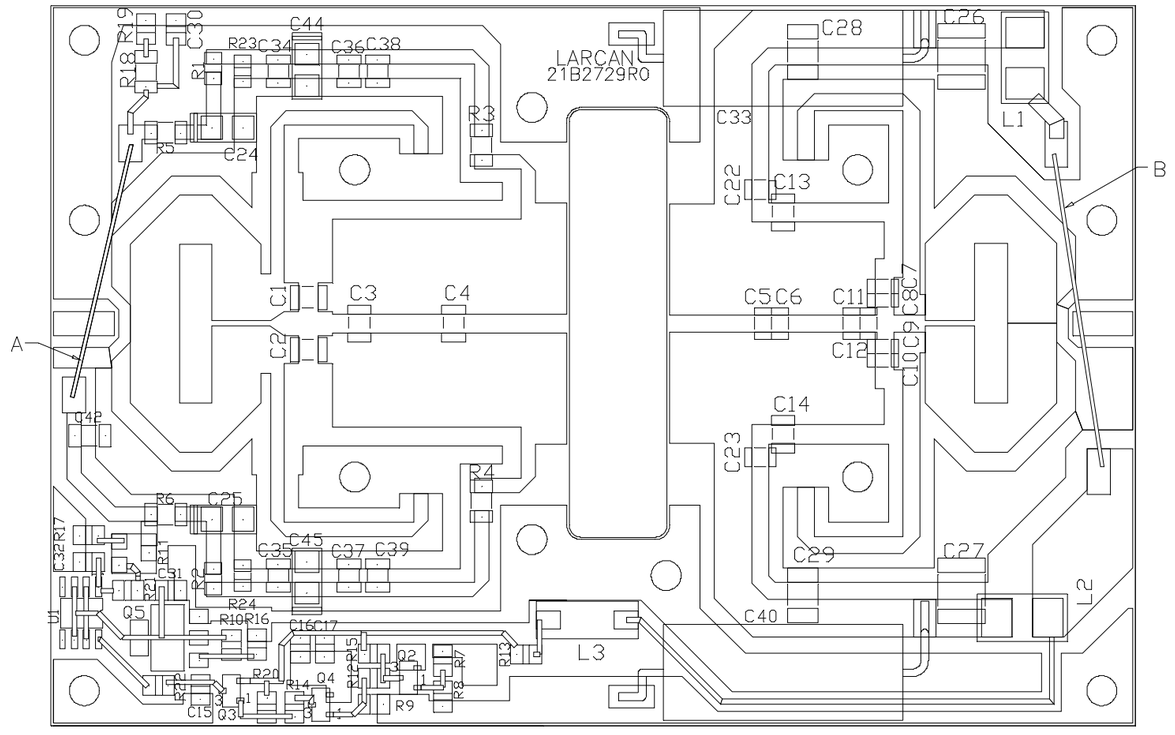
ALL DIMENSIONS ARE IN INCHES UNLESS NOTED OTHERWISE

LARCAN

DWG NO.	SHT 1 OF 1	REV
	21A2729A1	0

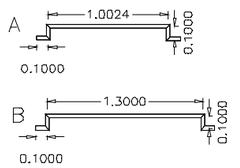
TITLE
PALLET AMPLIFIER
USED ON :

REVISIONS		APPR
0	RN10-014 25 JAN 10 DS	



ASSEMBLY

1. Capacitors C1,2,3,4,5,6,7,8,9,10,11,12,22,23 mount on side edge
2. Capacitor C17 is not used.
3. Install two jumpers A and B-buss wire AWG 18.



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DWG NO.	SHT 1 OF 1	REV
	21B2729A1	0
DRAWN BY : DANIELA S.		CHKD BY : A.SADOWSKI
NEXT ASSY:		
DO NOT SCALE DWG.	SAVED AS : 1B2729A1R0	DATE: 25:JAN:10
		SCALE : 2/1

Figure 6 21B2729A1 Pallet Circuit Assembly

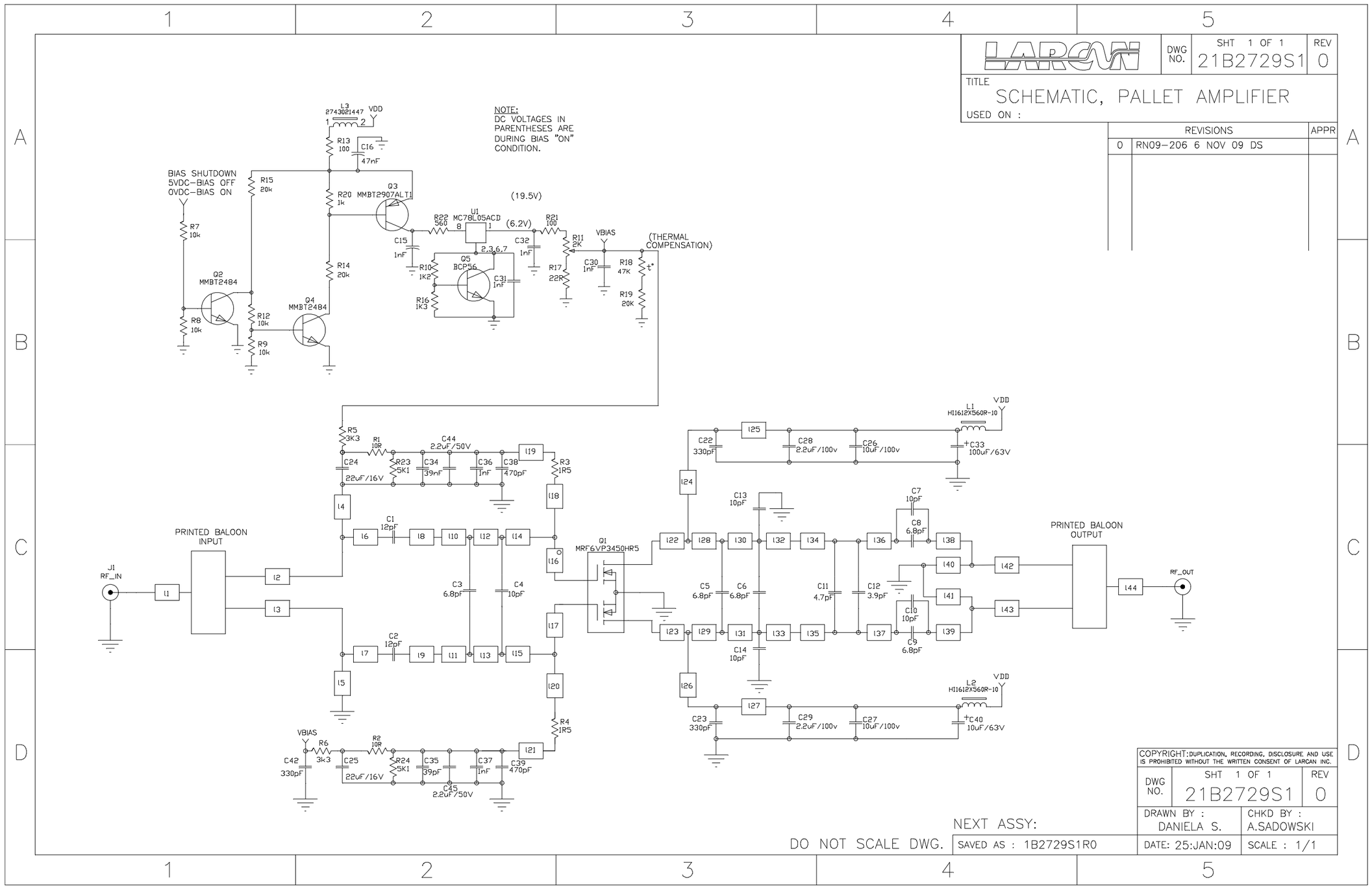


Figure 7 21B2729S1 Pallet Circuit Schematic

TOLERANCES	
UNLESS OTHERWISE SPECIFIED	
3 DECIMAL PLACES	±.005
2 DECIMAL PLACES	±.010
FRACTIONS	±1/64
ANGLES	±1°
MACHINE FINISH	63

LARCAN

DWG NO.	SHT 1 OF 1	REV
	21B2745A1	0

TITLE ASSEMBLY 5 WAY SPLTR MXi501

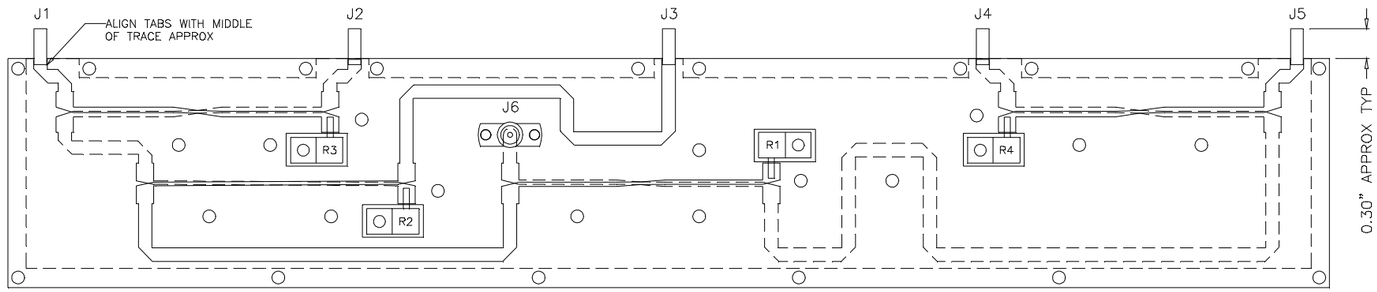
USED ON : MXi501 UHF AMPLIFIER

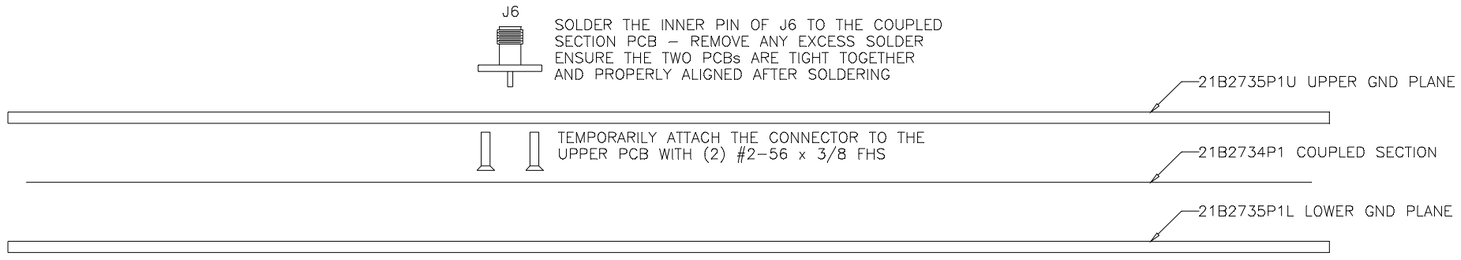
ALL DIMENSIONS ARE IN INCHES UNLESS NOTED OTHERWISE

REVISIONS			APPR
0	RN10-003	5 FEB 2010 MPT	

OUTPUT TABS
0.35 LONG x 0.125 (1/8") WIDE
TIN PLATED COPPER STRIP
4-5MIL THICK (0.004"-0.005")
TYPICAL 5 REQUIRED
NOTE: FLATTEN ENDS AFTER CUTTING

NOTE ON INSTALLING TABS:
OUTPUT TABS ARE SOLDERED TO THE COUPLED SECTION PCB USING THE ABSOLUTE MINIMUM AMOUNT OF SOLDER – WICK ANY EXCESS AWAY
ENSURE THAT THE TABS ARE CENTRED ON THE TRACE AND STRAIGHT (SQUARE TO BOARD EDGE)





ASSEMBLY SEQUENCE
1. INSTALL COPPER OUTPUT TABS ON COUPLED SECTION PCB 21B2734P1 AS SHOWN (SEE NOTES).
2. INSTALL INPUT CONNECTOR J6 ON UPPER GND PLANE AND COUPLED SECTION PCBS AS SHOWN.
3. POSITION TERMINATIONS R1,R3,R4 IN THEIR CUTOUT LOCATION IN THE UPPER GND PLANE WITH THE TABS IN BETWEEN THE UPPER GND PLANE AND THE COUPLED SECTION PCB (MASKING TAPE ON THE UPPER GND PLANE CAN BE USED TO HOLD THEM IN POSITION).
4. POSITION THE LOWER GND PLANE PCB ON THE HEATSINK.
5. INSTALL TERMINATION R2 AND LIGHTLY TIGHTEN ITS MOUNTING SCREWS.
6. POSITION THE PREVIOUSLY ASSEMBLED UPPER GND PLANE AND COUPLED SECTION PCBs ON TOP OF THE LOWER GND PLANE.
7. INSTALL ALL PCB AND TERMINATION MOUNTING SCREWS AND LIGHTLY TIGHTEN.
8. TIGHTEN ALL OF THE PCB MOUNTING SCREWS STARTING NEAR THE MIDDLE OF THE ASSEMBLY AND WORKING TOWARD THE EDGES.
9. TIGHTEN THE TERMINATION MOUNTING SCREWS.

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NEXT ASSY:

DO NOT SCALE DWG.

DWG NO.	SHT 1 OF 1	REV
	21B2745A1	0
DRAWN BY : M.THIELE	CHKD BY :	
SAVED AS : 1B2745A1R0.dwg	DATE: 5:FEB:2010	SCALE : FULL

LQS-052 Rev 0

PLOT SCALE 1:1.20

Figure 8 21B2444A1 5 Way Splitter Assembly

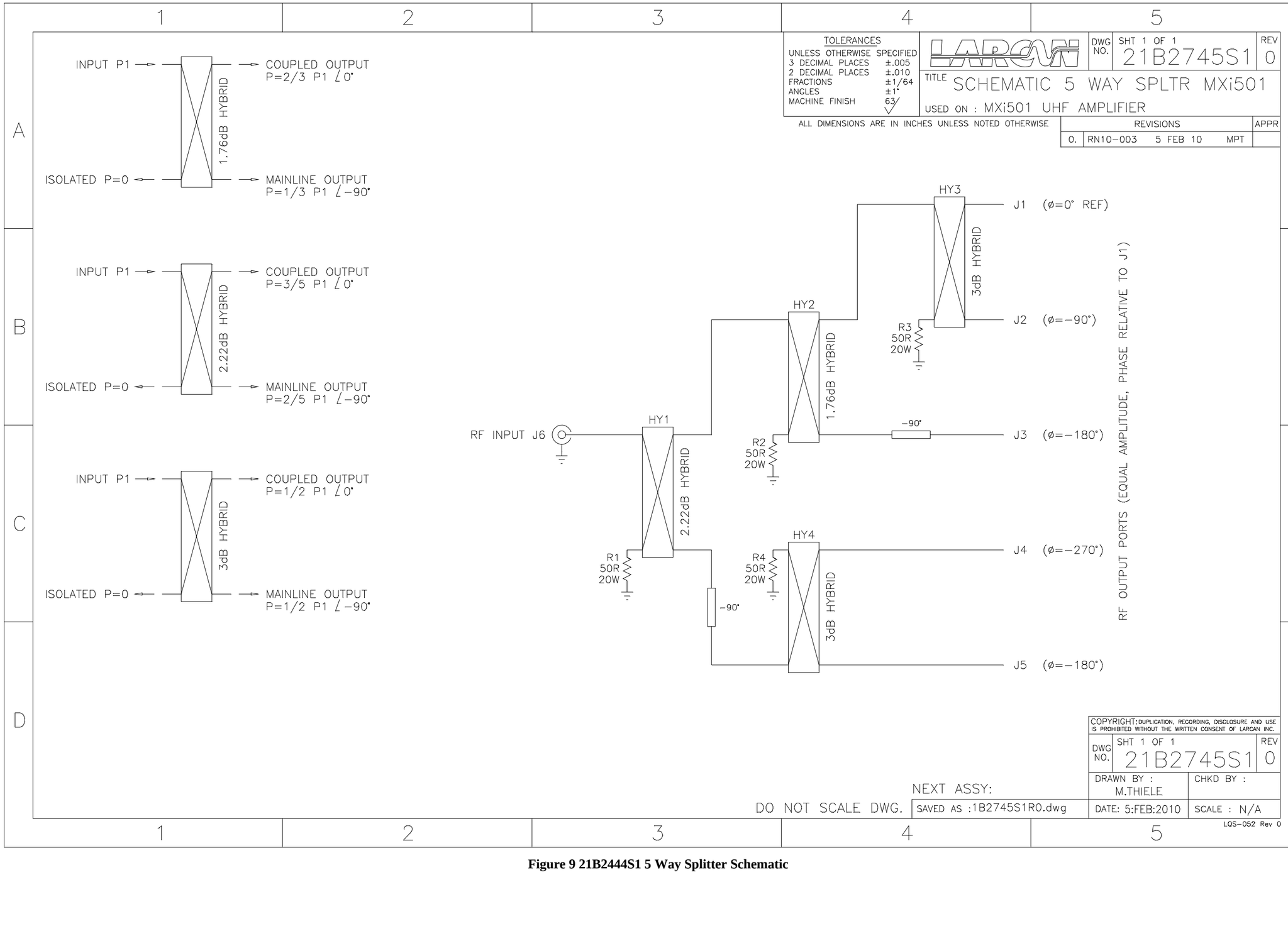


Figure 9 21B2444S1 5 Way Splitter Schematic

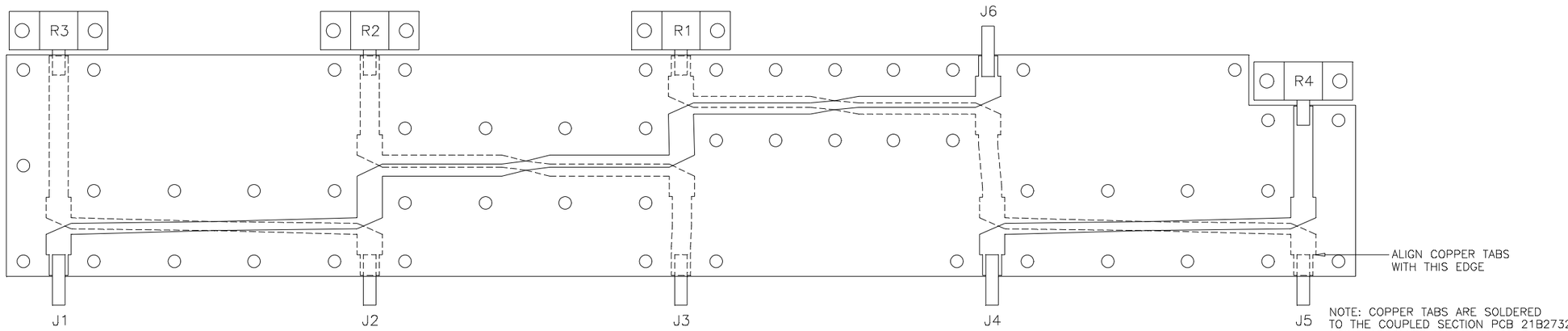
				APPR	TOLERANCES	LARCAN
0.	RN10-003	5 FEB 10	MPT		UNLESS OTHERWISE SPECIFIED 3 DECIMAL PLACES ±.005 2 DECIMAL PLACES ±.010 FRACTIONS ±1/64 ANGLES ±1° MACHINE FINISH 63	DWG NO. 21B2744A1 SHT 1 OF 1 REV 0

TITLE ASSEMBLY 5 WAY COMB MXi501

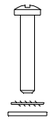
USED ON : MXi501 UHF AMPLFIER

NOTE R1-R4: DO NOT INSTALL POWER TERMINATIONS R1-R4 UNTIL MOUNTING THE BOARDS ON THE HEATSINK. NOTE THAT POWER TERMINATION TABS ARE NOT SOLDERED.

INPUT / OUTPUT TABS
0.50 LONG x 0.125 (1/8") WIDE
TIN PLATED COPPER STRIP
4-5MIL THICK (0.004"-0.005")
TYPICAL 6 REQUIRED
NOTE: FLATTEN ENDS AFTER CUTTING



NOTE: COPPER TABS ARE SOLDERED TO THE COUPLED SECTION PCB 21B2732P1 USING ABSOLUTE MINIMAL AMOUNT OF SOLDER - WICK AWAY ANY EXCESS ENSURE TABS ARE CENTRED ON THE TRACE AND STRAIGHT (SQUARE TO THE BOARD EDGE)



#4-40 x 5/8 LONG RHS
#4 TOOTHED L/WSHR
#4 FLAT WASHER
TYPICAL (50) PLACES

ASSEMBLY SEQUENCE:
1. INSTALL COPPER TABS ON COUPLED SECTION PCB 21B2732P1 AS SHOWN (SEE NOTES).
2. POSITION LOWER GND PLANE PCB ON HEATSINK.
3. INSTALL POWER TERMINATIONS R1-R3 (NOT R4) AND LIGHTLY TIGHTEN THEIR MOUNTING SCREWS.
4. POSITION THE COUPLED SECTION PCB OVER THE LOWER GND PLANE PCB.
5. INSTALL POWER TERMINATION R4 AND LIGHTLY TIGHTEN ITS MOUNTING SCREWS.
6. POSITION THE UPPER GND PLANE PCB OVER THE COUPLED SECTION PCB.
7. INSTALL ALL PCB MOUNTING SCREWS AND LIGHTLY TIGHTEN.
8. TIGHTEN ALL PCB MOUNTING SCREWS STARTING NEAR THE MIDDLE OF THE ASSEMBLY AND WORKING TOWARDS THE EDGES.
9. TIGHTEN THE POWER TERMINATIONS R1-R4.

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DO NOT SCALE DWG.

NEXT ASSY:

SAVED AS :1B2744A1R0.dwg

DWG NO. 21B2744A1 SHT 1 OF 1 REV 0	
DRAWN BY : M.THIELE	CHKD BY :
DATE: 5:FEB:2010	SCALE : FULL

LQS-052 Rev 0

Figure 10 21B2445A1 5 Way Combiner Assembly

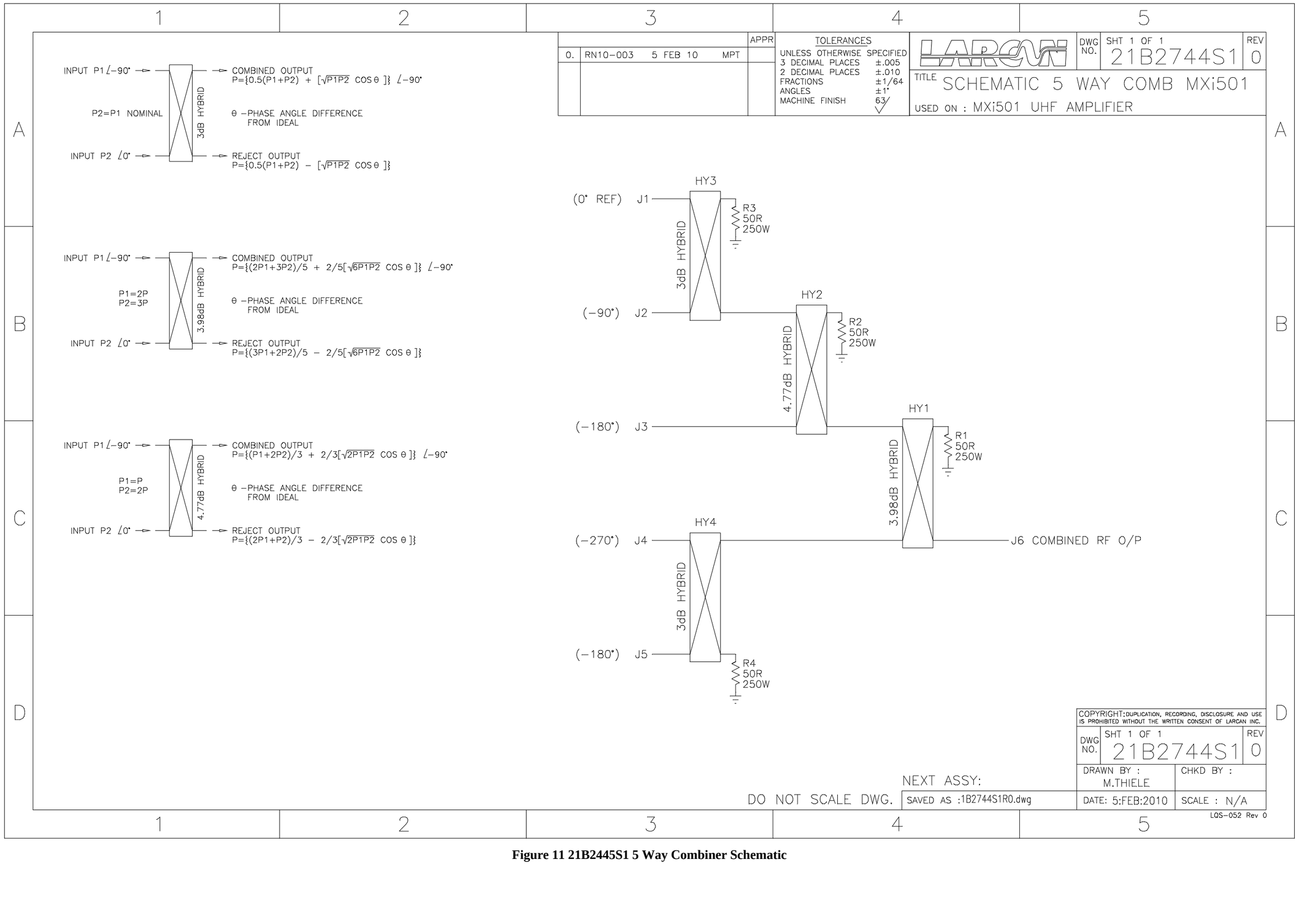
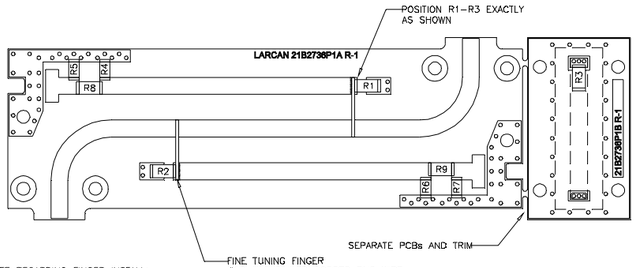


Figure 11 21B2445S1 5 Way Combiner Schematic

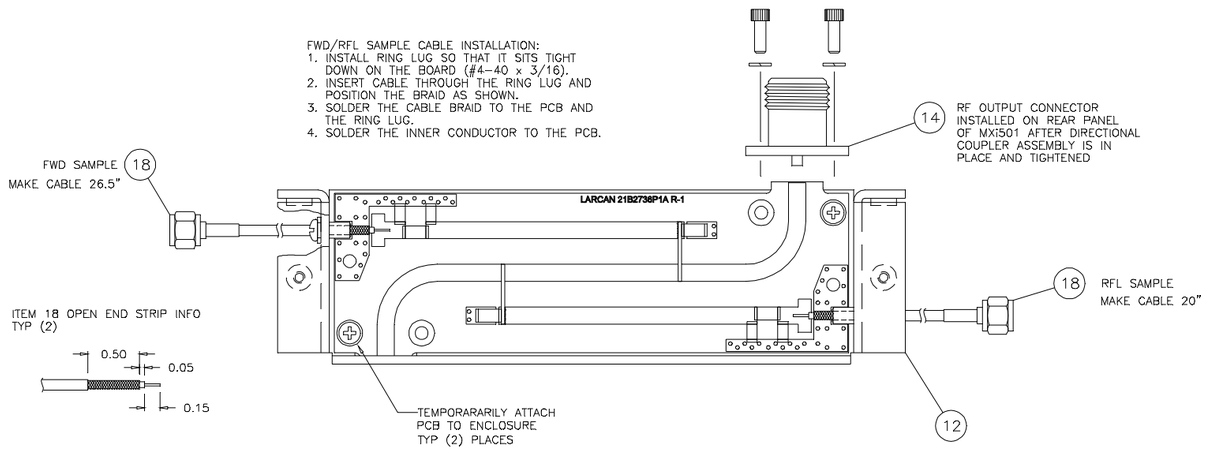
PCB ASSEMBLY: ITEMS 5,7,8,9



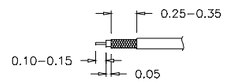
NOTE REGARDING FINGER INSTALL:
PREPARE THE #18 AWG WIRE BY STRETCHING TO REMOVE KINKS AND BENDS. ACCURATELY CUT THE WIRE USING AN EXACTO KNIFE AND REMOVE ANY SHARP EDGES ON THE END THAT OVERLAPS THE MAIN LINE. AFTER SOLDERING THE FINGER IN PLACE, HOLD THE SOLDERED END DOWN AND LIFT UP THE OPEN END. SLIP A 0.020" THICK TEFLON SHIM UNDER THE FINGER AS CLOSE TO THE SOLDERED END AS IT WILL GO. PRESS DOWN ON THE OPEN END SO THAT THE FINGER LAYS PARALLEL TO THE BOARD, BUT 0.020" ABOVE IT.

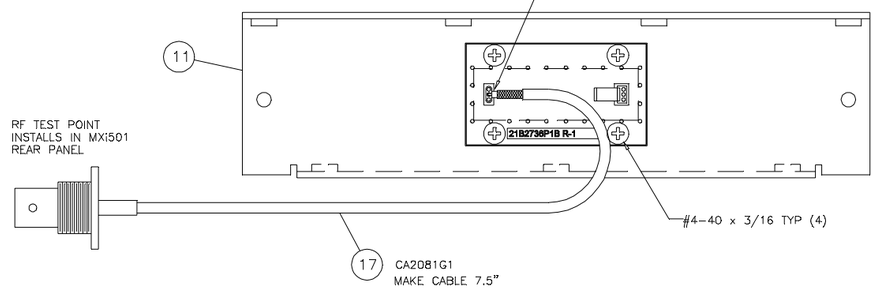
PANDUIT P14–6R–M
RING LUG #14–16
BEND AS SHOWN
TYPICAL 2 REQUIRED

FWD/RFL SAMPLE CABLE INSTALLATION:
1. INSTALL RING LUG SO THAT IT SITS TIGHT DOWN ON THE BOARD (#4–40 x 3/16).
2. INSERT CABLE THROUGH THE RING LUG AND POSITION THE BRAID AS SHOWN.
3. SOLDER THE CABLE BRAID TO THE PCB AND THE RING LUG.
4. SOLDER THE INNER CONDUCTOR TO THE PCB.



ITEM 17 OPEN END STRIP INFO





TEST INFORMATION:
1. ONLY THE DIRECTIOANL COUPLER ASSEMBLY SHOULD BE INSTALLED ON THE MXI501 CHASSIS (NO COMBINER OR PALLETS IN PLACE).
2. THE REAR PANEL MUST BE INSTALLED AS WELL AS THE OUTPUT RF CONNECTOR.
3. INSTALL INPUT TEST FIXTURE PCB 21B2736P2 ALONG WITH SPACER PLATE.
4. ADJUST FINE TUNING FINGERS SO THAT THEY ARE 0.03–0.04" ABOVE THE MAINLINE TRACE AND PARALLEL TO IT.
5. VERIFY THAT THE MAINLINE RETURN LOSS IS 30dB OR BETTER WITH THE COVER INSTALLED.
6. ADJUST THE FINE TUNING FINGERS SO THAT THE DIRECTIVITY OF BOTH THE FORWARD AND REFLECTED VSWR SAMPLE OUTPUTS IS 30dB OR BETTER (COVER ON).
7. VERIFY THAT THE MAINLINE RETURN LOSS IS STILL 30dB OR BETTER (COVER ON).
8. VERIFY RETURN LOSS ON ALL SAMPLE CABLES IS 30dB OR BETTER.
9. VERIFY FWD COUPLING ON THE TEST POINT.

TOLERANCES	
UNLESS OTHERWISE SPECIFIED	
3 DECIMAL PLACES	±.005
2 DECIMAL PLACES	±.010
FRACTIONS	±1/64
ANGLES	±1°
MACHINE FINISH	63

ALL DIMENSIONS ARE IN INCHES UNLESS NOTED OTHERWISE

DWG NO. 21B2746A1 | SHT 1 OF 1 | REV 2

TITLE: ASSEMBLY OP DIR CPLR MXi501

USED ON : MXi501 UHF AMPLIFIER

REVISIONS				APPR
0	RN10–003	5 FEB 2010	MPT	DB
1	RN10–146	20 SEPT 2010	MPT	DB
2	RN10–153	2 DED 2010	DCB	

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DWG NO. 21B2746A1 | SHT 1 OF 1 | REV 2

DRAWN BY : M.THIELE | CHKD BY : D.BROCKLEHURST

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NEXT ASSY:

LQS–052 Rev 0

PLOT SCALE 1:1.20

Figure 12 21B2446S1 Directional Coupler Assembly

				APPR
0.	RN10-003	5 FEB 10	MPT	DB
1.	RN10-146	20 SEPT 10	MPT	

TOLERANCES

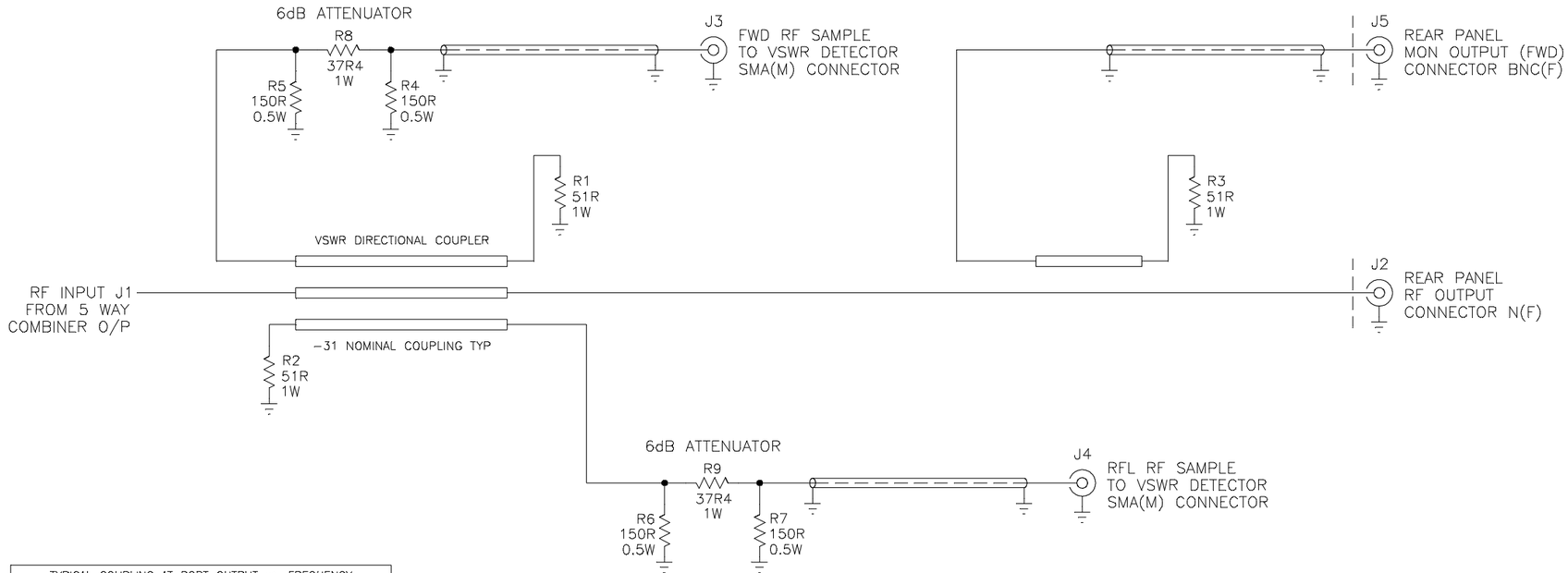
UNLESS OTHERWISE SPECIFIED	
3 DECIMAL PLACES	±.005
2 DECIMAL PLACES	±.010
FRACTIONS	±1/64
ANGLES	±1°
MACHINE FINISH	63

LARCAN

DWG NO. 21B2746S1 | SHT 1 OF 1 | REV 1

TITLE SCHEMATIC OP DIR CPLR MXi501

USED ON : MXi501 UHF AMPLIFIER



TYPICAL COUPLING AT PORT OUTPUT vs. FREQUENCY					
PORT	470 MHz	550 MHz	650 MHz	750 MHz	860 MHz
J3	-37.5dB	-37.1dB	-37.1dB	-37.6dB	-38.6dB
J4	-37.5dB	-37.1dB	-37.1dB	-37.6dB	-38.6dB
J5	-50.6dB	-49.6dB	-48.6dB	-47.7dB	-47.1dB

NOTES:
1. COUPLING AT J3/J4 ±0.5dB
2. DIRECTIVITY AT J3/J4 >30dB
3. COUPLING AT J5 ±1.0dB
4. DIRECTIVITY AT J5 NOT APPLICABLE

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DWG NO. 21B2746S1 | SHT 1 OF 1 | REV 1

DRAWN BY : M.THIELE | CHKD BY : D.BROCKLEHURST

DATE: 5:FEB:2010 | SCALE : N/A

NEXT ASSY:

DO NOT SCALE DWG. | SAVED AS : 1B2746S1R1.dwg

LOS-052 Rev 0

Figure 13 21B2446S1 Directional Coupler Schematic

NOTES