SiBEAM
A Lattice Semiconductor Technology

LATTICE SEMICONDUCTOR

GigaRay™

MOD65412 Wireless Link Module Set

Preliminary **Data Brief**

SB-DB-02006-0.80

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1. General Description

The Lattice MOD65412 Wireless Link Module Set is a two-board wireless link evaluation platform that includes a MOD65410 baseband board that conforms to the PCI Express (PCIe) Half-Mini Card specification and a MOD63422 RF board that includes a printed circuit board (PCB) antenna. The baseband board contains the SB6541 device, a single-chip IEEE 802.11ad-based baseband processor for industrial, and communication applications. The RF board contains the SiI6342 device, a 60 GHz RF transceiver for medium-range access, backhaul, and bridging applications. The baseband and RF boards are connected by a Flexible Printed Circuit (FPC) cable.

The module set can be integrated with a host network processor via PCIe to provide wireless station (STA) or access point (AP) functions in a gigabit network link.

1.1. Applications

- Fixed wireless broadband backhaul and access
- Indoor/outdoor Wi-Fi wireless backhaul
- Indoor/outdoor 4G LTE small-cell wireless backhaul
- Municipal and Enterprise backhaul

1.2. Features

- IEEE 802.11ad single-carrier PHY MCS modes 1-8, with PHY data rate up to 2.3 Gb/s
- IEEE 802.11ad control PHY MCS mode 0
- IEEE 802.11ad channels 2 and 3 (59.4 – 63.7 GHz)
- PCI Express 1.1 x1 interface to host system
- 1.7 Gb/s effective maximum bidirectional TCP/IP throughput
- Transmitter EIRP (typical)
  - 37 dBm @ MCS4
- Rx sensitivity (typical)
  - –86 dBm @ MCS4
- Dual firmware image support with 2 MB flash
- Adaptive beamforming with ±45° steering angle (-3dB point)
- Integrated EMI shield, heat sink and antenna on RF board simplify system integration
- Operating temperature range: –25 °C to +90 °C case temperature; start-up at –40 °C
- Board dimensions:
  - Half-Mini card (30 mm × 26.8 mm × 1 mm)
  - RF board (64 mm × 52 mm × 8.2 mm)
- Linux driver supporting kernel version 3.10 to 4.0
- Regulatory certification: FCC

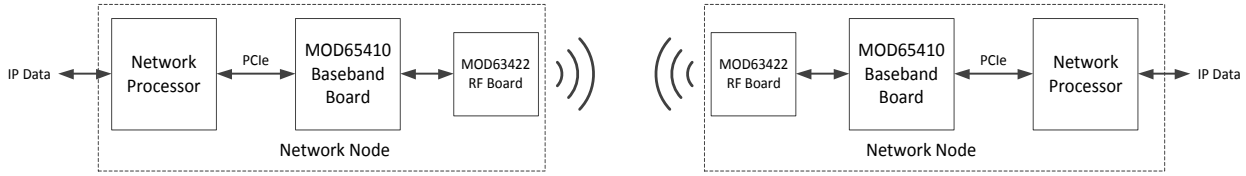

Figure 1.1. Typical Application

2. System Description

2.1. Block Diagram

The MOD65412 Wireless Link Module Set block diagram is presented below (Figure 2.1).

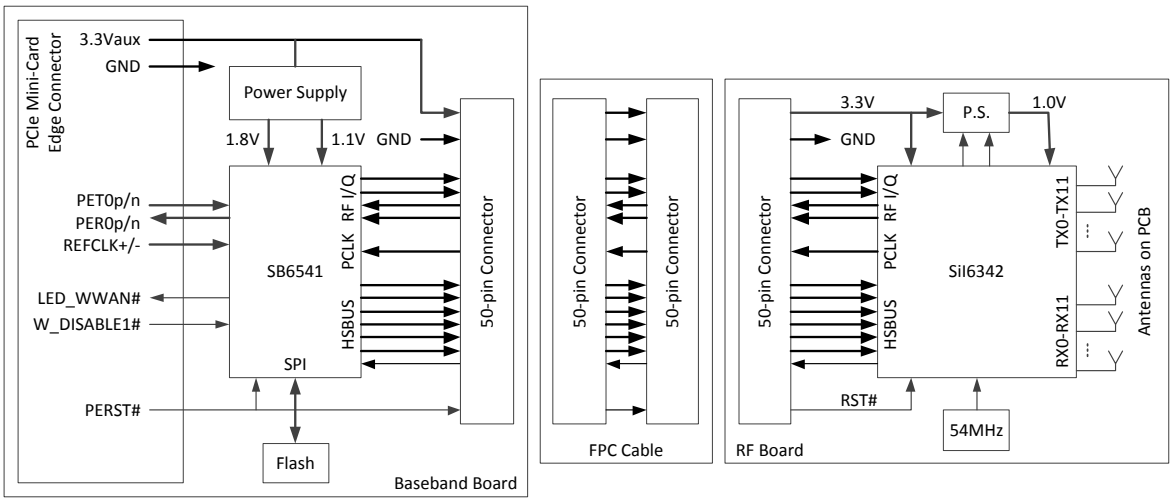

Figure 2.1. Wireless Link Module Set Block Diagram

2.2. Baseband Board Dimensions

The MOD65410 baseband board is a PCI Express Half-Mini Card. Refer to the *PCI Express® Mini Card Electromechanical Specification, Revision 2.0,* for the bare PCB dimensions. The PCI Express system connectoris card edge is 0.8 mm pitch, 52 pins.

The baseband board is 30 mm × 26.8 mm × 4.6 mm, with an EMI enclosure on the top side and without the FPC cable attached. The board is 30 mm × 26.8 mm × 5.1 mm with a standard height FPC connector attached.

The two mounting screws are M2: ISO 7045:2011 M2×0.4 Pan head screws with type H or Z crosscut drive or M2.5: ISO 7045:2011 M2.5×0.45 Pan head screws with type H or Z crosscut drive.

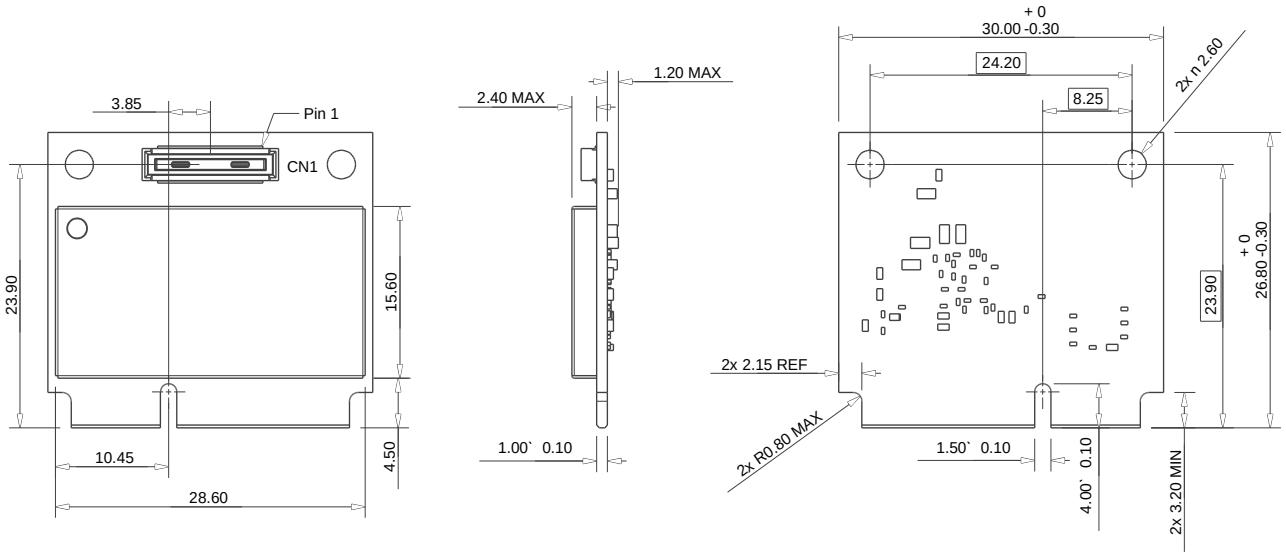

Figure 2.2. Baseband Board Mechanical Dimensions

2.3. RF Board Dimensions

The MOD63422 RF board is 62.6 mm × 51.6 mm × 7.4 mm. The PCB bottom side is covered by a combination EMI shield/heat sink block. There are two M2×0.4 threaded screw holes in the heat sink for attaching a cable retention plate, if needed to prevent the FPC cable from working loose due to shock and vibration. There are four holes in the PCB and heat sink that can be used to mount the module to the system assembly. These holes are 2.4 mm in diameter. M2 wafer head screws are recommended for mounting the module to the system.

The four mounting screws are M2: ISO 7045:2011 M2×0.4 Wafer head screws with type H or Z crosscut drive.

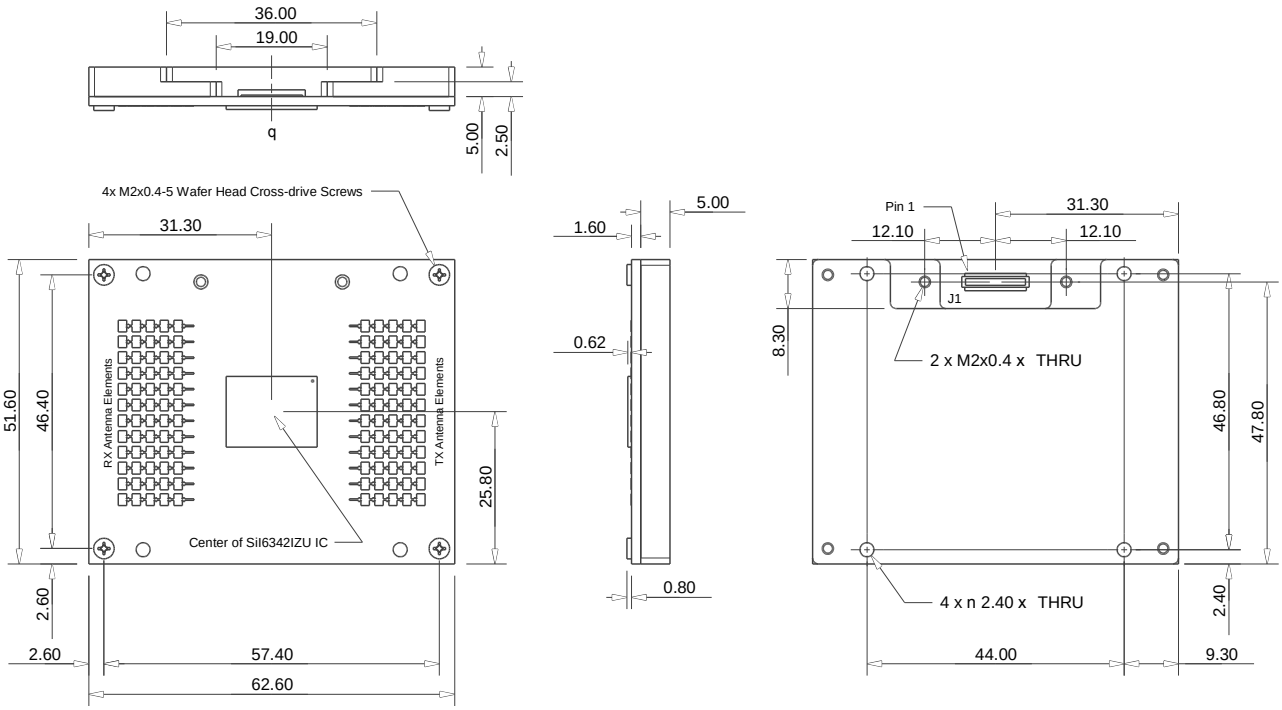

Figure 2.3. RF Board Mechanical Dimensions

2.4. Baseband and RF Board Interconnect

The baseband and RF boards each have connectors for FPC cable.

On the baseband board

- Connector type: Hirose DDF40C series
- Part number: DF40C-50DS-0.4V(51)
- Description: Dual row board-to-board socket, 0.4 mm pitch, 50 pins, 1.5 mm stacking height

On the RF board

- Connector type: Hirose DF40C series
- Part number: DF40C-50DP-0.4V(51)
- Description: Dual row board-to-board plug, 0.4 mm pitch, 50 pins, 1.5 mm stack height

The FPC cable has mating connectors on each end.

- Connector types: Hirose DF40C series
- Part numbers:DF40C-50DP-0.4V(51) on the baseband board end
  DF40C-50DS-0.4V(51) on the RF board end

For technical details of the connectors, refer to the information provided by the manufacturer at https://www.hirose.com/product/en/products/DF40/

2.5. Board Interconnect Cable

MOD65412 Wireless Link Module Set uses an FPC cable to connect high speed signals between the baseband board and the RF board.

This implementation of the FPC interconnect is 150 mm long, with board-to-board connectors at either end. The cable is folded to connect the baseband board inside the host system to the RF board mounted on an exterior surface of the host system. The FPC has two layers, with all signals routed on one layer and a ground plane on the second layer. The construction of the FPC cable is shown in Table 2.1 below. The geometry used with this implementation is 165 µm traces for single-ended 50 Ω signals and 100/100/100 µm trace/space/trace for 100 Ω differential signal pairs.

In designing a system specific FPC cable, care must be taken to match the trace lengths of the two signals in a differential pair as closely as possible. In addition to matching pair trace lengths, the lengths of the TXI/TXQ pairs must be matched, the lengths of the RXI/RXQ pairs must be matched, and the lengths of the HSD[0-3]/HSCS/HSCLK pairs must be matched. The cable included with the Starter Kit matches differential pair trace lengths and group trace lengths to <5 µm.

Table 2.1. FPC Interconnect Cable Cross Section

Circuit Layer	Thickness	Unit	Material	FPC Construction
—	12.5	µm	Polyamide	Top Coverlay
—	15	µm	Adhesive	
Top	34	µm	Copper	Double-sided FPC
—	20	µm	Adhesive	
—	50	µm	Polyamide	
—	20	µm	Adhesive	
Bottom	34	µm	Copper	
—	15	µm	Adhesive	Bottom Coverlay
—	12.5	µm	Polyamide	
Total thickness	213	µm	—	—

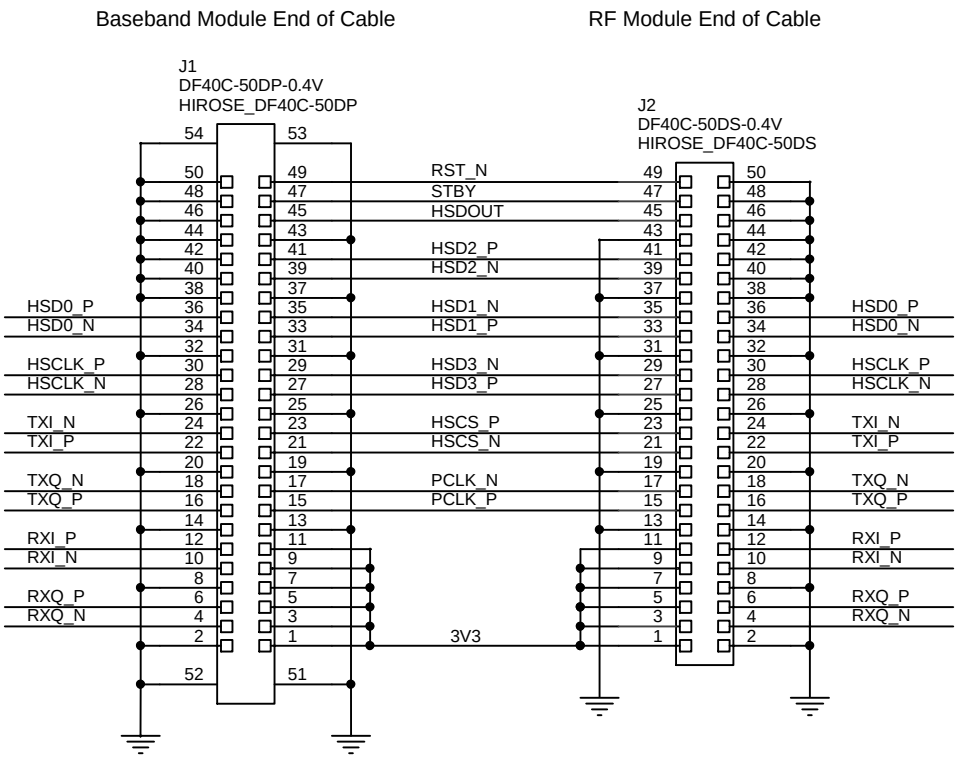

Figure 2.4. FPC Interconnect Cable Schematic

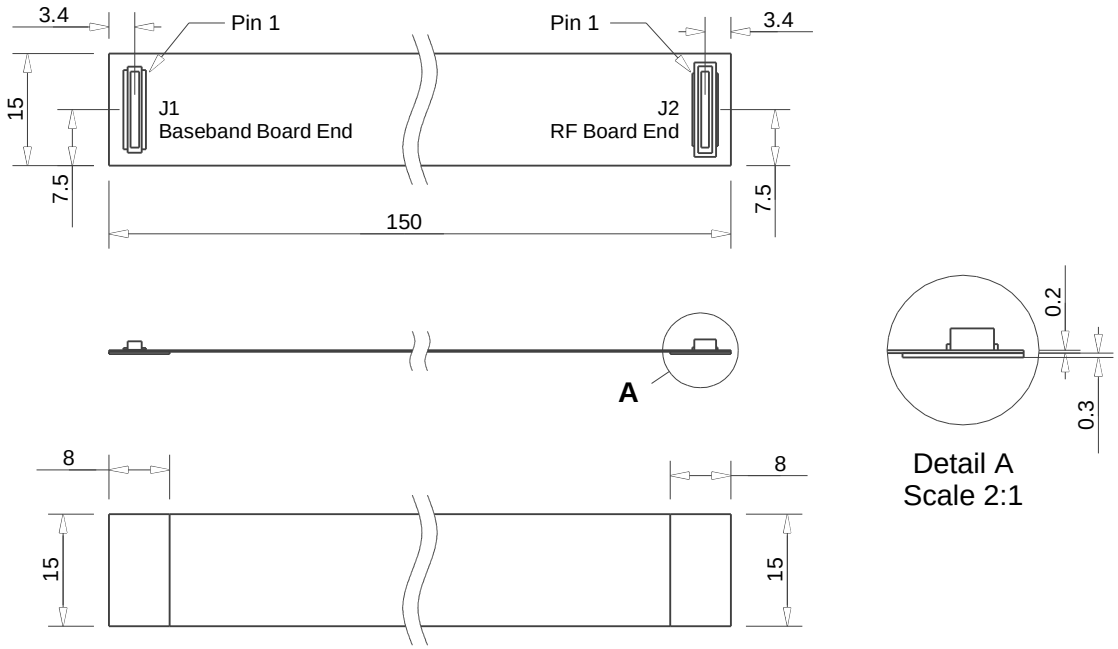

Figure 2.5. FPC Interconnect Cable Mechanical Dimensions

3. Electrical Interface

This section describes the Electrical Interface between the module set and the host system. The system connector is a 52-pin card edge connector that is compliant with the PCIe Mini Card specification. Refer to the *PCI Express® Mini Card Electromechanical Specification, Revision 2.0,* for complete details on the card form factor and interface signals.

3.1. Pin Out

Table 3.1. System Interface Pin Out

Name	Pin Number	Signal Type	Direction	Description	Function Group
PETn0[†]	31	—	I	PCI Express differential transmit pair	System data/control
PETp0[†]	33	—	I		
PERn0[†]	23	—	O	PCI Express differential receive pair	System data/control
PERp0[†]	25	—	O		
REFCLK-	11	—	I	PCI Express differential reference clock (100 MHz)	System data/control
REFCLK+	13	—	I		
CLKREQ#	7	LVCMOS	O	Reference clock request	System control
PERST#	22	LVCMOS	I	Functional reset to the module	System control
W_DISABLE1#	20	Open-Drain 3.3V tolerant	I	Radio operation disable signal	System control
LED_WLAN#	44	Open-Drain 3.3V tolerant	O	LED control signal to indicate radio enabled for transmitting	System control
3.3Vaux	2, 24, 39, 41, 52	3.3 V ± 5%, 1 A	—	3.3 V source	Module power
GND	4, 9, 15, 18, 21, 26, 27, 29, 34, 35, 37, 40, 43, 50	Electrical Ground	—	Ground	Module power
RSVD/NC	1, 3, 5, 6, 8, 10, 12, 14, 16, 17, 19, 28, 30, 32, 36, 38, 42, 44, 45, 46, 47, 48, 49, 51	N/C	—	Card edge pins not used by module	Reserved pins

[†] The PET and PER differential pairs are named from the system board point of view. The PETp0 and PETn0 pins are connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the SB6541 device on the baseband board. The PERp0 and PERn0 pins are connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the SB6541 device on the baseband board.

3.2. Description

3.2.1. 3.3 V

The PCI Express Mini Card edge connector supplies 3.3 V power to the module set. Due to the nature of the wireless power optimization implemented in this module set, the average power consumed by the module is much lower than the peak power, which is transient.

Parameter	Value
Power Input VIN	3.3 V DC, 1.1 A
Max Input Voltage Ripple	±9%
Max Power	Baseband: 1.0W, RF: 2.7W
Typical Power (at MCS6)	Baseband: 0.7W, RF: 1.5W
Idle Power	Baseband: 0.6W, RF: 0.9W

3.2.2. GND

These pins provide the common power and signal ground returns for the module.

3.2.3. PCI Express x1 Lane

The PETp0/PETn0 and PERp0/PERn0 differential pairs make up a ×1 PCI Express Lane that are the primary means of communicating with and controlling the module setMOD65412 Wireless Link Module Set. The signals are named with respect to the host platform. The PETp0/PETn0 signals are the input pair and are connected to the receiver pins on the SB6541 device on the baseband board. The PERp0/PERn0 signals are the output pair and are connected to the transmitter pins on the SB6541 device through DC-blocking capacitors.

3.2.4. Reference Clock

The REFCLK+/REFCLK- differential pair is an input to the baseband board. The reference clock is a 100 MHz clock used to assist the synchronization of the SB6541 device PCI Express interface timing circuits. The reference clock is required by the SB6541 device for proper operation.

3.2.5. CLKREQ#

The CLKREQ# signal is an active low output from the baseband board. It is used by the baseband board to request that the host platform supply a PCI Express reference clock. The baseband board ties this signal low through a 1 KΩ pull-down.

3.2.6. PERST#

The PERST# signal is an input to the baseband board. It is used by the host platform to indicate the system power source state and to force a hardware reset on the module. The host platform de-asserts (drives high) the signal when the system power sources are stable and within tolerance specifications. The host platform asserts (drives low) the signal when the system power is turned off or goes out of spec.

3.2.7. W_DISABLE1#

The W_DISABLE1# signal is an active low input to the baseband board. The host platform can use this signal to indicate to the baseband processor that the radio should be disabled.

3.2.8. LED_WWAN#

The LED_WWAN# signal is an active low output from the baseband board intended to drive an LED indicator on the host platform. It is used to indicate when the module has enabled the radio for transmission.

4. Grants and Labeling

The MOD65412 Module Set is subject to modular approval in regulatory regions. The United States of America (FCC) is the first region that the module is certified. In order to comply with radiation exposure limit set by the FCC, the system where the module is installed must operate at a distance of 30 cm away from any person. It is under such condition that the system integrator can use the MOD65412 modular grant.

The MOD65412 modular grant covers three components of the module: the baseband board, the RF board, and the FPC cable. The grant allows the system integrator to use different lengths of the FPC cable between 75 mm and 250 mm to meet specific system design requirements. The FPC cable reference design can be obtained through Lattice Semiconductor sales representatives.

The following grants have been issued for the MOD65412 module set:

Model: MOD65412:
FCC (USA): UK2-MOD65412

4.1. Module Label Examples

The labels attached to the model set provide identification and traceability in addition to displaying regulatory grants. Example labels are shown below. The exact layout may differ, but all important information should be displayed clearly.

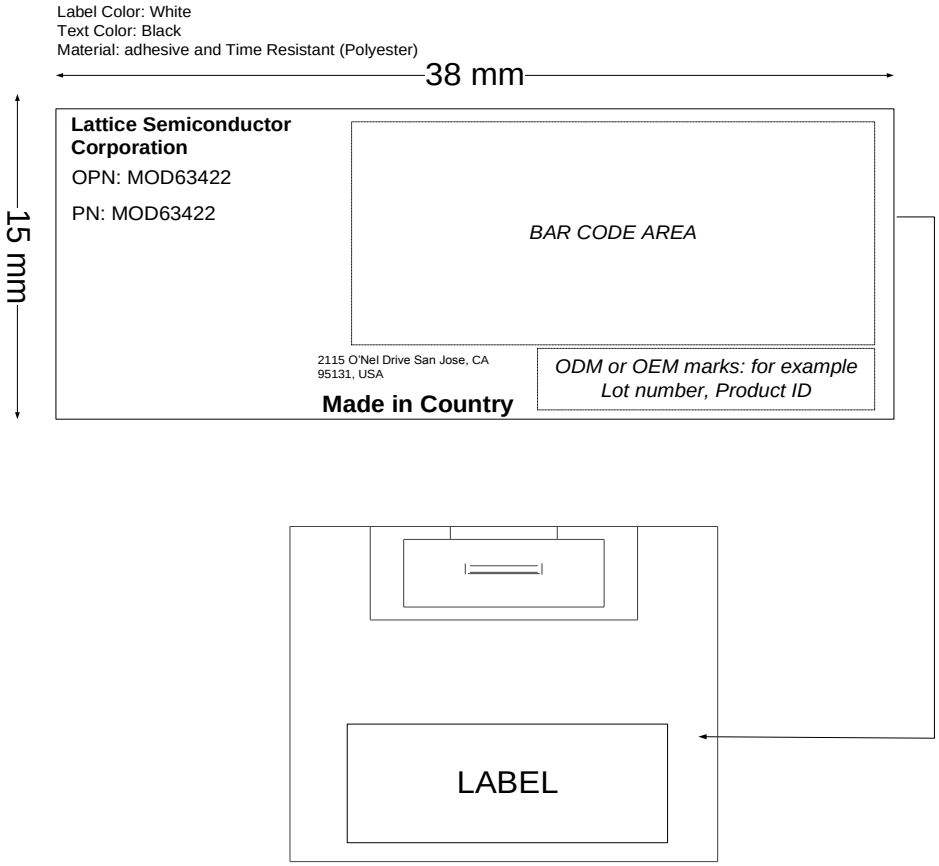

Figure 4.1. Example Label on MOD63422

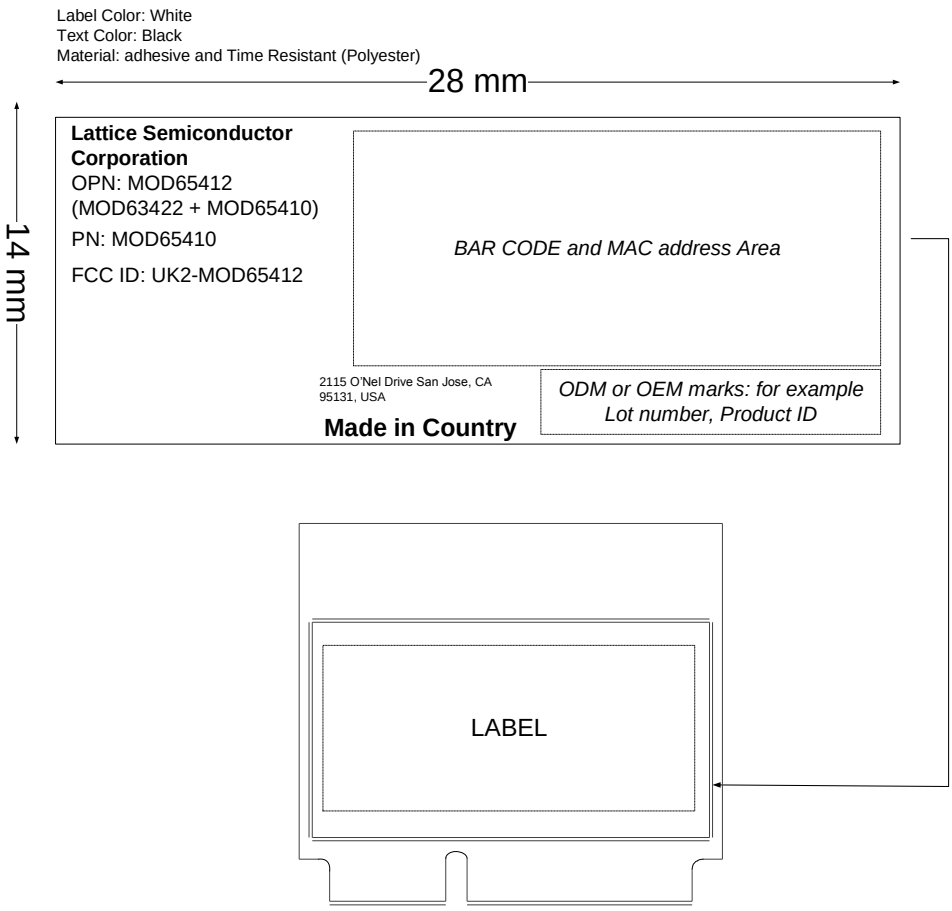

Figure 4.2. Example Label on MOD65410

Ordering Information

Device	Ordering Part Number
Lattice GigaRay Module Set	MOD65412

Appendix A. OEM Installation

A.1. Interference Statement

USA - Federal Communications Commission (FCC)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the instructions, it may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
2. This product does not contain any user serviceable components. Any unauthorized product changes or modifications will invalidate warranty and all applicable regulatory certifications and approvals.
3. Caution: Exposure to Radio Frequency Radiation: The installer of this radio equipment must place the module inside the enclosure of a stationary system intended to operate 30 cm away from the end user body in typical operation. This implies that this module shall not be integrated in battery operated devices, handheld devices, wearable accessories for example.
4. The antenna(s) used for this transceiver must not be collocated or operating in conjunction with any other antenna or transmitter within a host device, except in accordance with FCC multi-transmitter product procedures. Other antennas shall be installed with a minimum 30 cm separation from the 60 GHz device antenna present in this module.
5. Caution: User is cautioned that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
6. FCC rule 15.255(a) prohibits the use of this device on aircrafts or satellites.
7. This module is intended for the OEM integrator.

Additional note to System Integrator/OEM:

The regulatory label on the final system must include the exact statement:

“Contains FCC ID: UK2-MOD65412” on the enclosure

Revision History

Revision 0.80, February 2018

First preliminary release.

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