TYPE 340 PRECISION INCREMENTAL CRT DISPLAY

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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COPY NO. 55

INTRODUCTION

This manual is one of a series of documents needed for understanding, operating, and maintaining the Type 340 Precision Incremental CRT Display. The maintenance manual for the computer used is the primary supporting document, as it contains specific information on the operation of the computer, a generalized instruction list, a treatise on maintenance, an explanation of the operation of each type of module used in the computer, logical block diagrams and schematics of all the circuits in the computer, and an explanation of the logical symbology used in the drawings.

An important subsidiary document is the Digital System Modules Catalog, C-100. This publication contains operating descriptions and logical diagrams of many of the modules used in the computer and display, as well as explanations of the voltage and timing characteristics of standard signals, examples of various applications which aid in understanding the equipment, and an explanation of Digital logical symbology.

A series of MAINDEC program tapes and manuals are included in the supporting documentation. A MAINDEC program tape is a punched paper tape containing a series of maintenance programs that exercise various parts of the equipment. These exercises are designed to localize or specify the cause of any failure in various portions of the equipment. A MAINDEC manual contains a description of the associated program tests, operating instructions, flow diagrams, and a listing of the programs on the tape. These manuals are listed in Section 4, Maintenance.

The remainder of the supporting documentation consists of the maintenance manuals provided by other manufacturers for their items, such as special power supplies, which are used in the computer and display.

CONTENTS

Section		Page
1	DESCRIPTION	1-1
	Physical Description	1-3
2	PROGRAMMING	2-1
	340 Instruction Format	2-2
	Parameter Mode (000)	2-2
	Point Mode (001)	2-3
	Slave Mode (010)	2-4
	Character Mode (011)	2-5
	Vector Mode (100)	2-5
	Vector Continue Mode (101)	2-6
	Increment Mode (110)	2-6
	Subroutine Mode (111)	2-7
	PDP-1 Programming	2-9
	PDP-4 and PDP-7 Programming	2-11
	PDP-6 Programming	2-13
3	LOGICAL OPERATION	3-1
	Signal Flow	3-1
	Initial Starting	3-1
	Parameter Mode	3-2
	Point Mode	3-4
	Vector Mode	3-6
	Vector Continue Mode	3-7
	Increment Mode	3-8
	Character Mode	3-11
	Subroutine Mode	3-12
	Slave Mode	3-13
	Circuit Operation	3-13
	Initializing	3-14

CONTENTS (continued)

Section		Page
	Transferring	3-15
	Storing	3-18
	Deflecting	3-22
	Repeating	3-25
	Vector Generating	3-28
	Incrementing	3-31
	Character Byte Selecting	3-34
	Move Circuit	3-35
	AC Power Control and Distribution	3-36
	Special Module Circuit Description	3-36
	Type 1567 Display Preamplifier	3-36
	Type 1575 Follow or Hold Circuit	3-38
	Type 1579 Feed Forward	3-40
4	MAINTENANCE	4-1
	Preventive Maintenance	4-3
	Mechanical Checks	4-4
	Power Supply Checks	4-5
	Marginal Checks	4-7
	Corrective Maintenance	4-10
	Preliminary Investigation	4-11
	System Troubleshooting	4-11
	Circuit Troubleshooting	4-12
	Repair	4-16
	Validation Test	4-17
	Log Entry	4-18
	Assembly and Disassembly	4-18
	Logic Modules	4-18
	Power Supplies	4-18
	Deflection Output Amplifier	4-19

CONTENTS (continued)

Section		Page
	Cathode Ray Tube	4-19
	Coil Assembly	4-22
	Adjustments	4-24
	Centering Magnet Adjustment	4-24
	Coil Adjustment	4-25
	Focus	4-26
	Raster Position	4-26
	Raster Size	4-27
	Common Mode Current	4-28
	Brightness	4-29
	Straightness	4-29
	Deflection Speedup	4-33
	Delay Time	4-36
	Repeatability	4-37
	Spare Parts	4-38
5	INSTALLATION	5-1
	Site Requirements	5-1
	Physical Requirements	5-1
	Electrical Requirements	5-2
	Installing	5-4
6	ENGINEERING DRAWINGS	6-1
	Logic Signals	6-1

ILLUSTRATIONS

Figure		
1-1	Type 340 Layout and Dimensions	1-5
2-1	Parameter Mode Bit Format	2-2
2-2	Point Mode Bit Format	2-3

ILLUSTRATIONS (continued)

Figure		Page
2-3	Slave Mode Bit Format	2-4
2-4	Character Mode Bit Format	2-5
2-5	Vector and Vector Continue Modes Bit Format	2-6
2-6	Increment Mode Bit Format	2-7
2-7	Subroutine Mode Bit Format	2-7
2-8	Priority Interrupt System Bit Format	2-13
2-9	Display Interface Conditions Bit Format	2-14
3-1	Type 340 Signal Flow Diagram	3-3
3-2	Deflection Compensation Characteristics	3-25
4-1	Component Mounting Plate	4-20
4-2	CRT Assembly in Cabinet	4-21
4-3	Coil Assembly Components	4-23
4-4	Type 1567 Adjustment Locations	4-27
4-5	Type 1568 Adjustment Locations	4-32
4-6	Feed Forward Waveform Adjustments	4-34
4-7	Type 1579 Adjustment Locations	4-36
6-1	Digital Logic Symbols	6-2
6-2	Digital Cable and Component Numbering	6-5
6-3	Type 340 Block Diagram	6-7
6-4	Type 340 Timing and Pulse Control Logic, BS-E-340-0-31	6-9
6-5	Type 340 Input Register and Parameter Store Logic, BS-D-340-0-28	6-11
6-6	Binary Rate Multiplier and Increment Logic, BS-E-340-0-29	6-13
6-7	Horizontal and Vertical Deflection Registers, BS-E-340-0-30	6-15
6-8	Type 340 Deflection Logic, BS-D-340-0-27	6-17
6-9	Deflection Amplifier Heat Sink Wiring Diagram, WD-B-22106	6-19
6-10	Deflection Amplifier Resistor Stack Wiring Diagram, WD-C-22106	6-20
6-11	Deflection Amplifier Printed Circuit Layout, MA-B-22116	6-21
6-12	Deflection Output Amplifier Schematic, CS-B-22100	6-22
6-13	Display Preamplifier, CS-1567	6-23
6-14	Follow or Hold, CS-1575	6-23

ILLUSTRATIONS (continued)

Figure		Page
6-15	Feed Forward, CS-1579	6-24
6-16	Type 826 Power Control	6-24

TABLES

Table		
1-1	Type 340 Physical Specifications	1-4
1-2	Type 340 Operating Specifications	1-6
2-1	Typical PDP-1 IOT Display Instructions	2-10
2-2	PDP-4 and PDP-7 Display IOT's	2-12
2-3	Typical PDP-6 Programming Examples	2-17
3-1	Increment Mode Operation	3-9
3-2	Scale Level Relationships	3-21
3-3	Vector Generator Comparisons	3-31
4-1	Maintenance Equipment	4-1
4-2	Maintenance Controls and Indicators	4-2
4-3	Power Supply Outputs	4-6
4-4	10-Bit Digital-To-Analog Converter Adjustment	4-31
4-5	Spare Parts Provisioning	4-38
4-6	Other Modules Used in Display	4-39
5-1	Interface Signals at FJ	5-3
5-2	Interface Signals at H27	5-4

Type 340 Precision Incremental CRT Display

SECTION 1

DESCRIPTION

The Type 340 Precision Incremental CRT Display was specifically designed for use by the Programmed Data Processors -1, -4, -6, and -7 made by the Digital Equipment Corporation, but it may be used by any digital computer. The display receives a word of digital data from the computer, interprets the word as control or data information, automatically performs the required operations, and signals the computer when it is finished. Information can be displayed as either single random-position dots, straight lines, curved lines, or characters. Only logic levels are used in communicating between the display and the computer, making the operation of the display asynchronous with the computer. The digital word which contains the control and data information is 18 bits long. This word is loaded into a storage buffer register within 3 microseconds after the computer supplies a pulse or level with a fast (0.2 microsecond) rise time. The computer is then free for other operations, and may load another word into the display anytime after the display generates a level indicating it has completed its operation.

With the addition of the direct access channel option the Type 340 is uniquely suited to operate as a small computer. The direct access channel contains an indexable address register that provides direct access to the computer memory without disturbing the main computer operation. The computer loads the starting address of a block in memory into this register and initiates a display operation. Each time the display completes an operation, it breaks the computer program for one cycle while it fetches the word specified by this address register and loads it into the buffer register. The address register is then indexed by one, so it points to the next word in the block, much as a program counter does. The block in memory therefore acts as a subroutine program for the display. This series of operations terminates when a word with the stop bit set is received. The display then signals the computer that it has finished its operation.

Communication between the user and the computer can be increased by using the Type 370 Light Pen option. The light pen is a fast-response photosensitive device that produces a pulse and sets a flag when it sees any single spot displayed during the 0.5-microsecond intensification time. By this means the computer can be signaled to perform some preprogrammed function at a specific time and/or location.

The Type 340 is capable of eight modes of operation. Each word contains information that specifies the mode of operation for the next succeeding word and operation. These modes are:

(1) PARAMETER MODE — When the display has been set to the parameter mode, it interprets the next word as containing information that may change its present mode, scale, intensity, light pen control, and interruption control parameters.

(2) POINT MODE — When the display has been set to the point mode, it interprets the next word as containing a coordinate location and information that may change its present mode, light pen, and intensify control parameters.

(3) VECTOR MODE — When the display has been set to the vector mode, it interprets the next word as containing the vector size and direction information, as well as intensify control and escape information. The display remains in the vector mode until the escape bit is set, at which time it reverts to the parameter mode. If the edge of the raster is violated, a flag is set and the display returns to the parameter mode.

(4) VECTOR CONTINUE MODE — When the display has been set to the vector continue mode, it interprets each succeeding word as containing direction information of a vector from the starting point to the edge of the raster, as well as intensify control and escape information. In this respect it is similar to the vector mode. When the vector violates the edge of the raster, the display returns to the parameter mode.

(5) INCREMENT MODE — When the display has been set to the increment mode, it interprets each succeeding word as containing information to move the spot to four successive locations, each adjacent to the preceding spot. The spot can be placed into any one of the eight adjacent locations at each movement. The word also contains intensify control and escape information. The display remains in the increment mode until the escape bit is set, at which time it returns to the parameter mode.

(6) CHARACTER MODE — The display only operates in the character mode when it is equipped with the Type 342 Character Generator option. In this mode, the display interprets each succeeding word as containing three alphanumeric characters or other symbols, each specified by six bits. The display remains in the character mode until a special code is encountered, at which time it reverts to the parameter mode.

(7) SUBROUTINE MODE — The display only operates in the subroutine mode when it is equipped with the Type 347 Subroutine Interface option. When set to this mode, the display interprets the next word as a jump instruction to some different location in memory. The subroutine word also sets the mode for the next word to be transferred. Three different jump instructions are decoded and implemented by the Type 347.

(8) SLAVE MODE — The display only operates in the slave mode when it is equipped with the Type 343 Monitor option. When set to the slave mode, the display interprets the next word as a control word for up to four individual slave monitor displays in one of four different slave groups. This word turns on or off the intensity circuits and light pens of the particular slave on command. Up to 16 slaves can be used to monitor all or any part of the presentation of the main display. The slave word also sets the mode for the next word to be transferred.

PHYSICAL DESCRIPTION

The 340 is housed in two vertical equipment bays, as shown in the frontispiece. The bays are connected together and supported by eight castered rollers. The display can be easily moved about within the area dictated by the 50 foot cables to the computer and ac power receptacle.

The cathode ray tube, its deflection circuits, and special power supplies are mounted in the left-hand bay. The CRT is located in the center of the bay and is inclined 30° to provide the best working angle. A small table top projects out beneath the CRT mounting panel for the convenience of the user.

All the logical circuits which control the display are located in the right-hand bay, along with their indicators and power supplies. The indicators are located at the top of the bay, above the double doors in front. The logical circuits are located in racks behind these doors. The power supplies are mounted on a plenum door in the rear of the bay, behind a pair of swinging doors. Figure 1-1 shows the physical shape and equipment layout of the display.

The system modules which make up the logical control circuits plug into sockets mounted on a rack. Each rack is identified by a letter indicating the location of the rack in the display. These letters are combined with the socket number to specify a particular module. For example, E09 specifies the ninth module from the left (when looking at the front, or wiring side, of the rack) in rack E (fifth from the top) of bay 1.

Each rack socket and module plug contain 22 terminals, identified by the letters of the alphabet (G, I, O, and Q are not used), starting at the top. All terminals are therefore identified by adding the terminal letter as a suffix to the module location code. An example is E09Z, the last terminal of the previous module location example.

Cable receptacles and the corresponding plugs are designated with the same system of bay number and rack designation, with the numbers 26 through 29 added as a suffix. If the number is 26 or 27, the socket is located on the right side of the rack at the rear, while the numbers 28 or 29 are for the corresponding location on the left side. Terminal boards and standoff terminals are also numbered in a similar fashion, as shown in Figure 6-1.

TABLE 1-1 TYPE 340 PHYSICAL SPECIFICATIONS

Dimensions	42 inches wide, 51 inches deep (with table), 69-1/8 inches high, 27-1/2 inches table top height.
Weight	Approximately 700 pounds, supported on eight castered rollers and two screw pads.
Housing	Two vertical DEC cabinets, one with an extension on the front. Paint is blue, with off-white table and charcoal brown accent panel. Anodized brushed aluminum trim.

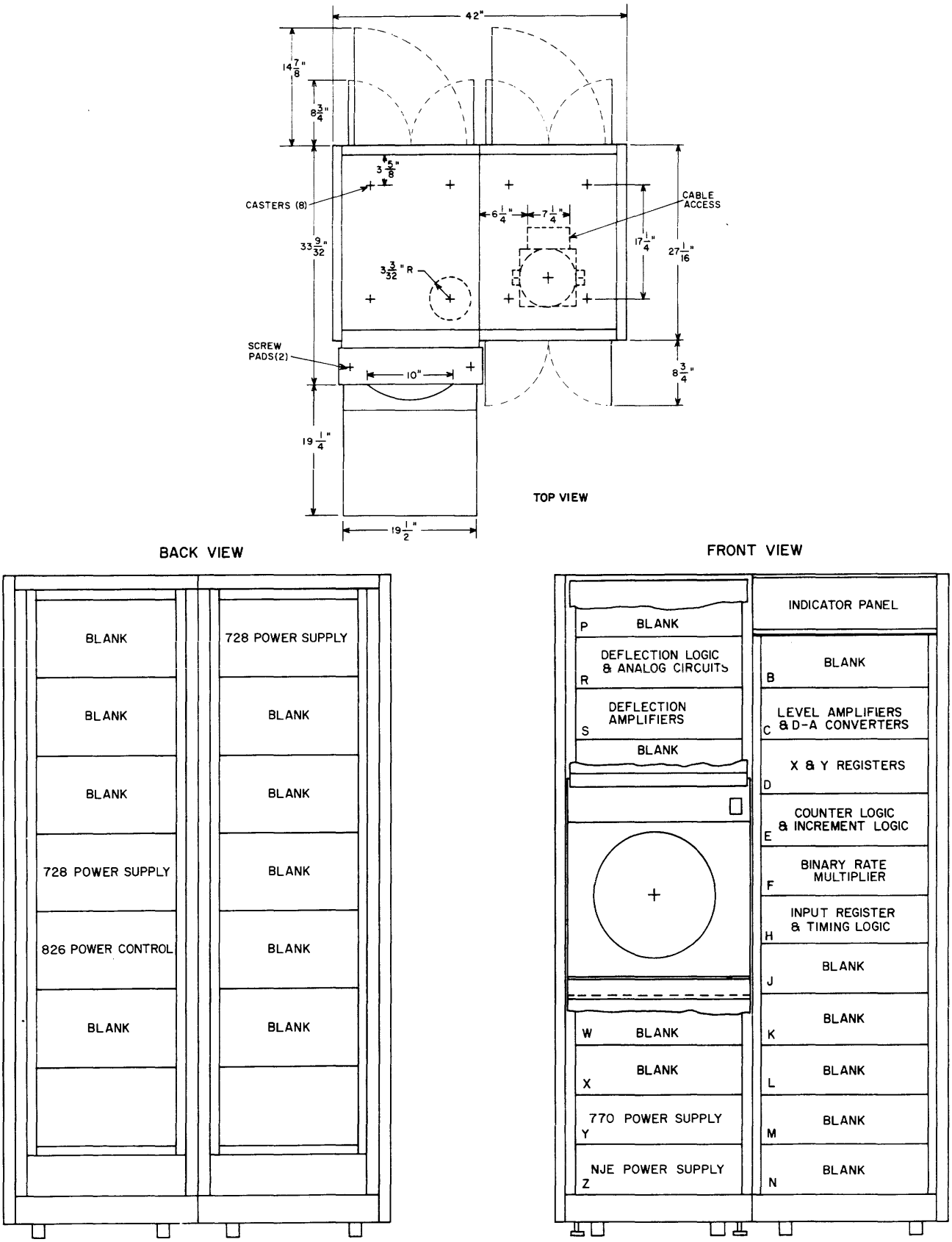


Figure 1-1 Type 340 Layout and Dimensions

TABLE 1-1 TYPE 340 PHYSICAL SPECIFICATIONS (continued)

Clearance	Three feet of access room is required at the rear for maintenance. Two feet is recommended on the left side.
Controls	The light pen gain control located at the lower left of the front panel is the only operating control.
Display Tube	Fixed mount in center of left bay. The tube is tilted 30°. A 1/8-inch sheet of form-fitted plexiglass protects the face of the tube.

TABLE 1-2 TYPE 340 OPERATING SPECIFICATIONS

Input Power	115 ±10 volts, 60 cycle single phase, at 13 amps (20 amps surge). 50 cycle and/or 220- to 250-volt power supplies available.
Power and Heat Dissipation	1.5 kilowatts, 4950 Btu/hour.
Ambient Temperature	50°F (10°C) to 110°F (43°C).
Cathode Ray Tube	16ADP7A. Radius of curvature 40 inches.
Raster Size	9-3/8 inches by 9-3/8 inches, containing 1,024 points by 1,024 points.
Pincushion Distortion	Less than 3/32 inch per side.
Deflection and Focus	Magnetic.
Spot Size	Approximately 0.030 inch, 0.015 inch at the half-light output points.
Address Scheme	2's complement, with (0,0) located at the lower left-hand corner of the raster.
Stability	±0.05 inch in 8 hours at a nearly constant temperature (±3°F).
Repeatability	±0.05 inch regardless of the location of the previous spot.

TABLE 1-2 TYPE 340 OPERATING SPECIFICATIONS (continued)

Timing	3 microseconds for information transfer, 35 microseconds per point for random positioning, 1.5 microseconds per point in the vector, vector continue, increment, and character modes.
Modes	Parameter, point, vector, vector continue, increment, and character.
Intensification	Preset at 0.5 microseconds per point.
Indicators	The current state of the coordinate registers and all control flip-flops is shown by indicator lights at the top of the right-hand bay.

SECTION 2

PROGRAMMING

The Type 340 is controlled completely by the computer to which it is attached. The programming of this computer and display combination varies for almost all installations because of the differences in the computers and the different options used with the display. This section discusses some of the general aspects of writing programs for the display and lists many of the instructions used by the PDP-1, PDP-4, PDP-7, and the PDP-6.

Of primary importance, when writing a display program, is the manner in which the 18-bit word is transferred to the display. In most cases, this word contains information which is the result of some previous operation and therefore is stored in the memory of the computer. In the simplest type of installation, this word must be retrieved from memory and placed into the computer output register by one instruction and then transferred to the display by another instruction. The display then operates on this word and signals the computer when it has finished, at which time the computer must repeat the transfer process. This causes frequent and time-consuming interruptions of the main program of the computer.

This disadvantage can be relieved with the use of the direct access channel, an option with the PDP-1 and standard with the PDP-4 and PDP-7. The required information words are loaded into a table, or block of successive memory locations, and the beginning location of this table is loaded into a special register called the display address counter (DAC). The output of the DAC is applied directly to the inputs of the memory address (MA) register. A data break is then initiated by either the display or the computer, and this address is read into the MA. The computer then goes through a break cycle in which it fetches the word from memory and places it into its memory buffer (MB) register from where it is transferred directly to the buffer register (BR) in the display. During this time, the display starts its operation and the DAC is incremented by one. The computer program counter (PC) is not incremented during the break cycle. At the end of the break cycle the computer continues its main program until the display requires another data break.

340 INSTRUCTION FORMAT

The 18-bit word which is transferred to the 340 is interpreted differently in each mode of operation. Each mode requires that the information in the word follow a definite format. These formats are described in the following section.

Parameter Mode (000)

The parameter mode is specified by 0_8 in the mode register. This occurs when bits 2, 3, and 4 of the previous word were zero, or the escape bit was set, or an edge was violated. It also occurs when the computer issues an instruction which produces the DPY GO pulse. When in this mode, the display interprets the word in its buffer register (BR) according to the bit map in Figure 2-1.

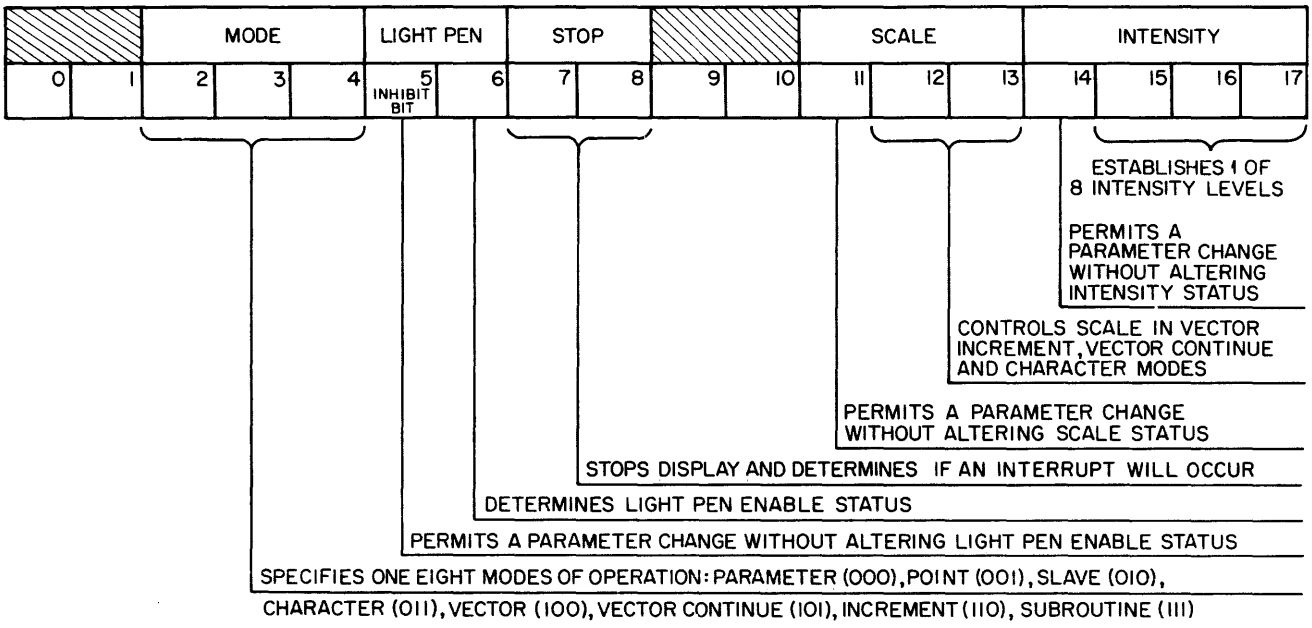


Figure 2-1 Parameter Mode Bit Format

Bits 0 and 1 are not used. Bits 2, 3, and 4 set the mode register for the next word to be transferred. Bit 5 permits the light pen enable circuit to be set or cleared (according to bit 6) when it is a 1, and prevents the circuit from being changed when it is a 0. Bit 6 sets the LP enable flip-flop when it is a 1, and clears it when it is a 0, provided bit 5 is a 1. Bit 7 stops the display operation when it is a 1, and bit 8 generates a STOP INTERRUPT signal when it is a 1 if

bit 7 is also a 1. Bits 9 and 10 are not used. Bit 11 allows the scale register to be set and/or cleared when it is a 1, and prevents changing the register when it is a 0. Bits 12 and 13 determine the number of positions each succeeding spot is moved in the vector, vector continue, increment, and character modes. These are 1, 2, 4, or 8 positions for 00, 01, 10, or 11, respectively. Bit 14 allows the intensity register to be set and/or cleared when it is a 1, and prevents the register from being changed when it is a 0. Bits 15, 16, and 17 are loaded into the intensity register when bit 14 is a 1. These bits determine the intensity level according to their octal value, with 0_8 the dimmest and 7_8 the brightest.

Point Mode (001)

The point mode is specified by 1_8 in the mode register. When in this mode, the display interprets the word in its BR according to the bit map in Figure 2-2.

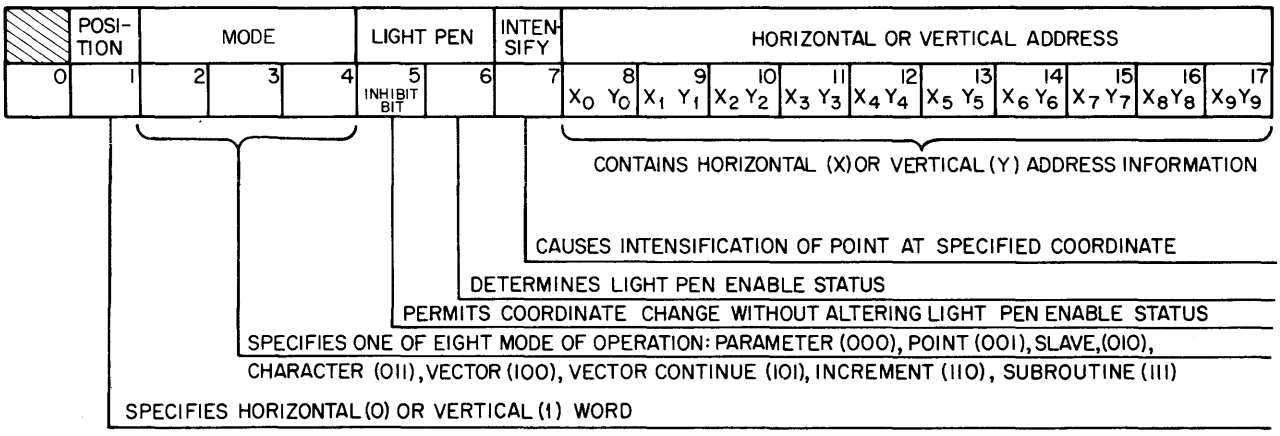


Figure 2-2 Point Mode Bit Format

Bit 0 is not used. Bit 1 determines the axis of the coordinate address; horizontal coordinate words are 0 and vertical coordinate words are 1. Bits 2, 3, and 4 set the mode register for the next word to be transferred. Bit 5 permits the LP enable flip-flop to be set or cleared according to bit 6. The LP enable flip-flop is set when bit 6 is a 1, and cleared when bit 6 is a 0, provided bit 5 is a 1. Bit 7 is the intensify bit, causing a spot of light to appear at the specified coordinates when it is a 1, and preventing the spot from occurring when it is a 0. Bits 8 through 17 consititute the coordinate byte. This is a 10-bit positive binary word, with zero specifying the left-hand or bottom coordinate.

Slave Mode (010)

The display can only use the slave mode when it is equipped with the Type 343 Monitor option. The slave mode is specified by 2_8 in the mode register. When in this mode, the display interprets the 18-bit word in its BR according to the bit map in Figure 2-3.

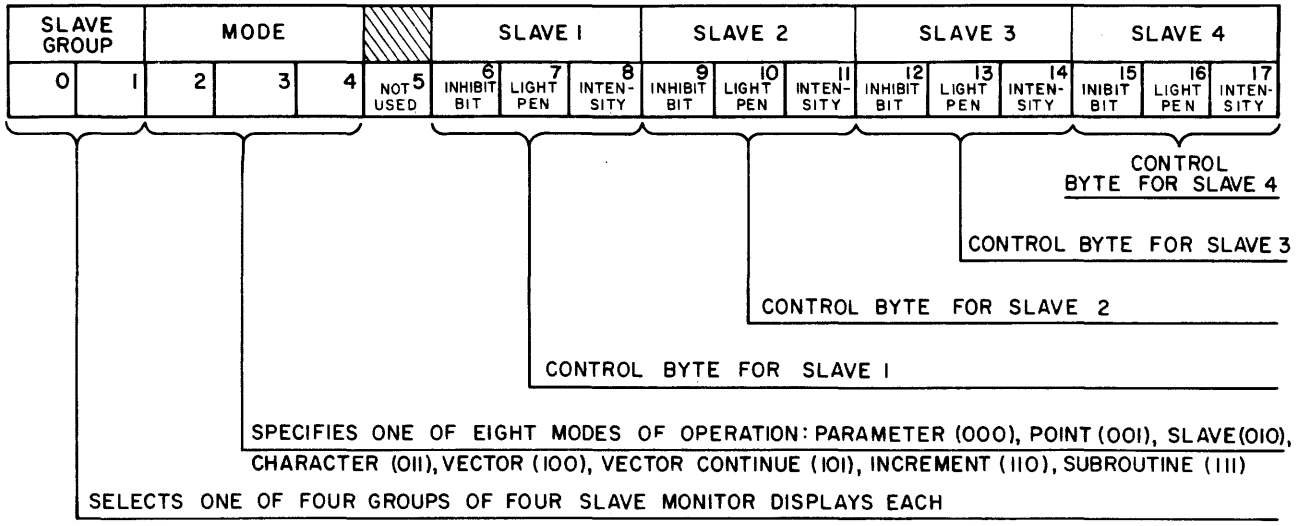


Figure 2-3 Slave Mode Bit Format

Bits 0 and 1 select one of four groups of up to four slave monitor displays according to the binary value of these bits. If the display only has one group, these bits are not used. Bits 2, 3, and 4 set the mode register for the next word to be transferred. Bit 5 is not used. Bits 6 through 17 are divided into four identical 3-bit bytes, one for each of the four slave monitor displays in the group.

The most-significant bit in each byte (bits 6, 9, 12 and 15) permits the light pen and intensify control circuits to be enabled or disabled according to the other two bits when it is a 1, and prevents these circuits from being changed when it is a 0. The middle bit in each byte (bits 7, 10, 13, and 16) controls the light pen circuit when the most-significant bit is a 1. This circuit is enabled (allowing the light pen in the particular slave monitor display to generate a program interrupt signal) when the bit is a 1, and is disabled when the bit is a 0. The least-significant bit of each byte (bits 8, 11, 14, and 17) controls the intensify circuit when the most-significant bit is a 1. This circuit is enabled (allowing the picture on the Type 340 to be repeated on the particular slave monitor display) when the bit is a 1, and is disabled when the bit is a 0.

Character Mode (011)

To use the character mode, the display must be equipped with the Type 342 Character Generator. The character mode is specified by 3_8 in the mode register. In this mode the display interprets all succeeding words as character words and transfers them to the Type 342. The display can only escape from the character mode when the Type 342 decodes an escape character and produces an escape pulse (or the computer issues an IOT that produces the DPY GO pulse). In either case, the mode register will be cleared, returning the display to the parameter mode.

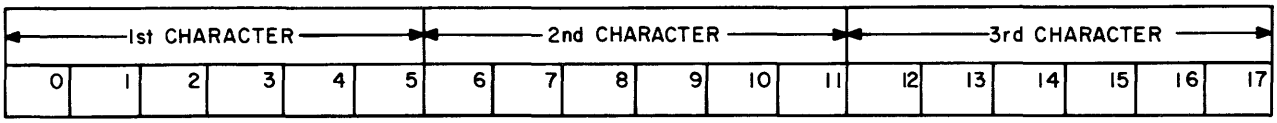


Figure 2-4 Character Mode Bit Format

The display transfers a 6-bit byte to the character generator, which then produces a series of pulses that causes the display to plot the character point-by-point. After the character generator finishes its operation, it signals the display, which then either transfers the next byte to the character generator or generates a request for more data from the computer.

Vector Mode (100)

The vector mode is specified by 4_8 in the mode register. When in this mode, the display interprets the word in its BR according to the bit map in Figure 2-5. The display remains in the vector mode until a word is transferred to it with the escape bit set or it moves a spot past the edge of the raster. Violating an edge sets the edge flag flip-flop and generates an interrupt signal that causes the computer to break its main program.

Bit 0 is the escape bit. When it is a 1, the display clears its mode register, returning to the parameter mode. Bit 1 is the intensify bit. When it is a 1, all successive points of the vector are intensified. Bits 2 through 17 consist of two 8-bit bytes. Each byte specifies the size of the vector component along one of the coordinate axis, and the direction from the starting point. Bits 2 through 9 comprise the Y component byte and bits 10 through 17 comprise the X component byte. The most-significant bit of each byte is the sign bit, with 0 signifying a positive (up or right) direction and 1 signifying a negative (down or left) direction.

The remaining 7 bits of each byte specify the number of increments the vector will be moved along the respective axis. Since this is a binary number, a maximum of 128 increments is possible. The display calculates whether or not to move the spot at each incrementing time (every 1.5 microseconds), using both bytes simultaneously. The resultant vector is straight only on vertical, horizontal, or 45° lines; however, at other angles the dot is never more than one incremental unit from a straight line. If the smallest (X1) scale is used, the incremental unit is about 2/3 the spot diameter, so the line looks straight.

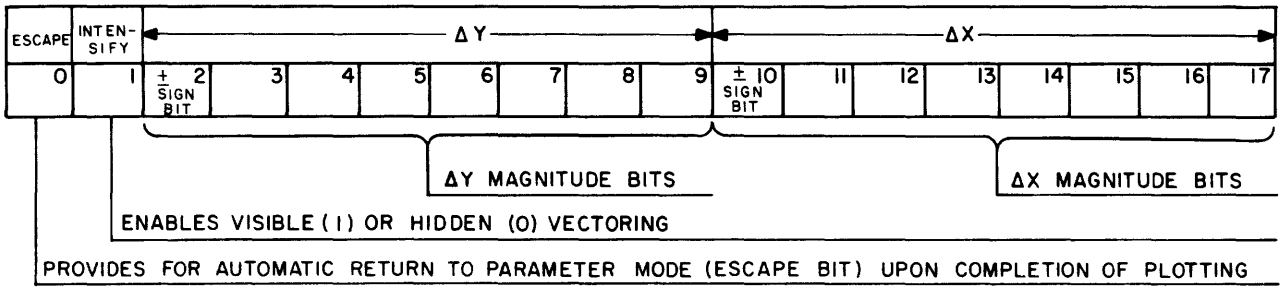


Figure 2-5 Vector and Vector Continue Modes Bit Format

Vector Continue Mode (101)

The vector continue mode is specified by 5_8 in the mode register. This mode is essentially the same as the vector mode and uses the same word format, shown in Figure 2-5. The only difference is that, when the vector has been drawn to the end point specified by the two component bytes, the display does not halt but continues drawing the vector at the same angle until it reaches the edge of the raster. The display then stops, requests a new word from the computer, and automatically escapes into the parameter mode. At this time the beam is located on the opposite side of the raster from where it violated the edge.

Increment Mode (110)

The increment mode is specified by 6_8 in the mode register. When in this mode, the display interprets the word in the BR according to the bit map in Figure 2-6. Once the display is placed in the increment mode, it can only return to the parameter mode when it either receives a word with the escape bit set, increments beyond the edge of the raster, or receives from the computer an IOT which produces the DPY GO pulse.

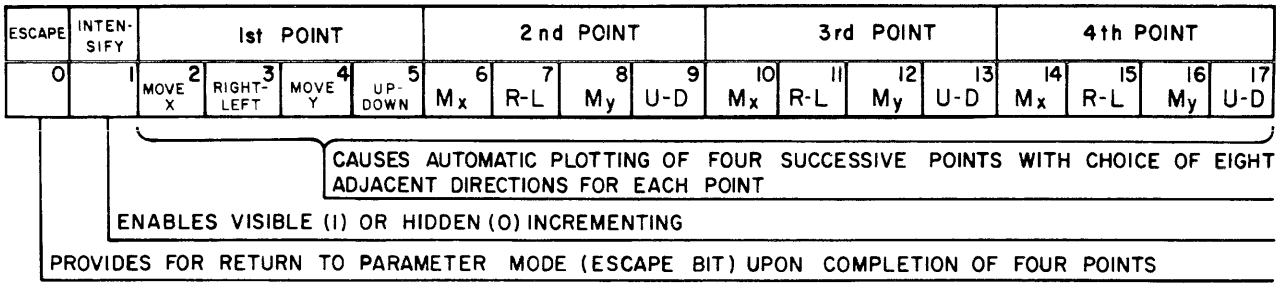


Figure 2-6 Increment Mode Bit Format

Bit 0 is the escape bit. When it is a 1, the display clears the mode register, escaping to the parameter mode. Bit 1 is the intensify bit. When it is a 1, each incremental point is displayed, while the spot is moved but not displayed if it is a 0. Bits 2 through 17 consist of four 4-bit bytes, each of which specifies if and when the spot is to be moved from its previous location. The bytes are operated on separately, requiring 1.5 microseconds each. The complete word is processed in approximately 9 microseconds from the starting pulse to the next request for data signal.

Subroutine Mode (111)

The display can only use the subroutine mode if it is equipped with a Type 347 Subroutine Interface option. The subroutine mode is specified by 7_8 in the mode register. When in this mode, the display interprets the word in its BR according to the bit map in Figure 2-7.

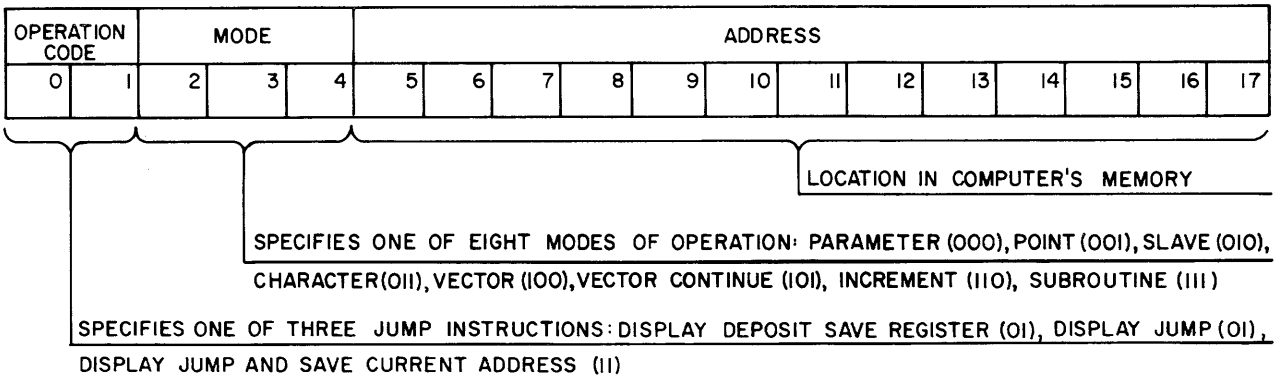


Figure 2-7 Subroutine Mode Bit Format

Bits 0 and 1 constitute the instruction part of the word. Bits 2, 3, and 4 set the mode register for the next word to be transferred. Bits 5 through 17 contain a 13-bit address, specifying a location in the computer memory.

The instruction bits are decoded to select one of three jump instructions; the fourth combination (00) is not used. These instructions are:

1. DDS - Display Deposit Save Register. This instruction is specified by 01 in the instruction bits. It causes a word to be deposited in memory at the location specified by the 13-bit address byte and sets the mode register for the next word in the table. The DDS instruction is the return jump instruction for multilevel subroutines and is placed at the top of the subroutine table (the DJS instruction which calls this multilevel subroutine must specify the subroutine mode). The word which is transferred contains a jump instruction to the location following the DJS instruction which called the multilevel subroutine and returns the display to the parameter mode.

2. DJP - Display Jump. This instruction is specified by 10 in the instruction bits. It causes the address contained in the address byte to be loaded into the display address counter (DAC) and sets the mode register for the next word (first word in the subroutine). The previous address held by the DAC is lost. The DJP instruction is a non-return jump to a subroutine.

3. DJS - Display Jump and Save. This instruction is specified by 11 in the instruction bits. It causes the address contained in the address byte to be loaded into the DAC, increments and transfers the address which was in the DAC to the address save register (ASR), and sets the mode register for the next word (first word in the subroutine). In single-level subroutines, when the display escapes from the vector, vector continue, or increment modes, the address saved in the ASR is automatically transferred to the DAC, returning the program back to the location following the jump. In multilevel subroutine calls the return address saved in the ASR must be transferred to memory before any other jumps are made. This is accomplished with the DDS instruction

which precedes the other instructions in the subroutine and requires that the DJS instruction specify the subroutine mode.

PDP-1 PROGRAMMING

Most PDP-1/340 combinations utilize the Type 19 High Speed Channel Control and the direct access channel configuration. The IOT display load address counter (DLA, 720015) loads the display address counter (DAC) from the I/O register by a 1's transfer. DLA first clears the DAC and mode register and sets the request for data (RFD) flip-flop in the display; then it loads the DAC with the address from the I/O. During the break cycle initiated by the RFD, the address in the DAC is read into the MA, the selected word in memory is transferred to the memory buffer (MB), the DAC is incremented but the program counter (PC) is not, and the display reads the word from the MB into its buffer register (BR). Since the display is in the parameter mode (because the mode register was cleared), it sets various control flip-flops as specified by the information in the word and also sets the RFD flip-flop to generate another break cycle if the stop bit is not set. This operation occurs before the computer has finished its break cycle; so unless the stop bit has been set, the next computer cycle is another break cycle.

During this second cycle the computer transfers the second word from the table to the display, which interprets it in one of the operating modes determined by the mode bits of the preceding parameter word. This word is generally a point mode word containing the Y, or vertical, coordinate address. The word is loaded into the BR in the usual manner. The coordinate address is then transferred into the Y register, and finally the RFD flip-flop is set to request another word. (This occurs before the PDP-1 finishes its break cycle.) A third break cycle then occurs, in which the computer transfers another point mode word containing the X, or horizontal, coordinate address. When this coordinate is loaded into the X register, it initiates a 35-microsecond delay. During this time, the computer is freed to continue its main program. At the end of the 35 microseconds, a spot of light appears if the intensify bit has been set, and the RFD flip-flop is set to request another break cycle.

The next word will probably be an increment, vector, vector continue, or character mode word, depending on the mode bits of the last point mode word. If this is the case, the display performs the required operation and requests another break cycle when it is done, but does not

clear the mode register (unless the escape bit is set or an edge is violated). Each succeeding word is interpreted as being in the same mode. When the display is in the increment, vector, or vector continue modes and receives a word with the escape bit set, it clears the mode register when it requests another break cycle; so the next word is interpreted in the parameter mode. If the display is in the character mode, the character generator produces an escape pulse (when it encounters an escape character) which also clears the mode register. During the display operations, which can last as long as 1.5 milliseconds, the computer is free to continue with its main program.

The last word in a series of display operations must be a parameter word in order to stop the display. When the stop bit is set in this word, the stop flip-flop is set. The interrupt bit of this word must also be set to generate an interrupt signal, as no RFD is generated.

If the Type 370 Light Pen is being used and sees a spot of light, it stops the X and Y registers from being loaded or the other modes from continuing, preventing the RFD flip-flop from being set. The display halts its operations and produces a light pen flag signal for the computer, causing a program interrupt. The computer jumps to a subroutine to service the interrupt and then issues the IOT display resume sequence (DRS, 720115), which clears the light pen flip-flops and allows the display to finish the interrupted operation.

The IOT instructions which control the operation of the PDP-1/340 system are listed in Table 2-1. (The octal values of these instructions may be different for some computers.) These instructions can be microprogrammed (combined) by adding the center two octal digits of two or more listed instructions to make a new instruction. The last two digits of each instruction used in microprogramming must always be the same (as must the first two). Example: DSE (display skip on edge violation, 721417) is the combination of DSV and DSH.

TABLE 2-1 TYPICAL PDP-1 IOT DISPLAY INSTRUCTIONS

Mnemonic	Octal Value	Name/Explanation
DLA	720015 ~~720005~~ 720025	Display Load Address Counter /C(IO) ⇒ C(DAC), DPY GO starts the display operation.

TABLE 2-1 TYPICAL PDP-1 IOT DISPLAY INSTRUCTIONS (continued)

Mnemonic	Octal Value	Name/Explanation
DRS	720115 720125	Display Resume Sequence /Clears light pen flag and restarts the interrupted display operation.
DCF	720215 720225	Display Clear Flags /Clears the light pen, edge violation, and request for data flags.
DRA	720016 720026	Display Read Address Counter /C(DAC) ⇒ C(IO).
DRC	720116 720126	Display Read Coordinates /$C(X_{0-8}) \Rightarrow C(IO_{0-8})$, $C(Y_{0-8}) \Rightarrow C(IO_{9-17})$.
DSP	720117 720127	Display Skip on Light Pen Flag /C(PC) + 1 ⇒ C(PC) if LP FLAG occurs.
DSS	720217 720227	Display Skip on Stop Interrupt /C(PC) + 1 ⇒ C(PC) if stop interrupt occurs.
DSV	720417 720427	Display Skip on Vertical Edge Violation /C(PC) + 1 ⇒ C(PC) if spot moves past top edge. Interrupt will occur except in vector continue mode.
DSH	721017 721027	Display Skip on Horizontal Edge Violation /C(PC) + 1 ⇒ C(PC) if spot moves past right edge. Interrupt will occur except in vector continue mode.

PDP-4 AND PDP-7 PROGRAMMING

Both the PDP-4 and the PDP-7 computers use the same symbolic and machine language, and perform the same functions. The primary difference between the two computers is their memory cycle time: the PDP-4 requires 8 microseconds, while the PDP-7 requires only 1.75 microseconds (this can be slowed to 3.75 microseconds for slow-speed information transfer). Most installations use the 4,096 or 8.192 word core memories, requiring a 13-bit display address counter (DAC) in the direct access channel option. However, any extended memory system requires a 15-bit DAC.

If the Type 340 is the only peripheral device requiring direct access to the memory of the computer, the real time control provides the necessary access when using a DAC. However, if additional options also require direct memory access, a Type 133 Data Interrupt Multiplexer is required. Both the real time control and the data interrupt multiplexer allow the display to have access to memory via a break cycle in the same fashion as that described for the PDP-1. In the case of the PDP-7, the data break occurs at the slow (3.75 microsecond) memory cycle speed.

The mnemonics of the symbolic language are mainly the same as for the PDP-1. However, the octal values of the machine language are different. These are listed in Table 2-2. As with the PDP-1, microprogramming is possible by combining two or more IOT's that differ only in the least-significant octal bit.

TABLE 2-2 PDP-4 AND PDP-7 DISPLAY IOT'S

Mnemonic	Octal Value	Name/Explanation
DSE	700501	Display Skip on Edge Violation /C(PC) + 1 ⇒ C(PC) when an edge flag occurs.
DRA	700502	Display Read Address Counter /C(DAC) ⇒ C(AC).
DRS	700504	Display Resume Sequence /Clears light pen flag and restarts the interrupted display operation.
DSI	700601	Display Skip on Stop Interrupt /C(PC) + 1 ⇒ C(PC) if a stop interrupt occurs.
DCA	700602	Display Clear Address Counter /0 ⇒ C(DAC).
DLA	700604	Display Load Address Counter /C(AC) ⇒ C(DAC), DPY GO starts the display operation.
DSP	700701	Display Skip on Light Pen Flag /C(PC) + 1 ⇒ C(PC) if a light pen flag has occurred.
DRC	700702	Display Read Coordinates /$C(X_{0-8}) \Rightarrow C(AC_{0-8})$, $C(Y_{0-8}) \Rightarrow C(AC_{9-17})$.
DCF	700704	Display Clear Flags/Clear light pen, edge violation, and request for data flags.

All 340 Displays operated by a PDP-6 require a 344 Interface. This interface stores the 36-bit data word from the PDP-6 and applies it as two 18-bit words to the 340 when requested. (The left half of the word is always used before the right half.) The 344 also contains the logic circuits which produce the required control signals, interrupt and flag signals, and coordinate register status signals.

Normally the PDP-6 operates the 340 in the priority interrupt mode, although this is not necessary when no other time demands are made on the computer. Two different priority interrupt channels are used by the 340 because of the two types of conditions under which the display stops operating. One channel is used to request a new data word when the display transfers the second half of the word in the interface buffer (IB) into its buffer register (BR) and commences its second operating cycle. The other channel generates an interrupt signal when any of the special display stop conditions occur; i.e., the light pen has seen a spot, an edge has been violated (except in the vector continue mode), or the stop bit was set.

When using the priority interrupt mode, one or two priority interrupt channels in the computer must first be turned on. This is accomplished with the CONO instruction to the priority interrupt system (PI) according to the bit map shown in Figure 2-8.

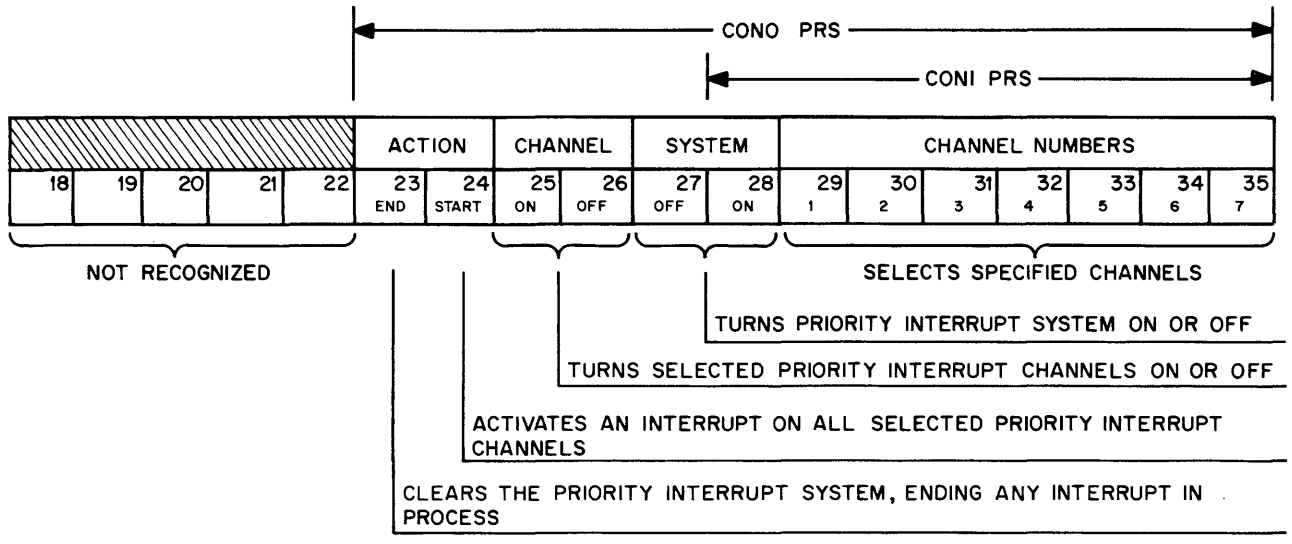


Figure 2-8 Priority Interrupt System Bit Format

The same channels must then be assigned to the display. This is accomplished with a CONO instruction to the display (DIS), as shown by the bit map in Figure 2-9. In this case, bits 30, 31, and 32 specify the octal number of the special priority interrupt channel, and bits 33, 34, and 35 specify the octal number of the data priority interrupt channel. When the initialize bit (29) is set, the done flag is set and a data interrupt request generated, and the DPY GO pulse is produced and applied to the display, clearing the light pen flag circuit and stop flip-flop and generating a request for data signal. The CONO instruction always produces the RESUME pulse, to clear the light pen flag flip-flops, and restarts the interrupted instruction (except in the character mode) unless bit 29 is set.

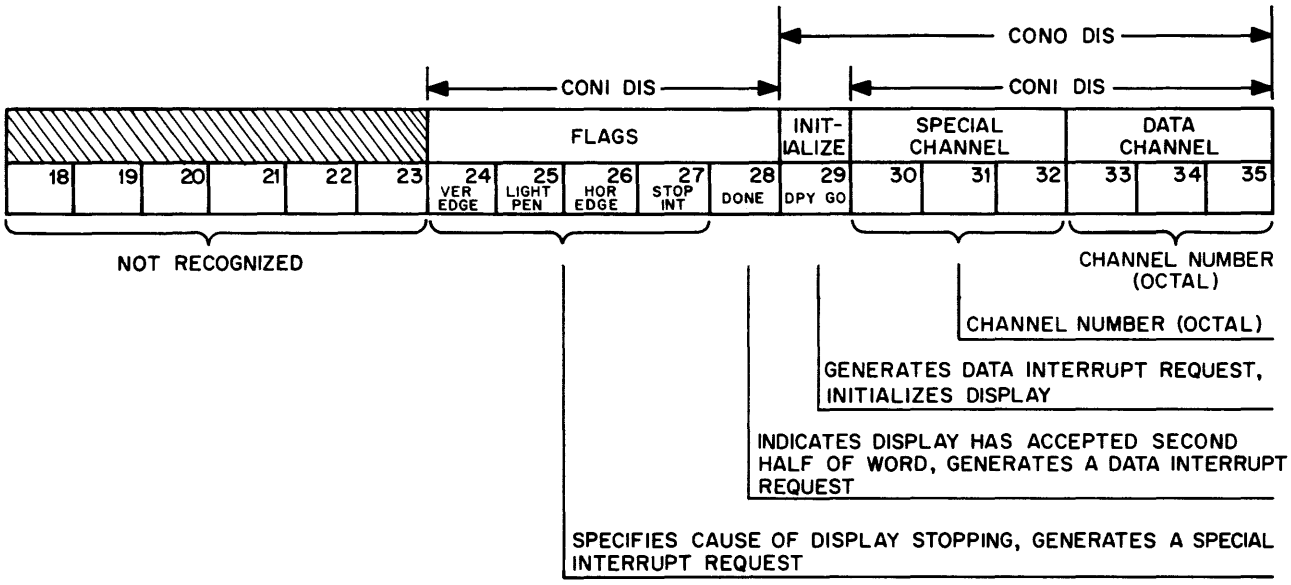


Figure 2-9 Display Interface Conditions Bit Format

When the computer grants an interrupt request, it executes the instruction contained in location 40 + 2J (where J is the number of the priority interrupt channel) without incrementing the program counter. As long as this instruction does not change the program counter, the computer will resume its program at the point where the interrupt occurred. However, if it is a jump or similar instruction that does change the program counter, some means must be provided to return the program to its interrupted location.

Normally the instruction in location 40 + 2J will be a jump to subroutine, JSR or a BLKO. In the case of the JSR the PDP-6 processor first calculates the effective address, then stores the

current program flags in the left half of the effective address and the contents of the program counter (which has been incremented and points to the next instruction in the normal sequence) in the right half of the effective address; and lastly jumps to the effective address + 1. This is the beginning of a subroutine that services the interrupt. At or near the end of this subroutine must be a JRST or CONO instruction to dismiss the priority interrupt channel; otherwise no interruptions can occur from lower or equal priority interrupt channels if they exist. The last entry in the subroutine may be a jump and restore (JRST) instruction that jumps indirectly back to the first address in the subroutine. In this location are stored the contents of the flags and program counter, so the program resumes at the location specified in the right half of this word. The JRST instruction must have the number 12 in its accumulator field to dismiss the priority interrupt channel and restore the flags and program counter.

The BLKO instruction is used to transmit a block of data words, one word at a time to the interface for use by the display. This instruction goes to its effective address to pick up a pointer word. In the left half of the pointer word is the negative of the number of words in the table, and in the right half of the word is the location -1 of the beginning of the table. This pointer word is retrieved from memory and each half incremented by one. The computer then fetches the word specified by the address in the right half of the pointer word, places it on the I/O bus, and produces the DATAO CLEAR and DATAO SET pulses to transfer this word to the display. At the same time, the left half of the pointer word is tested for a zero to determine the next action. If the left half is zero (end of block condition), the computer next executes the instruction in location 41 + 2J (without disturbing the program counter). This instruction must be a JSR to a subroutine that will dismiss the priority interrupt channel and return the computer to its interrupted program location and may reset the pointer. If the left half of the pointer word is not zero, the priority interrupt channel is automatically dismissed and the computer returns to its normal program at the location specified by the program counter.

The DATAO instruction transfers just the one word specified by the effective address to the interface buffer. The DATAI instruction transfers the X and Y coordinates to the location specified by the effective address. The Y coordinate is contained in bits 8 through 17 (right justified in the left half of the word), and the X coordinate is contained in bits 26 through 35 (right justified in the right half of the word).

Either the CONI, CONSZ, or CONSO instruction will transfer the current states of the flag and priority interrupt flip-flops to the effective address. These are located in bits 24 through 34 (except 29) as shown in Figure 2-9. The CONSZ and CONSO instructions test these bits against a mask in the effective address. If all the bits in the mask which are ones match the ones in the flag and interrupt bits, the CONSO executes the next instruction in sequence while the CONSZ skips this instruction and executes the second instruction in sequence. However, if any mask bit which is a one coincides with a zero in the flag and interrupt bits, the CONSZ executes the next instruction while the CONSO skips this and executes the second instruction.

A demonstration program is listed in Table 2-3. This program continously draws the figure ꟾB in the lower right corner of the raster. If the light pen sees any part of the figure except the lower left dot of the B, the program halts until the I/O RESET key is depressed. If this particular dot is seen by the light pen, the display gets brighter and the computer halts. If the figure violates an edge of the raster, the display moves until no violation occurs.

This program is written for the MACRO6 Assembler. All numbers are octal (radix 8). If many increment modes words are used, they can be coded easier in numbers to the radix 4, (see Figure 2-6). Notice that the first word (left half) in the last data table entry stops the display and generates a new data interrupt. Since the first data interrupt has not yet been dismissed, the computer does another BLKO instruction, sees that the left half of the pointer word is zero, and enters the REPEAT subroutine. This renews the pointer word and dismisses the interrupt channel, at which time the second data interrupt is entered and the display cycle repeats itself.

If the display data table is to be changed or modified, thus varying its length, the last word in the table should be 003000_8, which would halt the display, set the stop flag, and generate a special interrupt request. The stop flag subroutine must then renew the pointer word. The table length then becomes independent of the pointer word as long as it does not exceed the value specified.

TABLE 2-3 TYPICAL PDP-6 PROGRAMMING EXAMPLES

```
Location : Instruction AC , Address (Index) ; Comments
         .............
         CONO      PI, 2203          ; ASSIGNS AND TURNS ON PI CHANNELS 6
                                     ; AND 7.
         .............
         CONO     DIS, 167           ; ASSIGNS PI CHANNELS 6 AND 7 TO DISPLAY,
                                     ; SETS DONE FLAG AND GENERATES DATA IN-
                                     ; TERRUPT ON PI CHANNEL 7.
         .............
LOC 54 : JSR          , WHY          ; SPECIAL INTERRUPT SUBROUTINE.
         Z                           ; NOT USED.
LOC 56 : BLKO     DIS, TABLE         ; DATA INTERRUPT, TRANSFERS 1 WORD.
         JSR          , REPEAT       ; JUMP TO RESTORE POINTER WORD.
         .............
 TABLE : XWD       -13, TABLE        ; POINTER WORD.
         XWD    030133, 220000       ; SETS PARAMETERS, Y AXIS.
         XWD    103760, 703100       ; SETS X AXIS, DRAWS LINE.
         XWD    140000, 304210       ; SETS MODE, DRAWS CURVE.
         XWD    325063, 631777       ; DRAWS CURVE.
         XWD    100000, 600210       ; SETS MODE, DRAWS LINE.
         XWD    140000, 237463       ; SETS MODE, DRAWS CURVE.
         XWD    231673, 704210       ; DRAWS CURVE.
         XWD    100000, 203400       ; SETS MODE, DRAWS LINE.
         XWD    600203, 140000       ; DRAWS LINE, SETS MODE.
         XWD    377463, 631273       ; DRAWS CURVE.
         XWD    002000, 000000       ; STOPS, SETS DONE FLAG, GENERATES DATA
                                     ; INTERRUPT.
         .............
REPEAT : Z                           ; BLANK TO STORE FLAGS AND PC.
         MOVE         0, POINT       ; FETCH POINTER WORD.
         MOVEM        0, TABLE       ; RENEW POINTER WORD.
         JRST        12, @.-3        ; DISMISSES PI CHANNEL, RESTORES FLAGS
                                     ; AND PC.
 POINT : XWD       -13, TABLE        ; POINTER WORD FOR DATA INTERRUPT.
         .............
   WHY : Z                           ; BLANK TO STORE FLAGS AND PC.
         CONSZ    DIS, 2000          ; TEST FOR LIGHT PEN INTERRUPT.
         JSR          , LPFLAG       ; JUMP IF LP FLAG IS SET.
         CONSZ    DIS, 1000          ; TEST FOR HORIZONTAL EDGE VIOLATION.
         JSR          , HFLAG        ; JUMP IF HOR EDGE FLAG IS SET.
         CONSZ    DIS, 4000          ; TEST FOR VERTICAL EDGE VIOLATION.
         JSR          , VFLAG        ; JUMP IF VER EDGE FLAG IS SET.
         CONSZ    DIS, 400           ; TEST FOR STOP INTERRUPT.
         JSR          , STOP         ; JUMP IF STOP FLAG IS SET.
```

TABLE 2-3 TYPICAL PDP-6 PROGRAMMING EXAMPLES (continued)

```
Location : Instruction AC , Address (Index) ; Comments

         JRST      12, @WHY          ; JUMP INDIRECT TO WHY, RESTORE FLAGS
                                     ; AND PC, AND DISMISS PI CHANNEL.
         .............
LPFLAG : Z                           ; BLANK TO STORE FLAGS AND PC.
         CONO      DIS, 67           ; COMPLETES DISPLAY.
         JSR         , SAVEAC        ; JUMP TO SUBROUTINE, THEN RETURN.
         DATAI     DIS, STORE        ; STORE X AND Y COORDINATES.
         HLRZ        2, STORE        ; Y COORDINATE TO AC2, SWAPPED.
         TRNE        2, 1777         ; TEST FOR BOTTOM EDGE OF RASTER.
         JRST         , HOLD         ; JUMP IF NOT BOTTOM EDGE.
         HRRZ        2, STORE        ; X COORDINATE TO AC2.
         TRNE        2, 1003         ; TEST FOR VERTICAL BAR.
         JRST         , HOLD         ; JUMP IF NOT VERTICAL BAR.
         MOVS        3, TABLE+1      ; RETRIEVE PARAMETER WORD, SWAPPED.
         ADDI        3, 1601         ; INCREMENTS INTENSITY, SETS DONE
                                     ; FLAG AFTER SECOND TIME.
         MOVSM       3, TABLE+1      ; REPLACE PARAMETER WORD, SWAPPED.
         JSR         , RSTAC         ; JUMP TO SUBROUTINE, THEN RETURN.
         JRST        2, @LPFLAG      ; JUMPS INDIRECT TO LPFLAG, RESTORES
                                     ; FLAGS AND PC.
  HOLD : JRST        4, .-2          ; HALTS UNTIL I/O RESET KEY IS DEPRESSED,
                                     ; THEN RESUMES.
 STORE : Z                           ; BLANK TO STORE X AND Y COORDINATES.
         .............
 HFLAG : Z                           ; BLANK TO STORE FLAGS AND PC.
         JSR         , SAVEAC        ; JUMP TO SUBROUTINE, THEN RETURN.
         MOVS        3, TABLE+2      ; RETRIEVE PARAMETER WORD, SWAPPED.
         ADDI        3, 1            ; INCREMENT X COORDINATE.
         MOVSM       3, TABLE+2      ; REPLACE PARAMETER WORD, SWAPPED.
         JSR         , RSTAC         ; JUMP TO SUBROUTINE, THEN RETURN.
         JRST        2, @HFLAG       ; JUMPS INDIRECT TO HFLAG, RESTORES
                                     ; FLAGS AND PC.
         .............
 VFLAG : Z                           ; BLANK TO STORE FLAGS AND PC.
         JSR         , SAVEAC        ; JUMP TO SUBROUTINE, THEN RETURN.
         HRR         3, TABLE+1      ; Y COORDINATE RETRIEVED.
         ADDI        3, 1            ; INCREMENT Y COORDINATE.
         HRRM        3, TABLE+1      ; REPLACES Y COORDINATE.
         JSR         , RSTAC         ; JUMP TO SUBROUTINE, THEN RETURN.
         JRST        2, @VFLAG       ; JUMPS INDIRECT TO VFLAG, RESTORES
                                     ; FLAGS AND PC.
         .............
```

TABLE 2-3 TYPICAL PDP-6 PROGRAMMING EXAMPLES (continued)

```
Location : Instruction AC , Address (Index) ; Comments

  STOP : Z                                  ; BLANK TO STORE FLAGS AND PC.
         JRST      16, @STOP                ; RESTORES FLAGS AND PC, DISMISSES
                                            ; INTERRUPT, AND HALTS.
         .............
SAVEAC : Z                                  ; BLANK TO STORE FLAGS AND PC.
         MOVEM      0, ACCMTB               ; STORE AC0 IN TABLE.
         MOVE       0, .+3                  ; FETCH BLOCK DESIGNATOR WORD.
         BLT        0, ACCMTB+17            ; STORE ACCUMULATORS.
         JRST       2, @SAVEAC              ; JUMP INDIRECT TO SAVEAC, RESTORE
                                            ; FLAGS AND PC.
         XWD        1, .+2                  ; BLOCK DESIGNATOR WORD.
ACCMTB : BLOCK     20,                      ; SIXTEEN BLANK LOCATIONS TO STORE
                                            ; ACCUMULATORS IN.
         .............
  RSTAC : Z                                 ; BLANK TO STORE FLAGS AND PC.
         MOVE      17, .+3                  ; FETCH BLOCK DESIGNATOR WORD.
         BLT       17, 17                   ; RESTORE ACCUMULATORS.
         JRST       2, @RSTAC               ; JUMP INDIRECT TO RSTAC, RESTORE
                                            ; FLAGS AND PC.
         XWD  ACCMTB, 0                     ; BLOCK DESIGNATOR WORD.
```

SECTION 3

LOGICAL OPERATION

The Type 340 operates as a small, special purpose, stored program computer. It uses part of the memory in its controlling computer to store its program, performs the instruction contained in this memory in a step by step sequence, calculates the hypotenuse of a right triangle in the vector and vector continue modes, and is capable of jumping to subroutines in the subroutine mode. In order to understand the operation of the display, it is necessary first to know what the display does in each of its modes, and then to follow the path of a signal through the display's circuits in these modes. This can best be accomplished with the signal flow diagram shown in Figure 3-1.

SIGNAL FLOW

Initial Starting

The Type 340 is turned on either by throwing the switch on the power control panel to ON or by the computer supplying a -15 volt remote turn on signal. When this occurs, power is immediately available for the logic circuits, but the CRT and its ultor voltage power supply require a few seconds warmup time. Initially the flip-flops are arbitrarily set, but this does not affect most of the registers as they are cleared before they are loaded. However, some of the control flip-flops must be preset before the display can begin normal operation. This is accomplished with the IOT display load address counter, DLA, ~~if a PDP-1, PDP-4, or PDP-7 is used, or the CONO DIS 0001XY if the PDP-6 is used~~. These instructions produce the DPY GO pulse.

This pulse, shown on the lower part of Figure 3-1, clears the 3-bit mode register, the three light pen flip-flops, and the stop flip-flop. It also generates the RFD pulse which clears the two edge flag flip-flops (HEF and VEF) and sets the RFD flip-flop, generating the RFD ⟶ LT level which requests a data word from the computer. When the computer grants this request, the first word is interpreted in the parameter mode and sets up the parameter flip-flops according to the information contained in it.

Parameter Mode

When the three mode flip-flops hold the octal number 0, the next word loaded into the buffer register is interpreted in the parameter mode. The information in this word sets the mode register flip-flops to the mode for the next word and may set the stop flip-flop, generate a STOP INTERRUPT signal, and set or clear the light pen enabling flip-flop, the scale register flip-flops, and the intensity register flip-flops. The parameter word bit map is shown in Figure 2-1.

The computer issues a DATA SYNC pulse either just before or when the requested 18-bit data word is available on the input cable. This pulse, shown at the top left of Figure 3-1, starts the display's operation. It generates the CLR BR pulse which (1) clears the buffer register (BR) and the RFD flip-flops; (2) produces the CRL BRM pulse that clears the binary rate multiplier (BRM), sequence register (S), the two edge flag flip-flops (HEF and VEF), and the halt and move flip-flops; and (3) initiates a 2.8-microsecond setup delay. This delay allows the input word time to set up the readin gates to the BR and for the carries in the BRM to die out.

At the end of the setup delay period a READ TO S pulse is produced. This pulse sets the LP flag flip-flop if the light pen is enabled and saw a spot during the last display operation. The READ TO S pulse also generates the LOAD BR ~~and SHIFT IB~~ pulse and initiates an 0.5-microsecond intensify s delay. The LOAD BR pulse transfers those bits of the input word which are logic ones to the buffer register. ~~The SHIFT IB pulse is only used with the PDP-6, and it shifts the right half of the interface buffer (IB) into the left half with a jam transfer.~~ The 0.5-microsecond delay allows time for the BR to be loaded and its output to stabilize, but the duration is set as the spot intenisfication time when in the increment, vector, or vector continue modes. At the end of this delay an intensify delay pulse (IDP) is produced. The display now chooses how it will interpret the word in its BR.

Since this is the parameter mode, a READ TO MODE pulse and a parameter mode pulse (PM PULSE) are produced. The READ TO MODE pulse loads the 3-bit mode register with the contents of BR2, BR3, and BR4, setting the mode for the next word. If BR5 is a 1, the READ TO MODE pulse sets or clears the light pen enable (LP enable) flip-flop, according to BR6. LP enable is set when BR6 is a 1 and is cleared when BR6 is a 0.

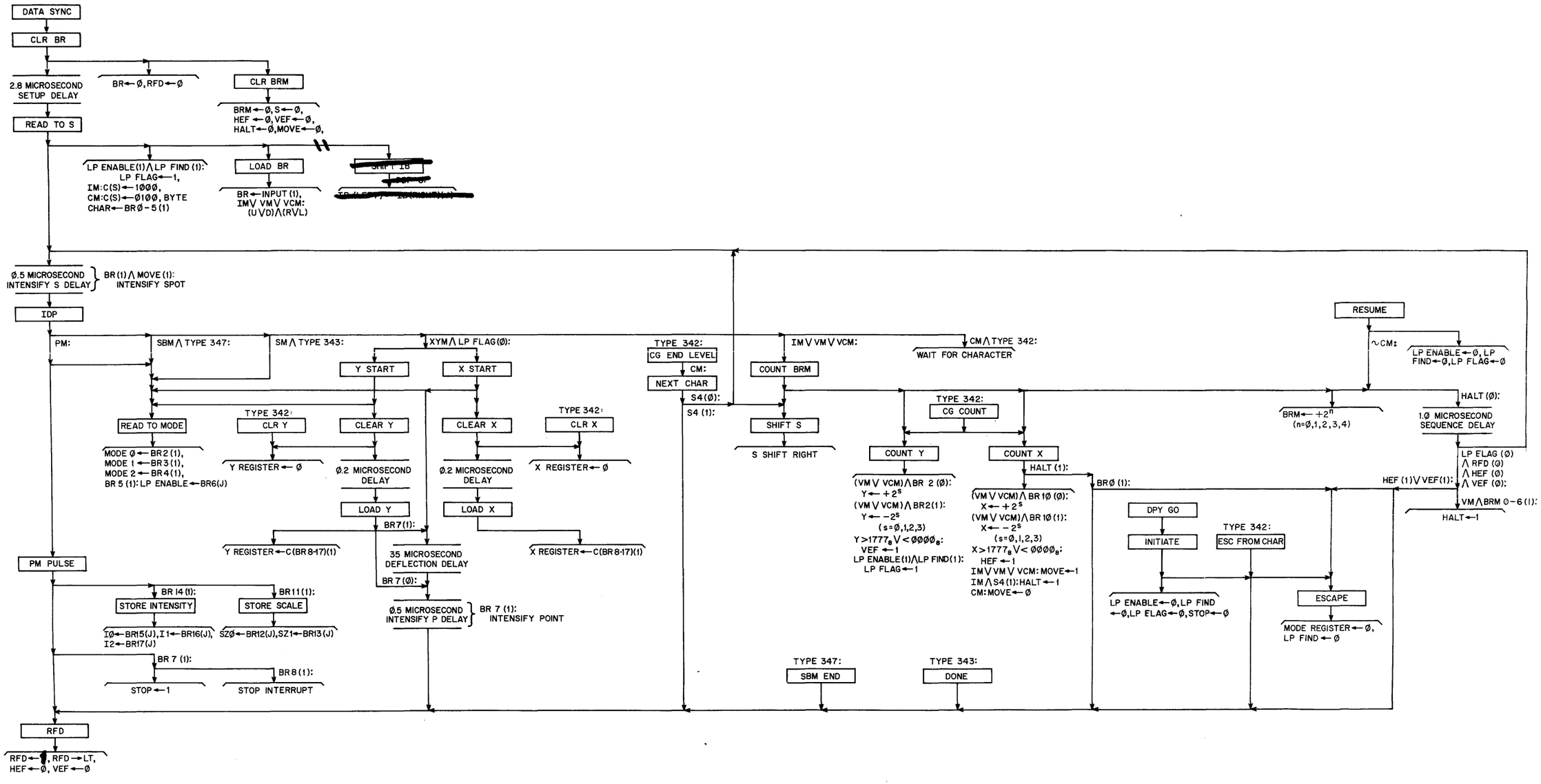


Figure 3-1 Flow Diagram

The PM PULSE performs various functions, depending on the states of BR7, BR8, BR11, and BR14. If another data break or word is needed, BR7 is a 0 and allows the RFD pulse to be generated. This pulse clears the two edge flag flip-flops and sets the RFD flip-flop, generating the request for data signal. If BR7 is a 1, the stop flip-flop is set and no data request is generated, stopping the display's operation. If BR8 is also a 1, a STOP INTERRUPT signal is produced, generating an interrupt request for the computer. When BR11 is a 1, a STORE SCALE pulse is produced which loads the 2-bit scale register (SZ) with the contents of BR12 and BR13. When BR14 is a 1, a STORE INT. LEVEL pulse is produced that loads the 3-bit intensity level register (I) with the contents of BR15, BR16, and BR17.

When the stop flip-flop is set and the display halts, the computer must restart operation by either another display load address counter IOT or by issuing another word and a DATA SYNC pulse after the IOT display clear flags, DCF.

Point Mode

When the display is in the point mode, it sets the horizontal (X) and vertical (Y) registers to the coordinates of the spot location. This requires two word transfers, one for each coordinate. Since magnetic deflection is used, a 35-microsecond set up time is required before the spot can be intensified. Either word transfer can intensify the spot if desired, or this can be the starting location of a line, curve, or character specified by the next word(s) to be transferred.

Operation in the point mode only occurs if the previous word (either a parameter, point, slave, or a subroutine) had set the mode register to 001 (1_8). When the display has been placed in the point, or XY, mode it interprets the 18-bit word according to Figure 2-2. The series of events from the setting of the RFD flip-flop to the generation of the IDP pulse is the same as described for the parameter mode. At this point, provided the light pen flag is not set, the display examines the state of BR1. When BR1 is a 0, the display interprets the word as a horizontal point word and generates an X START pulse; and when BR1 is a 1, the display interprets the word as a vertical point word and generates a Y START pulse. If the LP flag is set, the display halts.

Either an X START pulse or a Y START pulse will generate the READ TO MODE pulse, loading the mode register with the contents of BR2, BR3, and BR4 for the next word's mode. The X START pulse

also generates a CLEAR X pulse and initiates a 35-microsecond delay. This is the deflection setup delay, allowing the deflection currents to stabilize at their final value before the spot is intensified. The CLEAR X pulse clears the X register and, 0.2-microseconds later, generates a LOAD X pulse which loads the X register with those bits in BR8 through BR17 which are ones. The Y START pulse also generates a CLEAR Y pulse which clears the Y register and, 0.2-microseconds later, generates a LOAD Y pulse which loads the Y register with those bits in BR8 through BR17 which are ones.

At this point the display examines the intensify bit, BR7. If this bit is a 0, the LOAD Y pulse initiates an 0.5-microsecond intensify p delay. (This is the intensify delay for the point mode.) At the end of this delay the RFD pulse is produced, clearing the two edge flag flip-flops and setting the RFD flip-flop, but not intensifying the spot.

However, if BR7 is a 1, the LOAD Y pulse will initiate the 35-microsecond delay. When this deflection setup time is over, the 0.5-microsecond intensify p delay is initiated. During this period an INT signal is produced which unblanks the CRT and produces a spot of light at the coordinates specified by the X and Y registers. When the intensify delay is over, the RFD pulse is produced and the display halts with a request for data generated.

> NOTE: The X point mode always produces the 35-microsecond deflection setup delay, whether or not the intensify bit is set; while the Y point mode only produces the 35-microsecond deflection delay if the intensify bit is set. Therefore the Y axis should precede the X axis when both axes are loaded to avoid an unnecessary delay.

Light Pen Interrupt

If the point mode operation is halted by the light pen seeing the previous spot, the IDP pulse will not produce an X START or Y START pulse. The computer can issue an instruction which produces the RESUME pulse in order for the display to complete its operation. (This is the IOT display resume, DRS.) ~~for the PDP-1, PDP-4, or PDP-7 and the CONO DIS 000 0XY for the PDP-6.)~~

The RESUME pulse clears the LP enable, LP find, and LP flag flip-flops and initiates a 1.0-microsecond delay. At the end of this time the 0.5-microsecond intensify s delay is again initiated and the display continues its operations where it left off.

Vector Mode

When the display is in the vector mode, it interprets the 18-bit word contained in its buffer register (BR) as two 8-bit bytes, an intensify bit, and an escape bit; as shown in Figure 2-4. The display is placed into the vector mode by either a parameter, point, slave, or subroutine word whose mode bits set the mode register to 100 (4_8). Once in the vector mode, the display can only escape back to the parameter mode when the escape bit is set or when a vector is drawn past an edge of the raster.

The initial operation in the vector mode is the same through the generation of the intensify delay pulse (IDP) as in all other modes. Since this is the vector mode, the IDP pulse generates a COUNT BRM pulse which complements the least-significant bit of the binary rate multiplier (BRM_6) and other less significant BRM bits as determined by the magnitude of the larger component byte. (As many as five least-significant BRM bits are complemented simultaneously, one more than the number of most-signifcant zeros in the largest byte.) The COUNT BRM pulse also generates a SHIFT S pulse, COUNT Y pulse, and a COUNT X pulse, and it initiates a 1.0-microsecond sequence delay. The SHIFT S pulse has no effect in the vector mode.

During the 1.0-microsecond operating time of the delay, the COUNT X and COUNT Y pulses either increment or decrement their respective registers according to the sign of each component byte. The bit which is complemented in the registers is determined by the scale factor S held in the scale (SZ) register. The COUNT X pulse also sets the move flip-flop.

At the end of the 1.0-microsecond sequence delay a pulse is produced which initiates the 0.5-microsecond intensify S delay again, forming a 1.5-microsecond loop. Since the move flip-flop has been set, the spot is now intensified if the intensity bit (BR1) is also set. At the end of the intensify S delay the COUNT BRM pulse is again produced and the process repeats itself.

NOTE: The vector is first intensified after the first move from the starting location. If necessary, the starting location must be intensified by the word which precedes the vector.

During the vector display operation, the light pen may see the spot. When this occurs the LP find flip-flop is set if the LP enable flip-flop is set. The COUNT Y pulse then sets the LP flag flip-flop, preventing the intensify delay from being initiated at the end of the sequence delay and generating an interrupt signal. The display then halts its operation before it has finished the vector. The computer must service the interrupt and issue the IOT display resume, DRS, which produces the RESUME pulse. Since this clears the LP enable flip-flop, the next parameter word should reset it.

If either the COUNT Y or COUNT X pulse causes its register to overflow (become negative when counting down or exceed 1777_8 when counting up), the associated edge flag flip-flop is set. This produces an interrupt signal for the computer and generates an ESCAPE pulse at the end of the sequence delay which clears the three mode register flip-flops. This also prevents the intensify s delay from being reinitiated; so the display halts when the vector violates an edge of the raster. The computer must service the interrupt and either issue the IOT display load address counter, DLA, or transfer a parameter word with a DATA SYNC pulse to restart the display.

Normally the display will complete the vector. When the last point of the vector is computed, the BRM is filled. The halt flip-flop is then set at the end of the 1.0-microsecond sequence delay. This prevents the next COUNT BRM pulse from reinitiating the delay and causes the COUNT X pulse to produce the DPY pulse. If this vector word has its escape bit set, the COUNT X pulse also produces the ESCAPE pulse, clearing the mode register so that the next word transferred is interpreted as a parameter word.

Vector Continue Mode

The vector continue mode is essentially the same as the vector mode in its operations. It differs in only two operations, both of which occur at the end of the 1.0-microsecond sequence delay.

First, when the BRM has finished computing the vector specified by the two component bytes, the halt flip-flop is not set. Instead, the BRM starts over again at zero, computing a new

vector of the same angle and length as before, starting where the old one left off. This process continues until an edge is hit, when the edge flag flip-flop is set. This halts the display and generates both the ESCAPE and the RFD pulses. No program interrupt is generated when the edge is violated.

Increment Mode

When the display is in the increment mode, it interprets the 18-bit word contained in its buffer register (BR) as four 4-bit bytes, an intensify bit, and an escape bit, as shown in Figure 2-5. The display is placed into the increment mode by either a parameter, point, slave, or subroutine word whose mode bits set the mode register to 110 (6_8). Once in the increment mode, the display can only escape back to the parameter mode when the escape bit is set or when a point is plotted beyond an edge of the raster.

Operation of the display in the increment mode is the same as in all other modes through generation of the intensify delay pulse (IDP). Note that the READ TO S pulse set the most-significant (S 1) flip-flop in the sequence register.

The IDP pulse generates the COUNT BRM pulse, just as in the vector mode. However, incrementing the BRM has no effect on the display's operation in the increment mode. The SHIFT S, COUNT Y, and COUNT X pulses are produced, and the 1.0-microsecond sequence delay is initiated just as in the vector mode. The COUNT Y and COUNT X pulses produce the same incrementing or decrementing operation in their respective registers, but this is only done once for each byte.

The COUNT X pulse is also used to set the halt flip-flop as the fourth byte is being processed. After this byte is processed, the RFD pulse is produced (the ESCAPE pulse may also be produced) in the same manner as in the vector mode. Following the sequence of events listed in Table 3-1 makes clear the display's incrementing operation.

TABLE 3-1 INCREMENT MODE OPERATION

Pulse or Delay	Operation
CLR BR	Clears buffer register and RFD flip-flops.
CLR BRM	Clears binary rate multiplier, sequence registers, and the edge flag, halt, and move flip-flops.
Setup Delay	2.8 microsecond delay time.
READ TO S	Sets sequence register to 1000.
LOAD BR	Buffer register loaded with 18-bit increment word.
Intensify S Delay	0.5 microsecond delay time. Direction levels (U or D) and (R or L) produced as specified by byte 1. Spot not intensified because move is cleared.
IDP	Produces COUNT BRM pulse.
COUNT BRM	Increments BRM (no effect); produces SHIFT S, COUNT X, and COUNT Y pulses.
COUNT X	Changes X register by the amount specified by the size register if an R or L direction level exists, sets move.
COUNT Y	Changes Y register by the amount specified by the size register if a U or D direction level exists.
SHIFT S	Shifts the sequence register right one place (0100).
Sequence Delay	1.0 microsecond delay time. Byte 2 direction levels produced.
Intensify S Delay	First increment intensified if BR1 is set.
IDP	Produces COUNT BRM pulse.
COUNT BRM	Increments BRM (no effect); produces SHIFT S, COUNT X, and COUNT Y pulses.
COUNT X	Changes X according to byte 2 direction levels.
COUNT Y	Changes Y according to byte 2 direction levels; may set LP FLAG.
SHIFT S	Shifts the sequence register right one place (0010).

TABLE 3-1 INCREMENT MODE OPERATION (continued)

Pulse or Delay	Operation
Sequence Delay	1.0 microsecond delay time. Byte 3 direction levels produced.
Intensify S Delay	Second increment intensified if BR1 is set.
IDP	Produces COUNT BRM pulse.
COUNT BRM	Increments BRM (no effect); produces SHIFT S, COUNT X, and COUNT Y pulses.
COUNT X	Changes X according to byte 3 direction levels.
COUNT Y	Changes Y according to byte 3 direction levels; may set LP FLAG
SHIFT S	Shifts the sequence register right one place (0010).
Sequence Delay	1.0 microsecond delay time. Byte 4 direction levels produced.
Intensify S Delay	Third increment intensified if BR1 is set.
IDP	Produces COUNT BRM pulse.
COUNT BRM	Increments BRM (no effect); produces SHIFT S, COUNT X, and COUNT Y pulses.
COUNT X	Changes X according to byte 4 direction levels, sets halt.
COUNT Y	Changes Y according to byte 4 direction levels; may set LP FLAG
SHIFT S	Shifts the sequence register right one place (0000).
Sequence Delay	1.0 microsecond delay time. No direction levels produced.
Intensify S Delay	Fourth increment intensified if BR1 is set.
IDP	Produces COUNT BRM pulse.
COUNT BRM	Increments BRM (no effect); produces COUNT X, COUNT Y, and SHIFT S pulses.
COUNT X	Produces RFD pulse, and the ESCAPE pulse if BR0 is set.
COUNT Y	May set LP FLAG.

TABLE 3-1 INCREMENT MODE OPERATION (continued)

Pulse or Delay	Operation
SHIFT S	No effect.
RFD	Sets RFD flip-flop, clears edge flag flip-flops.
ESCAPE	Clears mode register to the parameter mode.

Character Mode

When the display is in the character mode, it interprets the 18-bit word in its BR as three 6-bit character bytes. (These bytes are shown in Figure 2-6.) The display is placed in the character mode when its mode register contains 011 (3_8). Once in the character mode, the display can only escape back to the parameter mode when the character generator (CG) decodes an escape character and produces the ESC FROM CHAR pulse or when the computer issues the instruction which produces the DPY GO pulse.

Initial operation of the display is the same as in all other modes through the production of the IDP pulse. From this point on, the CG produces the necessary control levels and pulses to operate the display in a manner similar to the increment mode. Note that the READ TO S pulse loads the sequence register with 0100, which places the first character byte (BR0 through BR5) on the input cable to the CG. Also, the spot is not intensified because the move flip-flop was cleared by the CLR BRM pulse. (This flip-flop is never set in the character mode.)

The CG decodes the 6-bit character byte into one of 64 characters or functions. The IDP pulse starts a chain of timing pulses in the CG which produces direction control levels, (U or D) and (R or L), COUNT pulses, and INTENSIFY levels according to the specific character. There may be as many as 30 pulses produced for each character, one every 1.5 microseconds.

Each COUNT pulse produces a COUNT X pulse and a COUNT Y pulse. These pulses are applied to the X and Y registers and increment or decrement the registers if the necessary

direction control level is present. The amount the register is changed depends on the scale factor held by the size register. This increments the spot one unit from its previous location.

If the spot is to be intensified, the CG supplies an INTENSIFY signal 1.0 microsecond after the COUNT pulse. This is an 0.5 microsecond level which lasts until the next COUNT pulse.

When the character has been processed, an END LEVEL signal is produced. Since the display is in the character mode, this produces the NEXT CHAR pulse. As long as the least-significant flip-flop (S4) in the sequence register holds a 0, the NEXT CHAR pulse produces a SHIFT S pulse and initiates the 0.5 microsecond intensify S delay. This shifts the sequence register to the right (applying the next character byte to the input cable of the CG) and then produces the IDP pulse that starts the CG operating again.

The first END LEVEL signal changes the sequence register to 0010, which places the second character byte (BR6 through BR11) on the input cable. The second END LEVEL signal changes the sequence register to 0001, which places the third character byte (BR12 through BR17) on the input cable. Since S4 now holds a 1, the third END LEVEL signal produces the RFD pulse, which requests another word from the computer, and the process repeats itself.

The CG decodes two special function bytes to produce extra control pulses. These are the carriage return (74_8) and escape (00_8) characters. When the escape character occurs, the first timing pulse produces the ESC FROM CHAR pulse. This produces both the ESCAPE and RFD pulses in the display, returning the display to the parameter mode and generating a request for data.

When the carriage return character occurs, the first timing pulse produces a carriage return (CR) pulse. This produces the CLEAR X (but not the LOAD X) pulse, returning the beam to the left-hand edge of the raster. Nine COUNT pulses also occur, dropping the beam down nine spaces. No INTENSIFY signals occur.

Subroutine Mode

When the display in the subroutine mode, it interprets the word in its BR according to Figure 2-7. If the display is equipped with the Type 347 Subroutine Interface, this word is decoded into

one of three jump instructions and the required operation is implemented. However, without the Type 347 the display only sets its mode register according to bits BR2, BR3, and BR4, and then halts without generating a request for data or interrupt signal.

The series of events within the display is the same as the other modes through the generation of the IDP pulse. Since this is the subroutine mode, the READ TO MODE pulse is also produced. This sets the mode register to the mode specified by the mode bits for the next word to be transferred. Nothing more happens in the display until the Type 347 finishes its operations.

When the Type 347 has completed its operation, it generates an SBM END pulse which produces the RFD pulse. This generates a new request for data signal for the computer, which then transfers the next word to the display.

Slave Mode

When the display is in the slave mode, it interprets the word in its BR according to Figure 2-3. If the display is equipped with the Type 343 Monitor option, this word is decoded into control signals for one or more of up to 16 slave monitor displays. However, without the Type 343 the display will only set the mode register for the next word and halt without requesting a new data word.

The series of events within the display is the same as all the other modes through the generation of the IDP pulse. Since this is the slave mode, the READ TO MODE pulse is also produced. This loads the mode register with the contents of BR2, BR3, and BR4, specifing the mode for the next word to be transferred. The Type 343 then produces a DONE pulse which generates the RFD pulse. This generates a new request for data signal for the computer, which then transfers the next word to the display.

CIRCUIT OPERATION

The various signal flow paths described previously control the operation of the 340 Display as far as the operation of each mode. However, there is much more involved in getting a spot of light to appear at a particular location on the face of the CRT. A thorough understanding of the operation of the display can only be obtained after going through the circuit block diagrams in Figures 6-4 through 6-8. Once this is done, reference to the signal flow diagram,

Figure 3-1, and the overall block diagram, Figure 6-3, is sufficient to review the theory of operation. In the discussion that follows, the signal path and operation of each of the circuits on the block diagram, Figure 6-3, are explained in relation to the circuits shown in Figures 6-4 through 6-8.

In order to understand the operation of the various modules in the display, refer to the System Module Catalog, C-100. Almost all of the modules used in the display are listed in this catalog, and those which are not are described in the end of this section. A detailed explanation of the various types of circuits is contained in the computer maintenance manual. The symbols used in the block schematics in Figures 6-4 through 6-8 are generally simplified versions of those shown in the module catalog. These symbols are explained in Figure 6-1.

Initializing

When the computer is ready to begin a display operation, it produces a DPY GO signal. This signal, a negative 400-nanosecond pulse or negative-going 2- to 5-volt level with a 200-nanosecond maximum rise time, is applied to the initiate circuit shown in the lower left corner of Figure 6-3. The initiate circuit is a 4604 Pulse Amplifier (shown in the right center section of Figure 6-4) which produces the INITIATE signal. This is a 400-nanosecond negative pulse that is applied to the escape circuit, light pen flag circuit, and the request for data circuit.

In the escape circuit, the INITIATE pulse produces the ESCAPE pulse which is applied to the mode register and decoder and the light pen flag circuit. The ESCAPE pulse is a 400-nanosecond positive pulse that clears the three mode register flip-flops and the LP find flip-flop. The INITIATE pulse is complemented by the inverter buffer in H24, shown in the lower right section of Figure 6-5, and triggers the 4604 Escape Pulse Amplifier to produce the ESCAPE pulse. This is applied to the direct clear input of the four flip-flops in E09, shown at the center left section of Figure 6-5. When the mode register flip-flops are cleared the register holds 0_8, which is decoded as the parameter (PM) mode by the 4150 Binary-to-Octal Decoder in E08.

In the light pen flag circuit, the INITIATE pulse clears both the LP find and the LP flag flip-flops. The INITIATE pulse is applied to inverter buffers in the lower left corner of Figure 6-6. The LP find flip-flop is cleared by momentarily grounding its 1 output terminal while the LP flag flip-flop is cleared by applying a positive pulse to its O gated input.

In the request for data circuit, the INITIATE pulse produces the request for data (RFD) pulse. The RFD pulse is a negative 400-nanosecond pulse that is applied to the RFD flag circuit and the edge violation circuit. In the right center section of Figure 6-4, the INITIATE pulse is complemented by an inverter buffer, triggering the 4604 Request for Data Pulse Amplifier. In the RFD flag circuit, the RFD pulse is complemented by an inverter buffer in the upper right section of Figure 6-4, momentarily grounding the O output of the RFD flip-flop in E11. This sets the RFD flip-flop to its 1 state, placing its O output at ground. This ground signal turns on the inverter buffer in F06 to produce the -3 volt RFD ⟶ LT signal, which is the "request for data" or "data request" that is applied to the computer to initiate a break cycle and transfer a word. In the edge violation circuit, the RFD pulse clears both the horizontal edge violation flag (HEF) and the vertical edge violation flag (VEF) flip-flops. The RFD pulse is applied to an inverter at the left center of Figure 6-7 (marked REQ FOR DATA), which applies a positive pulse to the O gated inputs of each flip-flop. This clears any flip-flop that may have been set during the preceding display cycle.

> NOTE: When the display is operated by the PDP-4 or PDP-7, only one edge violation flip-flop may be used. In this case, only the 1209 Flip-Flop is in the circuit, marked CF (for corner flag). Its 1 input receives both the X and Y OVERFLOW pulses ORed together, and it does not use the 6113 NOR gate and CF inverter.

Transferring

When the PDP-1, -4, or -7 controls the display, the RFD ⟶ LT signal ("request for data" or "data request") initiates a break cycle during which one 18-bit word is fetched from the computer's memory and placed on the input gates of the buffer register. The computer then issues a DATA SYNC pulse which starts the display operation, and then resumes its main program operation. (This assumes that the direct access channel option is used. If not, the RFD ⟶ LT signal generates a program interrupt and the transfer is done by an IOT command.) The DATA SYNC signal is applied to the transfer circuit, producing four pulses that start the display operation. The CLR BR and the CLR BRM pulses are produced immediately, and are used to clear the buffer register, edge violation circuit, binary rate multiplier, sequence register, the halt and move circuits, and the RFD flag. The transfer circuit then produces the READ TO S and LOAD BR pulses which load the 18-bit word into the buffer register, samples the condition

of the flip-flops in the light pen flag circuit, initiates the intensify s delay, presets the sequence register, (if in the character or increment modes), and applies a SHIFT IB pulse to the Type 344 Interface if the display is used with a PDP-6.

Clearing the Registers and Flip-Flops

The transfer circuit is shown in the left center of Figure 6-4. The DATA SYNC pulse, a negative 400-microsecond pulse or a 2- to 5-volt negative level with a 200-microsecond maximum rise time, is applied to a 4603 Pulse Amplifier in H07. This pulse amplifier produces the CLR BR pulse, a negative 400-nanosecond pulse that is applied to another pulse amplifier in the same module, to a 4301 Delay in H08, to an inverter in E17 which clears the RFD flip-flop (located in the right center of Figure 6-4), and to the direct clear inputs of the buffer register (BR) located in the upper part of Figure 6-5. Each BR module contains 6 flip-flops which are cleared by a single pulse inverter.

The second 4603 Pulse Amplifier in H07 produces a positive clear binary rate multiplier (CLR BRM) pulse. This pulse is applied to the direct clear inputs of the halt and move flip-flops in H16 (shown in the upper right corner of Figure 6-4), to the direct clear inputs of the 7-bit binary rate multiplier (BRM) shown in the upper left corner of Figure 6-6, to the direct clear inputs of the sequence register (the CLR BRM pulse is labeled CLEAR S) shown in upper right corner of Figure 6-6, and to the direct clear inputs of the vertical and horizontal edge violation flip-flops in the edge violation circuit shown on the left side of Figure 6-7. This pulse clears all 33 flip-flops when it occurs.

Setup Delay Timing

The CLR BR pulse triggers the setup delay in H08, shown in the left center of Figure 6-4. This delay is adjusted from 1.0- to 2.8-microseconds, depending on the computer used. The PDP-4 uses a 4301 Delay which is set for 2.8 microseconds, while other computers may use a 1304 or a 6304 Delay for a faster setup delay time. After the setup delay, a negative READ TO S pulse is produced and applied to the light pen flag circuit and the sequence register. In the light pen flag circuit, the READ TO S pulse is applied to the base of a 6106 inverter gate in H14 (shown in the lower left of Figure 6-6). This inverter gate produces a positive pulse that sets the LP flag flip-flop to its 1 state if the emitter of the inverter has a ground potential on it. This

occurs when both the LP enable and the LP find flip-flops are set, activating the 4113 NAND gate in F08. This is not possible on the first word transfer because the INITIATE pulse previously cleared the LP find flip-flop.

Presetting the Sequence Register

The READ TO S pulse is applied to two 4113 NAND gates in E16 at the upper right corner of Figure 6-6. If the display is in either the increment or character modes, one of these gates is enabled, and the READ TO S pulse momentarily grounds the O output of either the S1 or S2 flip-flop in the sequence register, presetting the register to its required number. This cannot occur on the first word transfer because the mode register is set to the parameter mode by the ESCAPE pulse.

Loading the Buffer Register

The READ TO S pulse triggers the third 4603 Pulse Amplifier in H07, shown in the left center of Figure 6-4, producing the 400-nanosecond negative LOAD BR pulse. This pulse is applied to the load pulse inverter in each BR module shown at the top of Figure 6-5. Each pulse inverter complements the LOAD BR pulse, producing a positive trigger pulse that is applied to the input of the six capacitor-diode gates in the module. Each of these capacitor-diode gates that has a logic 1 ground potential on its level input for at least 1 microsecond is enabled, and these gates differentiate the trigger input to produce a positive output pulse that sets the associated flip-flop to its 1 state. This transfers the 18-bit input word into the BR, because those bits of the input word which are 1's set their associated flip-flop to 1 and those bits which are zeros do not change their associated flip-flops.

The 4220 Flip-Flop modules in the buffer register have only one output terminal per flip-flop. This is internally jumpered to the O output of the flip-flop, which is ground when the flip-flop is in the 1 state. Each of these outputs are applied to the base of a 4102 Inverter, which complements the bit and increases the driving power. The outputs of these inverter buffers are labeled BBR with a subscript to note the bit number and a superscript 1 to denote the logic state of the flip-flop when this signal is a - 3 volt level.

Storing

~~If the display is used with the PDP-6 computer, the LOAD BR pulse is applied to the Type 341 Display Interface as the SHIFT IB pulse. This pulse shifts the right half of the 36-bit word in the interface buffer (IB) to the left half, for the next transfer to the display.~~ The LOAD BR pulse is also applied through a 6102 Inverter (which improves the pulse rise time) to trigger a 1609 Pulse Amplifier in H09. This pulse amplifier produces a 70-nanosecond negative pulse that is applied to 1304 Delay in H12. This is the intensify s delay; adjusted for a 0.5-microsecond period. During the delay's operating time a -3 volt int s signal is produced from terminal J. This is applied to a 1615 NAND gate in H15 (located in the lower right of the center section of Figure 6-4). This gate is never enabled the first time the delay is activated because the move flip-flop was previously cleared by the CLR BRM pulse. However, if the display is set to its increment, vector, or vector continue modes the move flip-flop will later be set allowing the INT S signal to intensify the spot each time the intensify s delay again is triggered, (if the intensify bit, BR1, is set).

At the end of the intensify delay period an intensify delay pulse (IDP) is produced. This pulse is applied to the parameter store circuit, y axis circuit, x axis circuit, repeat circuit, and is available as a timing pulse for the Type 342 Character Generator or for other options. The IDP pulse goes up the left side of Figure 6-4, and is applied to a 6106 Inverter in H21 that is part of the parameter store circuit. This inverter gate is enabled by the 6113 NAND gate in H23 when the display is in the parameter (PM) mode. (This gate may also be qualified by the RI(0) signal from the PDP-6 interface.) The output of the inverter gate triggers the read to mode circuit directly (shown on the block diagram as the PM PULSE) and triggers a 4604 Pulse Amplifier in H25. This pulse amplifier produces the PM PULSE, a 70-nanosecond negative pulse that is applied to the store intensity circuit, store scale circuit, stop flag circuit, and request for data circuit.

Storing the Mode

The read to mode circuit is a 4606 Pulse Amplifier in H11, shown at the top left of Figure 6-4. This pulse amplifier produces the READ TO MODE (RTM) pulse, a negative 400-nanosecond pulse that is applied to the mode register and decoder and the light pen flag circuit. This pulse is applied to the pulse inverter in the 4218 Flip-Flop in E09 (shown at the left center of Figure 6-5),

producing a positive trigger pulse that is applied to all the capacitor-diode gates in the module. Three of these flip-flops, with their associated set and clear capacitor-diode gates, constitute the mode register. These gates are controlled by BR2, BR3, and BR4. The fourth pair of capacitor-diode gates are permanently disabled by a -3 volt potential on their level inputs. The RTM pulse therefore sets the mode flip-flops to the state of the mode bits in the BR.

Arming the Light Pen Circuit

The RTM pulse also sets the LP enable flip-flop if required. This is shown in the lower right corner of Figure 6-5. Two 6115 NAND gates receive the RTM, BR5, and BR6 signals. When BR5 is a 1, one of these two gates will be enabled by BR6, depending on the state of the BR6 flip-flop. The RTM pulse then produces a ground output from the enabled NAND gate which sets the flip-flop if BR6 is a 1 and clears the flip-flop if BR6 is a 0.

Loading the Deflection Registers

The Y axis circuit and X axis circuit are similar, therefore only the latter circuit will be described and the differences between the two noted. The IDP pulse is applied to a 6106 Inverter gate in D11, part of the X axis circuit shown at the left center of Figure 6-4. This inverter gate is enabled by the 6115 NAND gates in E20 when the mode register is in the point (XYM) mode, the LP flag flip-flop is not set (holds a 0), and the direction selection bit, BR1, is a 1 for the horizontal direction (or a 0 for the vertical direction). When this occurs, the inverter gate triggers a 1609 Pulse Amplifier in D13, producing the negative 70-nanosecond X START pulse. This pulse is complemented by a 6106 Inverter and triggers a second 1609 Pulse Amplifier in D13 that produces the CLEAR X pulse. This positive 70-nanosecond pulse is applied to the direct clear inputs of all 10 X register flip-flops, shown in the lower half of Figure 6-7. The CLEAR X pulse can also be produced by the CR, or CR FROM CG, pulse from the character generator.

> NOTE: When the display is used with the PDP-4 and has the character generator option, the CLEAR Y pulse may be produced in the same fashion as the CLEAR X pulse. The input from the character generator is the CLR Y pulse and the CR pulse may appear as the CLR X pulse.

The X START pulse goes through a 1311 Delay Line in D14, and triggers a 1609 Pulse Amplifier 0.2-microsecond later. This pulse amplifier produces a negative 70-nanosecond LOAD X pulse that is applied to ten inverter gates in the X register, shown in the bottom half of Figure 6-7. Those inverter gates, which are enabled by a ground bBR signal, set their associated flip-flops to the 1 states. The bBR signals are obtained from the 6102 Inverters shown under the Y register at the top of Figure 6-7.

Loading the Intensity Level Register

The PM PULSE produces the STORE INT LEVEL pulse from the store intensity circuit when BR14 is a 1. This pulse is applied to the 3-bit intensity level register, causing the intensity level specified by BR15, BR16, and BR17 to be jam transferred into the register. The store intensity circuit consists of a 6102 Inverter, a 6106 Inverter gate, and a 4604 Pulse Amplifier as shown in the upper left section of Figure 6-4. The BR14 signal is applied to the base of the 6106 Inverter, and allows the inverter to conduct when the signal is - 3 volts if there is a ground potential on the inverter emitter. This occurs when the PM PULSE is applied to the base of the 6102 Inverter. The pulse amplifier is then activated, producing the negative 400-nanosecond STORE INT LEVEL.

This signal is applied to the pulse inverter in the 4218 Flip-Flop module in E10, shown in the lower right corner of Figure 6-5. The pulse inverter complements the signal, producing a trigger pulse that is applied to the pulse inputs of all the capacitor-diode gates in the module. One pair of these gates (for the LP enable flip-flop) are permanently disabled by - 3 volts on their level inputs. The other three pairs of capacitor-diode gates receive the complementary voltages from bits 15, 16, and 17 on their level inputs. The capacitor-diode gate in each pair which is enabled by a ground potential applies a positive pulse to the flip-flop, clearing or setting it as the case may be.

The O output terminal of each of the intensity level flip-flops is applied directly to the CRT bias and focus circuit, a 4688 Variable Amplitude Negative Intensifier module in R21, shown in the upper right of Figure 6-8. These three signals control the cathode bias of the CRT when it is unblanked by the INT (INTENSIFY LEVEL) signal, varying the intensity of the displayed spot.

Loading the Scale Register

When BR11 is a 1, the PM PULSE produces a STORE SCALE pulse from the store scale circuit. This pulse is applied to the 2-bit scale register and decoder, causing the states of the scale bits (BR12 and BR13) to be jam transferred into the scale register. The store scale circuit and register are composed of the same circuit element types as the store intensity circuit and register and operates in the same fashion. The store scale circuit is located directly above the store scale circuit on Figure 6-4. The scale register is composed of two flip-flops (SZ0 and SZ1) in the 4218 Flip-Flop module in E11, shown in the lower left of Figure 6-5.

The scale register decoder, shown in the lower center of Figure 6-5, produces three output levels (SC, SCX4, and SCX8). In the normal or smallest scale the register holds 00 and all three levels are -3 volts, as indicated in Table 3-2. At this scale every spot on the raster is spaced at the minimum distance of approximately 0.01 inch. When the scale register holds 01, the SC level goes to ground, and the spots are spaced approximately 0.02 inch apart. Similarly, when the register holds ten, both the SC and SCX4 levels are ground and the spots are spaced approximately 0.04 inch apart; when the register holds 11, both the SC and SCX8 levels are ground and the spots are spaced approximately 0.08 inch apart.

The output levels of the scale register decoder are applied to the vertical and horizontal speedup circuits to determine the magnitude of the momentary signal increase when the spot is being moved in either the increment, vector, or vector continue modes. These signals are also applied to the X and Y registers, along with the complement of the SCX8 level to determine the amount the registers are incremented in the same modes.

TABLE 3-2 SCALE LEVEL RELATIONSHIPS

Scale Register	Spot Spacing	SC Level	SCX4 Level	SCX8 Level	Feed Forward Load Resistance
0 0	1	-3v	-3v	-3v	18,000 ohms
0 1	2	0	-3v	-3v	6,430 ohms
1 0	4	0	0	-3v	1,200 ohms
1 1	8	0	-3v	0	465 ohms

Deflecting

Both the horizontal and vertical deflection channels are identical; therefore they are described together. Each deflection channel consists of a 10-bit register, ten level amplifiers a digital-to-analog converter, a follow or hold circuit, a speedup circuit, a deflection preamplifier, and a deflection amplifier. Basically each deflection channel converts the 10-bit binary word in its register into an equivalent analog voltage, then uses this voltage to generate two currents that flow in opposing coils within the deflection yoke. The resultant magnetic field from the two coils deflects the beam of the CRT to the desired location on the raster.

The loading of the X and Y registers has been previously described. These registers are 10-bit parallel up/down counters shown in Figure 6-7. Each flip-flop is loaded by a 1's transfer through an inverter gate. A second inverter gate in each flip-flop module applies a pulse to the complement input at each flip-flop every time the COUNT X or COUNT Y pulse occurs if the gate is enabled by a ground potential on its emitter. (The most-significant bit flip-flop in each register has two complement inputs, each of which produce a propagate pulse from a separate propagate output. These propagate pulses are used to produce the X OVERFLOW or Y OVERFLOW pulse, whenever the contents of the register overflows either its minimum or maximum values.) These gates are used to increment the register in the character, increment, vector, or vector continue modes, causing the register to count up or down (according to the direction level present) by an amount determined by the scale register.

Digital-to-Analog Conversion

The O output of each flip-flop is applied to the input of a 1677 Level Amplifier, shown in the lower section of Figure 6-8. This terminal is ground when the flip-flop is in its 1 state, cutting the level amplifier off. The level amplifier is turned on by a -3 volt input when the flip-flop holds a 0.

Each level amplifier acts as an electronic switch, switching its output between two voltage levels. One of these voltage levels is a stable -10 volt reference voltage from the 1562 module in C01, and the other is approximately ground. The output of each level amplifier is applied to the input of a 1568 Digital-to-Analog Converter (located in C02 for the horizontal

axis and in C08 for the vertical axis. The output of the digital-to-analog converter is an analog deflection voltage that varies between ground and -10 volts according to the value of the 10-bit binary number applied to the converter.

Deflection

The analog deflection voltage is applied to the input of a 1575 Follow or Hold module, located in R07 for the horizontal axis and in R17 for the vertical axis. The output voltage of the 1575 follows the input voltage except when a COUNT X pulse occurs, then for 0.3 microsecond the output voltage remains constant. During this time the D-A converter produces transients, and the 1575 prevents these transients from being applied to the deflection amplifiers.

The output of the follow or hold circuit is applied to one input of a differential amplifier in the 1567 Deflection Preamplifier. These are located in R06 for the horizontal axis and in R18 for the vertical axis. The other input of the differential amplifier is a -5 volt reference potential. Each of these signals is added in superposition with a feedback voltage from the deflection amplifier, and applied to one input of the differential amplifier. Assuming the analog input voltage equals the -5 volt reference input, each half of the differential amplifier is balanced and conducts equally, producing two equal outputs which are converted to the current mode and applied to the two halves of the deflection amplifier. These control the conduction of the deflection current through the coils in the deflection yoke. Since the two coils have equal currents in opposite directions, the magnetic fields cancel out and the beam is not deflected. As the analog signal from the follow or hold circuit changes, each half of the differential amplifier changes its conduction proportionately but in opposite directions. The result is that the currents through each deflection coil change inversely by the same amount and deflect the electron beam.

Deflection Speedup

The speedup circuit momentarily increases the amplitude of the analog signal's change so that the current reaches its required value in the deflection coils faster. The increase is accomplished by overdriving either the reference or the analog input voltage with the speedup pulse, and the amount increased is determined by the scale register.

The speedup circuits, shown in the center of Figure 6-8, each consist of two identical sections. The COUNT X pulse, which occurs 1 microsecond before the spot is to be displayed, activates one or two of the 6113 NAND gates in R12, depending upon the direction the spot is to be moved. The gate(s) produces a positive 70-nanosecond pulse that is complemented by an inverter in R13 and triggers a 4604 Pulse Amplifier, producing a 400-nanosecond negative pulse. This pulse turns on one of the two identical sections of the 1579 Feed Forward module, causing the output stage to conduct. The amount this stage conducts depends on its load resistance, which is a function of the three scale levels. These resistances are listed in Table 3-2.

Compensation

When a coordinate address is changed, a voltage step is produced in the analog deflection voltage. Since abrupt changes of current in the deflection coils produce ringing and the spot oscillates, the deflection coils are damped. The amount of damping used is slightly less than critical in order to minimize the deflection setup delay time.

An abrupt voltage change to the deflection preamplifier does not cause an abrupt change in the deflection current due to the large inductance of the deflection coils. Instead, the current changes semilinearly from its previous value to a value close to that desired, as shown in Figure 3-2. Because of the coupling between the focus coil and deflection coils and the hysteresis of the paramagnetic items in close proximity to the coils, the magnetic field does not completely stabilize at its final value. For about 150 microseconds after the change of address a slightly uncertain undershot value exists that is a little less than the required value. Therefore a compensation network, shown between the 1575's and 1567's, is used to introduce some initial overshoot into the change of the analog signal, driving the currents to the required value so that repeated spots will fall in the same place.

The compensation network is a simple RC circuit with a time constant of about 0.1 millisecond that applies a signal to the preamplifier which is initially much greater than required, and which decreases exponentially toward that value. This overshoot causes the magnetic field to approximately reach its required value by the end of the 35-microsecond deflection setup delay. The overshoot is a fixed percentage, while the undershoot varies somewhat depending upon the previous address; therefore the compensation is not exactly complete. However, with proper adjustment of the compensation network, the resulting spot movement is negligible.

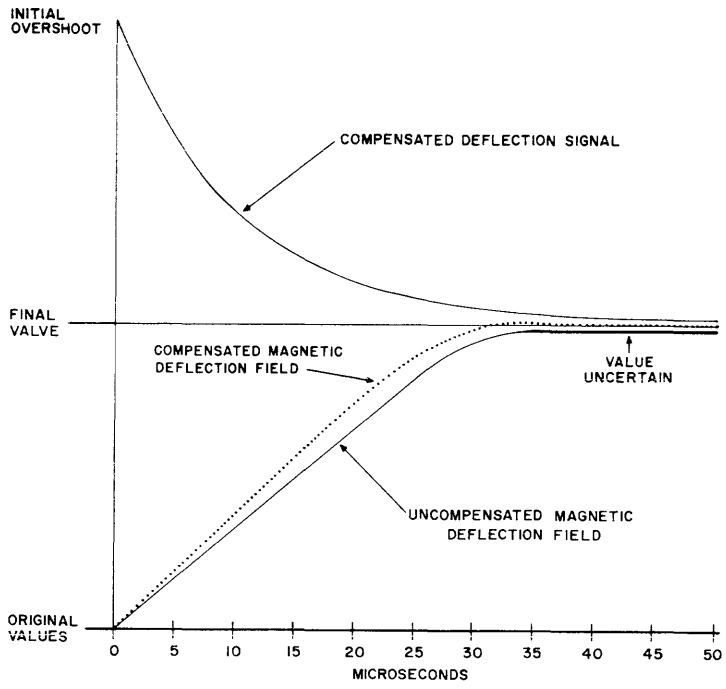


Figure 3-2 Deflection Compensation Characteristics

Repeating

The operation of the display in the increment, vector, and vector continue modes is controlled by a repetitive 1.5-microsecond timing loop. This loop starts with the initiation of the intensify s delay by the LOAD BR pulse. During the 0.5-microsecond operation time of this delay, an INT S level is produced and applied to the intensity gates in the deflection setup and intensify circuit. This produces the INT pulse that is applied to the CRT bias and focus circuit, unblanking the scope and displaying the spot if the intensify bit, BR1, and the move flip-flop are set. (The move flip-flop is located in the move circuit and is only set in the increment, vector, or vector continue modes by the COUNT X pulse, which does not occur until the first intensify s delay operation.)

Spot Intensifying

The intensify s delay circuit consists of the 1304 Delay module in H12, located in the lower left section of Figure 6-4, and the 6102 Inverter and 1609 Pulse Amplifier in the upper right of the delay. The LOAD BR pulse is complemented by the inverter, triggering the pulse amplifier. The pulse amplifier produces a negative 70-nanosecond pulse that is applied to an

inverter in the 1304 module, producing a positive pulse that triggers the delay. During the 0.5-microsecond operating time of the delay, the - 3 volt INT S signal is produced from terminal J and applied to one input of a 6115 NAND gate in H15, located in the lower right of Figure 6-4. If both the BR1 and move flip-flops are set, they each apply - 3 volt enabling signals to this gate, and the output of the gate goes to ground. This turns on the 6102 Inverter in F18 and produces the - 3 volt INT signal.

At the end of the 0.5-microsecond intensify s delay period, an intensify delay pulse (IDP) is produced and applied to the repeat circuit, and is also available as a timing pulse for the character generator. If the display is in the increment (IM), vector (VM), or vector continue modes (VCM), the repeat circuit will produce the COUNT BRM pulse. This pulse is applied to the binary rate multiplier, count circuit, shift circuit, and sequence delay circuit. The sequence delay circuit produces the sequence delay pulse (SDP) 1.0-microsecond after it has been initiated by the COUNT BRM pulse if the halt flip-flop has not been set (shown by the negative input on the block diagram, Figure 6-3). The SDP pulse is applied to the halt circuit, request for data circuit, restart circuit, and escape circuit. Provided the flag circuit has not been activated by an interrupt signal, the restart circuit will produce the RST pulse which is applied back to the intensify s delay, completing the 1.5-microsecond timing loop.

Light Pen Interrupting

If the light pen sees any of the displayed spots while the display is in its repeating cycle, the light pen flag flip-flop will be set, an interrupt signal will be generated, and the cycle will stop. When the computer issues the IOT resume, the display will finish its interrupted cycle. Otherwise the computer must issue the IOT which produces the DPY GO signal to start another display operation. The light pen generally does not respond fast enough to generate a light pen interrupt signal if it only sees the last spot displayed in any vector or increment.

The light pen flag circuit consists of the LP enable, LP find, and LP flag flip-flops, and their associated gates. The LP enable flip-flop is located in the 4218 module in E10 with the three intensity level flip-flops. This flip-flop is set and cleared by the READ TO MODE (RTM) pulse if BR5 is set, as described under Arming The Light Pen Circuit. Both the LP find and LP flag flip-flops, shown in the lower left section of Figure 6-6, are cleared by the INITIATE pulse,

as described under Setup Delay Timing. All three flip-flops are cleared by the RESUME pulse. In addition, the LP flag flip-flop is cleared by the IOT display clear flags, producing the CLR FLAGS pulse.

When the light pen sees a spot of light, the light pen photomultiplier produces an LP SIGNAL that is applied to the light pen gain control circuit. This circuit in turn produces the LP PULSE which is applied to the light pen flag circuit. The light pen gain control circuit is shown in the right center of Figure 6-8. Each time the pen sees a spot of light, it produces a negative signal on terminal B of its output plug. This signal is attenuated by the light pen gain control potentiometer and applied to the base of a 6106 Inverter in R13. This inverter is connected as an emitter follower to buffer the input to a second inverter in the same module.

The output of this second inverter triggers a 4604 Pulse Amplifier in R24, which produces the negative 400-nanosecond LP PULSE.

The LP PULSE is applied to one input of a 6113 NAND gate in H23, shown in the lower left section of Figure 6-6. This gate is enabled when the LP enable flip-flop is set, and its output momentarily grounds the O output terminal of the LP find flip-flop, setting it to 1. When this flip-flop is set, it applies a - 3 volt level in F08 to a 4113 NAND gate which produces a ground enabling potential for two inverter gates. Either the READ TO S or COUNT Y pulse turns on its associated inverter gate, producing a positive pulse output that sets the LP flag flip-flop to 1. This produces the LP FLAG signal which is applied to the X and Y axis circuits, the flag circuit, and the computer or interface (as a program interrupt signal).

The LP FLAG signal prevents the X and Y axis circuits from operating when the IDP pulse occurs. If the light pen interrupted an operation in the point (XYM) mode, the RESUME pulse clears the light pen flip-flops and initiates the sequence delay circuit. The SDP pulse then activates the restart circuit, producing the RST pulse which initiates the intensify s delay and produces a new IDP pulse.

The LP FLAG signal activates the flag circuit, producing the - 3 volt FLAG which is applied to the computer as a program interrupt. This signal disables the restart circuit and prevents the SDP pulse from producing the RST pulse. Again, the RESUME pulse clears the LP flag flip-flop, restoring the flag and restart circuits to their normal conditions.

Vector Generating

When the display is in the vector mode (VM) or vector continue mode (VCM), it calculates the hypotenuse of the right triangle specified by the X and Y component bytes, deflects the CRT beam along this hypotenuse in an approximately straight line, and displays this line if the intensify bit (BR1) is set. In vector mode, the display halts and generates a request for data signal when the vector operation is complete. If the display is in vector continue mode, it continues to calculate and display the vector until the beam violates the edge of the raster. In either mode, when the edge of the raster is violated the display halts and generates program interrupt. In vector continue mode a request for data signal is also generated.

When the vector or vector continue word is loaded into the display, the binary rate multiplier (BRM) is cleared by the CLR BRM pulse. At this time all seven flip-flops in the BRM (BRM0-6) apply - 3 volts to the vector generator. The vector generator produces horizontal (HOR) signal if bit BR3 is a 1, and vertical (VER) signal if bit BR11 is a 1. These signals are applied to two identical direction selector circuits, producing one of two directional levels if the signal is - 3 volts. Which of the two direction levels is produced depends on the direction bit, BR2 or BR10.

Any one of the four direction levels sets the move flip-flop when the COUNT X pulse occurs, producing the MOVE signal. This signal is applied to the deflection setup and intensify circuit, allow succeeding INT S pulses to produce the INT pulses and display the spot if the intensify bit (BR1) is set. The direction levels are also complemented by the direction level inverters and applied to the X and Y registers. Each register uses the two complementary voltage levels of both direction levels to select the gates used for parallel up or down counting. Finally, each speedup circuit receives the two opposing direction levels to select the output used for momentary signal gain.

The binary rate multiplier consists of the seven 1204 Flip-Flops in the upper left of Figure 6-6 and all the associated gates underneath the flip-flops. The BRM is a parallel up counter that counts from 0 to some number between 7 and 127 depending on the number of significant digits in the largest component byte. The counter is incremented every 1.5-microseconds by the COUNT BRM pulse. This pulse is applied directly to the complement input of the least-significant bit flip-flop (BRM6), and through parallel inverter gates and pulse amplifiers to the complement inputs of the more significant bit flip-flops. The 61130 (or 61230) gates in F14

are controlled by two gating circuits, one which samples the states of the BRM to determine which flip-flops are to be complemented, and another which looks at the four most-significant bits of both component bytes to determine to what number the BRM counts.

Parallel Counting

The BRM is cleared initially by the CLR BRM pulse when a word is transferred to the display. After the word is loaded into the buffer register and the initial intensify s delay, the repeat circuit produces the first COUNT BRM pulse. This is a negative 70-nanosecond pulse produced by the 1609 module in H09, shown in the lower left section of Figure 6-4. This pulse complements BRM6 (setting it to its 1 state) but not any of the other BRM flip-flops. (Each of these other flip-flops are only complemented when all of the less-significant flip-flops are in the 1 state when the count pulse occurs.) The left-most 6113 NOR gate in F15 is now activated by BRM6, and applies an enabling -3 volt level to the left-most 61230 Inverter Gate in F14. The next COUNT BRM pulse complements BRM6 back to 0 and also complements BRM5 to its 1 state. This is possible because of the approxiamtely 100-nanosecond delay between the application of the complement input and the change in the outputs of the flip-flops. Since the left-most 6113 NOR gate is now disabled, the third COUNT BRM pulse only compelemnts BRM6. Now both the left-most NOR gate and the NAND gate below and to the right of it are enabled by both BRM5 and BRM6 (thereby enabling the NOR gate directly above it), so the fourth COUNT BRM pulse complements BRM6, BRM5, and BRM4. In this manner each succeeding COUNT BRM pulse increments the binary rate multiplier by one.

When all seven BRM flip-flops are set to the 1 state and the display is in the vector mode, the 4115 NAND gate in F17 (located beneath BRM0) is activated and produces the BRM0-6(1) signal. This signal enables an inverter gate in the halt circuit, shown in the upper right of Figure 6-4, allowing the SDP pulse to set the halt flip-flop. This breaks the repeat timing loop after the next COUNT BRM pulse because the 6102 Inverter in H10, located in the lower center of Figure 6-4, is cut off. The last COUNT BRM pulse complements the entire binary rate multiplier (setting it back to zero) and generates the usual COUNT X pulse. The halt flip-flop also turns off the 6102 Inverter in H24, located in the lower right of Figure 6-4, which enables the 6106 Inverter Gate in H18 and allows the COUNT X pulse to produce the request for data (RFD) pulse.

Shortening the Count

The four NAND gates at the left center of Figure 6-6 are used to shorten the BRM count when possible. The left-most 4113 NAND gate checks the most-significant bit (BR3 and BR11) of each component byte. If both of these bits are zeros, indicating no more than six significant bits in either byte, this gate is activated and enables the left-most 6113 NOR Gate in F15. Every COUNT BRM pulse therefore complements both BRM6 and BRM5, effectively shortening the BRM to 6 bits and a count of 63. The next NAND gate, the left-most 4115 gate in F17, checks the next less significant bit in each component byte (BR4 and BR12), as well as the more-significant bits. If all four of these bits are zeros, indicating no more than five significant bits in the larger component byte, the second 6113 NOR Gate in F15 is also enabled. Each COUNT BRM pulse then complements BRM6, BRM5, and BRM4 each time it occurs, effectively shortening the binary rate multiplier to 5 bits with a count of 31. In a similar fashion, each of the other two 4115 NAND gates in F17 checks the next less-significant bit of each complement byte and shortens the binary rate multiplier by one bit if both of these are zeros. The BRM can be shortened to an equivalent of three bits, with a minimum count of seven.

Component Byte Bit Comparing

Each bit of the component byte that is a 1 generates a direction level. The number of times a level is generated depends on the binary weight of the bit. These levels are generated by comparing each bit of the byte with the contents of the binary rate multiplier. When the comparison conditions are met, a horizontal (HOR) and/or vertical (VER) signal is produced and applied to the direction selector, where the specific direction level is produced.

The most-significant bit of each component byte (BR3 and BR11) is compared with the least-significant bit (RBM6) of the binary rate multiplier. Every time BRM6 is a 0, the vector generator produces the VER or HOR levels if bit BR3 or BR11 is a 1, respectively. Therefore, a direction level is produced at every other count of the BRM. When BRM6 is a 1 and BRM5 is a 0, bits BR4 and BR12 of the component bytes are investigated. If these bits are ones, a direction level is produced at every fourth count, interspaced between the possible direction levels of bits BR3 and BR11. Similarly, when BRM6 and BRM5 are ones and BRM4 is a 0, the status of bits BR5 and BR13 is investigated. When these bits are ones, a direction level is produced at

every eighth count, interspaced between the possible direction levels from bits BR4 and BR12. In a similar fashion every component byte bit is investigates when the inversely corresponding bit of the BRM is a 0 and all the less-significant BRM bits are ones. This is shown in Table 3-3.

TABLE 3-3 VECTOR GENERATOR COMPARISONS

Binary Rate Multiplier Contents							Component Byte Bit Compared						
6	5	4	3	2	1	0	3,11	4,12	5,13	6,14	7,15	8,16	9,17
0	0	0	0	0	0	0	X						
1	0	0	0	0	0	0		X					
1	1	0	0	0	0	0			X				
1	1	1	0	0	0	0				X			
1	1	1	1	0	0	0					X		
1	1	1	1	1	0	0						X	
1	1	1	1	1	1	0							X

The vector generator is composed of two identical sections, one for each component byte. These are shown as the vertical column of 4115 NAND Gates in the center of Figure 6-6. Each section contains seven NAND gates, one for each bit of the component byte. The outputs of the seven gates are ORed together because they share a common clamped load resistor. When the three (two for the most-significant component byte bit) inputs of any level is produced; when BR2 is a 1, the down (D) direction level is produced. The right (R) and left (L) direction levels are produced when BR10 is a 0 or a 1, respectively.

Incrementing

When the display is in either the increment or character modes, it moves the spot from point to point one unit at a time by counting the X and Y registers up or down as necessary. Again, each movement requires 1.5-microseconds, with 1.0 microseconds to increment the register and change

the deflection currents and 0.5 microseconds to intensify the spot. The increment mode uses the 1.5-microsecond timing loop described under Repeating, while the character mode requires an external 342 Character Generator to provide the timing pulses and direction levels.

In the increment mode each IDP pulse produces a COUNT BRM pulse every 1.5 microseconds. This pulse is applied to: the count circuit producing the COUNT Y and COUNT X pulses; the shift circuit producing the SHIFT S pulse; and the sequence delay circuit producing the SDP pulse as long as the half flip-flop is 0. The COUNT X and COUNT Y pulses increment the X and Y registers and activate the speedup circuits as described under Vector Generating. The COUNT X pulse sets the move and RFD flip-flops in the same manner as before, but sets the halt flip-flop in a different manner. The COUNT Y pulse also sets the LP flag flip-flop in the same manner as described under Light Pen Interrupting. The SHIFT S pulse shifts the number held by the sequence register one place to the right each time it occurs. In the increment mode the sequence register is used to select one of the four increment bytes and to set the halt flip-flop.

The COUNT BRM pulse is complemented by a 6102 Inverter in H10 and applied to a 4606 Pulse Amplifier in H11, as shown in the lower center of Figure 6-4. These items constitute the shift circuit, producing the negative 400-nanosecond SHIFT S pulse when the PA is triggered. (This pulse amplifier is also activated by the NEXT CHAR pulse when the display is in the character mode and operated by the character generator, and flip-flop S4 in the sequence register is a 0.) The SHIFT S pulse is applied to a pulse inverter in the 4218 Flip-Flop module in E18, shown in the upper right of Figure 6-6. The pulse inverter produces a positive trigger pulse that is applied to the pulse input of all the capacitor-diode gates in the module. This pulse sets S1 to 0 and shifts the current contents of each flip-flop down to the next less-significant flip-flop. This is possible because the output levels from the flip-flops do not change until approximately 100-nanoseconds after a pulse input.

These four flip-flops, and the inverters and gates immediately above and below them constitute the shift register. The flip-flops are initially cleared by the CLR BRM (shown as the CLEAR S) pulse when the increment word is transferred to the display. The READ TO S pulse, which occurs after the setup delay, then presets this register to 1000. This is accomplished by the 4113 NAND Gate in E16 (which is enabled by the IM mode level) when it momentarily grounds the 0 output

of the S1 flip-flop. As long as this flip-flop is set, it cuts off the 6102 Inverter above and to the left of it, producing the - 3 volt S1 signal. The first SHIFT S pulse shifts the 1 in the register to flip-flop S2, which in turn cuts off the left pair of 6102 Inverters in E17 below the flip-flop, producing the S2 level. Similarly, as each of the other flip-flops is set to 1, it cuts off the inverters beneath it, producing the S3 and S4 levels. The S4(0) signal is obtained directly from the 0 output of the S4 flip-flop.

Increment Byte Selecting

One of the four increment bytes is selected in the increment generator by each - 3 volt (S1 through S4) sequence level from the sequence register. The increment generator is composed of the vertical column of 4113 NAND Gates to the left of the sequence register of Figure 6-6. It is divided into four groups of four 2-input NAND gates each, one group for each bit of the byte. One of the inputs of each gate is connected to the buffered output of the buffer register. Those flip-flops in the BR which are set to 1 apply an enabling - 3 volt potential to the gate. The other input is one of the four sequence levels, each of which enables one of the four gates in each section. For example, when the sequence register holds 1000, S1 is - 3 volts and the gates connected to BR2, BR3, BR4, and BR5 are enabled. The outputs of the four gates in the group are ORed together by sharing a common clamped load resistor. When any gate in the group is activated, the output goes to ground, producing the MOVE X signal. This signal is complemented by a 6102 Inverter in E12 and applied to one of the three inputs of each of the two 6115 NAND gates in E13, which constitutes the direction selector.

The second group of four 4113 NAND Gates receives one input from the R/L bits. The ORed outputs of these gates are applied directly to one of the direction selector gates, and are complemented by another 6102 Inverter before being applied to the other direction selector gate. When both the BR flip-flops selected by the sequence register are set, the upper direction selector gate is activated and produces the right (R) direction level. If the move X bit flip-flop is set and the R/L bit flip-flop is not set, the lower direction selector gate is activated, producing the left (L) direction level. When the move X bit flip-flop is not set, neither direction level is produced.

The other half of the increment generator and the other direction selector work in the identical manner to produce the up (U) or down (D) direction levels. These circuits are shown on Figure 6-6 directly below the circuits previously described.

Halting

The third SHIFT S pulse sets flip-flop S4 to 1, producing a -3 volt S4 signal. This is applied to a 4113 NAND gate in F08, located in the upper right of Figure 6-4, producing a ground output when in the increment mode. The fourth COUNT BRM pulse produces a COUNT X pulse approximately 100 nanoseconds before the S4 flip-flop is cleared, activating the 6106 Inverter in H14 and producing a positive pulse that sets the halt flip-flop to 1. This cuts off the 6102 Inverter in H10 (shown in the lower right of Figure 6-4) allowing the next COUNT X pulse to activate the RFD pulse amplifier which sets the RFD flip-flop and produces the RFD ⟶ LT request for data signal.

Character Byte Selecting

The character byte selector gates the 18-bit output of the buffer register, selecting one of the three 6-bit character bytes for presentation to the 342 Character Generator. These bytes are selected by the S2, S3, S4 signals from the sequence register. When the display is in the character mode, the READ TO S pulse sets the sequence register to 0100. This is accomplished by the 4113 NAND Gate in E16 shown in the upper right of Figure 6-6, which momentarily grounds the 0 output of the S2 flip-flop in the sequence register. This flip-flop then produces the S2 signal from the left-most of the lower three 6102 Inverters in E17, enabling the six 4113 NAND Gates in F23. Those bits of the first character byte in the buffer register which are ones activate their associated NAND gates, producing ground logic 1 signals.

When the sequence register holds 0010, the S3 selection level is -3 volts and activates the six 4113 NAND Gates in F24. This selects the second character bits for presentation to the character generator. Similarly, when the sequence register holds 0001, the S4 selection level is -3 volts and activates the 4113 NAND Gates in F25.

When the character generator finishes its operation on a byte, it produces a CG END LEVEL signal that is applied to the restart character circuit. This is the 4606 Pulse Amplifier in H11

shown in the lower left of Figure 6-4. When the display is in the character mode, the transition of this signal from ground to - 3 volts triggers the capacitor-diode gate and activates the pulse amplifier, producing a 400-nanosecond NEXT CHAR pulse. This pulse is applied to the shift circuit, the second 4606 Pulse Amplifier in H11 shown at the lower center of Figure 6-4. As long as flip-flop S4 in the sequence register is a 0, this pulse amplifier is activated and produces the SHIFT S pulse. (Note that when the second character byte operation is finished and the second SHIFT S pulse is produced. S4 is then set to a 1 and prevents a third SHIFT S pulse from being produced at the end of the third character byte operation.)

The NEXT CHAR pulse is also complemented by a 6102 Inverter in H10 which triggers a 1609 Pulse Amplifier in H09 and activates a 6106 Inverter gate in H14 if the S4 flip-flop is a 0. The pulse amplifier produces a negative 70-nanosecond NEXT CHAR pulse that is applied to the 6102 Inverter in H17 shown at the lower right corner of Figure 6-4. As long as flip-flop S4 is a 0, the NEXT CHAR pulse activates the intensify s delay, producing the IDP pulse 0.5 microseconds later. This pulse is used to restart the operation of the character generator. However, when S4 is a 1, the NEXT CHAR pulse activates the RFD pulse amplifier in the request for data circuit, producing the RFD pulse that sets the RFD flip-flop and generates the RFD ⟶ LT request for data signal.

Move Circuit

The move circuit is composed of the 1209 Move Flip-Flop in H16, the 6106 and 6102 Inverters, and the 6115 NOR Gate shown in the upper right of Figure 6-4. This flip-flop is cleared by the CLR BRM pulse every time a word is transferred to the display. When the display is in the increment, vector, or vector continue modes and the spot is going to be moved by incrementing a coordinate register(s), one or two direction levels are produced and activate the NOR gate. This produces a - 3 volt output that disables the clear inverter in H18 and is complemented to enable the set inverter in H16. The COUNT X pulse then sets the move flip-flop to its 1 state. The 1 output of the move flip-flop is applied to one of the three inputs of the 6115 NAND Gate in H15, allowing the INT S signal to produce the INT pulse when the intensify bit (BR1) is set. The effect of the move flip-flop is to prevent the beam from being intensified until after the spot has been moved. If the spot is not moved during any incrementing step (as when drawing a line), the beam is not intensified, preventing two spots from occurring at the same location.

AC Power Control and Distribution

The primary 115 volt, 60 cycle ac power is applied through two filters (FL1 and FL2) in the Type 826 Power Control Panel to circuit breaker CB1, see Figure 6-16. From CB1 it goes through the contacts of relay K1, which must be energized, and through another pair of filters (FL3 and FL4) to five female ac sockets. Three of these sockets provide the ac power for the logic and bias power supplies and the fans, and the others are spares. The ac power for the deflection and ultor voltage power supplies is obtained from two other female ac sockets through the contacts of a second delay, K2, and a third pair of filters (FL5 and FL6).

The power for the coil of K1 is obtained by two methods. When switch S1 is in the LOCAL (up) position, K1 is energized directly from the circuit breaker. When switch S1 is in the REMOTE (down) position, K1 is energized through the contacts of relay K3, which is energized by a -15 volt remote turn on (RTO) signal from the computer.

The ac power for the deflection and ultor voltage power supplies is controlled by relay K2. The circuit for the coil of K2 goes through serial contacts of relays K4 and K1. K4 is energized by a negative voltage at terminal 4 of TB1 as long as the thermoswitch and plenum door interlock switches are closed. If either rear panel door is opened or if the deflection amplifier overheats, K4 opens and removes the deflection and ultor voltages.

SPECIAL MODULE CIRCUIT DESCRIPTIONS

Type 1567 Display Preamplifier

The 1567 Display Preamplifier is used with a special Digital deflection amplifier to control the magnetic deflection of a cathode ray tube along one coordinate axis. Figure 6-13 shows the schematic for this module. The circuit is divided into two symmetrical sections on the left and right sides with a third section across the bottom. It consists of two current amplifiers, Q1 and Q2, and a differential amplifier composed of Q3, Q4, and Q5.

Transistor Q5 functions as a constant current source for the differential amplifier Q4. The base of this transistor is held at a constant negative voltage developed by the voltage divider R14

and R15 between ground and a -10 volt stable reference voltage. The collector-to-emitter current through Q5 is the common mode current for the differential amplifier. This current is a function of the resistance of the variable resistor, R17 (see Figure 4-5).

Both Q3 and Q4 are dual transistors selected for balanced gain in each half. Each half of Q4 acts as a summing amplifier, algebraically adding signals from two or more sources. The resultant of these signals is amplified and applied directly to the bases of the two inverters in Q3. Q3 is a high current gain emitter follower, whose dc output is applied through a 6-diode string of forward-biased diodes to the base of a current amplifier, Q1 or Q2. These transistors are also current gain emitter followers, and their outputs are taken from terminals F and Y and applied to the deflection amplifier.

The 1567 may operate as either a single-input or dual-input preamplifier. This is possible because the input on terminal W is connected internally to a - 5 volt reference potential developed by resistors R1, R2, and R3 between ground and the -10 volt stable reference voltage. When this is the case, the other input on terminal Z is supplied by a digital-to-analog converter with a voltage range from ground to -10 volts and an output impedance of 1000 ohms. Each input to the differential amplifier at terminal W and Z is therefore equal to 2000 ohms. The display amplifier provides negative feedback from six parallel transistors in each half. These are applied through the six 12,000 ohm resistors on either side of Figure 6-13. Their equivalent resistance is 2000 ohms, so the equivalent input resistance to each half of Q4 is 1000 ohms.

Assume that the analog input signal is at - 5 volts, and the reference input on terminal W is also at - 5 volts. Under these conditions, each half of the differential amplifier conducts equally and their outputs are at approximately +10 volts. This is reduced to approximately +4 volts by the diode string, producing two equal outputs on terminals F and Y that are approximately +3.5 volts.

When the analog input signal on terminal Z goes more positive (as it does when the digital value applied to the D-A converter decreases), more current is applied to the base of the transistor shown in the right half up through 4, increasing its conduction and making its collector more negative. This draws more current from the base of the transistor in the right half of Q3, increasing its conduction, and its emitter also goes more negative. Since the current through

Q5 is a constant, the increased current in the transistors shown in the right half of Q3 and Q4 is obtained by decreasing the conduction of the transistors shown in the left half of Q3 and Q4 by an equal amount. Therefore the emitter of the transistor shown in the left half of Q3 goes more positive by the same amount that the other emitter went more negative.

These two voltage changes are immediately transmitted to the bases of Q1 and Q2 by speedup capacitors C3 and C5, and are dc coupled to the same places after the thermo delay of the diode string. This causes Q1 to decrease its conduction and Q2 to increase its conduction by equal amounts. The deflection output amplifier transistors shown in the right half of Figure 6-12 therefore decrease their conduction, while the transistors shown in the left half of Figure 6-12 increase their conduction by the same amount. The resistors shown at the bottom of Figure 6-12 develop feedback voltages that are applied through the 12,000 ohm resistors on the sides of Figure 6-13. The change in the feedback voltage applied to the right half of Figure 6-13 is opposite in polarity to the change of the input signal on terminal Z, therefore these voltages almost cancel out. Due to the 1:1 ratio of the input resistances to the base of Q4, the voltage gain of the preamplifier and output amplifier combination is kept to less than one for maximum stability.

If the analog input voltage on terminal Z had gone negative instead of positive, the operation of the circuit would be the reverse of that previously described. The variable resistor R16 between terminal Z and terminal W controls the overall gain of the differential amplifier by controlling the amount of signal applied to the opposite input of the differential amplifier. The 1567 operates in the same manner if another current-source signal is applied to terminal W.

Type 1575 Follow or Hold Circuit

The 1575 Follower Hold Circuit module is used to momentarily isolate the input of a display preamplifier while the digital-to-analog converter is changing its value. During this time large transients can appear at the output of the D-A converter due to the nonsimultaneous change times of the flip-flops in the register. While the 1575 is isolating the display preamplifier, it maintains the input at the previous value from the D-A converter. This is only done in the increment, vector, or vector continue modes when the currents in the deflection coils must be changed and stabilized within one microsecond.

The 1575 consists essentially of an input PNP emitter follower Q1, a bidirectional transistor switch Q4 and Q5, an output NPN emitter follower Q8, and a transistor gate Q3, shown in Figure 6-14. The analog signal applied through terminal E to the base of Q1 can vary from ground to -10 volts. Since the collector of Q1 is tied to ground and the emitter is supplied by the +10 volts through voltage isolation transistor Q2, the emitter of Q1 will always be slightly more positive than the signal on its base. The base of Q2 is held much more negative than the emitter by the voltage drop across Zener diode D1, assuring that the transistor is constantly turned on. Current therefore flows through R3 and Q2 as determined by the requirements of Q1. The voltage developed across R3 is isolated from the collector of Q2 because this current is never great enough to saturate Q2.

In a similar fashion the NPN emitter follower Q8 produces an output between ground and -10 volts that is slightly more negative than the input on its base. This is possible because the collector of Q8 is at a constant positive voltage obtained from Zener diode D1, and its emitter is returned to -15 volts through voltage isolation transistor Q7. (Q7 is constantly turned on by a -3 volt potential on its base, and the current demanded by Q8 is not great enough to saturate it.)

Q4 and Q5 act as a bidirectional switch, allowing current to flow in either direction when they are turned on. When this is the case, Q1 charges the storage capacitors C5 and C6 as it drives the base of Q8. However, when Q4 and Q5 are cut off, the storage capacitors can only discharge through Q8. Q8 therefore initially continues to produce an output equal to the input at the time Q4 and Q5 were cut off, and this output gradually rises towards ground until Q4 and Q5 are turned on again.

When either Q4 or Q5 is conducting, its base current is returned through a 1000 ohm resistor through Q6 and R8 to -15 volts. Diode D2 prevents the current from going through R4. The base of Q6 is held at -12 volts by R10 and the diode string between it and -15 volts, so Q6 always conducts. However, since Q4 or Q5 cannot supply enough current to saturate Q6, its collector is isolated from the voltage developed across R8.

When a -3 volt signal is applied to the gate input on terminal K, the base of Q3 goes negative and the transistor conducts. This supplies a ground potential from the collector of Q3 through

diode D2 to the base resistors R7 and R8, cutting off Q4 and Q5. The emitter of Q3 is clamped to ground bh D3. Therefore when a ground signal is applied to the gate input on terminal K, Q3 is cutoff by a positive 1 volt level, turning on Q4 and Q5.

Type 1579 Feed Forward

The 1579 Feed Forward is used to momentarily increase the signal applied to a 1567 Display Preamplifier, causing the deflection currents to be quickly changed and stabilized at a new value. This is accomplished by drawing a fixed current from one of the two preamplifier inputs. Which input the current is drawn from depends on which circuit is activated, and the amount of current drawn depends on the gain control for this circuit and the effective load resistance of this circuit. The effective load resistance in turn is dependent on which of three inverters are on and which are off.

The 1579 Feed Forward shown in Figure 6-15 is divided into three portions: two identical gated variable current sinks (shown in the upper left and lower left), and a load resistance selector (shown in the upper right and center). Each gated variable current sink consists of a PNP inverter gate and an NPN emitter follower. When the inverter gate, Q1, or Q2, is cut off by a ground input signal, its collector is clamped at the -10 volt stable reference potential by diode D1 or D2. This produces a negative potential between -13.5 and -15 volts on the base of an NPN emitter follower, Q3 or Q4, depending on the setting of a variable resistor, R7 or R9. The collector of the emitter follower is connected to a source that can vary between ground and -10 volts, and the emitter is connected to -15 volts through one or more resistors. Therefore, the emitter draws a small amount of current. This current is dependent on the emitter potential (slightly less than the base potential) and the effective load resistance, which is 18,000 ohms in parallel with some combination of the three resistors shown to the right.

A - 3 volt input signal turns gate Q1 or Q2 on, and its collector goes to ground. This produces a more positive voltage on the base and the emitter follower (-10.5v to -15 volts, depending on the setting of the variable resistor), increasing the conduction through the transistor until the emitter voltage is just slightly less than the base voltage. This increased current is drawn from the preamplifier input, effectively increasing the signal applied to the preamplifier.

The load resistance selector consists of three inverters (Q5, Q6, and Q7), each of which controls a pair of load resistors. Eight different values of load resistance can be selected depending on the octal value of the input signals to terminals J, K, and L. When an input is at -3 volts, the associated transistor conducts and its collector goes to ground. The conduction path is through the resistor directly below the transistor and through the pair of diodes and resistors to -15 volts. The potential developed at the junction between the two diodes and the resistor is much greater that on the emitter of the NPN emitter follower, so this pair of resistors are removed from the parallel load resistance of the emitter followers. However, when a ground signal is applied to terminals J, K, or L, the transistor is cutoff and the collector goes to -15 volts. The pair of resistors are now effectively placed in parallel with the 18,000 ohm resistor of the emitter followers.

SECTION 4

MAINTENANCE

Maintenance of the Type 340 consists of procedures repeated periodically as preventive maintenance and tasks performed as corrective maintenance in the event of equipment malfunction. Maintenance activities require use of the equipment listed in Table 4-1, or equivalent, as well as the use of standard hand tools, cleansers, and test cables and probes. Substitution for specified items requires identical or superior parameters.

TABLE 4-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Designation
Potentiometric Voltmeter	John Fluke	Model 801H
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Hewlett-Packard	Model 175A
Voltage Probe	Hewlett-Packard	Model 10003A
Clip-on Current Probe	Hewlett-Packard	Model 1110A
Current Probe Amplifier	Hewlett-Packard	Model 1111A
High-Gain Plug-in	Hewlett-Packard	Model 1752A
Delay Generator	Hewlett-Packard	Model 1781A
System Module Extender*	DEC	Type 1954
System Module Puller*	DEC	Type 1960
Maindec Display Test, 134, 434, 634, or 734**	DEC	F-39-134, F-39-434, F-39-634, or F-39-734
Paint Spray Can*	DEC	DEC Blue 5150-865
Paint Spray Can*	DEC	DEC Gray 3277-1R55
Maindec Display Exercise, LLP	DEC	1-148, 4-52, 06-6342, or 7-51**
Air Filter*	Research Products Corp.	E Z Kleen 2-inch Type MV
Filter-Kote*	Research Products Corp.	By Name

*One is supplied with the computer
**Supplied with the display

The Maindec routines are programs designed to exercise or diagnostically test specific functions within the display. Maindec routines are prepared as a perforated-paper program tape in readin mode format, and are accompanied by a detailed description of the program contained on the tape, procedures for using the program, and information on analyzing the program results, to locate specific circuit failures. Use of these routines is indicated at appropriate points in this manual as they apply to preventive or corrective maintenance.

If it is necessary to remove a module during either preventive or corrective maintenance, the Type 1960 System Module Puller should be used. Turn off all power before extracting or inserting modules. Carefully hook the small flange of the module puller over the center of the module rim, and gently pull the module from the rack. Use a straight even pull to avoid damage to plug connections or twisting of the printed-wiring board. Since the puller does not fasten to the module, grasp the rim of the module to prevent it from falling. Access to controls on the module for use in adjustment, or access to points used in signal tracing can be gained by removing the module, connecting a Type 1954 System Module Extender into the vacated module connector in the mounting panel, and then inserting the module into the extender.

The procedures presented here assume that the reader understands the function of the keys, switches, and indicators on the computer's operator console and is familiar with machine programming as described in the computer's programming handbook.

In addition to the controls and indicators on the operator console and on the Teletype unit, maintenance operations use controls and indicators on component assemblies mounted on the plenum doors of the computer and display. The function of these controls and indicators is described in Table 4-2.

TABLE 4-2 MAINTENANCE CONTROLS AND INDICATORS

Control or Indicator	Function
826 Power Control (located in the display)	
Circuit breaker	Protects the power source from overload due to failure of the display power circuits.

TABLE 4-2 MAINTENANCE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
	826 Power Control (continued)
REMOTE/LOCAL switch	Allows control of the primary power from the back of the machine during maintenance. In the REMOTE position, application and removal of power is controlled by the lock and POWER switches on the computer's operator console. In the LOCAL position the display is energized regardless of the position of operator console switches or door interlocks.
	737 (Marginal-Check) Power Supply (located in the computer)
-15/off/+10 switch	Controls the output of the marginal-check power supply. in the -15 position the output is negative and is connected to the blue connector on each module mounting panel. In the off (center) position the supply is de-energized and the output is disconnected. In the +10 position the output is positive and is connected to the green connector on each module mounting panel.
MARGINAL CHECK voltmeter	Indicates the output voltages of the marginal-check power supply.
Control knob	Controls the amplitude of the marginal-check voltage between 0 and 20 v.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks will forestall possible future failure by discovering progressive deterioration and correcting minor damage at an early stage. Data obtained during the performance of each preventive maintenance task should be recorded in a log book. Analysis of this data will indicate the rate of circuit operation deterioration and provide information to determine when components should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks, which include cleaning and visual inspections; marginal checks, which aggravate border line circuit conditions or intermittent failures so that they can be detected and corrected; and checks of specific circuit elements

such as the power supplies, and bias voltages. All preventive maintenance tasks should be performed as a function of conditions at the installation site. Perform the mechanical checks at least once each month or as often as required to allow efficient functioning of the air filter. All other tasks should be performed on a regular schedule, at the same interval as the computer, determined by the reliability requirements of the system. For a typical application, a schedule of every 600 equipment operating hours or every four months, whichever occur first, is suggested.

> NOTE: Loss of cooling air due to clogged air filters causes over heating and machine failures. Be sure to perform the mechanical checks at least once a month or as often as is required to allow efficient functioning of the air filter.

Mechanical Checks

Assure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard conditions found:

1. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

2. Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filter in soapy water and dry it in an oven or by spraying with compressed gas. Spray the filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin).

3. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC blue tweed paint number 5150-865 or DEC grey enamel number 3277-1R55.

5. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

6. Inspect the following for mechanical security: lamp assemblies, jacks, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.

7. Inspect all module mounting panels to assure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

Power Supply Checks

Check the output voltage and ripple content of the 728 Power Supplies, and assure that they are within the tolerance specified in Table 4-3. Use a multimeter to make the output voltage measurements without disconnecting the load. Use the oscilloscope to measure the peak-to-peak ripple content on dc outputs of the supply. This supply is not adjustable, so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be undertaken.

Check the +50 vdc deflection voltage of the NJE Power Supply* in the same manner as the 728 Power Supplies. This supply is adjustable. If additional information is needed, consult the NJE 60-6 Power Supply Manual supplied with the display.

Check the -135 and +260 vdc CRT bias voltages and 6.3 vac filament voltage outputs of the 770 Power Supply in the same manner as the 728 Power Supplies. DO NOT ATTEMPT TO CHECK THE +10,000 VDC ULTOR VOLTAGE.

WARNING

The 770 Power Supply produces high voltages which can be lethal if contacted. Exercise extreme caution whenever the power is on. Do not place any conduction item within 3 inches of the ultor voltage cable or the CRT tube shield.

* Some displays use a Trygon PHR-60-5S Power Supply instead of the NJE. For those cases, use the Trygon manual supplied with the display.

TABLE 4-3 POWER SUPPLY OUTPUTS

Measurement Terminals at the Power Supply Output	Nominal Output Voltage	Output Voltage Range	Maximum Peak-to-Peak Output Ripple
	Type 728 Power Supply		
Red (+) to Yellow	+10	9.0 to 11.0	0.7 v
Yellow to Blue (-)	-15	14.0 to 16.0	0.7 v
	NJE Power Supply		
8 (+) to 11 (-)	+50	none	1.0 mv
R22V (+) to R22D (gnd)	+260	252 to 268	15.0 v
R22D (gnd) to R22V (-)	-150	145 to 155	0.4 v
Brown wires on standoff terminals of Component Mounting Plate	6.3 ac	5.7 to 6.9	8.0 min 9.7 max
A (+, center) to B (gnd, shield) of Ulter Voltage Cable Socket	+10,000	9,700 to 10,300	150 v

Precision Power Supply Check and Adjustment

The -10 volt output of the 1562 Reference Supply module at location C01 supplies the reference voltage used by the level amplifiers and determines the accuracy of the analog voltage generated by the converter ladder network. A rough check of this adjustment can be made using the oscilloscope. However, an accurate check or adjustment must be made with a high impedance instrument which is accurate to within at least 0.1%, such as the John Fluke potentiometric voltmeter. Adjustment of the supply must be performed within 1 minute due to drifting of the voltmeter. To adjust the supply:

1. Calibrate the potentiometric voltmeter.

2. Connect the potentiometric voltmeter between terminals C01D (ground) and C01E (-10 volts).

3. Turn the screw driver adjustment, accessible through the hole in the handle of the module, until the voltmeter indicates -10 vdc ±40 mv.

Marginal Checks

Marginal checking utilizes the Maindec diagnostic programs to test the functional capabilities of the display with the module operation voltages biased above and below the nominal levels within a specified margin. Biasing the operating voltages aggravates borderline circuit conditions within the modules to produce failures which are detected by the program. When the program detects an error, it usually provides a printout or visual indication which is helpful in locating the source of the fault, and then halts. Therefore, marginal components can be replaced during scheduled preventive maintenance to forestall possible future equipment failure. If no marginal components exist, the operating voltages are biased beyond the specified margins, and the operating voltages at which circuits fail are recorded in the maintenance log. By plotting the bias voltages obtained during each scheduled preventive maintenance operation, progressive deterioration can be observed and expected failure dates can be predicted. In this manner these checks provide a means of planned replacement. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors.

Raising the operating voltage above +10 volts increases the transistor cut-off bias that must be overcome by the previous driving transistor. Therefore low-gain transistors fail. Lowering the bias voltage below +10 volts reduces transistor base bias and noise rejection and thus provides a test to detect high-leakage transistors and simulates high temperature conditions (to check for thermal run away). Raising and lowering the -15 volt supply increases and decreases the output pulse amplitude of pulse amplifier modules. Since the -15 volt supply is the collector load voltage (which is clamped at -3 volts in most modules), raising and lowering this source would have little effect upon the logic circuits. Therefore, wiring in the display allows marginal checking of the -15 volt supply connected to pulse amplifier modules only.

The +10 volt margin should be about ±5 volts, and the -15 volt margin should be about +3 (-18 v) and -8 (-7 v) volts. It is important that the -15 volt margin not be increased above 18 volts or damage can result within the logic.

The 728 Power Supply produces the normal module operating voltages of +10 vdc and -15 vdc. The 734 or 737 Power Supply in the computer produces an adjustable voltage which is used to check for marginal circuit operations under biased conditions. The output of this supply can

be selected to be positive, disconnected, or negative by means of a -15/off/+10 switch; is adjusted by means of the large knob on the supply; and is indicated on a MARGINAL CHECK voltmeter on the supply. Outputs from both of these supplies are connected to each module mounting panel through a color-coded connector at the right side of each panel, as seen from the module side. The color coding of these connectors is as follows, from top to bottom:

a. Green, +10 vdc marginal-check supply
b. Red, normal +10 vdc supply
c. Black, ground
d. Blue, normal -15 vdc supply
e. Yellow, -15 vdc marginal-check supply

Three single-pole double-throw, normal/marginal switches at the end of each module mounting panel allow selection of either the normal power source or the marginal-check power supply output for distribution to the modules. The top switch selects the +10 volt supply routed to terminal A of all modules in the panel. In the down position the normal fixed +10 volt supply connected to the rear terminal is supplied to the modules, and in the up position the marginal-check voltage supplied to the green terminal is supplied to terminal A of the modules. The center switch performs the same selection as the top switch for connection of a nominal +10 volt level to terminal B of all modules in the panel. The bottom switch selects the -15 volt supply to be routed to terminal C of all pulse amplifier modules in the panel. In the down position the normal 15-volt output of the fixed power supply, received at the blue terminal, is supplied to pulse amplifier modules. In the up position the marginal-check voltage, connected to the yellow terminal, is supplied to terminal C of all pulse amplifier modules.

CAUTION

Be sure that the marginal check power is off before turning any marginal check switch on or off. Extensive damage will result if -15 volts is placed on a +10 volt bus.

To perform the marginal voltage checks:

1. Assure that all three normal/marginal-check switches on each module mounting panel are in the down position.

2. Set the -15/off/+10 switch on the marginal-check power supply to the +10 position.

3. Adjust the output of the marginal-check power supply so that the MARGINAL CHECK voltmeter indicates 10 volts.

4. Set the top normal/marginal switch to the up position on the panel to be checked.

5. Start computer operation in a diagnostic program or routine which fully utilizes the circuits in the panel to be tested. If no program is suggested by the normal system application, select an appropriate Maindec program. To completely test the display, all Maindec programs should be performed at elevated and reduced voltages for each terminal (+10A, +10B, and -15C) and for each module mounting panel.

6. Decrease the marginal-check power supply output until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired. Readjust the marginal-check power supply output to the nominal +10 volt level.

7. Restart computer operation. Increase the marginal-check supply output until normal computer operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced. Readjust the marginal-check power supply to the nominal +10 volt level.

8. Return the top normal/marginal switch to the down position.

9. Repeat steps 4 through 8 for the center normal/marginal switch on the mounting panel being checked.

10. Set the -15/off/+10 switch on the marginal-check power supply to the -15 position and adjust the output until the MARGINAL CHECK voltmeter indicates 15 volts.

11. Set the bottom normal/marginal switch to the up position for the panel to be checked, then repeat step 5.

12. Repeat steps 6 and 7, readjusting the marginal-check power supply to the nominal -15 volt level at the end of each step. Return the bottom normal/marginal switch to the down position.

13. Repeat steps 2 through 12 for each module mounting panel to be tested.

14. Turn the marginal-check power supply control knob fully counterclockwise, and set the -15/off/+10 switch to the off position.

CORRECTIVE MAINTENANCE

The Type 340 is constructed of highly reliable transistorized modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment down time due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. No special tools or test equipment are required for corrective maintenance other than a standard multimeter and a broad-bandwidth oscilloscope with a clip-on current probe, current probe amplifier, and a high-gain preamplifier. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the logic drawings, the operation of specific module circuits, and the location of mechanical and electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems. However, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the display.

b. System troubleshooting to locate the fault to within a module through the use of Maindec diagnostic troubleshooting, signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of the malfunction.

e. Validation tests to assure that the fault has been corrected.

f. Log entry to record pertinent data.

Preliminary Investigation

Ascertain all possible information concerning any unusual function of the machine prior to the fault and all possible data about the symptoms given when the fault occurred, such as the program in progress, condition of operator console indicators, etc. Search the maintenance log to determine if this type of fault has occurred before or if there is any cyclic histroy of this kind of fault, and determine how this condition was previously corrected. When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are working properly and that there are no power short circuits by performing the Power Supply Checks as described under Preventive Maintenance. Check the condition of the air filter in the bottom of the cabinet. If this filter becomes clogged, the temperature within the cabinet might rise sufficiently to cause marginal semiconductors to become defective.

System Troubleshooting

Do not attempt to troubleshoot the system without first gathering all information possible concerning the fault, as outlined in the Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to assure that the display, not the computer or program, is actually at fault before continuing with corrective maintenance procedures. Faulty ground connections between the display and the computer are a common source of trouble. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

If the fault has been determined to be within the display but cannot be immediately localized to a specific logic function, it can usually be determined to be within either the deflection circuits or the logical control circuits. Perform the appropriate Maindec diagnostic tests to further localize the fault. When the location of a fault has been narrowed to a single element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation test should be employed to locate the source of the fault.

Signal Tracing

If the fault has been located within a functional logic element, program the computer to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace signal flow through the suspected logic element. The oscilloscope sweep can be synchronized by control signals, which are available on individual module terminals at the wiring side (front) of the equipment. Trace output signals from the interface connector back to the origin, and trace input signals from the connector to the final destination. The signal tracing method can be used to certify signal qualities such as pulse amplitude, duration, rise time, and the correct timing sequence. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

Aggravation Tests

Intermittent faults should be traced through aggravation techniques. Intermittent logic malfunctions are located by the performance of marginal-check procedures as described under Preventive Maintenance.

Intermittent failures caused by poor wiring connections can often be revealed by vibrating modules while running a repetitive test program. Often, the handle of a screw driver passing across the back of a suspect panel of modules is a useful technique. By repeatedly starting the test program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector; check the module connector for wear or misalignment; and check the module wiring for cold solder joints or wiring kinks.

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the down time limitations of equipment use. Where down time must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module, power supply, or standard component which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. Static and dynamic bench tests can then be performed without interfering with system operation. Where down time is not critical, the spare parts list can be reduced and module

2. Remove the module to be checked from the module mounting panel; replace it with the modified extender, and insert the module in the extender.

3. Connect test leads A, B, and C to the appropriate terminals of the color-coded connector at the end of the mounting panel. The module being checked can draw the power from the marginal-check power supply via the green (+10 vdc) or yellow (-15 vdc) terminals, or from the normal power supply via the red (+10 vdc) or blue (-15 vdc) terminals. Note that the marginal check switches at the end of the rack should remain in the down position during the entire procedure.

4. Restore the display power, adjust the marginal-check power supply to provide the nominal voltage output, and start operation of a routine which fully utilizes the module being checked. The procedures and routines suggested in Preventive Maintenance for use in marginal checking the computer can be used as a guide to marginal checking modules.

5. Increase or decrease the output of the marginal-check power supply until the routine stops, indicating module failure. Record each bias voltage at which the module fails. Also record the condition of all indicators when a failure occurs. This information indicates the module input conditions at the time of the failure and is often helpful in tracing the cause of a fault to a particular component part.

CAUTION

Be sure that the marginal check power is off before turning any marginal check switch on or off. Extensive damage will result if -15 volts is placed on a +10 volt bus.

6. Repeat steps 4 and 5 for each of the three bias voltages. If margins of ±5 volts on the ±10 vdc supplies can be obtained, and the -15 vdc supply can be adjusted between -7 volts and -18 volts without module failure, a module can be assumed to be operating satisfactorily. If the module fails before these margins are obtained, use normal signal tracing techniques within the module to locate the source of the fault.

If an external dual-voltage variable power supply is available, such as a DEC 730, perform steps 1 and 2; connect test leads A, B, and C to either the normal power supplies at the red (+10 vdc) and blue (-15 vdc) terminals at the end of the module panel or directly to output at this supply; then continue the procedure from step 4. When using this connector, the ground connections of the dual-voltage supply must be connected to the display signal ground. This connection can be made to the black connector at the end of any module mounting panel.

Static Bench Tests

Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Most catastrophic failures are due to short circuits between the collector and the emitter or are due to an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions, a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connection, and both the emitter and collector are assumed to be the cathode.

Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damaged or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short durations, caused by an intermittent connection, can be detected by connecting a 1.5-volt flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic Bench Tests

Dynamic bench testing of modules can be performed through the use of special equipment. A 922 Test Power Cable and either a 730 or 765 Power Supply can be used to energize a system module. These supplies provide both the +10 vdc and -15 vdc operating supply for the module as well as ground and -3 volt sources which may be used as signal inputs. The signal inputs can be connected to any terminal normally supplied by a logic level by means of eyelets provided on the power cable. Type 911 Patch Cords may be used to make these connections between eyelets on the plug. In this manner logic operations and voltage measurements can be made. When using the 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semiconductor

devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

b. Use a 6-volt soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

c. Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all the leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or greater quality and equal or narrower tolerance.

Validation Test

Following the replacement of any electrical component of the equipment, a test should be performed to assure the correction of the fault condition and to make any adjustments affected by the replacement. This test should be taken from the Preventive Maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor is replaced in a section of the 728 Power Supply, the ripple check for that section should be repeated as specified under Power Supply Checks. If repairs or replacement are made in an area which is not checked during preventive maintenance, Maindecs should be run or an appropriate operational test should be devised. For example, if a flip-flop is repaired or replaced, the register or control function performed by the flip-flop should be completely checked by manual setting and clearing, by improvised programmed exercise of the function, or by performance of the appropriate diagnostic program. If the repairs or replacement affects any adjustment, perform the appropriate steps listed in the adjustment procedures.

When time permits, it is suggested that the entire preventive maintenance task be performed as a validation test. The reasons for this are:

a. If one fault has been detected and corrected, other components may be marginal.

b. While the equipment is down and available, preventive maintenance can be performed and need not be scheduled again for four months (or the normal period).

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.

ASSEMBLY AND DISASSEMBLY

Logic Modules

All logic modules may be easily removed simply by unplugging them from their racks. Access to the modules is gained by opening the rear plenum doors. A Type 1960 System Module Puller should be used when removing any logic module.

NOTE: When removing or inserting a module, be sure all power is turned off.

NOTE: Never interchange modules with different type numbers, or similar type modules which contain jumpers or potentiometers.

Power Supplies

The power supplies are fastened directly to the rack or to a plenum door. To remove or replace any power supply, remove all plugs and/or wires to the power supply (label all wires) and then remove the mounting screws. Reassembly is the reverse of removal.

NOTE: When removing or replacing a power supply, be sure all power is turned off.

Deflection Output Amplifier

The output amplifier heat sink module and the two resistor stack modules in rack S can be removed by unplugging them from the rack. This is accomplished in the following manner:

a. Turn off all power in the display.

b. Remove the 115 vac fan power cables from the side of the cabinet.

c. Tag and remove the thermoswitch wires from the output amplifier heat sink module.

d. Loosen the two screws on the front (wiring side) of the rack which secure the resistor stack modules.

e. Remove the two resistor stack modules.

f. Remove the output amplifier heat sink module.

Cathode Ray Tube

The cathode ray tube (CRT) can be removed and replaced with a minimum of adjustments if the deflection yoke and focus coil alignments are not disturbed. If either one or both of these items are disturbed, the coil alignment procedure must be done after the equipment is reassembled. In removing the CRT, the entire CRT Assembly must be removed first. This job requires two men.

CRT Assembly Removal

The CRT Assembly must be removed from the display's cabinet before the CRT itself can be removed. This is accomplished in the following manner:

a. Turn off all power to the display.

b. Remove the side panel next to the CRT by lifting it up and out.

c. Remove the two screws which fasten the table bars to the cabinet, and slide the table out of the cabinet.

d. Unplug the focus and deflection cables from the Component Mounting Plate (Figure 4-1).

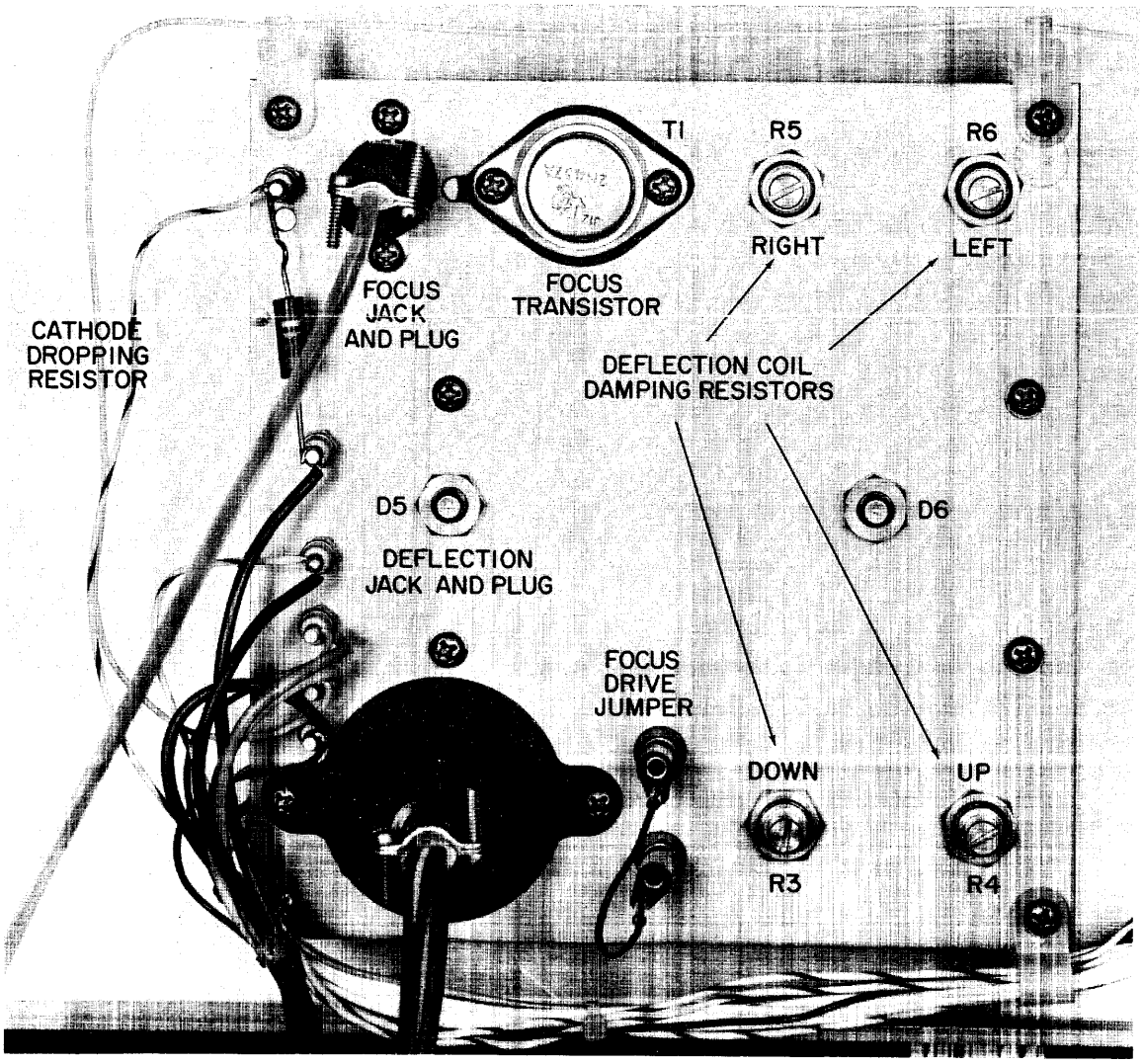


Figure 4-1 Component Mounting Plate

e. Unplug the bias and power cable from the rear of the CRT.

f. Unscrew the bolt in the upper left-hand corner of the assembly casting and remove the ultor cable shield. Temporarily replace the bolt (see Figure 4-2).

g. Loosen the single outside bolt of the upper right tube clamp, and slide the clamp backwards.

h. Slip the ultor voltage cable out of the hole in the insulating jacket, and replace the tube clamp.

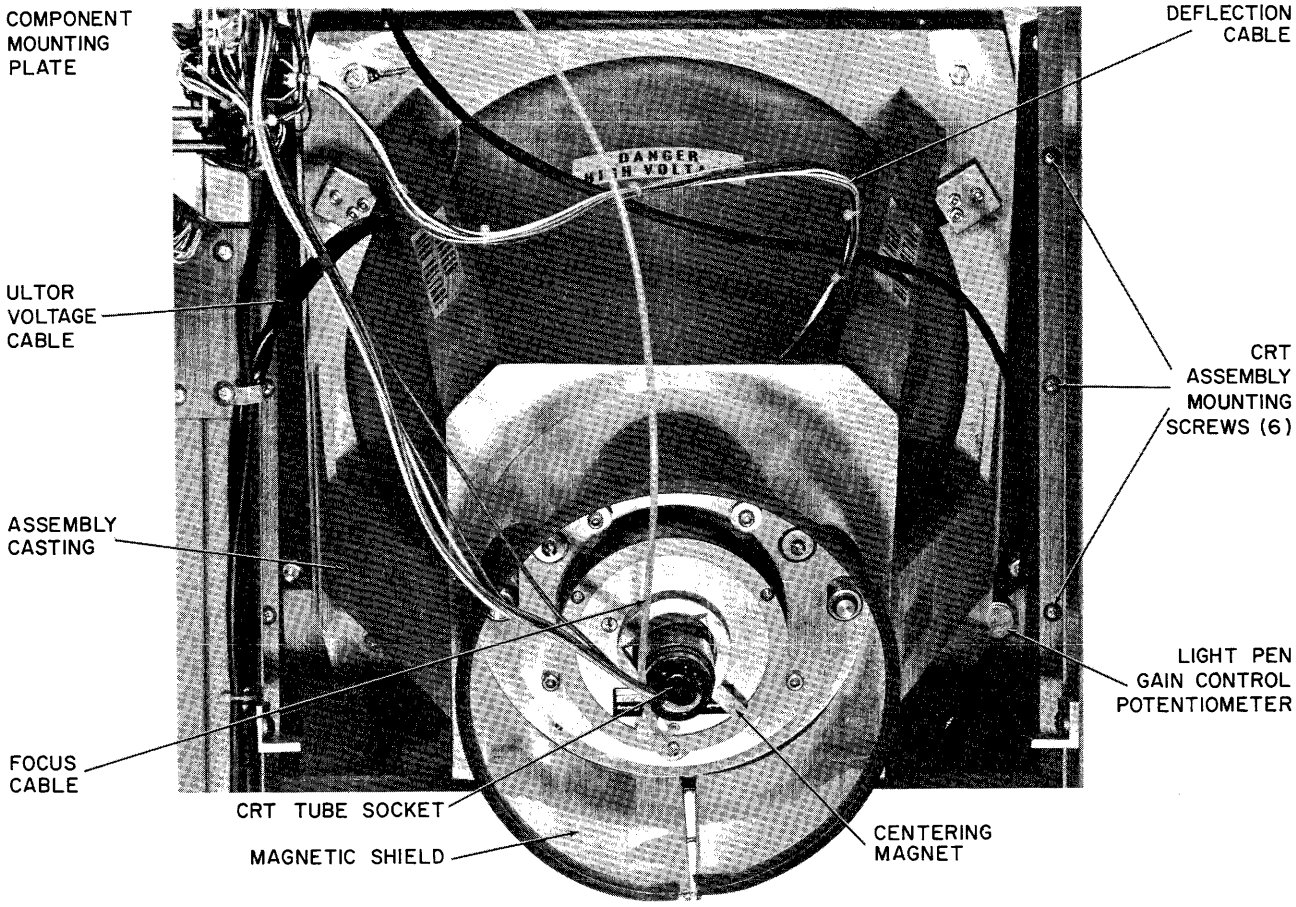


Figure 4-2 CRT Assembly in Cabinet

i. Loosen the set screw in the rear of the Light Pen Gain Control knob. Remove the knob.

j. Unscrew the nut from the gain control potentiometer, and remove the potentiometer.

k. Remove the two lower screws on each side of the cabinet (Figure 4-2) which fasten the CRT Assembly to the main frame.

l. Support the CRT Assembly in both the front and rear, and remove the remaining screw on each side. Carefully slip the CRT Assembly out of the cabinet and place it on a bench.

assembly is disturbed it might change the alignment of either the focus or the deflection coil, and necessitate realignment as described in the coil alignment procedure. To disassemble the coil assembly, proceed as follows:

a. Unscrew and remove the three bolts which spring-load the coil assembly to the casting.

b. Gently slide the assembly off its two guide pins. If the CRT is in the CRT assembly, the centering magnets and the bias and power cable socket must first be removed.

c. Remove the three bolts which hold the focus coil retaining ring to the assembly, and remove the ring. The focus coil can now be removed.

d. Turn the assembly over and unscrew the three clamps which hold the deflection coil in the assembly. The deflection coil can now be removed.

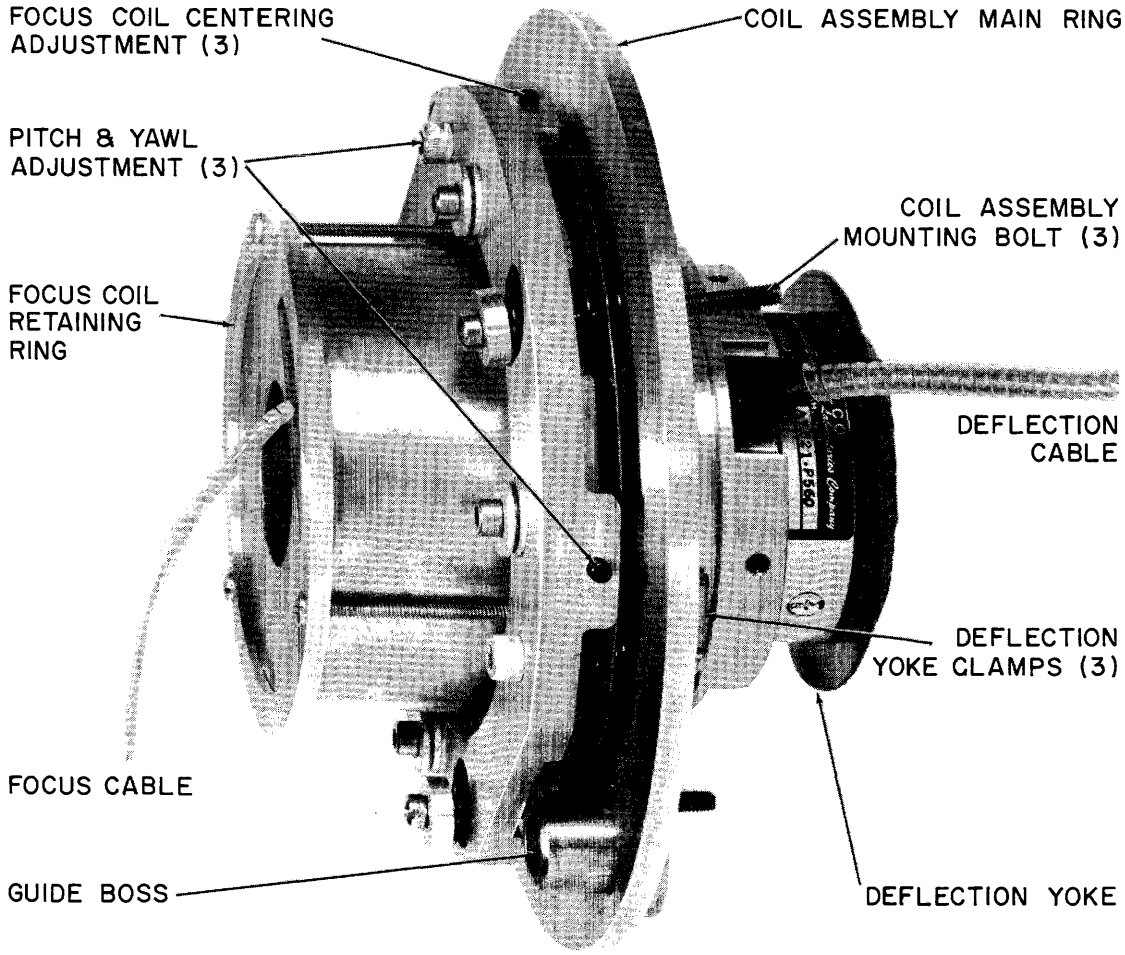


Figure 4-3 Coil Assembly Components

Reassembly is the reverse of the disassembly procedure. After the deflection coil is fastened to the assembly, adjust the three bolts which control the pitch and yaw of the focus coil mounting plate until it is approximately parallel to the deflection coil mounting plate. Then adjust the three set screws in the focus coil mounting plate until the hole in the deflection shield is aligned with the hole through the deflection coil. The focus coil can then be attached and the assembly replaced on the casting.

ADJUSTMENTS

There are no operator controls to be adjusted on the standard 340. If the display has a 370 Light Pen, a gain control potentiometer for the light pen amplifier is located in the lower left corner of the CRT face plate. Clockwise rotation of this knob increases the gain of the amplifier, lowering the light threshold level necessary to activate the light pen circuit.

Centering Magnet Adjustment

Any time the CRT or coil assembly is removed, the centering magnet (Figure 4-2) must be re-adjusted. This is accomplished in the following manner:

a. Turn off all power to the display.

b. Unplug the deflection and focus cables from the component mounting plate (Figure 4-1), and remove the short jumper.

c. Turn the display power back on.

d. Load the LLP Maindec program into the computer and start routine 1 (ADDRESS switches set to 40_8). A large, dim, unfocused spot should appear near the center of the CRT screen.

e. Locate the geometric center of the CRT screen. Adjust the two handles of the centering magnet until the spot is centered at this position.

f. Stop the display, turn off the main power, and replace the jumper and the focus and deflection cable plugs in the component mounting plate.

g. Turn the main power back on.

Coil Adjustment

Whenever the alignment of either the focus or deflection coils has been disturbed or if the CRT has been changed, these coils must be realigned. This is accomplished in the following manner:

a. Perform the centering magnet adjustment procedure through step e.

b. Turn off the main power to the display and plug the focus cable back into the component mounting plate. Leave the jumper and deflection cable out.

c. Connect the output of an audio oscillator or other source of a low frequency, low voltage sinusoidal signal to the two jacks on the component mounting plate.

d. Turn the display power back on, and start routine 1 of the LLP Maindec program (ADDRESS switches set to 40_8). A spot should be seen in the center of the CRT screen that is alternately focused and defocused.

e. Adjust the three set screws around the rim of the focus coil mounting plate (Figure 4-3) until the spot is roughly centered at the geometric center of the CRT screen.

f. Adjust the three pitch control bolts (Figure 4-3) until the focused and defocused spots are concentric.

g. Repeat steps e and f until the spot is centered and perfectly concentric.

CAUTION

Do not apply any force to the neck of the CRT. The focus coil and deflection coil should not touch the CRT.

h. Turn the display power off, disconnect the audio oscillator from the jacks on the component mounting plate, and replace the jumper in the jacks. Plug the deflection cable back into the component mounting plate.

i. Turn the display power back on. A pattern consisting of a center point and a series of squares should be seen. Throw AC switch 0 up and two diagonals will be seen.

j. Loosen the three clamps which hold the deflection coil to the coil assembly, and rotate the coil until the pattern on the CRT raster is aligned in the horizontal and vertical axes.

k. Tighten the three clamps. This completes the mechanical coil alignment procedure. Inspect the pattern on the CRT screen to determine if the focus, raster size, raster position, D-A conversion, intensity, or speedup adjustments must be made.

Focus

The focus of the displayed spot is controlled by a steady current through the focus coil. Because of the tube geometry, the spot cannot be perfectly focused both in the center and at the corners of the raster, so the best compromise is used. The focus current is adjusted as follows:

a. Turn the computer and display power on.

b. Load the LLP Maindec tape into the computer, and display routine 1 (ADDRESS switches set to 40_8) with the diagonal lines. Observe the overall focus of the picture.

c. Adjust potentiometer R5 (bottom rear) in the 1705 module located in R22 for the best focus over the entire raster.

Raster Position

The square raster of the display should be centered in the CRT screen after the centering magnet and focus coil adjustments are made. If it is not, due to unequal deflection centering, it may be moved by the following procedure:

a. Turn the computer and display power on.

b. Load the LLP Maindec program into the computer, and display routine 10 (ADDRESS switches set to 51_8). A square should be seen at the edges of the raster, with either a horizontal or vertical line through the center of the raster.

c. To move the raster along the horizontal (X) axis, adjust potentiometer R2 (center hole, Figure 4-4) in the 1567 module located at R06.

d. To move the raster along the vertical (Y) axis, adjust potentiometer R2 (center hole, Figure 4-4) in the 1567 module located at R18.

Raster Size

The size of the raster on the face of the CRT should be 9-3/8 inches from side-to-side as measured through the center of the raster. The raster size should only be adjusted after the raster has been centered. The raster size is adjusted in the following manner:

a. Turn the display and computer power on.

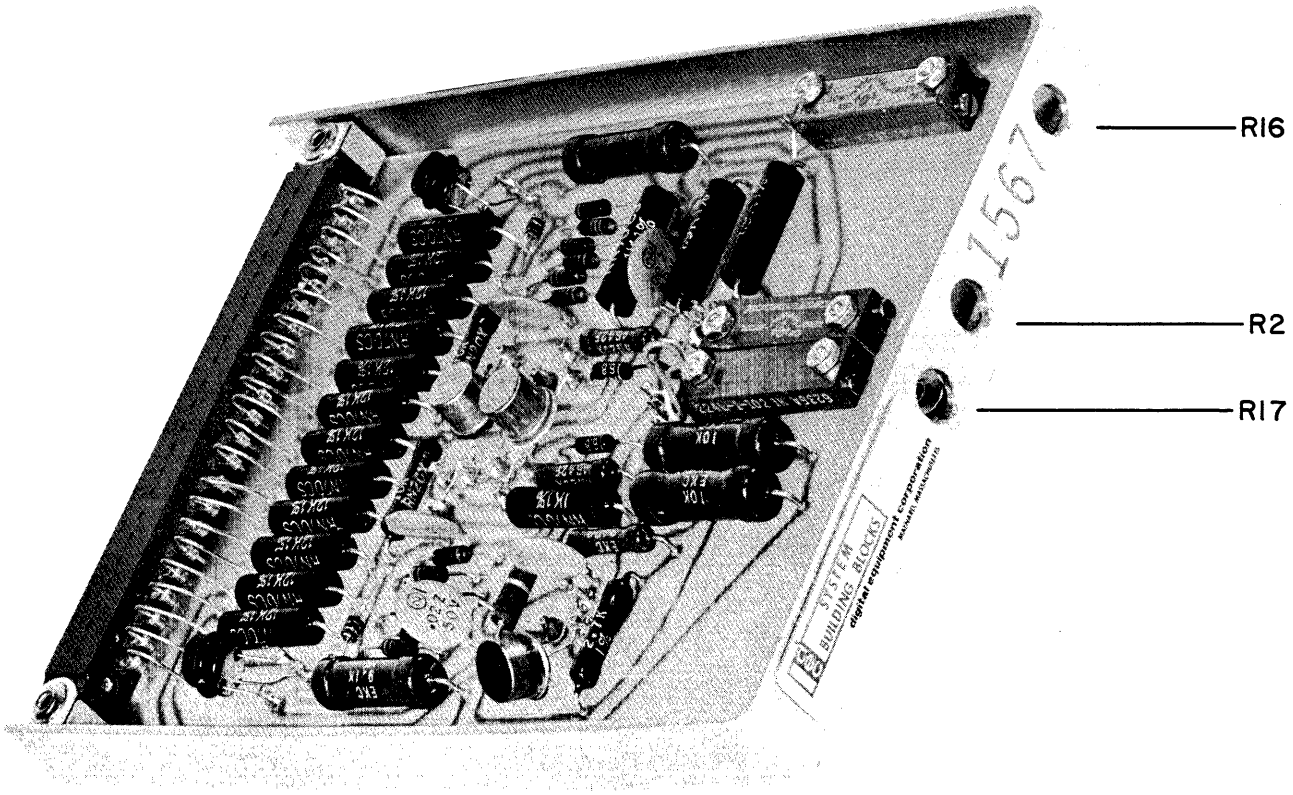


Figure 4-4 Type 1567 Adjustment Locations

b. Load the LLP Maindec programs into the computer, and display routine 10 (ADDRESS switches set to 51_8). A square should be seen around the edge of the raster with either a horizontal or vertical line through the center.

c. Place AC switch 0 up. The vertical line will be displayed. Measure this line.

d. Adjust potentiometer R16 (lower hole, Figure 4-4) in the 1567 module located at R18 until the center vertical line measures 9-3/8 inches.

e. Place AC switch 0 down. The horizontal line will be displayed. Measure this line.

f. Adjust potentiometer R16 (lower hole, Figure 4-4) in the 1567 module located at R06 until the center horizontal line measures 9-3/8 inches.

Common Mode Current

If a 1567 Display Preamplifier module has been changed or repaired or an adjustment of the raster position or size has been made, the common mode current should be checked and adjusted if necessary. The method of checking and adjusting the common mode current in these modules is as follows:

a. Turn the computer and display power on.

b. Load the LLP Maindec program into the computer, and display routine 7 (ADDRESS switches set 46_8). Place AC switches 0 and 1 up and all the others down. The four corner points will be displayed with the two lower points displayed three times as often as the two upper points.

c. Connect an oscilloscope probe to terminal R06Y and measure the two dc voltages seen. These voltages should be approximately +0.5 volts and +6 volts.

d. If the voltage range is greater than this, adjust potentiometer R17 (upper hole, Figure 4-4) in the 1567 module at R06 so that the lower voltage is at least +0.5 volts.

CAUTION

If the upper voltage is too great (approximately +7 volts), the deflection amplifier will overconduct and may be damaged.

e. Place AC switch 1 down. Now the two points on the left will be displayed three times as often as the other two points.

f. Connect the oscilloscope probe to terminal R18Y and repeat steps c and d for the Y axis preamplifier.

Brightness

The relative brightness of all displayed intensity levels is controlled by the cathode-to-grid bias. This bias can be adjusted to vary all the intensity levels as follows:

a. Turn on the computer and display power.

b. Load the LLP Maindec program into the computer and display routine 8 (ADDRESS switches set to 47_8). Eight horizontal lines will be seen on the CRT screen, one at each intensity level.

c. Adjust the bias control potentiometer R3 (lowest hole) of the 1705 module in R22 for the best levels of intensity. The dimmest level should be just visible.

CAUTION

Reducing the cathode-to-grid bias by too great an amount will produce extremely bright spots. These are capable of burning the phosphor coating of the CRT screen, producing holes which cannot display the spot.

Straightness

The horizontal and vertical lines drawn by the display must be straight (except for pincushion distortion) with no waviness or ripple. If they are not, the digital-to-analog converters must

be adjusted. These items must also be adjusted if a 1677 Level Amplifier module or any output transistor in these modules is replaced. The D-A converter is checked and adjusted as follows:

a. Turn on the display and computer power.

b. Load the LLP Maindec program into the computer, and display routine 9 (ADDRESS switches set to 50_8). A straight line will be seen passing through the center of the raster. This line will be horizontal if AC switch 0 is down and vertical if the switch is up.

c. Carefully observe this line for straightness. Every group of four spots should fall on a straight line and the spots in the group should appear straight (a very small misalignment of the spots in the group will occur but should not ordinarily be noticable). If the line is not straight, the 1568 Digital-to-Analog Converter module in that axis must be adjusted.

d. Turn the display power off, remove the 1568 D-A Converter module with a 1960 System Module Puller, insert a 1954 System Module Extender into the vacant location, and plug the 1568 into the 1954. The horizontal D-A converter is located in C02, and the vertical D-A converter is located in C08.

e. Remove the 1567 Deflection Preamplifier in the axis being adjusted. This is located in R06 for the horizontal axis and R18 for the vertical axis.

f. Individually turn off the deflection (770) and ultor (NJE) power supplies located beneath the CRT. The main ac power for the display may now be turned back on.

g. Change the LLP Maindec program in the computer to routine 2 (ADDRESS switches set to 41_8). Set AC switch 1 up if the vertical axis is being adjusted and down if the horizontal axis is being adjusted. All other AC switches should be down.

h. Connect the direct probe from the horizontal input of the oscilloscope to terminal E of the module being adjusted. Set the oscilloscope for 5 mv/cm or greater vertical dc sensitivity and internal sync.

i. Adjust the oscilloscope time base so that two horizontal lines appear on the screen. Measure the voltage difference of these two lines as well as possible and record this value as △1 (see Table 4-4). This voltage should be approximately 10 millivolts.

j. Set AC switch 17 up. Measure the voltage difference of the two new lines and record this value as △2. Add the values of △1 and △2, and

TABLE 4-4 10-BIT DIGITAL-TO-ANALOG CONVERTER ADJUSTMENT

DIGITAL INPUT TO BUFFER										OUTPUT CHANGE (millivolts)
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9	
0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	1 0	△1 ____
0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	1 0	0 1	△2 ____
0 0	0 0	0 0	0 0	0 0	0 0	0 0	1 0	0 1	0 1	△3 ____
0 0	0 0	0 0	0 0	0 0	0 0	1 0	0 1	0 1	0 1	△4 ____
0 0	0 0	0 0	0 0	0 0	1 0	0 1	0 1	0 1	0 1	△5 ____
0 0	0 0	0 0	0 0	1 0	0 1	0 1	0 1	0 1	0 1	△6 ____
0 0	0 0	0 0	1 0	0 1	0 1	0 1	0 1	0 1	0 1	△7 ____
0 0	0 0	1 0	0 1	0 1	0 1	0 1	0 1	0 1	0 1	△8 ____
0 0	1 0	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	△9 ____
0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	△10 ____

$$\frac{\triangle 1 + \triangle 2}{2} = \frac{\qquad\qquad}{2} = \qquad \text{millivolts}$$

divide by two. This is the average value of the two nonadjustable, least-significant bits of the D-A converter. The slight difference between them is caused by the slight differences in tolerances in both the D-A converter and the level amplifier output transistors. If these two values are not close (±1 millivolt), check both circuits for a malfunction.

k. Set AC switches 16 and 17 up, and measure the voltage difference between the two lines. If this voltage is different from the average value of △1 and △2, adjust the bit 7 potentiometer (bottom rear, Figure 4-5) of the D-A converter module. When adjusted, record this value as △3.

l. Repeat step k for the seven other adjustable bits. Do each step in order, setting the next more-significant AC switch up for each step.

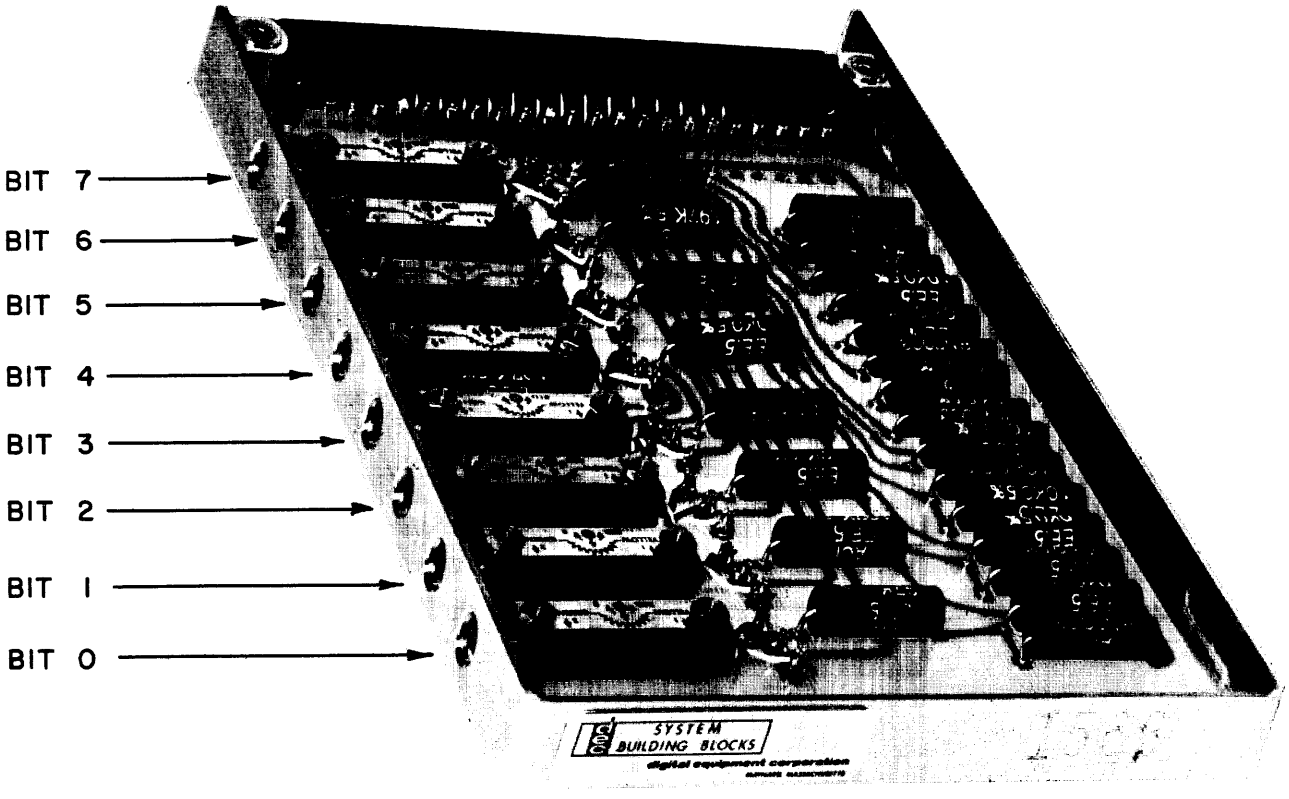


Figure 4-5 Type 1568 Adjustment Locations

NOTE: If any bit cannot be adjusted, especially the more significant bits, it is necessary to assume a slightly different value for the average of $\Delta 1$ and $\Delta 2$; then readjust all the adjustable bits in turn for this value.

Deflection Speedup

The 1.5 microsecond per point display rate in the increment, vector, vector continue, and character modes requires that the signal to the deflection preamplifiers be momentarily much greater than normal in order to establish the new level of current in the deflection coils before the spot is intensified. The amount of signal increase is controlled by the 1579 Feed Forward modules, and may be adjusted for the correct value by the procedure listed below. To insure adequate repeatability, the deflection coil damping resistors must also be adjusted at the same time.

a. Turn the computer and display power on.

b. Load the LLP Maindec program into the computer, and display routine 11 (ADDRESS switches set to 52_8). A square will be drawn on the CRT screen with its lower left corner at the center of the raster. The size of this square is controlled by AC switches 12 and 13; and the intensity is controlled by AC switches 15, 16, and 17.

c. Set the oscilloscope for main sweep delayed, and adjust the sweep delay for 20 microseconds per centimeter. The main sweep time should be set for 0.5 microsecond per centimeter. Start the delayed sweep with the STOP INTER signal from F06X, and trigger the armed main sweep from the output of the speedup delay at R11J.

d. Connect the current probe and current probe amplifier to the input of the high-gain plug-in unit, and set the sensitivity for 0.5 volt per centimeter. Crisscross the red and brown lead-in wires of the vertical deflection coils, and clip the current probe around the wires where they cross.

e. Observe a picture similar to Figure 4-6a on the oscilloscope. (The sweep delay may have to be readjusted slightly to arm the main sweep at a convenient time.) There should be four steps in both the rising and falling portions of the waveshape.

f. Adjust the potentiometer R5 (top hole, Figure 4-7) of the 1579 Feed Forward module in R16 to flatten the last part of each of the 1.5-microsecond rising steps. This is the current through the deflection coils while the spot is being intensified, and it must not vary if the spot is to be motionless. See Figure 4-6b.

g. Adjust the lower right potentiometer on the component mounting plate to eliminate the overshoot or undershoot after the fourth rising step. See Figure 4-6c. This is the damping resistance across the upwards deflection coil.

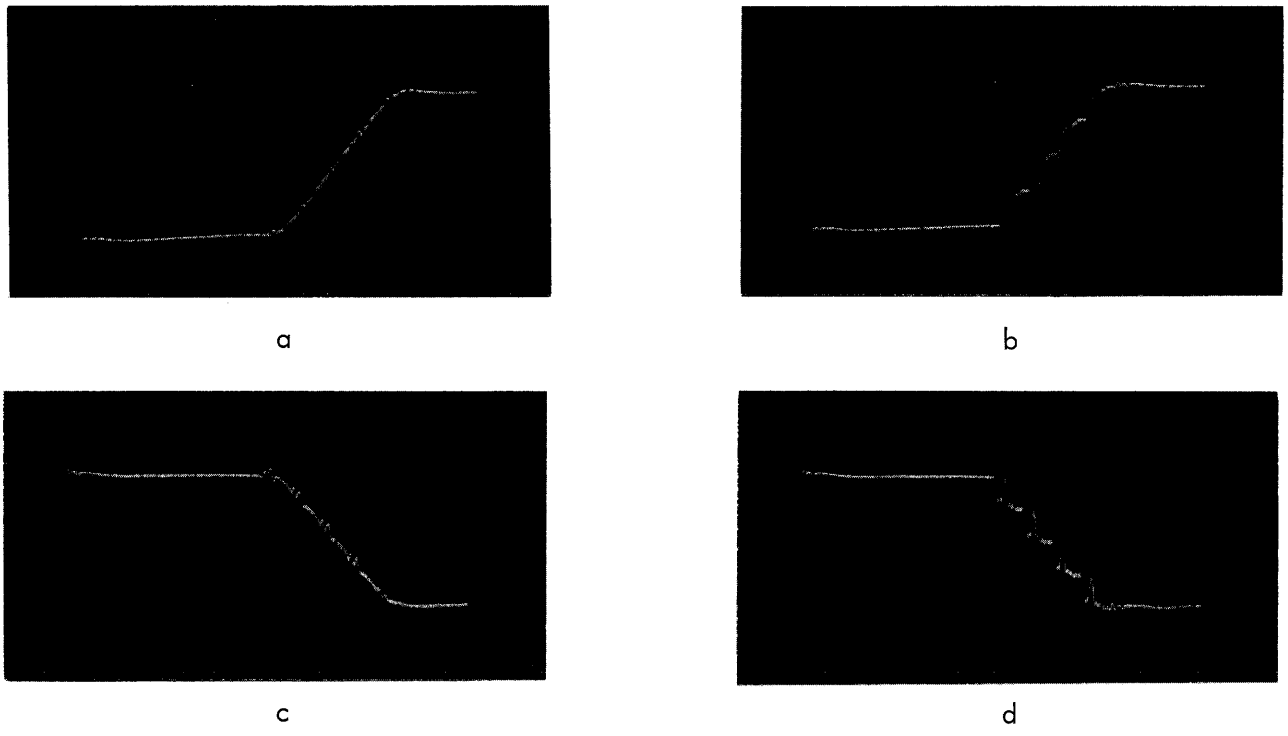


Figure 4-6 Feed Forward Waveform Adjustments

h. Readjust R5 and the damping resistor so that the level part of the fourth step is the same amplitude as the long line of the waveform. This line must be straight and of constant amplitude if the spot is to be capable of repeating itself. See Figure 4-6d.

i. Repeat steps f, g, and h for the four falling steps. R23 (lower hole in the center, Figure 4-7) of the 1579 module in R16 controls the amplitude of the speedup pulse and the lower left potentiometer on the component mounting plate controls the damping of the downwards deflection coil.

j. Remove the current probe from the vertical deflection wires and clip it around the orange and yellow horizontal deflection coils.

k. Repeat steps e through i for the horizontal deflection speedup circuit located in R08. Potentiometer R5 (upper hole, Figure 4-7) in the 1579 module and the upper right potentiometer on the component mounting plate adjust the four rising steps and the right deflection coil. Potentiometer R23 (lower hole in the center, Figure 4-7) in the 1579 module and the upper left potentiometer on the component mounting plate adjust the four falling steps and the left deflection coil.

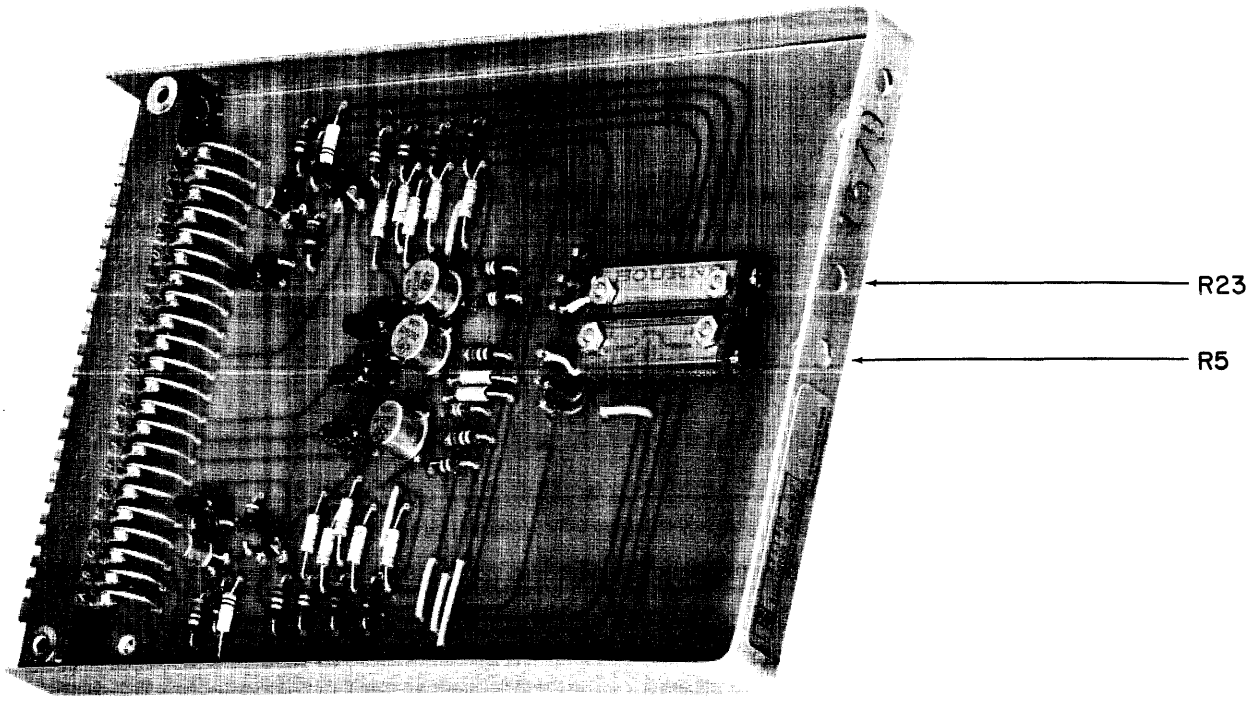


Figure 4-7 Type 1579 Adjustment Locations

Delay Time

The operating time of the various monostable multivibrator delays is adjustable over various ranges by an internal potentiometer. These delays are adjusted at the factory, and should not need readjusting unless the module is changed or repaired. Some of the delays may be set for a different value than that mentioned in Section 3 or shown on the engineering drawing. Be sure you know what the time of the delay should be before adjusting it. The adjustment procedure is as follows:

a. Connect an oscilloscope (set for dc input and negative internal sync) to terminal J of the module to be adjusted.

b. Trigger the delay with the program by connecting a 0.01 microfarad capacitor (which has previously been shorted) between terminal X and ground. A -3 volt level should be observed for the required duration.

c. To change the duration of the delay, adjust potentiometer R7 through the access hole in the back of the module.

d. With the oscilloscope adjusted to be triggered with the delay trigger, connect the probe to terminal E and check for a -3 volt pulse starting at the end of the delay period.

Repeatability

When the display is operating properly, all spots addressed to the same location appear at the same place on the raster regardless of the previous spot location. When this occurs at a rate greater than the eye's response time, the repeated spot location appears as a single dot. If the repeated spot location appears elongated or fuzzy, the compensation network(s) is poorly adjusted or malfunctioning. These circuits may be checked and adjusted by the procedure listed below. Refer to the Compensating description for an explanation of how and why they are used. Note that the two electrolytic capacitors are back-to-back, so that one is functioning properly and the other is short circuited whenever a change in voltage occurs.

a. Turn on the computer and display power.

b. Load the LLP Maindec program into the computer, and display routine 7 (ADDRESS switches set to 46_8) with AC switches 0 and 8 up. Eight points should be observed, one in each corner and two each at the center of both the top and bottom edges. If the compensation networks are correctly adjusted, both the dual spots will appear as a single spot.

c. Place AC switch 1 up. The two dual spots will be combined at the center of the raster (1000, 1000). If the compensation networks are properly adjusted, the quadruple spot will appear as a single spot.

d. Alternate between routine 7 and routine 3 by repeatedly changing the ADDRESS switches between 42_8 and 46_8. The same 5-dot pattern will be observed each time but the intensity of the center spot will vary. Carefully check the center spot to see if it changes size or location. If it does, the comensation networks must be adjusted.

e. If the quadruple spot is elongated or displaced in the X axis, adjust the potentiometer on component board R37 until the quadruple spot is no wider than the single spot.

f. If the quadruple spot is elongated or displaced in the Y axis, adjust the potentiometer on component board R47 until the quadruple spot is no higher than the single spot.

g. Repeat steps d, e, and f if necessary until the quadruple spot is the same size and at the same location as the single spot.

h. After this repeatability adjustment is finished, check the deflection speedup adjustment. These two adjustments interact with each other, and a change in one usually requires readjustment of the other.

SPARE PARTS

The modules listed in Table 4-5 are recommended for spare parts provisioning. Table 4-6 lists all other types of modules used in the display. Repair of these modules, the power supplies, and the deflection amplifier require standard commercially-available components. Parts such as the cathode ray tube, coils, and fans can be ordered directly from the manufacturer.

TABLE 4-5 SPARE PARTS PROVISIONING

Type	Number	Type	Number
1201	2	1677	1
1562	1	1705	1
1567	1	4150	1
1575	1	4220	1
1579	1	4688	1

TABLE 4-6 OTHER MODULES USED IN DISPLAY

Type	Type	Type
1204	4102	4604
1209	4113	4606
1304	4115	6102
1311	4218	6106
1568	4307	6113
1609	4603	6115

SECTION 5

INSTALLATION

SITE REQUIREMENTS

The Type 340 Incremental CRT Display is easy to install at any location which meets the physical and electrical requirements. As long as room is available in the area of the computer installation, these requirements will be met.

Physical Requirements

Space

The 340 occupies two standard Digital vertical cabinets, with an extension and a table attached to the front of the left cabinet (see Figure 1-2). It requires at least an area approximately 42 inches wide by 53 inches deep and 75 inches high to contain the display. In addition, a minimum of 2 feet is needed in front and rear for operation and maintenance. It is recommended that 4 feet of clearance space be available in front, and 3 feet both in the rear and along one side (preferably the left side).

The 340 weighs approximately 700 pounds, and is supported on eight castered rollers and two screw pads (see Figure 1-2). The flooring in the installation area must be capable of supporting this weight as the display is wheeled about.

Environment

The 340 will operate satisfactorily under ordinary conditions of humidity, shock, and vibration throughout a 50° F to 105° F temperature range, at up to 95% relative humidity. However, 70° F to 85° F temperature and 30% to 80% relative humidity ranges are recommended (also best for the operating personnel). The 340 dissipates approximately 1700 watts of power, releasing 5900 BTU per hour. When used in a crowded installation, the room might have to be air conditioned if the total equipment heat dissipation is too great.

Electrical Requirements

The 340 requires two sources of electrical connections, one for power and one for information and control signals. Each source requires one or more cables which enter the equipment through the bottom of the right cabinet (see Figure 1-2).

Power

A separate source of 105- to 125-volt, 60-cycle, single-phase power is required to operate the power supplies in the display. A 20-foot 3-wire cable equipped with a 30-amp Hubbel twistlock plug is provided for connection to the ac power source. On special request, the display can be equipped for 50-cycle and/or 220- to 250-volt power. The power source must maintain its nominal frequency within ±2%.

Interface

All the signals between the computer and the display, with its various options, constitute the interface signals. These are contained in a 25-foot, 50-wire shielded cable with Amphenol 115-114P male connectors at both ends when a PDP-1, PDP-4, or PDP-7 is used; and in four 18-conductor coaxial I/O bus cables when a PDP-6 is used. The latter are cut to length on order, and have Amphenol 1-900-309 female conductors at both ends.

Whether the display is controlled directly by the computer or through some intermediate optional equipment such as the direct access channel, all the interface signals go through the 50-pin jack behind rack F, marked FJ on the engineering drawings, and the 22-pin connector H27. Except for the marginal voltage, remote turn on (RTO) signal, and ground, all the interface signals are standard DEC voltage levels or pulses. Refer to the DEC System Module Catalog C-100 for a description of these. Table 5-1 lists the signals in jack FJ, and Table 5-2 lists the signals in H27.

TABLE 5-1 INTERFACE SIGNALS AT FJ

Wire Color	Connector Terminal	Display Connection	Line Name	Wire Color	Connector Terminal	Display Connection	Line Name
wht	1	H01F	Bit 0	blu	26	E03N	X7(1)
wht	2	H01J	Bit 2	blu	27	E01U	X8(1)
wht	3	H01L	Bit 3	blu	28	E115	Y0(1)
wht	4	H01N	Bit 4	blu	29	E19N	Y1(1)
wht	5	H01R	Bit 5	blu	30	E19T	Y2(1)
wht	6	H01T	Bit 6	blu	31	E19S	Y3(1)
wht	7	H02F	Bit 6	blu	32	E20N	Y4(1)
wht	8	H02J	Bit 7	blu	33	E20M	Y5(1)
wht	9	H02L	Bit 8	blu	34	E20L	Y6(1)
wht	10	H02N	Bit 9	blu	35	E23M	Y7(1)
wht	11	H02R	Bit 10	blu	36	E25U	Y8(1)
wht	12	H02T	Bit 11	blu	37	F12Z*	HEF*
wht	13	H03F	Bit 12	gry	38	H22N	DPY GO
wht	14	H03J	Bit 13	wht	39	F06T	RFD ⟶ LT
wht	15	H03L	Bit 14	gry	40	H07Y	DATA SYNC
wht	16	H03N	Bit 15	wht	41	F00X	STOP INTER
wht	17	H03R	Bit 16	blu	42	H06Z	LP FLAG
wht	18	H03T	Bit 17	gry	43	F06K	RESUME
blu	19	E110	X0(1)	blu	44	E25R	Y9(1)
blu	20	E07N	X1(1)	blu	45	H06P*	VEF*
blu	21	E07T	X2(1)	gry	46	F06Y	CLR FLAGS
blu	22	E04R	X3(1)	blu	47	E01R	X9(1)
blu	23	E06N	X4(1)	red	48	826-5	Marginal Check
blu	24	E03T	X5(1)	red	49	F106	RTO
blu	25	E03S	X6(1)	red	50	Chassis	Ground

*With the PDP-4 and PDP-7, the HEF (37) and VEF (45) signals are not used, but are A ORed to form the CF signal at terminal 45, from connection at H06P.

TABLE 5-2 INTERFACE SIGNALS AT H27

Wire Color	Connector Terminal	Display Connection	Line Name	Wire Color	Connector Terminal	Display Connection	Line Name
wht	A	H21S	IDP	wht	N	F25W	CHAR 4
gry	B	H10P	CG COUNT	wht	P	F25Z	CHAR 5
wht	C	H11K	END LEVEL	gry	R	H10W	RESUME
wht	D	H17E	CM	gry	S	D11Y	CR FROM CG
gry	E	H17Y	ESC FROM CHAR	wht	T	H14J	FLAG
gry	F	H24E	INITIATE	gry	U	D13J	CLR Y
blk	H	Chassis	Ground	wht	V	F18Y	INTENSIFY
wht	J	F25H	CHAR 0	wht	W	H15E	L
wht	K	F25L	CHAR 1	wht	X	H15F	R
wht	L	F25P	CHAR 2	wht	Y	H15H	U
wht	M	F25T	CHAR 3	wht	Z	H15J	D

INSTALLING

The display is shipped as a single unit with the table removed. To install the display, it is necessary to unpack it, assemble the table, connect it to the computer and a source of ac power, and check it out. This is accomplished by the procedure listed below. If the display is to be reshipped, it is recommended that the reverse of this procedure be followed.

a. With a fork-lift truck or similar pallet-handling equipment, place the packed display within a few feet of its installation site.

b. Cut the tape which secures the table to the vertical plank, and remove the table. The protective wrapping on the table can be removed when convenient.

c. Cut the two steel shipping straps which secure the wooden top to the wooden pallet. Remove the straps.

d. Pry the vertical plank off both the wooden top and the pallet. Remove the plank.

e. Lift the form-fitting wooden top off the display, and remove the cellulose matting from beneath it.

f. Remove the fitted plastic bag from around the display. This bag should be saved if the display is to be reshipped.

g. Lift each side panel up and off.

h. From the center of the lower cabinet frame remove the bolt that fastens each side to the wooden pallet. These nuts, bolts, and washers should be saved if the computer is to be reshipped.

i. Tilt the display slightly and slide a wooden batten under the two castered wheels that are lifted. Repeat in the opposite direction for the other pair of wheels. This transfers the support of the display from the frame to the wheels.

j. Place a ramp alongside the pallet, and carefully roll the display off the pallet, down the ramp, and to its installation site.

k. Open the rear doors of each bay, and remove the two bolts which secure each plenum door. These bolts should be placed in the holders provided on the doors.

l. Remove the tape which secures the modules, cables, and light pen (if supplied) to the cabinet. Assure that all modules are securely mounted in their connectors.

m. Remove the two bolts from the table clamps at the rear of the left bay, and slide the arms of the table into the slots of the clamps. Replace the bolts through the holes in the end of the table arms to secure the table.

n. Remove the fan and filter assembly from the bottom of the right bay by disconnecting the captive screw at each side of the filter housing.

o. Slide the two sections of the cable port apart, and pass the cables through the port. It may be necessary to tilt the display slightly to get the connectors under the edge of the cabinet.

p. After the power and signal cables are out, slide the cable port sections together, and replace the fan and filter assembly.

q. Connect the power cable to an ac receptacle and turn on the power. Throw the LOCAL/REMOTE switch on the 826 Power Control panel to the LOCAL (up) position, and perform the power supply checks listed in Section 4. When finished, throw the switch to the REMOTE (down) position.

r. Connect the signal cable(s) to the display jack(s) and to the computer. Turn on the computer and check that the display is also turned on.

s. Remove the protective cover from the CRT and light pen.

t. Load the MAINDEC diagnostic test program into the computer. Perform all the required tests listed in the MAINDEC manual to ascertain correct operation of the display's logic circuits.

u. Perform all the above tests over again, using the marginal voltage of the display. Perform all the tests as many times as necessary to obtain the voltage margins at which each rack in the display fails. Record these margins in the log for later use. Refer to Section 4 of this manual for a description of marginal voltage checking.

v. Load the MAINDEC LLP program into the computer, and perform all the routines listed in the MAINDEC manual. This checks for proper adjustment of the display. If any picture on the CRT does not correspond to its description, perform the adjustment procedures listed in Section 4 of this manual.

SECTION 6

ENGINEERING DRAWINGS

Reduced block schematic engineering drawings are contained in this section as an aid to understanding and maintaining the system. Refer to the Table of Contents for a list of these drawings and the pages on which they appear. A complete set of formal engineering drawings is supplied separately with each system. Should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume the formal drawings to be correct.

Logic Signals

All logic signals are either standard Digital logic levels or standard Digital pulses. A standard Digital logic level is either a ground (0 to -0.3 volts) or -3 volts (-2.5 to -3.5 volts). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (——◇) indicates that the signal is a level and that ground represents assertion; a solid diamond (——◆) indicates that the signal is a level and that -3 volts represents assertion. All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present either 1 or 3 microseconds (depending on the module used) before an input triggering pulse is applied to the gate.

The standard Digital negative pulse is indicated by a solid triangle (——▶) and goes from ground to -2.5 or -3 volts (-2.3 to -3.5 volt tolerances). The standard Digital positive pulse, indicated by an open triangle (——▷), goes either from -3 volts to ground or from ground to +2.5 volts (+2.3 to +3.0 volts). The width of the standard pulses used in this equipment is either 1.0, 0.4, or 0.07 microseconds, depending on the module and application.

Any other signal is non-standard and is indicated by an arrowhead (——➤) pointing in the direction of signal flow. Figure 6-1 shows the standard symbols used in all Digital logic drawings.

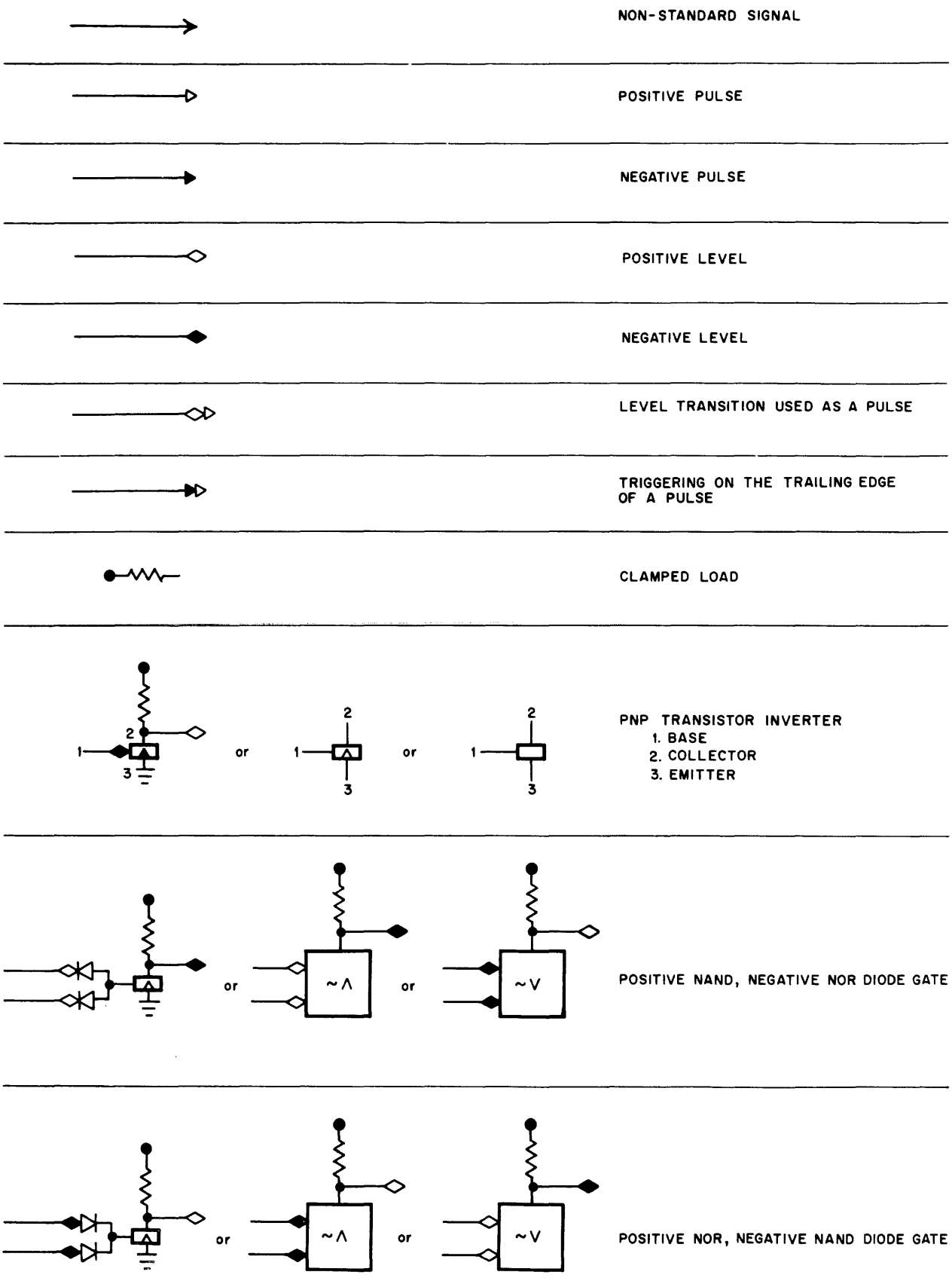
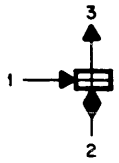
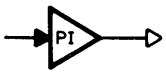


Figure 6-1 Digital Logic Symbols

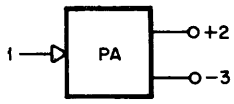


CAPACITOR-DIODE GATE, POSITIVE OR NEGATIVE INDICATED BY POLARITY OF THE INPUTS.

1. PULSE INPUT
2. CONDITIONING LEVEL INPUT
3. PULSE OUTPUT



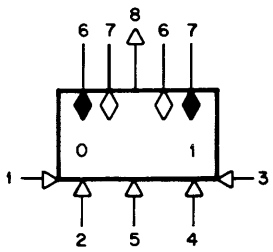
PULSE INVERTER



PULSE AMPLIFIER

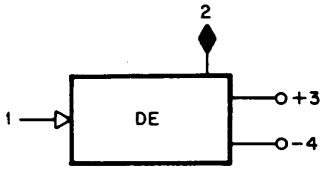
1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL

2,3. TRANSFORMER-COUPLED PULSE OUTPUT



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):

1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1
8. CARRY PULSE OUTPUT

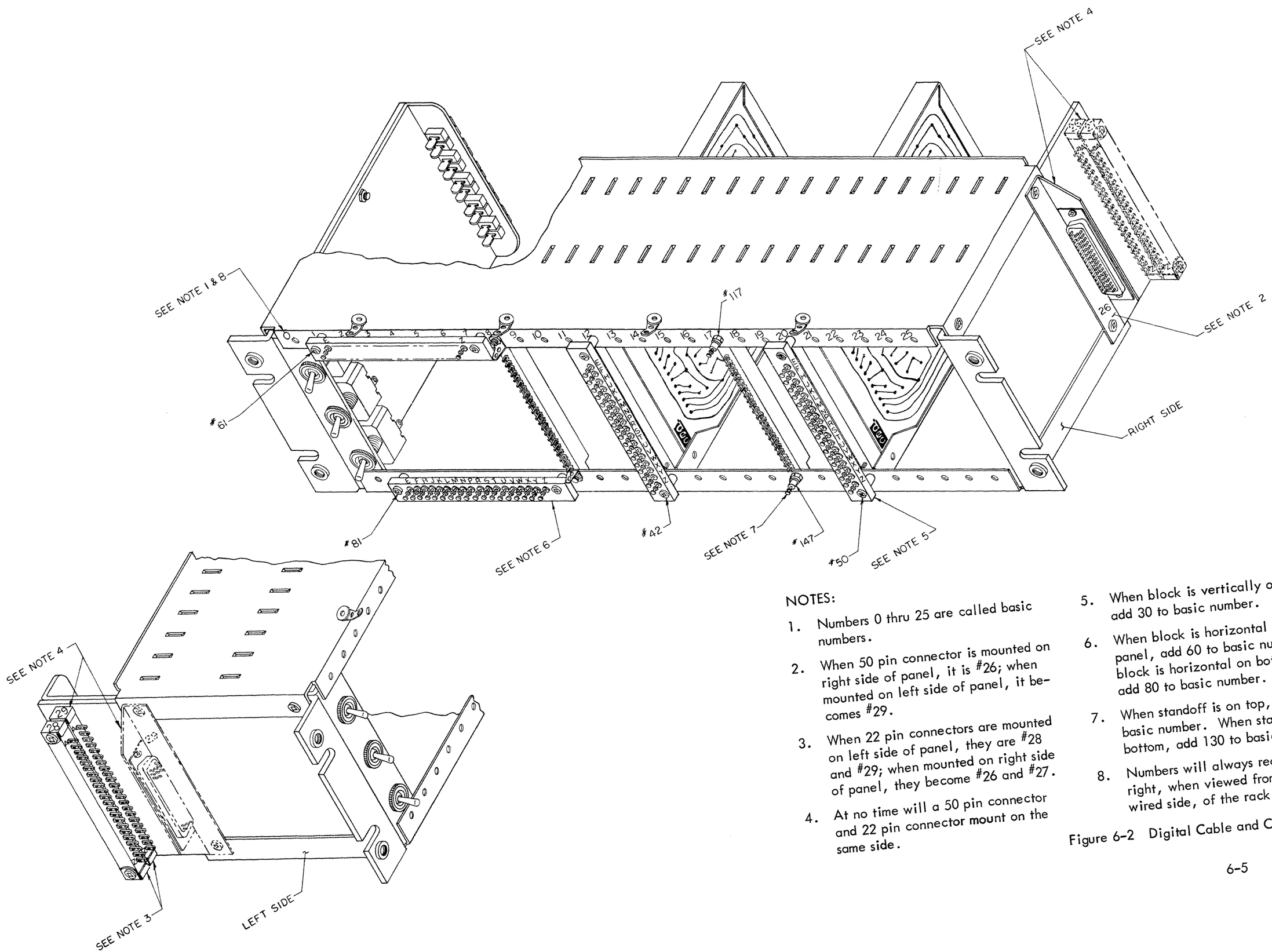


DELAY (ONE-SHOT MULTIVIBRATOR)

1. INPUT PULSE
2. OUTPUT LEVEL, -3V DURING DELAY

3,4. TRANSFORMER-COUPLED PULSE OUTPUT

Figure 6-1 Digital Logic Symbols (continued)



NOTES:

1. Numbers 0 thru 25 are called basic numbers.
2. When 50 pin connector is mounted on right side of panel, it is #26; when mounted on left side of panel, it becomes #29.
3. When 22 pin connectors are mounted on left side of panel, they are #28 and #29; when mounted on right side of panel, they become #26 and #27.
4. At no time will a 50 pin connector and 22 pin connector mount on the same side.
5. When block is vertically over position, add 30 to basic number.
6. When block is horizontal on top of panel, add 60 to basic number. When block is horizontal on bottom of panel, add 80 to basic number.
7. When standoff is on top, add 100 to basic number. When standoff is on the bottom, add 130 to basic number.
8. Numbers will always read from left to right, when viewed from the front, or wired side, of the rack.

Figure 6-2 Digital Cable and Component Numbe

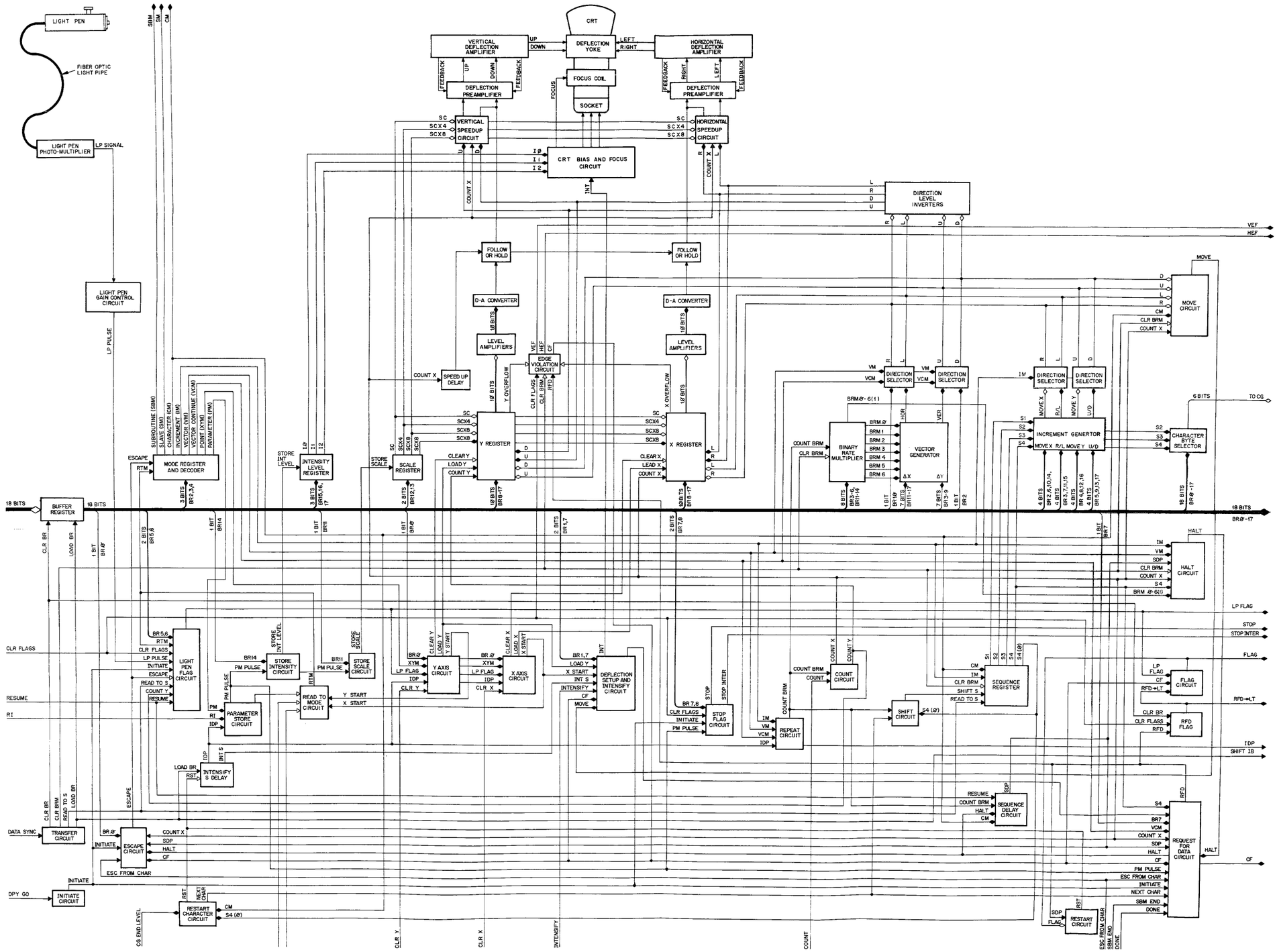


Figure 6-3 Type 340 Block Diagram

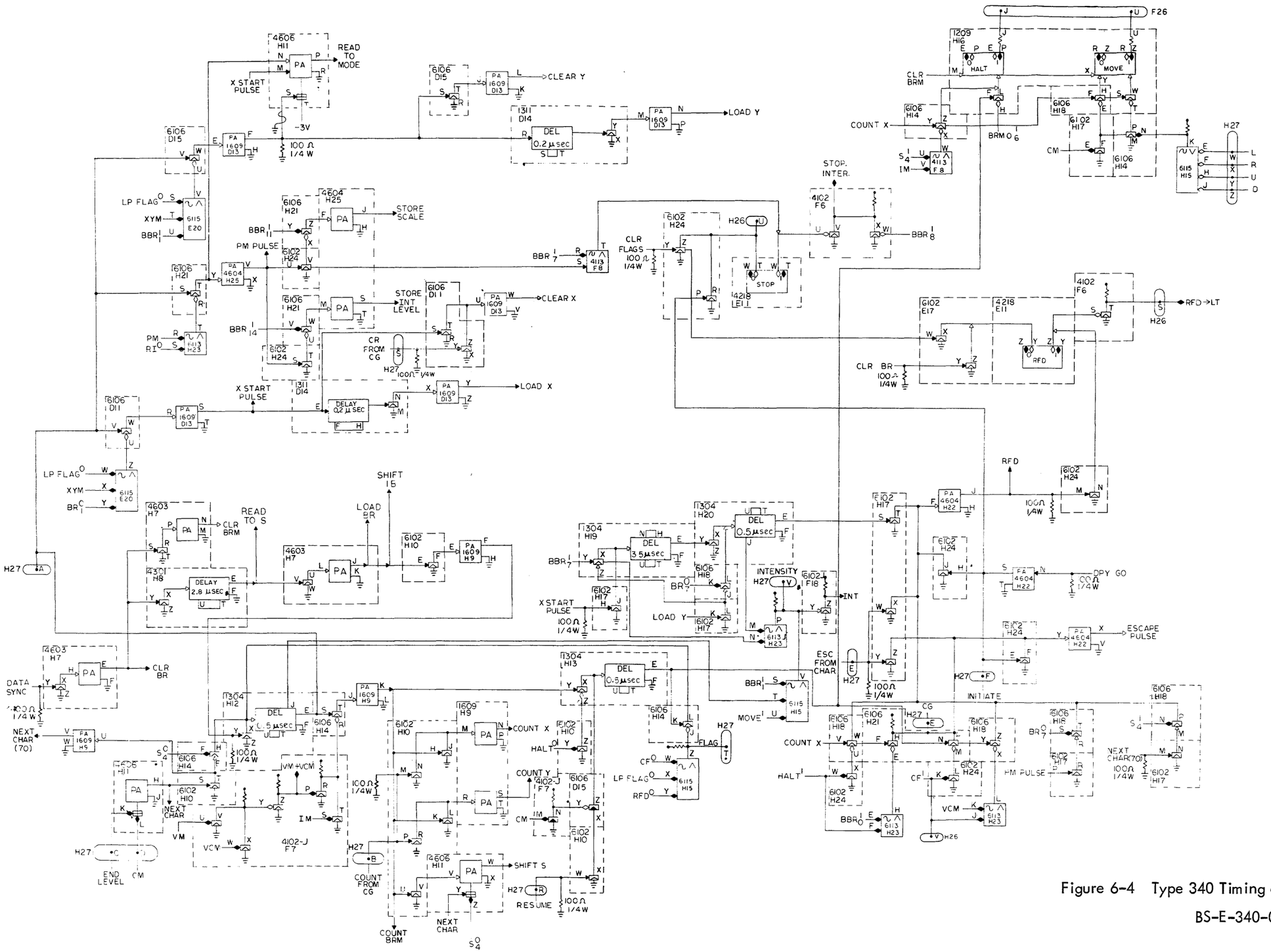


Figure 6-4 Type 340 Timing and Pulse Control Logic

BS-E-340-0-31

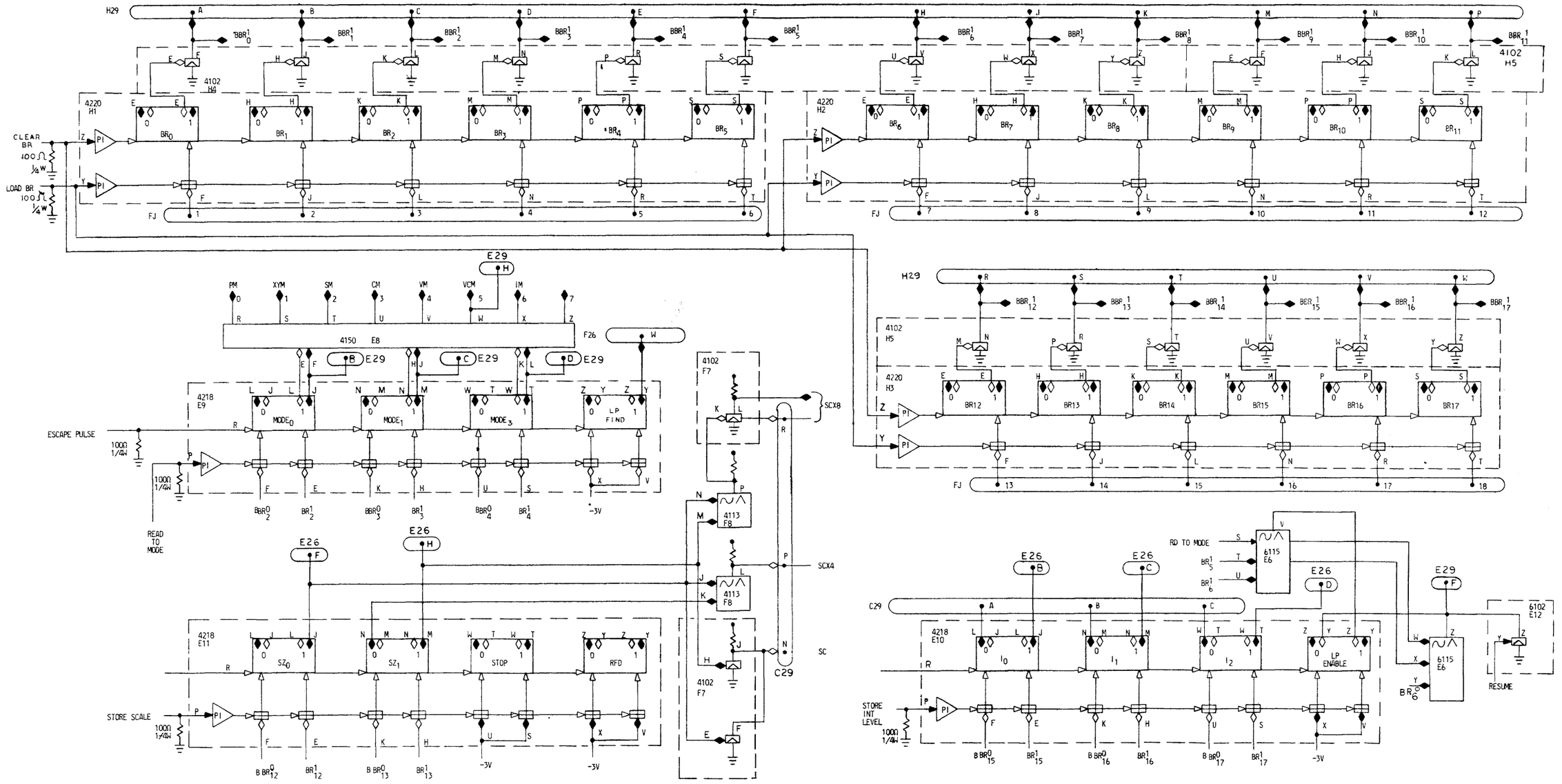


Figure 6-5 Type 340 Input Register and Parameter Store Logic

BS-D-340-0-28

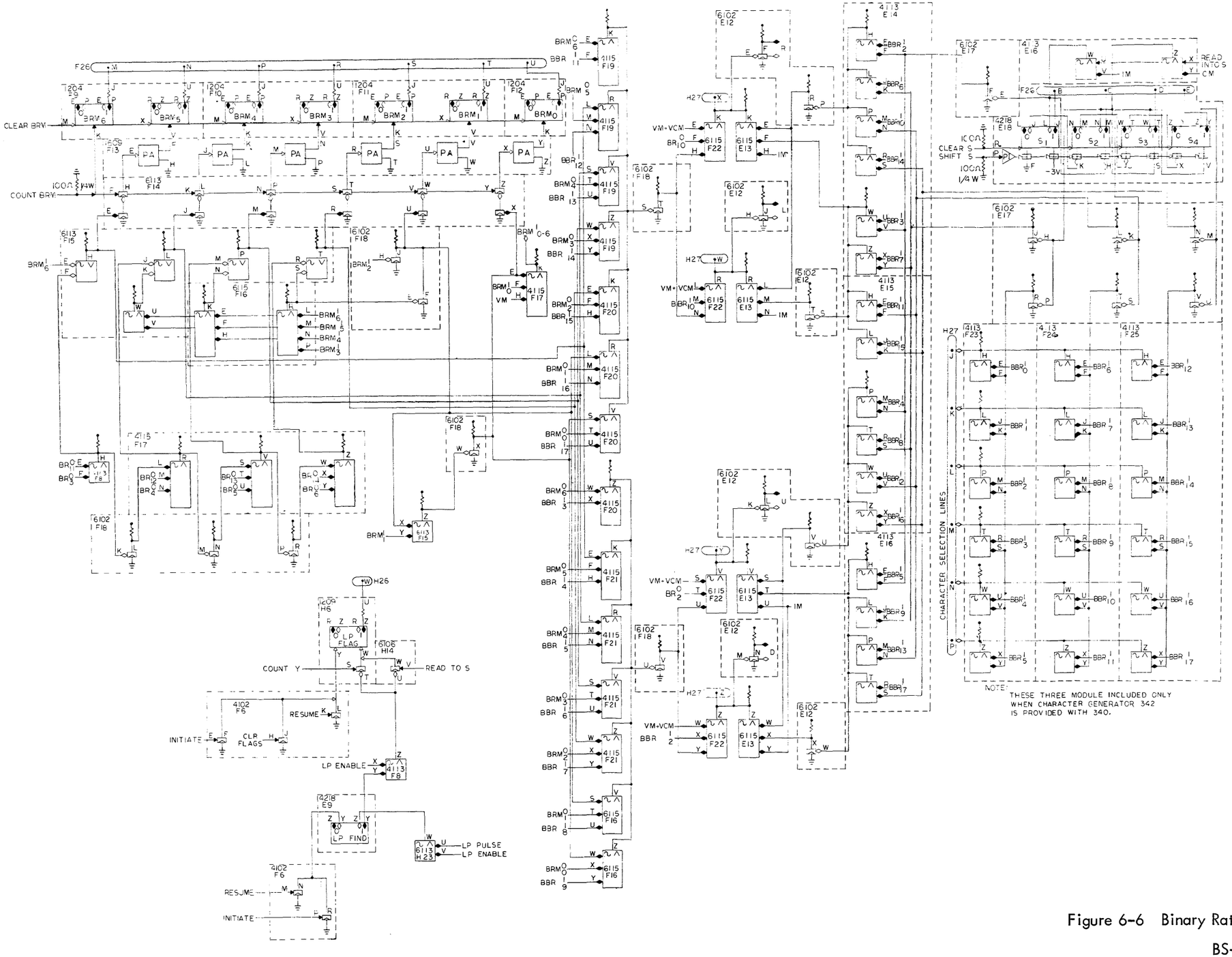


Figure 6-6 Binary Rate Multiplier and Increment Logic

BS-E-340-0-29

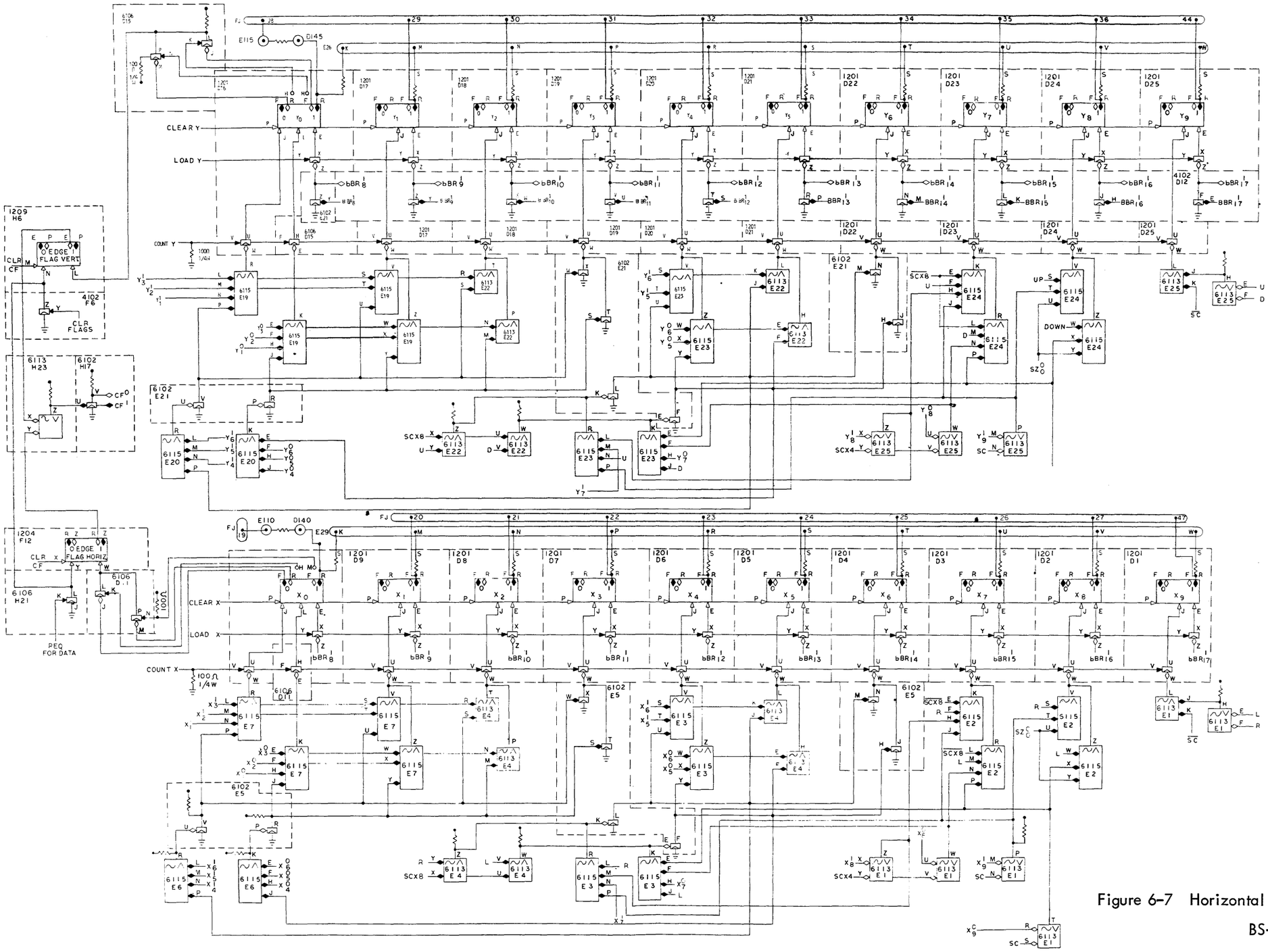


Figure 6-7 Horizontal and Vertical Deflection Registers

BS-E-340-0-30

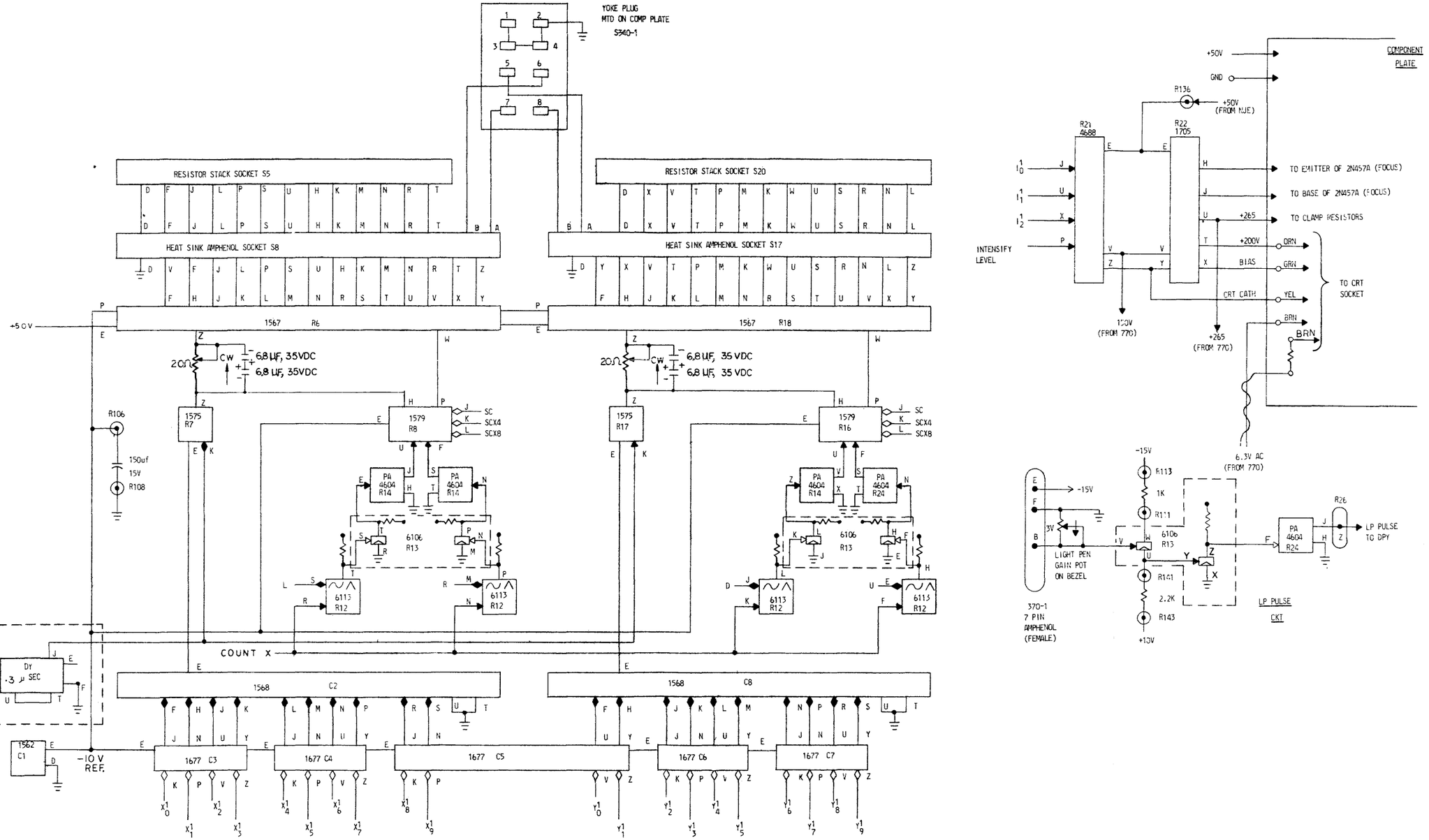


Figure 6-8 Type 340 Deflection Logic
BS-D-340-0-27

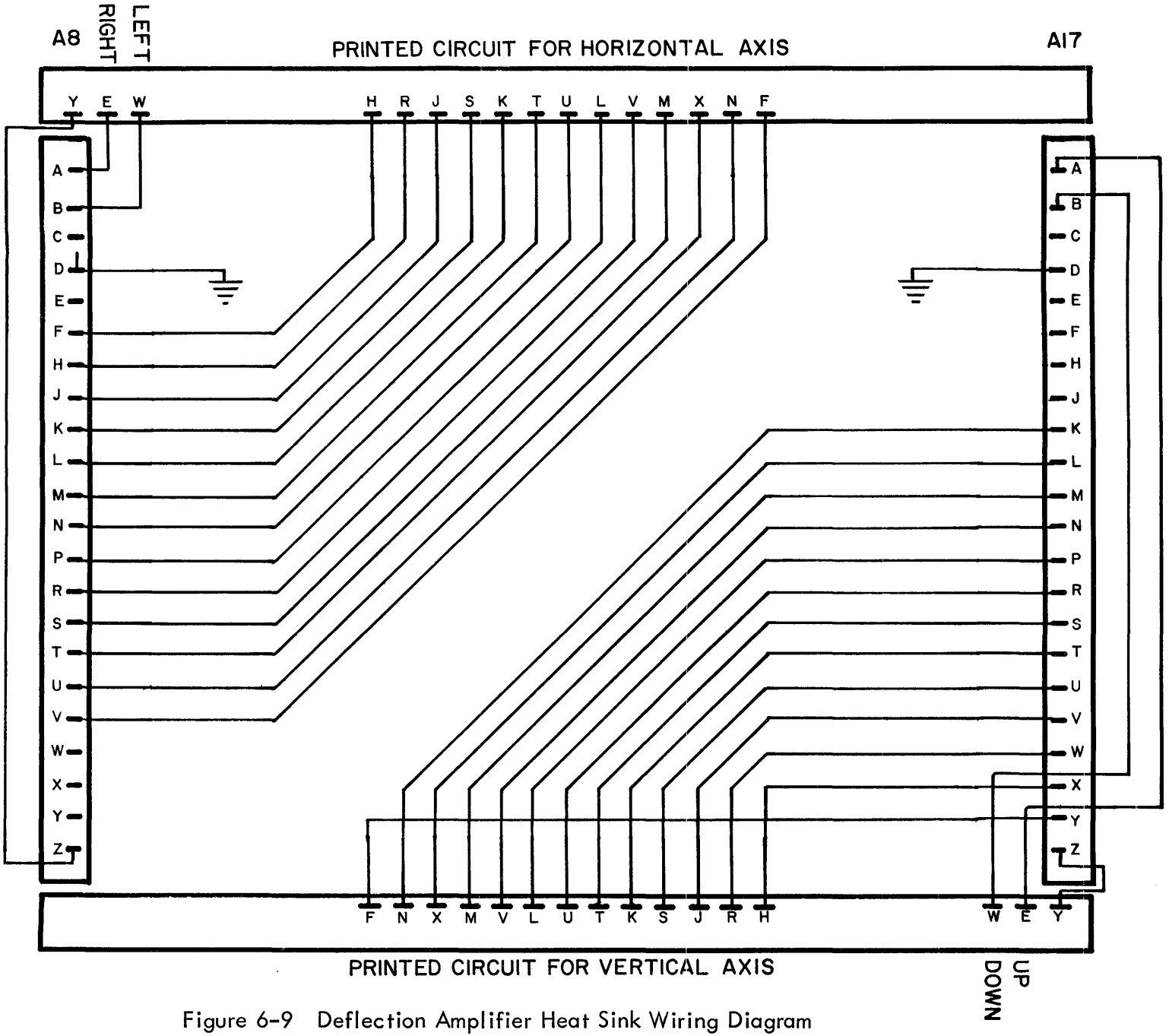
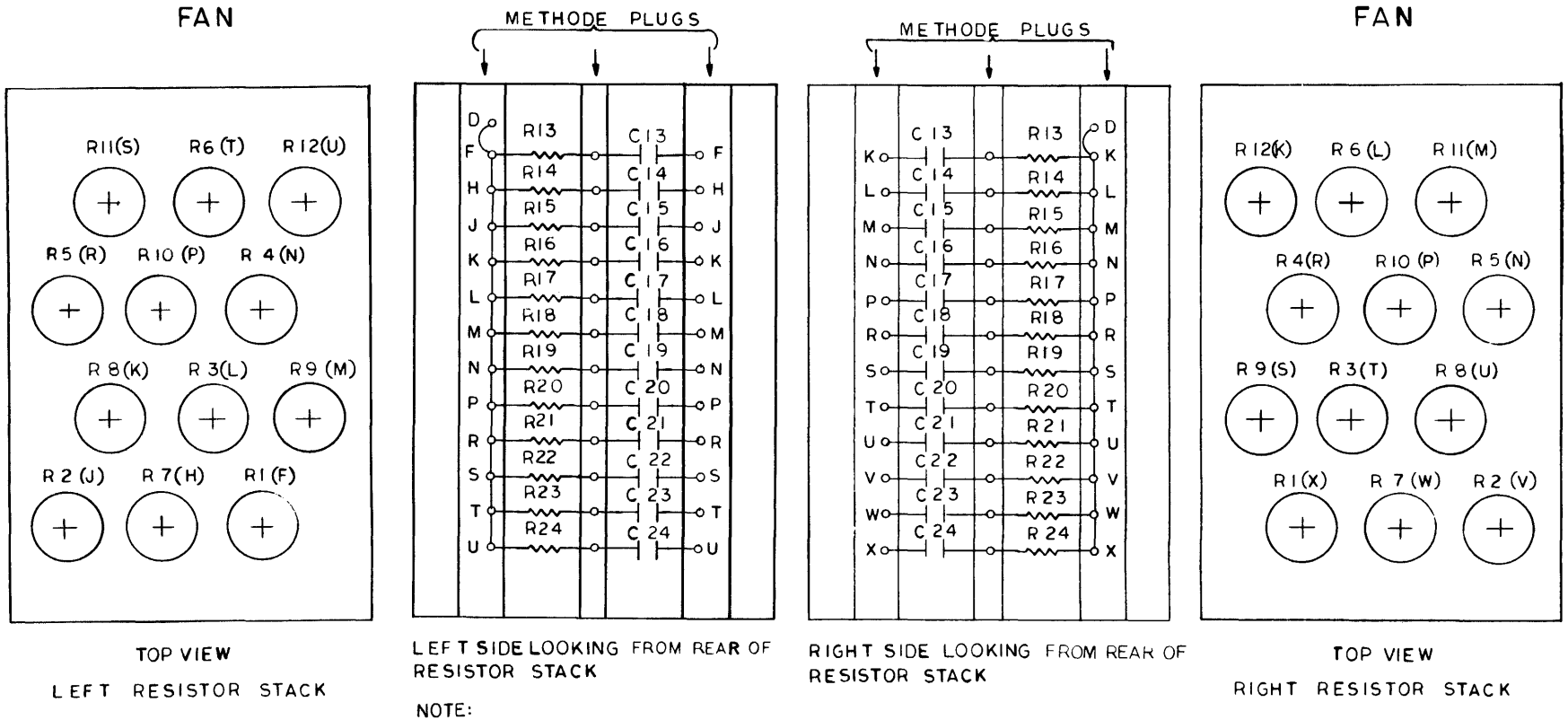


Figure 6-9 Deflection Amplifier Heat Sink Wiring Diagram

WD-B-22106

DEFLECTION AMPLIFIER HEAT SINK WIRING DIAGRAM



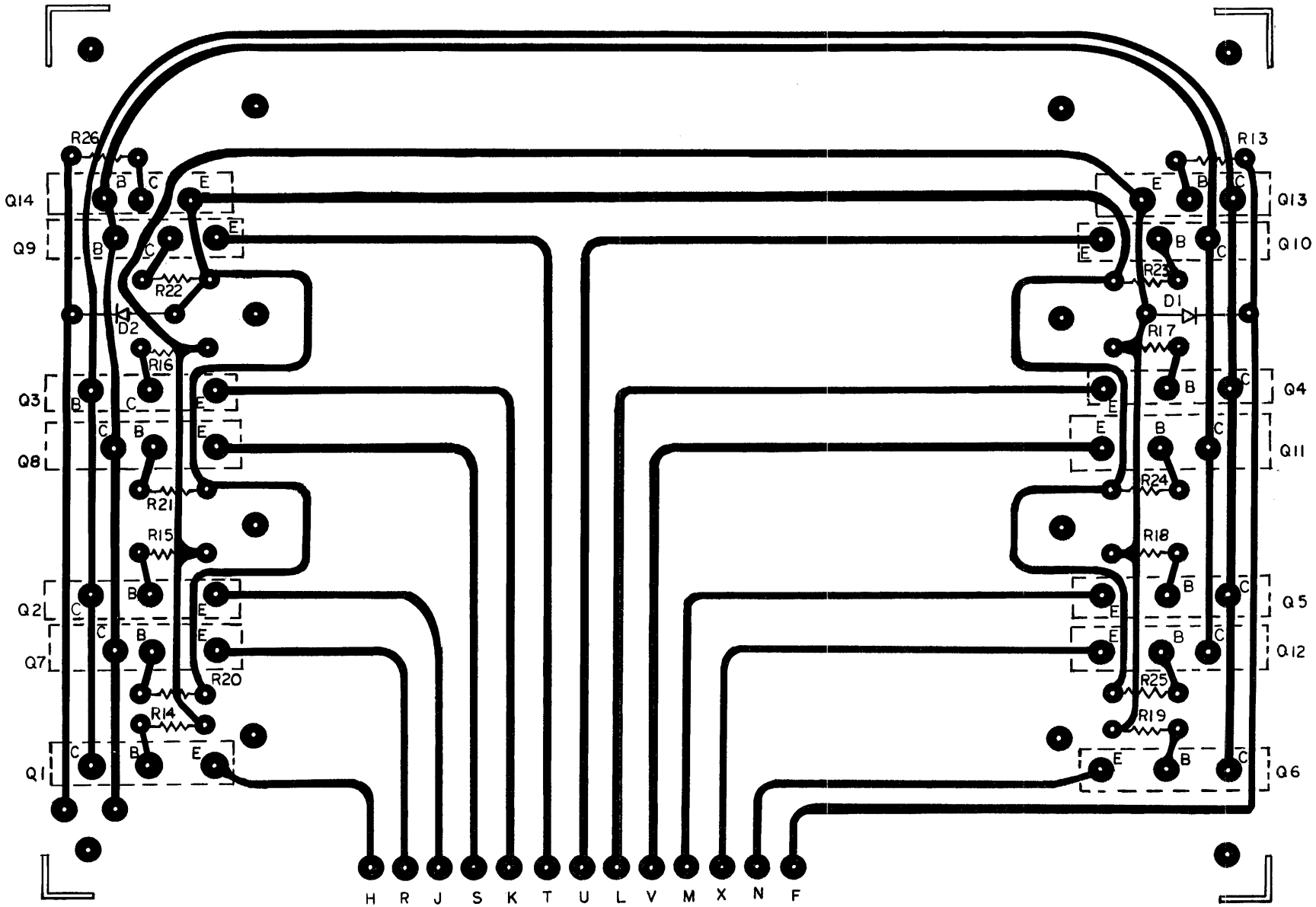
NOTE:

1. ON METHODE (22P) PLUG THE FOLLOWING NUMBERS CORRESPOND TO THE FOLLOWING LETTERS
   1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
   A B C D E F H J K L M N P R S T U V W X Y Z
2. C 13 - C 24 GOODALL .05 ufd, ±10% 100 VOLTS
3. R 13 - R24 ½ WATT, 10 % 20 COMPOSITION RESISTOR

Figure 6-10 Deflection Amplifier Resistor Stack Wiring Diagram

WD-C-22106

PANEL REAR



PANEL FRONT

Figure 6-11 Deflection Amplifier Printed Circuit Layout

MA-B-22116

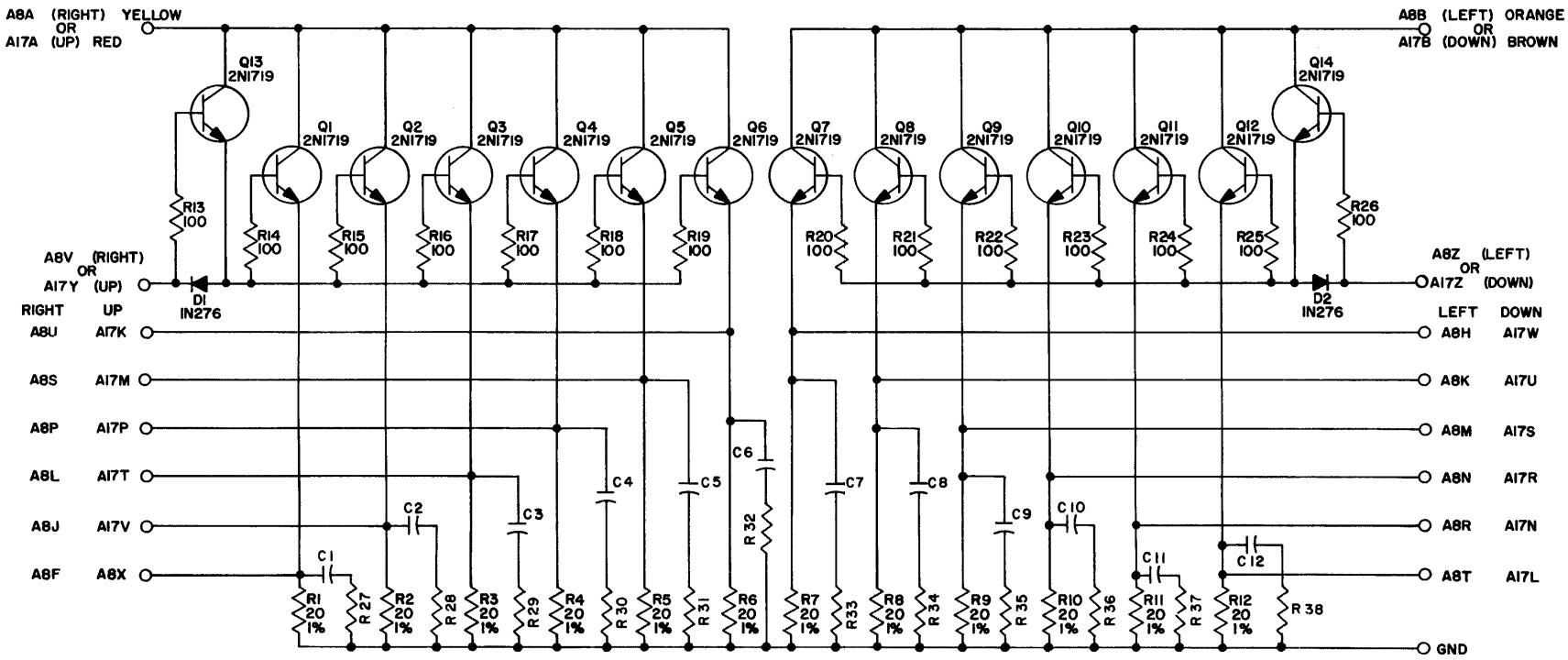
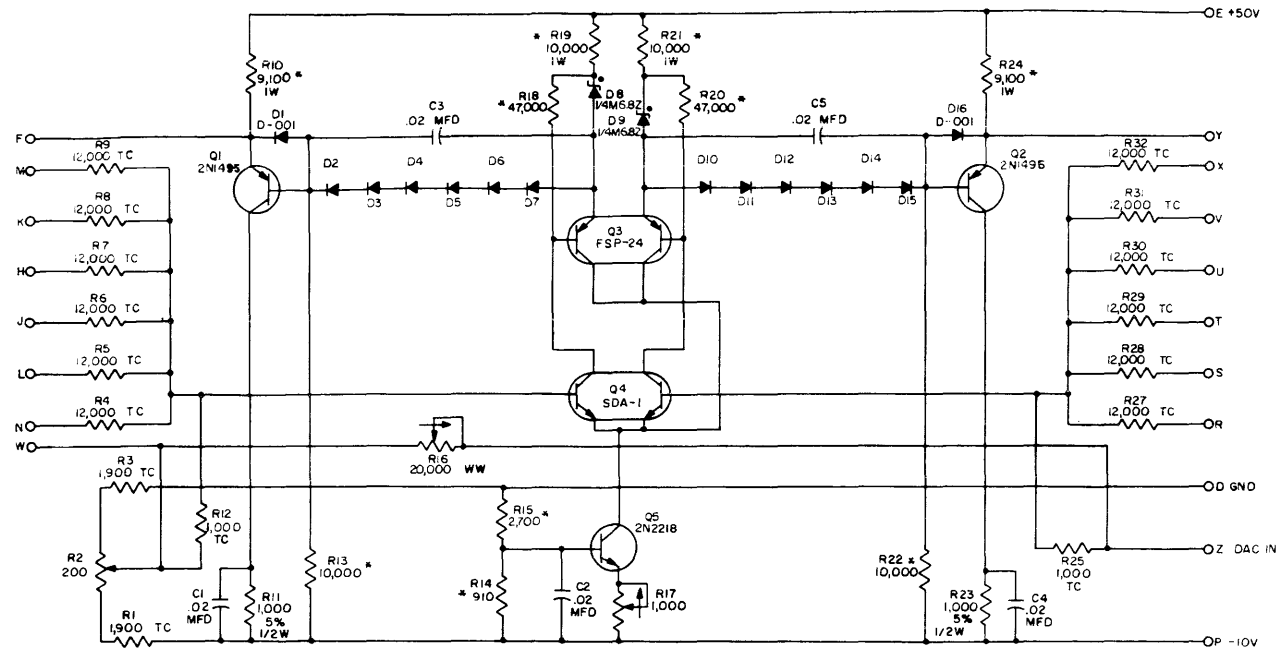


Figure 6-12 Deflection Output Amplifier Schematic

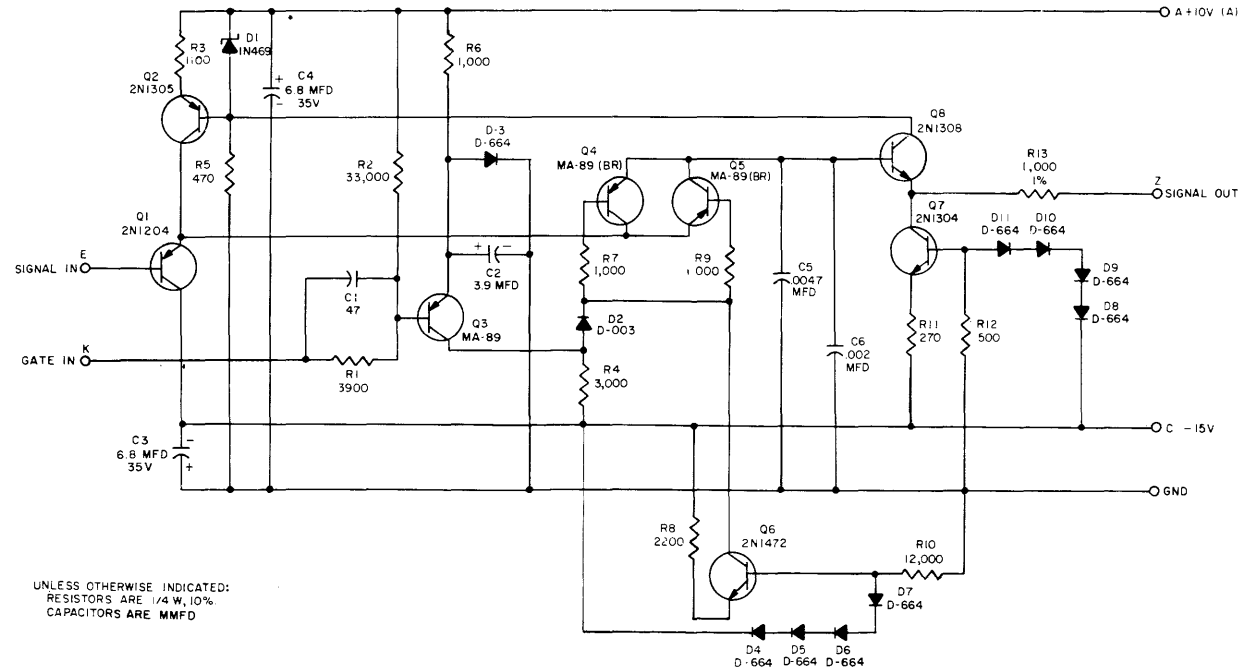
CS-B-22100



UNLESS OTHERWISE INDICATED:
TC-LOW TEMP. COEF., METALLIC FILM, ±1%, 1/2W
* RESISTOR DEPOSITED CARBON, ±1%
POTS ARE BOURNS
DIODES ARE D-662

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1495	2N1495	D-001	IN276
FSP-24	FSP-24	1/4M6.8Z	1/4M6.8Z
SDA-1	2N2060		
2N2218	2N2218		
D-662	IN645		

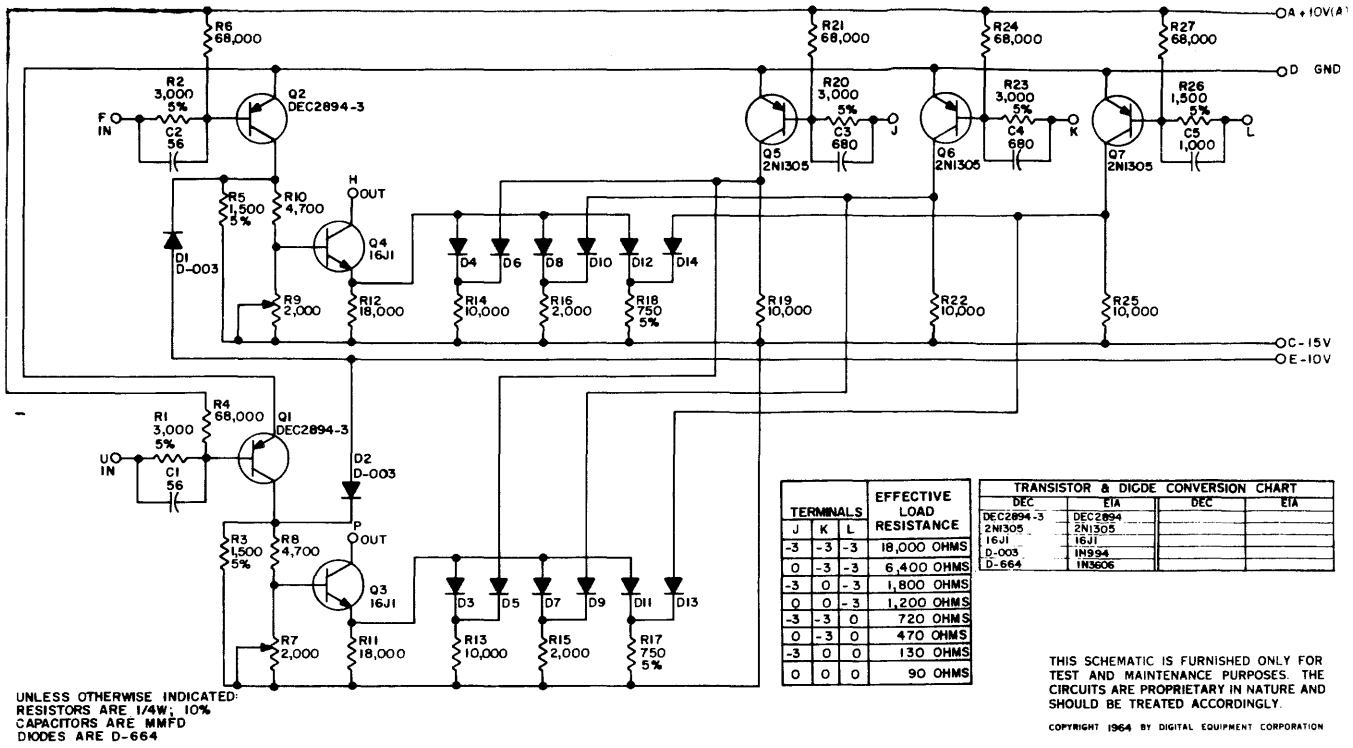
Figure 6-13 Display Preamplifier



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MA-89	2N2451	2N1308	2N1308
MA-89(BR)	2N2451 *	2N1304	2N1304
2N1305	2N1305	2N1472	2N1472
2N1204	2N1204	D-003	IN994
IN469	IN469	D-664	IN914

Figure 6-14 Follow or Hold



TERMINALS J	K	L	EFFECTIVE LOAD RESISTANCE
-3	-3	-3	18,000 OHMS
0	-3	-3	6,400 OHMS
-3	0	-3	1,800 OHMS
0	0	-3	1,200 OHMS
-3	-3	0	720 OHMS
0	-3	0	470 OHMS
-3	0	0	130 OHMS
0	0	0	90 OHMS

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-3	DEC2894		
2N1305	2N1305		
16JI	16JI		
D-003	IN994		
D-664	IN3606		

Figure 6-15 Feed Forward, CS-1579

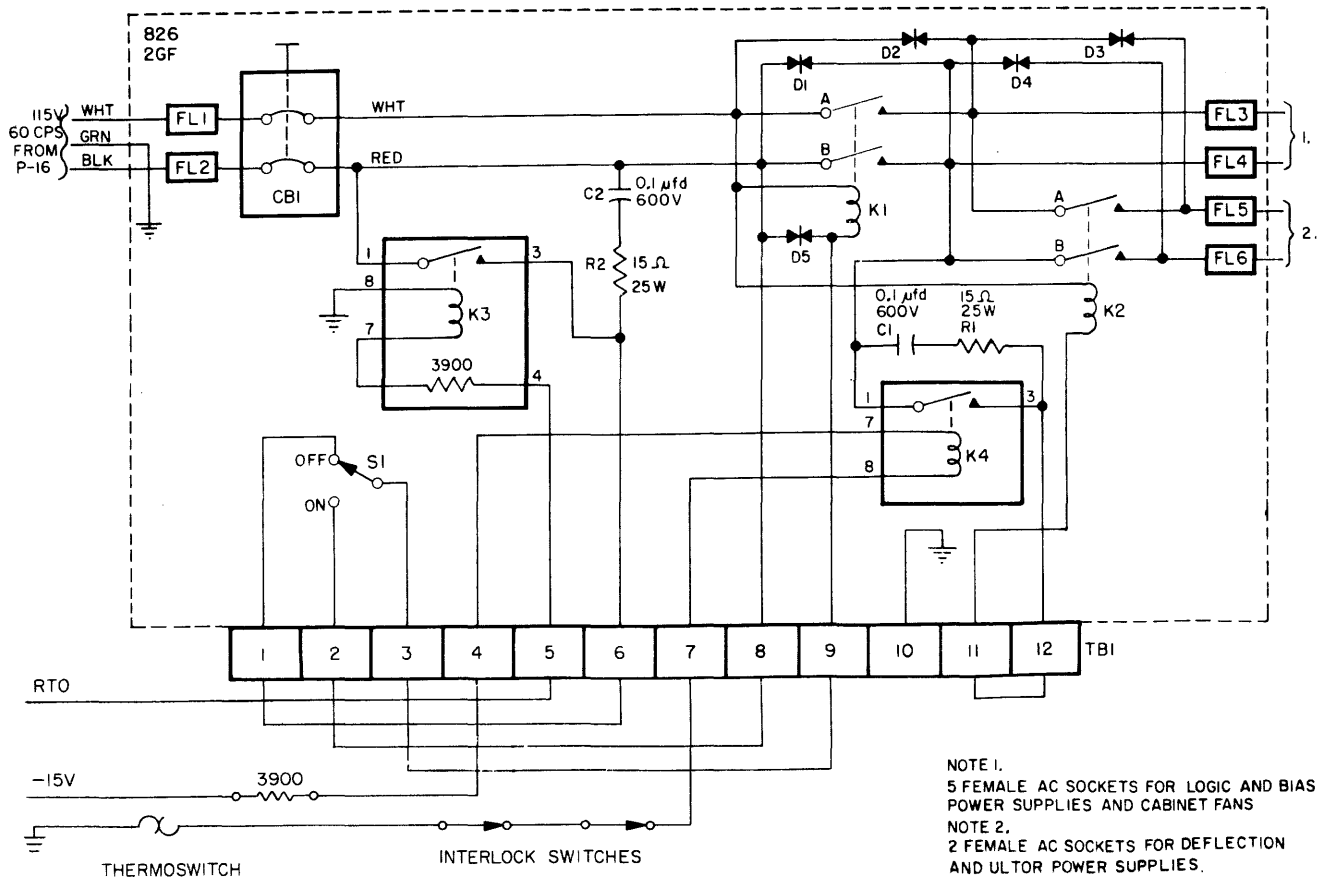


Figure 6-16 Type 826 Power Control

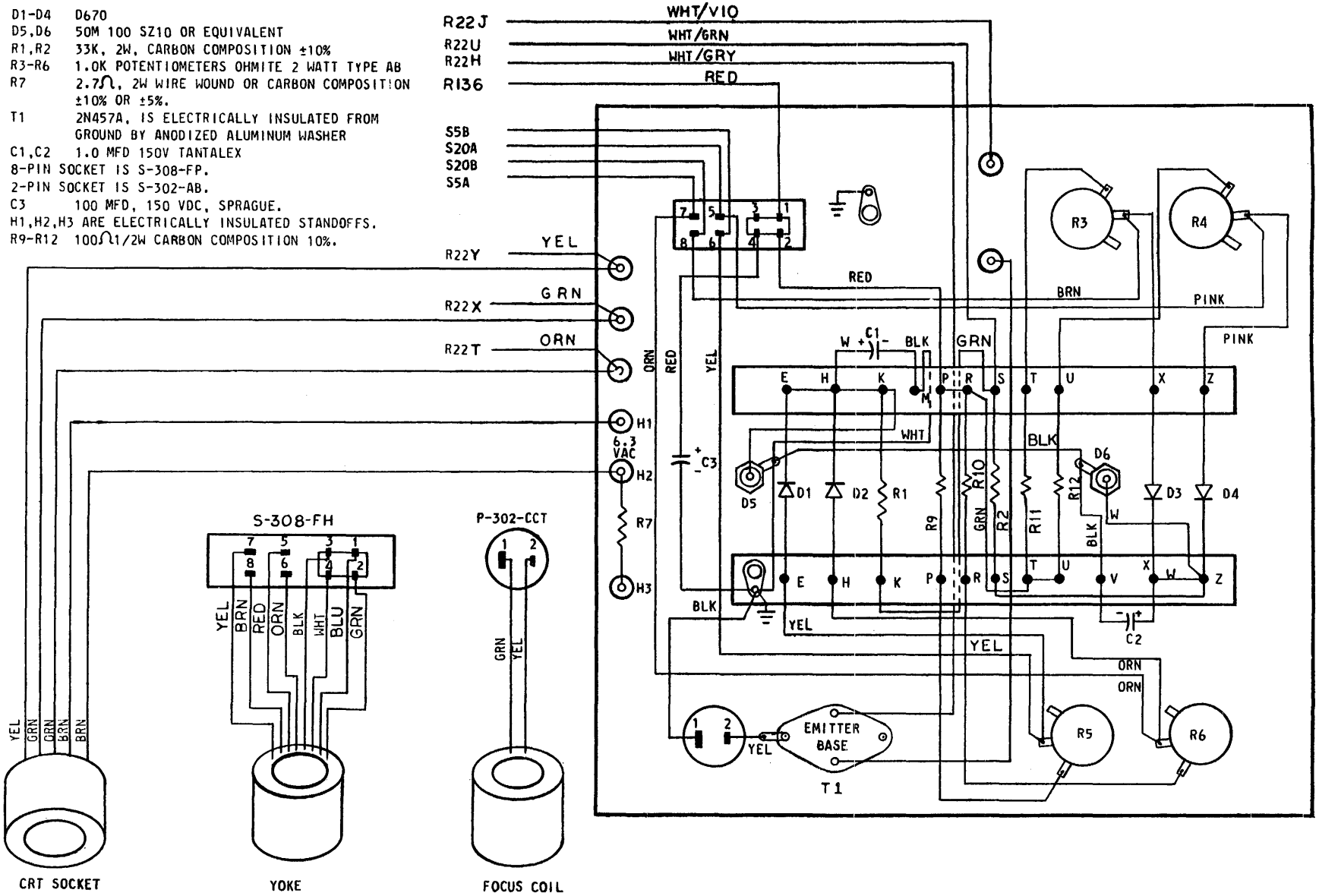


Figure 6-17 Component Mounting Plate

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