FIH CONFIDENTIAL

MODEL NAME : SF4H8
Board Number :
FILE NAME : Main Board

Revision History and Current Revision :

Revision	Description Of Changes	Date (M-D-Y)	Phase
A10	BOM cost estimate	08-04-2010	PR1
A11	Schematic Update	11-19-2010	PR1
A12	BOM LOCK DOWN	11-25-2010	PR1
A20	BOM LOCK DOWN	12-03-2010	PR1.5
B10	Schematic Update	02-11-2011	PR2
B11	BOM LOCK DOWN	03-17-2011	PR2
B20	Schematic Update	03-17-2011	PR2.5

Page Description

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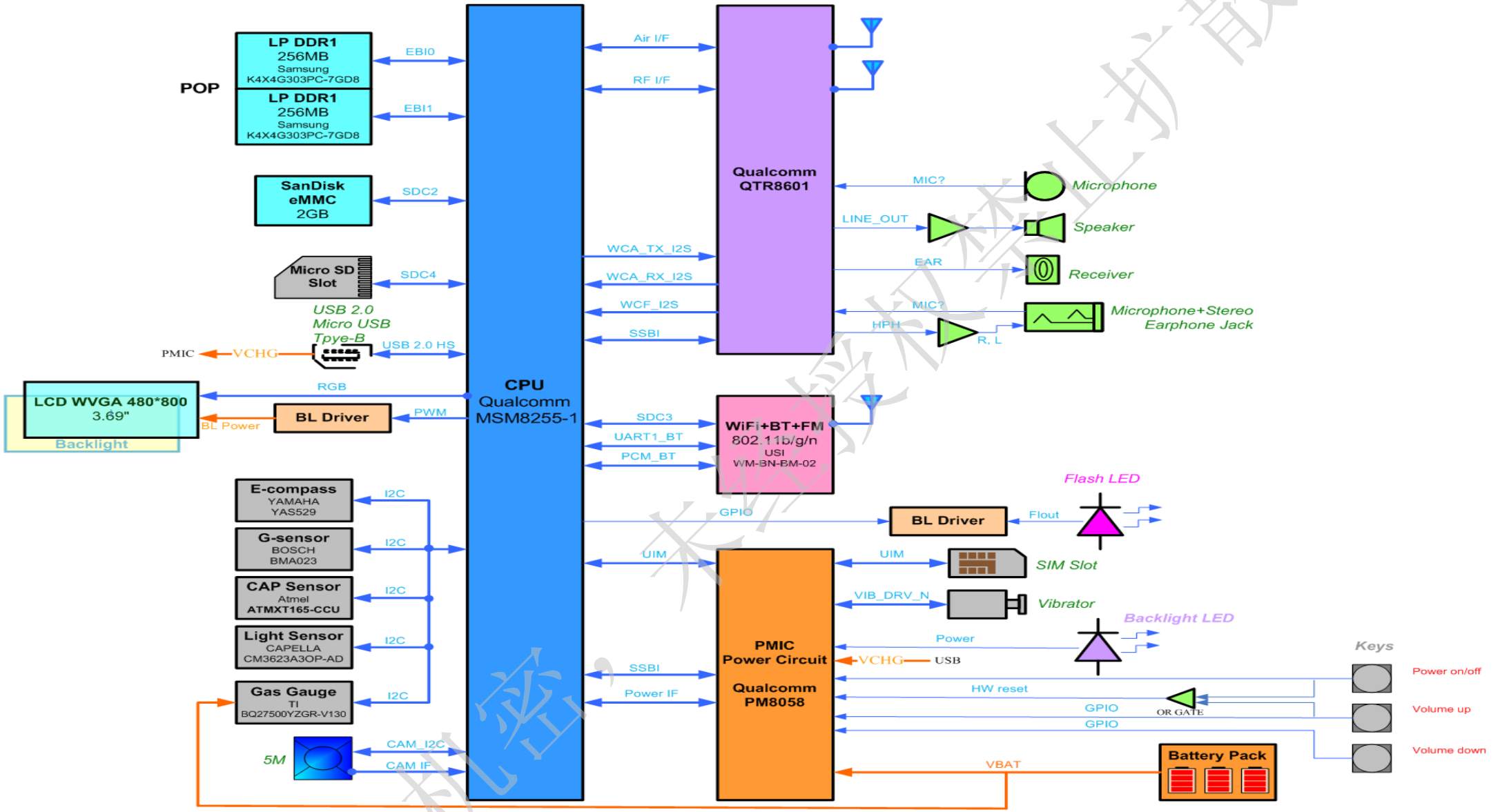

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Title	System Block	
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Title	Power Block		
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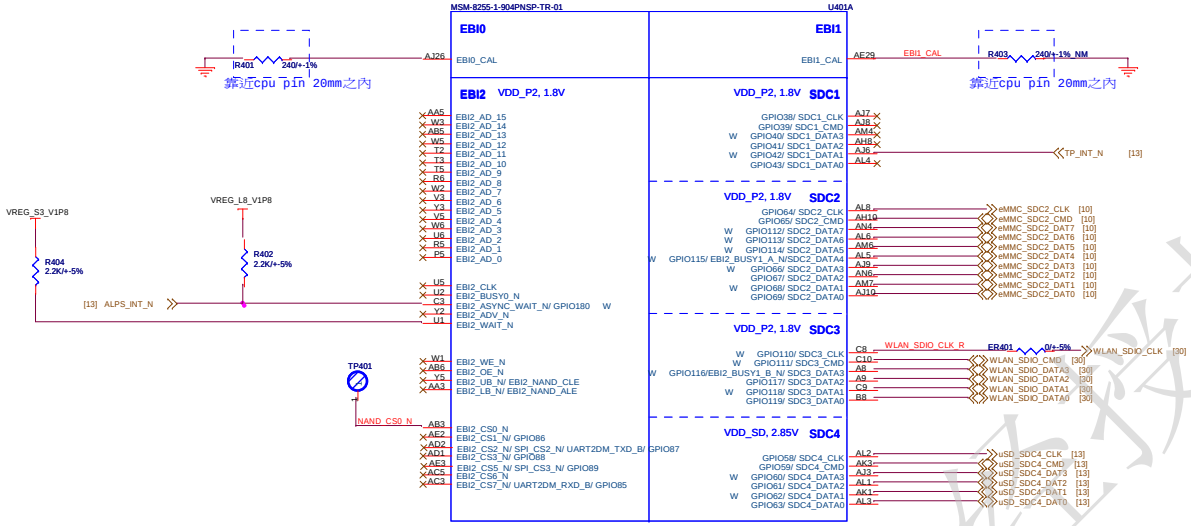

FIH

Title	CPU MSM8255-1_Memory & SDIO	
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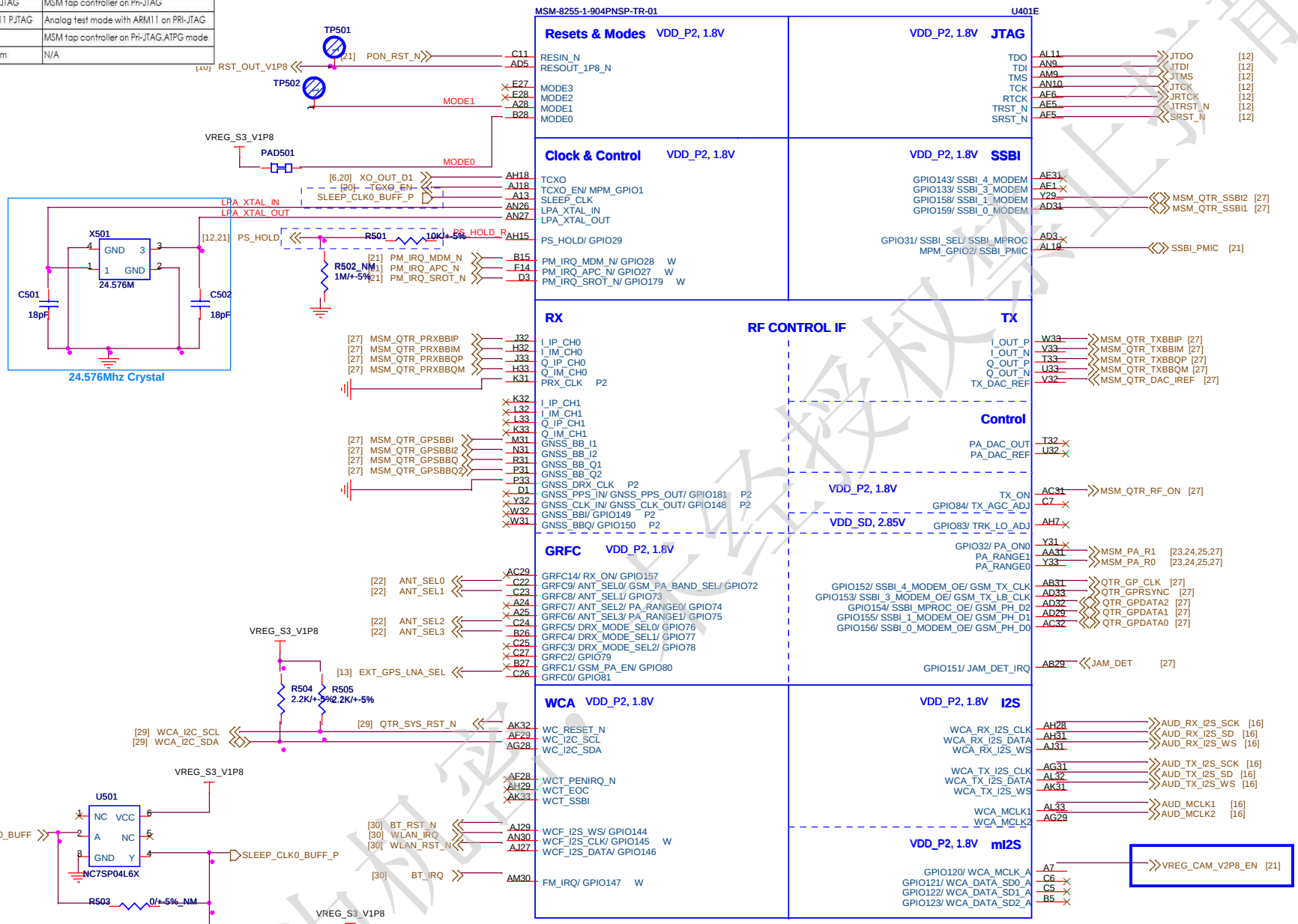
Modes	Function	Description
0000	MPOC only	ARM11 on Pri-JTAG
0001	SW Modes	JTAG SW controlled modes
0011	SC only	SC on pirmary JTAG
0100	Native MSM JTAG	MSM tap controller on Pri-JTAG
0110	Analog,ARM11 PJTAG	Analog test mode with ARM11 on PRI-JTAG
1100	MSM JTAG	MSM tap controller on Pri-JTAG,ATPG mode
1101	JTAG fuse pgm	N/A



FIH

Title	CPU MSM8255-1_RF & WCA & Ctr
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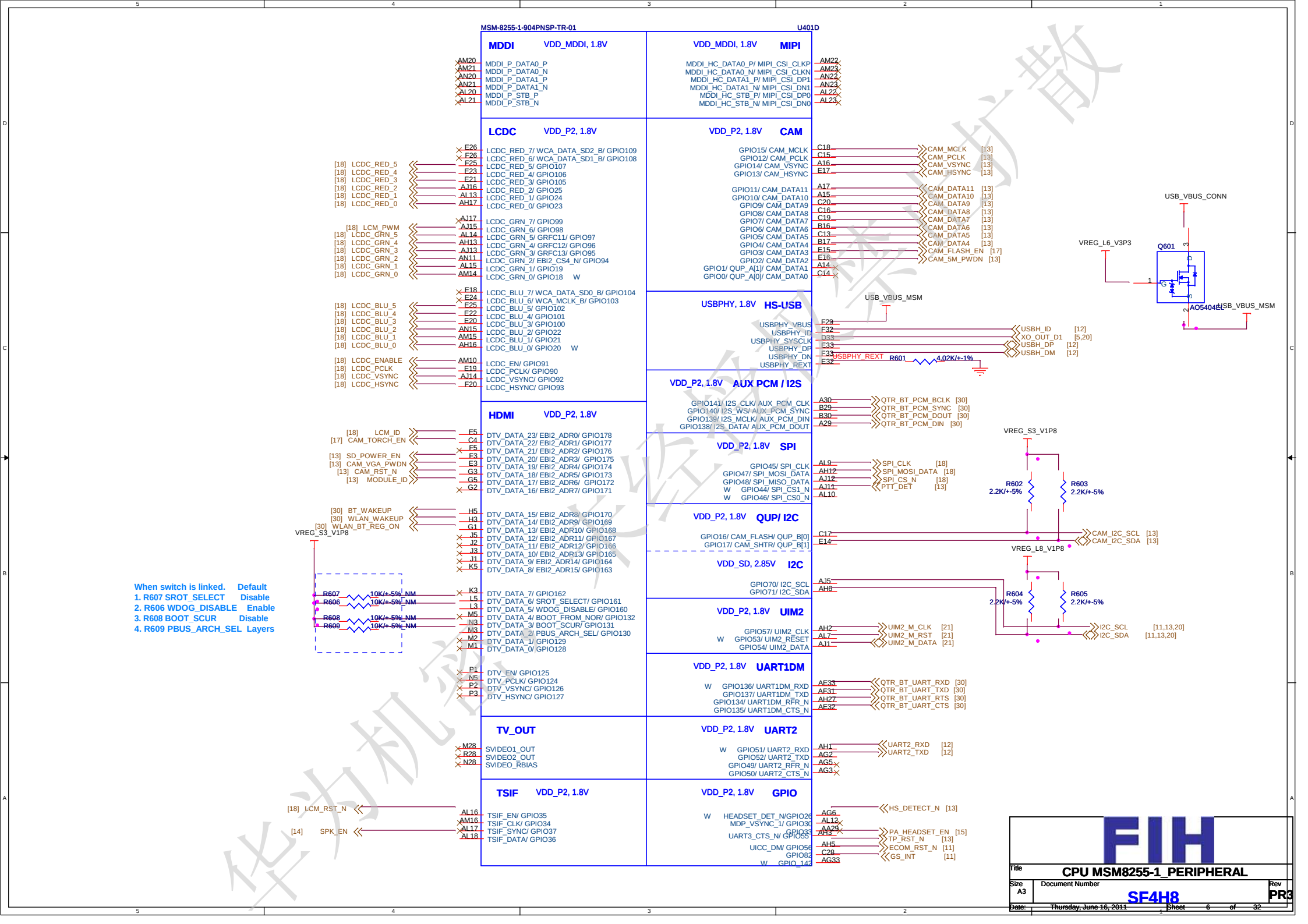
MSM-8255-1-904PNSP-TR-01
U401D
MDDI
VDD_MDDI, 1.8V
MDDI_P_DATA0_P
MDDI_P_DATA0_N
MDDI_P_DATA1_P
MDDI_P_DATA1_N
MDDI_P_STB_P
MDDI_P_STB_N
VDD_MDDI, 1.8V
MIPI
MDDI_HC_DATA0_P/ MIPI_CSI_CLKP
MDDI_HC_DATA0_N/ MIPI_CSI_CLKN
MDDI_HC_DATA1_P/ MIPI_CSI_DP1
MDDI_HC_DATA1_N/ MIPI_CSI_DN1
MDDI_HC_STB_P/ MIPI_CSI_DP0
MDDI_HC_STB_N/ MIPI_CSI_DN0
LCDC
VDD_P2, 1.8V
LCDC_RED_7/ WCA_DATA_SD2_B/ GPIO109
LCDC_RED_6/ WCA_DATA_SD1_B/ GPIO108
LCDC_RED_5/ GPIO107
LCDC_RED_4/ GPIO106
LCDC_RED_3/ GPIO105
LCDC_RED_2/ GPIO25
LCDC_RED_1/ GPIO24
LCDC_RED_0/ GPIO23
LCDC_GRN_7/ GPIO99
LCDC_GRN_6/ GPIO98
LCDC_GRN_5/ GRFC11/ GPIO97
LCDC_GRN_4/ GRFC12/ GPIO96
LCDC_GRN_3/ GRFC13/ GPIO95
LCDC_GRN_2/ EBI2_CS4_N/ GPIO94
LCDC_GRN_1/ GPIO19
LCDC_GRN_0/ GPIO18 W
LCDC_BLU_7/ WCA_DATA_SD0_B/ GPIO104
LCDC_BLU_6/ WCA_MCLK_B/ GPIO103
LCDC_BLU_5/ GPIO102
LCDC_BLU_4/ GPIO101
LCDC_BLU_3/ GPIO100
LCDC_BLU_2/ GPIO22
LCDC_BLU_1/ GPIO21
LCDC_BLU_0/ GPIO20 W
LCDC_EN/ GPIO91
LCDC_PCLK/ GPIO90
LCDC_VSYNC/ GPIO92
LCDC_HSYNC/ GPIO93
VDD_P2, 1.8V
CAM
GPIO15/ CAM_MCLK
GPIO12/ CAM_PCLK
GPIO14/ CAM_VSYNC
GPIO13/ CAM_HSYNC
GPIO11/ CAM_DATA11
GPIO10/ CAM_DATA10
GPIO9/ CAM_DATA9
GPIO8/ CAM_DATA8
GPIO7/ CAM_DATA7
GPIO6/ CAM_DATA6
GPIO5/ CAM_DATA5
GPIO4/ CAM_DATA4
GPIO3/ CAM_DATA3
GPIO2/ CAM_DATA2
GPIO1/ QUP_A[1]/ CAM_DATA1
GPIO0/ QUP_A[0]/ CAM_DATA0
CAM_MCLK [13]
CAM_PCLK [13]
CAM_VSYNC [13]
CAM_HSYNC [13]
CAM_DATA11 [13]
CAM_DATA10 [13]
CAM_DATA9 [13]
CAM_DATA8 [13]
CAM_DATA7 [13]
CAM_DATA6 [13]
CAM_DATA5 [13]
CAM_DATA4 [13]
CAM_FLASH_EN [17]
CAM_5M_PWDN [13]
USBPHY, 1.8V
HS-USB
USBPHY_VBUS
USBPHY_ID
USBPHY_SYSCLK
USBPHY_DP
USBPHY_DN
USBPHY_REXT
USB_VBUS_MSM
USBH_ID [12]
XO_OUT_D1 [5,20]
USBH_DP [12]
USBH_DM [12]
USBPHY_REXT
R601
4.02K/+-1%
USB_VBUS_CONN
VREG_L6_V3P3
Q601
AO5404E
USB_VBUS_MSM
VDD_P2, 1.8V
AUX PCM / I2S
GPIO141/ I2S_CLK/ AUX_PCM_CLK
GPIO140/ I2S_WS/ AUX_PCM_SYNC
GPIO139/ I2S_MCLK/ AUX_PCM_DIN
GPIO138/ I2S_DATA/ AUX_PCM_DOUT
QTR_BT_PCM_BCLK [30]
QTR_BT_PCM_SYNC [30]
QTR_BT_PCM_DOUT [30]
QTR_BT_PCM_DIN [30]
VDD_P2, 1.8V
SPI
GPIO45/ SPI_CLK
GPIO47/ SPI_MOSI_DATA
GPIO48/ SPI_MISO_DATA
GPIO44/ SPI_CS1_N
GPIO46/ SPI_CS0_N
SPI_CLK [18]
SPI_MOSI_DATA [18]
SPI_CS_N [18]
PTT_DET [13]
VREG_S3_V1P8
R602
2.2K/+-5%
R603
2.2K/+-5%
VDD_P2, 1.8V
QUP/ I2C
GPIO16/ CAM_FLASH/ QUP_B[0]
GPIO17/ CAM_SHTR/ QUP_B[1]
CAM_I2C_SCL [13]
CAM_I2C_SDA [13]
VDD_SD, 2.85V
I2C
GPIO70/ I2C_SCL
GPIO71/ I2C_SDA
VREG_L8_V1P8
R604
2.2K/+-5%
R605
2.2K/+-5%
I2C_SCL [11,13,20]
I2C_SDA [11,13,20]
VDD_P2, 1.8V
UIM2
GPIO57/ UIM2_CLK
GPIO53/ UIM2_RESET
GPIO54/ UIM2_DATA
UIM2_M_CLK [21]
UIM2_M_RST [21]
UIM2_M_DATA [21]
VDD_P2, 1.8V
UART1DM
GPIO136/ UART1DM_RXD
GPIO137/ UART1DM_TXD
GPIO134/ UART1DM_RFR_N
GPIO135/ UART1DM_CTS_N
QTR_BT_UART_RXD [30]
QTR_BT_UART_TXD [30]
QTR_BT_UART_RTS [30]
QTR_BT_UART_CTS [30]
HDMI
VDD_P2, 1.8V
DTV_DATA_23/ EBI2_ADR0/ GPIO178
DTV_DATA_22/ EBI2_ADR1/ GPIO177
DTV_DATA_21/ EBI2_ADR2/ GPIO176
DTV_DATA_20/ EBI2_ADR3/ GPIO175
DTV_DATA_19/ EBI2_ADR4/ GPIO174
DTV_DATA_18/ EBI2_ADR5/ GPIO173
DTV_DATA_17/ EBI2_ADR6/ GPIO172
DTV_DATA_16/ EBI2_ADR7/ GPIO171
DTV_DATA_15/ EBI2_ADR8/ GPIO170
DTV_DATA_14/ EBI2_ADR9/ GPIO169
DTV_DATA_13/ EBI2_ADR10/ GPIO168
DTV_DATA_12/ EBI2_ADR11/ GPIO167
DTV_DATA_11/ EBI2_ADR12/ GPIO166
DTV_DATA_10/ EBI2_ADR13/ GPIO165
DTV_DATA_9/ EBI2_ADR14/ GPIO164
DTV_DATA_8/ EBI2_ADR15/ GPIO163
DTV_DATA_7/ GPIO162
DTV_DATA_6/ SROT_SELECT/ GPIO161
DTV_DATA_5/ WDOG_DISABLE/ GPIO160
DTV_DATA_4/ BOOT_FROM_NOR/ GPIO132
DTV_DATA_3/ BOOT_SCUR/ GPIO131
DTV_DATA_2/ PBUS_ARCH_SEL/ GPIO130
DTV_DATA_1/ GPIO129
DTV_DATA_0/ GPIO128
DTV_EN/ GPIO125
DTV_PCLK/ GPIO124
DTV_VSYNC/ GPIO126
DTV_HSYNC/ GPIO127
VDD_P2, 1.8V
UART2
GPIO51/ UART2_RXD
GPIO52/ UART2_TXD
GPIO49/ UART2_RFR_N
GPIO50/ UART2_CTS_N
UART2_RXD [12]
UART2_TXD [12]
TV_OUT
SVIDEO1_OUT
SVIDEO2_OUT
SVIDEO_RBIAS
TSIF
VDD_P2, 1.8V
TSIF_EN/ GPIO35
TSIF_CLK/ GPIO34
TSIF_SYNC/ GPIO37
TSIF_DATA/ GPIO36
VDD_P2, 1.8V
GPIO
HEADSET_DET_N/GPIO26
MDP_VSYNC_1/ GPIO30
GPIO33
UART3_CTS_N/ GPIO55
UICC_DM/ GPIO56
GPIO82
GPIO_142
HS_DETECT_N [13]
PA_HEADSET_EN [15]
TP_RST_N [13]
ECOM_RST_N [11]
GS_INT [11]
LCM_ID
CAM_TORCH_EN
SD_POWER_EN
CAM_VGA_PWDN
CAM_RST_N
MODULE_ID
BT_WAKEUP
WLAN_WAKEUP
WLAN_BT_REG_ON
VREG_S3_V1P8
R607 10K/+-5% NM
R606 10K/+-5% NM
R608 10K/+-5% NM
R609 10K/+-5% NM
When switch is linked. Default
1. R607 SROT_SELECT Disable
2. R606 WDOG_DISABLE Enable
3. R608 BOOT_SCUR Disable
4. R609 PBUS_ARCH_SEL Layers
LCM_RST_N
SPK_EN
Title
CPU MSM8255-1_PERIPHERAL
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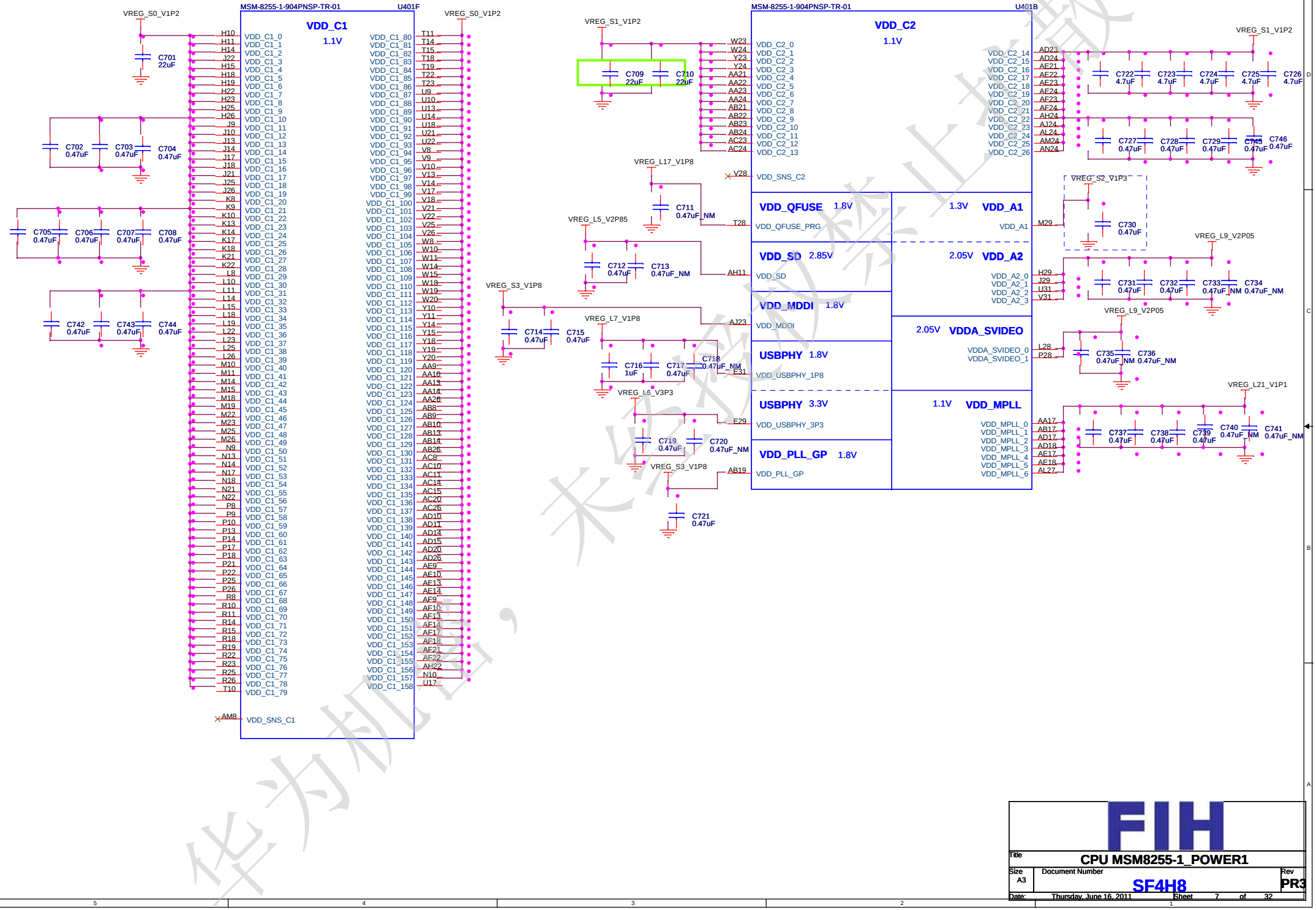

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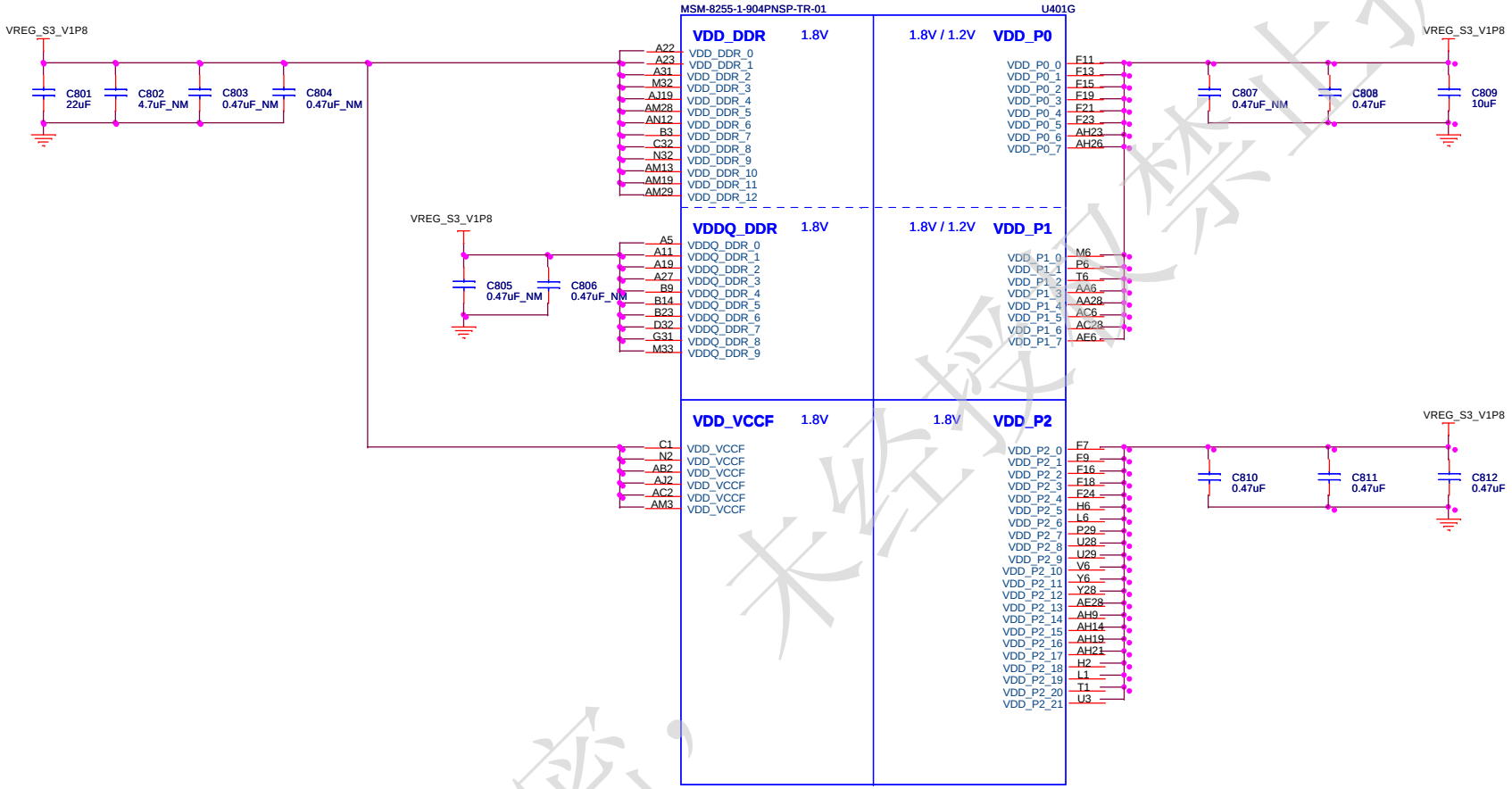

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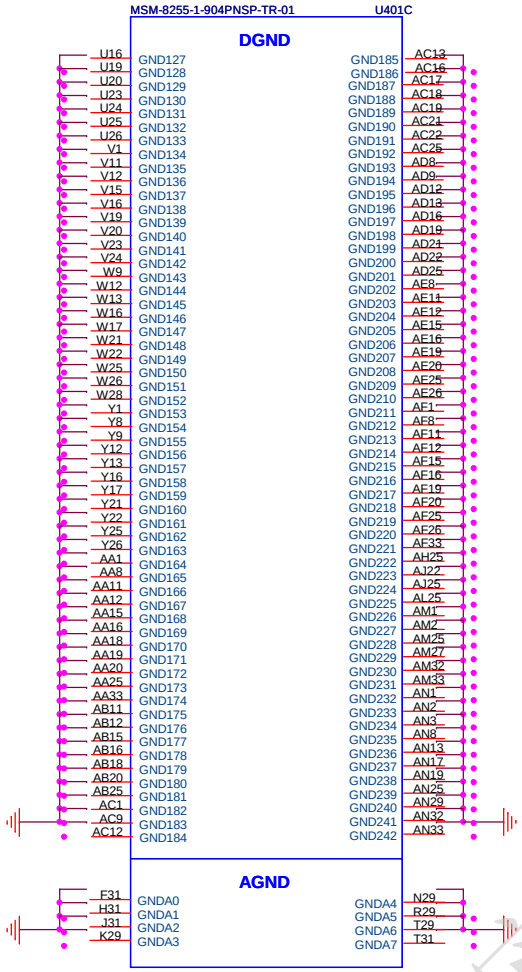

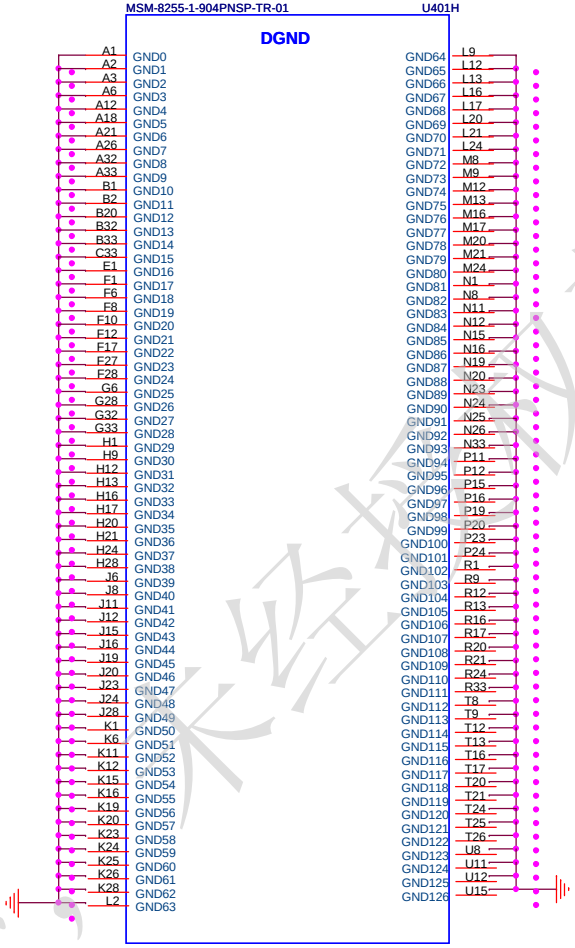

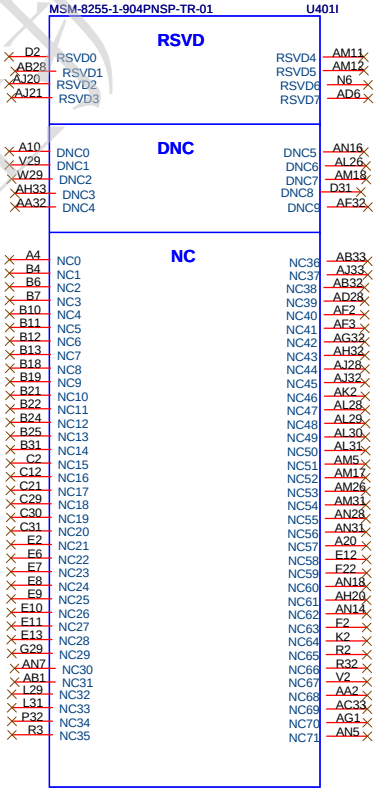

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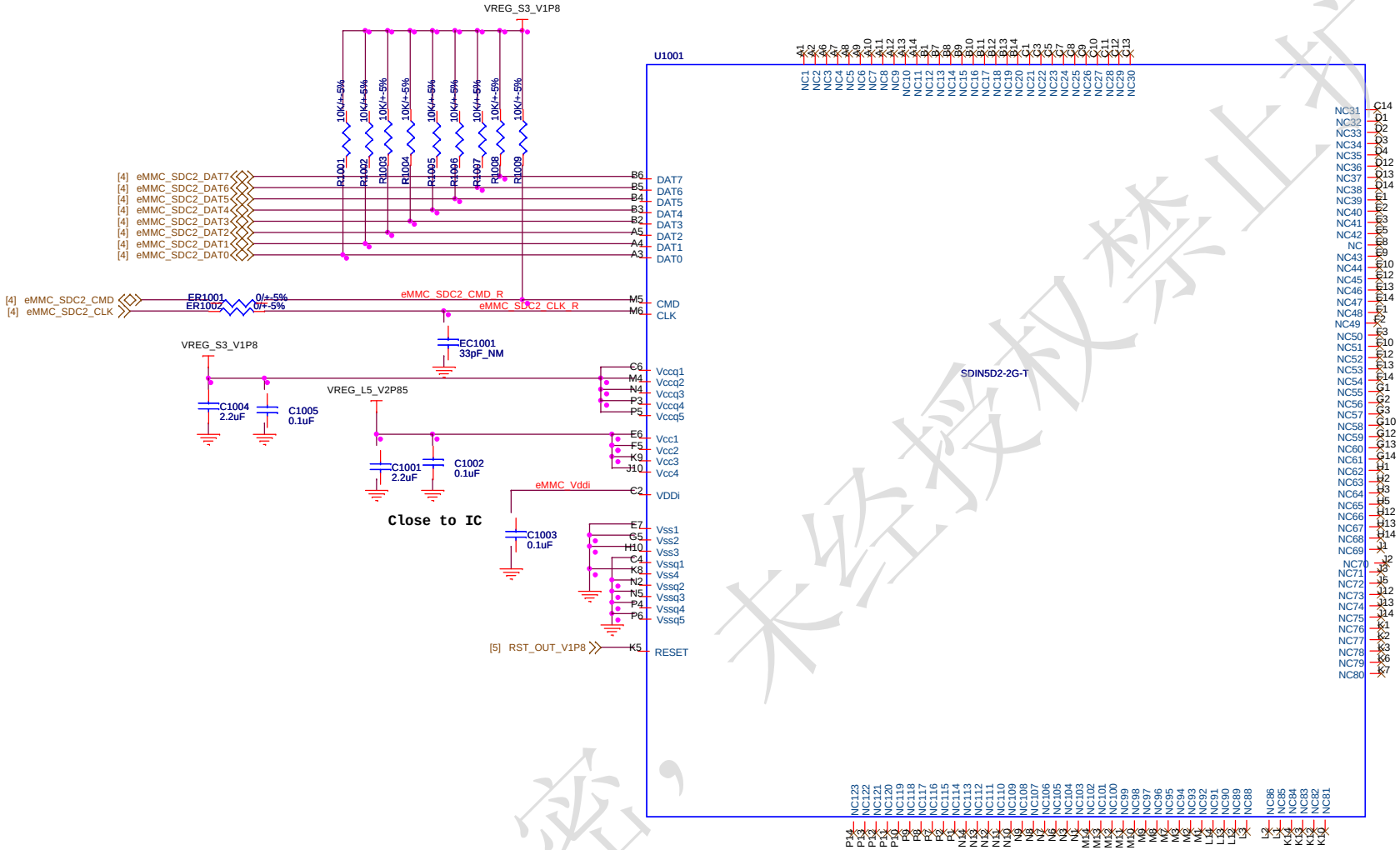
Sandisk eMMC 2GB



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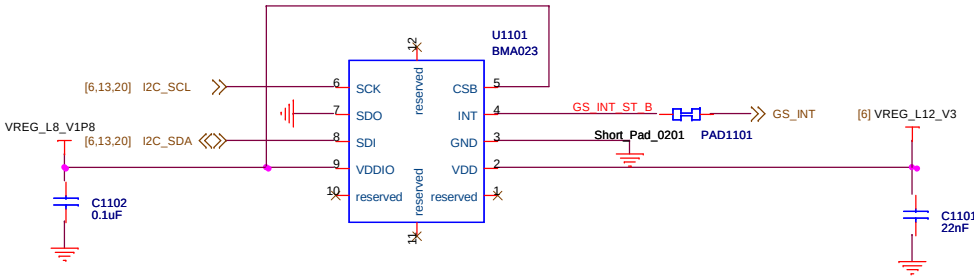
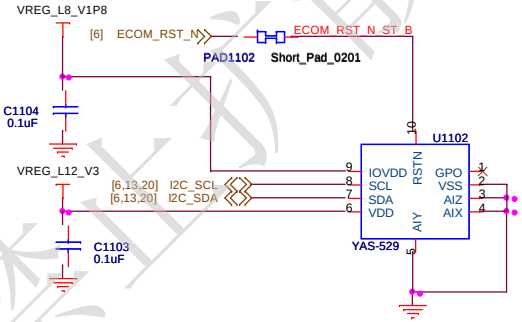
G-Sensor



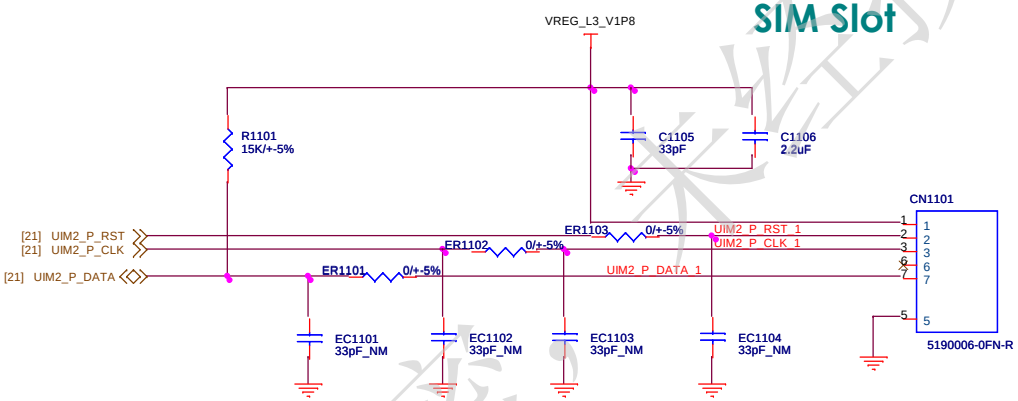
I2C Address: 0111000b (38h)

E-Compass (YAMAHA)

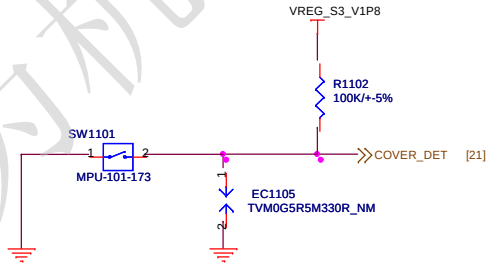


I2C Address: 0101110b (2Eh)
If RSTN no use, connect it to IOVDD

SIM Slot



Cover Detect Switch



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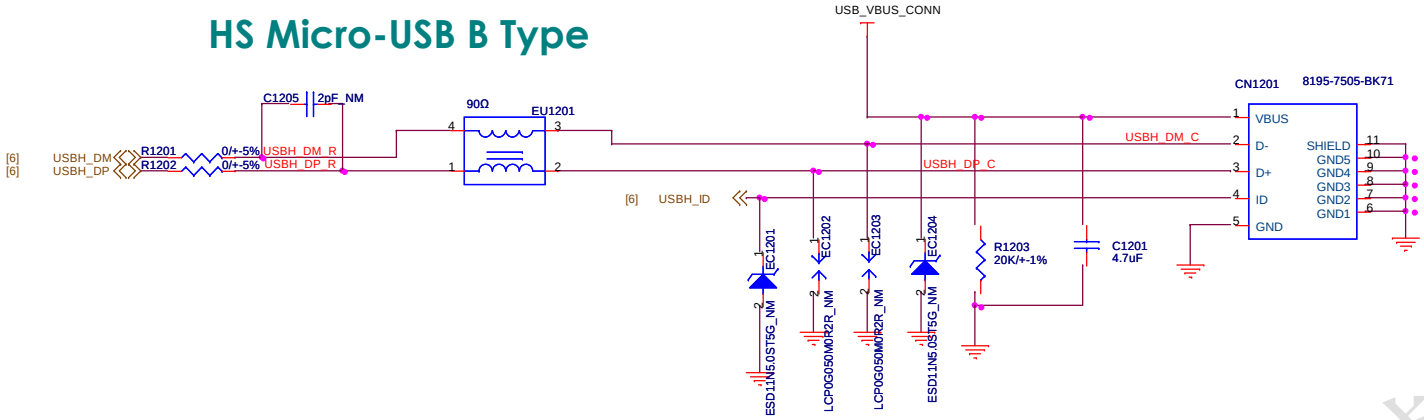
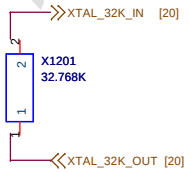
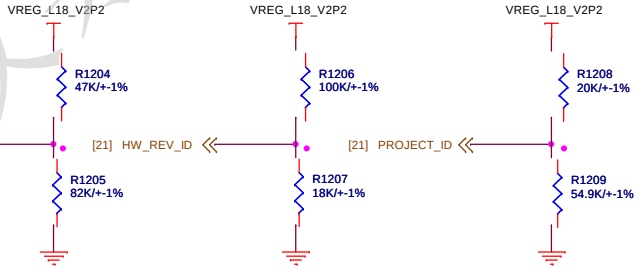
HS Micro-USB B Type



32.768K Sleep CLK

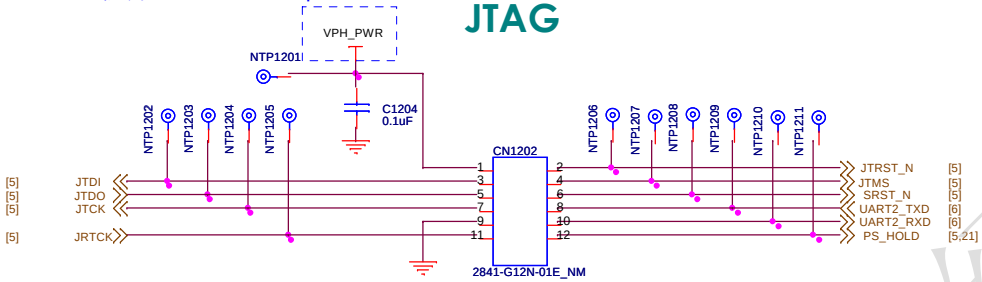


Board ID

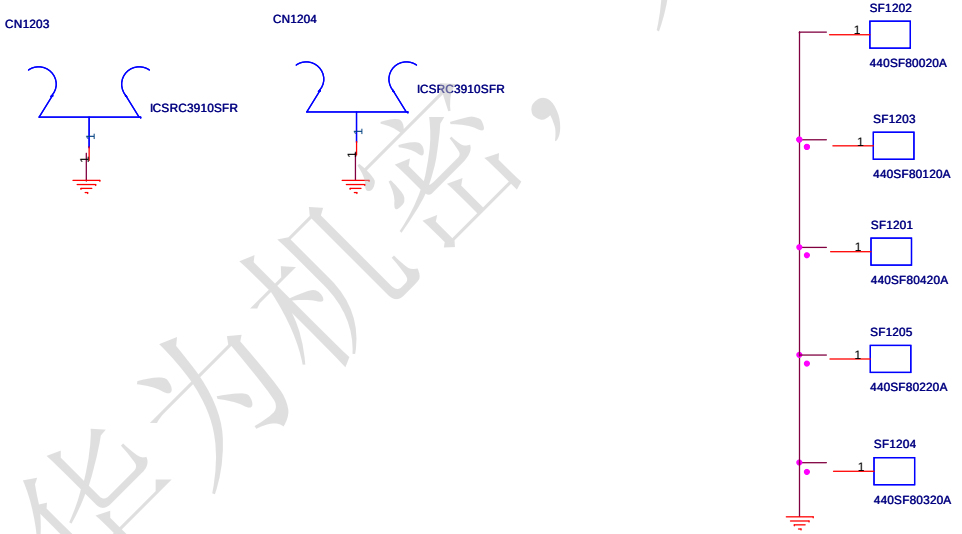


JTAG

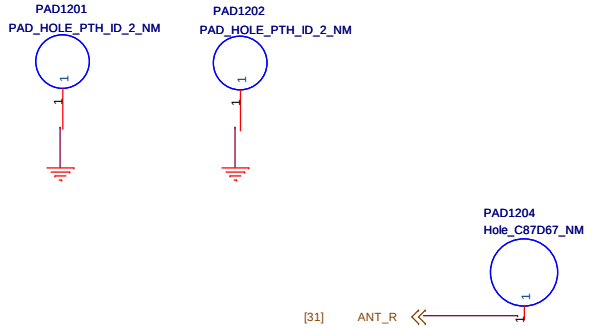
根據JTAG Board Update.



Shielding Frame



PTH



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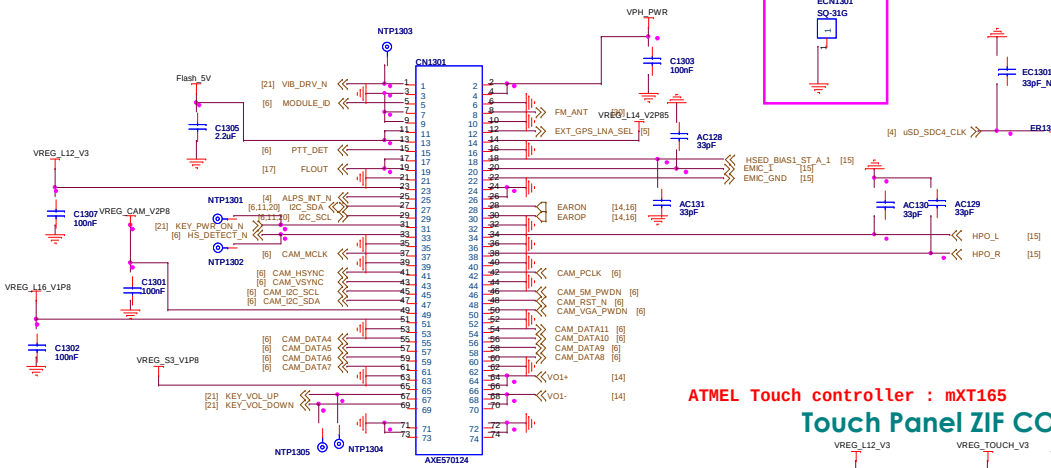
EMC 20101103 update

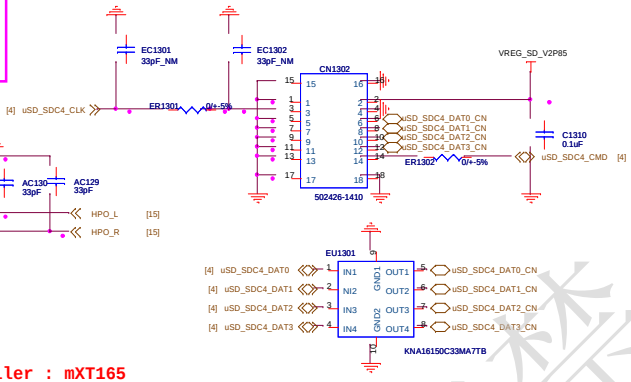
EMC 20110221 update

LINK FPC



ECN1301
SQ-31G

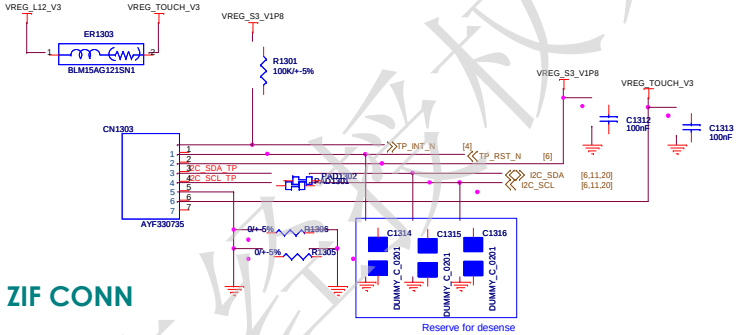
SD_Board B2B



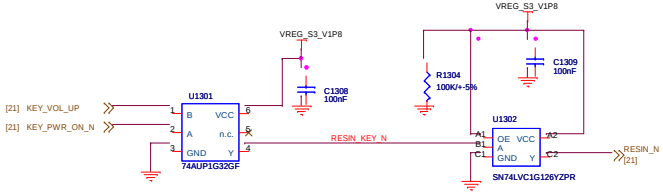
ATMEL Touch controller : mXT165

Touch Panel ZIF CONN

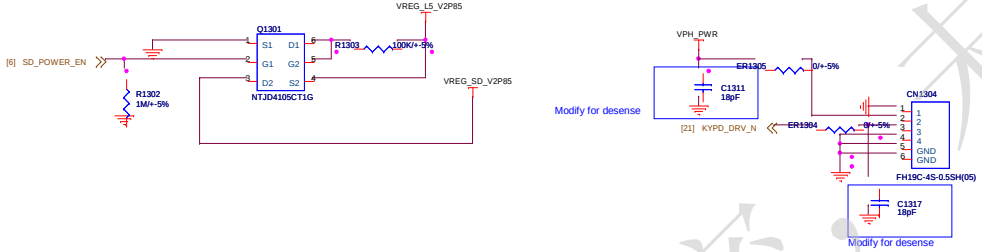
KNA16150C33MA5TS



HW RESET



LED ZIF CONN



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Title: B2B

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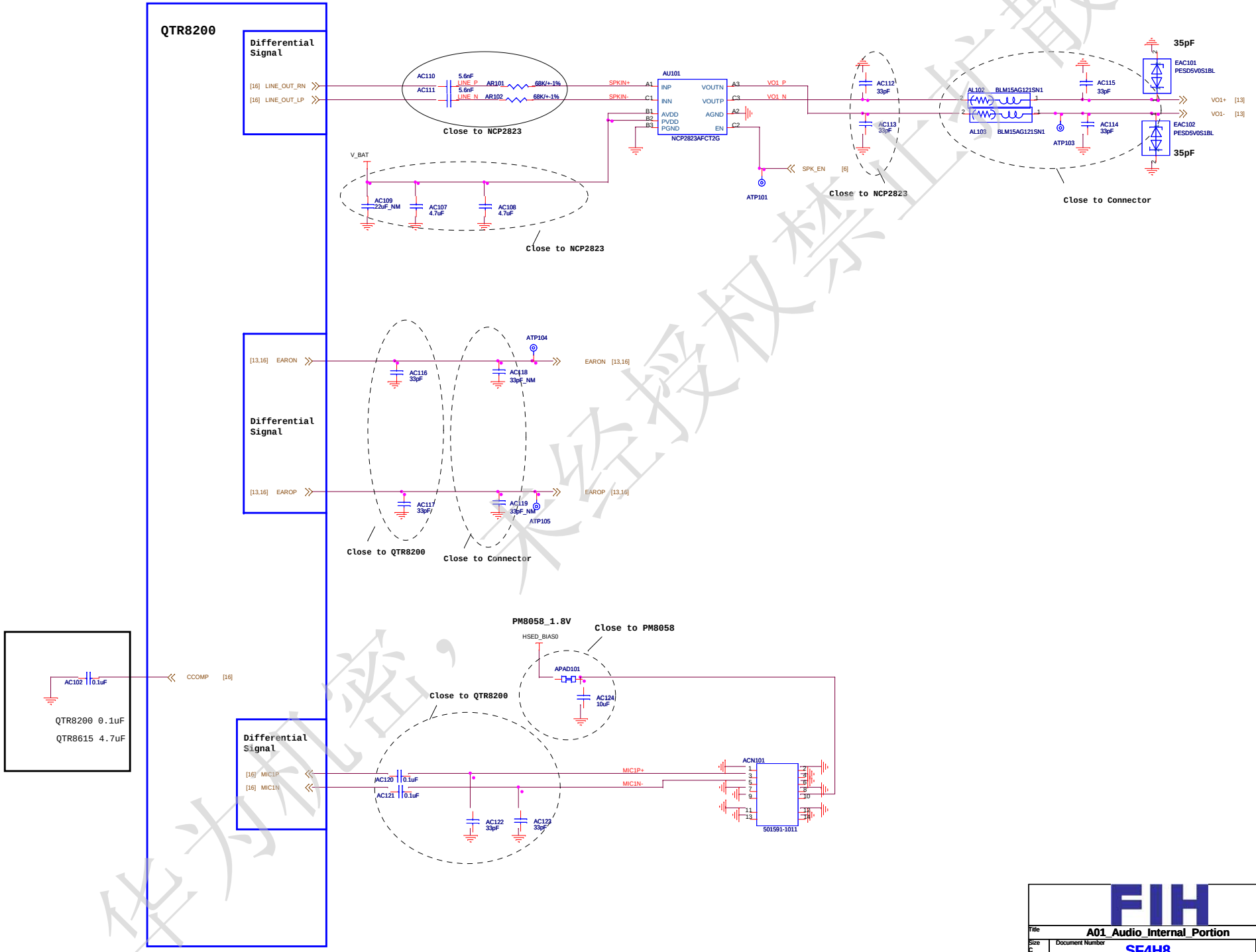
Internal Audio SCH



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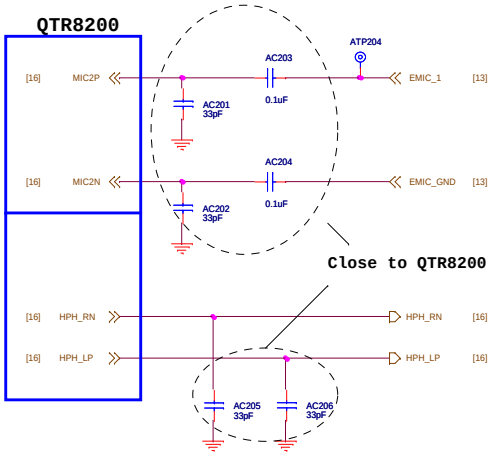
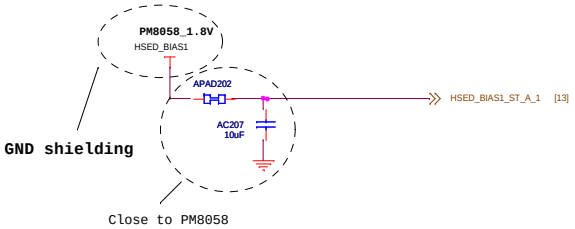
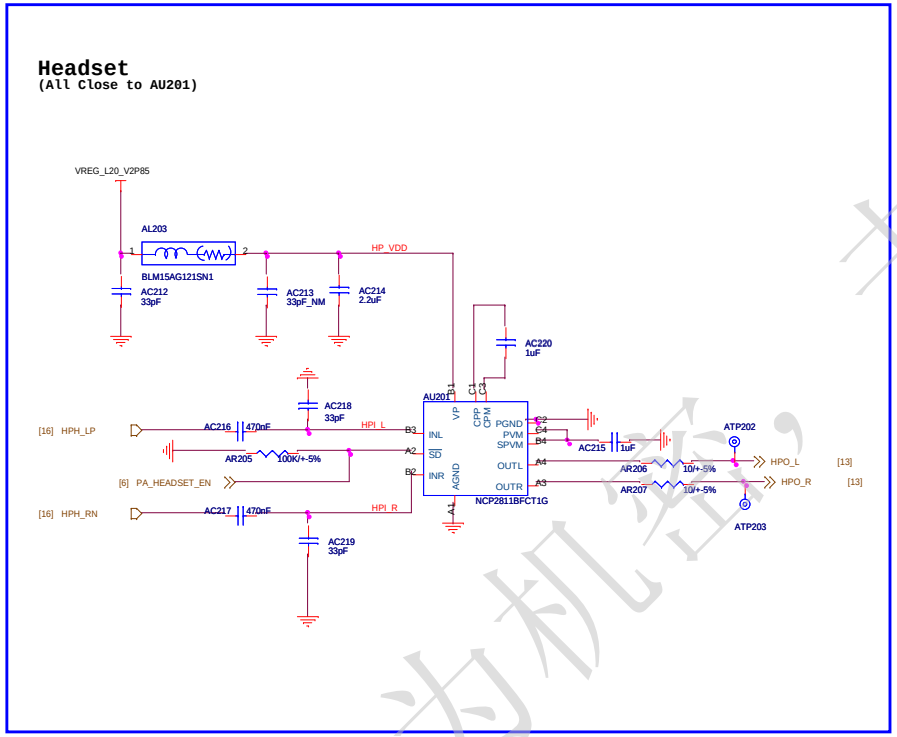




PTT_DET	State
H	Have push
L	No push



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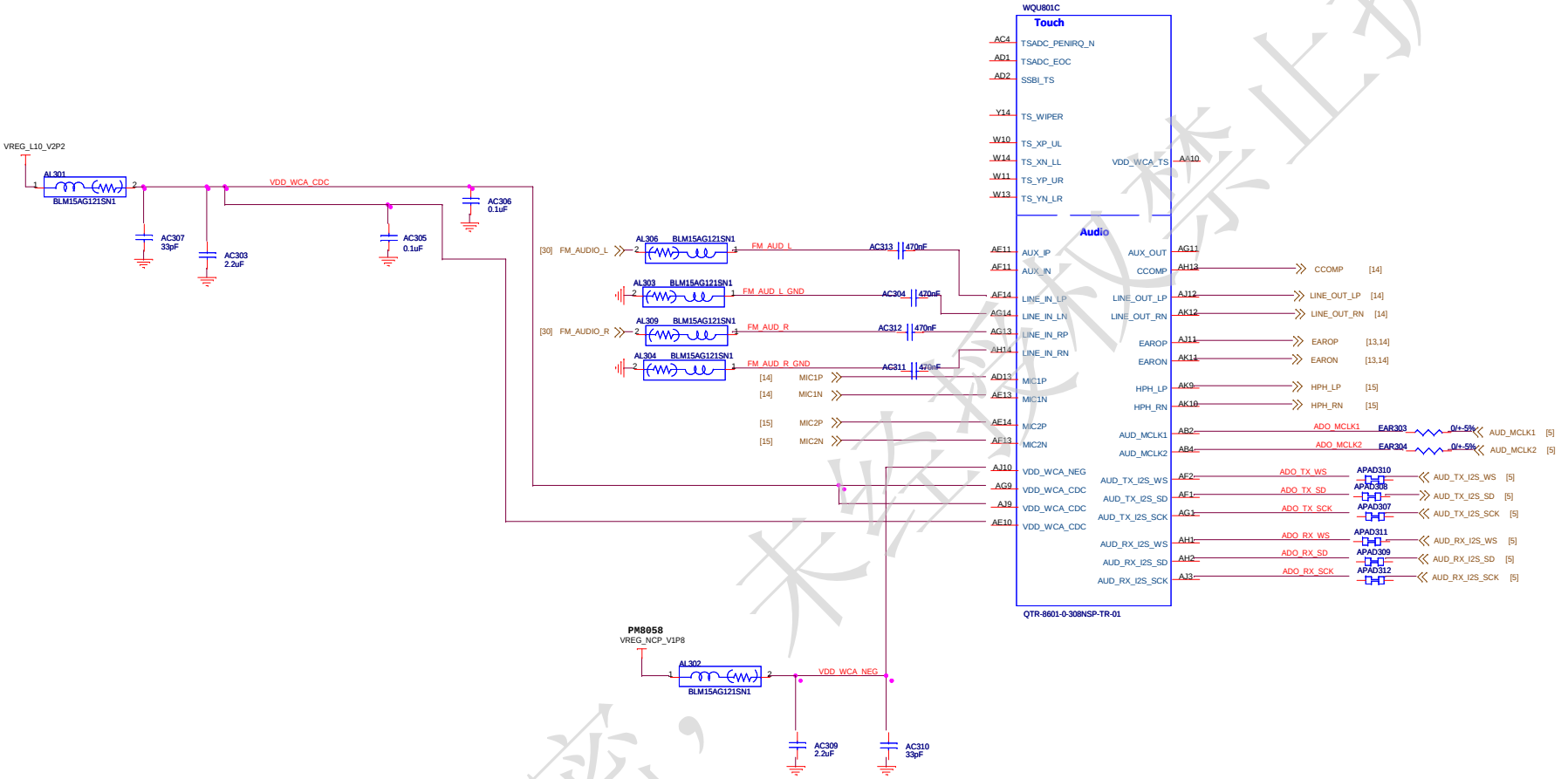

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Title	A03_Audio_CODEC	
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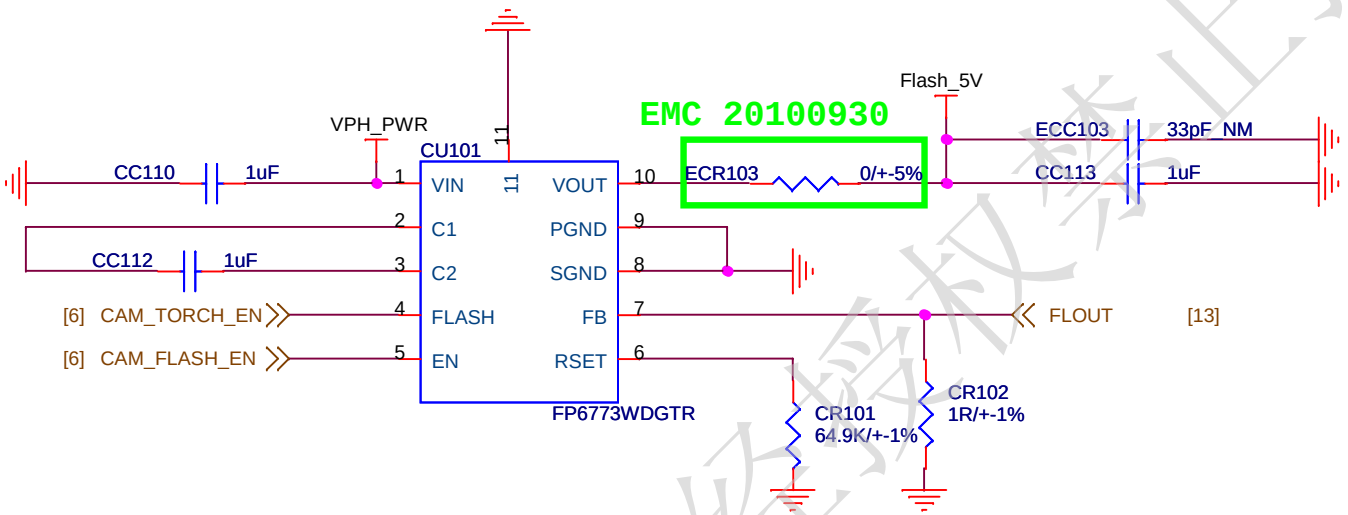
FLASH DRIVER



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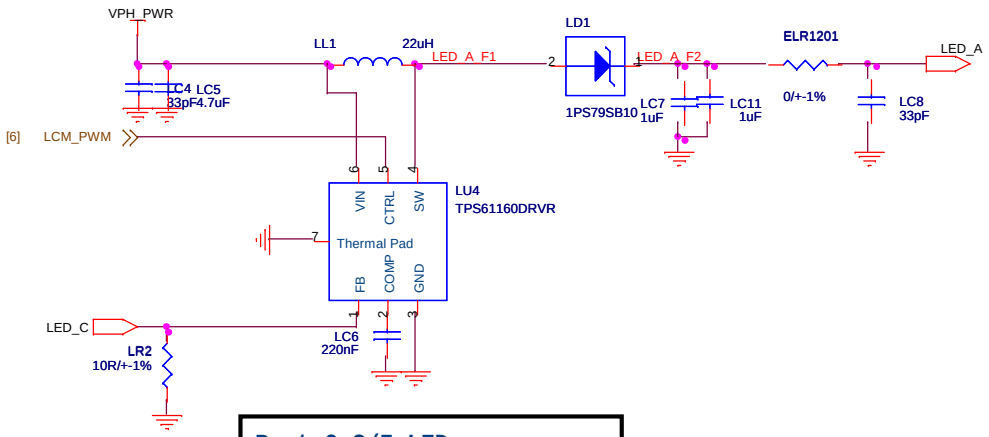
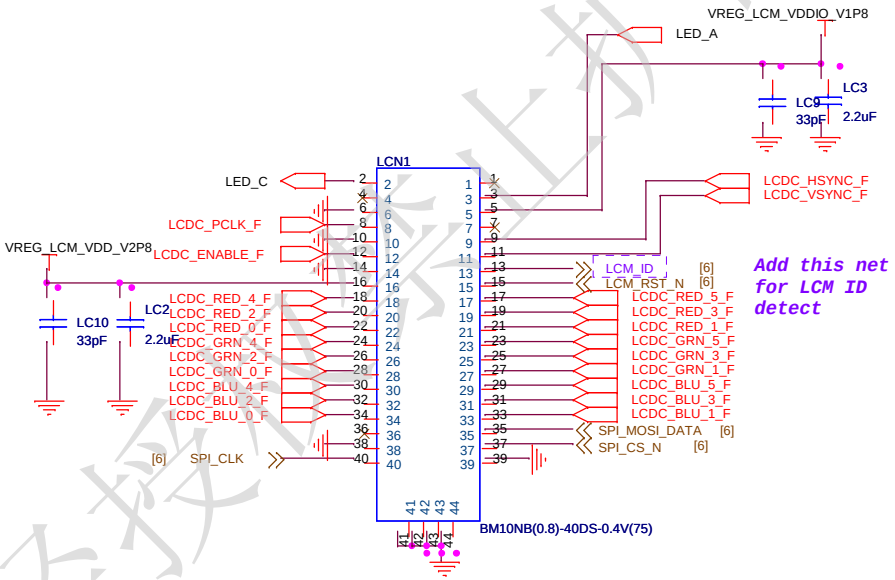


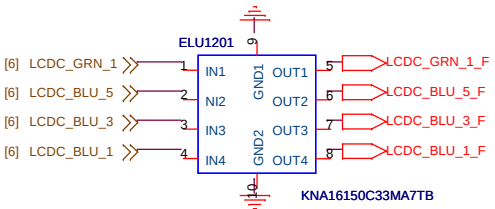
Rset=0.2/I_LED
I_LED=20mA, RSET=10 ohm

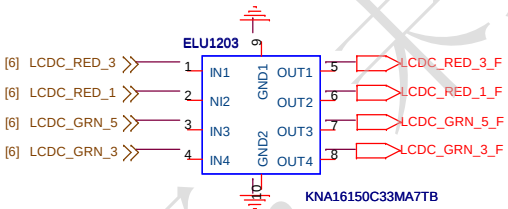
B/L_Boost_Driver IC_For 7 LED

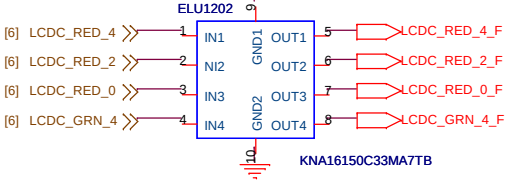


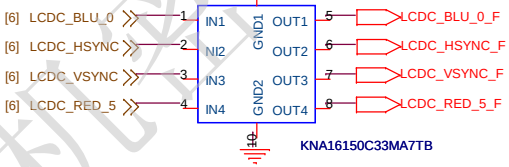
Add this net for LCM ID detect

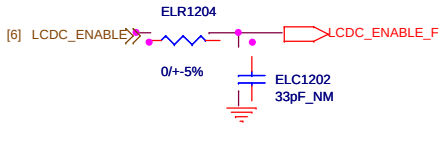
1. LED_PWM
2. LED-
3. LED+
4. NC
5. VDD
6. GND
7. MTP_2
8. DOTCLK
9. HSYNC
10. GND
11. VSYNC
12. ENABLE
13. ID0
14. GND
15. RESETB/ID1
16. AVDD
17. R5
18. R4
19. R3
20. R2
21. R1
22. R0
23. G5
24. G4
25. G3
26. G2
27. G1
28. G0
29. B5
30. B4
31. B3
32. B2
33. B1
34. B0
35. SPI_DI
36. NC
37. SPI_CS
38. GND
39. MTP_1
40. SPI_CLK

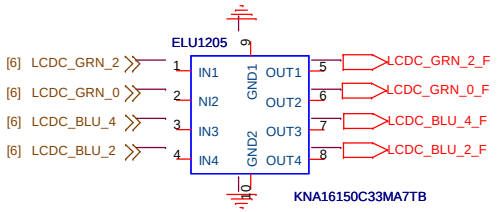








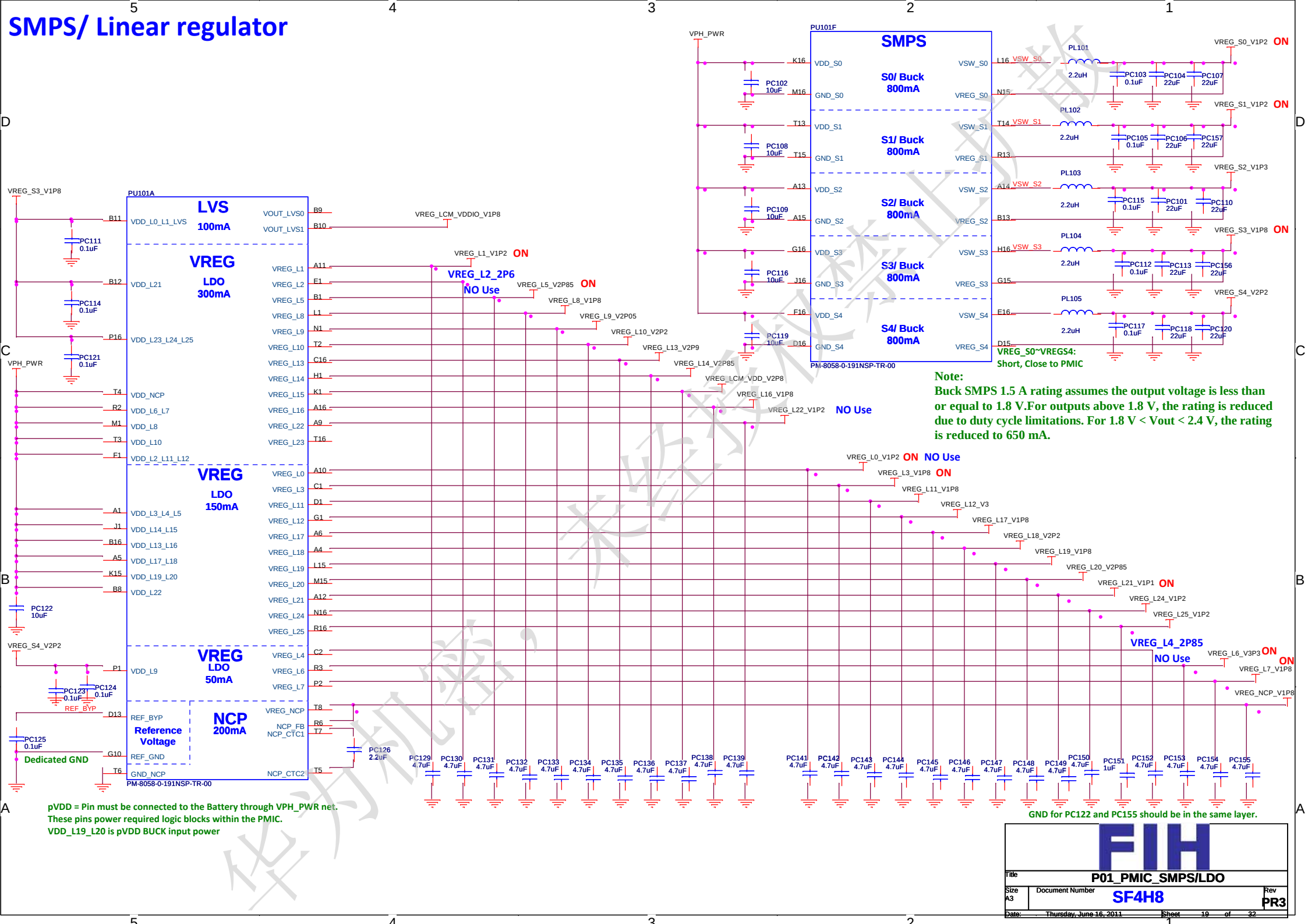




SONY_3.69"_LCM_Connector

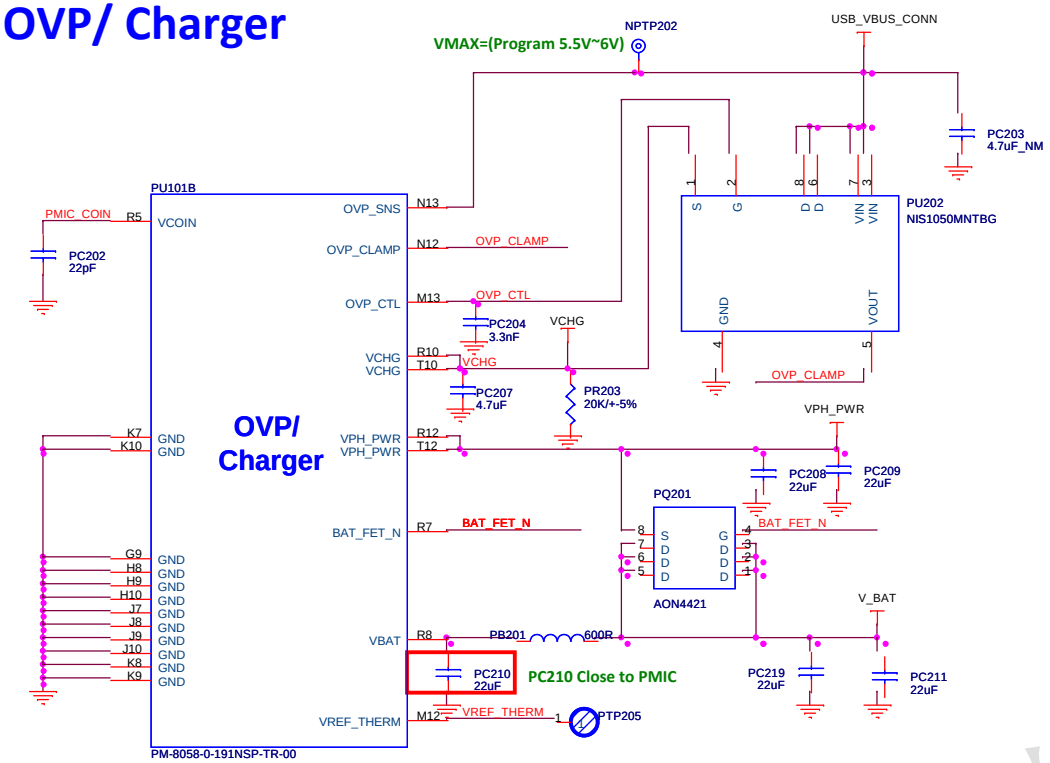
Title	L01_Display_3.69"_LCM	
Size B	Document Number SF4H8	Rev PR3
Date: Thursday, June 16, 2011	Sheet 18 of 32	

SMPS/ Linear regulator



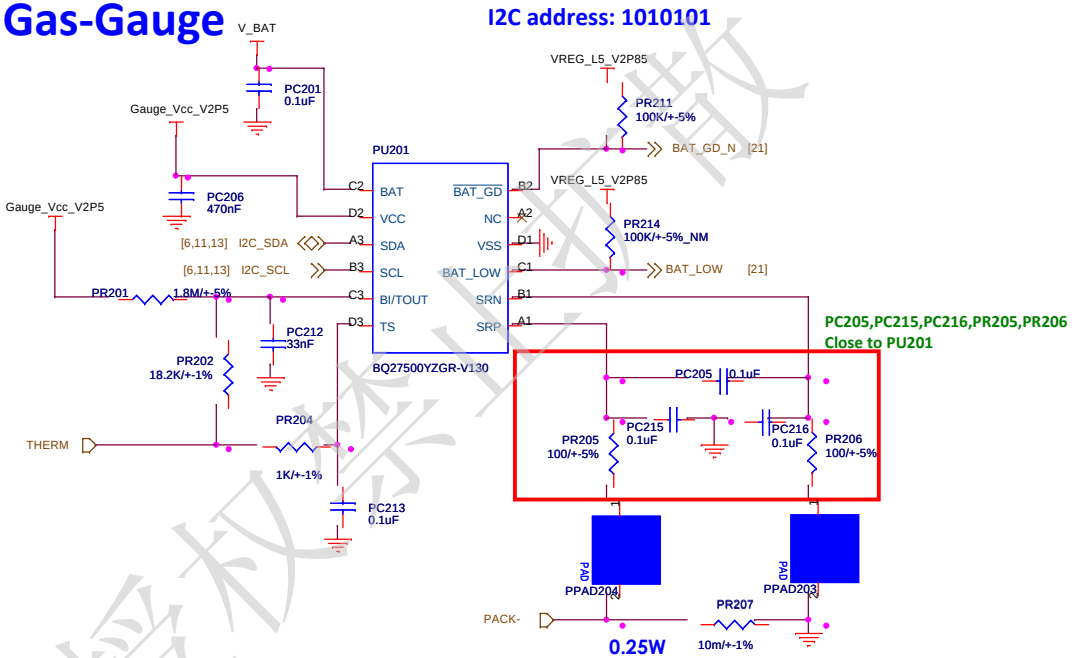
Title	P01_PMIC_SMPS/LDO
Size	A3
Document Number	SF4H8
Rev	PR3
Date:	Thursday, June 16, 2011
Sheet	19 of 32

OVP/ Charger

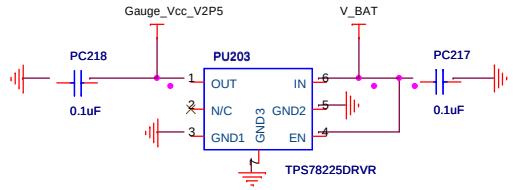


Gas-Gauge

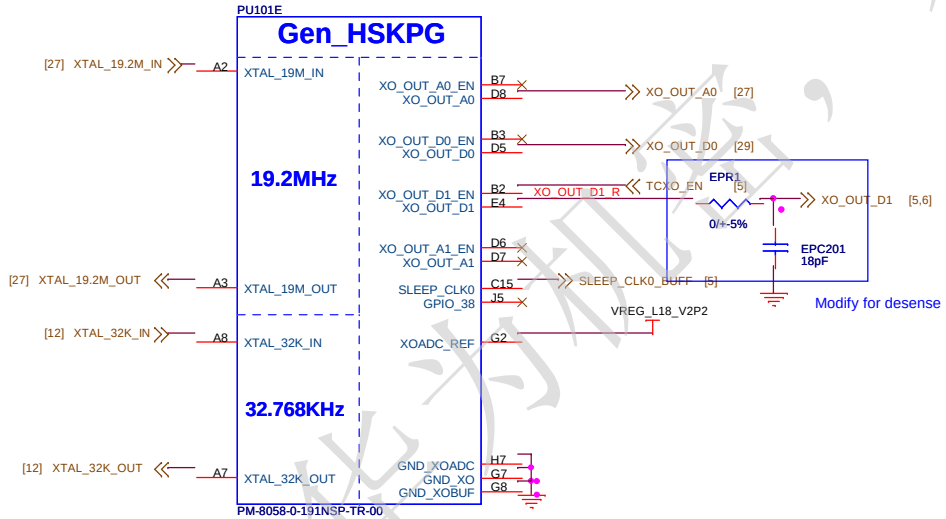
I2C address: 1010101



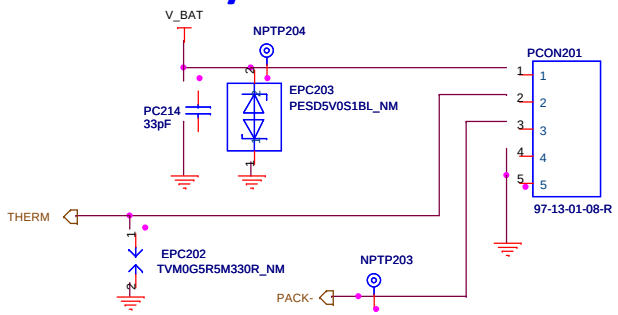
Gauge external power



General Housekeeping

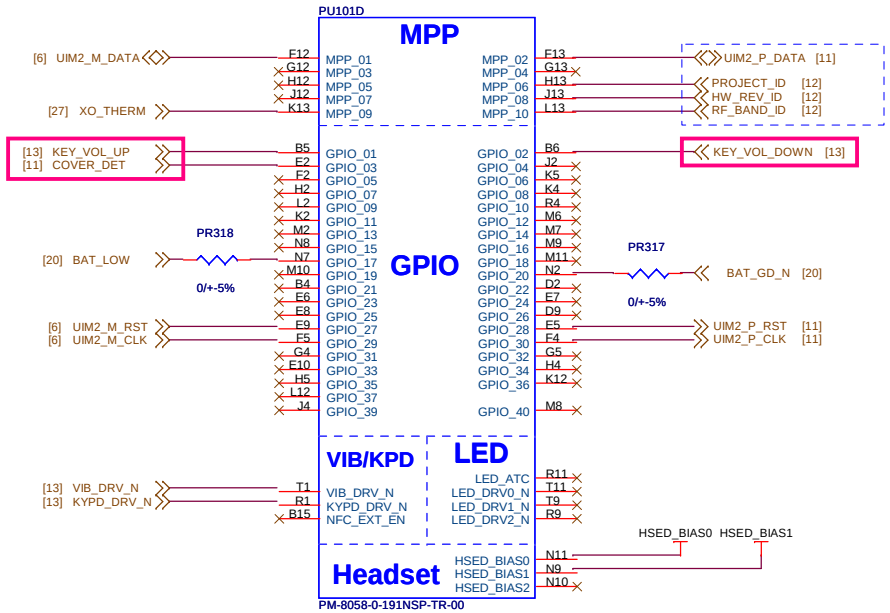


Battery Connector

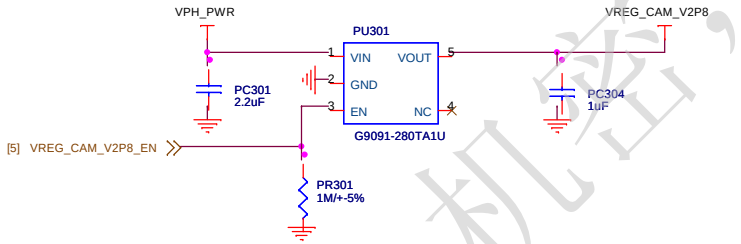


Title	P02_PMIC_Charger		
Size A3	Document Number SF4H8		Rev PR3
Date: Wednesday, June 29, 2011	Sheet 20 of 32		

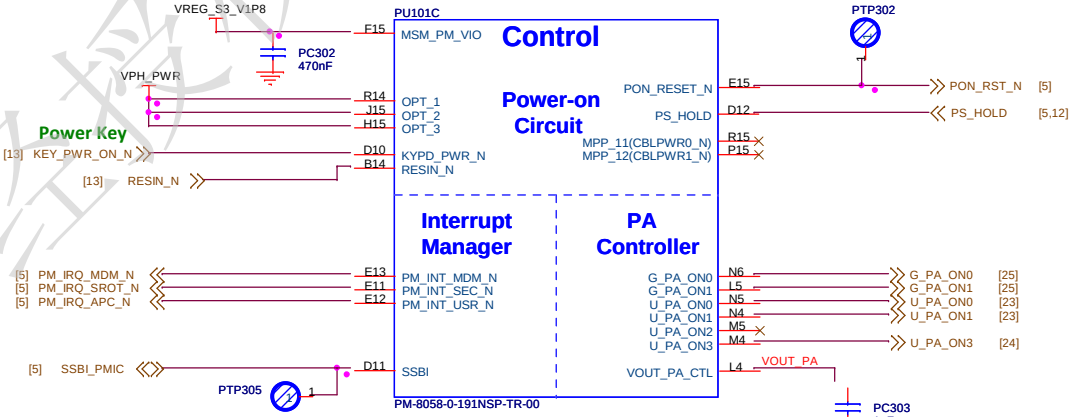
MPP/GPIO



Camera Power



Control



Title	Control/MPP/GPIO	
Size A3	Document Number SF4H8	Rev PR3
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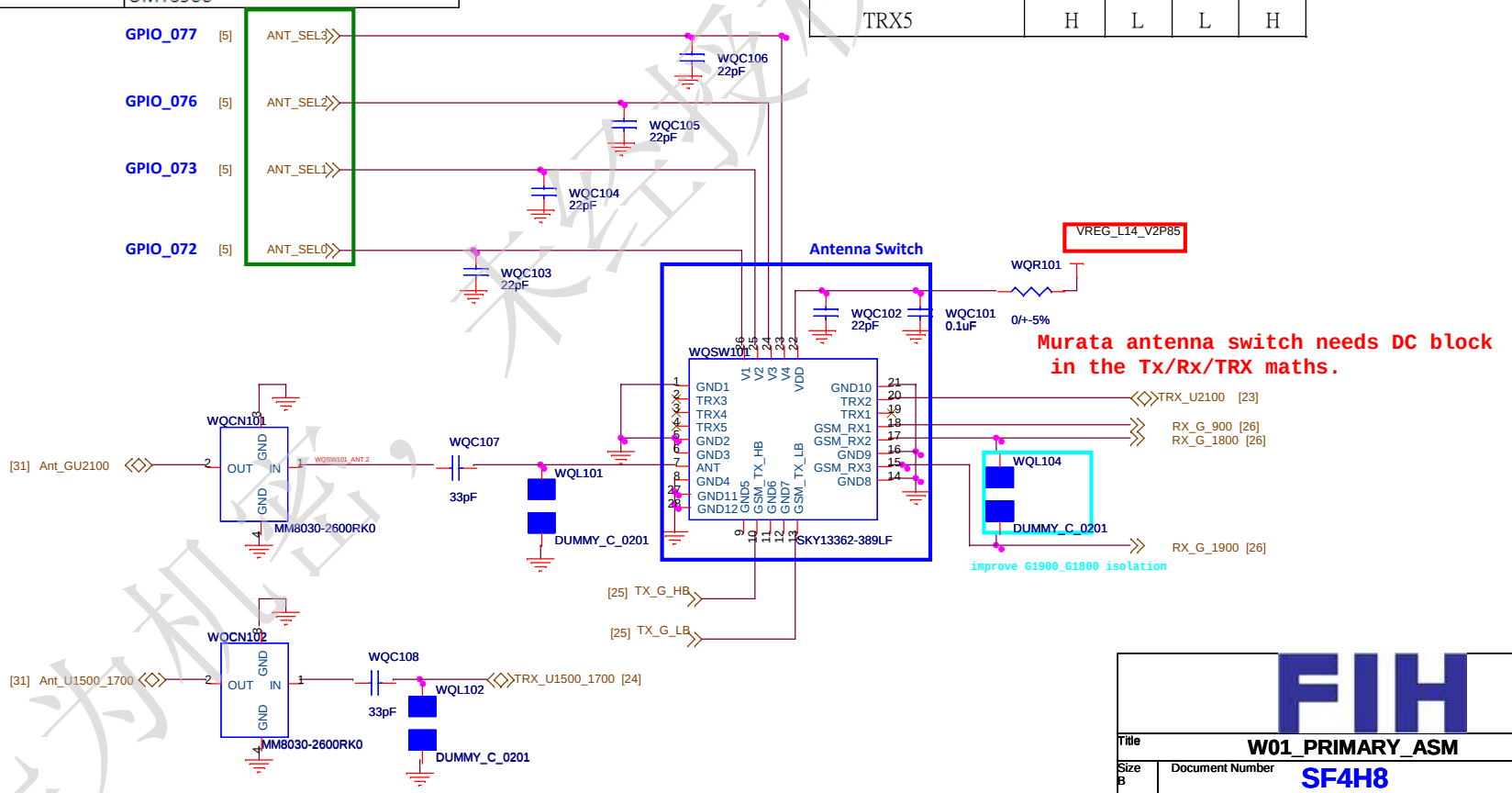
RX	GLOBAL	GLOBAL SUBSET C
QTR input		
PRX HB	AWS	AWS
PRX MB1	UMTS 2100	UMTS 2100
PRX MB2	UMTS 1900	UMTS 1900
PRX LB1	UMTS 850/GSM850	UMTS 900/GSM900
PRX LB2	UMTS900	
DRX MB1	GSM1800/1900(2:1 SAW)	GSM1800/1900(2:1 SAW)
DRX LB2	GSM900	GSM850
TX	**GLOBAL**	**GLOBAL SUBSET C**
TX_MB4	UMTS 2100	UMTS 2100
TX_MB3	UMTS 1900	UMTS 1900
TX_MB2	AWS	AWS
TX_MB1	GSM1800/GSM1900	GSM1800/GSM1900
TX_LB4	GSM850/GSM900	GSM850/GSM900
TX_LB3	UMTS900	
TX_LB1	UMTS850	UMTS900

Active Path	Vctrl			
	V1	V2	V3	V4
GSM LB Tx	H	H	L	L
GSM HB Tx	H	L	L	L
GSM_RX1(900)	L	L	H	L
GSM_RX2(1800)	L	H	H	L
GSM_RX3(1900)	L	H	L	L
TRX1	H	L	H	L
TRX2(U2100)	H	H	H	L
TRX3	H	L	H	H
TRX4(U1500/U1700)	H	H	H	H
TRX5	H	L	L	H



FIH

Title	W01_PRIMARY_ASM	
Size B	Document Number SF4H8	Rev PR3
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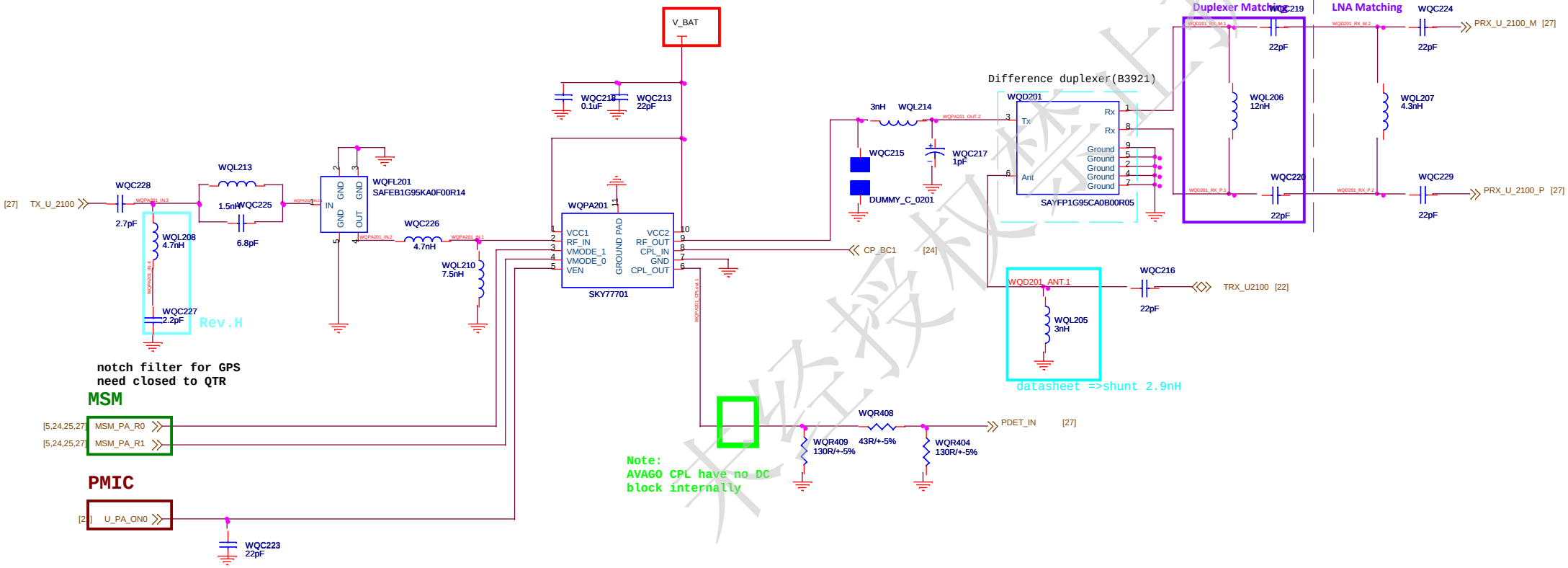
WCDMA TX CHAIN (BC1)



POWER MODE	PA_R1	PA_R0
HIGH POWER	L	L
MEDIUM POWER	L	H
LOW POWER	H	H

FIH

Title	W03_TX_CHAIN_BC1(Skyworks)	
Size: Custom	Document Number: SF4H8	Rev: PR3
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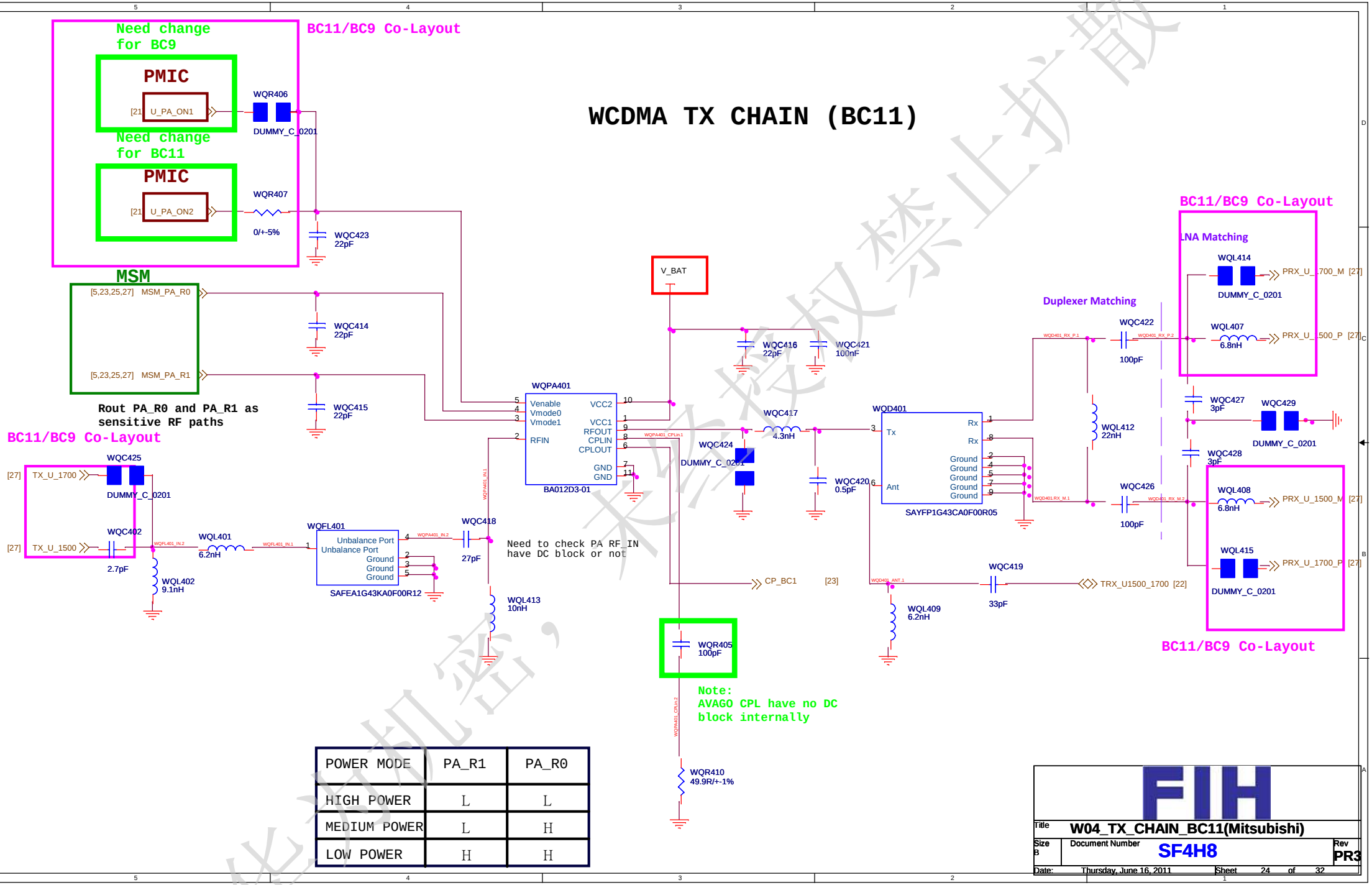
WCDMA TX CHAIN (BC11)



POWER MODE	PA_R1	PA_R0
HIGH POWER	L	L
MEDIUM POWER	L	H
LOW POWER	H	H

FIH

Title	W04_TX_CHAIN_BC11(Mitsubishi)	
Size B	Document Number SF4H8	Rev PR3
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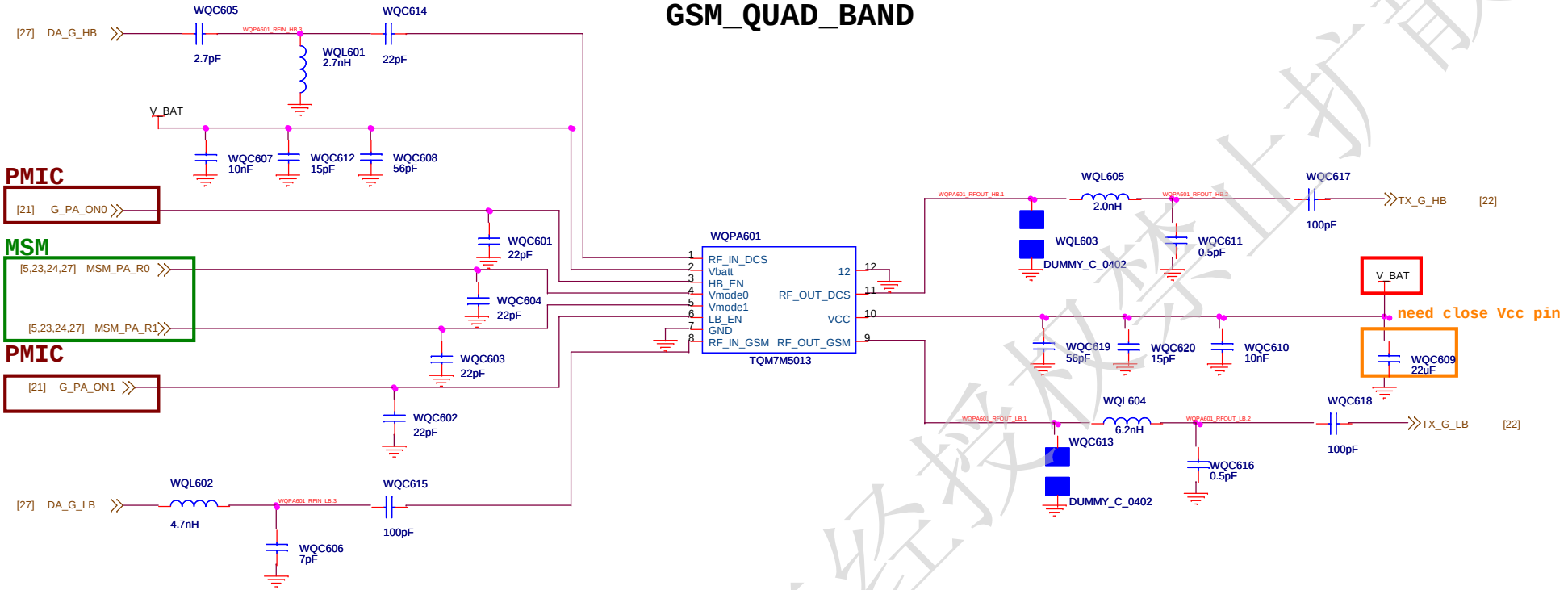
GSM_QUAD_BAND



MODE	PA_ON_G_LB	PA_ON_G_HB	PA_R0	PA_R1
Low band – High-power mode	H	L	L	L
Low band – Medium Power mode	H	L	L	H
Low band – Low-power mode	H	L	H	L
Low band – Ultra-Low-power mode	H	L	H	H
High band – High-power mode	L	H	L	L
High band – Low-power mode	L	H	H	L
High band – Ultra-Low-power mode	L	H	H	H

FIH

Title	W06_GSM_TX_QUAD_BAND_PA	
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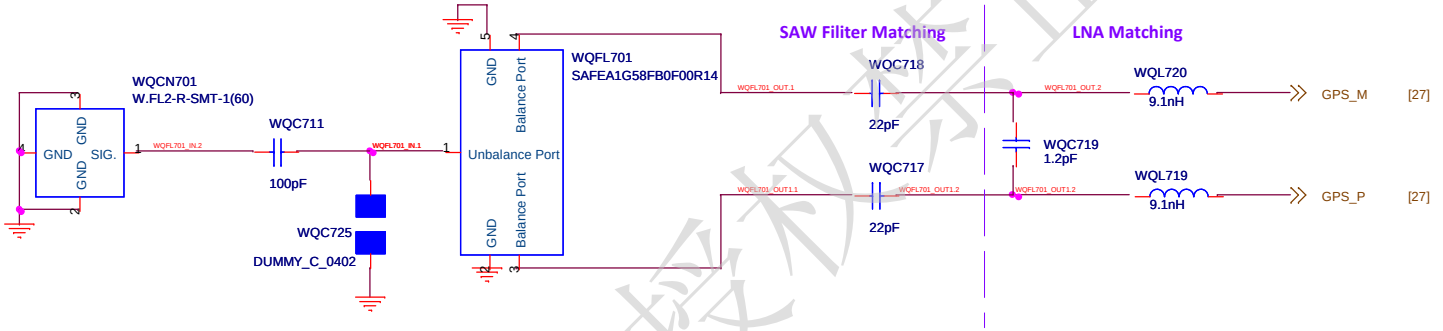
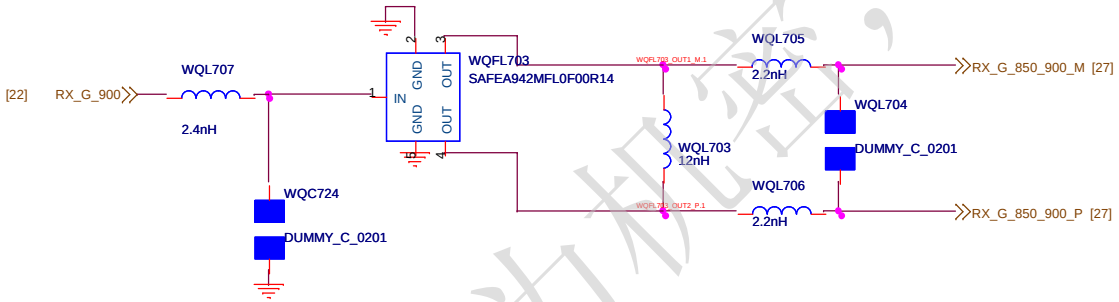
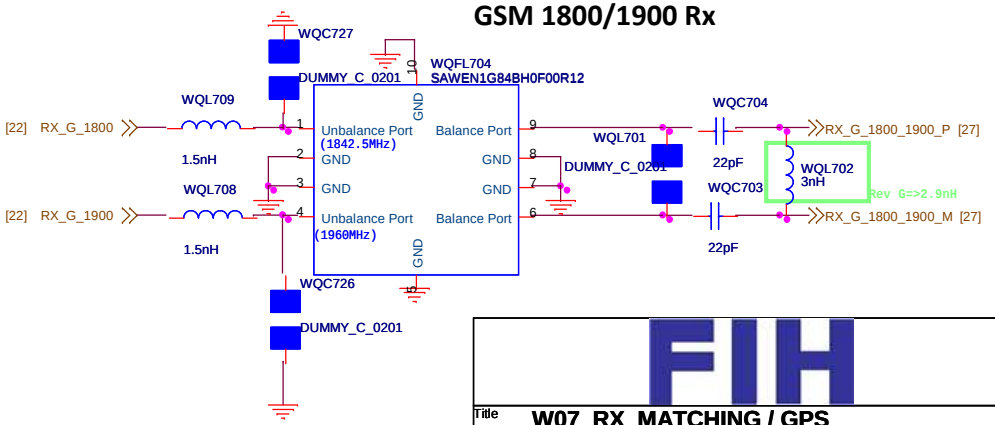
GPS RX CHAIN (Close to GPS antenna)



GSM 900 Rx



GSM 1800/1900 Rx



FIH

Title	W07_RX_MATCHING / GPS	
Size B	Document Number SF4H8	Rev PR3
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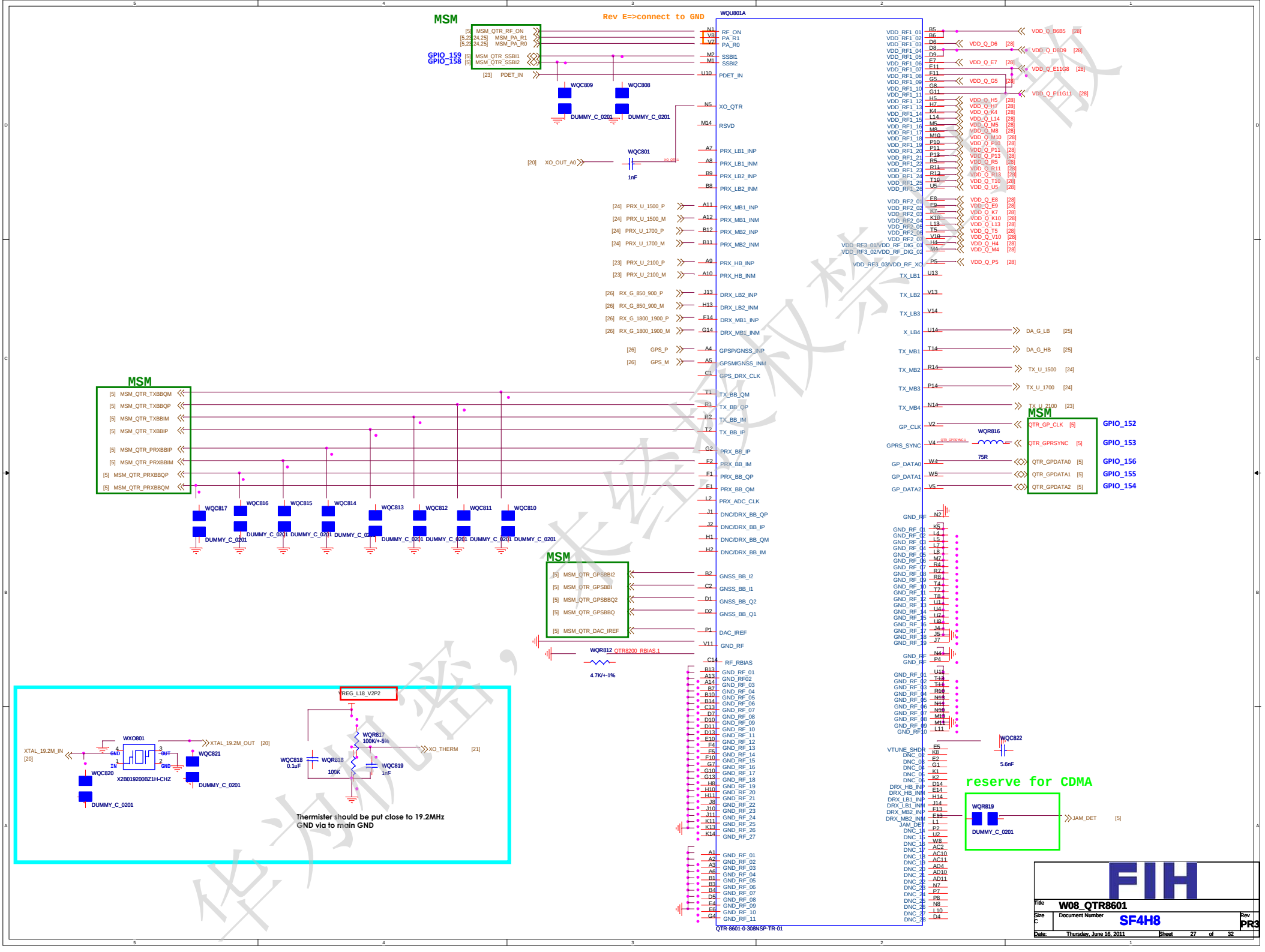
MSM
Rev E=>connect to GND
WQU801A
RF_ON
PA_R1
PA_R0
SSBI1
SSBI2
PDET_IN
XO_QTR
RSVD
PRX_LB1_INP
PRX_LB1_INM
PRX_LB2_INP
PRX_LB2_INM
PRX_MB1_INP
PRX_MB1_INM
PRX_MB2_INP
PRX_MB2_INM
PRX_HB_INP
PRX_HB_INM
DRX_LB2_INP
DRX_LB2_INM
DRX_MB1_INP
DRX_MB1_INM
GPSP/GNSS_INP
GPSM/GNSS_INM
GPS_DRX_CLK
TX_BB_QM
TX_BB_QP
TX_BB_IM
TX_BB_IP
PRX_BB_IP
PRX_BB_IM
PRX_BB_QP
PRX_BB_QM
PRX_ADC_CLK
DNC/DRX_BB_QP
DNC/DRX_BB_IP
DNC/DRX_BB_QM
DNC/DRX_BB_IM
GNSS_BB_I2
GNSS_BB_I1
GNSS_BB_Q2
GNSS_BB_Q1
DAC_IREF
GND_RF
RF_RBIAS
GND_RF_01
GND_RF02
GND_RF_03
GND_RF_04
GND_RF_05
GND_RF_06
GND_RF_07
GND_RF_08
GND_RF_09
GND_RF_10
GND_RF_11
GND_RF_12
GND_RF_13
GND_RF_14
GND_RF_15
GND_RF_16
GND_RF_17
GND_RF_18
GND_RF_19
GND_RF_20
GND_RF_21
GND_RF_22
GND_RF_23
GND_RF_24
GND_RF_25
GND_RF_26
GND_RF_27
GND_RF_01
GND_RF_02
GND_RF_03
GND_RF_04
GND_RF_05
GND_RF_06
GND_RF_07
GND_RF_08
GND_RF_09
GND_RF_10
GND_RF_11
QTR-8601-0-308NSP-TR-01
VDD_RF1_01
VDD_RF1_02
VDD_RF1_03
VDD_RF1_04
VDD_RF1_05
VDD_RF1_06
VDD_RF1_07
VDD_RF1_08
VDD_RF1_09
VDD_RF1_10
VDD_RF1_11
VDD_RF1_12
VDD_RF1_13
VDD_RF1_14
VDD_RF1_15
VDD_RF1_16
VDD_RF1_17
VDD_RF1_18
VDD_RF1_19
VDD_RF1_20
VDD_RF1_21
VDD_RF1_22
VDD_RF1_23
VDD_RF1_24
VDD_RF1_25
VDD_RF1_26
VDD_RF2_01
VDD_RF2_02
VDD_RF2_03
VDD_RF2_04
VDD_RF2_05
VDD_RF2_06
VDD_RF2_07
VDD_RF3_01/VDD_RF_DIG_01
VDD_RF3_02/VDD_RF_DIG_02
VDD_RF3_03/VDD_RF_XO
TX_LB1
TX_LB2
TX_LB3
X_LB4
TX_MB1
TX_MB2
TX_MB3
TX_MB4
GP_CLK
GPRS_SYNC
GP_DATA0
GP_DATA1
GP_DATA2
GND_RF
VTUNE_SHDR
DRX_HB_INP
DRX_HB_INM
DRX_LB1_INP
DRX_LB1_INM
DRX_MB2_INP
DRX_MB2_INM
JAM_DET
WQC809
WQC808
WQC801
WQC817
WQC816
WQC815
WQC814
WQC813
WQC812
WQC811
WQC810
WQC820
WQC821
WQC822
WQR812 QTR8200_RBIAS.1
4.7K/+-1%
WQR816
75R
WQR817
100K/+-5%
WQC818
0.1uF
WQR818
100K
WQC819
1nF
5.6nF
WQR819
DUMMY_C_0201
1nF
WXO801
X2B019200BZ1H-CHZ
XTAL_19.2M_IN
XTAL_19.2M_OUT
XO_THERM
VREG_L18_V2P2
Thermister should be put close to 19.2MHz
GND via to main GND
reserve for CDMA
GPIO_152
GPIO_153
GPIO_156
GPIO_155
GPIO_154
FIH
W08_QTR8601
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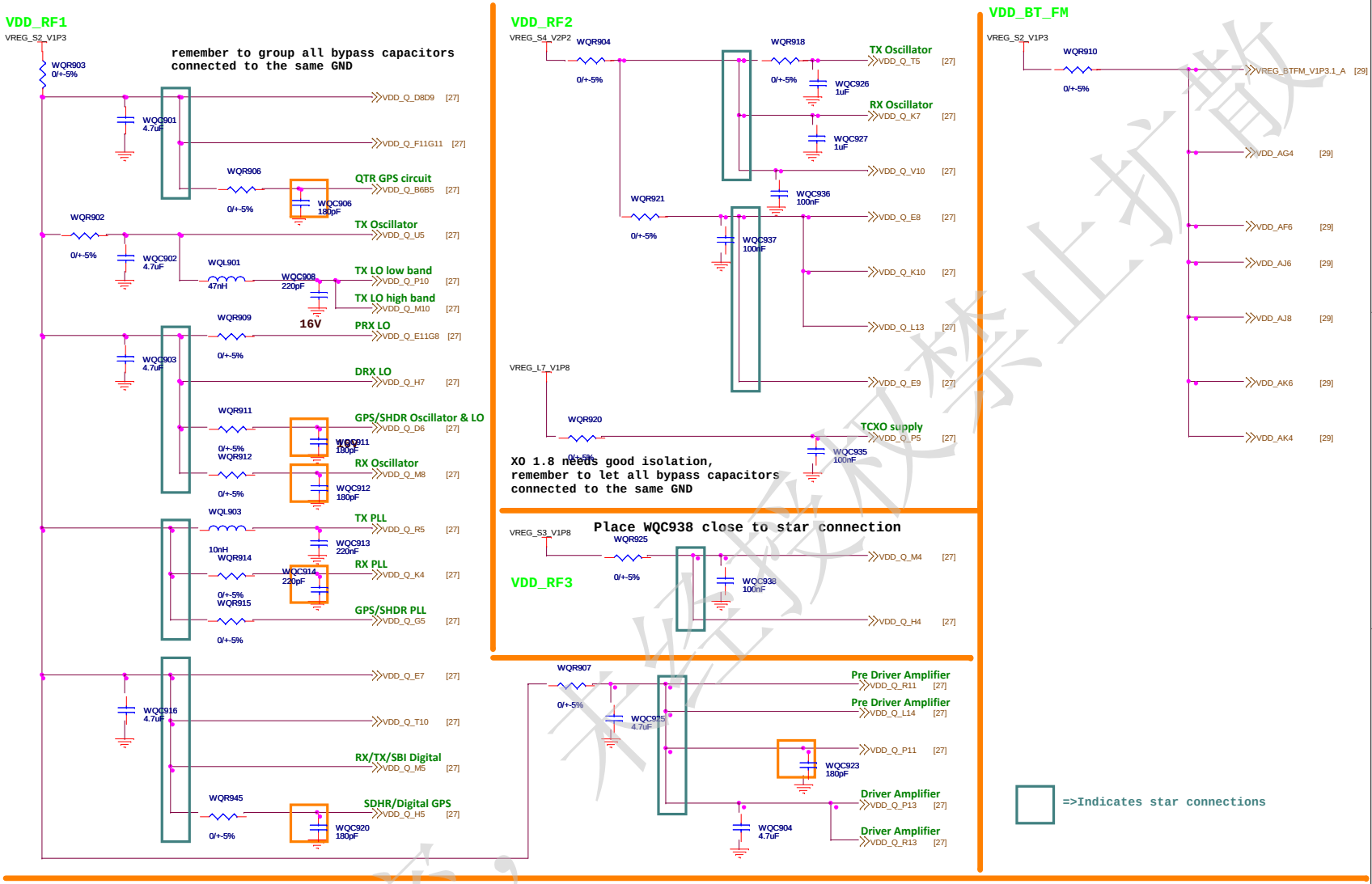

Sensitive RF Supply Pins - See next schematic page

Description	Pin #	Noise Generator	Noise Sensitive	Decoupling Purpose	Priority
TX Oscillator	T5, U5	Yes (RF harmonics)	Yes (most sensitive)	Noise Suppression	First
RX Oscillator	K7, M8	Yes (RF harmonics)	Yes (most sensitive)	Noise Suppression	First
GPS/SHDR Oscillator & LO	D6	Yes (RF harmonics)	Yes	Noise Suppression	First
RX PLL	K4	Yes (2nd aggressor)	Yes (2nd sensitive)	Noise Suppression	First
TX PLL	R5	Yes (2nd aggressor)	Yes (2nd sensitive)	Noise Suppression	First
GPS/SHDR PLL	G5	Yes (2nd aggressor)	Yes (2nd sensitive)	Noise Suppression	First
RX/TX/SBI Digital	M5	Yes (1st aggressor)	No	Noise Suppression	First
SDHR/Digital GPS	H5	Yes (1st aggressor)	No	Noise Suppression	First
TCXO Supply	P5	Yes (1st aggressor)	Yes (most sensitive)	TCXO Harmonic Suppression, improves PLL ref clock noise	First
Driver Amplifier	P13, R13	Yes (RF harmonics)	Yes	Improves Tx fundamental/harmonic, RX band noise/emissions	Third
Pre Driver Amplifier	L14, R11	Yes (RF harmonics)	Yes	Improves TX Path Stability, fundamental/harmonic, RX band noise/emissions	Third
PRX LO	E11, G8	No	Yes	Improves RX blocking, integrated phase noise, TX IM2	Second
DRX LO	H7	No	Yes	Improves RX blocking, integrated phase noise, TX IM2	Second
TX LO	P10, M10	No	Yes	Improves RX band noise/emissions	Second

NOTE: For single-sided board designs, first priority decoupling must be placed closest to the QTR device corresponding pins. Second priority decoupling can be placed after all first priority placements, and so on.

FIH

Title: W09_QTR8601_PWR

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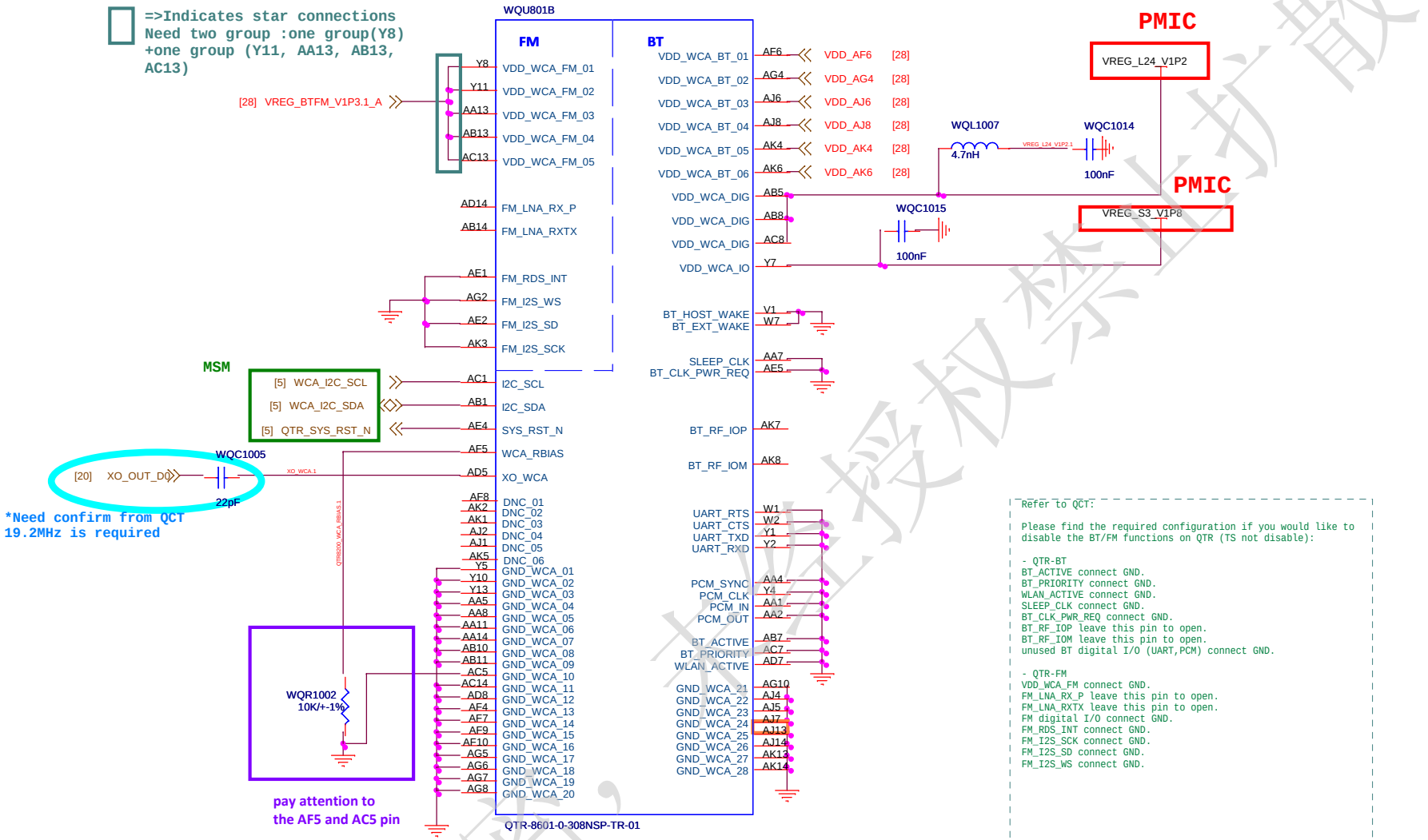

1.Place WQC1010 and WQC1009 next to BALUN for common mode rejection
2. Pin AJ13 need through "VIA" connect to main ground independently and the trace width=10 mil

Title	W10_QTR8601_WCA	
Size B	Document Number SF4H8	Rev PR3
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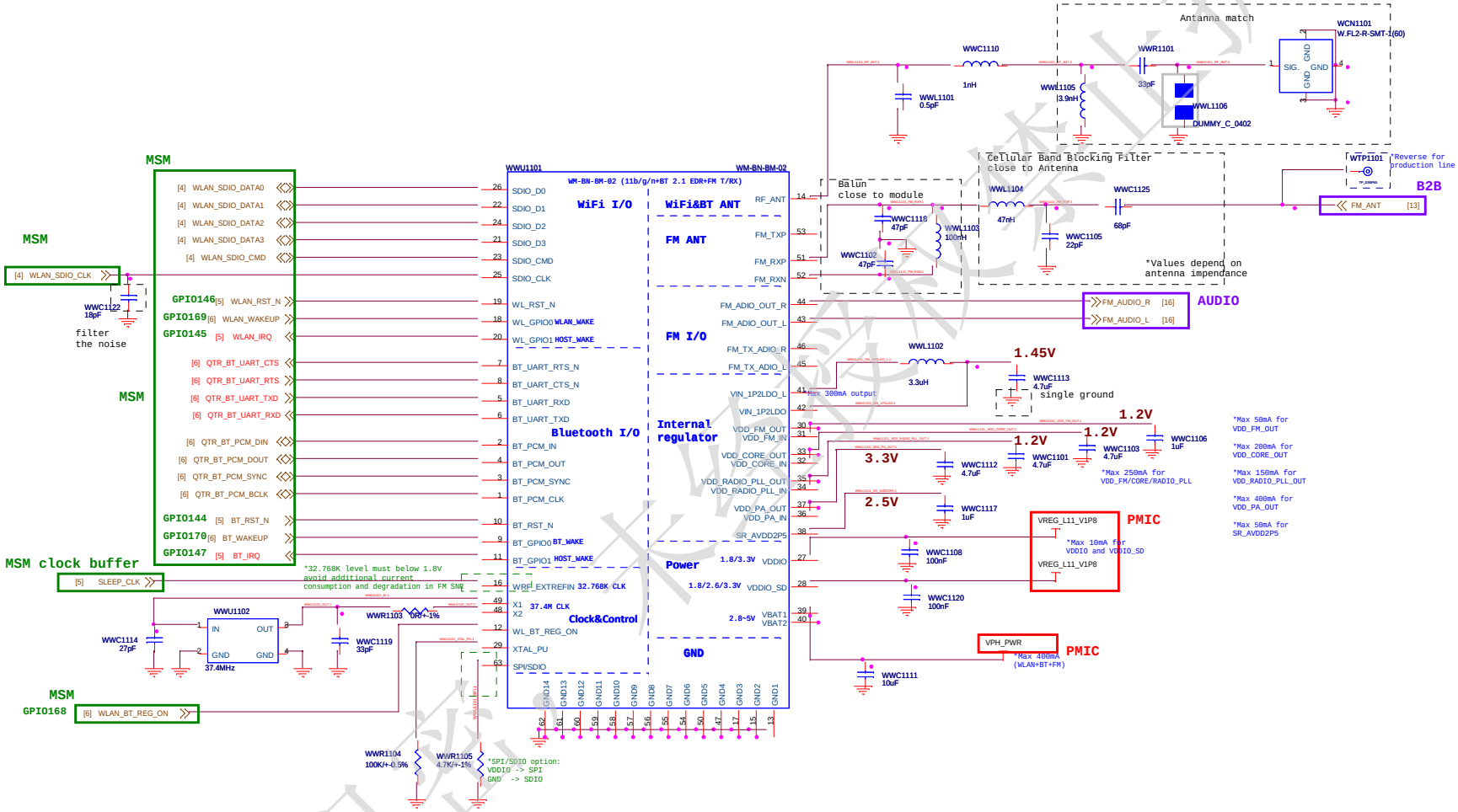

FIH

Title	W11_WLAN/BT/FM_USI(WM-BN-BM-02)
Size C	Document Number SF4H8
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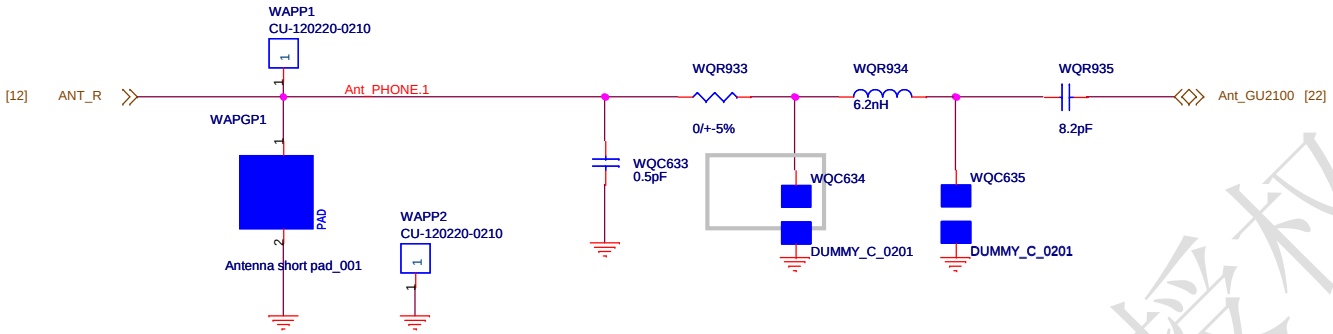
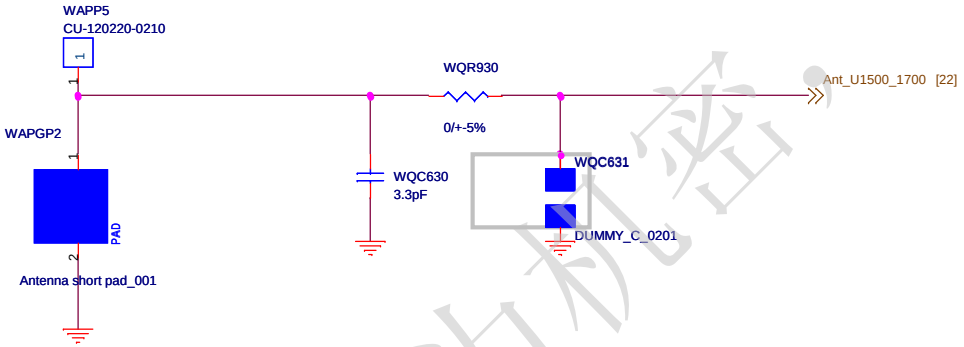
Phone Antenna



U1500_1700 Antenna



Title	W12_Antenna Page	
Size B	Document Number SF4H8	Rev PR3
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Date	Sheet	Contents	Remark
2011/02/21	04	Add R404 pull high to VREG_S3_V1P8 ; Remove GPIO40: GS_INT	
	13	Change R1301.2 pull up to VREG_S3_V1P8 , CN1303.3 connect to VREG_S3_V1P8	
		Add CN1301.5: MODULE_ID	
		ECN1301換料, SC-346 change to SQ-31G.	
		EU1301換料, NFA18SL307V1A45L change to KNA16150C33MA5TS.	
	C01	Change CR101 to 62K Ohm	
	12	R1207 change to 18K ohm ; Remove C1202 , C1203 ; X1201換料 爲 P/N:Q13FC1350000200	
	06	Add GPIO_142: GS_INT ; GPIO172:Module_ID ; GPIO173:CAM_RST_N ; GPIO174:CAM_VGA_PWDN	
		Remove GPIO8: CAM_VGA_PWDN , GPIO1: CAM_RST_N	
		Change NET:CAM_I2C_SCL , CAM_I2C_SDA pull up to VREG_S3_V1P8	
	L01	change the manufacturer of ELU1021~1205 from murata to kyocera	
	P02	Change PR208 to PB101 ; change PC210 from 4.7uF to 22uF ; Add PC219	
2011/02/23	10	Change eMMC to P/N: SDIN5D2-2G-T ; Add net: RST_OUT_V1P8	
	5	Add NET:RST_OUT_V1P8	
2011/02/24	10	Change R1001~R1009 to 10K ohm	
	W03	Add WQF1201.	
	W04	Change WQC418 to 27pF, WQL413 to 10nH,	
		WQC417 to 4.3nH, WQC420 to 0.5pF	
	W05	Remove WQR601, WQR602, WQR603, WQR604, WQR605, WQR606.	
	5	C501 , C502 change to 18pF	
2011/02/27	W12	Change WQC633 to 1.3pF, WQR933 to 0 ohm,	
		WQR934 to 2.4pF, WQR935 to 5.6nH, WQC630 to 3.3pF	
	12	Remove CN1204	
2011/03/01	P02	Change PU203 to P/N:TPS78225DRVR	
2011/03/02	12	Change CN1201 to P/N:8195-7505-AK81	
	A01	Change AC107 to Ni ; Modify value of AC108 to 4.7uF.	
2011/03/03	06	Change NET:SPI_CS_N from GPIO46 to GPIO48	
	12	Change CN1201 to P/N:8195-7505-BK71	
2011/03/04	P02	Change PB101 to PB201 ; Change PC207 on board	
	W11	change WWL1101 to 0.5pF ; WWC1110 to 1nH ; WWL1105 to 3.9nH ; WWR1101 to 33pF	
2011/05/16	A01	Change AC107 and AC108 to 4.7uF	
		Remove AL101 and net SPK_VDD	
	L01	ELC1201 改爲上件	
2011/05/17	W03	Change WQC226 to 4.7nH, WQL210 to 7.5nH	
	W12	Change WQC633 to 0.5pF, WQR934 to 6.2nH,	
		WQC635 to NI, WQR935 to 8.2pF	

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Changed List

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