DATA BOOK

O A K
HORIZON
CHIP SET
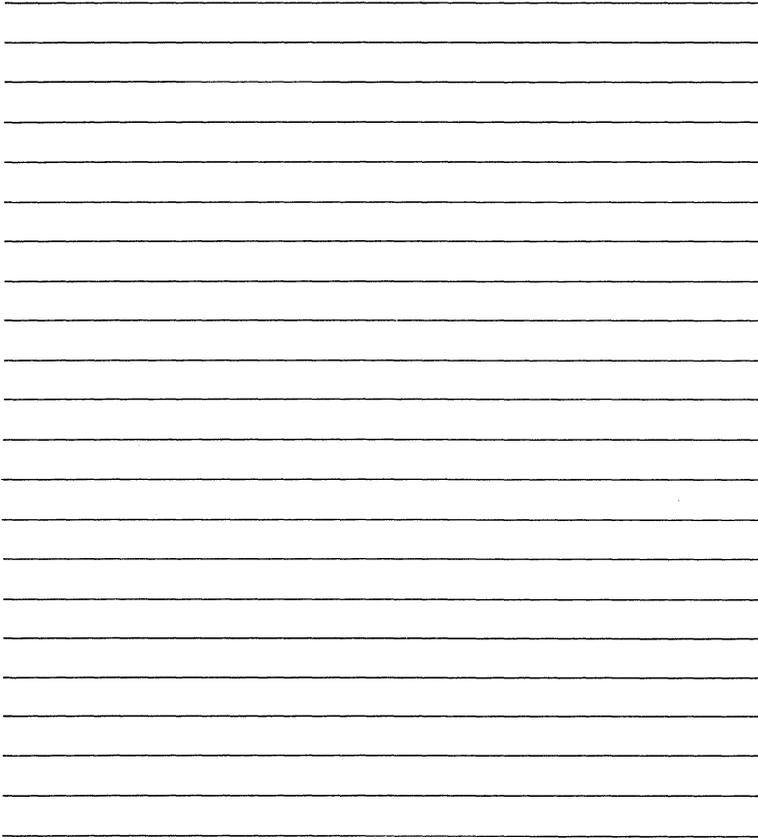LAPTOP AND DESKTOP

OAK TECHNOLOGY, INC.

OakHorizon™ CHIP SET

DATA MANUAL

November 1, 1989

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CONTENTS

OakHorizon CHIP SET DATA MANUAL   **PAGE NUMBER**

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SYSTEM OVERVIEW

The OakHorizon chip set is a highly integrated core logic chip set designed to support IBM-compatible systems based on the 80286 and 80386SX processors. Two versions of the chip set are available. The OTI-050LAP is specifically designed for use in battery powered systems and includes the OTI-055 power manager chip. For desktop and other AC-powered applications, the OTI-050DESK chip set provides the same high performance as the laptop version without the need for the OTI-055 power manager.

The OakHorizon chip set includes the following chips:

- OTI-051: System Support Logic

- OTI-052: I/O Control Logic

- OTI-053: DMA and Memory Controller

- OTI-054: Address Buffer/Real Time Clock/CMOS RAM

- OTI-055: Data Buffer and Power Manager
  (Only needed for battery powered systems.)

OTI-051 integrates all the system support logic functions.

- Supports 80286 as well as 80386SX processors

- Command cycle controller generates memory and I/O cycles with programmable normal and fast timing

- Address and data path control that also supports bus conversion for 16 bit to sequential 8 bit operation of memory and I/O cycles

- Supports fast reset to switch from protected mode to real mode

- Timeout counter to prevent I/O devices from hanging the system

- NMI generation logic

- Memory parity checker and generator

- Power management scheme for LAPTOP system design

OTI-052 integrates I/O devices.

- 8254 compatible timer/counter

- One 16C450 compatible serial communication controller

- Parallel port controller

- Two 8259 compatible interrupt controllers

- Chip select logic for serial/parallel ports, disk controllers, video controller

- Co-processor interface

OTI-053 integrates the DMA controller and memory controller functions.

- Memory timing generator, refresh cycle generator, memory segment allocation control, EMS logic that supports EMS 4.0 specifications

- Bus arbiter arbitrates the system bus between the CPU, DMA, and DRAM memory refresh cycle

- Two 82C37 DMA controllers running up to 12.5 MHz

- DMA support logic provides 7 channels of DMA page map address, burst mode DMA

OTI-054 integrates all the TTL address buffers, a Real Time Clock and CMOS RAM.

- Integrates address buffers on the system board

- 146818 compatible real-time clock with 128 bytes of CMOS RAM

OTI-055 integrates all the TTL data buffers and the power manager.

- Integrates data buffers on the system board

- 16 general purpose user programmable bidirectional control/status pins

- Automatic wakeup timer/counter

- NMI logic

- Battery level inputs

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SECTION 1

OTI-051

SYSTEM SUPPORT LOGIC

1.0 INTRODUCTION TO THE OTI-051 SYSTEM CONTROLLER

OTI-051 is a custom integrated circuit designed for the OakHorizon chip set running with 80286 and 80386SX microprocessors. The chip provides all the system support logic for the system. It integrates all the functions of CPU interface and data flow control.

A summary of the special features provided by OTI-051 is listed below.

System Control: - Supports 8 MHz, 10 MHz, 12.5 MHz, 16 MHz and 20 MHz system speeds

I/O Channel: - Asynchronous mode: 8 MHz independent of system speed
   - Synchronous mode: 8, 10 or 12.5 MHz dependent on the system speed
   - Programmable wait states

Laptop Support: - Power management scheme

Misc: - Fast RESET
   - Timeout Counter

System Block Diagram
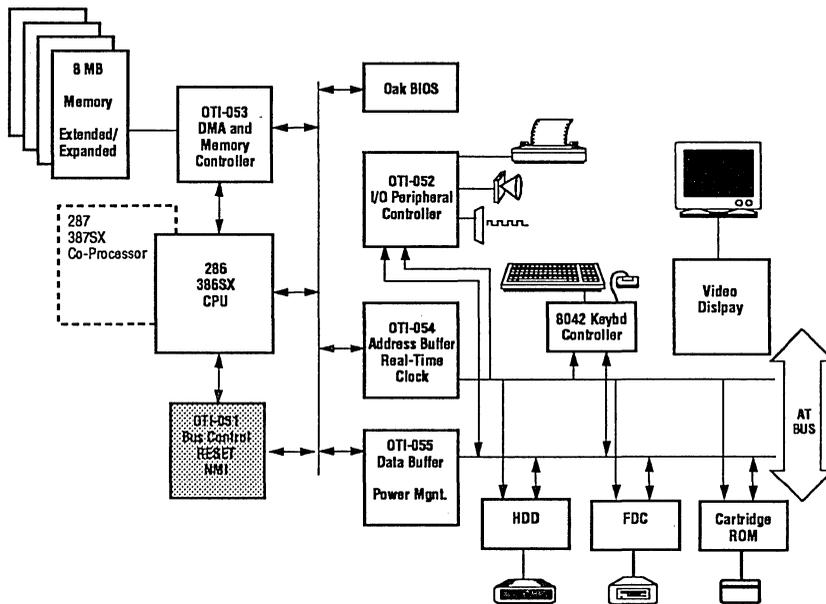
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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-051 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
			*** CPU INTERFACE ***
SA23 - SA0	68-62,60-44	I	ADDRESS BUS: These are address bus lines corresponding to A23-A0 of the 80286/80386SX and 80287/80387SX bus. OTI-051 monitors these lines when the CPU or co-processor is in control of the bus.
SD15 - SD0	98-95,93-91 89-81	I/O	DATA BUS: These are the bidirectional data bus lines corresponding to D15-D0 of the 80286/80386SX CPU.
S0-/WR- S1-/DC	77 78	I	BUS CYCLE STATUS: These signals together with M/IO and COD/INTA- are used to decode different bus cycles.

80286 Bus Cycle Status Definition*				
COD/INTA	M/IO	S1	S0	Bus Cycle Initiated
0 (Low)	0	0	0	Interrupt acknowledge
0	0	0	1	Will not occur
0	0	1	0	Will not occur
0	0	1	1	None; not a status cycle
0	1	0	0	IF A1=1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status signal
1 (High)	0	0	0	Will not occur
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Will not occur
1	1	0	1	Memory instruction read
1	1	1	0	Will not occur
1	1	1	1	None; not a status signal

80386SX Bus Cycle Status Definition*			
M/IO	D/C#	W/R #	Bus Cycle Type
0	0	0	Interrupt Acknowledge
0	0	1	Will not occur
0	1	0	I/O Data Read
0	1	1	I/O Data Write
1	0	0	Memory Code Read
1	0	1	Halt: Shutdown Address = 2 Address = 1 (BE0# 1 (BE0# 0 BE1# 1 BE1# 1 BE2# 0 BE2# 1 BE3# 1 BE3# 1 A2-A31 0) A2-A31 0)
1	1	0	Memory data read
1	1	1	Memory data write

* For more information on CPU bus cycle status, refer to the CPU databook.

M/IO-	79	I	MEMORY OR I/O CYCLE: is an input signal from the CPU indicating whether the present cycle is memory or I/O access.

Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
SRDY-	80	I/O	SYSTEM READY: is an active low signal to acknowledge to the CPU that a data transfer for either memory or I/O is complete.
ADS-	76	I	ADDRESS STROBE: is an active low signal coming from 80386SX. This input is also used to detect the presence of a 80386SX.

*** BUS INTERFACE ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
IORD-	26	I/O	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
IOWR-	25	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus. This pin becomes an input during the MASTER mode.
MEMRD-	28	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
MEMWR-	27	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus. This pin becomes an input during the MASTER mode.
INTA-	29	O	INTERRUPT ACKNOWLEDGE: is an active low signal to enable the interrupt controller's interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
ALE	38	O	ADDRESS LATCH ENABLE: is an active high pulse signal during TS of any bus cycle including DMA and memory refresh cycle. The address should be latched using the ALE falling edge.
BHE-	42	I	BYTE HIGH ENABLE: is an active low signal used to enable data onto the most significant half of the data bus (D15 - D8). It is an input line when the CPU is in control.
GATEA20	40	I	GATE A20: is an active high signal from 8042 used to gate address A20.
A20	39	I/O	ADDRESS A20: is Address A20 line gated by GATEA20 from 8042 and the alternate A20 gate from port 92(Hex). This pin becomes an input during the MASTER mode.
A0	41	I/O	ADDRESS LINE 0: is the latched version of address 0. It is used along with BHE signal to distinguish the 8/16 bit and odd/even byte operation:

BHE-	A0	OPERATION
0	0	Word (D15 - D0)
0	1	Odd Byte (D15 - D8)
1	0	Even Byte (D7 - D0)
1	1	Not Used

This pin becomes an input during the MASTER mode.

SYMBOL	PIN #	TYPE	NAME and FUNCTION
WS0-	7	I	ZERO WAIT STATE: is an active low signal indicating the present cycle can be completed without any wait state.
IOCS16-	8	I	16-BIT I/O CHIP SELECT: indicates to the system that the present data transfer is a 1 wait-state, 16-bit I/O cycle.
MEMCS16-	9	I	16-BIT MEMORY CHIP SELECT: indicates to the system that the present data transfer is a 1 wait-state, 16-bit memory cycle.

Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
CMDEN-	20	O	COMMAND ENABLE: is an active low control signal to enable or disable the command buffer going to the I/O channel bus (PC bus). It is used to prevent bus contention between I/O devices that share the same address space resided in the X bus and in the I/O channel bus. CMDEN- is active if: 1. Non DMA, all I/O cycles except: 1.1 Floppy I/O if an on-board floppy is enabled. 1.2 Hard Disk I/O if an on-board hard disk controller is enabled. 1.3 Serial Com #1 if an on-board serial com. is enabled. 1.4 Parallel I/O if an on-board parallel port is enabled. 1.5 Video I/O if on-board video is enabled. 1.6 Co-processor I/O. 2. During DMA cycle. 3. During memory refresh cycle. 4. Non-DMA, PC memory cycle except: 4.1 On-board video is enabled and an on-board Video BIOS ROM has been specified. 4.2 On-board video is enabled and an on-board Video Memory has been specified.
PCDIR	21	O	PC DATA BUS DIRECTION: is the control signal to the data transceiver between the CPU and PC data bus: - PCDIR is high ==> the CPU drives the PC data bus (write cycle). - PCDIR is low ==> the PC drives the CPU data bus (read cycle). PCDIR is normally high. It becomes low when: 1. Interrupt acknowledge cycle. 2. Non DMA, memory read cycle. 3. Non DMA, I/O read cycle. 4. DMA, memory cycle.
PCENH-	22	O	PC DATA BYTE HIGH BUS ENABLE: is an active low control signal to enable the data buffer (D15 - D8) between the CPU and PC data bus. PCENH- is active if: 1. Non DMA, I/O odd byte write cycle, except co-processor I/O. 2. Non DMA, PC odd byte memory write cycle. 3. DMA, on-board odd byte system memory on either read or write cycle. 4. Interrupt acknowledge cycle. (INTA- active) 5. Non DMA, PC memory read cycle. (Neither ROM nor system memory is accessed) 6. Non DMA, I/O read cycle if those I/O are not in OTI-051, except co-processor I/O.
PCENL-	23	O	PC DATA BYTE LOW BUS ENABLE: is an active low control signal to enable the data buffer (D7 - D0) between the CPU and PC data bus. PCENL- is active if: 1. Non DMA, I/O even byte write cycle, except co-processor I/O. 2. Non DMA, PC even byte memory write cycle. 3. DMA, on-board even byte system memory on either read or write cycle. 4. Interrupt acknowledge cycle. (INTA- active) 5. Non DMA, PC memory read cycle. (Neither ROM nor system memory is accessed) 6. Non DMA, I/O read cycle if those I/O devices are not in OTI-051, except co-processor I/O.

Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
ENSWAP	24	O	ENABLE DATA SWAP: is an output to control the output enable of the data buffer for byte swap.
PCALE	11	O	PC ADDRESS LATCH ENABLE: is an active high pulse signal during TS of any bus cycle. It is similar to the ALE signal except during the DMA cycle this signal is active high throughout the cycle. It is synchronized to the 8 MHz BUSCLK.
IOCHRDY	5	I	I/O CHANNEL READY: is an active high ready signal from an I/O channel. Pulled low inactive by a memory or I/O device to lengthen memory or I/O cycles. For every system clock cycle this signal is inactive, one wait state is added.
MASTER-	4	I	MASTER: this signal is used together with a DRQ line to gain control of the system.
MREF-	2	I	MEMORY REFRESH: is an active low signal indicating that a refresh cycle is going on. It is forced low when D/SRAM- is low to enable the self-refresh feature of the pseudo-static RAM during the SHUTDOWN mode.
AEN	3	I	ADDRESS ENABLE: is an active high signal during the DMA cycle to degate the I/O devices from the I/O channel to allow DMA transfers to take place.
SEL0	14	O	SELECT FUNCTION 0: is the special select status signal decoder for address range and active on-board video memory space at the current cycle:

SEL0	FUNCTION
0	Nothing selected
1	A15 - A10 = 0 (I/O)

See more detail in 4.4 Memory and I/O Decoder and Buffer Control

SYMBOL	PIN #	TYPE	NAME and FUNCTION
VDIOSEL-	15	O	VIDEO I/O CHIP SELECT: is the active low chip select signal for on-board video I/O address space.
VDPMSEL-	16	O	VIDEO ROM CHIP SELECT: is the active low chip select signal for on-board video ROM address space.
VDRMSEL-	17	O	VIDEO RAM CHIP SELECT: is the active low chip select signal for on-board video RAM address space.

*** SYSTEM INTERFACE ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
CLKIN0	73	I	CLOCK INPUT 0: is a 32 MHz TTL clock input with 50% duty cycle. It is used for: the system clock generation with the CPU running at 8 or 16 MHz, internal DMA control and memory refresh time.
CLKIN1	71	I	CLOCK INPUT 1: is an optional 25 or 40 MHz TTL clock input with 50% duty cycle. It is used for system clock generation with the CPU running at 10, 12.5 or 20 MHz.
BUSCLK	1	O	PC-BUS CLOCK: is a MOS driven clock signal for 80287 and the I/O channel. It has a 50% duty cycle.
CPUCLK	69	O	CPU CLOCK: is a 50% duty cycle MOS driven clock signal to the 80286 CPU. The frequency is programmable through I/O port 0019(Hex).
CLK8	75	O	8 MHz CLOCK: is a 50% duty cycle 8 MHz MOS driven clock signal to the memory controller for memory and refresh timing. It is also used by the 8042 keyboard controller.
RSTIN-	74	I	RESET INPUT: is an active low signal generated from the external RESET switch together with the RC circuitry. OTI-051 provides a Schmitt triggered input.

Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
PWRGOOD	70	I	POWER GOOD: PWRGOOD comes from a power supply to indicate that power is stable. The signal is inactive if an under voltage condition occurs. The PWRGOOD signal has a turn-on delay that is in between 100 ms and 500 ms. OTI-051 provides a Schmitt trigger input for POWERGOOD.
RST8042-	32	I	RESET FROM 8042: is an active low signal from 8042 to reset the CPU.
RESET	31	O	RESET: is an active high signal synchronized to the system clock to reset the system.
RESETCPU	33	O	RESET CPU: is an active high output to reset the CPU.
NPRST	30	O	CO-PROCESSOR RESET: is an active high signal to reset the numerical co-processor.

*** MISCELLANEOUS ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
PAR0 PAR1	100 99	I/O	PARITY BIT (0 - 1): are the memory (odd type) parity bits for even and odd bytes of the memory bank. Each parity bit is generated and written during the memory write operation. Each is checked and reported as an error to the system at the end of the memory read cycle. PAR0 is the memory parity bit for an even byte, PAR1 is the memory parity bit for an odd byte.
COMRQ-	37	I/O	COMMAND REQUEST: active low bidirectional signal. In the output phase, it sends a signal to OTI-053 indicating when to wakeup from the SHUTDOWN mode. In the input phase, it receives a request from OTI-053 to generate the PC memory cycle. The signal is in the output phase when AEN is HIGH and is in the input phase during other times.
IOCK	6	I/O	CHANNEL CHECK: part of port 61(Hex). An I/O channel condition will be reported to the CPU when this port is read.
TIMER2	35	I	TIMER 2 OUTPUT: status signal on 8254 timer channel 2. This signal comes from OTI-052.
NMI	12	O	NON-MASKABLE INTERRUPT: is an active high signal to the CPU indicating that an error has occurred in one of the following areas: - memory parity error - I/O channel check signal from the PC bus.
INTR	13	I	INTERRUPT: interrupt request from OTI-052 interrupt controller.
ROMCS	18	O	ROM CHIP SELECT: is an active low signal used to enable the ROM BIOS to output data on to the data bus.
SECCHK	34	I	SECURITY CHECK: is an active high input coming from the on-board jumper. Security check is enabled if this input is high.
VDD	10,36,61,94		POWER: +5 V supply. 4 pins
VSS	19,43,72,90		GROUND: 4 pins

NOTE: OTI-051 would go into TEST mode under the following input pin combination: RSTIN-, PWRGOOD, MASTER - all at logic 0.

Top pins (left to right):

PAR0 · PAR1 · SD15 · SD14 · SD13 · SD12 · VDD · SD11 · SD10 · SD9 · VSS · SD8 · SD7 · SD6 · SD5 · SD4 · SD3 · SD2 · SD1 · SD0

Pin	Signal (left)		Pin	Signal (right)
1	BUSCLK		80	SRDY-
2	MREF- (Index)		79	M/IO-
3	AEN		78	SI-/DC-
4	MASTER-		77	SO-/WR-
5	IOCHRDY		76	ADS-
6	IOCK		75	CLK8
7	WS0-		74	RSTIN-
8	WOCS16-		73	CLKIN0
9	MEMCS16-		72	VSS
10	VDD		71	CLKIN1
11	PCALE		70	PWRGOOD
12	NMI		69	CPUCLK
13	INTR		68	SA23
14	SEL0		67	SA22
15	VDIOSEL-		66	SA21
16	VDPMSEL-		65	SA20
17	VDRMSEL-		64	SA19
18	ROMCS		63	SA18
19	VSS		62	SA17
20	CMDEN-		61	VDD
21	PCDIR		60	SA16
22	PCENH-		59	SA15
23	PCENL-		58	SA14
24	ENSWAP		57	SA13
25	IOWR-		56	SA12
26	IORD-		55	SA11
27	MEMWR-		54	SA10
28	MEMRD-		53	SA9
29	INTA-		52	SA8
30	NPRST		51	SA7

Bottom pins (left to right):

31 RESET · 32 RST8042- · 33 RESETCPU · 34 SECCHK · 35 TIMER2 · 36 VDD · 37 COMRQ- · 38 ALE · 39 A20 · 40 GATEA20 · 41 A0 · 42 BHE- · 43 VSS · 44 SA0 · 45 SA1 · 46 SA2 · 47 SA3 · 48 SA4 · 49 SA5 · 50 SA6

3.0 OTI-051 FUNCTIONAL DESCRIPTION

OTI-051 functions can be categorized as follows:

1. Command Cycle Control

2. Address and Data Path

3. Clock Generator and Reset Control

4. Memory and I/O Decoder and Buffer Control

5. System Ready Generator

6. Power Management

7. Miscellaneous

8. System Control and Status Registers

3.1 Command Cycle Control

Command Cycle Control contains a state machine that generates the CPU cycles:
- Memory Read/Write Cycle if memory access is outside of on-board system memory.
- I/O Read/Write Cycle.
- Interrupt Acknowledge Cycle.
- ROM BIOS Read Cycle.

In addition to these functions, Command Cycle Control also generates the ALE signal when it detects a change on the CPU Status lines: S0 - S1 and M/IO at TS time to mark the beginning of the CPU cycle.

The Command Cycle Control can be clocked by two different clock sources. Two different timing modes can be selected by programming indexed port 03(Hex) as described in section 6.3.1. In the Synchronous mode, SYSCLK is used. The state machine is either clocked by CPUCLK/2 or CPUCLK/4. If indexed port 03(Hex) bit 0 (SPD0) is 1, then CPUCLK/4 is used. If SPD0 is 0, then CPUCLK/2 is used.

In the asynchronous mode, BUSCLK is used. The state machine would always be running at BUSCLK speed, independent of the CPU speed. In this mode, a very high speed CPU can be used and the system can still maintain AT-compatible bus timing. The command pulse width and command recovery time is independent of CPU speed. PCALE is synchronized to the 50% duty cycle BUSCLK on the PC-BUS. Commands are synchronized to the bus clock. The minimum command length and recovery time is referenced to BUSCLK.

In either mode, the command width and command recovery time can be adjusted by programming indexed port 01(Hex) for PC memory and indexed port 02(Hex) for I/O cycles.

3.1.1 Memory Read/Write Cycle

The state machine samples the CMDRQ- signal from the System Memory Control section at the end of the TS cycle. If the memory being accessed does not reside in either system memory or the EMS/Extended memory area, CMDRQ- is asserted. MRD- or MWR- command is active during the TC cycle. Normal command length is five 8 MHz clocks, but the user can program the speed control register (indexed port 03(Hex)) to reduce the command length to three 8 MHz clocks for fast PC- memory cycles.

If IOCHRDY is asserted low, the command will be extended. The command is terminated three 8 MHz clocks minimum after the IOCHRDY is asserted high.

If the current cycle is a 16 bit memory operation to 8 bit memory devices, the state machine performs a double memory cycle operation with the first cycle accessing the low byte (A0 is low) and the second cycle accessing the high byte (A0 is high). From the end of the first cycle to the beginning of the second cycle (i.e. RECOVERY TIME) is three 8 MHz clocks. For a memory read cycle, the low byte of data is stored and outputted to the CPU bus at the second cycle along with the high byte. If MEMCS16- is low and the current cycle is a 16 bit memory operation, then no double cycle is generated. The memory cycle would also be a 1 wait state command cycle.

PC Memory Wait State Control Register:Indexed Port 0001(Hex) R/W:

Bit	Function
7-6	Additional Wait States for Memory Command width

bit 7	bit 6	
1	1	3 additional wait states
1	0	2 additional wait states
0	1	1 additional wait state
0	0	no additional wait state

Bit	Function
5-4	Additional Wait States before Memory Command starts

bit 5	bit 4	
1	1	3 additional wait states
1	0	2 additional wait states
0	1	1 additional wait state
0	0	no additional wait state

Bit	Function
3	FAST: for fast PC Memory command cycles.
	0 - normal PC memory command width with number of wait states as programmed in bits 7 and 6
	1 - normal PC memory command width as programmed in bits 7 and 6 minus 3 wait states
2-0	Not used, read as 000.

At Power On or Reset, the content of indexed port 01(Hex) is 00(Hex).

3.1.2 I/O Read/Write Cycle

The state machine generates and provides the timing for every I/O cycle. During the I/O cycle, the IORD- or IOWR- commands are asserted at the beginning of TC. Command length is fixed at five 8 MHz clocks and recovery time at three 8 MHz clocks.

If IOCHRDY is asserted low, the command will be extended. The command will be terminated three 8 MHz clocks minimum after the IOCHRDY is asserted high.

Similar to memory commands, if the current cycle is a 16 bit I/O operation to 8 bit I/O devices, the state machine will perform a double cycle with a recovery time of three 8 MHz clocks.

However, if IOCS16- is low, no double cycle will be generated, and the current cycle is a 1 wait state command cycle.

I/O Command Wait State Control Register: Indexed Port 0002(Hex) R/W:

Bit	Function		
7-6	Additional Wait States for I/O Command width		
	bit 7	bit 6	
	1	1	3 additional wait states
	1	0	2 additional wait states
	0	1	1 additional wait state
	0	0	no additional wait state
5-4	Additional Wait States before I/O Command starts		
	bit 5	bit 4	
	1	1	3 additional wait states
	1	0	2 additional wait states
	0	1	1 additional wait state
	0	0	no additional wait state
3-0	Not used, read as 0000.		

At Power On or Reset, the content of indexed port 02(Hex) is 00(Hex).

3.1.3 Interrupt Acknowledge Cycle

Two consecutive cycles of interrupt acknowledge (INTA-) are generated to an interrupt controller in response to an interrupt signal to the CPU. During the first cycle, the interrupt controller resolves the priority if there is more than one interrupt pending. In the second cycle, the interrupt controller outputs onto the 8 bit data bus (D0 - D7) the interrupt vector address pointing to the interrupt routine table. INTA- is asserted at the beginning of TC. IOCHRDY can also extend the duration of the cycle. The cycle will be terminated 3 clocks minimum after IOCHRDY is asserted high. The minimum period (if IOCHRDY is always high) of INTA- is two 8 MHz clocks. BUS HOLD Request to the CPU is blocked between the two INTA- cycles to assure the execution of the second INTA- cycle.

3.1.4 ROM BIOS Read Cycle

The state machine generates the MRD- command if there is a memory access between 0E0000 and 0FFFFF memory space. MRD- is asserted at the middle of TS with 1-4 user programmable wait states. The user can select shadow ROM implementation for zero wait state ROM cycles.

Memory Wait State Control Register: Indexed Port 001B(Hex) W/R:

Bit	Function		
7-4	Not used		
3-2	Number of Wait states in ROM cycle		
	bit 3	bit 2	
	1	1	4 wait states
	1	0	3 wait states
	0	1	2 wait states
	0	0	1 wait state
1	Reserved, read as 0.		
0	Number of Wait states in RAM cycle during page hit		
	0 - 0 wait state		
	1 - 1 wait state		

At Power On or Reset, the content of indexed port 1B(Hex) is 0D(Hex).

3.2 Address and Data Path

OTI-051 is connected directly to the address and data bus of the CPU. OTI-051 latches the address bus internally to form an address bus LA(0-23). The CPU data bus is connected to the transceiver internally to form the 16 bit data bus: LD(0-15).

- SA to LA during CPU or Coprocessor access time.
- 8 bit data registers, both input and output are connected to LD(0-7). It is used to latch the read data from an 8 bit device at the first cycle of a 16 bit operation.
- 8 bit data transceiver connected between LD(0-7) and LD(8-15). It is used to swap the data path between the low byte and high byte to access to an 8 bit internal device. During a 16 bit operation to a 16 bit device, this transceiver is disabled.

If an 80286 is used, ALE is generated during the 2nd phase of TS. If an 80386SX is used, ALE is generated at the rising edge of ADS-. ALE is active high and the pulse width is one CPUCLK. (one phase)

3.3 Clock Generator and Reset Control

3.3.1 Clock Generator

OTI-051 supports system speeds ranging from 8 MHz, 10 MHz, 12.5 MHz, 16 MHz and up to 20 MHz.

Two clock inputs are available for users:
CLKIN0: 32 MHz
CLKIN1: 25 MHz, 40 MHz

CLKIN0 is required. OTI-051 uses CLKIN0 to derive the 8 MHz internal clock for asynchronous bus timing and CPU power save mode. It also uses CLKIN0 for 16 MHz system operation. CLKIN1 is optional. The user can input a 25 MHz clock for 12.5 MHz system operation, or a 40 MHz clock for 10 MHz or 20 MHz system operation. During power-up, the system defaults to 8 MHz operation. Different clock inputs and system speeds can be selected by programming indexed port 03(Hex).

The Clock Generator provides clocks to the CPU, Memory Controller, DMA controller, and the rest of the system. It can be broken down to 2 blocks based on their functions:
- Multiplexer and Deglitching Circuit based on CLKIN0, and the presence of CLKIN1.
- Dividers: by 2, by 4 or by 8.

The Speed Control Register is an indexed I/O port used to change the speed of the CPU clock.

OTI-051 also generates an 8 MHz 50% duty cycle clock output. This clock is used by OTI-053 for memory refresh timing and RAS pulse width timing. The 8042 keyboard controller also uses this clock signal.

3.3.2 Reset Control

There are several conditions that will generate a system reset:
- At power on, the power supply provides a POWERGOOD signal. It indicates proper operation of the power supply and gives advance warning when power is turned off.
- At reset switch, RSTIN-, an active low pulse signal. OTI-051 provides a Schmitt trigger input so that an RC circuit can be used to establish a reset pulse of proper duration.
- At mode switching from Protected Mode to Real Mode by writing to either port 64(Hex) or port 92(Hex) for a fast reset. Only the CPU is reset in this case and no system reset is issued.
- When the CPU executes a shutdown instruction. Only the CPU is reset in this case and no system reset is issued.

During a system reset, OTI-051 generates an active high pulse signal synchronized to the CPUCLK to reset the CPU and system.

During a CPU reset, OTI-051 only generates a RESET signal to the CPU but not to the system. The RESET signal generated is active for the number of clocks to satisfy the requirements of the CPU. During system reset, OTI-051 also generates NPRST to reset the co-processor. OTI-051 also responds to the I/O WRITE instruction to port F1(Hex). When port F1 is written to with 00, NPRST is generated.

Depending on the type of co-processor installed, the NPRST would remain active for the appropriate number of clocks to reset the co-processor.

3.4 Memory and I/O Decoder and Buffer Control

This section provides the decoder for the devices on the memory and I/O spaces in the system and also internal and external buffer enable and direction controls for memory and I/O channels (PC). It also generates a status signal (e.g. SEL0 to OTI-052) as the address range status information for OTI-052 to control and enable the current cycle:

SEL0	FUNCTION
0	Not used [1]
1	A15 - A10 = 0 (I/O) [2]
Note:	1. A15 - A10 during a CPU I/O cycle (DMA cycle is not included) are not 0's or
	2. A15 - A10 during a CPU I/O cycle (DMA cycle is not included) are 0's

3.5 System Ready Generator

System Ready will be active only at the end of the CPU or co-processor cycle. There are 2 sources that generate a system ready to the CPU to end the cycle:
- Memory Control if the access is in the system or EMS memory range. System ready will be generated during TC and ended at TS or TI time for a period of 1 system clock.
- Command Generator that generates the cycle besides the system memory. System ready will be generated at the rising edge of the last TC and ended at the rising edge of TS or TI time for a period of 1 system clock.
- During the co-processor I/O cycle, OTI-051 generates SRDY- to terminate the I/O cycle.

3.6 Power Management

Three modes of power saving operations:

SHUTDOWN Mode - CPU clock is stopped, OTI-053 takes over the bus. OTI-053 generates REFRESH CYCLES. DMA requests are blocked. When the system wakes up, the CPU is reset.

SLEEP Mode - CPU is running at 2 MHz, OTI-053 takes over the bus. OTI-053 generates REFRESH CYCLES. DMA requests are blocked. When the system wakes up, the CPU continues to run without reset.

SLOW Mode - CPU runs at 4 MHz and DMA and REFRESH cycles are served in the same manner as in normal system speed.

The 3 different CPU power-off modes can be selected by programming indexed port 03(Hex). The CPU can be awakened from the SHUTDOWN or SLEEP mode through an interrupt (INTR) from the interrupt controller. Once OTI-051 receives the INTR signal, it activates the CMDRQ- signal to OTI-053 indicating that it is time to release the HOLD signal to the CPU.

3.7 Miscellaneous

3.7.1 Memory Parity Check and Generation

Memory parity is generated by OTI-051 during a system memory write. During a system memory read, OTI-051 also checks the parity bit against the memory data. The parity error information is latched into port 61(Hex).

3.7.2 Timeout Counter

A 16-bit counter is provided for the implementation of a watchdog timer. The user can program the counter to determine how long he wants to wait for any cycle to finish before terminating the cycle. When the maximum count is reached, OTI-051 will terminate the present cycle automatically, generate an NMI, set indexed port 0E(Hex) bit 0 and latch the I/O address into port 0E(Hex). The timeout counter helps in preventing system hang when an I/O device is not functioning properly.

3.7.3 System Control and Status Registers

SYSCNLB: System Control Port B is an 8 bit I/O read/write port used to enable/disable the parity check, and some peripherals:

SYSCNLB: I/O Port 0061 R/W:

Bit	Function
7	R Memory parity check
6	R I/O Channel Check
5	R Timer 2 output
4	R Toggles with each memory refresh request on a read operation
3	R/W DIS/EN- IOCHCK signal. When set to 1, this bit disables IOCHCK from generating an NMI. When cleared to 0, an NMI is generated when IOCHCK goes active.
2	R/W DIS/EN- memory parity check. When set to 1, this bit disables parity error generation caused by system memory including the EMS memory from generating an NMI. When cleared to 0, an NMI is generated when a memory parity error is sensed.
1	R/W EN/DIS- Beeper Data output. This bit gates the output of timer 2. It is used to disable the timer's sound source or modify its output. When set to 1, this bit enables the output, and when cleared, it forces the output to zero.
0	R/W EN/DIS- Timer 2 Gate. This line is routed to the timer input at gate 2. When this bit is cleared to 0, the timer operation is halted. This bit and bit 1 control the operation of the timer's sound source.

At Power On or Reset, SYSCNTL = 00.

NMICTL: NMI Control Register is an 8 bit I/O write only port used to enable/disable an NMI to the CPU:

NMICTL: I/O Port 0070 W:

Bit	Function
7	DIS/EN- NMI to the CPU.
6-0	Not used. Reserved as 0's.

At Power On or Reset, NMICTL is set disabled (bit 7 = 1).

SYSCTLA: System Control Port A is an 8 bit I/O read and write port used to control the security lock and Gate A20.

SYSCNLA: I/O Port 0092 R/W:

Bit	Function
7-4	Reserved
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Reserved

At Power On or Reset, SYSCNLA reads as 00.

4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

Table 2. AC Characteristics of OTI-051

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t1	CLKIN0 Period	31		ns	
t1a	CLKIN0 HIGH Time	12		ns	
t1b	CLKIN0 LOW Time	12		ns	
t2	CLKIN1 Period	25		ns	
t2a	CLKIN1 HIGH Time	10		ns	
t2b	CLKIN1 LOW Time	10		ns	
t3	CPUCLK Period	25		ns	CL=30 pF
t3a	CPUCLK HIGH Time	10		ns	CL=30 pF
t3b	CPUCLK LOW Time	10		ns	CL=30 pF
t4	BUSCLK to PCALE		45	ns	CL=200 pF
t5	BUSCLK to COMMAND		35	ns	CL=50 pF
t6	Read Valid Data		100	ns	CL=100 pF
t7	COMMAND Pulse Width	650		ns	
t8	INTAN Pulse Width	310		ns	
t9	IOCHRDY from COMMAND Active		520	ns	
t10	IOCHRDY to COMMAND Inactive	240		ns	
t11	Read Data HOLD Time	10		ns	CL=100 pF
t12	LA Address from SA Address		25	ns	CL=100 pF
t13	IOCS16N SETUP Time	20		ns	
t14	IOCS16N, MEMCS16N HOLD Time		15	ns	
t15	IOCHRDY from I/O Active		20	ns	
t16	MEMCS16N SETUP Time	20		ns	
t17	IOCHRDY from MEMORY Active		35	ns	
t18	PC Address from PCALE		25	ns	CL=200 pF
t19	ALE from CPUCLK		25	ns	CL=20 pF
t20	PAR0, PAR1 from SD		35	ns	CL=100 pF
t21	SRDYN Active from CPUCLK		12	ns	CL=50 pF

Table 2. AC Characteristics (Continued)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t22	SRDYN Inactive from CPUCLK		35	ns	CL=50 pF
t23	PWRGOOD, RSTINN SETUP Time		20	ns	See Note
t24	RESET from CPUCLK		20	ns	CL=200 pF
t25	RESETCPU from CPUCLK		10	ns	CL=20 pF
t26	NPRST from CPUCLK		10	ns	CL=20 pF
t27	VDXXSELN Valid from ALE		50	ns	CL=100 pF
t28	ROMCSN Valid from ALE		50	ns	CL=20 pF
t29	A20 Valid from SA20		20	ns	CL=30 pF
t30	A0 Valid from SA0		25	ns	CL=30 pF
t31	SEL0 Valid to COMMAND	45		ns	CL=15 pF
t32	PCDIR Valid from S1 & S0		45	ns	CL=15 pF
t33	PCDIR Inactive from BUSCLK		35	ns	CL=15 pF
t34	PCENHN, PCENLN, ENSWAP Active from Read COMMAND		20	ns	CL=15 pF
t35	PCENHN, PCENLN, ENSWAP Inactive from BUSCLK		35	ns	CL=15 pF
t36	PCENHN, PCENLN, ENSWAP Active from COMRQN during Write		50	ns	CL=15 pF

NOTE: SETUP time is only for testing purposes.

4.2 D.C. Characteristics

D.C. Characteristics: TA=0 deg C to 70 deg C,VDD=5V+/-5%,VSS=0V

Table 3. DC Characteristics of OTI-051

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 µA
VOL1	Output LOW Voltage		0.45	V	IOL=20 mA, Note 1
VOL2	Output LOW Voltage		0.45	V	IOL=16 mA, Note 1
VOL3	Output LOW Voltage		0.45	V	IOL=10 mA, Note 1
VOL4	Output LOW Voltage		0.45	V	IOL= 8 mA, Note 1
VOL5	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 1
VOL6	Output LOW Voltage		0.45	V	IOL= 2 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmitt Input HIGH	2.4	VDD+0.5	V	Schmitt, Note 2
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		30	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

NOTES:

1. Output Current (IOL) Capabilities:

20 mA:	PCALE, RESET
8 mA:	A20, A0, SRDYN, PAR0, PAR1
4 mA:	BUSCLK, VDIOSELN, VDPMSELN, VDRMSELN, ROMCSN, IOWRN, IORDN, MEMWRN, MEMRDN, CPUCLK, CLK8, SD0-SD15
2 mA:	NMI, SEL0, CMDENN, PCDIR, PCENHN, PCENLN, ENSWAP, RESETCPU, ALE, COMRQN

2. Input Structures:

Schmitt triggered:	PWRGOOD, RSTINN
TTL:	all others
Input with pullup:	BHEN, S0, S1, MIO, SRDYN, SD0-15

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5.0 OTI-051 TIMING DIAGRAMS

FIGURE 1-1.

8 BIT PC CYCLE TIMING DIAGRAM
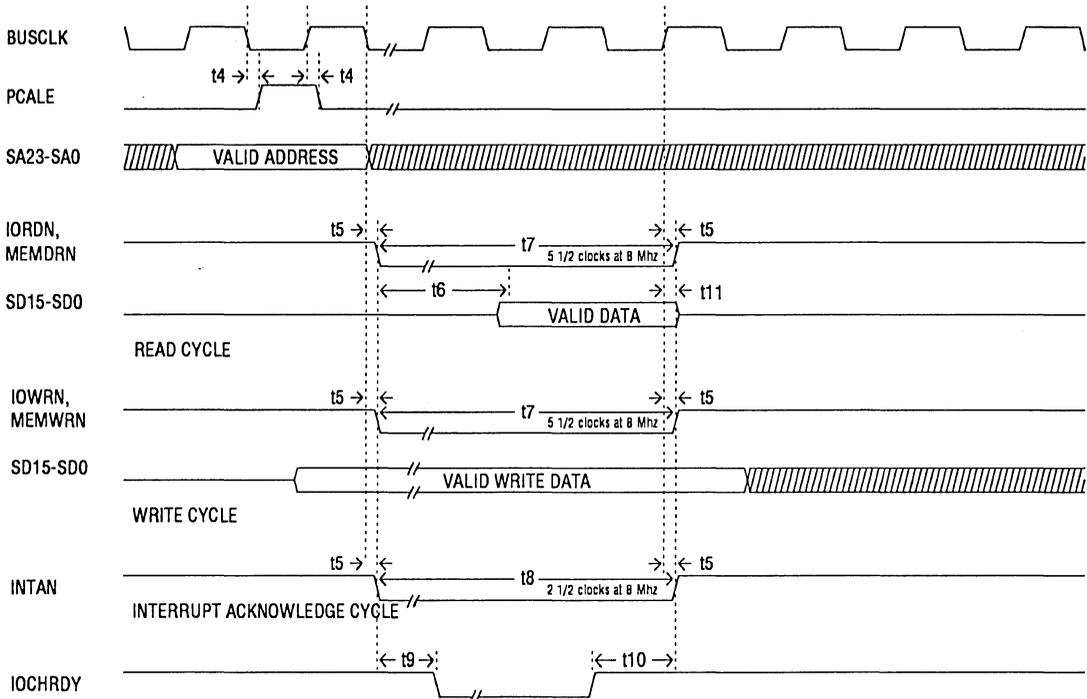
FIGURE 1-2.

16 BIT I/O CYCLE
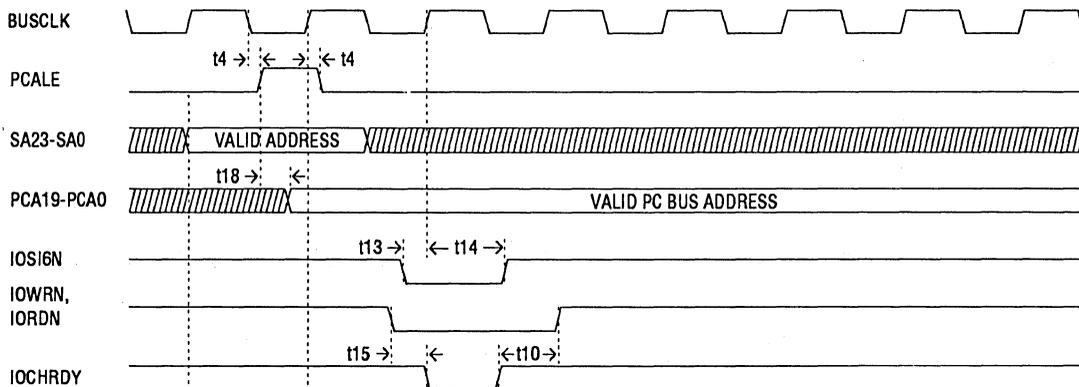
16 BIT MEMORY CYCLE (1 WAIT STATE)
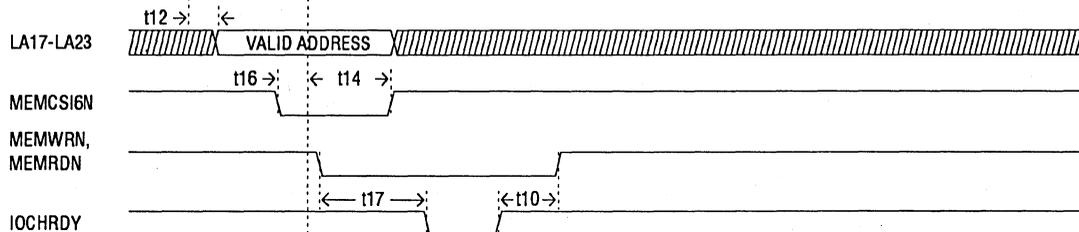
16 BIT MEMORY CYCLE (0 WAIT STATE)
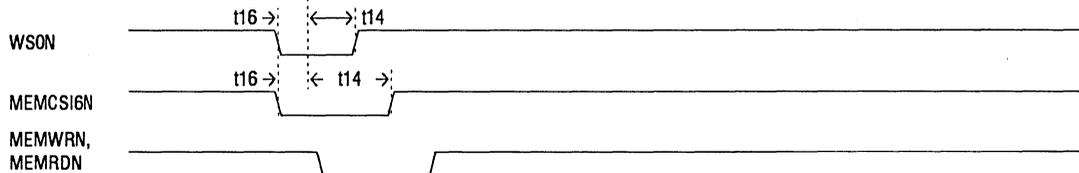
FIGURE 1-3.

CPU CLOCK TIMING
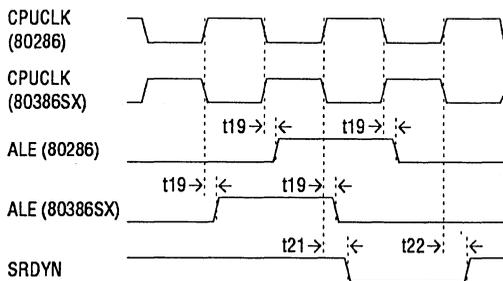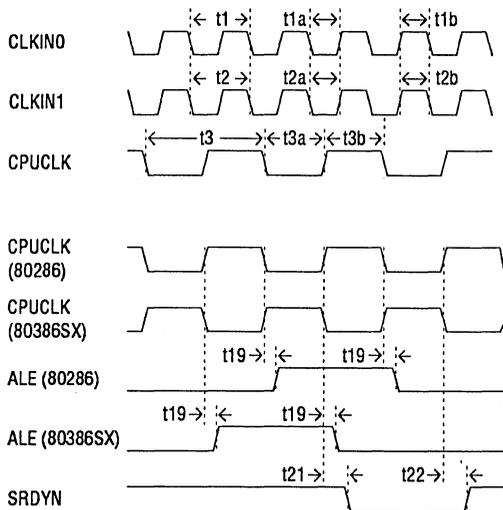
SYSTEM TIMING
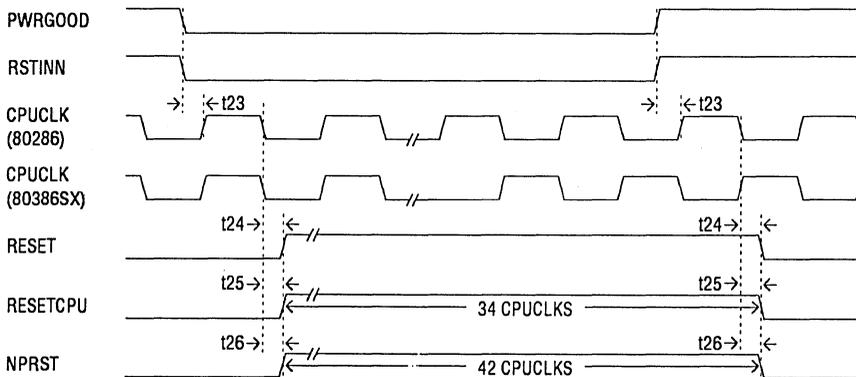
FIGURES 1-4&5.

ADDRESS & CHIP SELECT TIMING
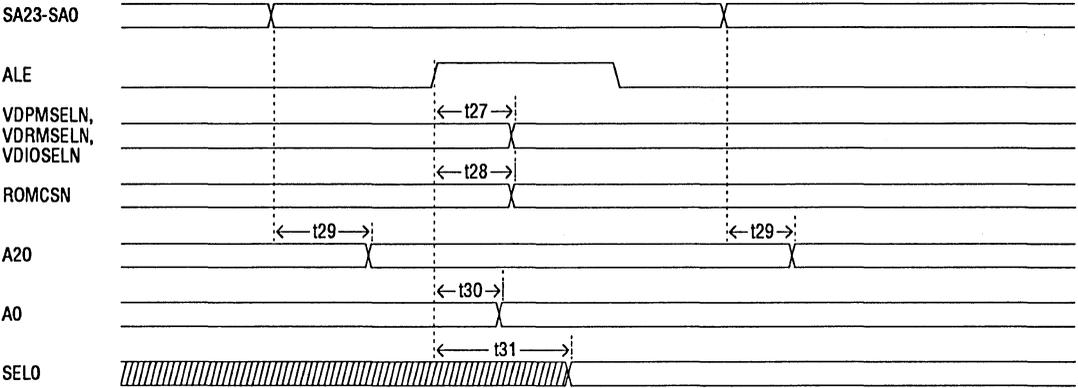
PARITY GENERATION TIMING
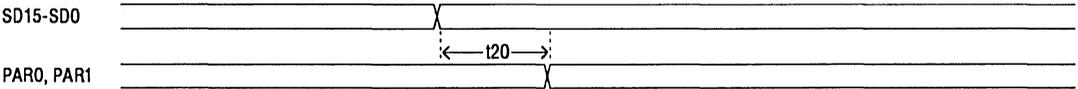
COMMAND & DATA BUFFER CONTROL TIMING

SECTION 2

OTI-052
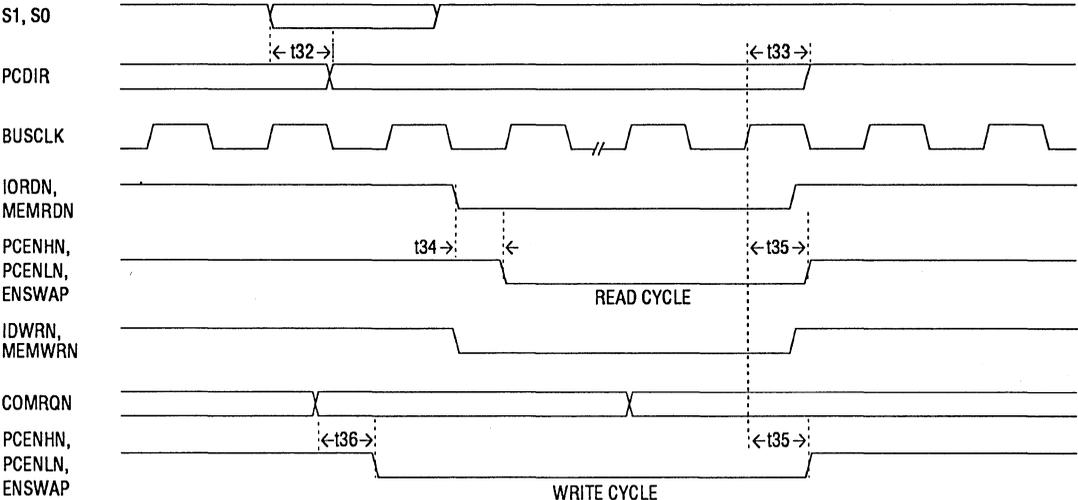
I/O CONTROL LOGIC

1.0 INTRODUCTION TO THE OTI-052 I/O CONTROLLER

OTI-052 is an integrated I/O peripheral controller. It consists of the following functional blocks:

- Dual 8259 compatible interrupt controllers

- 8254 compatible timer/counter

- 16450 compatible serial communication controllers

- Parallel port controller

- Chip select logic for floppy disk controller (OTI-033), hard disk subsystem, keyboard controller, and co-processor

- Co-processor interface logic

System Block Diagram

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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-052 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
			*** Bus Interface ***
XDATA7-XDATA0	7-14	I/O	XDATA BUS: bi-directional data lines to/from the I/O channel bus.
SADR9-SADR0	19-22,24-29	I	ADDRESS BUS: from I/O channel. It determines which I/O device the CPU is accessing.
PCAEN	79	I	ADDRESS ENABLE: signal to de-gate the I/O devices from the I/O channel and allow DMA transfers to take place.
IORD-	54	I	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus.
IOWR-	53	I	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus.
MEMRD-	52	I	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus.
MEMWR-	51	I	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to read the data present on the data bus.
MREF-	80	I	MEMORY REFRESH REQUEST: active low. It indicates that the system is in the memory refresh cycle.
REFRQT	81	O	REFRESH REQUEST: indicates to the CPU that the DRAM needs refreshing.
ADSEL0	98	I	SELECT FUNCTION 0: is the special select status signal decoder for address range and active on-board video memory space at the current cycle:

SEL0	FUNCTION
0	Nothing selected
1	A15 - A10 = 0 (I/O)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
VDPMSEL-	99	I	VIDEO ROM CHIP SELECT: is the chip select signal for on-board video ROM address space.
VDRMSEL-	100	I	VIDEO RAM CHIP SELECT: is the chip select signal for on-board video RAM address space.
XBFRD	78	O	X-BUS DIRECTION: active low signal to OTI-054. When this signal is low, data is read from the internal bus to the I/O channel. When this signal is high, data is written from the I/O channel to the internal bus.
RESET	17	I	RESET INPUT: active high signal which is used to reset the internal logic of OTI-052.
			*** Timer Counter ***
SPKOUT	55	O	SPEAKER DATA OUTPUT: speaker output data to be connected to a speaker driver to drive the speaker or beeper.
TIMER2	56	O	TIMER 2 OUTPUT: status signal on 8254 timer channel 2. This signal goes to OTI-051.

Table 1. OTI-052 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
			*** Interrupt Controller ***
IRQ1, IRQ3-12, IRQ14-15	84-90,92-97	I	INTERRUPT REQUEST INPUTS: asynchronous interrupt request inputs to the internal 8259 controllers.
INTR	82	O	INTERRUPT REQUEST: interrupt request to the CPU and is generated whenever a valid IRQ is received.
INTA-	83	I	INTERRUPT ACKNOWLEDGE: is an active low signal from OTI-051 indicating an interrupt acknowledge cycle is in progress.
			*** Parallel Port Interface ***
PD0-PD7	62-65,67-70	I/O	PARALLEL PORT DATA BUS: the bi-directional data lines to the parallel port device. When printer mode is selected, these lines are used as output lines. When input mode is selected, these lines are used as input lines.
ACK-	71	I	PRINTER ACKNOWLEDGE: active low. This pin indicates that the data has been received by the printer.
BUSY	77	I	PRINTER BUSY: indicates that the printer is unable to receive data.
PTPERR	60	I	PRINTER PAPER END OR ERROR: indicates that the end of paper has been detected.
SLCT	76	I	PRINTER SELECT: indicates that the printer is selected.
AUTOFD-	72	O	PRINTER AUTO FEED: active low. It causes the printer to generate a line feed after each line is printed.
ERROR-	75	I	PRINTER ERROR: active low. Indicates that a printer error has occurred.
INIT-	61	O	PRINTER INITIALIZE: active low. It initializes the printer.
SELIN-	74	O	PRINTER SELECT IN: active low. It selects a printer.
STROBE-	59	O	PRINTER STROBE: active low. Its function is to control the "strobe" signal to the printer.
			*** Serial Port Interface ***
CLKSER	39	I	CLOCK INPUT: a 32 MHz TTL clock input.
TXD1	37	O	TRANSMIT DATA 1: the serial output data from UART1.
RXD1	30	I	RECEIVE DATA 1: the serial input data to UART1.
DTR1-	36	O	DATA TERMINAL READY: active low. Notify the MODEM or data set that UART1 is ready to transfer characters.
RTS1-	35	O	REQUEST TO SEND: active low. Handshake signal notifying the MODEM or data set that UART1 is ready to transmit data.
CTS1-	34	I	CLEAR TO SEND: active low. Handshake signal notifying UART1 that the MODEM or dataset is ready to receive data.
DSR1-	33	I	DATA SET READY: active low. The signal indicates that the MODEM or data set is ready to establish the communication link with the UARTS. The CPU can read the UART register to find out the MODEM's ready condition.

Table 1. OTI-052 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
DCD1-	31	I	CARRIER DETECT: active low. The MODEM or data set uses these pins to notify UART1 that the carrier signal has been detected.
RIN1-	32	I	RING INDICATOR: active low. It notifies UART1 that a telephone ringing signal has been detected by the MODEM or data set.

*** Keyboard and Mouse Interface ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
SELKBD-	18	O	SELECT KEYBOARD: active low. Indicates the keyboard controller is selected .

*** Floppy Disk Controller ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
FLPCS-	40	O	FLOPPY SELECT: active low. This pin selects the floppy disk controller (OTI-033).
RD3F0-	41	O	READ RAS PORT A: active low. It enables RAS Port-A.
RD3F1-	42	O	READ RAS PORT B: active low. It enables RAS Port-B.
HIGDNTY	44	O	HIGH DENSITY: high current output to the input of the floppy drive high density media support. This pin supports both AT and Model 30-286 types.
DACK2-	43	I	DMA ACKNOWLEDGE: active low. It indicates that the floppy disk controller has been granted a DMA cycle.
PREN	46	O	PRECOMP: selects the precompensation value for the floppy disk controller.
DRVTYPE	47	O	DRIVE TYPE: controls the data rate for the floppy disk controller.

*** Hard Disk Controller ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
HDINS-	48	I/O	HARD DISK INSTALLED: active low input indicating that an on-board IBM hard disk is installed. When a Conner's hard disk is installed, this pin is used as one of the chip select output decoding addresses 3F6 and 3F7.
SELHDK-	49	O	HARD DISK SELECT: active low. It selects an on-board hard disk drive for an I/O operation.
DACK3-	50	I	DMA ACKNOWLEDGE: active low. It indicates that the on- board hard disk controller has been granted a DMA cycle.

*** Co-processor Interfaces ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
NPEREQ	5	I	NUMERICAL PROCESSOR REQUEST: active high. It indicates that the co-processor is requesting an operand transfer. This pin comes from the PEREQ output of the co-processor.
CPEREQ	6	O	CPU REQUEST: active high. It indicates to the CPU that the co-processor is requesting an operand transfer. This pin goes to the CPU to request the transfer.
NPERR-	1	I	NUMERICAL PROCESSOR INTERRUPT: active low. It indicates that an unmasked exception has occurred during a numeric instruction execution when an 80287 interrupt is enabled.
NPBSY-	2	I	NUMERICAL PROCESSOR BUSY: active low. It is connected directly to the BUSY signal of the co-processor.

Table 1. OTI-052 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
NPCS-	3	O	NUMERICAL PROCESSOR CHIP SELECT: When low, the co-processor is selected for an I/O operation.
BUSYCPU-	4	O	BUSY TO CPU: active low. It is connected directly to the BUSY input of 80286 or 80386SX.
			*** POWER Management ***
MINCLK	16	I	MINUTE CLOCK: minute clock signal from OTI-054.
			*** Others ***
CLK14	57	I	14.318 MHz TTL level clock input signal used to generate internally the clock for 8254.
VSS	15,45,58,66,91	I	GROUND: 5 pins 0V
VDD	23,38,73	I	POWER: 3 pins 5V

NOTE: OTI-052 would go into the TEST mode under the following input combination:

    RESET = '0'
    DACK3- = '0'
    DACK2- = '0'

Top pins (left to right):

VDRM SEL- · VDPM SEL · ADSEL0 · IRQ15 · IRQ14 · IRQ12 · IRQ11 · IRQ10 · IRQ9 · VSS · IRQ8 · IRQ7 · IRQ6 · IRQ5 · IRQ4 · IRQ3 · IRQ1 · INTA- · INTR · REF RQT

Left side pins (1–30):

Pin	Signal
1	NPERR-
2	NPBSY-
3	NPCS-
4	BUSYCPU-
5	NPEREQ
6	CPEREQ
7	XDATA7
8	XDATA6
9	XDATA5
10	XDATA4
11	XDATA3
12	XDATA2
13	XDATA1
14	XDATA0
15	VSS
16	MINCLK
17	RESET
18	SELKBD-
19	SADR9
20	SADR8
21	SADR7
22	SADR6
23	VDD
24	SADR5
25	SADR4
26	SADR3
27	SADR2
28	SADR1
29	SADR0
30	RXDI

Right side pins (51–80):

Pin	Signal
80	MREF-
79	PCAEN
78	XBFRD-
77	BUSY
76	SLCT
75	ERROR-
74	SELIN-
73	VDD
72	AUTOFD-
71	ACK-
70	PD7
69	PD6
68	PD5
67	PD4
66	VSS
65	PD3
64	PD2
63	PD1
62	PD0
61	INIT-
60	PTPERR
59	STROBE-
58	VSS
57	CLK14
56	TIMER2
55	SPKOUT
54	IORD-
53	IOWR-
52	MEMD-
51	MEMWR-

Bottom pins (31–50, left to right):

DCDI- · RIN1- · DSRI- · CTSI- · RTSI- · DTRI- · TXDI · VDD · CLK SER · FLPCS- · RD3F0- · RD3F1- · DACK2- · HIGD NTY · VSS · PREN · DRV TYPE · HIDNS- · SEL HDK- · DACK3-

Index

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3.0 OTI-052 FUNCTIONAL DESCRIPTION

OTI-052 functions can be categorized as follows:

1. Interrupt Control Logic

2. Timer Controller

3. Serial Communication Controller

4. Parallel Port Controller

5. Floppy Disk Decode and Control Logic

6. Hard Disk Decode Logic

7. Power Management

8. System Control and Status Registers

9. Co-processor Interface

3.1 Interrupt Control Logic

The interrupt control logic includes two Intel 8259A compatible interrupt controllers. It has 15 levels of interrupt that are handled according to programmed priority in the OTI-052 chip. The following table shows the hardware interrupts and their availability to the I/O channel (PC bus).

Table 2. Availability of Hardware Interrupts to the I/O Channel

Level	OTI-052 chip	System Board	I/O channel
IRQ0	Timer Channel 0	Not available	Not available
IRQ1	Not used	Keyboard interface	Not available
IRQ2	Slave	Not Available	Not available
IRQ3	COM2	Not used	Available
IRQ4	COM1	Not used	Available
IRQ5	Not used	Parallel port 2	Available
IRQ6	Not used	Diskette drive (OTI-033)	Available
IRQ7	Parallel port	Not used	Available
IRQ8	Not used	Real Time Clock	Not Available
IRQ9	Not used	Software redirects to INT 0A(Hex) (IRQ2)	Available
IRQ10	Not used	Not used	Available
IRQ11	Not used	Not used	Available
IRQ12	Not used	Mouse	Not Available
IRQ13	Coprocessor	Not used	Not Available
IRQ14	Not used	Fixed Disk Controller	Available
IRQ15	Not used	Not used	Available

The I/O address for each register in the interrupt controllers is defined in the following table:

Table 3. I/O Addresses for Registers in the Interrupt Controllers

Master Interrupt Controller

ADDRESS	W/R	Function
		*** Initialization Mode ***
0020	W	initialization command word ICW1
0021	W	initialization command word ICW2, ICW3, ICW4
		*** Operation Mode ***
0021	W	operation control word OCW1
0020	W	operation control word OCW2, OCW3
		*** Read Status Register (Operation Mode) ***
0021	R	interrupt mask register (IMR)
0020	R	interrupt request register (IRR) and interrupt service register (ISR). IRR and ISR are selected through bit 0 and bit 1 in OCW3

Slave Interrupt Controller

ADDRESS	W/R	Function
		*** Initialization Mode ***
00A0	W	initialization command word ICW1
00A1	W	initialization command word ICW2, ICW3, ICW4
		*** Operation Mode ***
00A1	W	operation control word OCW1
00A0	W	operation control word OCW2, OCW3
		*** Read Status Register (Operation Mode) ***
00A1	R	interrupt mask register (IMR)
00A0	R	interrupt request register (IRR) and interrupt service register (ISR). IRR and ISR are selected through bit 0 and bit 1 in OCW3

The interrupt acknowledge cycle requires two wait states.

3.2 Timer Controller

The timer controller is compatible with the Intel 8254. It is a programmable interval timer/counter. The function of timer controller is to generate a constant system time and control the tone of the speaker. This controller contains three timer channels. Each channel is described as follows:

Channel 0:

This channel is a general purpose timer providing a constant time base for the operating system. The input clock (CLK IN 0) runs at 1.19 MHz frequency. The enable clock input (GATE 0) is always enabled after power up. The output (CLK OUT 0) of this channel is connected to interrupt channel 0 (IRQ0) of the interrupt controller (8259A).

Channel 1:

This channel is used to control the DRAM refresh cycles. The input clock (CLK IN 1) runs at 1.19 MHz. The enable clock input (GATE 1) is always enabled after power up. The output (CLK OUT 1) of this channel goes to OTI-051 to request a periodic DRAM refresh cycle.

Channel 2:

This channel controls the tone of the speaker. The input clock (CLK IN 2) runs at 1.19 MHz. The enable clock input (GATE 2) is turned on/off by bit 0 of system control register 061(Hex). When bit 0 of I/O PORT 061h is set to one, the frequency of tone is controlled by the counting number in the counter register 2. The output (CLK OUT 2) of this channel is connected to the driver of the speaker. After power on or reset, bit 0 of I/O port 061h is reset to zero. More detailed information will be described in the section on the system control register 061(Hex).

The I/O address for each register in the timer controller is defined below:

ADDRESS	W/R	Function
0040	W/R	counter register 0
0041	W/R	counter register 1
0042	W/R	counter register 2
0043	W	control mode register

The control mode register selects the operation mode for each channel in the timer controller. There are six different modes. They are listed below:

- mode 0: interrupt on terminal count
- mode 1: programmable one-shot
- mode 2: rate generator
- mode 3: square wave rate generator
- mode 4: software triggered strobe
- mode 5: hardware triggered strobe

More detailed information can be found in the Intel 8254 data sheet.

3.3 Serial Communication Controller

The OTI-052 chip incorporates a serial communication controller which can be optionally selected to be COM1 or COM2 through the BIOS set-up menu. The serial communication controller is fully compatible with the NS16450A. It will add and remove start, stop and parity bits. A programmable baud-rate generator allows operation from 50 baud to 9600 baud. These controllers support 5, 6, 7 and 8 bit characters with 1, 1.5 or 2 stop bits. A prioritized interrupt system controls transmitting, receiving, error, and line status as well as data-set interrupt. The clock applied to the serial communication controllers is 1.84 MHZ which is derived from the 32 MHz clock.

Addressing of the accessible registers in the serial communication controllers is shown in the table below.

Table 4. Addressing Registers in Serial Communications Controllers

DLAB	A2	A1	A0	Register
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Flag (read)
X	0	1	1	Byte Format
X	1	0	0	Modem Control
X	1	0	1	Line status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor LSB
1	0	0	1	Divisor MSB

Notes: X = Don't Care
    DLAB = Divisor Latch Access Bit

The serial port provides the following RS-232 signals which include modem control interfaces:

- RXD: Receive Data
- CTS: Clear To Send
- DSR: Data Set Ready
- DCD: Data Carry Detect
- RI: Ring Indicator
- TXD: Transmit Data
- DTR: Data Terminal Ready
- RTS: Request To Send

Interrupt of the serial communication controller in COM1 mode is internally connected to the IRQ4 of the interrupt controller in the OTI-052 chip. The I/O address for each register in the serial communication controller in COM1 mode is listed in the following table:

Table 5. I/O Addresses for Registers in Serial Communications Controller in COM1 Mode

ADDRESS	W/R	FUNCTION
03F8	W	transmitter holding register
03F8	R	receive buffer register
03F9	W/R	interrupt enable register
03FA	R	interrupt identification register
03FB	W/R	line control register
03FC	W/R	modem status register
03FD	R	line status register
03FE	R	modem status register
03FF	W/R	scratch register

Interrupt of the serial communication controller in COM2 mode is internally connected to the IRQ3 of the interrupt controller in the OTI-052 chip.

The I/O address for each register in the serial communication controller in COM2 mode is listed in the following table:

Table 6. I/O Address for Serial Communications Controllers in COM2 Mode

ADDRESS	W/R	FUNCTION
02F8	W	transmitter holding register
02F8	R	receive buffer register
02F9	W/R	interrupt enable register
02FA	R	interrupt identification register
02FB	W/R	line control register
02FC	W/R	modem status register
02FD	R	line status register
02FE	R	modem status register
02FF	W/R	scratch register

More detailed information can be found in National's data book.

3.4 Bi-directional Parallel Port Controller

The parallel port controller can be configured to be one of two modes. The first mode is "printer mode." The function of the printer mode is to attach a printer with parallel interface to the system. The second mode is "input mode" that allows the system to receive data through the parallel port from external devices when the direction bit in the printer control register is set to read. The input mode of the parallel port controller is selected by writing a 0 to bit 7 of POS byte 102(Hex). Refer to IBM's documentation for POS register definitions.

There are two output ports and three input ports in the parallel port controller. The following is a detailed description of each port.

Data port:

The data port is an 8-bit port for both the printer mode and input mode. For the printer mode, a write operation to this port immediately presents data to the connector pins. A read operation from this port in the printer port produces the data that was last written to it. In the input mode, a write operation to this port does not affect the output of the data port if the direction bit is set to read. A read operation in the input read mode produces the data on the connector pins from external devices.

Status Port:

The status port is a read-only port for either mode. When an interrupt is pending, the interrupt status bit is set to 0. The following table shows the bit definition of the status port:

Table 7. Bit Definition of the Status Port, Parallel Port Controller

Bit	Function	
7	BUSY-:	When this bit is active, the printer is busy and can not accept data.
6	ACK-:	When this bit is 0, the printer is ready to accept data.
5	PE-:	When this bit is set to 1, the printer has detected the end of the paper.
4	SLCT-:	When this bit is set to 1, the printer has been selected.
3	ERROR-:	When this bit is set to 0, the printer has detected an error condition.
2	IRQ-:	When this bit is set to 0, the printer has acknowledged the previous transfer using the "-ACK" signal.
1	Reserved	
0	Reserved	

Output Control Port:

The Output Control Port is a read or write port. The following table shows the bit definition of the Output Control Port:

Table 8. Bit Definition of the Output Control Port, Parallel Port Controller

Bit	Function	
7	Reserved	
6	Reserved	
5	Direction:	1 to enable read input mode
4	IRQ EN:	When this bit is set to 1, the interrupt logic is enabled.
3	SLCT IN:	This bit controls the "SLCT IN" signal on connector pin 17. When this bit is set to 1, the printer is selected.
2	INIT:	This bit controls the "-INIT" signal on connector pin 16. When this bit is set to 1, the printer starts.
1	AUTO-FD:	This bit controls the "AUTO-FD" signal on connector pin 14. When this bit is set to 1, the printer will automatically line feed after each line is printed.
0	STROBE:	This bit controls the "STROBE" signal on connector pin 1. When this bit is set to 1, data is pulse-clocked into the printer.

An interrupt from the parallel port controller is connected to IRQ7 of the interrupt controller in OTI-052. This port can be configured into either LPT1, LPT2 or LPT3. The I/O address for each register in different port configurations is listed in the following table:

Table 9. I/O Addresses for Parallel Port Controller Registers

PORT NO.	ADDRESS	W/R	Function
LPT1	03BC	W/R	data register
LPT2	0378	W/R	data register
LPT3	0278	W/R	data register
LPT1	03BE	W/R	printer control register
LPT2	037A	W/R	printer control register
LPT3	027A	W/R	printer control register
			b7 - b6 not used
			b5 = Direction
			(1=input, 0=output)
			b4 = enable/disable interrupt
			(1=enable,0=disable)
			b3 = select printer device
			(1=select, 0=not select)
			b2 = start printer device
			(1=stop, 0=start)
			b1 = enable line feed
			(1=enable, 0=disable)
			b0 = data strobe
			(1=data valid, 0=data invalid)
LPT1	03BD	W/R	status register
LPT2	0379	W/R	status register
LPT3	0279	W/R	status register
			b7 = printer busy
			(1=not busy, 0=busy)
			b6 = printer acknowledge
			(1=no-ACK, 0=ACK)
			b5 = end of paper
			(1=no paper, 0=paper)
			b4 = printer selected
			(1=selected, 0=not selected)
			b3 = printer error
			(1=no error, 0=error)
			b2 = IRQ status
			b1-b0 = not used

3.5 Floppy Disk Controller Address Decode and Control Registers

OTI-052 is capable of decoding the I/O address and generating the select signal for the on-board floppy disk controller. OTI-052 can also control the data buffer between the I/O extended bus and the I/O Channel during an I/O cycle or DMA cycle for the floppy disk controller.

RAS A Port and RAS B Port are implemented externally, OTI-052 generates the chip select signal for these two ports.

Table 10. Floppy Disk Controller Address and Cotrol Registers

ADDRESS	W/R	FUNCTION	
RAS A PORT			
03F0	R	b7 =	IRQ6
		b6 =	DRQ2
		b5 =	step (latched)
		b4 =	track 0
		b3 =	head 1 select
		b2 =	index
		b1 =	write protect
		b0 =	direction
RAS B PORT			
03F1	R	b7 =	not used
		b6 =	drive select 1
		b5 =	drive select 0
		b4 =	write data (latched)
		b3 =	read data (latched)
		b2 =	write enable (latched)
		b1 =	drive select 3
		b0 =	drive select 2
DIGITAL OUTPUT REGISTER			
03F2	W	b6-7=	reserved
		b5 =	motor enable 1
		b4 =	motor enable 0
		b3 =	DMA and interrupt enable
		b1,b0 =	drive select
			00 selects drive 0
			01 selects drive 1
			10 selects drive 2
			11 selects drive 3
DIGITAL INPUT REGISTER			
03F7	R	b7 =	diskette change
		b6-b4=	reserved
		b3 =	DMA enable
		b2 =	No write precomp
		b1 =	250 rate select
		b0 =	high density select
CONFIGURATION CONTROL REGISTER			
03F7	W	b7-3 =	reserved = 0
		b2 =	No write precomp
		b1 =	250 rate select
		b0 =	used only for 1.2M drive

More detailed information on all the floppy control and status registers can be found in the specification on Oak Technology's floppy controller and data separator chip (OTI-033) and in NEC's floppy controller (NEC 765) data sheet.

3.6 Address Decode for Hard Disk Controller

OTI-052 is capable of decoding the I/O address for the on-board hard disk controller and generating the select signal for the controller. OTI-052 can also control the data buffers between the I/O extended bus and I/O Channel during an I/O cycle or DMA cycle for the hard disk controller. The I/O address range for the PS/2 hard disk controller is between 320(Hex) to 32F(Hex). It uses DMA channel 3 for DMA access. OTI-052 also supports IDE-type hard disk drives. The I/O range for IDE-type drives is 1F0-1F7 and 3F6-3F7(Hex).

3.7 Power Management

OTI-052 incorporates several activity monitors, which together with the power management circuits residing in the other chips of the chipset, enable the system designer to design a very power efficient laptop system.

3.8 System Control and Status Registers

These I/O ports reside in OTI-052 and are used to either control the system or provide various system status.

System Control Register PORT B (061h)

The system control register (061h) is used for speaker control, I/O channel check, and memory parity check enable on the system board. This register is a read/write port. However, the port is only writable in OTI-052. When port 61(Hex) is being read, data would be coming from OTI-051. The bit definitions of this register are defined as follows:

ADDRESS	W	Function
0061		
	W	b1=speaker data, enable/disable the output of 8254-timer 2 (1=enable,0=disable,default=disable)
	W	b0=enable/disable 8253-Timer 2 (1=enable,0=disable,default=disable)

Bit 1 is used to gate speaker data. This bit gates the output of timer 2. It can disable the timer's sound source or modify its output. When set to 1, this bit enables the output. When cleared to 0, it forces the output to zero.

Bit 0 is routed to the timer input at GATE 2. When this bit is cleared to 0, the timer operation is halted. This bit and bit 1 (speaker data) control the operation of the timer's sound source.

After power on or reset, this register is cleared.

3.9 Co-processor Interface

OTI-052 supports both the 80287 and the 80387SX co-processors. When an 80286 is used as the CPU, the 80287 is supported. When an 80386SX is used as the CPU, either an 80287 or 80387SX can be used as the co-processor.

OTI-052 decodes I/O address range 0F8-0FF(Hex) for the co-processor. During hardware reset, OTI-052 latches the status of NPERR- from the co-processor into bit 6 of control/status port 2. If the latched bit is low, it implies an 80387SX is used; if the bit is high, an 80287 is assumed. BIOS should then detect the existence of the co-processor and set bit 3 of the system status register 2.

OTI-052 generates IRQ13 and drives BUSYCPU- low when NPERR- is active. And if an 80386SX is used, CPEREQ and NPCS- will be forced high. INTA- signal is used to clear the above latched error condition. BIOS can also write to ports F0 and F1 to clear it. IRQ13 is reset to low only by writing to F0 or F1.

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4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 11. A.C. Characteristics of OTI-052

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t1	Timer Output Delay		180	ns	CL=150 pF
t2	IRQ to INTR		90	ns	CL=150 pF
t3	INTAN to XD Valid		150	ns	
t4	XD Invalid from INTAN	5		ns	
t5	Address SETUP Time	50		ns	
t6	SEL0 SETUP Time	40		ns	
t7	WRITE Data SETUP Time	100		ns	
t8	WRITE Data HOLD Time	20		ns	
t9	READ Data Valid from IORDN		100	ns	CL=200 pF
t10	READ Data Float from IORDN	5		ns	CL=200 pF
t11	XBFRDN from READ Command		45	ns	
t12	Chip Selects from Address		40	ns	CL=50 pF
t13	Floppy Port Read Command		40	ns	
t14	Floppy Control from IOWRN		45	ns	
t15	Printer Control from IOWRN		45	ns	CL=150 pF
t16	BUSYCPU from IOWRN		10	ns	
t17	CPEREQ from IOWRN		10	ns	
t18	NPCSN(387SX) from IOWRN		10	ns	
t19	NPCSN(287) from IOWRN		10	ns	
t20	BUSYCPU from NPBSYN		30	ns	
t21	CPEREQ from NPERRN		35	ns	
t22	NPCSN(287) from NPERRN		35	ns	
t23	NPCSN(387SX) from NPERRN		35	ns	

4.2 DC Characteristics

Table 12. DC Characteristics of OTI-052

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output High Voltage	2.4		V	IOH=400 μA
VOL1	Output Low Voltage		0.45	V	IOL=20 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL=16 mA, Note 1
VOL3	Output Low Voltage		0.45	V	IOL=10 mA, Note 1
VOL4	Output Low Voltage		0.45	V	IOL= 8 mA, Note 1
VOL5	Output Low Voltage		0.45	V	IOL= 4 mA, Note 1
VOL6	Output Low Voltage		0.45	V	IOL= 2 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmitt Input High	2.4	Vdd+0.5	V	Schmitt, Note 2
VIC	CMOS Input High Voltage	3.8	Vdd+0.5	V	CMOS, Note 2
ILI	Input Leakage Current	- 10	10	μA	
OLI	Output Leakage Current	- 10	10	μA	
ICC	Operating Supply Current		30	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

1. Output Current (IOL) Capabilities:

20 mA :	HIGDNTY, PD0 - PD7
10 mA :	STROBE-, INIT-, AUTOFD-, SELIN-
8 mA :	DATA0-7, SELHDK-, HDINS-
4 mA :	NPCS-, BUSYCPU, CPEREQ, SELKBD-, RTS1-, DTR1-, TXD1,FLPCS-, RD3F0-, RD3F1-, SPKOUT, TIMEOUT2, XBFRD-, REFREQ, INTR
2 mA :	PREN, DRVTYPE, IRQ3,4,7

2. Input Structures:

Schmitt Triggered :	LKSER, CLK14, MINCLK
CMOS :	
TTL :	All Others
Input With Pullup :	NPERR-, NPBSY-, RXD1, DCD1-, RIN1-, DSR1-, CTS1-, IRQ

5.0 OTI-052 TIMING DIAGRAMS

FIGURE 2-1.

TIMING/COUNTER TIMING

CLK14

REFREQ,
SPKOUT,
TIMER2

INTERRUPT CONTROLLER TIMING

IRQ1-15

INTR

INTAN

XDATA7-0

I/O CYCLE TIMING

SARD9-0

SEL0

IOWRN

XDATA7-0

IORDN

XDATA7-0
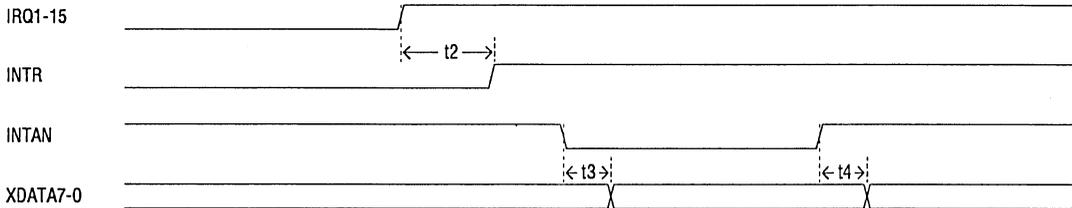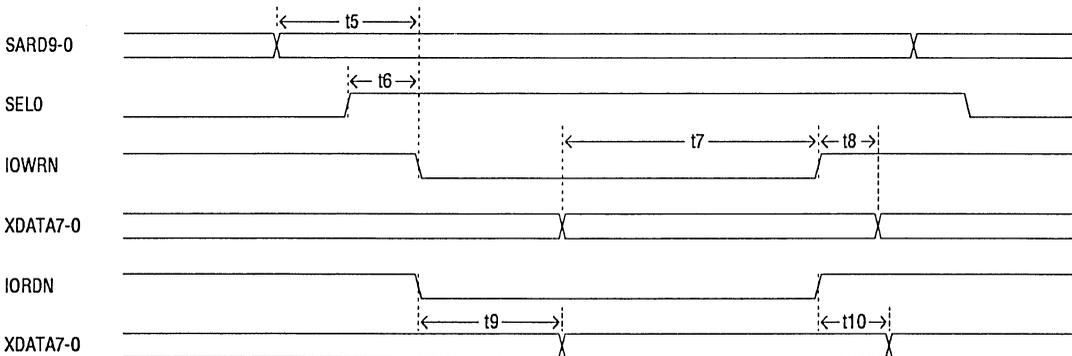
FIGURE 2-2.

X-BUFFER CONTROL TIMING
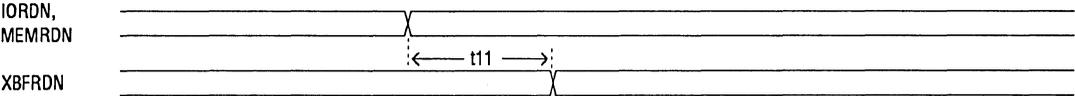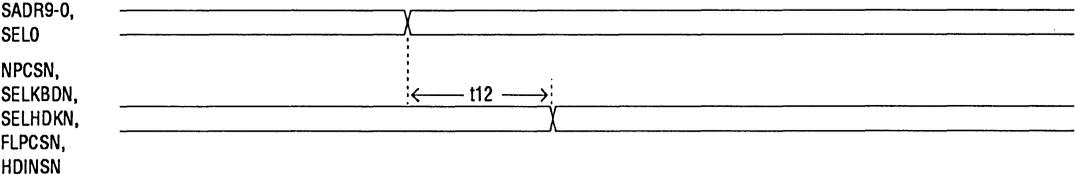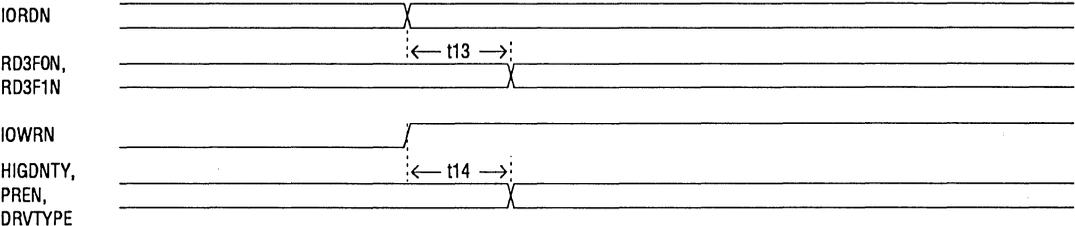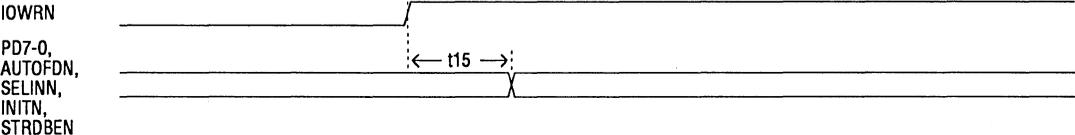
IORDN,
MEMRDN

$\leftarrow$ t11 $\rightarrow$

XBFRDN

CHIP SELECT TIMING

SADR9-0,
SEL0

NPCSN,
SELKBDN,
SELHDKN,
FLPCSN,
HDINSN

$\leftarrow$ t12 $\rightarrow$

FLOPPY CONTROL TIMING

IORDN

RD3FON,
RD3F1N

$\leftarrow$ t13 $\rightarrow$

IOWRN

HIGDNTY,
PREN,
DRVTYPE

$\leftarrow$ t14 $\rightarrow$

PRINTER CONTROL TIMING

IOWRN

PD7-0,
AUTOFDN,
SELINN,
INITN,
STRDBEN

$\leftarrow$ t15 $\rightarrow$

FIGURE 2-3.

I/O TIMING

IOWRN	
BUSYCPU	t16
CPEREQ	t17
NPCSN (80387SX)	t18
NPCSN (80287)	t19

CO-PROCESSOR TIMING

NPBSYN	
NPERRN	
BUSYCPU	t20
CPEREQ	t21
NPCSN (80287)	t22
NPCSN (80387SX)	t23

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SECTION 3
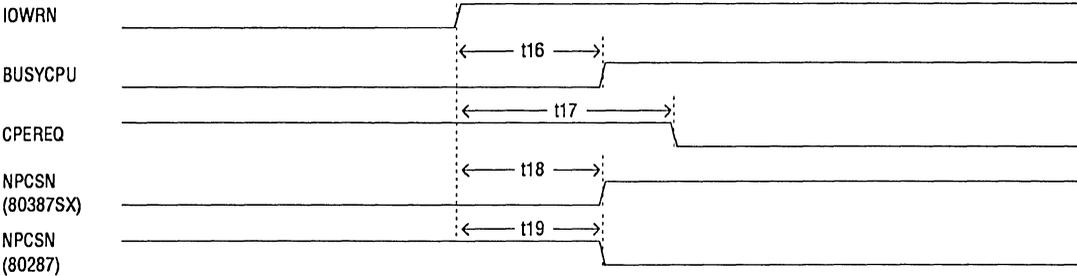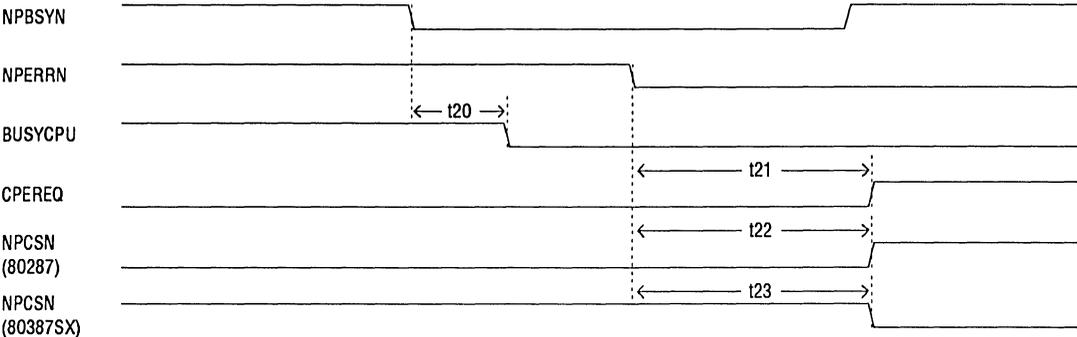
OTI-053

DMA & MEMORY CONTROLLER

1.0 INTRODUCTION TO OTI-053 DMA AND MEMORY CONTROLLER

OTI-053 integrates all the functions of a DMA controller and memory controller.

A summary of the special features provided by OTI-053 is listed below:

Memory Control: - page mode and interleave mode for zero wait state cycles

- supports 60ns up to 120ns DRAMs

- system speed up to 20 MHz

- programmable wait states for slower speed DRAMs

- zero wait state ROM cycle with shadow RAM

- EMS 4.0

- supports 640 KB of system memory up to 8MB of total on-board memory including extended/expanded memory.

- supports 256K and 1M type DRAMs

- supports pseudo-SRAM for laptop model

- cartridge ROM support

DMA Control: - supports fast and normal DMA mode with embedded 8237 at up to 10 MHz

Laptop Support: - power saving scheme

System Block Diagram

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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-053 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
			*** SYSTEM INTERFACE ***
SA1-SA19 SA21-23	48-54,56-62,64-68 71-73	I/O	ADDRESS LINE (1-19,21-23): SA21-SA23 are the CPU address lines (unlatch).
A0	47	I/O	ADDRESS LINE 0: address line from OTI-051.
A20	70	I/O	ADDRESS LINE 20: address line 20 from OTI-051 gated by 8042 output and port 92(Hex) output.
S0-/WR- S1-/DC-	40 39	I	BUS CYCLE STATUS: These signals together with M/IO and COD/INTA- are used to decode different bus cycles.
M/IO-	37	I	MEMORY OR I/O CYCLE: is an input signal from the CPU indicating whether the present cycle is memory or I/O access.
SRDY-	45	I/O	SYSTEM READY: is an active low signal to acknowledge the CPU that the data transfer for system memory is complete.
BHE-	46	I/O	BYTE HIGH ENABLE: is an active low signal used to enable data onto the most significant half of the data bus (D15 - D8). It is an input line when the CPU is in control. OTI-051 starts driving this signal during the DMA and refresh time.
ADS-	41	I	ADDRESS STROBE: is an active low signal coming from 80386SX. This pin is also used to detect whether an 80286 or 80386SX is used.
CPUCLK	43	I	CPU CLOCK: is a 50% duty cycle input clock.
RESET	42	I	RESET: is an active high signal synchronized to the system clock to reset the system.
			*** DMA INTERFACE ***
DRQ0-3 DRQ5-7	100-97 96,95,93	I	DMA REQUEST (0-3,5-7): are asynchronous active high signal channel request inputs used by peripheral devices to obtain DMA service. DACK will acknowledge the recognition of a DRQ signal. These signals are compatible to the DRQ signals of 8237.
DACK0-3 DACK5-7	92-89 88,86,85	O	DMA ACKNOWLEDGE: are active low signals to notify the individual peripherals when one has been granted a DMA cycle. These signals are compatible to the DACK signals of 8237.
TC	79	O	TERMINAL COUNT: is an active high output pulse signal when the terminal count for any DMA channel is reached.
AEN	80	O	ADDRESS ENABLE: is an active high signal during the DMA cycle to degate the I/O devices from the I/O channel to allow DMA transfers to take place.
CPUHRQ	78	O	HOLD REQUEST: is an active high signal connected directly to HOLD of the CPU. This signal is used by the chip to request the bus from the CPU.
CPUHLDA	77	I	HOLD ACKNOWLEDGE: is an active high signal connected directly to HLDA of the CPU. This signal is used by the chip to determine if the bus request has been granted by the CPU.

Table 1. OTI-053 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
IOCHRDY	76	I	I/O CHANNEL READY: is an active high ready signal from an I/O channel. It is pulled low in active by a memory or I/O device to lengthen memory or I/O cycles. For every system clock cycle this signal is inactive, one wait state is added.
MASTER-	75	I	MASTER: this signal is used together with a DRQ line to gain control of the system.
IORD-	83	I/O	I/O READ COMMAND: active low command to instruct an I/O device to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
IOWR-	84	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus. This pin becomes an input during the MASTER mode.
MEMRD-	81	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
MEMWR-	82	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus. This pin becomes an input during the MASTER mode.

*** MEMORY INTERFACE ***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
REFREQ	34	I	MEMORY REFRESH REQUEST: is the memory request signal from 8253 Timer channel 1 which comes from OTI-052.
COMRQ-	33	I/O	COMMAND REQUEST: active low bidirectional signal. In the input phase, it receives a signal from OTI-051 indicating when to wake up from the SHUTDOWN mode. In the output phase, it requests the OTI-051 to generate the PC memory cycle. The signal is in the input phase when AEN is HIGH, and it is in the output phase during other times.
MREF-	31	I/O	MEMORY REFRESH: is an active low signal indicating that a refresh cycle is going on. It is forced low when D/SRAM- is low to enable the self-refresh feature of the pseudo-static RAM during the SHUTDOWN mode.
CLK8	36	I	8 MHZ CLOCK: is an 8 MHz 50% duty cycle clock input to the RAS pulse width counter as well as the memory refresh counter.
MDIR	32	O	MEMORY DIRECTION: is the status signal to memory write enable of memory devices and also the data direction transceiver between the CPU and system memory bus: MDIR = high ==> memory read MDIR = low ==> memory write MDIR is normally low. It becomes high when: 1. Non-DMA, system memory read cycle. 2. Non-DMA, ROM access cycle. 3. DMA, system memory read cycle.
MA(1-10)	11-7,5-1	I/O	MEMORY ADDRESS (1-10): During memory cycles, it is a time multiplexed memory address bus for 1M memory type (for 256K memory type MA(10) is not used). During the memory cycle, MA(1-10) is the row address output until 1 unit time delay has elapsed, and then the MA(1-10) starts outputting the column address. MA1-8 is multiplexed with XDATA during I/O cycles.
/XD7 - XD0	3-5,7-11	I/O	XDATA BUS: bi-directional data lines to/from the I/O channel bus. It is multiplexed with MA8-1 during I/O cycles.

Table 1. OTI-053 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
RAS0- - RAS7-	21-18,16-13	O	ROW ADDRESS STROBE (0 - 7): If D/SRAM- is high, they are active low control signals to the DRAM system memory to inform that a row address is present on the address bus. RAS0 and RAS1 are for the first memory bank, RAS2 and RAS3 are for the 2nd bank, RAS4 and RAS5 are for the third bank and RAS6 and RAS7 are for the last bank.
/SRA(14 - 17)	21-18	O	SRAM ADDRESS (14 - 17): If D/SRAM- is low, they are the four most significant addresses of the 128K x 8 pseudo-SRAM. SRA(14-17) are multiplexed with RAS(0-3)- using D/SRAM- as select.
/SRA(18 - 21)	16-13	O	SRAM ADDRESS (18 - 21): If D/SRAM- is low, they are inputs to the pseudo- SRAM address decoder for the Expanded/Extended Memory option. The combinations of SRA(18 - 21) are capable of selecting 128K x 8 pseudo-SRAM organized word wide for a total of 4M minus 256KB. Expanded/extended memory is not selected if SRA(18 - 21) are 1111. SRA(18-21) are multiplexed with RAS(4-7)- using D/SRAM- as select.
CASH3-0- CASL3-0-	22-25,27-30	O	COLUMN ADDRESS STROBE (High and Low): If D/SRAM- is high, they are active low control signals to the on-board DRAM system to inform that a column address is present on the address bus: - CASH- for odd byte [D(15-8)]. - CASL- for even byte [D(7-0)].
/SRCS(0 - 3)-	22-25	O	STATIC RAM CHIP SELECT (0 - 3): If D/SRAM- is low, these are the pseudo-Static RAM Memory Chip Selects (active low signals). SRCS(0-3)- are multiplexed with CASH3-0 using D/SRAM- as select. Each signal selects 2 banks of 128K x 8 type pseudo-SRAM for a total of 1MB of memory: **SIGNAL** **MEMORY SPACE** SRCS0- 00000 - 7FFFF(even word) SRCS1- 00000 - 7FFFF(odd word) SRCS2- 80000 - FFFFF(even word) SRCS3- 80000 - FFFFF(odd word)
/SRE-	27	O	SRAM READ ENABLE: If D/SRAM- is low, it is an active low read enable signal for SRAM memory. SRE- is multiplexed with CASL3- using D/SRAM- as select.
/MRAS-	28	O	STATIC RAM TIMING: IF D/SRAM- is low, it is an active low signal used for SRAM memory timing. MRAS- is multiplexed with CASL2- using D/SRAM- as select.
/SWEH- SWEL-	29-30	O	SRAM WRITE ENABLE (high and low): If D/SRAM- is low, they are active low write enable signals for SRAM: - SWEH- for odd byte. - SWEL- for even byte. SWEH- and SWEL- are multiplexed with CASL1- and CASL0- using D/SRAM- as select.
CROMCS0-	35	O	CARTRIDGE ROM CHIP SELECT: is an active low signal used to enable the CARTRIDGE ROM to output data on to the data bus.
VDD	12,38,63,74		POWER: +5 V supply, 4 pins
VSS	6,17,26,44, 55,69,87,94		GROUND: 8 pins

Pin diagram for OTI-053 (100-pin QFP).

Top side (pins 100–81):

DRQ0 (100), DRQ1 (99), DRQ2 (98), DRQ3 (97), DRQ5 (96), DRQ6 (95), VSS (94), DRQ7 (93), DACK0 (92), DACK1 (91), DACK2 (90), DACK3 (89), DACK5 (88), VSS (87), DACK6 (86), DACK7 (85), IOWR- (84), IORD- (83), MEM WR- (82), MEMRD- (81)

Left side (pins 1–30):

Pin	Signal
1	MA10
2	MA9 (Index)
3	MA8/XD7
4	MA7/XD6
5	MA6/XD5
6	VSS
7	MA5/XD4
8	MA4/XD3
9	MA3/XD2
10	MA2/XD1
11	MA1/XD0
12	VDD
13	RAS7-/SRA21
14	RAS6-/SRA20
15	RAS5-/SRA19
16	RAS4-/SRA18
17	VSS
18	RAS3-/SRA17
19	RAS2-/SRA16
20	RAS1-/SRA15
21	RAS0-/SRA14
22	CASH3/SRCS0-
23	CASH2/SRCS1-
24	CASH1/SRCS2-
25	CASH0/SRCS3-
26	VSS
27	CASL3/SRE
28	CASL2/MRAS
29	CASL1/SWEH
30	CASL0/SWEL

Right side (pins 80–51):

Pin	Signal
80	AEN
79	TC
78	CPUHRQ
77	CPUHLDA
76	IOCHRDY
75	MASTER-
74	VDD
73	SA23
72	SA22
71	SA21
70	A20
69	VSS
68	SA19
67	SA18
66	SA17
65	SA16
64	SA15
63	VDD
62	SA14
61	SA13
60	SA12
59	SA11
58	SA10
57	SA9
56	SA8
55	VSS
54	SA7
53	SA6
52	SA5
51	SA4

Bottom side (pins 31–50):

MREF- (31), MDIR (32), COM RQ- (33), REF REQ (34), CRO MCS0 (35), CLK8 (36), M/10 (37), VDD (38), S1-/DL- (39), S0-IWR- (40), ADS- (41), RE SET (42), CPU CLK (43), VSS (44), SRDY- (45), BHE- (46), A0 (47), SA1 (48), SA2 (49), SA3 (50)

3.0 OTI-053 FUNCTIONAL DESCRIPTION

OTI-053 functions can be categorized as follows:

1.   Memory Control Unit

2.   DMA Control

3.   Arbiter and Refresh Control

4.   Miscellaneous

3.1 Memory Control Unit

OTI-053 offers either a Dynamic or Pseudo-Static RAM memory control unit depending on the D/SRAM- input signal in OTI-055. If the D/SRAM- input is not available, then the system defaults to dynamic memory support.

- If D/SRAM- is strapped high (to VCC), OTI-053 will exercise on-board DRAM memory control. It supports 640KB of system memory plus another 384KB for shadow RAM implementation, EMS or remapped to above the 1M address space. OTI-053 supports full specification of EMS 4.0 which makes multitasking possible. The chip supports both 256K and 1M type memories. The memory size can vary from a minimum of 1 MB to a maximum of 8 MB.

- If D/SRAM- is strapped low (to GROUND), OTI-053 will exercise on-board pseudo-SRAM memory control. It supports 640KB of system memory and 384K of EMS memory using 128K x 8 type of pseudo-SRAM. It also supports pseudo-SRAM up to 4M minus 256KB of 128K x 8 type of memory for memory addresses above the 1M boundary. It provides 4 bit address select [SRA(18 - 21)] that can select 1 out of 16 banks of memory (256KB each). However, if EMS SRAM is not accessed, SRA(18 - 21) will be all 1's. Hence, only 15 possible ways are used. The decoding has to be done external to the chip on the mother board.

The function of Memory Control Units can be broken down to 5 sub-blocks:
   1. System Memory Control
   2. EMS Control
   3. Memory Request Control
   4. Memory Parity
   5. Memory Address Generator

3.1.1 System Memory Control

3.1.1.1 System ROM Area

Two ROM address spaces are implemented:
   0E0000 - 0FFFFF (128K)
   FE0000 - FFFFFF (128K)

Physical ROM area is only 128KBytes, therefore both address spaces address the same physical ROM. Shadow RAM implementation is adopted for zero wait state operation. Shadow RAM address space covers:
   0C0000 - 0CFFFF (video ROM area)
   0D0000 - 0DFFFF (PC bus external device ROM area)
   0E0000 - 0EFFFF (Model 30 - 286 BIOS area or EMS area)
   0F0000 - 0FFFFF (Model 30 - 286 BIOS area)

An indexed port 19(Hex) can be programmed to indicate to the system whether the memory space is used for shadow RAM implementation. If the address space is not used, then it can be used as expanded memory or mapped to 1M through 1.384M address space. Protection circuitry on-chip can prevent writing to the shadow RAM area after the RAM content is loaded. The shadow RAM area is write enabled after power-up.

The sequence of loading after power-up is listed below:
   1. ROM read cycles to download contents from ROM to shadow RAM area (wait states for slow ROM access time).
   2. Disable access to physical ROM, enable shadow RAM write protection circuitry for ROM BIOS. Only RAM READ cycles are generated afterward.
   3. Download video ROM content to shadow RAM.
   4. Disable access to physical ROM, enable shadow RAM write-protection circuitry. Only RAM READ cycles are generated for the address space.

3.1.1.2 System Memory Map

Tabel 2. System Memory Map

System ROM	FFFFFF(Hex)
	FE0000(Hex)
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	
Expanded Memory	Boundary detected by EMM driver
Extended Memory	Boundary determined by register
	100000(Hex)
Shadow RAM/Expanded Memory	0FFFFF(Hex)
	0A0000(Hex)
System Memory	09FFFF(Hex)
	000000(Hex)

RAS, CAS are generated for the 640K system memory space if they are enabled by the planar RAM register. PC cycles are generated if the memory space is disabled through the SYSTEM BOARD MEMORY ENABLE register.

0F0000 - 0FFFFF	ROM READ and RAM WRITE cycle during initialization, RAM READ only after it is write-protected
0E0000 - 0EFFFF	ROM READ and RAM WRITE cycle during initialization, RAM READ only after it is write-protected. If it is not used as shadow ROM, PC cycles are generated to the PC bus. If it is used as shadow ROM, none of the EMS registers should be mapped to this area.
0D0000 - 0DFFFF 0C0000 - 0CFFFF	PC cycles generated during initialization, RAM READ only after it is write-protected. If it is used as shadow ROM, no EMS register should be mapped to this area. PC cycles are generated if it is not used as shadow ROM.

If neither Shadow RAM nor EMS is used, the physical memory between 0A0000(Hex) to 0FFFFF(Hex) can be mapped to the address space 1M to 1.384M through the POS register or indexed port 1A(Hex).

3.1.1.3 Shadow RAM Control Registers

Shadow RAM Control Register 0: I/O Port Index 0018(Hex) R/W:

Bit	Function
7	DIS/EN- WRITE TO SHADOW RAM, C0000-C3FFF
6	DIS/EN- WRITE TO SHADOW RAM, C4000-C7FFF
5	DIS/EN- WRITE TO SHADOW RAM, C8000-CBFFF
4	DIS/EN-WRITE TO SHADOW RAM, CC000-CFFFF
3	EN/DIS- SHADOW RAM, C0000-C3FFF
2	EN/DIS- SHADOW RAM, C4000-C7FFF
1	EN/DIS-SHADOW RAM, C8000-CBFFF
0	EN/DIS-SHADOW RAM, CC000-CFFFF

At Power On or Reset, the content of Shadow RAM Control Register 0 is 00.

Shadow RAM Control Register 1:I/O Port Index 0019(Hex) R/W:

Bit	Function
7	Not used
6	DIS/EN- WRITE TO SHADOW RAM, D0000-DFFFF
5	DIS/EN- WRITE TO SHADOW RAM, E0000-EFFFF
4	DIS/EN- WRITE TO SHADOW RAM, F0000-FFFFF
3	Not used
2	EN/DIS- SHADOW RAM, D0000-DFFFF
1	EN/DIS- SHADOW RAM, E0000-EFFFF
0	EN/DIS- SHADOW RAM, F0000-FFFFF

At Power On or Reset, the content of Shadow RAM Control Register 1 is 00.

3.1.1.4 System Memory Configurations

The 640K of system memory can be disabled individually in 128K blocks. At power-up, if certain memory is determined to be bad by POST, or if I/O memory is detected in any of the 5 blocks, POST will automatically disable that particular memory block by writing to System Board Memory Enable Register (port 104(Hex)).

System Board Memory Enable Register: I/O Port 0104 (Hex) R/W:

Bit	Function	
7-5	Not used	
4	Enable/Disable- 5th Bank	080000-09FFFF
3	Enable/Disable- 4th Bank	060000-07FFFF
2	Enable/Disable- 3rd Bank	040000-05FFFF
1	Enable/Disable- 2nd Bank	020000-03FFFF
0	Enable/Disable- 1st Bank	000000-01FFFF

At Power On or Reset, the content of port 104(Hex) is 1F(Hex).

OTI-053 supports both 256K type and 1M type DRAMs. In order to extract the highest performance out of the memory system, both page mode and interleave mode memory accessing techniques are implemented.

Maximum page size for 256K DRAM is 512 x 2bytes = 1 KBytes, and 1K x 2 Bytes = 2 KBytes for 1M type DRAM. Interleaving is done at page boundaries, which could increase the page size by 2.

Two-way Interleaved Memory: between BANK 0 and 1 or BANK 2 and 3

BANK 0	BANK 1
Page 0	Page 1
Page 2	Page 3
.	.
.	.
.	.
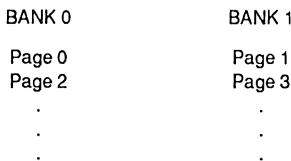
Four-way Interleaved Memory:

BANK 0	BANK 1	BANK 2	BANK 3
Page 0	Page 1	Page 2	Page 3
Page 4	Page 5	Page 6	Page 7
.	.	.	.
.	.	.	.

Since interleaving is done at the page boundary, it is unlikely that a program executing in the page could exceed the page boundary of 1KB or 2KB. With two-way interleaved memory, it is not likely that consecutive memory access will be from a different page on the same bank. Interleaving at the page boundary is better than interleaving at even and odd bytes, in which case there will be a problem if consecutive memory access is on even bytes alone (e.g. access an array with all even indices).

Table 3. Total Memory Size Versus Memory Type

Memory Size	BANK 0	BANK 1	BANK 2	BANK 3
1M	256K-RAS0,1	0	0	0
1M	256K-RAS0	256K-RAS2	0	0
2M	256K-RAS0,1	256K-RAS2,3	0	0
2M	256K-RAS0	256K-RAS2	256K-RAS4	256K-RAS6
2M	1M-RAS0	0	0	0
3M	256K-RAS0,1	0	1M-RAS4	0
3M	256K-RAS0	256K-RAS2	1M-RAS4	0
3M	256K-RAS0,1	256K-RAS2,3	256K-RAS4,5	0
3M	256K-RAS0,1	256K-RAS2,3	256K-RAS4	256K-RAS6
4M	256K-RAS0,1	256K-RAS2,3	256K-RAS4,5	256K-RAS6,7
4M	1M-RAS0	1M-RAS2	0	0
5M	256K-RAS0,1	0	1M-RAS4	1M-RAS6
5M	256K-RAS0	256K-RAS2	1M-RAS4	1M-RAS6
5M	1M-RAS0	1M-RAS2	256K-RAS4	256K-RAS6
5M	1M-RAS0	1M-RAS2	256K-RAS4,5	
6M	256K-RAS0,1	256K-RAS2,3	1M-RAS4	1M-RAS6
6M	1M-RAS0	1M-RAS2	256K-RAS4,5	256K-RAS6,7
8M	1M-RAS0	1M-RAS2	1M-RAS4	1M-RAS6

RAS0, RAS2, RAS4, RAS6 are to be used for both 256K type or 1M type DRAMs. RAS1, RAS3, RAS5, RAS7 are only to be used with 256K type of DRAMs. OTI-053 supports up to 8MB of memory including system memory, shadow RAM, extended memory and expanded memory.

3.1.1.5 RAS Pulse Width Counter

There is a limitation to the number of consecutive DRAM cycles. The RAS pulse width cannot exceed a certain spec (10,000ns, 30,000ns or 100,000ns). A register is provided for the user to set the spec. A counter counts the number of consecutive memory accesses to the same page and would raise the RAS if the maximum count is exceeded. Wait states would be inserted to accommodate the RAS precharge time, and the next memory access can then continue with the counter being reset to zero.

3.1.1.5 Memory Timing Schemes

Two memory timing schemes are used to accommodate the different system speed requirements.

Scheme 1	Used at 8 or 10 MHz system speed. There is one wait state added at page miss for RAS precharge at 8 or 10 MHz operations. The scheme supports 120ns DRAMs with a zero wait state when there is a page hit.
Scheme 2	Used at 12.5, 16 and 20 MHz system speed. The default timing would be 1 wait state during normal access and 3 wait states during page miss and one wait state for the start of the first memory access from other cycles. This default timing would support 120ns DRAMs running up to 20 MHz system speed. User programmability (indexed port 03(Hex)) is added so that the user can reduce the number of wait states if he is using higher speed memories or running at a slower system speed.

Table 4. Wait States versus Memory Speed

DRAM SPEED	SYSTEM SPEED (MHZ)				
	8	10	12.5	16	20
120NS	0/0/1	0/0/1	1/0/2	2/0/3*	-
100NS	0/0/1	0/0/1	1/0/2	2/0/3*	2/0/3*
80NS	0/0/1	0/0/1	1/0/2	1/0/2	2/0/3
60NS	no page	no page	no page	no page	1/0/2

wait state at 1st access / wait state for page hit / wait state for page miss

* 2/1/3 may be required for slow DRAMs.

During no page mode, memory system is running at zero wait state for memory read and 1 wait state for memory write.

PSEUDO SRAM SPEED	SYSTEM SPEED (MHZ)				
	8	10	12.5	16	20
120NS	no wait	1/0	1/0	2/1	2/1
100NS	no wait	no wait	1/0	2/1	2/1

w.s. on CE- pulse width / w.s. on CE- precharge

3.1.1.6 Pseudo-SRAM Control

The system memory control generates 4 SRAM chip selects [SRCS(0 - 3)-] and read/write control signals (SRE-, SWEH-, SWEL-):

SIGNAL	MEMORY SPACE
SRCS0 -	00000 - 7FFFF(even word)
SRCS1 -	00000 - 7FFFF(odd word)
SRCS2 -	80000 - FFFFF(even word)
SRCS3 -	80000 - FFFFF(odd word)

Address lines SRA(14-17) are the most significant bits for the 128k x 8 pseudo-static RAM. Address lines SRA(18-21) are used to decode the additional 4M - 256KB of expanded/extended memory. External decoding logic is required. SRA(18-21) is qualified with MRAS- in the external decoder. The SRCS- lines should be connected to the OE- signal of the pseudo-static RAMs. The user can select either a one wait state operation or a two wait state operation by programming indexed port 1B(Hex) to the appropriate value. During power-down mode, MREF- will stay at low all the time to start the SELF-REFRESH mode of the pseudo-static RAM. MREF- should be tied to the /RFSH signal of the pseudo-SRAM.

The default memory type is DRAM. Pseudo-SRAM mode is selected by programming 0 to bit 4 on index port 1E.

3.1.2 EMS 4.0 and Cartridge ROM Control

EMS Control consists of EMS Current Map, EMS Alternate Map and EMS memory parity check and parity generator.

Current and Alternate Maps are 60 words by 10-bit register files each, containing enable bit and the physical address 22 to 14 of the EMS memory: MAP(0:9). The memory space is logically broken down into 64 pages of 16KB each. However, the ROM BIOS area (F0000 - FFFFF) is reserved and is not mappable to the EMS memory. Each block of 16KB size can be mapped to one of any of n blocks of EMS memory based on the content of the EMS Memory Map (if D/SRAM- is high, n = 128 for 256K memory type, n = 512 for 1M memory type; if D/SRAM- is low, n = 60). During the memory access, the LA(14-19) is used to select the content of the Current and Alternate Map. Cartridge ROM is supported through the EMS mapping scheme. When EMS is disabled and CROM is enabled, CROMCS0- would be generated to select the cartridge ROM. The EMS mapper would also output the corresponding high order ROM address for the cartridge ROM.

3.1.3 Memory Request Control

Memory Request Control generates the internal RAS- timing control signal. Every memory cycle at system or EMS memory will follow this as a basic timing. There are 3 sources of timing to determine the RAS cycle:

During the CPU memory access, RAS- starts in the middle or at the end of TS and ends at the end of TC. CAS- signals are generated 1 to 1 1/2 clocks after RAS- if it is a memory read cycle, and 2 system clocks after RAS- if it is a memory write cycle.

During the DMA transfer, RAS- follows the memory read or memory write commands (MRD- or MWR-) that are synchronized to the system clock. CAS- signals are generated 2/3 clocks after RAS- if it is a memory read cycle, and 1 system clock after RAS- if it is a memory write cycle.

During memory refresh cycle, RAS- will follow the MRD- command. No CAS- signals are generated.

CAS signals are generated based on which byte is enabled and not during a memory refresh cycle.

3.1.4 Memory Parity Check and Generator

Parity is checked and generated by OTI-051 at an individual byte (odd byte or even byte) during memory read and write respectively.

3.1.5 Memory Address Generator

For DRAM control, the memory address generator takes the system memory address, EDR content of EMS MAP and LA address to generate the 20 bit address for memory. During the memory cycle, the lower order addresses A(0-9) are outputted through MA(1-10). At 1/2 to 1 clock after the RAS-, the higher order addresses A(9 or 19, 10- 18) start to drive the MA(1-10). During the memory refresh, the MA(1-10) is driven from LA(0-9). During the column address time, MA(1) carries address A9 if 256K type DRAMs are used, and carries

address A19 if 1M type DRAMs are used. During Cartridge ROM access cycles, address A14 - A22 would be coming out through MA 1 - 9 to access the cartridge ROM.

3.2 DMA CONTROL

DMA Control consists of 3 blocks:
- 2 82C37 DMA Controllers
- DMA Page Registers
- DMA Ready Generator

3.2.1 8237 DMA Controller

The embedded 82C37 DMA Controllers together provide a 7 channel DMA operating at up to 10 MHz synchronized to the system speed. It is used to support 8 and 16-bit transfer operations between memory and peripherals capable of doing the DMA request and transferring data from such devices as a Floppy Controller. Their function is equivalent to the 8237 DMA chip. The DMA channels are assigned as follows:

Channel	Assignment	
Channel0 :	DRQ0	Reserved
Channel1 :	DRQ1	Reserved
Channel2 :	DRQ2	Diskette
Channel3 :	DRQ3	Fixed Disk
Channel4 :	DRQ4	Cascade for Ctrl 1
Channel5 :	DRQ5	Reserved
Channel6 :	DRQ6	Reserved
Channel7 :	DRQ7	Reserved

DMA controller 1 contains channels 0 to 3. It supports 8 bit DMA transfers. Each channel can transfer data throughout the 16MB system address space in 64KB per block at a time. The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller #1
Address	A23<---------------->A16	15<------->A0

Note: The signal, 'byte high enable' (BHE-), is generated by inverting address line A0.

DMA controller 2 contains channels 4 to 7. Channel 4 is used to cascade with DMA controller 1. Channels 5, 6, and 7 support 16-bit data transfers throughout the 16M system address space in 128K blocks. However, data cannot be transferred on odd byte boundaries. The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller #2
Address	A23<---------------->A17	16<------->A1

Note: The signal, 'byte high enable' (BHE-) and A0 are forced to a logical 0.

Seven DMA channels (0,1,2,3,5,6,7) are available on the I/O channel.

The 8237 DMA controller command code addresses follow:

Table 5. DMA Controller Command Code Addresses

I/O Address (in hex)	Register Function
0000	Channel 0 base and current address reg.
0001	Channel 0 base and current word count
0002	Channel 1 base and current address reg.
0003	Channel 1 base and current word count
0004	Channel 2 base and current address reg.
0005	Channel 2 base and current word count
0006	Channel 3 base and current address reg.
0007	Channel 3 base and current word count
0008	Read Status Reg./Write Command Reg.
0009	Write Request Reg.
000A	Write Single Mask Register Bit
000B	Write Mode Reg.
000C	Clear Byte Pointer Flip-Flop
000D	Read Temporary Reg./Write Master Clear
000E	Clear Mask Reg.
000F	Write All Mask Register Bits
00C0	Channel 4 base and current address reg.
00C2	Channel 4 base and current word count
00C4	Channel 5 base and current address reg.
00C6	Channel 5 base and current word count
00C8	Channel 6 base and current address reg.
00CA	Channel 6 base and current word count
00CC	Channel 7 base and current address reg.
00CE	Channel 7 base and current word count
00D0	Read Status Reg./Write Command Reg.
00D2	Write Request Reg.
00D4	Write Single Mask Register Bit
00D6	Write Mode Reg.
00D8	Clear Byte Pointer Flip-Flop
00DA	Read Temporary Reg./Write Master Clear
00DC	Clear Mask Reg.
00DE	Write All Mask Register Bits

3.2.2 DMA Page Register

DMA Page Register can be accessed through the 8 bit I/O ports. These can be read or write ports. The following figure shows the address for the page register.

Page Register	I/O Address (in Hex)
DMA channel 0	0087
DMA channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

Addresses for all DMA channels do not increase or decrease through page boundaries (64KB for channels 0-3, 128KB for channels 5-7).

3.2.3 DMA Ready Generator

DMA Ready Generator controls the length of command time during the DMA cycle. At normal speed, the minimum DMA command cycle (IOCHRDY is not asserted) is 6/4 DMA clocks:

IORD - (MRD-)   6 clocks

MWR-(IOWR-)   4 clocks
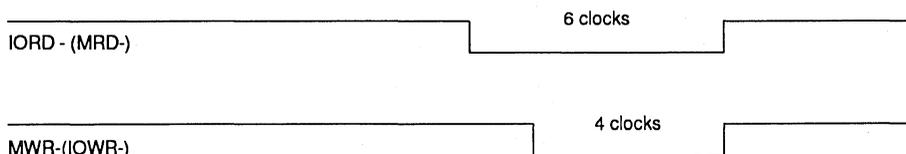
During FAST DMA cycle, the minimum DMA command cycle is 4/2 DMA clocks:

IORD-(MRD-)   4 clocks

MWR-(IOWR-)   2 clocks
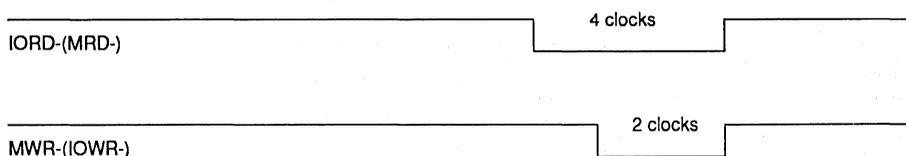
FAST DMA timing can be selected through indexed port 1E(Hex) bit 6.

3.3 Arbiter and Refresh Control

Arbiter and Refresh Control consists of:
- Arbiter
- Memory Refresh Control
- Memory Refresh Address Generator

3.3.1 Arbiter

Arbiter is a synchronous state machine monitoring the DMA requests from the 8237 DMA control unit as well as memory refresh requests. Once the CPU recognizes the request, it will grant the bus through the HLDA line and release control of the bus. At the end of either DMA (until PCRQ- is deasserted) or memory refresh cycle (until MRD- is deasserted), the arbiter checks if there is another request pending. If there is one, it will continue giving the bus to the one that requests it or otherwise release the bus through the HLDA line to the CPU.

3.3.2 Memory Refresh Control Cycle

Memory Refresh Request is generated approximately every 15us from 8254 channel 0 inside OTI-052. REFRQT is fed to the arbiter inside OTI-053. Once the arbiter grants the cycle (MREF- is asserted), it outputs the AEN, ALE, PCALE and MRD- signals. The minimum refresh cycle is 5 system clocks for a system running at 8 MHz.

3.3.3 Memory Refresh Address Generator

Memory Refresh Address Generator drives all 24 address lines through the CPU bus during memory refresh cycle time (MREF- is low). Address 0-9 is outputted from a 10 bit binary counter (which will increment the count at the end of the cycle), and address 10 - 23 is driven low during the memory refresh cycle.

3.4. Miscellaneous

3.4.1 System Ready Generator

System Ready will be active low only at the end of the CPU or co-processor cycle. There are 2 sources that generate the system ready to the CPU to end the cycle:

- Memory Control if the access is in the system or EMS memory range. System ready will be generated by OTI-053 during TC and ended at TS or TI time for a period of 1 system clock.

- Command Generator that generates the cycle besides the system memory. System ready will be generated by OTI-051 at the rising edge of the last TC and ended at the rising edge of TS or TI time for a period of 1 system clock.

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4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 6. A.C. Characteristics of OTI-053

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t1	REFRQT SETUP Time	35		ns	
t2	CPUHRQ from CLK8		40	ns	
t3	CPUHLDA SETUP Time	35		ns	
t4	AEN from CLK8		50	ns	
t5	MREFN from CLK8		50	ns	
t6	Refresh MEMRDN from CLK8		40	ns	
t7	Refresh RASN from CLK8		55	ns	
t8	Refresh Address Valid		60	ns	
t9	DACKN from AEN		5 1/2 TDCY + 70	ns	Note 1
t10	MEMRDN, IORDN from AEN		6 TDCY + 70	ns	Note 1
t11	MEMRDN, IORDN Pulse Width	6 TDCY		ns	Note 1
t12	MEMWRN, IOWRN from IORDN, MEMRDN	2 TDCY		ns	Note 1
t13	MEMWRN, IOWRN Pulse Width	4 TDCY		ns	Note 1
t14	AEN from End of DMA Command		2 TDCY + 50	ns	Note 1
t15	DACKN from End of DMA Command		1/2 TDCY + 70	ns	Note 1
t16	WRITE Data SETUP Time	100		ns	
t17	WRITE Data HOLD Time	20		ns	
t18	READ Data from IORDN		100	ns	
t19	READ Data Float from IORDN	5		ns	
t20	CROMCSN from CPUCLK		40	ns	
t21	RASN from CPUCLK(Mode 1&2)		27	ns	
t22	CAS from CPUCLK(Mode 1&2)		35	ns	
t23	MDIR High from CPU STATUS		25	ns	
t24	MDIR High from Address		50	ns	

Table 6. AC Characteristics of OTI-053 (Continued)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t25	MDIR Low from CPUCLK		40	ns	
t26	SRDYN Low from CPUCLK (Mode 1&2)		25	ns	
t27	SRDYN High from CPUCLK		35	ns	
t28	ROW Address from SA		50	ns	
t29	COLUMN Address from CPUCLK		35	ns	
t30	CAS to MA Hold Time	TCLK-10		ns	Note 2
t31	RASN from CPUCLK (Mode 3)		25	ns	
t32	CAS from CPUCLK (Mode 3)		35	ns	
t33	SRDYN Low from CPUCLK (Mode 3)		30	ns	
t34	SRCSN from CPUCLK		25	ns	
t35	SREN from CPUCLK		25	ns	
t36	MRASN from CPUCLK		25	ns	
t37	SWEHN, SWELN from CPUCLK		25	ns	
t38	Static RAM Address from SA		50	ns	

4.2 D.C. Characteristics of OTI-053

Table 7. D.C. Characteristics of OTI-053

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 μA
VOL1	Output LOW Voltage		0.45	V	IOL=20 mA, Note 3
VOL2	Output LOW Voltage		0.45	V	IOL=16 mA, Note 3
VOL3	Output LOW Voltage		0.45	V	IOL=12 mA, Note 3
VOL4	Output LOW Voltage		0.45	V	IOL= 8 mA, Note 3
VOL5	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 3
VOL6	Output LOW Voltage		0.45	V	IOL= 2 mA, Note 3
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmit Input HIGH	2.4	VDD+0.5	V	Schmitt, Note 4
VIC	CMOS Input HIGH Voltage	3.8'	VDD+0.5	V	CMOS, Note 4
ILI	Input Leakage Current	- 10	10	μA	
OLI	Output Leakage Current	- 10	10	μA	
ICC	Operating Supply Current		100	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

Notes:

1. TDCY is the internal DMA clock. Minimum period is 80ns.

2. TCLK is CPUCLK period.

3. Output Current (IOL) Capabilities:

20 mA :	MREFN, TC, AEN, DACK7-0
12 mA :	MA1-10
8 mA :	RASN0-7, CASHN0-3, CASLN0-3, SRDYN
4 mA :	MDIR, CROMCSN, A0, SA1-19, A20, SA21-23, MEMRDN, MEMWRN, IORDN, IOWRN
2 mA :	COMRQN, CPUHRQ

4. Input Structures:

Schmitt triggered:

CMOS :	CPUCLK, A20
TTL :	all others

Input with pullup:

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5.0 OTI-053 TIMING DIAGRAMS

FIGURE 3-1&2.

MEMORY REFRESH TIMING
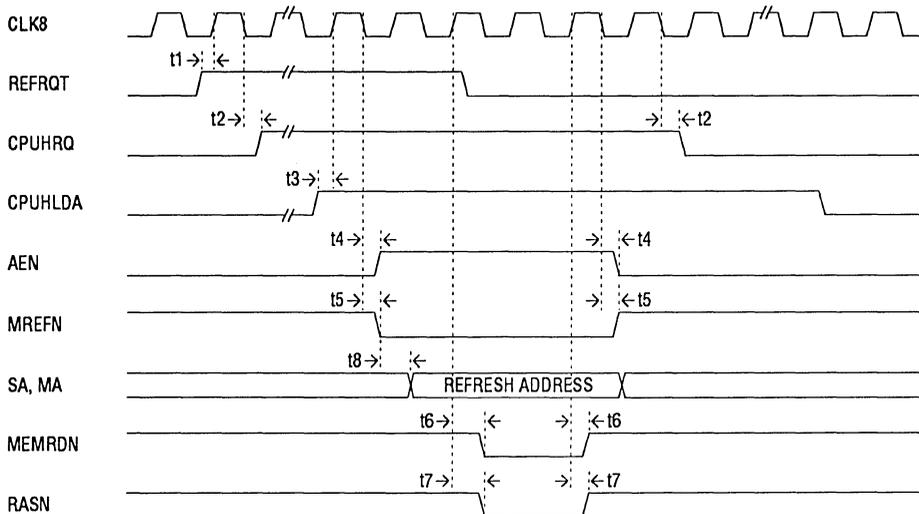
DMA TIMING
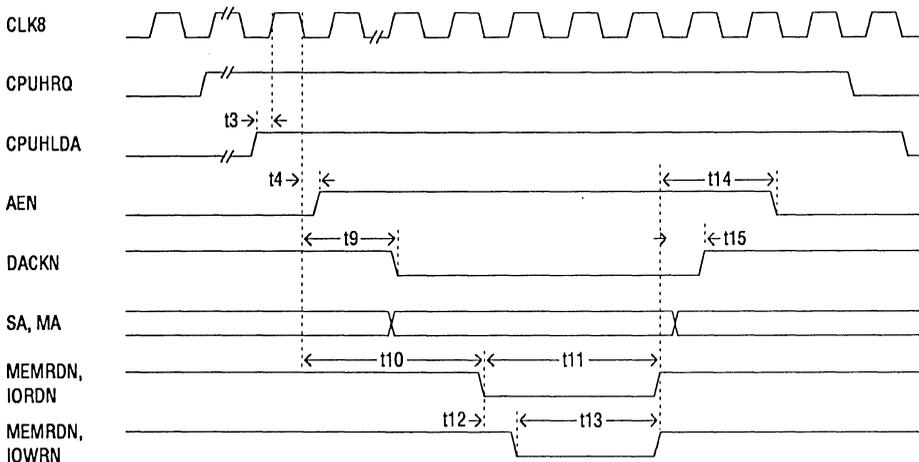
FIGURE 3-4&5.

SYSTEM MEMORY TIMING MODE 1
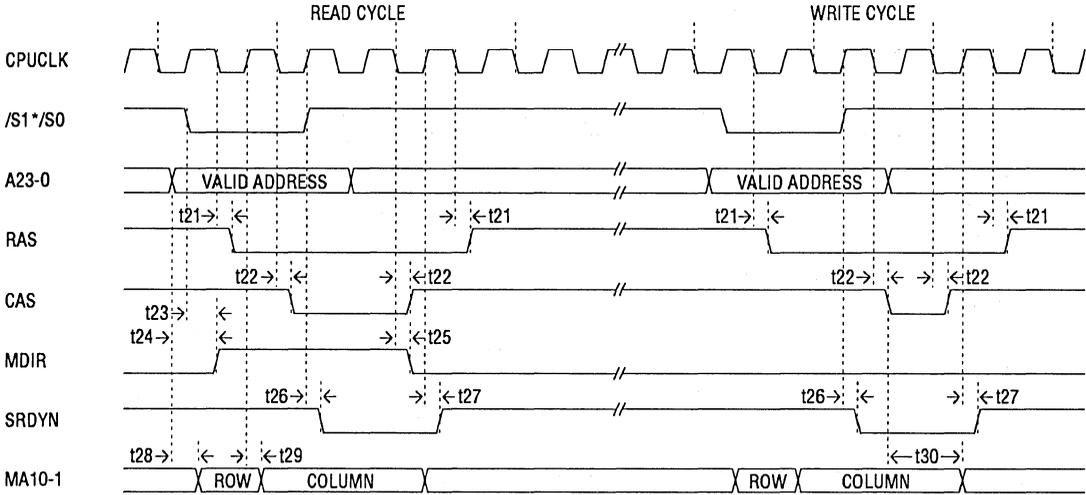
SYSTEM MEMORY TIMING MODE 2
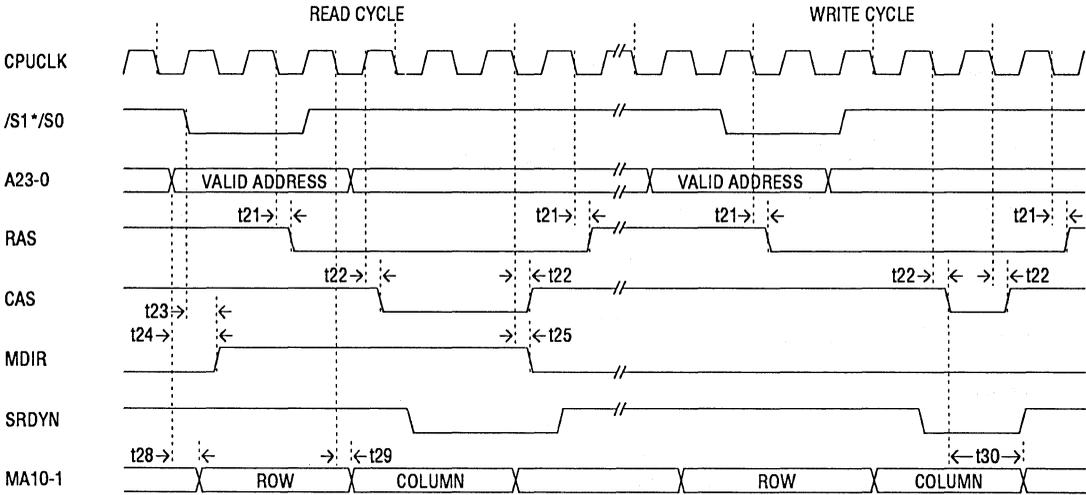
FIGURE 3-6&7.

SYSTEM MEMORY TIMING MODE 3
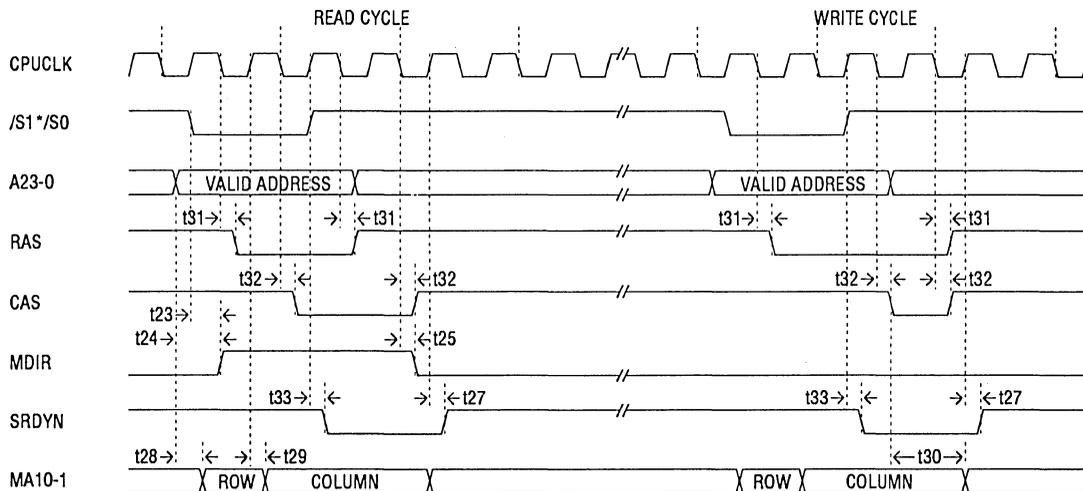
SYSTEM MEMORY TIMING MODE 4
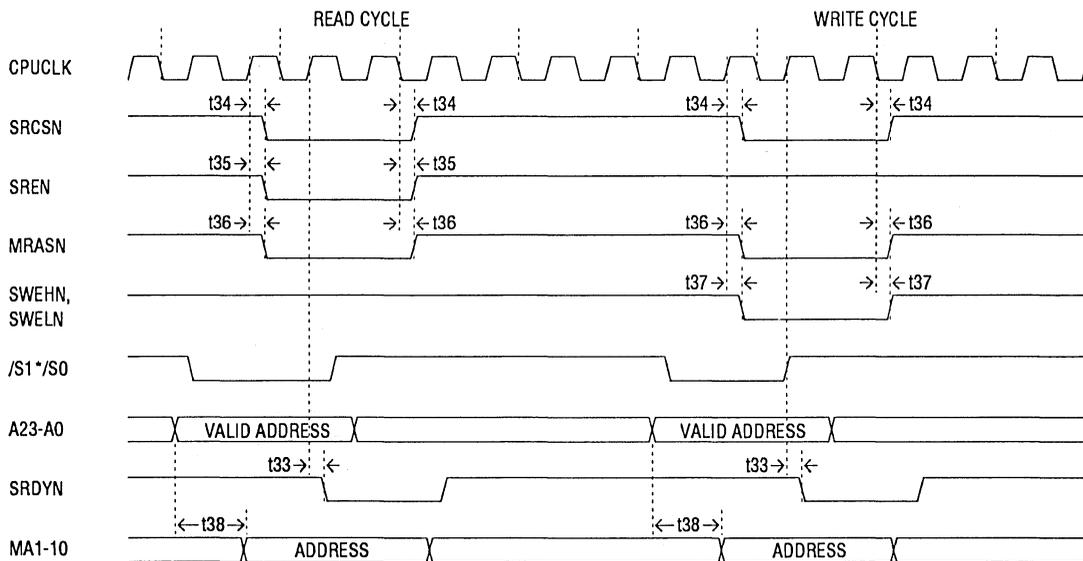
FIGURE 4-1.

AT-BUS ADDRESS TIMING

AT-BUS COMMAND TIMING

MASTER MODE TIMING

SECTION 4
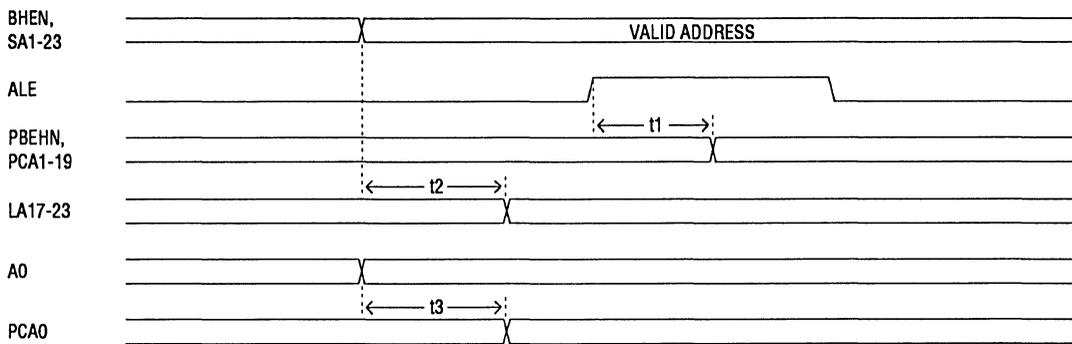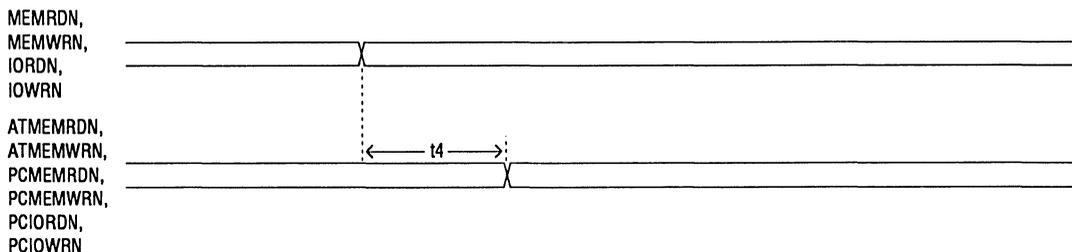
OTI-054

ADDRESS BUFFER & REAL TIME CLOCK
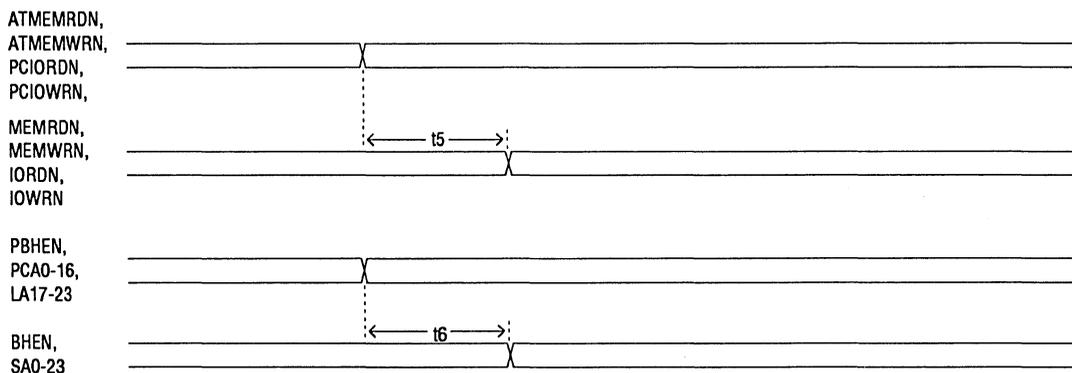
1.0 INTRODUCTION TO OTI-054 ADDRESS BUFFER and REAL TIME CLOCK

OTI-054 contains the address buffer drivers for IBM AT or Model 30 - 286 compatible systems and replaces all the TTL address and command drivers that are normally required on the system board. In addition to the Address drivers, OTI-054 also includes a Real Time Clock. The Real Time Clock is compatible to MC146818 with the following exceptions:

- 128 Bytes of CMOS RAM total
- no CKFS (clock select input)
- no SQW (square wave output)

System Block Diagram

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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-054 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
SA1-SA19 SA21-SA23	3-6,8-14,18-21, 23-26,28-30	I/O	ADDRESS LINE (1-19,21-23): are the CPU address lines (unlatched).
A0	2	I/O	ADDRESS LINE 0: address line 0 from OTI-051.
A20	27	I/O	ADDRESS LINE 20: address line 20 from OTI-051 gated by 8042 output and port 92(Hex) output.
BHE-	1	I/O	BYTE HIGH ENABLE: is an active low signal from OTI-051 and is used to enable data onto the most significant half of the data bus.
PCBHE-	100	I/O	I/O CHANNEL BYTE HIGH ENABLE: is an active low signal on the I/O channel. It is a latched version of BHE-. When MASTER- is low, it becomes an input to form BHE-.
ALE	16	I	ADDRESS LATCH ENABLE: is an active high pulse signal during the beginning of either the CPU or DMA cycle. A(1-23) will be latched internally using the ALE falling edge.
PCA(0-16)	99,98,96-92,90, 88,86-84,82-78	I/O	PC BUS ADDRESS (0-16): are the latched address version of SA(0-16). When ALE is high, PCA(0-16) are the transparent signals of A0 and SA(1- 16). PCA(0-16) are latched at the falling edge of ALE and stay latched until ALE is high again.
PCA(17-19)	77-75	O	PC BUS ADDRESS (17-19): are the latched address version of SA(17- 19). When ALE is high, PCA(17-19) are the transparent signals of (17-19). PCA(17-19) are latched at the falling edge of ALE and stay latched until ALE is high again.
LA(17-23)	38-36,34-31	I/O	UNLATCHED ADDRESS (17-23): are the unlatched address version of SA(17- 23) in the synchronous mode when BUSCLK = CPUCLK/2. When BUSCLK = CPUCLK/4 or when the asynchronous mode is selected, LA17-23 are latched at the falling edge of ALE.
XD7 - XD0	60,59,57-52	I/O	XDATA BUS: bi-directional data lines to/from the CPU or I/O channel bus.
IORD-	73	I/O	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus.
IOWR-	72	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus.
MEMRD-	71	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus.
MEMWR-	70	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus.

Table 1. OTI-054 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION

CMDEN-	69	I	COMMAND ENABLE: is an active low control signal to enable or disable the command buffer going to the I/O channel bus (PC bus). It is used to prevent bus contention between I/O devices that share the same address space resided in the X bus and in the I/O channel bus. CMDEN- is active low if:
			1. Non DMA, all I/O cycles except:
			   1.1 Floppy I/O if an on-board floppy is enabled.
			   1.2 Hard Disk I/O if an on-board hard disk Controller is enabled.
			   1.3 Serial Com #1 if an on-board serial com. is enabled.
			   1.4 Parallel I/O if an on-board parallel port is enabled.
			   1.5 Video I/O if an on-board video is enabled.
			   1.6 Co-processor I/O.
			2. During DMA cycle.
			3. During memory refresh cycle.
			4. Non DMA, PC memory cycle except:
			   4.1 On-board video is enabled and an on-board Video BIOS ROM has been specified through port 1A(Hex)bit 4 to 7.
			   4.2 On-board video is enabled and an on-board Video Memory has been specified through port 1B(Hex)bit 0 to 5.

PCIORD-	68	I/O	I/O READ COMMAND: active low command to instruct the I/O device on the I/O channel to drive its data onto the data bus.
PCIOWR-	66	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device on the I/O channel to read the data present on the data bus.
PCMEMRD-	64	O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem on the I/O channel to drive its data onto the data bus. The current cycle is within the 1M address space.
PCMEMWR-	63	O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem on the I/O channel to store the data present on the data bus. The current cycle is within the 1M address space.
ATMEMRD-	62	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus.
ATMEMWR-	61	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus.
AEN	44	I	ADDRESS ENABLE: is an active high signal during the DMA cycle to degate the I/O devices from the I/O channel to allow DMA transfers to take place.
MASTER-	74	I	MASTER: this signal is used together with a DRQ line to gain control of the system.
PWRGOOD	43	I	POWER GOOD: PWRGOOD comes from a power supply to indicate that power is stable. The signal is inactive if an under voltage condition occurs. The PWRGOOD signal has a turn on delay that is in between 100ms and 500ms. The OTI-051 provides a Schmitt trigger input for POWERGOOD.
PGIOCS0-	42	O	PROGRAMMABLE I/O CHIP SELECT 0: is an active low I/O chip select signal with a programmable I/O address space.
PGIOCS1-	40	O	PROGRAMMABLE I/O CHIP SELECT 1: is an active low I/O chip select signal with a programmable I/O address space.
PGIOCS2-	39	O	PROGRAMMABLE I/O CHIP SELECT 2: is an active low I/O chip select signal with a programmable I/O address space.

Table 1. OTI-054 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION (Continued)
			*** REAL TIME CLOCK ***
XTAL1	46	I	XTAL INPUT FOR RTC: is the crystal input for the real time clock.
XTAL2	47	O	XTAL OUTPUT FOR RTC: is the crystal output for the real time clock.
MINCLK	48	O	MINUTE CLOCK: output signal from the minute count inside the Real Time Clock.
IRQRTC	50	O	INTERRUPT REQUEST FOR RTC: is an output from the real time clock requesting interrupt.
VDDRTC	49	I	POWER FOR RTC: battery power for the Real Time Clock.
			*** MISCELLANEOUS ***
MAXD-	51	O	ENABLE MA TO/FROM PCD: this is an active low signal used to enable the transceiver between MA1-8 and PCD0-7. This allows OTI-053 to be accessed through the PC-DATA bus.
VDD	17,41,65,87,91	I	5 V. SUPPLY: 5 pins
VSS	7,15,22,35,45, 58,67,83,89,97	I	GROUND: 10 pins.

NOTE: OTI-054 would enter into TEST mode under the following conditions:

MASTER-: '0'
PCIORD-: '0'
PCIOWR-: '0'

Pin	Signal		Signal	Pin
1	BHE-		PCA14	80
2	A0		PCA15	79
3	SA1	Index	PCA16	78
4	SA2		PCA17	77
5	SA3		PCA18	76
6	SA4		PCA19	75
7	VSS		MASTER-	74
8	SA5		IORD-	73
9	SA6		IOWR-	72
10	SA7		MEMRD-	71
11	SA8		MEMRW-	70
12	SA9		CMDEN-	69
13	SA10		PCIORD-	68
14	SA11		VSS	67
15	VSS		PCIOWR-	66
16	ALE		VDD	65
17	VDD		PCMEMRD-	64
18	SA12		PCMEMWR-	63
19	SA13		ATMEMRD-	62
20	SA14		ATMEWR-	61
21	SA15		XD7	60
22	VSS		XD6	59
23	SA16		VSS	58
24	SA17		XD5	57
25	SA18		XD4	56
26	SA19		XD3	55
27	A20		XD2	54
28	SA21		XD1	53
29	SA22		XD0	52
30	SA23		MAXD-	51

Top pins (100–81):

100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81
PCBHE	PCA0	PCA1	VSS	PCA2	PCA3	PCA4	PCA5	PCA6	VDD	PCA7	VSS	PCA8	VDD	PCA9	PCA10	PCA11	VSS	PCA12	PCA13

Bottom pins (31–50):

31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
LA23	LA22	LA21	LA20	VSS	LA19	LA18	LA17	PGIO CS2-	PGI OCS1-	VDD	PGIO CS0-	PWR GOOD	AEN	VSS	XTAL1	XTAL2	MIN CLK	VDD RTC	IRQ RTC

3.0 OTI-054 FUNCTIONAL DESCRIPTION

OTI-054 functions can be categorized as follows:

1. Address and Command Buffers

2. Real Time Clock

3. Programmable I/O Chip Selects

3.1 Address and Command Buffers

OTI-054 integrates all the address and command buffers that are specified in the AT bus. The propagation delay for all the buffers is 25ns. The output current on the AT bus side is 20 mA at a capacitive loading of 200 pF. On the CPU side, the capacitive loading is designed for 80 pF.

3.2 Real Time Clock

The Real Time Clock is compatible to MC146818 with the following exceptions:
- 128 Bytes of CMOS RAM total
- no CKFS (clock select input)
- no SQW (square wave output).

For a detailed description of the Real Time Clock, refer to the specification of MC146818.

Power to the Real Time Clock can be backed up by a 3V battery. When system power is down, battery power is routed to the Real Time Clock only, so that the Real Time Clock can still continue to run. Battery power is conserved, since it does not go to the other circuitry on the chip. The Real Time Clock has an extra output coming from the MINUTE counter. This signal is used by the power management circuitry as the MINUTE CLOCK in the other chips of the chipset. A total of 128 Bytes of CMOS RAM are implemented in the Real Time Clock. The extra 64 bytes can be accessed the same way as through the index register. The index range is 0 - 7F.

RT/CMOS and NMI Mask   I/O Port   0070(Hex) W:
Bit   **Function**
7   Non-maskable Interrupt (NMI)
                         0 - NMI enabled
                         1 - NMI disabled
6-0   RTC/CMOS RAM
         address register to access the CMOS RAM

CMOS RAM Data Register   I/O Port   0071(Hex) R/W:

To access the CMOS RAM, first write the index to port 70(Hex), then perform READ/WRITE to port 71.

4.3 Programmable I/O Chip Select

OTI-054 provides three programmable I/O chip select output pins. The I/O addresses for the 3 I/O chip selects can be programmed 8 bits at a time. Three indexed ports are provided for each I/O address to accomodate the 24-bit I/O address.

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4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 2. A.C. Characteristics of OTI-054

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t1	ALE to PC Address Valid		25	ns	CL=200 pF
t2	SA Address to LA Address		25	ns	CL=100 pF
t3	PCA0 from A0 Delay		25	ns	CL=200 pF
t4	AT-BUS Command Delay		25	ns	CL=200 pF
t5	Master Mode Command Delay		25	ns	CL=80 pF
t6	Master Mode Address Delay		25	ns	CL=100 pF
t7	Address Valid Before ALE	40		ns	
t8	ALE Before IOWRN	35		ns	
t9	WRITE Data SETUP Time	100		ns	
t10	WRITE Data HOLD Time	20		ns	
t11	READ Data Valid from IORDN		100	ns	
t12	READ Data Float from IORDN	5		ns	
t13	Chip Selects from ALE		40	ns	

4.2 DC Characteristics

Table 3. DC Characteristics of OTI-054

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 µA
VOL1	Output LOW Voltage		0.45	V	IOL=20 mA, Note 1
VOL2	Output LOW Voltage		0.45	V	IOL=16 mA, Note 1
VOL3	Output LOW Voltage		0.45	V	IOL=12 mA, Note 1
VOL4	Output LOW Voltage		0.45	V	IOL=10 mA, Note 1
VOL5	Output LOW Voltage		0.45	V	IOL= 8 mA, Note 1
VOL6	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 1
VOL7	Output LOW Voltage		0.45	V	IOL= 2 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmitt Input HIGH	2.4	VDD+0.5	V	Schmitt, Note 2
VIC	CMOS Input HIGH Voltage	3.8	VDD+0.5	V	CMOS, Note 2
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		20	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

1. Output Current (IOL) Capabilities:

    20 mA :   ATMEMWRN,ATMEMRDN,PCMEMWRN,PCMEMRDN, PCIOWRN,PCIORDN,IOWRN,IORDN,PCA0-19

    12 mA :   LA17-23

    10 mA :   BHEN,SA0-23,PGIOCSN,MINCLK,IRQRTC,MAXDN,XD0-7,PBHEN

    8 mA :   -

    4 mA :   -

    2 mA :   -

2. Input Structures:

    Schmitt triggered: -

    CMOS :   -

    TTL :   All Others

    Input with Pullup: -

5.0 OTI-054 TIMING DIAGRAMS

FIGURE 4-1.

AT-BUS ADDRESS TIMING
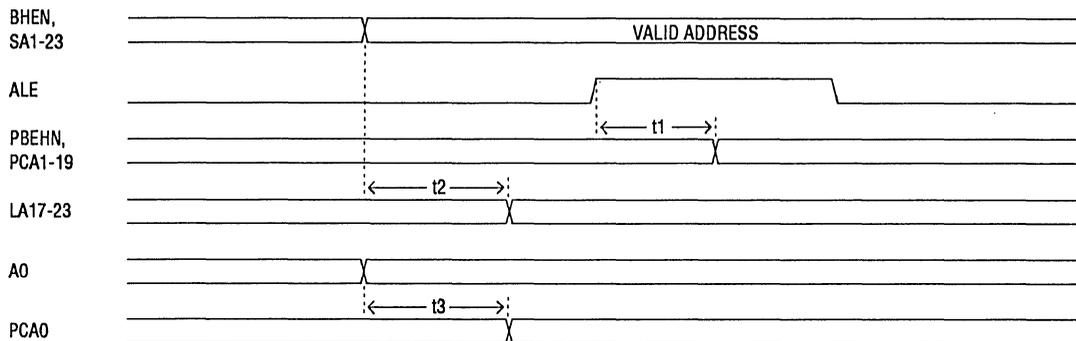
AT-BUS COMMAND TIMING
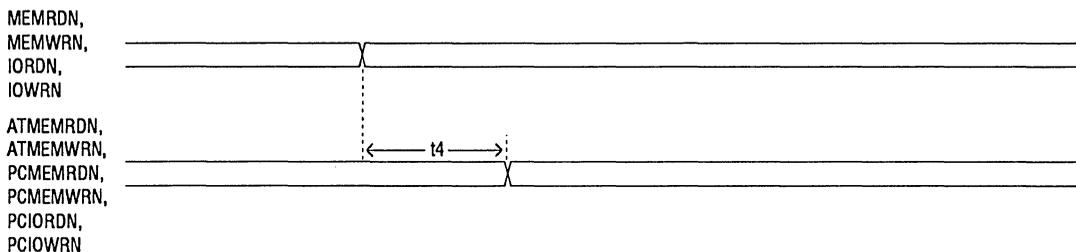
MASTER MODE TIMING
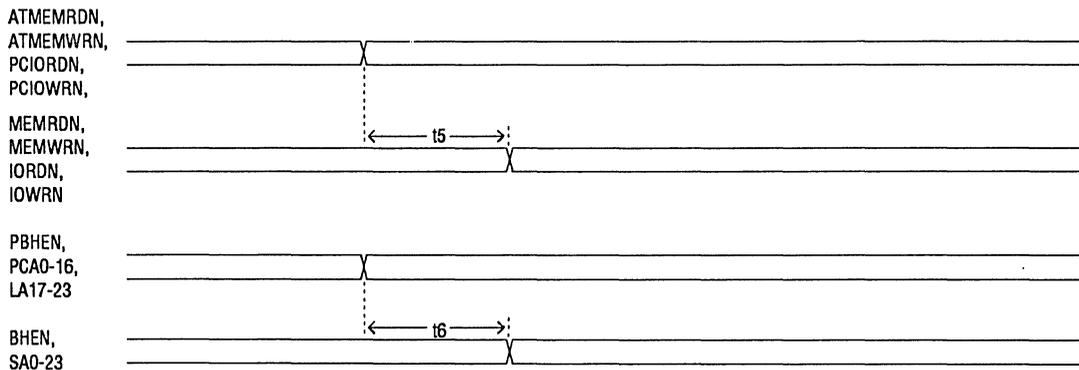
FIGURE 4-2.

I/O CYCLE TIMING

CHIP SELECT TIMING

SECTION 5
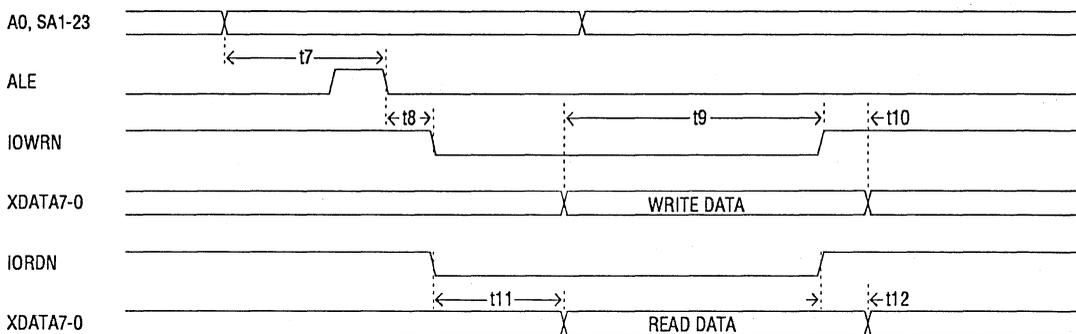
OTI-055

DATA BUFFER & POWER MANAGER
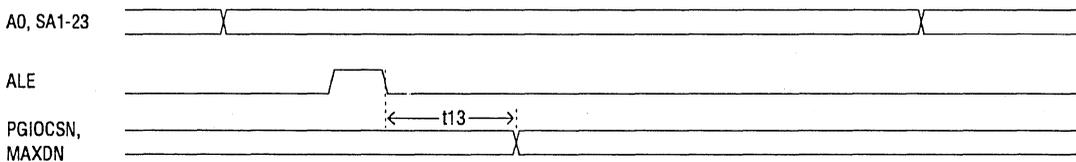
1.0 INTRODUCTION TO OTI-055 DATA BUFFER and POWER MANAGER

OTI-055 contains the data buffers for IBM AT or Model 30 - 286 compatible systems and replaces all the TTL data drivers that are normally required on the system board.

In addition to the data buffers on the chip, the OTI-055 also serves as a power manager in battery-powered systems. The OTI-055 has 16 general purpose bidirectional control/status lines available to the system manufacturer to control power distribution to various peripherals in the system. Besides the 16 signals, OTI-055 also has an internal timer/counter that allows the user to automatically turn on power to the whole system.

System Block Diagram
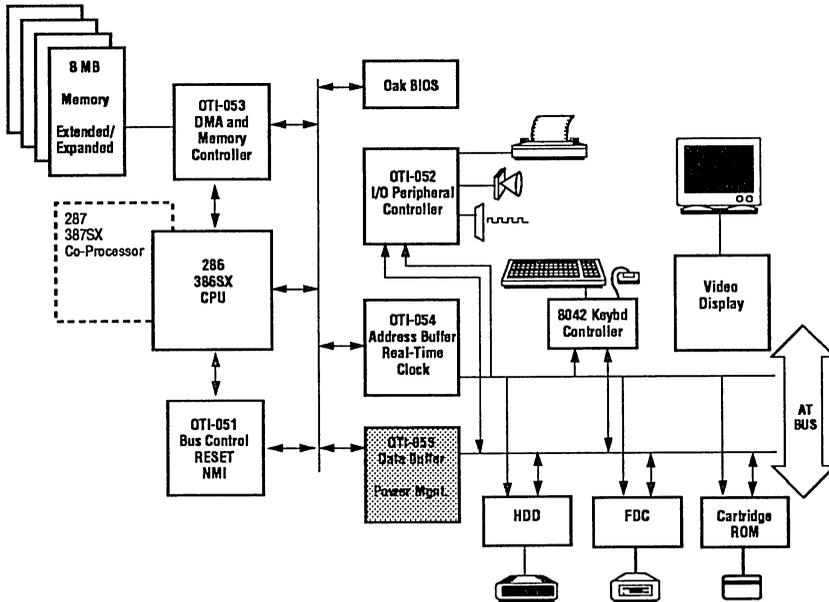
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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-055 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
PWCS-	15	I	POWER MANAGEMENT CHIP SELECT: is an active low input used to select the internal registers of the chip.
A0	14	I	ADDRESS LINE 0: is the latched version of address 0. A0 together with PWCS- is used to program the power management chip OTI-055. When A0 is 0, the index register is accessed; when A0 is 1, the data register is accessed.
PCD(0-15)	60-62,64-66,68,69, 71,72,74-76,78-80	I/O	PC DATA BUS (0-15): is the PC data bus. There are 2 sets of data transceivers that are connected internally i.e. between SD(0-7) and PCD(0-7) and between SD(8-15) and PCD(8-15) to form a 16 bit PC data bus: PCD(0-15).
SD(0-15)	81-84,86,87,89,90, 92,94-96,98-100,1	I/O	SYSTEM DATA BUS (0-15): is the system data bus. There are 2 sets of data transceivers that are connected internally i.e. between SD(0-7) and PCD(0-7) and between SD(8- 15) and PCD(8-15) to form a 16 bit PC data bus: PCD(0-15).
MA8 - MA1	55-49,47	I/O	MEMORY ADDRESS BUS: bi-directional lines between the memory address lines and I/O chanell bus. OTI-053 multiplexes the MA lines with the PC data bus.
MAXD-	46	I	MA TO DATA BUS CONTROL: active low signal from OTI-054 enabling the data path between the MA lines and PC data bus.
SEL0	36	I	SELECT 0: is an active high signal from OTI-051 indicating an I/O cycle with address A15-A10 all zeroes.
DENL-	3	I	DATA LOW ENABLE: is an active low control signal to enable/disable the internal data transceiver between SD(0-7) and PCD(0-7).
DENH-	4	I	DATA HIGH ENABLE: is an active low control signal to enable/disable the internal data transceiver between SD(8-15) and PCD(8-15).
PCDIR	2	I	PC DATA DIRECTION: is the direction control signal for the data transceivers between PCD(0-15) and SD(0-15): PCDIR = 0 ==>SD follows PCD bus. =1 ==>PCD follows SD bus.
ENSWAP	5	I	ENABLE DATA SWAP: is an input signal used for enabling the data buffer for data swap.
IORD-	12	I	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus.
IOWR-	13	I	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus.
RESET	10	I	RESET: is an active high signal synchronized to the system clock to reset the system.
NMIOUT	6	O	NMI: active high output to the CPU for non-maskable interrupt.
NMIIN0	8	I	NMI input 0: active high input ORed internally with other NMI generating sources to generate NMIOUT to the CPU.
NMIIN1	7	I	NMI input 1: active high input ORed internally with other NMI generating sources to generate NMIOUT to the CPU.

Table 1. OTI-055 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
D/SRAM-	34	I	DRAM OR SRAM SELECT: is an input signal to tell the chip the memory type used in the system: D/SRAM- =low ==>pseudo-static RAM D/SRAM- =high==>Dynamic RAM
TEST-	35	I	INTERNAL TEST: active low input signal to invoke the internal test circuitry.

*** POWER MANAGEMENT***

SYMBOL	PIN #	TYPE	NAME and FUNCTION
MINCLK	58	I	MINUTE CLOCK: input signal from the minute count from the Real Time Clock inside OTI-054.
RING-	9	I	RING SIGNAL: active low input indicating that there is ring signal detected from the modem.
POWERGOOD	38	I	POWER GOOD SIGNAL: active high signal indicating the system power is in the desired range +/- 5%.
BATT0-	45	I	BATTERY LEVEL 0: active low signal to indicate that battery low level 0 is reached. NMI might be generated to invoke the power saving routine.
BATT1-	44	I	BATTERY LEVEL 1: active low signal to indicate that battery low level 1 is reached. NMI might be generated to invoke the power saving routine.
BATT2-	43	I	BATTERY LEVEL 2: active low signal to indicate that battery level is getting low, and it should be recharged. This is just a warning signal.
SYSPWR	42	O	SYSTEM POWER: active high output controlling the regulator to turn on the system power.
MODPWR	40	O	MODEM POWER: active high output controlling the regulator to turn on the power to the modem.
PWOFF0	17	I/O	POWER OFF CONTROL 0: e.g. HARD DISK POWER CONTROL: active low signal to turn off power to hard disk. Output current is 4 mA.
PWOFF1	18	I/O	POWER OFF CONTROL 1: e.g. FLOPPY DISK POWER CONTROL: active low signal to turn off power to the floppy disk controller. Output current is 4 mA.
PWOFF2	19	I/O	POWER OFF CONTROL 2: e.g. DISPLAY POWER CONTROL: active low signal to turn off the display. Output current is 4 mA.
PWOFF3	20	I/O	POWER OFF CONTROL 3: e.g. DISPLAY POWER CONTROL: active low signal to turn off display. Output current is 4 mA.
PWOFF4	21	I/O	POWER OFF CONTROL 4: e.g. TRANSCEIVER POWER CONTROL: active low signal to turn off power to the RS-232 transceivers. Output current is 4 mA.
PWOFF5	22	I/O	POWER OFF CONTROL 5: e.g. CO-PROCESSOR POWER CONTROL: active low signal to turn off the math co-processor. Output current is 4 mA.
PWOFF6	23	I/O	POWER OFF CONTROL 6: general purpose control signal, also programmable to be a status input. Output current is 4 mA.
PWOFF7	24	I/O	POWER OFF CONTROL 7: general purpose control signal, also programmable to be a status input. Output current is 4 mA.
PWOFF8-11	25,26,28,29	I/O	POWER OFF CONTROL 8 - 11: general purpose control signals, also programmable to be status inputs. Output current drive is 4 mA.

Table 1. OTI-055 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
PWOFF12-15	30-33	I/O	POWER OFF CONTROL 12 - 15: general purpose control signals, also programmable to be status inputs. The output drive for these 4 pins are 8 mA each.
NC	37,57		NO CONNECT: 2 pins
VSS	16,27,41,48,56,63, 67,73,77,85,93,97	I	GROUND: 12 pins 0V
VDD	11,39,59,70,88,91	I	POWER: 6 pins 5V

Top pins (100–81):

SD14, SD13, SD12, VSS, SD11, SD10, SD9, VSS, SD8, VDD, SD7, SD6, VDD, SD5, SD4, VSS, SD3, SD2, SD1, SD0

Left side (1–30):

Pin	Signal
100	SD15
1	PCDIR
2	DENL-
3	DENH-
4	ENSWAP
5	NMIOUT
6	NMIIN1
7	NMIIN0
8	RING-
9	RESET
10	VDD
11	IORD-
12	IOWR-
13	A0
14	PWCS-
15	VSS
16	PWOFF0
17	PWOFF1
18	PWOFF2
19	PWOFF3
20	PWOFF4
21	PWOFF5
22	PWOFF6
23	PWOFF7
24	PWOFF8
25	PWOFF9
26	VSS
27	PWOFF10
28	PWOFF11
29	PWOFF12
30	

— Index

Right side (80–51):

Pin	Signal
80	PCD15
79	PCD14
78	PCD13
77	VSS
76	PCD12
75	PCD11
74	PCD10
73	VSS
72	PCD9
71	PCD8
70	VDD
69	PCD7
68	PCD6
67	VSS
66	PCD5
65	PCD4
64	PCD3
63	VSS
62	PCD2
61	PCD1
60	PCD0
59	VDD
58	MINCLK
57	NC
56	VSS
55	MA8
54	MA7
53	MA6
52	MA5
51	MA4

Bottom pins (31–50):

PW OFF13, PW OFF14, PW OFF15, D/S RAM-, TEST-, SELO, NC, POWER GOOD, VDD, MOD PWR, VSS, SYS PWR, BATT2-, BATT1-, BATT0-, MAXD-, MA1, VSS, MA2, MA3

3.0 OTI-055 FUNCTIONAL DESCRIPTION

OTI-055 functions can be categorized as follows:

1.   Data Buffers

2.   NMI Logic

3.   Power Manager

3.1 Data Buffers

OTI-055 integrates all the data buffers necessary for the PC data bus, the CPU data bus and the X-Bus. It also contains the logic for byte swap. All data buffers have a propagation delay of 25ns. The PC data bus loading is designed for 200 pF and 20 mA IOL. The capacitive loading on the system bus is 100 pF.

3.2 NMI Logic

Two external NMI inputs are provided so that the NMI output from OTI-051 can be gated together with another external NMI input to generate an NMI signal to the CPU. Internal NMI logic also allows other internal circuitry to generate NMI to invoke the power management routines. The NMI sources can be programmed through a control port.

3.3 Power Manager

OTI-055 provides system designers with the capability to manage power distribution to the various peripheral devices on the computer system. The key features include automatic power-on, programmable I/O control/status lines and NMI generation logic for invoking software control.

3.3.1 Automatic Power-ON

OTI-055 supports two modes of automatic power on:
- Self-timed Power-On: an internal counter allows the user to program the system to power on automatically in up to 11 days.
- Modem Power-On: internal circuitry to detect the RING signal coming from the modem to turn on the system automatically if the RING count exceeds the value programmed by the user.

3.3.2 Programmable Control/Status Lines

OTI-055 provides 16 programmable bidirectional control/status lines for the system designers. Each of the lines can be programmed to be an input or an output. Four of the outputs have 8 mA IOL current drive, while all the others have an output current drive of 4 mA. These programmable I/O lines allow the system designer to power ON or power OFF different devices on the system as well as monitor the status of the system. Three of the status inputs can be programmed to generate NMI.

Below are the control registers and program definitions for each of the 16 programmable pins:

Pins PWOFF7-0
(program bit 7 for pin PWOFF7,...bit 0 for pin PWOFF0)

Direction Control Register 0
PWRIOL I/O PORT 48(Hex) READ/WRITE

Programmable Value	Definition
0	Input (default)
1	Output

At Power-on Reset, indexed port 48(Hex) reads as 00.

Output Control Register 0
PWROTL I/O PORT Index 49(Hex) READ/WRITE

Programmable Value	Definition
0	output is "0" (default)
1	output is "1"

At Power-on Reset, indexed port 49(Hex) reads as 00.

Input Status Register 0
PWRINL I/O PORT Index 4A(Hex) READ

Programmable Value	Definition
0	input is "0"
1	input is "1"

Pins PWOFF15-8
(program bit 7 for pin PWOFF15,...bit 0 for pin PWOFF8)

Direction Control Register 1
PWRIOH I/O PORT Index 4B(Hex) READ/WRITE

Programmable Value	Definition
0	input (default)
1	output

At Power-on Reset, indexed port 4B(Hex) reads as 00.

Output Control Register 1
PWROTH I/O PORT Index 4C(Hex) READ/WRITE

Programmable Value	Definition
0	output is "0" (default)
1	output is "1"

At Power-on Reset, indexed port 4C(Hex) reads as 00.

Input Status Register 1
PWRINH I/O PORT Index 4D(Hex) READ

Programmable Value	Definition
0	input is "0"
1	input is "1"

4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 2. A.C. Characteristics of OTI-055

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t1	PCD,MA from SD		35	ns	CL=200 pF
t2	SD from PCD, MA		35	ns	CL=100 pF
t3	Address Valid Before IOWRN	40		ns	
t4	SEL0 Valid Before IOWRN	40		ns	
t5	WRITE Data SETUP Time	100		ns	
t6	WRITE Data HOLD Time	20		ns	
t7	READ Data Valid from IORDN		100	ns	
t8	READ Data Float from IORDN	5		ns	
t9	POFFx Delay from IOWRN		50	ns	

4.2 D.C. Characteristics

Table 3. D.C. Characteristics of OTI-055

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 µA
VOL1	Output LOW Voltage		0.45	V	IOL=24 mA, Note 1
VOL2	Output LOW Voltage		0.45	V	IOL=14 mA, Note 1
VOL3	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		30	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

1. Output Current (IOL) Capabilities:

24 mA :	PCD0-15
14 mA :	SD0-15, POFF12-15,MA1-8
4 mA :	NMIOUT, POFF0-11, MODPWR, SYSPWR

5.0 OTI-055 TIMING DIAGRAM

FIGURE 5-1.

DATA BUS TIMING
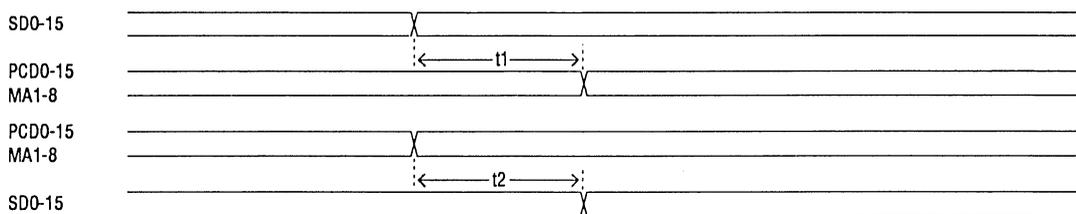
I/O CYCLE TIMING
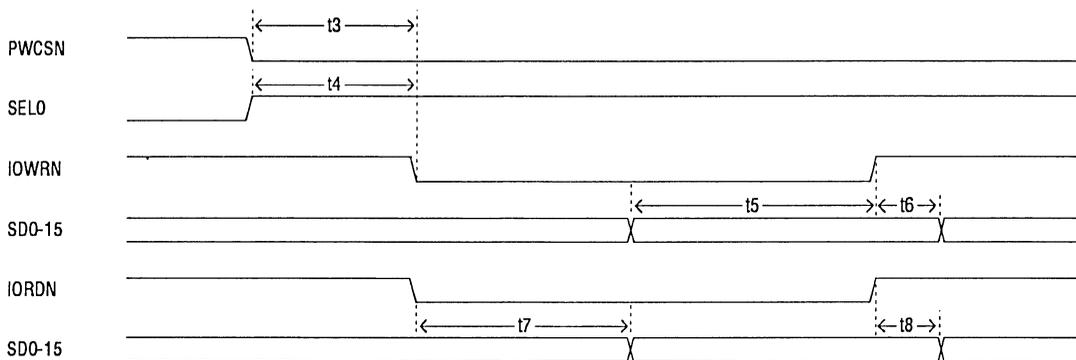
PROGRAMMABLE I/O TIMING

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SECTION 6

APPENDIX
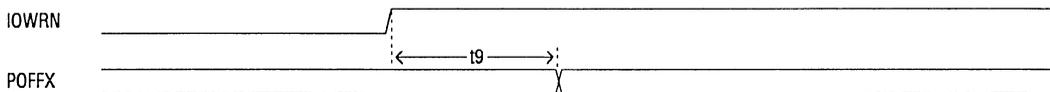
SYSTEM MEMORY MAP

The 80286 and 80386SX support 16 bit operations with 24 bit addressing to directly access up to 16MB of memory space. The system memory and an On-board Expanded/Extended Memory (if it's enabled) are byte and/or word accessible. Memory is mapped as follows:

HEX ADDRESS	DESCRIPTION	
00000 - 1FFFF	128KB : bank #1	
20000 - 2FFFF	64KB : bank #2	
30000 - 3FFFF	64KB : bank #3	
40000 - 4FFFF	64KB : bank #4	640K
50000 - 5FFFF	64KB : bank #5	System
60000 - 6FFFF	64KB : bank #6	Memory
70000 - 7FFFF	64KB : bank #7	
80000 - 8FFFF	64KB : bank #8	
90000 - 9FFFF	64KB : bank #9	
A0000 - BFFFF	128KB : Video Buffer	
C0000 - DFFFF	28KB : Reserved for BIOS on I/O Channel	
E0000 - FFFFF	128KB : System ROM	
100000 - XXXXXX	Extended Memory	
XXXXXX - YYYYYY	EMS Memory	
E00000 - FFFFFF	128KB ROM BIOS Area	

SYSTEM I/O MAP

I/O ADDRESS	FUNCTION	OTI-051 RESPONSE	OTI-052 RESPONSE	OTI-053 RESPONSE	OTI-054 RESPONSE
0000 - 000F	DMA Controller 1	none	none	R/W	
0010 - 0018	EMS Register	none	none	R/W	
001E	OAK Port Addr Ptr	R/W	W	W	
001F	OAK Data Register	R/W	R/W	R/W	
0020 - 003F	Interrupt Cont.1	none	R/W	none	
0040 - 0043	System Timer	none	R/W	none	
0060	System Data Port	none	none	none	
0061 - 006F (odd bytes)	Port B	R/W	W	none	
0070	NMI mask, RTC	W	none	none	W
0071 - 007F	Real-time Clock	none	none	none	R/W
0080 - 008F	DMA Page Register	none	none	R/W	W
0090 - 009F	Reserved	R/W	R/W	none	
00A0 - 00BF	Interrupt Cont.2	none	R/W	none	
00C0 - 00DE	DMA Controller 2	none	none	R/W	
00F0	Clear Copro. Busy	none	W	none	
00F1	Reset Co-proc.	W	W	none	
00F2 - 00F7	Reserved	none	none	none	
00F8 - 00FF	Math Co-processor	none	none	none	
0100 - 0107	Prog Option Select	R/W	R/W	R/W	
02F8 - 02FF	Serial Comm. #2	none	R/W	none	
01F0 - 01F7	Fixed Disk Cont.	none	R/W	none	
0320 - 032F	Fixed Disk Cont.	none	R/W	none	
0278 - 027A	Parallel Port 3	none	R/W	none	
0378 - 037A	Parallel Port 2	none	R/W	none	
03BC - 03BE	Parallel Port 1	none	R/W*	none	
03B0 - 03DF	Video System	W	R/W	none	
03F0 - 03F7	Floppy Disk Cont.	none	R/W*	none	
03F8 - 03FF	Serial Comm. #1	none	R/W*	none	

* The peripheral is built-in inside OTI-052. It can be enabled or disabled through POS Registers.

SPECIAL I/O MAP - OTI-051

INDEX ADDR	ACCESS	FUNCTION NAME
0001	R/W	PCMEWS : PC Memory W.S. Control Register
0002	R/W	PCIOWS : I/O W. S. Control Register
0003	R/W	SPCS : Speed Control Register
0004	R/W	VIDEO0 : Video BIOS and I/O Enable
0005	R/W	VIDEO1 : Video Memory Enable Register
0006 - 0007	R/W	TIMCTR : Count for TIME OUT
0008 - 0009	R/W	TIMADRL : I/O addr low 16 bit at Timeout
000A	R/W	TIMADRH : I/O addr high 8 bit at Timeout
000E	R/W	STAT51 : OTI-051 STATUS Register
000F	R	CHIPID : OTI-051 ID Register
0019	W	SHDRAM : SHADOW RAM CONTROL Register
001A	W	MEMCFG : MEMORY CONFIGURATION Register
001B	W	MEWTST : WAIT STATE CONTROL Register
I/O ADDRESS	**ACCESS**	**FUNCTION NAME**
001E	R/W	OAKADR : OAK PORTS INDEX Register
001F	R/W	OAKDAT : OAK PORTS DATA Register

NOTE: To access any OTI special port, write the index to port 1E(Hex) first, then perform READ/WRITE operation to data port 1F(Hex). After each access to port 1F(Hex), the index value inside port 1E(Hex) is automatically reset to 00(Hex).

SPECIAL I/O MAP - OTI-052

INDEX ADDRESS	ACCESS	FUNCTION NAME
0004	W	VIDEO - Video Interface Control Register
0005	W	VIDEO1 - Video Interface Control Register
00FF	R	CHIPID: OTI-052 ID
00FE	R/W	Floppy Interface Control
00FD	R/W	OTI-052 Control/Status Register
00FC	R/W	Activity Enable Register
00FB	R	Activity Monitor Status Register
00F9	R/W	System Activity Monitor Interrupt Enable
00F8	R/W	System Activity Monitor Timeout Value
00F7	R/W	Hard Disk Activity Monitor Interrupt Enable
00F6	R/W	Hard Disk Activity Monitor Timeout Value
00F5	R/W	Display Activity Monitor Interrupt Enable
00F4	R/W	Display Activity Monitor Timeout Value
00F3	R/W	Address Compare Enable High Byte Register
00F2	R/W	Address Compare Enable Low Byte Register
00F1	R/W	Address Compare Value High Byte Register
00F0	R/W	Address Compare Value Low Byte Register
I/O ADDRESS	**ACCESS**	**FUNCTION NAME**
001E	R/W	OAKADR: OAK PORTS INDEX Register
001F	R/W	OAKDAT: OAK PORTS DATA Register

NOTE: To access any OTI special port, write the index to port 1E(Hex) first, then perform READ/WRITE operation to data port 1F(Hex). After each access to port 1F(Hex), the index value inside port 1E(Hex) is automatically reset to 00(Hex).

SPECIAL I/O MAP - OTI-053

INDEX ADDR	ACCESS	FUNCTION NAME
0003	W	SPCS : Speed Control Register
0010	R/W	RASEN : RAS ENABLE Register
0011	R/W	RASWID : RAS Pulse Width Register
0019	R/W	SHDRAM : Shadow RAM Control Register
001A	R/W	MEMCFG : Memory Configuration Register
001B	R/W	MEWTST : Memory W. S. Control Register
001C	R/W	POFF : Power Off Register
001D	R/W	EXTMEM : Extended memory boundary (64K)
001E	R/W	OAKCTL : OAK System Control/Status Reg.
001F	R	CHIPID : OTI-053 ID Register
I/O ADDRESS	ACCESS	FUNCTION NAME
0010	R/W	EMSEN : EMS Enable Register
0011	R/W	CEAP : Current EMS Address Pointer
0012	R/W	CMAPL : Current EMS MAP - Low Byte
0013	R/W	CMAPH : Current EMS MAP - High Byte
0014	R/W	EMDMAL : Enable Alternate MAP for DMA
0015	R/W	AEAP : Alternate EMS Address Pointer
0016	R/W	AMAPL : Alternate EMS MAP - Low Byte
0017	R/W	AMAPH : Alternate EMS MAP - High Byte
0018	R/W	EMDMAH : Enable Alternate MAP for DMA
001E	R/W	OAKADR : OAK PORTS INDEX Register
001F	R/W	OAKDAT : OAK PORTS DATA Register

NOTE: To access any OTI special port, write the index to port 1E(Hex) first, then perform a READ/WRITE operation to data port 1F(Hex). After each access to port 1F(Hex), the index value inside port 1E(Hex) is automatically reset to 00(Hex).

SPECIAL I/O MAP - OTI-054

INDEX ADDR	ACCESS	FUNCTION NAME
0003	W(0-2,4)	SPCS : Speed Control Register
0030	R/W(0-7)	IOCS0L : I/O Addr 0 Low Byte
0031	R/W(0-7)	IOCS0M : I/O Addr 0 Middle Byte
0032	R/W(0-7)	IOCS0H : I/O Addr 0 High Byte
0033	R/W(0-7)	IOCS1L : I/O Addr 1 Low Byte
0034	R/W(0-7)	IOCS1M : I/O Addr 1 Middle Byte
0035	R/W(0-7)	IOCS1H : I/O Addr 1 High Byte
0036	R/W(0-7)	IOCS2L : I/O Addr 2 Low Byte
0037	R/W(0-7)	IOCS2M : I/O Addr 2 Middle Byte
0038	R/W(0-7)	IOCS2H : I/O Addr 2 High Byte
003F	R (0-7)	CHIPID : OTI-054 ID Register
I/O ADDRESS	**ACCESS**	**FUNCTION NAME**
001E	R/W(0-7)	OAKADR : OAK PORTS INDEX Register
001F	R/W(0-7)	OAKDAT : OAK PORTS DATA Register
0092	W (3)	SYSCNLA : SYSTEM CONTROL PORT A

NOTE: To access any OTI special port, write the index to port 1E(Hex) first, then perform READ/WRITE operation to data port 1F(Hex). After each access to port 1F(Hex), the index value inside port 1E(Hex) is automatically reset to 00(Hex).

SPECIAL I/O MAP - OTI-055

INDEX ADDR	ACCESS	FUNCTION NAME
0040	R/W(0-7)	NMICTL : NMI Enable Register
0041	R/W(0-7)	RNGCTR : Ring Count Register
0042	R/W(0-7)	TIMERL : Timer Count Register- Low byte
0043	R/W(0-7)	TIMERH : Timer Count Register-High byte
0044	R/W(0-1)	WAKEUP : WakeUp Control Register
0045	R/W(0-1)	PWRCTL : Power Control Register
0046	R(0-7)	OAKSTS : OTI-055 Status Register
0048	R/W(0-7)	PWRIOL : Direction Control Register 0
0049	R/W(0-7)	PWROTL : Output Control Register 0
004A	R(0-7)	PWRINL : Input Status Register 0
004B	R/W(0-7)	PWRIOH : Direction Control Register 1
004C	R/W(0-7)	PWROTH : Output Control Register 1
004D	R(0-7)	PWRINH : Input Status Register 1
004F	R(0-7)	CHIPID : OTI-055 ID Register
I/O ADDRESS	**ACCESS**	**FUNCTION NAME**
001E	R/W(0-7)	OAKADR : OAK PORTS INDEX Register
001F	R/W(0-7)	OAKDAT : OAK PORTS DATA Register

NOTE: To access any OTI special port, write the index to port 1E(Hex) first, then perform READ/WRITE operation to data port 1F(Hex). After each access to port 1F(Hex), the index value inside port 1E(Hex) is automatically reset to 00(Hex).

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SECTION 7

SCHEMATIC DIAGRAMS

VCC
R21
470 OHM

VCC
R24
4.7K

P3,4,5 SRDY-   SRDY-

P3,4 NPRST   NPRST

SA[0..23]   SA[0..23] P3,4,5,6

BHE-   BHE- P3,4,5,6

U21
P3,4,5 CPUCLK   CPUCLK   7 READY*
P3,4 RESETCPU   RESETCPU   15 CLK2
                             33 RESET

A1 18 SA1
A2 51 SA2
A3 53 SA3
A4 54 SA4
A5 55 SA5
A6 56 SA6
A7 57 SA7
A8 58 SA8
A9 59 SA9
A10 60 SA10
A11 61 SA11
A12 62 SA12
A13 64 SA13
A14 65 SA14
A15 66 SA15
A16 70 SA16
A17 72 SA17
A18 73 SA18
A19 74 SA19
A20 75 SA20
A21 76 SA21
A22 79 SA22
A23 80 SA23

P3,4,5 M/IO-   M/IO-   23 M/IO*
P3,7 NMI   NMI   26 LOCK*
P3,4,13 INTR   INTR   38 NMI
                            40 INTR

U22
                                49 READY*   D0 19 SD0
                                54 CPUCLK2   D1 20 SD1
                                51 RESETIN   D2 23 SD2
R23   D3 7 SD3
VCC   53 NUMCLK2   D4 5 SD4
4.7K   D5 6 SD5
                                40 STEN   D6 8 SD6
                                                D7 24 SD7
P3,5 CPUHRQ   CPUHRQ   4 HOLD   D8 28 SD8
P3,5 CPUHLDA   CPUHLDA   3 HLDA   D9 29 SD9
                                59 CKM   D10 30 SD10
VCC R22 20K   D11 16 SD11
P3,13 CPUBUSY-   CPUBUSY- 36 ERROR*   D12 15 SD12
P13 CPEREQ   CPEREQ   34 BUSY*   D13 12 SD13
                            37 PEREQ   D14 11 SD14
                                                D15   SD15

R26   44 NPS1*   ERROR* 35 NPERR-   NPERR- P3,13
51 OHM   SA23 45 NPS2   BUSY* 36 NPBSY-   NPBSY- P3,13
VCC   6 N/A*   SA2 48 CMDD*
39 VDD   W/R*   41
8 VDD   VCC   ADS*   47
10 VDD   BHE* 19 BHE*   39 HIGH1   PEREQ 56 NPEREQ   NPEREQ P3,13
21 VDD   50 HIGH2   READY* 57
32 VDD   D0 100 SD0
42 VDD   D1 99 SD1   26 VDD   VSS 14
48 VDD   D2 98 SD2   31 VDD   VSS 21
69 VDD   D3 96 SD3   33 VDD   VSS 25
69 VDD   D4 84 SD4   37 VDD   VSS 27
71 VDD   D5 93 SD5   46 VDD   VSS 32
84 VDD   D6 92 SD6   58 VDD   VSS 34
91 VDD   D7 90 SD7   64 VDD   VSS 39
92 VDD   D8 89 SD8   58 VDD   VSS 42
         D9 88 SD9   22 VDD   VSS 66
         D10 87 SD10   13 VDD   VSS 63
         D11 86 SD11   4 VDD   VSS 60
5 VSS   D12 83 SD12   9 VDD   VSS 61
11 VSS   D13 82 SD13
49 VSS   D14 81 SD14   IC, 80387SX
50 VSS   D15   SD15
63 VSS
67 VSS   BLE* 17 SA0
68 VSS
13 VSS   ADS* 16
14 VSS   DC* 24
77 VSS
78 VSS   W/R* 25   SD[0..15]   SD[0..15] P3,4,7,10,11
85 VSS   ADS-   ADS- P4,5
98 VSS   VSS 2
         VSS 41   S1-   S1- P3,4,5
IC, 80386SX VSS 35   S0-   S0- P3,4,5

R25   R27
4.7K VCC   4.7K VCC

P3,13 NPCS-   NPCS-

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Title
OAKHORIZON, 80386SX AND 80387SX
Size Document Number   REV
B   OTI-050   C
Date: September 5, 1989 Sheet 2 of 19

P2,4 NPRST

SA[0..23] SA[0..23] P2,4,5,6
BHE- BHE- P2,4,5,6

U31
IC, 80286

VCC R32 4.7K

U32
IC, 80287

P2,4,5 SRDY-
P2,4,5 CPUCLK
P2,4 RESETCPU

P2,4,5 S0-
        S1-

P2,4,5 M/IO-

P2,7 NMI
P2,4,13 INTR

P2,5 CPUHRQ
P2,5 CPUHLDA

P2,13 CPUBUSY-

NPERR- NPERR- P2,13
NPBSY- NPBSY- P2,13
NPEREQ NPEREQ P2,13

SD[0..15] SD[0..15] P2,4,7,10,11

P4,5,6,7,8,12,13,14,19 IORD-
P4,5,6,7,8,12,13,14,19 IOWR-
P2,13 NPCS-
P6,8,11,12,13,14,15,16,19 PCA[0..19]

JP31
CONN, 5 PIN HEADER

FOR 80386SX CPU:
- JUMP 1 TO 2
- JUMP 3 TO 4

FOR 80286 CPU:
- JUMP 2 TO 3
- JUMP 4 TO 5

CLK32M [CLK32M] P13

VCC
Y41
OUT 8
40MHZ

VCC
Y42
OUT 8
32MHZ

VCC
R44
4.7K
JP42
CONN, 3 PIN HEADER

R43
22 OHM
R42
22 OHM

VCC
D41
1N4148
RP41A
4.7K

R41
47 OHM
C41
0.047UF
JP41 1 2 3
RESET SW

IC, OTI-051
U41

Pin	Signal		Signal	Pin	Net	Ports

73 CLKIN0 — BUSCLK 1 BUSCLK [BUSCLK] P9
71 CLKIN1 — CLK8 31 CLK8 P5,7,8,12,13,14,16,19
74 RSTIN — RESET 4 RESET [RESET] P5,6,16
70 PWRGOOD — MASTER- 29 MASTER- [MASTER-] P13
80 SRDY- — INTA- 13 INTA- [INTA-] P2,3,13
12 NMI — INTR 3 INTR [INTR] P5,14,16,19
69 CPUCLK — IOCHRDY 5 IOCHRDY [IOCHRDY] P14,16
33 RESETCPU — IOCK- 6 IOCK- [IOCK-] P5,13,16
97 SD15 — MREF 2 MREF- [MREF-] P5
96 SD14 — PAR1 99 PAR1 [PAR1] P10
95 SD13 — PAR0 100 PAR0 [PAR0]
94 SD12 — COMRQ 37 COMRQ- [COMRQ-] P5
93 SD11 — WS0 7 0WS- [0WS-] P16
92 SD10 — IOCS16 8 IOCS16- [IOCS16-] P16,19
91 SD9 — MEMCS16 9 MEMCS16- [MEMCS16-] P16,19
90 SD8 — RESET8042 32 RESET8042- [RESET8042-] P8
89 SD7 — SECCHK 34
88 SD6 — TIMER2 35 TIMER2 [TIMER2] P13
87 SD5
86 SD4
85 SD3 — A20 39 A20 [A20] P5,6
84 SD2 — GATEA20 40 GATE20 [GATE20] P5,6,7
83 SD1 — A0 41 A0 [A0]
82 SD0 — BHE- 42 BHE- [BHE-] P2,3,5,6

76 ADS — PCALE 11 PCALE [PCALE] P16
77 S0-/WR- — ROMCS 18 ROMCS- [ROMCS-] P11
78 S1-/DC- — VDRMSEL 17 VDRMSEL- [VDRMSEL-] P13,14
79 M/IO- — VDPMSEL 16 VDPMSEL- [VDPMSEL-] P13
68 SA23 — VDIOSEL 15 VDIOSEL- [VDIOSEL-] P7,13
67 SA22 — SEL0 14 SEL0- [SEL0-] P14
66 SA21 — MEMRD 28 MEMRD- [MEMRD-] P5,6,11,13,14
65 SA20 — MEMWR 27 MEMWR- [MEMWR-] P5,6,13,14
64 SA19 — IORD 26 IORD- [IORD-] P3,5,6,7,8,12,13,14,19
63 SA18 — IOWR 25 IOWR- [IOWR-]
62 SA17 — CMDEN 20 CMDEN- [CMDEN-] P6
60 SA16
59 SA15 — PCENH 22 PCENH- [PCENH-] P7
58 SA14 — PCENL 23 PCENL- [PCENL-] P7
57 SA13 — ALE 38 ALE P6
56 SA12 — PCDIR 21 PCDIR [PCDIR] P7
55 SA11 — ENSWAP 24 ENSWAP [ENSWAP] P7
54 SA10 — AEN 36 AEN [AEN] P5,6,13,14,16
63 SA9 — VSS 90
52 SA8 — VSS 72
51 SA7 — VSS 43
50 SA6 — VSS 19
49 SA5 — NPRST 30 NPRST [NPRST] P2,3

P6,7,18 [PWRGOOD] PWRGOOD
P2,3,5 [SRDY-] SRDY-
P7 [NMIIN0] NMIIN0
P2,3,5 [CPUCLK] CPUCLK
P2,3 [RESETCPU] RESETCPU
R47 22 OHM

P2,3,7,10,11 [SD[0..15]] SD[0..15]
P2,3,5 [S0-] S0-
P2,3,5 [S1-] S1-
P2,3,5 [M/IO-] M/IO-

P2,5 [ADS-] ADS-
N.C. WHEN CPU IS 80286
R48 1M

P2,3,5,6 [SA[0..23]] SA[0..23]

SA4
SA3
SA2
SA1
SA0

R45 22 OHM
R46

OAK TECHNOLOGY, INC.
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Title
OAKHORIZON, OTI-051
Size B Document Number OTI-050 REV C
Date: September 5, 1989 Sheet 4 of 19

P9,12,16,19   DRQ[0..7]   DRQ[0..7]

U51
IC, OTI-053

P2,3,4   CPUCLK   CPUCLK   43 CPUCLK   DDDD DRQ5 96 DRQ5
P4   MDIR   MDIR   32 MDIR   RRRR DRQ6 95 DRQ6
P9   COMRQ-   COMRQ-   33 COMRQ   QQQQ DRQ7 93 DRQ7
P13   REFREQ   REFREQ   34 REFREQ   0123 DACK0 92 DACK0-   P16
P4,7,8,12,13,14,16,19   RESET   RESET   42 RESET   DACK1 91 DACK1-   P16
P2,3,4   SRDY-   SRDY-   40 SRDY   DACK2 90 DACK2-   P12,13,16
P4,13,16   MREF-   MREF-   31 MREF   DACK3 89 DACK3-   P13,16
                DACK4 88 DACK4-   P16
                DACK5 87 DACK5-   P16
P3,4,6,7,8,12,13,14,19   IOWR-   IOWR-   84 IOWR   DACK6 86 DACK6-   P16
P3,4,6,7,8,12,13,14,19   IORD-   IORD-   83 IORD   DACK7 85 DACK7-   P12,16
P4,6,11,13,14   MEMWR-   MEMWR-   81 MEMWR   TC 79 TC   P12,16
P2,3   MEMRD-   MEMRD-   82 MEMRD   AEN 80 AEN   P4,6,13,14,16
P2,3   CPUHRQ   CPUHRQ   78 CPUHRQ
P4,14,16,19   CPUHLDA   CPUHLDA   77 CPUHLDA   CROMCS0 35
P4,6,13   IOCHRDY   IOCHRDY   76 IOCHRDY   RAS7 13 RAS7-   P10
P4   MASTER-   MASTER-   75 MASTER   RAS6 14 RAS6-   P10
        CLK8   CLK8   36 CLK8   RAS5 15 RAS5-
                RAS4 16 RAS4-   P10
        VCC   74 VDD   RAS3 18 RAS3-
                63 VDD   RAS2 19 RAS2-   P10
                38 VDD   RAS1 20 RAS1-
                12 VDD   RAS0 22 RAS0-   P10
P4,6,7   A0   A0   47 A0   CASH3 23 CASH3-   P10
P2,4,6   BHE-   BHE-   46 BHE-   CASH2 24 CASH2-   P10
P2,4   ADS-   ADS-   41 ADS-   CASH1 25 CASH1-   P10
P2,3   S0-   S0-   40 S0-/WR-   CASH0 27 CASH0-   P10
P2,3   S1-   S1-   39 S1-/DC-   CASL3 28 CASL3-   P10
P2,3,4   M/IO-   M/IO-   37 M/IO-   CASL2 29 CASL2-   P10
                CASL1 30 CASL1-   P10
        SA23   73 SA23   CASL0 30 CASL0-   P10
        SA22   72 SA22   MA10 2 MA10
        SA21   71 SA21   MA9 3 MA9
P4,6   A20   A20   70 A20   MA8/XD7 4 MA8
        SA19   68 SA19   MA7/XD6 5 MA7
        SA18   67 SA18   MA6/XD5 6 MA6
        SA17   66 SA17   MA5/XD4 7 MA5
        SA16   65 SA16   MA4/XD3 9 MA4
        SA15   64 SA15   MA3/XD2 10 MA3
        SA14   62 SA14   MA2/XD1 11 MA2
        SA13   61 SA13   MA1/XD0 11 MA1
        SA12   60 SA12   VSS 94
        SA11   59 SA11   VSS 69   MA[0..10]   P7,9,10
        SA10   58 SA10   VSS 65
        SA9   57 SA9   VSS 44
        SA8   56 SA8   VSS 26
        SA7   54 SA7   VSS 6
        SA6   53 SA6
        SA5   52 SA5
        SA4
        SA3
        SA2
        SA1

P2,3,4,6   SA[1..23]   SA[1..23]

JP51   JP52
RAS0- 1 2 RAS1-   CASH0- 1 2 CASL0-
RAS2- 3 4 RAS3-   CASH1- 3 4 CASL1-
RAS4- 5 6 RAS5-   CASH2- 5 6 CASL2-
RAS6- 7 8 RAS7-   CASH3- 7 8 CASL3-
CONN, 4X2 PIN HEADER   CONN, 4X2 PIN HEADER

OAK TECHNOLOGY, INC.
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Title
OAKHORIZON, OTI-053
Size Document Number   REV
B   OTI-050   C
Date: September 5, 1989 Sheet 5 of 19

LA[17..23] LA[17..23] P16

U61
IC, OTI-054

P7
P4,5,16   MAXD-   MAXD-
           MASTER-   MASTER-   VCC

P8,9,12,13,14,16,19   XD[0..7]   XD[0..7]

P18   BATT   BATT
                        D61 1N4148
                        VCC   4.7UF
                        C61   C62
                        0.1UF
                        D62
                        1N4148

PCA[0..19] PCA[0..19] P3,8,11,12,13,14,15,16,19

P4,7,17   PWRGOOD   PWRGOOD
P7,13   MINCLK   MINCLK
P13   IRQ8   IRQ8

RP61B RP61D VCC
RP61A RP61C   RP61E
                    4.7K

P4,5,13,14,16   AEN   AEN
P4   CMDEN-   CMDEN-
P4,5,11,13,14   MEMRD-   MEMRD-
P4,5,13,14   MEMWR-   MEMWR-
P3,4,5,7,8,12,13,14,19 IORD-   IORD-
P3,4,5,7,8,12,13,14,19 IOWR-   IOWR-
P4   ALE   ALE

PCBHE-   PCBHE-   P16
PCIORD- PCIORD- P16
PCIOWR- PCIOWR- P16
PCMEMRD- PCMEMRD- P16
PCMEMWR- PCMEMWR- P16
ATMEMRD- ATMEMRD- P16
ATMEMWR- ATMEMWR- P16
PWCS-   PWCS-   P7

P4,5   A20   A20

Y61
32.768KHZ

C63   C64
20PF   20PF

P2,3,4,5   SA[1..23]   SA[1..23]

P4,5,7   A0   A0
P2,3,4,5   BHE-   BHE-

OAK TECHNOLOGY, INC.
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Title
OAKHORIZON, OTI-054
Size Document Number   REV
B   OTI-050   C
Date: September 5, 1989 Sheet 6 of 19

IC, OTI-055
U71

P13
P2,3
RING-   RING-
NMI   NMI

P4   NMIINO   NMIINO
P4   ENSWAP   ENSWAP
P4   PCENH-   PCENH-
P4   PCENL-   PCENL-
P4   PCDIR   PCDIR
P2,3,4,10,11   SD[0..15]   SD[0..15]

9   RING   VVVVVV   PCD15   80   PCD15
7   NMIOUT   DDDDDD   PCD14   79   PCD14
8   NMIIN1   DDDDDD   PCD13   78   PCD13
6   NMIIN0   PCD12   76   PCD12
5   ENSWAP   PCD11   75   PCD11
4   PCD10   74   PCD10
3   DENH   PCD9   72   PCD9
2   DENL   PCD8   71   PCD8
1   PCDIR   PCD7   69   PCD7
15   SD15   PCD6   68   PCD6
100   SD14   PCD5   66   PCD5
99   SD13   PCD4   65   PCD4
98   SD12   PCD3   64   PCD3
96   SD11   PCD2   62   PCD2
95   SD10   PCD1   61   PCD1
94   SD9   PCD0   60   PCD0
92   SD8
90   SD7
89   SD6   TEST   35
87   SD5   SEL0   36   VCC
86   SD4   N.C.   37
84   SD3   57
83   SD2
82   SD1
81   SD0

PCD[0..15]   PCD[0..15]   P16,19

SEL0   SEL0   P4

R71
51 OHM

P6   PWCS-   PWCS-
P4,5,6   A0   A0
P3,4,5,6,8,12,13,14,19   IORD-   IORD-
P3,4,5,6,8,12,13,14,19   IOWR-   IOWR-
P4,5,8,12,13,14,15,16,19   RESET   RESET
P4,6,17   PWRGOOD   PWRGOOD
P6   MAXD-   MAXD-

16   PWCS   PWOFF15   33   PWOFF15
14   A0   PWOFF14   32   PWOFF14
12   IORD-   PWOFF13   31   PWOFF13
13   IOWR-   PWOFF12   30   PWOFF12
10   RESET   PWOFF11   29   PWOFF11
38   POWERGOOD   PWOFF10   28   PWOFF10
46   MAXD   PWOFF9   26   PWOFF9
55   MA8   PWOFF8   25   PWOFF8
54   MA7   PWOFF7   24   PWOFF7
53   MA6   PWOFF6   23   PWOFF6
52   MA5   PWOFF5   21   PWOFF5
51   MA4   PWOFF4   20   PWOFF4
50   MA3   PWOFF3   19   PWOFF3
49   MA2   PWOFF2   18   PWOFF2
47   MA1   PWOFF1   17   PWOFF1
  PWOFF0   42
  SYSPWR   41
  MODPWR   40   GO TO POWER SUPPLY TO CONTROL INDIVIDUAL POWER OF VARIOUS DEVICES

MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1

P5,9,10   MA[1..10]   MA[1..10]

P6,13   MINCLK   MINCLK

58   MINCLK   VSS   97
43   BATT2   VSS   93
44   BATT1   VSS   85
45   BATT0   VSS   77
34   D/SRAM   VSS   73

VCC
R72
4.7K
R73
4.7K
R74
4.7K
VCC
R75
4.7K
VCC

123
JP71

JP72
PWOFF0   1   2   PWOFF1
PWOFF2   3   4   PWOFF3
PWOFF4   5   6   PWOFF5
PWOFF6   7   8   PWOFF7
PWOFF8   9   10   PWOFF9
PWOFF10   11   12   PWOFF11
PWOFF12   13   14   PWOFF13
PWOFF14   15   16   PWOFF15
CONN, 8X2 PIN HEADER

OAK TECHNOLOGY, INC.
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Title
OAKHORIZON, OTI-055
Size | Document Number | REV
B | OTI-050 | C
Date: September 5, 1989 | Sheet | 7 of | 19

P5,7,10,11 MAC0..10J   MAC1..10J

U91
MA1 2 1A1 1Y1 18 AMA1
MA2 4 1A2 1Y2 16 AMA2
MA3 6 1A3 1Y3 14 AMA3
MA4 8 1A4 1Y4 12 AMA4
MA5 11 2A1 2Y1 9   AMA5
MA6 13 2A2 2Y2 7   AMA6
MA7 15 2A3 2Y3 5   AMA7
MA8 17 2A4 2Y4 3   AMA8
1 1G
19 2G
IC, 74F244

AMAC1..10J AMAC1..10J P10

U92
MA1 2 1A1 1Y1 18 BMA1
MA2 4 1A2 1Y2 16 BMA2
MA3 6 1A3 1Y3 14 BMA3
MA4 8 1A4 1Y4 12 BMA4
MA5 11 2A1 2Y1 9   BMA5
MA6 13 2A2 2Y2 7   BMA6
MA7 15 2A3 2Y3 5   BMA7
MA8 17 2A4 2Y4 3   BMA8
1 1G
19 2G
IC, 74F244

BMAC1..10J BMAC1..10J P10

U93
MA1 2 1A1 1Y1 18 CMA1
MA2 4 1A2 1Y2 16 CMA2
MA3 6 1A3 1Y3 14 CMA3
MA4 8 1A4 1Y4 12 CMA4
MA5 11 2A1 2Y1 9   CMA5
MA6 13 2A2 2Y2 7   CMA6
MA7 15 2A3 2Y3 5   CMA7
MA8 17 2A4 2Y4 3   CMA8
1 1G
19 2G
IC, 74F244

CMAC1..10J CMAC1..10J P10

U94
MA9   2 1A1 1Y1 18 CMA9
      4 1A2 1Y2 16 BMA9
      6 1A3 1Y3 14 AMA9
MA10 8 1A4 1Y4 12 CMA10
P4 BUSCLK BUSCLK 11 2A1 2Y1 9 R91 22 OHM
              13 2A2 2Y2 7   BMA10   PCCLK PCCLK P16
P5 MDIR MDIR 15 2A3 2Y3 5   AMA10   BMDIR BMDIR P10
              17 2A4 2Y4 3
1 1G
19 2G
IC, 74F244

VCC
Y91
14.318MHZ
1 4
Q OUT 8
7

VCC
4.7K
R92

UD2A
1
2   3
IC, 74F00   BOSC BOSC P13,16

XDC0..7J XDC0..7J P6,8,12,13,14,19

U95
P12,19 FLPDIR FLPDIR 2 1A1 1Y1 18 XD0
P12,19 WRTPRT- WRTPRT- 4 1A2 1Y2 16 XD1
P12,19 INDEX-   INDEX-   6 1A3 1Y3 14 XD2
P12,19 HEAD   HEAD   8 1A4 1Y4 12 XD3
P12,19 TRK0-   TRK0-   11 2A1 2Y1 9   XD4
P12,19 STEP-   STEP-   13 2A2 2Y2 7   XD5
P5,12,16 DRQ2   DRQ2   15 2A3 2Y3 5   XD6
P12,13,16 IRQ6 IRQ6   17 2A4 2Y4 3   XD7
P13 RD3F0- RD3F0- 1 1G
                     19 2G
IC, 74ALS244

U96
2 1A1 1Y1 18 XD0
4 1A2 1Y2 16 XD1
6 1A3 1Y3 14 XD2
8 1A4 1Y4 12 XD3
11 2A1 2Y1 9   XD4
13 2A2 2Y2 7   XD5
15 2A3 2Y3 5   XD6
17 2A4 2Y4 3   XD7
1 1G
19 2G
IC, 74ALS244

P12,19 WGATE- WGATE-
P12,19 RDATA   RDATA
P12,19 WDATA   WDATA
P12,19 DRSELA- DRSELA-
P12,19 DRSELB- DRSELB-
P12,13 DRVTYPE DRVTYPE

P13 RD3F1- RD3F1-

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Title
OAKHORIZON, MEMORY ADDRESS BUS
Size Document Number   REV
B   OTI-050   C
Date: September 5, 1989 Sheet 9 of 19

2 MBYTE MEMORY SYSTEM
WITH 256K X 9 SIMM

OAK TECHNOLOGY, INC.
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Title
OAKHORIZON, SIMM SOCKETS

Size: B
Document Number: OTI-050
REV: C

Date: September 5, 1989 Sheet 10 of 19

U111

PCA1	10	A0	O0	11	SD0
PCA2	9	A1	O1	12	SD1
PCA3	8	A2	O2	13	SD2
PCA4	7	A3	O3	15	SD3
PCA5	6	A4	O4	16	SD4
PCA6	5	A5	O5	17	SD5
PCA7	4	A6	O6	18	SD6
PCA8	3	A7	O7	19	SD7
PCA9	25	A8
PCA10	24	A9
PCA11	21	A10
PCA12	23	A11
PCA13	2	A12
PCA14	26	A13
PCA15	27	A14
PCA16	1	A15
	20	CE
	22	OE

EPROM, 27C512

P4,5,6,13,14   MEMRD-   MEMRD-

U112

PCA1	10	A0	O0	11	SD8
PCA2	9	A1	O1	12	SD9
PCA3	8	A2	O2	13	SD10
PCA4	7	A3	O3	15	SD11
PCA5	6	A4	O4	16	SD12
PCA6	5	A5	O5	17	SD13
PCA7	4	A6	O6	18	SD14
PCA8	3	A7	O7	19	SD15
PCA9	25	A8
PCA10	24	A9
PCA11	21	A10
PCA12	23	A11
PCA13	2	A12
PCA14	26	A13
PCA15	27	A14
PCA16	1	A15
	20	CE
	22	OE

EPROM, 27C512

SD[0..15]   SD[0..15]   P2,3,4,7,10

P4   ROMCS-   ROMCS-

P3,6,8,12,13,14,15,16,19   PCA[1..16]   PCA[1..16]

P6,8,9,13,14,19   XD[0..7]   XD[0..7]

P3,6,8,11,12,13,14,15,16,19   PCA[0..2]   PCA[0..2]

P13
P3,4,5,6,7,8,13,14,19   FLPCS-   FLPCS-
P3,4,5,6,7,8,13,14,19   IORD-   IORD-
P5,9,16   IOWR-   IOWR-
P5,16   DRQ2   DRQ2
P9,13,16   TC   TC
P4,5,6,7,8,13,14,16,19   IRQ6   IRQ6
RESET   RESET

Y121
24MHZ

C122   C123
20PF   20PF

P5,13,16   DACK2-   DACK2-
P9,13   DRVTYPE   DRVTYPE
P13   PREN   PREN

VCC
C121
0.01UF

U121
XD0   22   D0   VCC   13
XD1   23   D1   VCCA   14
XD2   24   D2   WRTPRT   12
XD3   25   D3   INDEX   11
XD4   26   D4   TRK0   10
XD5   28   D5   STEP   50
XD6   29   D6   HDSEL   9
XD7   30   D7   DIR   3
PCA0   19   A0   WDATA   4
PCA1   20   A1   WGATE   49
PCA2   21   A2   DSKCHG/RG   35
FLPCS- 18   CS   RDATA   44
IORD- 17   RD   DR0   6
IOWR- 16   WR   DR1   5
DRQ2   31   DRQ   DR2   45
TC   33   TC   DR3   43
IRQ6   34   INT   MTR0   8
RESET 15   RESET   MTR1   7
       38   CLK/OS2   MTR2   52
       39   OSC1   MTR3   51
       27   GNDA   RPM/LC   48
       36   GNDB   SEICUR   46
       2   GNDC PUMP/PREN   40
       32   GNDD   FILTER   42
DACK2- 37   DACK   FGND250   42
DRVTYP 47   DRVTYP FGND500   41

IC, OTI-033PLCC

VCC
VCC
RP122B
RP122A
RP121B   RP122C
2.2K   RP122D
          RP122E
          RP122F
          150 OHM
6   7 23   2 3 4 5 6 7

VCC
RP121C   RP121D
2.2K   2.2K
4   5

WRTPRT-   WRTPRT-   P9,19
INDEX-   INDEX-   P9,19
TRK0-   TRK0-   P9,19
STEP-   STEP-   P9,19
HEAD   HEAD   P9,19
FLPDIR   FLPDIR   P9,19
WDATA   WDATA   P9,19
WGATE-   WGATE-   P9,19

RDATA   RDATA   P9,19
DRSELA-   DRSELA-   P9,19
DRSELB-   DRSELB-   P9,19

MTENA-   MTENA-   P19
MTENB-   MTENB-   P19

U01F
12   13
IC, 7406

DSKCHG-   DSKCHG-   P19

R121
5.6K

560 OHM
R123   R124
        560 OHM
R122
1M
C124   C126
1000PF   0.047UF
        C125
        0.033UF
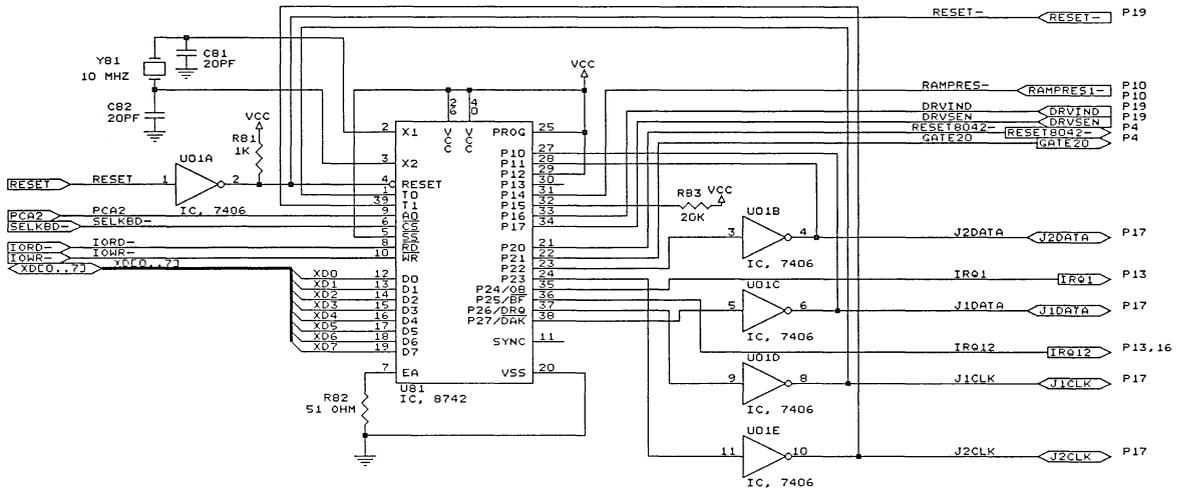
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Size Document Number   REV
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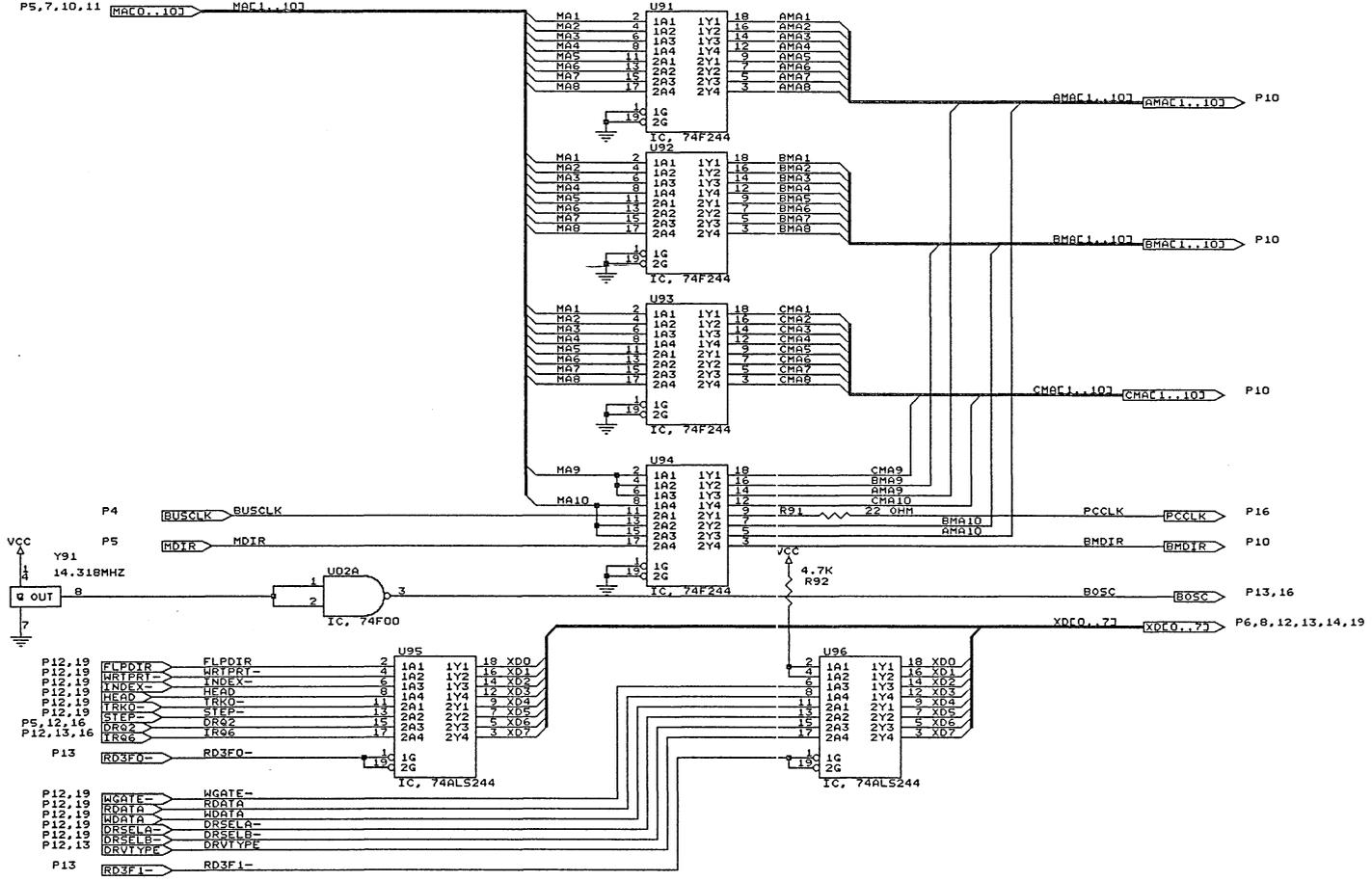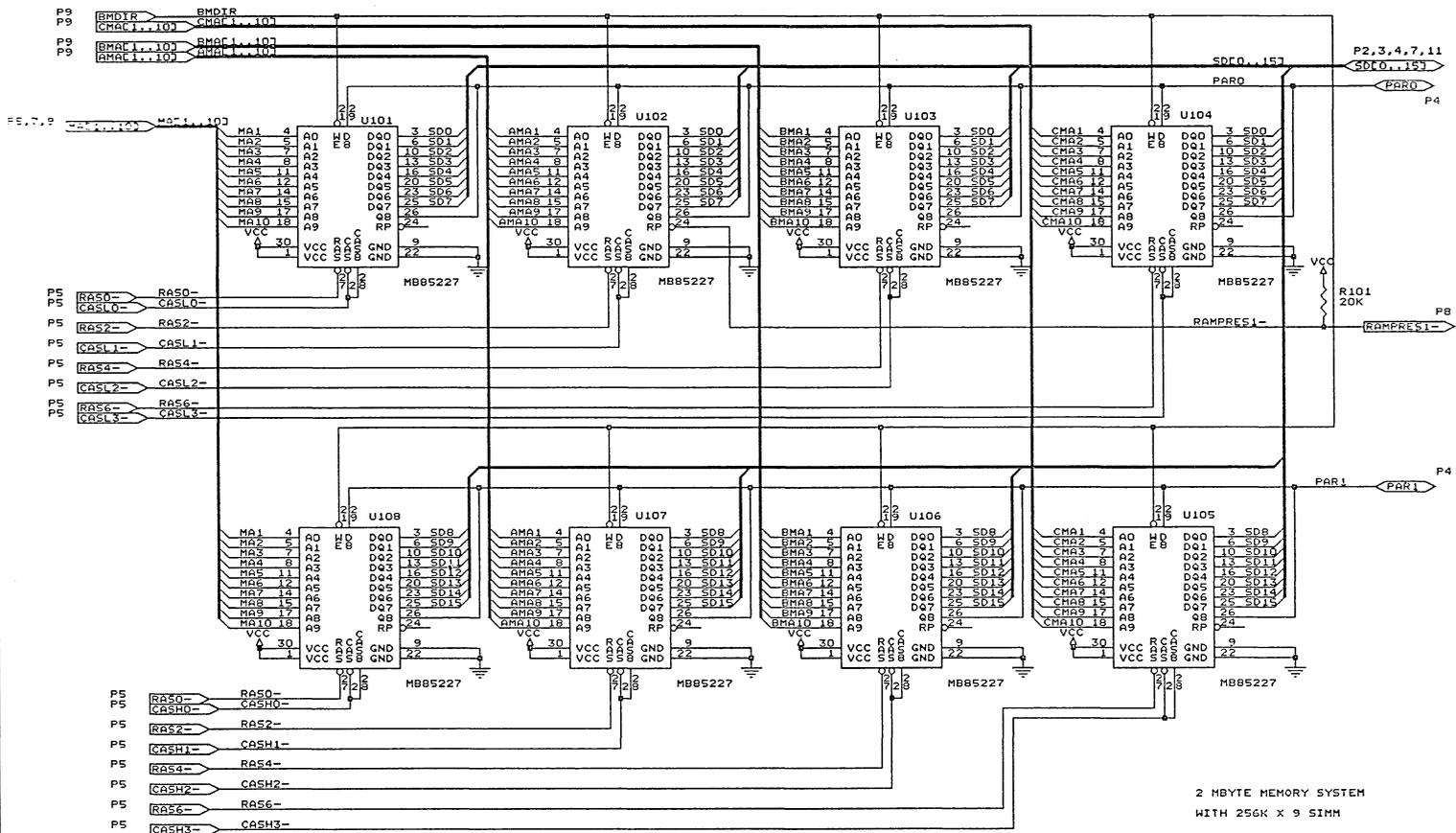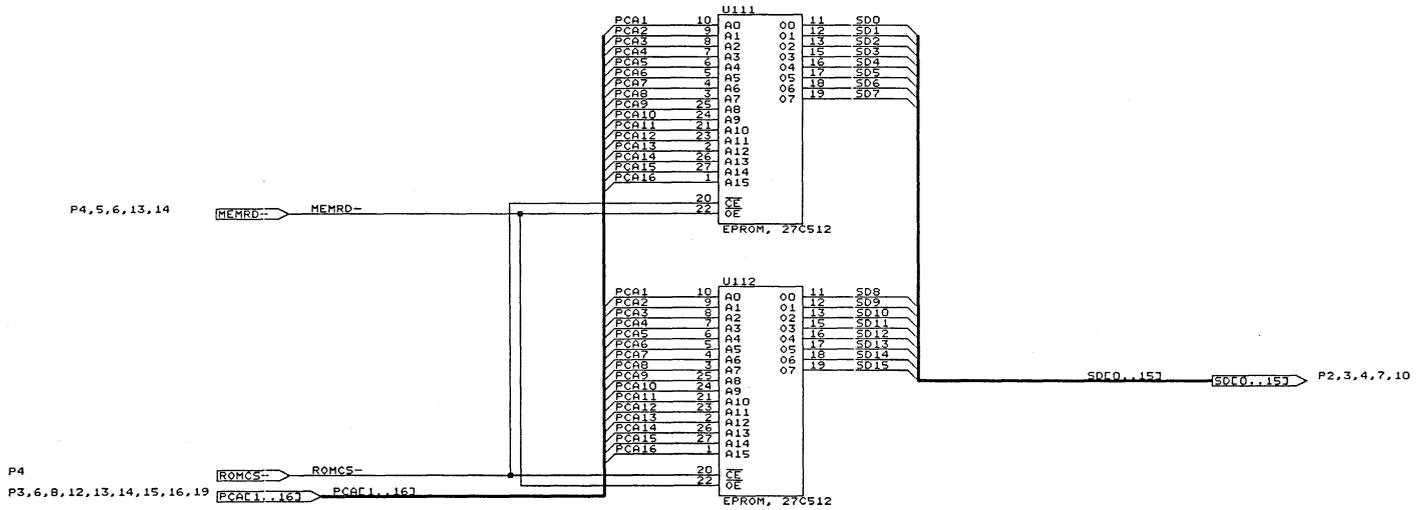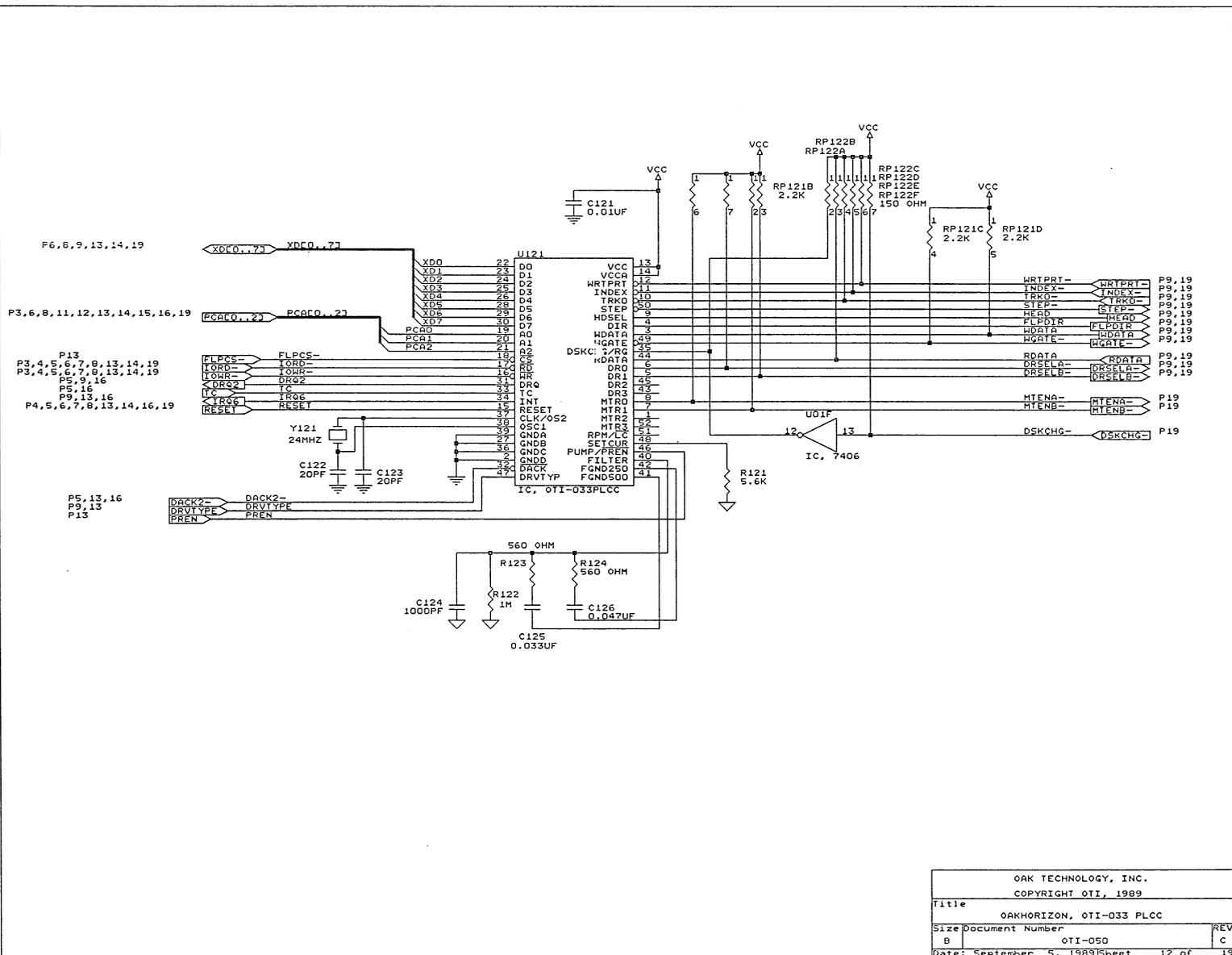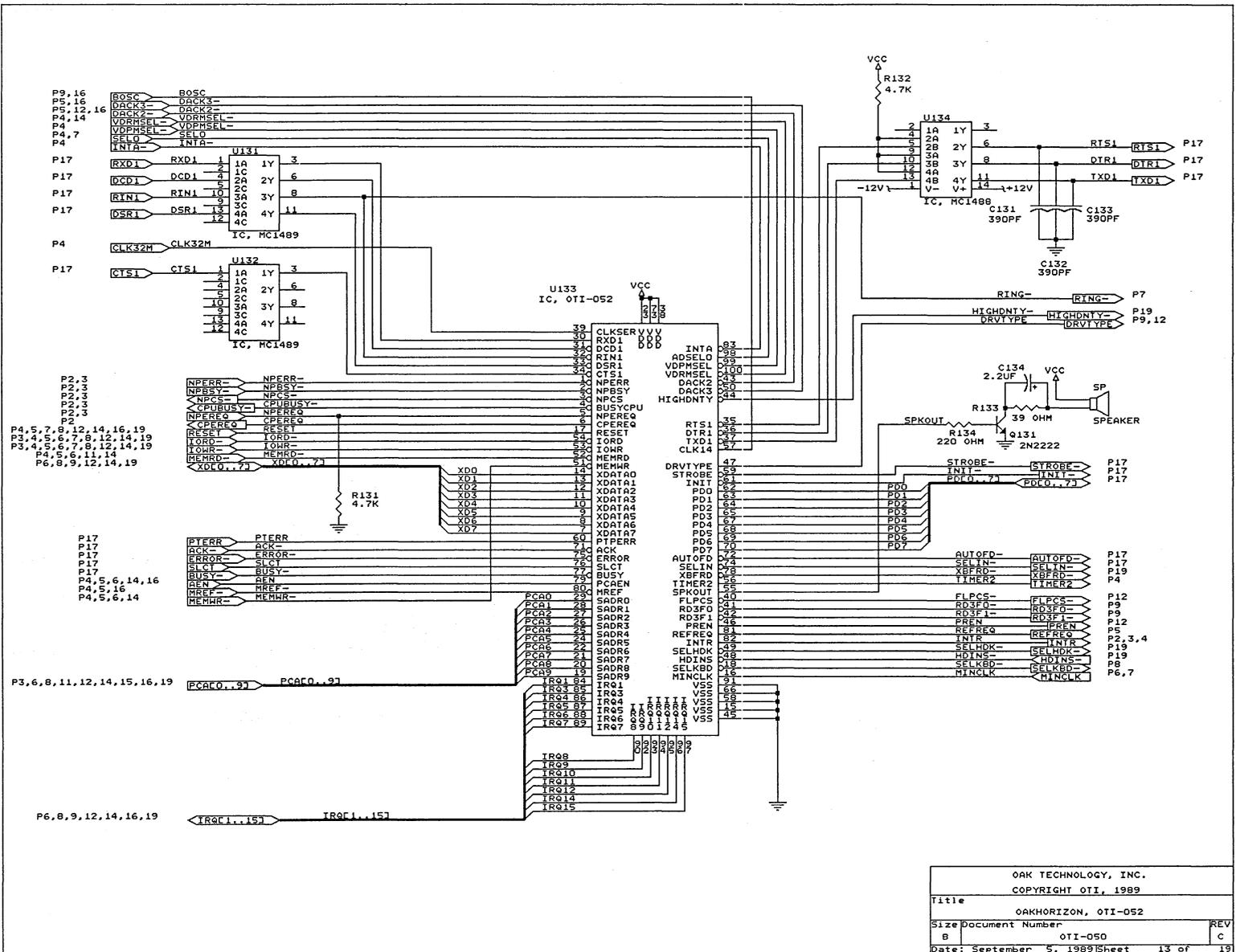Date: September 5, 1989 Sheet 12 of 19

Title
OAKHORIZON, IBM/AT BUS

Size	Document Number	REV
B	OTI-050	C

Date: September 5, 1989 Sheet 16 of 19

RP172C

VCC

RP172A RP172B   RP172D
4.7K   4.7K   4.7K 4.7K

PD7
PD6
PD5
PD4
P13 SELIN-   SELIN-   PD3
P13 INIT-   INIT-   PD2
P13 AUTOFD- AUTOFD- PD1
P13 STROBE- STROBE- PD0

PD[0..7]   PD[0..7] P13

C1713

C176 C178   C1712
C175 C177 C179 C1711
C1710
220PF

J7

SLCT   13
          25
PTERR   12
          24
BUSY-   11
          23
ACK-   10
          22
PD7   9
          21
PD6   8
          20
PD5   7
          19
PD4   6
          18
PD3   5
          17
SELIN-
PD2   4
          16
INIT-
PD1   3
          15
ERROR-
PD0   2
          14
AUTOFD-
STROBE-   1

PARALLEL PORT 1

JP13

STROBE-   1 2   AUTOFD-
PD0   3 4   ERROR-   ERROR- P13
PD1   5 6   INIT-
PD2   7 8   SELIN-
PD3   9 10
PD4   11 12
PD5   13 14
PD6   15 16
PD7   17 18
ACK-   19 20
P13 ACK-   21 22
P13 BUSY-   BUSY-
P13 PTERR   PTERR   23 24
P13 SLCT   SLCT   25 26

PARALLEL PORT 1

VCC

RP171A   RP171B
2.2K   2.2K

R171   3 OHM   2.2UH   J4
P8 J2DATA   J2DATA   1 A1
                       L171   2 A2
                          2.2UH 3 A3
P8 J2CLK   J2CLK   F171 L172   4 A4
             C172 C171 FUSE 1A 2.2UH 5 A5
             1000PF 1000PF 3 OHM L173 6 A6
                        R172

MOUSE CONNECTOR

J6

P13 DCD1   DCD1   1 2   RXD1   RXD1   P13
P13 TXD1   TXD1   3 4   DTR1   DTR1   P13
P13 RTS1   RTS1   5 6   DSR1   DSR1   P13
P13 RIN1   RIN1   7 8   CTS1   CTS1   P13
                   9 10

COM1

VCC

RP171C   RP171D
2.2K   2.2K

R173   3 OHM   2.2UH   J3
P8 J1DATA   J1DATA   1 A1
                       L174   2 A2
                          2.2UH 3 A3
P8 J1CLK   J1CLK   F172 L175   4 A4
             C174 C173 FUSE 1A 2.2UH 5 A5
             1000PF 1000PF 3 OHM L176 6 A6
                        R174

KEYBOARD CONNECTOR

P4,6,7 PWRGOOD PWRGOOD   J1
                           1 A1
                 +12V   2 A2
                 -12V   3 A3
                           4 A4
                           5 A5
                           6 A6

DC POWER CONNECTOR

VCC

J2
                 1 A1
-5V   2 A2
                 3 A3
                 4 A4
                 5 A5
                 6 A6

DC POWER CONNECTOR
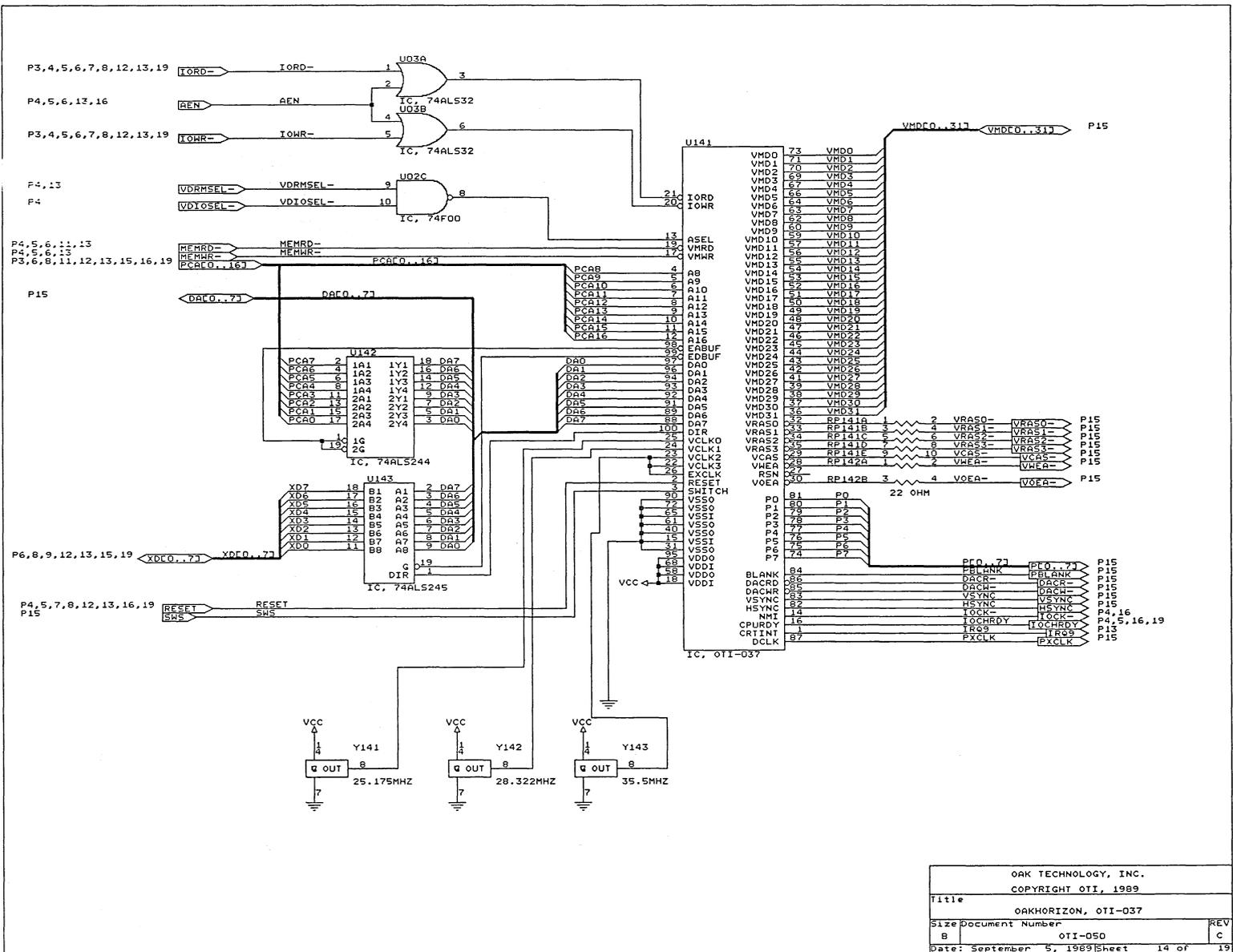
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OAKHORIZON, CONNECTORS

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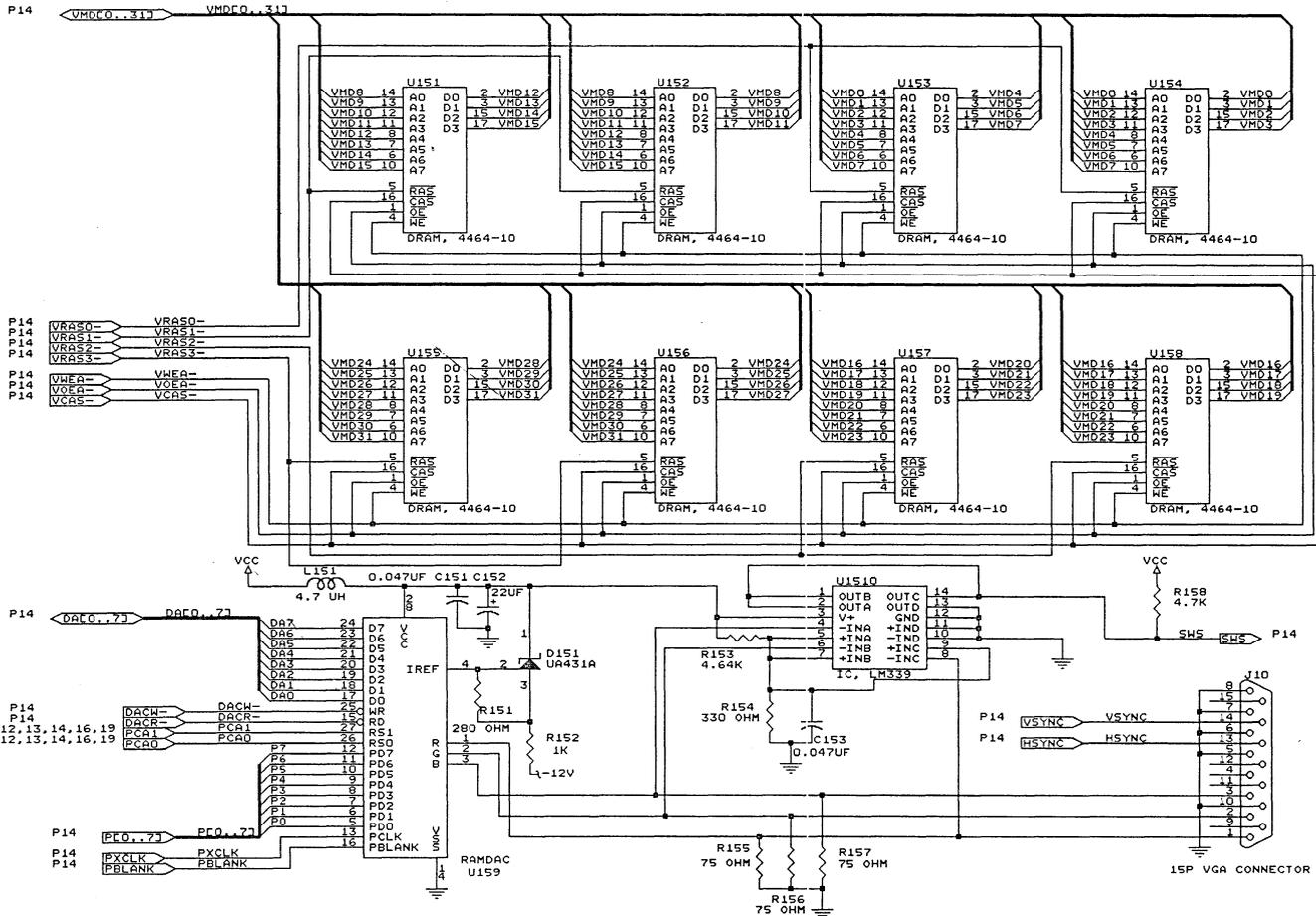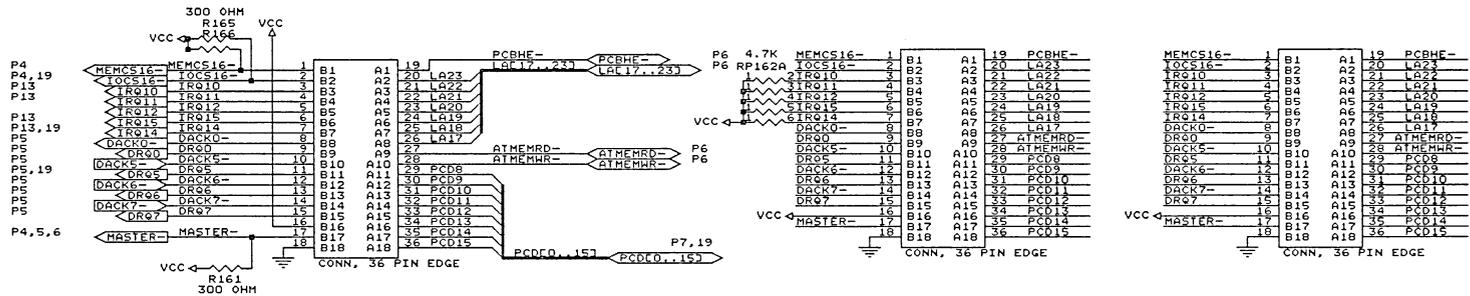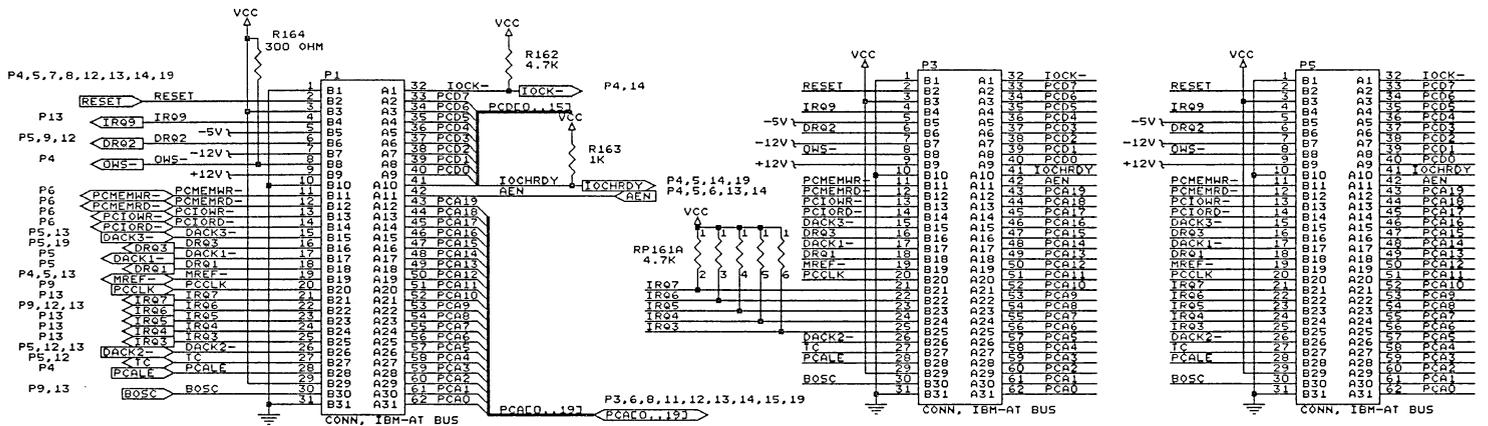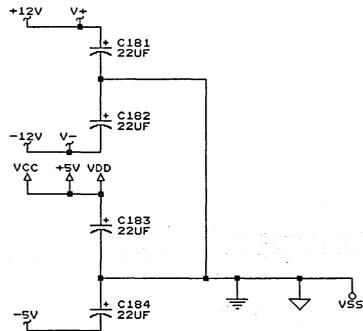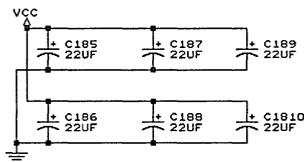
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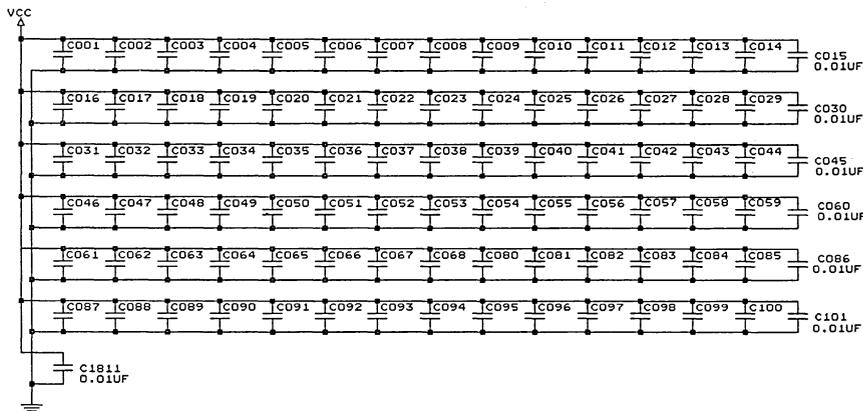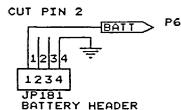
+12V V+
C181 22UF

C182 22UF
-12V V-

VCC +5V VDD
C183 22UF

C184 22UF
-5V

GND VSS

CAPACITORS AT POWER CONNECTORS

VCC
C185 22UF   C187 22UF   C189 22UF
C186 22UF   C188 22UF   C1810 22UF

CAPACITORS SCATTERED THROUGHOUT THE BOARD

VCC
CO69 10UF   CO70 10UF   CO71 10UF
CO72 10UF   CO73 10UF   CO74 10UF

CUT PIN 2
BATT   P6
1 2 3 4
JP181
BATTERY HEADER

VCC

C001 C002 C003 C004 C005 C006 C007 C008 C009 C010 C011 C012 C013 C014   C015 0.01UF
C016 C017 C018 C019 C020 C021 C022 C023 C024 C025 C026 C027 C028 C029   C030 0.01UF
C031 C032 C033 C034 C035 C036 C037 C038 C039 C040 C041 C042 C043 C044   C045 0.01UF
C046 C047 C048 C049 C050 C051 C052 C053 C054 C055 C056 C057 C058 C059   C060 0.01UF
C061 C062 C063 C064 C065 C066 C067 C068 C080 C081 C082 C083 C084 C085   C086 0.01UF
C087 C088 C089 C090 C091 C092 C093 C094 C095 C096 C097 C098 C099 C100   C101 0.01UF

C1811 0.01UF

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OAKHORIZON, BYPASS CAPACITORS
Size B
Document Number   OTI-050   REV C
Date: September 6, 1989   Sheet 18 of 19

CONNER'S AT HARD DISK INTERFACE

PCDC0..7]

U191

PCD0 2 A1 B1 18 XD0   XDC0..7]
PCD1 3 A2 B2 17 XD1
PCD2 4 A3 B3 16 XD2
PCD3 5 A4 B4 15 XD3
PCD4 6 A5 B5 14 XD4
PCD5 7 A6 B6 13 XD5
PCD6 8 A7 B7 12 XD6
PCD7 9 A8 B8 11 XD7

P13 XBFRD- XBFRD-
19 G
1 DIR

IC, 74ALS245

P8 RESET- RESET-

J12

XD7 2 A1 B1 21
XD6 3 A2 B2 22 PCD8
XD5 4 A3 B3 23 PCD9
XD4 5 A4 B4 24 PCD10
XD3 6 A5 B5 25 PCD11
XD2 7 A6 B6 26 PCD12
XD1 8 A7 B7 27 PCD13
XD0 9 A8 B8 28 PCD14
10 A9 B9 29 PCD15

P6,8,9,12,13,14 XDC0..7] XDC0..7] 11 A10 B10 30
P3,4,5,6,7,8,12,13,14,16 IOWR- IOWR- 12 A11 B11 31
P3,4,5,6,7,8,12,13,14,16 IORD- IORD- 13 A12 B12 32
14 A13 B13 33
15 A14 B14 34
P13,16 IRQ14 IRQ14 16 A15 B15 35
17 A16 B16 36 IOCS16- IOCS16- P4,16
PCA1 18 A17 B17 37
PCA0 19 A18 B18 38 PCA2
20 A19 B19 39 HDINS-
P3,6,8,11,12,13,14,15,16 PCAC0..19] PCAC0..3] A20 B20 40

P13 SELHDK- SELHDK-

CONN, 20X2 PIN HEADER

VCC D191 R191
LED 220 OHM

PCDC0..15] PCDC0..15] P7,16

IBM IDE HARD DISK INTERFACE
J9

VCC
VCC
R192
4.7K

P4,5,7,8,12,13,14,16 RESET RESET

XD0 1 A1 B1 23
XD1 2 A2 B2 24
XD2 3 A3 B3 25
XD3 4 A4 B4 26
XD4 5 A5 B5 27
XD5 6 A6 B6 28
XD6 7 A7 B7 29
XD7 8 A8 B8 30
9 A9 B9 31

HDINS- HDINS- P13

P6,8,9,12,13,14,19 XDC0..7] XDC0..7] 10 A10 B10 32
IORD- 11 A11 B11 33
IOWR- 12 A12 B12 34
SELHDK- 13 A13 B13 35
PCA0 14 A14 B14 36
PCA1 15 A15 B15 37
PCA2 16 A16 B16 38
PCAC0..19] 17 A17 B17 39
18 A18 B18 40
P5,16 DRQ3 DRQ3 19 A19 B19 41
IRQ14 20 A20 B20 42
P4,5,14,16 IOCHRDY IOCHRDY 21 A21 B21 43
22 A22 B22 44

+12V

J8 FLOPPY CONNECTOR

VCC

1 A1 B1 21 HIGHDNTY- HIGHDNTY- P13
2 A2 B2 22 DRVIND DRVIND P8
3 A3 B3 23
4 A4 B4 24 INDEX- INDEX- P9,12
5 A5 B5 25 MTENA- MTENA- P12
6 A6 B6 26 DRVSELB- DRSELB- P9,12
7 A7 B7 27 DRVSELA- DRSELA- P9,12
8 A8 B8 28 MTENB- MTENB- P12
9 A9 B9 29 FLPDIR FLPDIR P9,12
10 A10 B10 30 STEP- STEP- P9,12
11 A11 B11 31 WDATA WDATA P9,12
12 A12 B12 32 WGATE- WGATE- P9,12
13 A13 B13 33 TRK0- TRK0- P9,12
14 A14 B14 34 WRTPRT- WRTPRT- P9,12
15 A15 B15 35 RDATA RDATA P9,12
16 A16 B16 36 HEAD HEAD P9,12
17 A17 B17 37 DSKCHG- DSKCHG- P12
P8 DRVSEN DRVSEN 18 A18 B18 38
19 A19 B19 39
20 A20 B20 40

+12V

NOTE: USE 34-PIN CONNECTOR FOR AT-TYPE INTERFACE
ROW 18 TO 20 USED IN PS2-TYPE INTERFACE ONLY

SECTION 8

BILL OF MATERIAL

l.0 BILL OF MATERIAL - LAPTOP SYSTEM

Part Number	Description	Quantity
OakHorizon Chip Set:		
OTI-051	System Support Logic	1
OTI-052	I/O Controller	1
OTI-053	DMA and Memory Controller	1
OTI-054	Address Buffer/Real Time Clock	1
OTI-055	Data Buffer/Power Manager	1
Basic System:		
80286 or 80386SX	CPU	1
8042	Keyboard Controller	1
27C512-200	BIOS EPROM	2
Additional Logic:		
32 MHz	Oscillator	1
14.318 MHz	Oscillator	1
32.768 KHz	Crystal	1
10 MHz	Crystal	1
7406	IC	1
HCT00	IC	1
Memory	DRAM	Depends on system
Floppy Drive:*		
National/equiv.	Controller/Data Separator	1
24 MHz	Crystal	1
HCT244	IC	2(1)
Serial Port:*		
MAX239/equiv.	IC	1

* The OakHorizon chip set has built-in support for this peripheral and only requires the additional support logic shown.
(1) Only needed for PS/2 Model 30-286 compatibility.

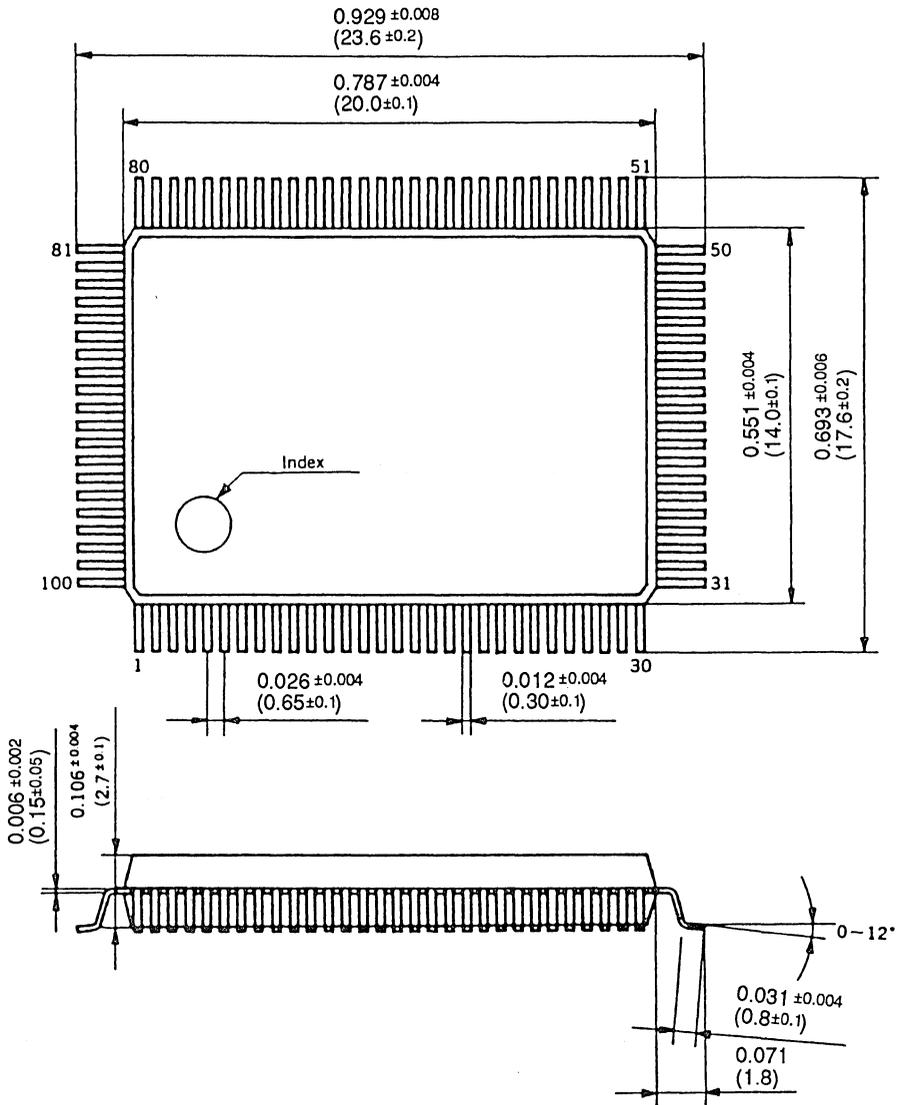# 1.0 BILL OF MATERIAL - DESKTOP SYSTEM

Part Number	Description	Quantity
OakHorizon Chip Set:		
OTI-051	System Support Logic	1
OTI-052	I/O Controller	1
OTI-053	DMA and Memory Controller	1
OTI-054	Address Buffer/Real Time Clock	1
Basic System:		
80286 or 80386SX	CPU	1
8042	Keyboard Controller	1
27C512-200	BIOS EPROM	2
Additional Logic:		
32 MHz	Oscillator	1
14.318 MHz	Oscillator	1
32.768 KHz	Crystal	1
10 MHz	Crystal	1
7406	IC	1
74ALS00	IC	1
74ALS245	IC	5
Memory	DRAM	Depends on system
Graphics:		
OTI-037	Super VGA Controller	1
IMS171	Color Palette	1
74ALS32	IC	1
74ALS244	IC	1
74ALS245	IC	1
TL431	Voltage Regulator	1
Floppy Drive:*		
National/equiv.	Controller/Data Separator	1
24 MHz	Crystal	1
ALS244	IC	2(1)
Serial Port:*		
MAX239/equiv.	IC	1

* The OakHorizon chip set has built-in support for this peripheral and only requires the additional support logic shown.
(1) Only needed for PS/2 Model 30-286 compatibility.

SECTION 9

PACKAGE OUTLINE

100-LEAD PLASTIC FLATPACK

unit: inch
(mm)

100-LEAD PLASTIC FLATPACK

0.929 ±0.008
(23.6 ±0.2)

0.787 ±0.004
(20.0±0.1)

80   51
81   50

Index

100   31
1   30

0.551 ±0.004
(14.0±0.1)

0.693 ±0.006
(17.6±0.2)

0.026 ±0.004
(0.65±0.1)

0.012 ±0.004
(0.30±0.1)

0.006 ±0.002
(0.15±0.05)

0.106 ±0.004
(2.7±0.1)

0 – 12°

0.031 ±0.004
(0.8±0.1)

0.071
(1.8)

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SECTION 10

SALES OFFICES &

REPRESENTATIVES

Oak Technology, Inc.
Corporate Office
139 Kifer Court
Sunnyvale, CA 94086
Telephone: (408) 737-0888
FAX: (408) 737-3838

UNITED STATES
Southern California
VARIGON INC.
21031 Ventura Blvd.
Suite 320
Woodland Hills, CA 91364
Telephone: (818) 594-5080
FAX: (818) 594-5869

MESA COMPONENTS, INC.
7525 Convoy Court
San Diego, CA 92653
Telephone: (714) 855-0233
(213) 634-2116
FAX: (714) 458-0854

Northern California
BROOKS TECHNICAL GROUP
883 N. Shoreline Blvd.
Mountain View, CA 94043
Telephone: (415) 960-3880
FAX: (415) 960-3615

Pacific Northwest
THORSON COMPANY NORTHWEST
12340 Northeast 8th Street Suite 201
Bellevue, WA 98005
Telephone: (206) 455-9180
FAX: (206) 455-9185

6700 S.W. 105th Avenue
Beaverton, OR 97005
Telephone: (503) 644-5900
FAX: (503) 644-5919

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Burlington, MA 01803
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FAX: (617) 272-7068

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67 Gloria Drive
Allendale, NJ 07401
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New York City
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FAX: (718) 851-0935

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FAX: (716) 586-2824

Illinois
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Arlington Heights, IL 60005
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Charlotte, NC 28210
Telephone (704) 523-8822
FAX (704) 527-3222

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Huntsville, AL 35801
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FAX: (205) 881-1182

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Mobile, AL 36606
Telephone: (205) 478-1036
FAX: (205) 476-4718

6855 Jimmy Carter Blvd. Suite 2440
Norcoss, GA 30071
Telephone: (404) 449-8680
FAX: (404) 447-1046

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Florida
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Clearwater, FL 34615
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FAX: (813) 443-6312

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Tamarac, FL 33319
Telephone: (305) 722-9369
FAX: (305) 726-4139

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Sanford, FL 32773
Telephone: (407) 330-0529
FAX: (407) 330-0563

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8350 Meadow Road, Suite 174
Dallas, TX 75231
Telephone: (214) 750-6082

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Suite 206
Houston, TX 77036
Telephone: (713) 988-6082
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Vancouver
Telephone: (604) 222-1645

EUROPE
France
NEWTEK
8 rue de l' Esterel, Silil 583
94663 Rungis Cedex
France
Telephone: (1) 46 87 22 00
FAX: (1) 46 87 80 49

4, rue de l'Europe
ZAC Font-Ratel
38640 CLAIX
France
Telephone: 76 98 56 01
FAX: 76 98 16 04

United Kingdom
ABACUS ELECTRONICS LTD.
Abacus House, Bone Lane
Newbury, Berks RG14 5SF
United Kingdom
Telephone: 0635 33311
FAX: 0635 38670

West Germany
TEKELEC AIRTRONIC GMBH
Kapuzinerstr. 9
8000 Munich 2
West Germany
Telephone: 089 5164 0
FAX: 089 516410

The Netherlands
TEKELEC AIRTRONIC B.V.
Postbus 63, 2700AB
Zoetermeer
The Netherlands
Telephone: 079-310100
FAX: 079-417504

FAR EAST
Taiwan
OAK TECHNOLOGY, INC.
TAIWAN
Room B, 7F, No. 370
Sec. 1, Fu Hsing S. Road
Taipei, Taiwan R.O.C.
Telephone: 886-2-784-9123
FAX: 886-2-706-7641

ARTISTEX INTERNATIONAL INC.
B2, 11th FL., NO. 126
Nan King E. Road, Sec. 4
Taipei, Taiwan 10568 R.O.C.

Japan
KANEMATSU SEMICONDUCTOR
CORP.
6-1, 1-Chome
Shintomi, Chou-ku
Tokyo, 104 Japan
Telephone: (813) 551 7791
FAX: (813) 551 7889

Hong Kong
GREAT CHINA COMPUTERS LMTD.
628B Ocean Center
Canton Road
Kowloon, Hong Kong
Telephone: 3-7302976
FAX: 852-3-7398690
Telex: 47590 GCCLHX
CABLE: DACHONGHWA

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