



ATWINC3400-MR210CA

IEEE 802.11 b/g/n Network Controller Module with Integrated Bluetooth Low Energy 4.0

Introduction

The ATWINC3400-MR210CA is an IEEE 802.11 b/g/n RF/Baseband/Medium Access Control (MAC) network controller module with Bluetooth Low Energy technology that is compliant with Bluetooth version 4.0. This module is optimized for low power and high performance mobile applications. This module features small form factor when integrating Power Amplifier (PA), Low-Noise Amplifier (LNA), Transmit/Receive (T/R) switch (for Wi-Fi and Bluetooth), Power Management Unit (PMU), and Chip Antenna. The ATWINC3400-MR210CA module requires a 32.768 kHz clock for Sleep operation.

The ATWINC3400-MR210CA module utilizes highly optimized IEEE 802.11 Bluetooth coexistence protocols, and provides Serial Peripheral Interface (SPI) to interface with the host controller.

Features

Wi-Fi features:

- IEEE 802.11 b/g/n RF/PHY/MAC
- IEEE 802.11 b/g/n (1x1) with single spatial stream, up to 72 Mbps PHY rate in 2.4 GHz ISM band
- Integrated chip antenna
- Superior sensitivity and range via advanced PHY signal processing
- Advanced equalization and channel estimation
- Advanced carrier and timing synchronization
- Supports Soft-AP
- Supports IEEE 802.11 WEP, WPA, and WPA2
- Superior MAC throughput through hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgment
- On-chip memory management engine to reduce the host load
- Operating temperature range from -40°C to +85°C
- Wi-Fi Alliance® certified for connectivity and optimizations
 - ID: [WFA62065](#)
- Integrated on-chip microcontroller
- SPI host interface
- Integrated Flash memory for Wi-Fi and Bluetooth system software
- Low leakage on-chip memory for state variables
- Fast AP re-association (150 ms)
- On-chip network stack to offload MCU
 - Integrated network IP stack to minimize the host CPU requirements
- Network features: Firmware version 1:2:x

- TCP, UDP, DHCP, ARP, HTTP, SSL, DNS, and SNTP

Bluetooth features:

- Bluetooth 4.0 (Bluetooth Low Energy) certifications
 - Controller QD ID - [77870](#)
 - Host QD ID - [77451](#)
- Class 2 transmission
- Adaptive Frequency Hopping (AFH)
- Superior sensitivity and range

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1. Ordering Information and Module Marking

The following table provides the ordering details for the ATWINC3400-MR210CA module.

Table 1-1. Ordering Details

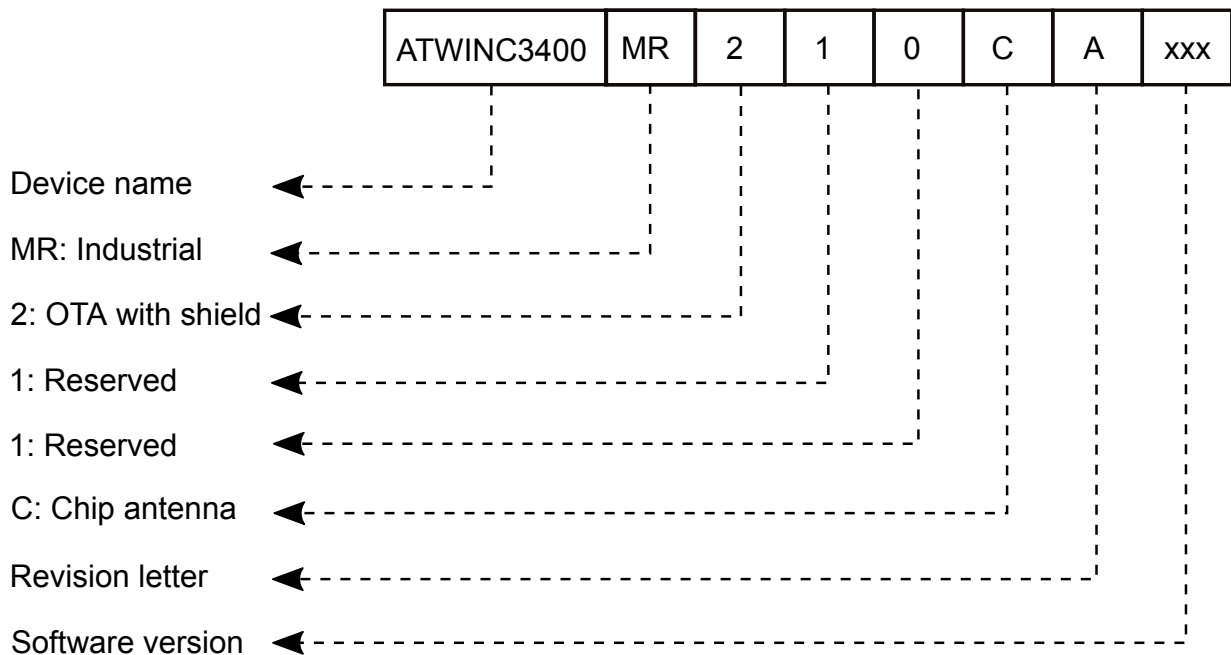
Model Number	Ordering Code	Package	Description	Regulatory Information
ATWINC3400-MR210CA	ATWINC3400-MR210CAxxx ¹	22.43 x 14.73 x 2.0 mm	Certified module with chip antenna	FCC, IC, CE ²

Note:

1. 'xxx' in the preceding table and following figure denotes the software version. Order code changes as per the software version. For example, current version of the software is v1.22, so its equivalent order code is ATWINC3400-MR210CA122.
2. CE certification pending.

The following figure illustrates the ATWINC3400-MR210CA module marking information.

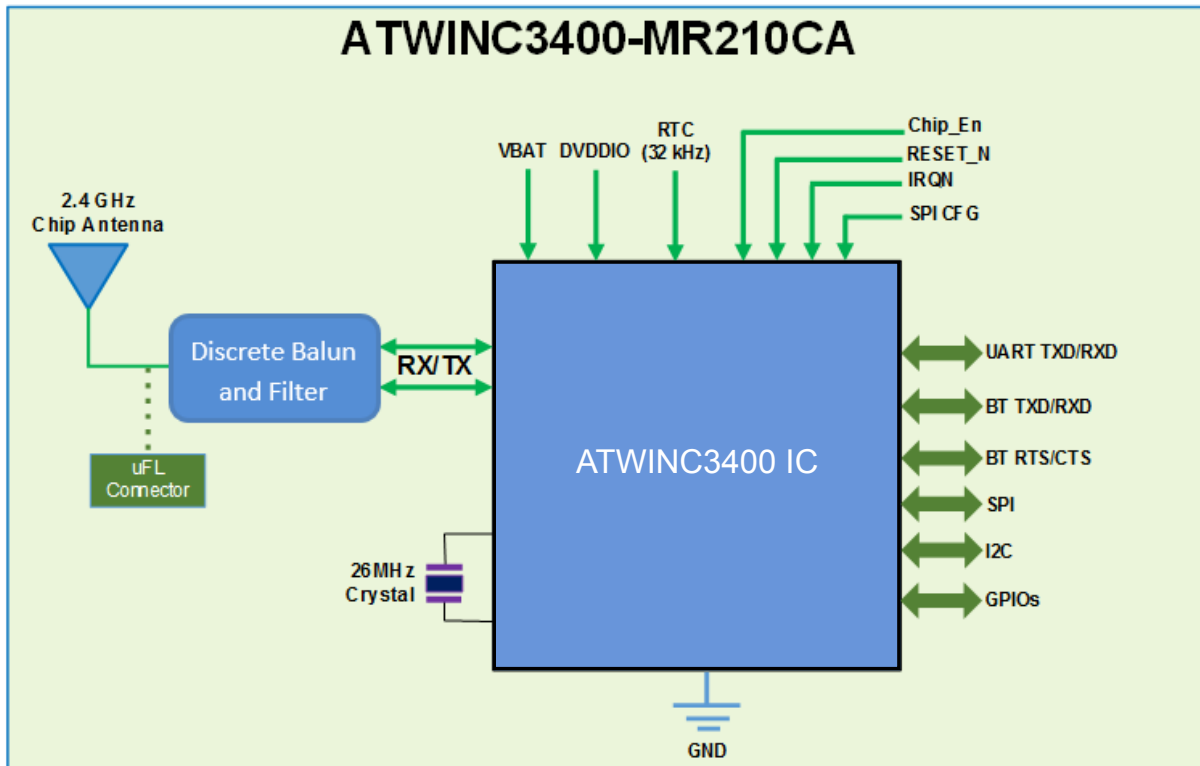
Figure 1-1. Marking Information



2. Block Diagram

The following figure shows the block diagram of the ATWINC3400-MR210CA module.

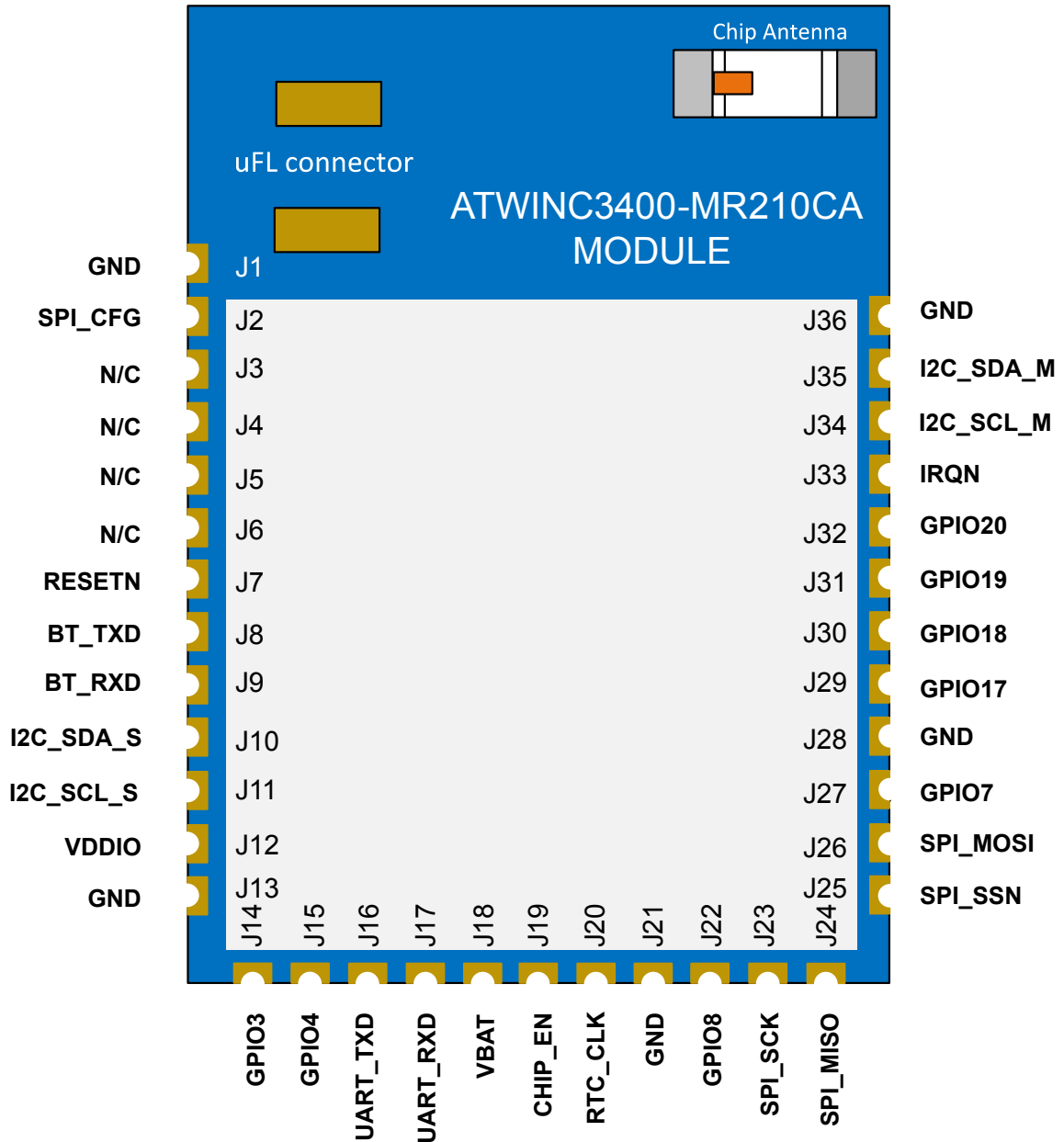
Figure 2-1. ATWINC3400-MR210CA Module Block Diagram



3. Pinout and Package Information

This package contains an exposed paddle that must be connected to the system board ground. The ATWINC3400-MR210CA module pin assignment is shown in following figure.

Figure 3-1. ATWINC3400-MR210CA Module Pin Assignment



The following table provides the ATWINC3400-MR210CA module pin description.

Table 3-1. ATWINC3400-MR210CA Module Pin Description

Pin #	Pin Name	Pin Type	Description
1	GND	GND	Ground pin.
2	SPI_CFG	Digital Input	Serial Peripheral Interface pin, which must be tied to VDDIO.
3	NC	-	No connection.
4	NC	-	No connection.
5	NC	-	No connection.
6	NC	-	No connection.
7	RESETN	Digital Input	<ul style="list-style-type: none"> Active-low hard Reset pin. When the Reset pin is asserted low, the module is in the Reset state. When the Reset pin is asserted high, the module functions normally. This pin must connect to a host output that is low by default on power-up. If the host output is tri-stated, add a 1 MOhm pull down resistor to ensure a low level at power-up.
8	BT_TXD	Digital I/O, Programmable pull up	Bluetooth UART transmit data output pin.
9	BT_RXD	Digital I/O, Programmable pull up	Bluetooth UART receive data input pin.
10	I2C_SDA_S	Digital I/O, Programmable pull up	<ul style="list-style-type: none"> I2C Slave data pin. Used only for debug development purposes. It is recommended to add a test point for this pin. I2C is the default configuration. <TBD>
11	I2C_SCL_S	Digital I/O, Programmable pull up	<ul style="list-style-type: none"> I2C Slave clock pin. Used only for debug development purposes. It is recommended to add a test point for this pin. I2C is the default configuration. <TBD>
12	VDDIO	Power	Digital I/O power supply.
13	GND	GND	Ground pin.
14	GPIO3	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
15	GPIO4	Digital I/O, Programmable pull up	General Purpose Input/Output pin.

Pin #	Pin Name	Pin Type	Description
16	UART_TXD	Digital I/O, Programmable pull up	<ul style="list-style-type: none"> • Wi-Fi UART TxD output pin. • Used only for debug development purposes. It is recommended to add a test point for this pin.
17	UART_RXD	Digital I/O, Programmable pull up	<ul style="list-style-type: none"> • Wi-Fi UART RxD input pin. • Used only for debug development purposes. It is recommended to add a test point for this pin.
18	VBAT	Power	Power supply pin for DC/DC converter and PA.
19	CHIP_EN	Digital Input	<ul style="list-style-type: none"> • PMU enable pin. • When the CHIP_EN pin is asserted high, the module is enabled. When the CHIP_EN pin is asserted low, the module is disabled or put into Power-Down mode. • Connect to a host output that is low by default at power-up. If the host output is tri-stated, add a 1 MOhm pull down resistor if necessary to ensure a low level at power-up.
20	RTC_CLK	Digital I/O, Programmable pull up	<ul style="list-style-type: none"> • RTC Clock input pin. • This pin must connect to a 32.768 kHz clock source.
21	GND	GND	Ground pin.
22	GPIO8	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
23	SPI_SCK	Digital I/O, Programmable pull up	SPI clock pin.
24	SPI_MISO	Digital I/O, Programmable pull up	SPI MISO (Master In Slave Out) pin.
25	SPI_SSN	Digital I/O, Programmable pull up	Active-low SPI SSN (Slave Select) pin.
26	SPI_MOSI	Digital I/O, Programmable pull up	SPI MOSI (Master Out Slave In) pin.
27	GPIO7	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
28	GND	GND	Ground pin.
29	GPIO17	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
30	GPIO18	Digital I/O, Programmable pull up	General Purpose Input/Output pin.

Pin #	Pin Name	Pin Type	Description
31	GPIO19	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
32	GPIO20	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
33	IRQN	Digital output, Programmable pull up	<ul style="list-style-type: none"> ATWINC3400-MR210CA module host interrupt request output pin. This pin must connect to a host interrupt pin.
34	I2C_SCL_M	Digital I/O, Programmable pull up	I2C Master clock pin.
35	I2C_SDA_M	Digital I/O, Programmable pull up	I2C Master data pin.
36	GND	GND	Ground pin.
37	PADDLE VSS	Power	Connect to system board ground.

3.1 Package Description

The following table provides the ATWINC3400-MR210CA module package dimensions.

Table 3-2. ATWINC3400-MR210CA Module Package Information

Parameter	Value	Unit
Pad count	36	-
Package size	22.43 x 14.73	mm
Total thickness	2.09	
Pad pitch	1.20	
Pad width	0.81	
Exposed pad size	4.4 x 4.4	

4. Electrical Characteristics

This chapter provides an overview of the electrical characteristics of the ATWINC3400-MR210CA module.

4.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings for the ATWINC3400-MR210CA module.

Table 4-1. ATWINC3400-MR210CA Module Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
VDDIO	I/O supply voltage	-0.3	5.0	V
VBAT	Battery supply voltage	-0.3	5.0	
V _{IN}	Digital input voltage	-0.3	VDDIO	
V _{AIN}	Analog input voltage	-0.3	1.5	
V _{ESDHBM}	Electrostatic discharge Human Body Model (HBM)	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
T _A	Storage temperature	-65	150	°C
-	Junction temperature	-	125	
-	RF input power	-	23	dBm

1. V_{IN} corresponds to all the digital pins.
2. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
 - 2.1. The Class 1 pins include all the pins (both analog and digital).
 - 2.2. The Class 2 pins include all digital pins only.
 - 2.3. V_{ESDHBM} is ±1 kV for Class 1 pins. V_{ESDHBM} is ± 2 kV for Class 2 pins.



Caution: Stresses beyond those listed under “Absolute Maximum Ratings” cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods affects the device reliability.

4.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for the ATWINC3400-MR210CA module.

Table 4-2. ATWINC3400-MR210CA Module Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDDIO	I/O supply voltage ⁽¹⁾	2.7	3.3	3.6	V
VBAT	Battery supply voltage ⁽²⁾⁽³⁾	3.0	3.6	4.2	V
-	Operating temperature	-40	-	85	°C

Note:

1. I/O supply voltage is applied to the VDDIO pin.
2. Battery supply voltage is applied to the VBAT pin.
3. The ATWINC3400-MR210CA module is functional across this range of voltages; however, optimal RF performance is guaranteed for VBAT in the range $\geq 3.0V$ VBAT $\leq 4.2V$.

4.3 DC Characteristics

The following table provides the DC characteristics for the ATWINC3400-MR210CA module digital pads.

Table 4-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V _{IL}	Input Low Voltage	-0.30	-	0.60	V
V _{IH}	Input High Voltage	VDDIO-0.60	-	VDDIO+0.30	
V _{OL}	Output Low Voltage	-	-	0.45	
V _{OH}	Output High Voltage	VDDIO-0.50	-	-	
-	Output Load Capacitance	-	-	20	pF
-	Digital Input Load Capacitance	-	-	6	

4.4 IEEE 802.11 b/g/n Radio Performance

4.4.1 Receiver Performance

The receiver performance is tested under following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C
- Measured after RF matching network

The following table provides the receiver performance characteristics for the ATWINC3400-MR210CA module.

Table 4-4. IEEE 802.11 Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412	-	2,472	MHz
Sensitivity 802.11b	1 Mbps DSSS	-	-95.0	-	dBm
	2 Mbps DSSS	-	-93.5	-	
	5.5 Mbps DSSS	-	-90.0	-	
	11 Mbps DSSS	-	-86.0	-	
Sensitivity 802.11g	6 Mbps OFDM	-	-90.0	-	dBm
	9 Mbps OFDM	-	-88.5	-	
	12 Mbps OFDM	-	-86.0	-	
	18 Mbps OFDM	-	-84.5	-	
	24 Mbps OFDM	-	-82.0	-	
	36 Mbps OFDM	-	-78.5	-	
	48 Mbps OFDM	-	-74.5	-	
	54 Mbps OFDM	-	-73.0	-	
Sensitivity 802.11n (BW=20 MHz, 800ns GI)	MCS 0	-	-89.0	-	dBm
	MCS 1	-	-87.0	-	
	MCS 2	-	-84.0	-	
	MCS 3	-	-81.5	-	
	MCS 4	-	-78.0	-	
	MCS 5	-	-74.0	-	
	MCS 6	-	-72.0	-	
	MCS 7	-	-70.0	-	
Maximum receive signal level	1-11 Mbps DSSS	-	0	-	dBm
	6-54 Mbps OFDM	-	0	-	
	MCS 0 - 7 (800ns GI)	-	0	-	
Adjacent channel rejection	1 Mbps DSSS (30 MHz offset)	-	50	-	dB
	11 Mbps DSSS (25 MHz offset)	-	43	-	
	6 Mbps OFDM (25 MHz offset)	-	40	-	
	54 Mbps OFDM (25 MHz offset)	-	25	-	
	MCS 0 – 20 MHz BW (25 MHz offset)	-	40	-	
	MCS 7 – 20 MHz BW (25 MHz offset)	-	20	-	

4.4.2 Transmitter Performance

The transmitter performance is tested under following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C

The following table provides the transmitter performance characteristics for the ATWINC3400-MR210CA module.

Table 4-5. IEEE 802.11 Transmitter Performance Characteristics

Parameter	Description	Minimum	Typical	Max.	Unit
Frequency	-	2,412	-	2,472	MHz
Output power	802.11b 1 Mbps	-	16.7 ⁽¹⁾	-	dBm
	802.11b 11 Mbps	-	17.5 ⁽¹⁾	-	
	802.11g OFDM 6 Mbps	-	18.3 ⁽¹⁾	-	
	802.11g OFDM 54 Mbps	-	13.0 ⁽¹⁾	-	
	802.11n HT20 MCS 0 (800ns GI)	-	17.5 ⁽¹⁾	-	
	802.11n HT20 MCS 7 (800ns GI)	-	12.5 ⁽¹⁾	-	
Tx power accuracy	-	-	±1.5 ⁽²⁾	-	dB
Carrier suppression	-	-	30.0	-	dBc
Harmonic output power (Radiated, Regulatory mode)	2 nd	-	-	-41	dBm/MHz
	3 rd	-	-	-41	

Note:

1. Measured at IEEE 802.11 specification compliant EVM/Spectral mask.
2. Measured after RF matching network.
3. Operating temperature range is -40°C to +85°C. RF performance guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. With respect to Tx power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
5. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.

4.5 Bluetooth Radio Performance

4.5.1 Receiver Performance

The receiver performance is tested under following conditions:

- VBAT = 3.3V

- VDDIO = 3.3V
- Temp: 25°C
- Measured after RF matching network.

The following table provides the Bluetooth receiver performance characteristics for the ATWINC3400-MR210CA module.

Table 4-6. Bluetooth Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,402	-	2,480	MHz
Sensitivity (ideal Tx)	Bluetooth Low Energy (GFSK)	-	-92.5	-	dBm
Maximum receive signal level	Bluetooth Low Energy (GFSK)	-	-3.5	-	
Interference performance (Bluetooth Low Energy)	Co-channel	-	12	-	dB
	adjacent + 1 MHz	-	0	-	
	adjacent - 1 MHz	-	3	-	
	adjacent + 2 MHz(image frequency)	-	-25	-	
	adjacent - 2 MHz	-	-41	-	
	adjacent + 3 MHz (adjacent to image)	-	-35	-	
	adjacent - 3 MHz	-	-35	-	
	adjacent + 4 MHz	-	-45	-	
	adjacent - 4 MHz	-	-30	-	
	adjacent +5 MHz	-	-34	-	
	adjacent - 5 MHz	-	-30	-	

4.5.2 Transmitter Performance

The transmitter performance is tested under following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp: 25°C
- Measured after RF matching network.

The following table provides the Bluetooth transmitter performance characteristics for the ATWINC3400-MR210CA module.

Table 4-7. Bluetooth Transmitter Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,402	-	2,480	MHz
Output power	Bluetooth Low Energy (GFSK)	-	3.2	3.7	dBm

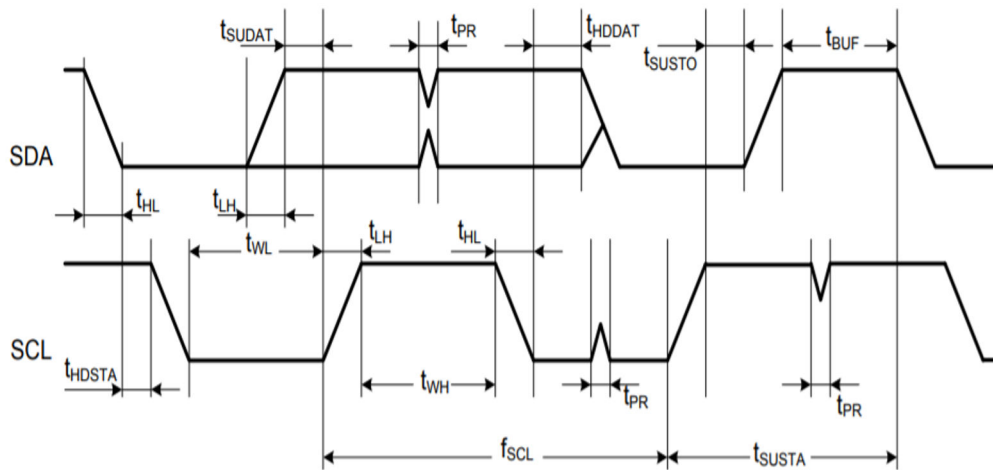
Parameter	Description	Min.	Typ.	Max.	Unit
In-band spurious emission (Bluetooth Low Energy)	N+2 (Image frequency)	-	-33	-	
	N + 3 (Adjacent to image frequency)	-	-32	-	
	N-2	-	-50	-	
	N-3	-	-49	-	

4.6 Timing Characteristics

4.6.1 I²C Slave Timing

The I²C Slave timing diagram for the ATWINC3400-MR210CA module is shown in the following figure.

Figure 4-1. I²C Slave Timing Diagram



The following table provides the I²C Slave timing parameters for the ATWINC3400-MR210CA module.

Table 4-8. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	-
SCL Low Pulse Width	t_{WL}	1.3	-	μ s	-
SCL High Pulse Width	t_{WH}	0.6	-		-
SCL, SDA Fall Time	t_{HL}	-	300	ns	-
SCL, SDA Rise Time	t_{LH}	-	300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6	-	μ s	-
START Hold Time	t_{HDSTA}	0.6	-		-
SDA Setup Time	t_{SUDAT}	100	-	ns	-
SDA Hold Time	t_{HDDAT}	0	-	ns	Slave and Master Default

Parameter	Symbol	Min.	Max.	Units	Remarks
		40	-	μs	Master Programming Option
STOP Setup Time	t_{SUSTO}	0.6	-	μs	-
Bus Free Time Between STOP and START	t_{BUF}	1.3	-		-
Glitch Pulse Reject	t_{PR}	0	50	ns	-

4.6.2 SPI Slave Timing

The SPI Slave timing for the ATWINC3400-MR210CA module is provided in the following figures.

Figure 4-2. SPI Slave Clock Polarity and Clock Phase Timing

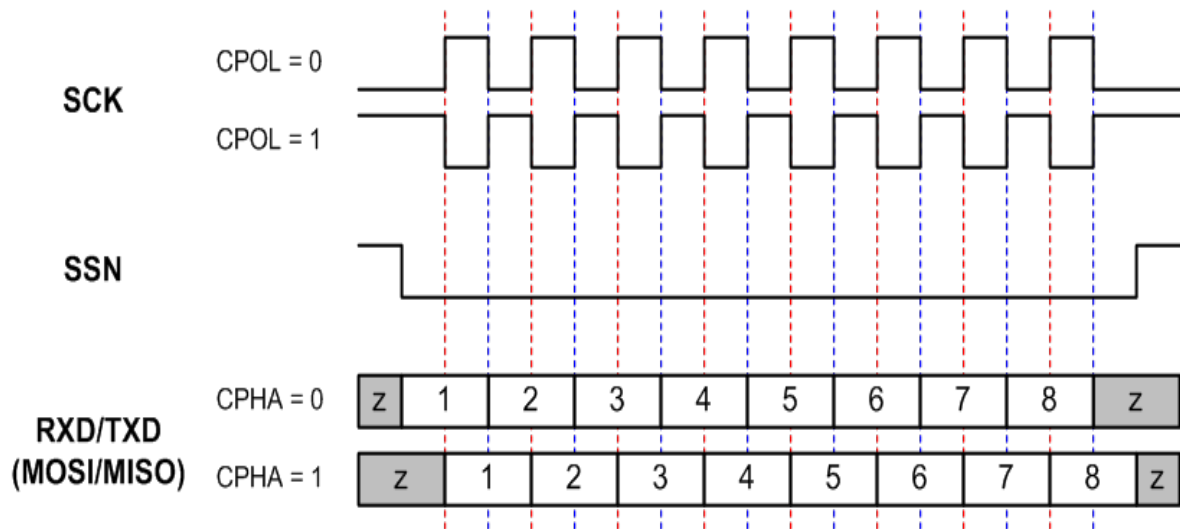
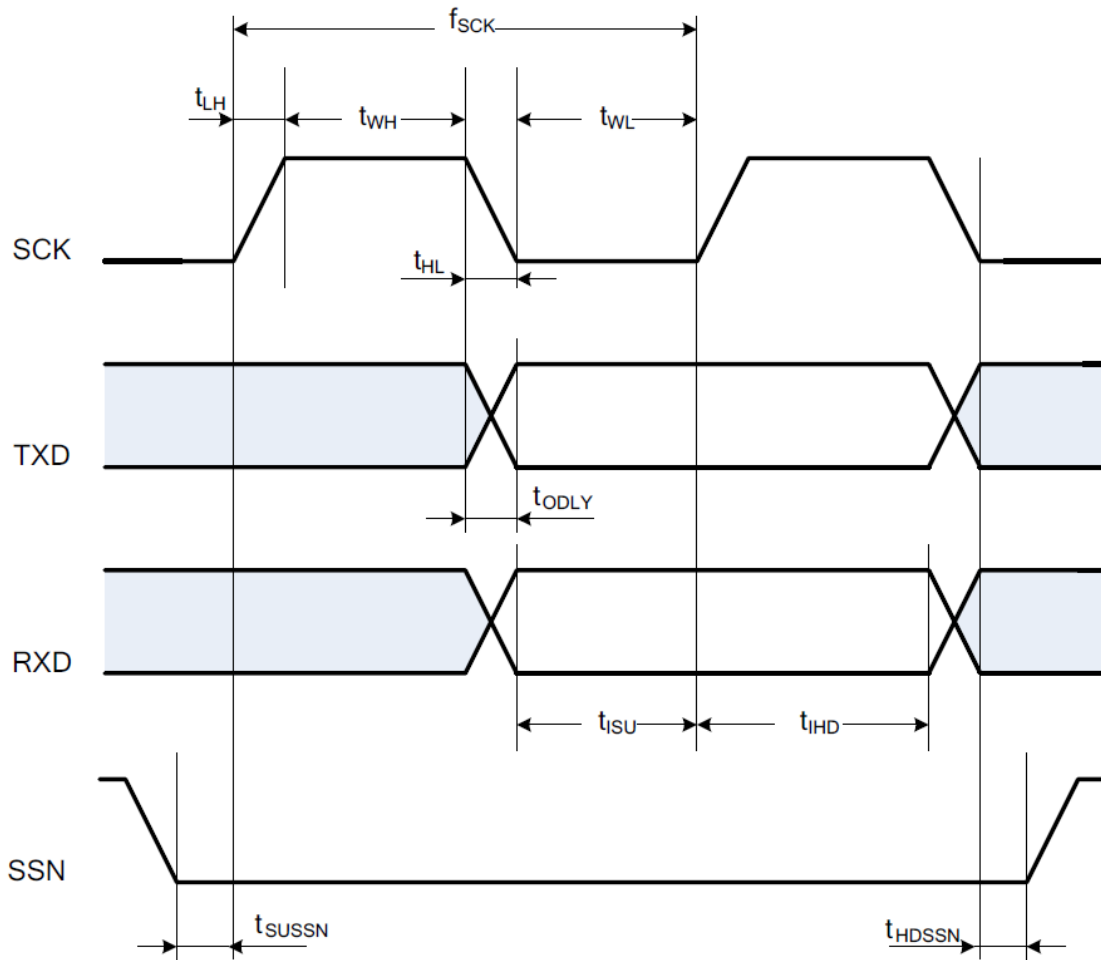


Figure 4-3. SPI Slave Timing Diagram



The following table provides the SPI Slave timing parameters for the ATWINC3400-MR210CA module.

Table 4-9. SPI Slave Timing Parameters ⁽¹⁾

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency ⁽²⁾	f_{SCK}	-	48	MHz
Clock Low Pulse Width	t_{WL}	6	-	ns
Clock High Pulse Width	t_{WH}	4	-	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay ⁽³⁾	t_{ODLY}	3	9 from SCK fall 11 from SCK rise	
RXD Input Setup Time	t_{ISU}	3	-	
RXD Input Hold Time	t_{IHD}	5	-	

Parameter	Symbol	Min.	Max.	Unit
SSN Input Setup Time	t_{SUSN}	5	-	
SSN Input Hold Time	t_{HDSSN}	5	-	

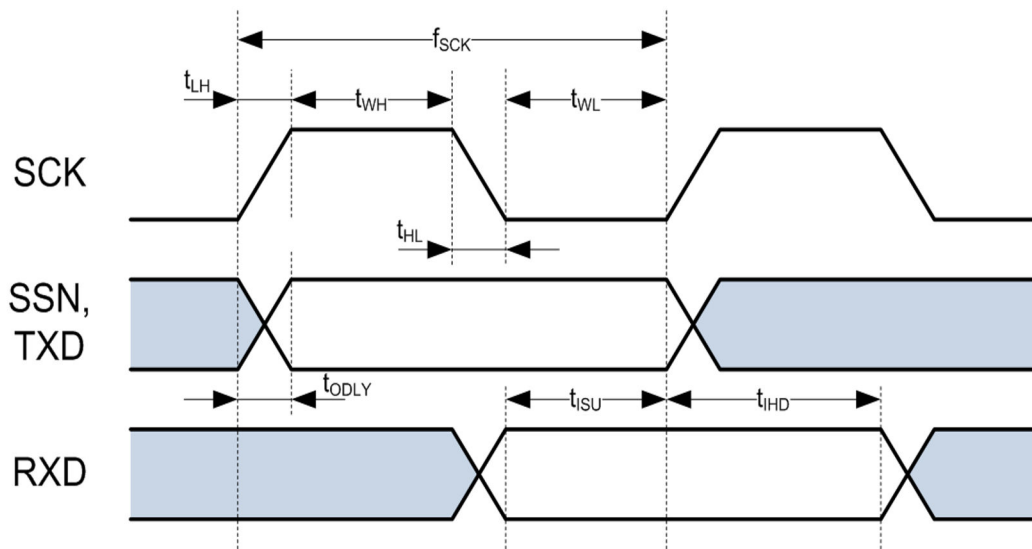
Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15 pF output loading.

4.6.3 SPI Master Timing

The SPI Master timing for the ATWINC3400-MR210CA module is shown in the following figure.

Figure 4-4. SPI Master Timing Diagram



The following table provides the SPI Master timing parameters for the ATWINC3400-MR210CA module .

Table 4-10. SPI Master Timing Parameters ⁽¹⁾

Parameter	Symbol	Min.	Max.	Unit
Clock Output Frequency ⁽²⁾	f_{SCK}	-	20	MHz
Clock Low Pulse Width	t_{WL}	19	-	ns
Clock High Pulse Width	t_{WH}	21	-	
Clock Rise Time ⁽³⁾	t_{LH}	-	11	
Clock Fall Time ⁽³⁾	t_{HL}	-	10	
RXD Input Setup Time	t_{ISU}	24	-	
RXD Input Hold Time	t_{IHD}	0	-	
SSN/TXD Output Delay ⁽³⁾	t_{ODLY}	-5	3	

Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Master interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15 pF output loading.

5. Power Management

5.1 Device States

The ATWINC3400-MR210CA module has multiple device states, based on the state of the IEEE 802.11 and Bluetooth subsystems. It is possible for both subsystems to be active at the same time. To simplify the device power consumption breakdown, the following basic states are defined. One subsystem can be active at a time:

- WiFi_ON_Transmit – Device actively transmits IEEE 802.11 signal
- WiFi_ON_Receive – Device actively receives IEEE 802.11 signal
- BT_ON_Transmit – Device actively transmits Bluetooth signal
- BT_ON_Receive – Device actively receives Bluetooth signal
- Doze – Device is powered on but it does not actively transmit or receive data
- Power_Down – Device core supply is powered off

5.2 Controlling Device States

The following table shows different device states and its power consumption. The device states can be switched using the following:

- CHIP_EN – Module pin (pin 19) enables or disables the DC/DC converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power-down sequence mentioned in [Figure 5-1](#). When VDDIO is OFF and CHIP_EN is low, the chip is powered off with no leakage.

Table 5-1. ATWINC3400-MR210CA Device States Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption ⁽¹⁾	
			I _{VBAT}	I _{VDDIO}
ON_WiFi_Transmit	802.11b 1 Mbps	16.7	271 mA	24 mA
	802.11b 11 Mbps	17.5	265 mA	24 mA
	802.11g 6 Mbps	18.3	275 mA	24 mA
	802.11g 54 Mbps	13.0	235 mA	24 mA
	802.11n MCS 0	17.5	272 mA	24 mA
	802.11n MCS 7	12.5	232 mA	24 mA
ON_WiFi_Receive	802.11b 1 Mbps	N/A	63.9 mA	23.7 mA
	802.11b 11 Mbps	N/A	63.9 mA	23.7 mA
	802.11g 6 Mbps	N/A	63.9 mA	23.7 mA
	802.11g 54 Mbps	N/A	63.9 mA	23.7 mA
	802.11n MCS 0	N/A	63.9 mA	23.7 mA

Device State	Code Rate	Output Power (dBm)	Current Consumption ⁽¹⁾	
			I _{VBAT}	I _{VDDIO}
	802.11n MCS 7	N/A	63.9 mA	23.7 mA
ON_BT_Transmit (@3.2 dBm Pout)	BLE 4.0 1 Mbps	1.5	79.37 mA	23.68 mA
ON_BT_Receive	BLE 4.0 1 Mbps	N/A	51.36 mA	23.68 mA
Doze (Bluetooth Low Energy Idle)	N/A	N/A	53 mA ⁽²⁾	
Doze (Bluetooth Low Energy Low Power)	N/A	N/A	1 mA ⁽²⁾	
Power_Down	N/A	N/A	10.5 μ A ⁽²⁾	

Note:

1. Conditions: VBAT = 3.3V, VDDIO = 3.3V, at 25°C.
2. Current consumption mentioned for these states is the sum of current consumed in VDDIO and VBAT voltage rails.

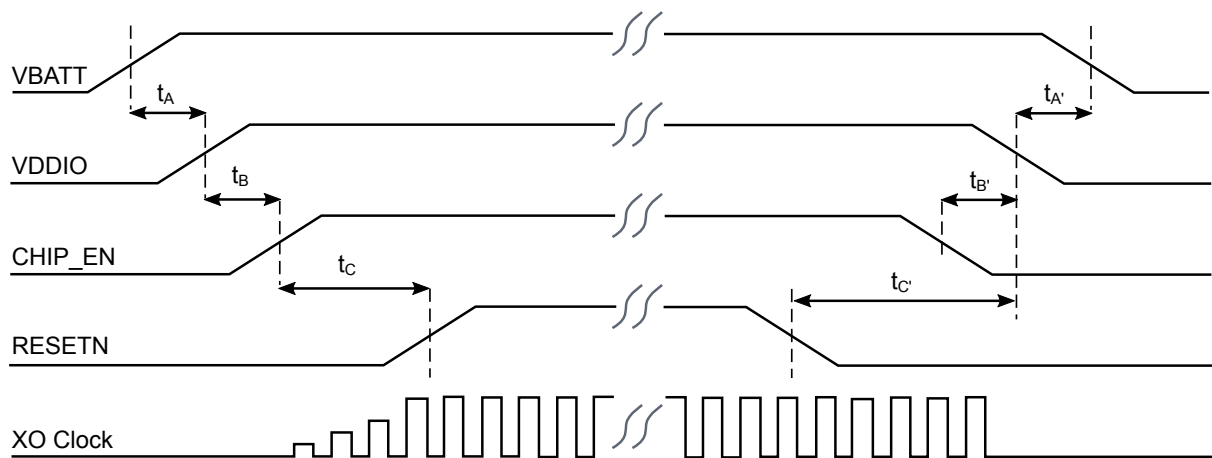
When power is not supplied to the device (DC/DC converter output and VDDIO are OFF, at ground potential), voltage cannot be applied to the ATWINC3400-MR210CA module pins because each pin contains an ESD diode from the pin to supply. This diode turns on when voltage higher than one diode-drop is supplied to the pin.

If voltage must be applied to the signal pads when the chip is in a low-power state, the VDDIO supply must be ON, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning ON, do not apply voltage that is more than one diode-drop below the ground to any pin.

5.3 Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWINC3400-MR210CA module.

Figure 5-1. Power-Up/Down Sequence



The following table provides power-up/down sequence timing parameters.

Table 5-2. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t _A	0	-	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.
t _B	0	-	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t _C	5	-	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
t _{A'}	0	-	ms	VDDIO fall to VBAT fall	VBAT and VDDIO fall simultaneously or connected together. VBAT must not fall before VDDIO.
t _{B'}	0	-	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
t _{C'}	0	-	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

5.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 5-3. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96 kOhm)
Power_Down: core supply OFF	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply and hard reset ON	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply ON, device out of reset and not programmed	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply ON, device programmed by firmware	High	High	High	Programmed by firmware for each pin: enabled or disabled	Opposite of Output Driver state	Programmed by firmware for each pin: enabled or disabled

6. Clocking

6.1 Low-Power Clock

The ATWINC3400-MR210CA module requires an external 32.768 kHz clock to be supplied at the module pin 20. This clock is used during the sleep operation. The frequency accuracy of this external clock must be within ± 200 ppm.

7. CPU and Memory Subsystem

7.1 Processor

The ATWINC3400-MR210CA module has two Cortus APS3 32-bit processors, one is used for Wi-Fi and the other is used for Bluetooth. In IEEE 802.11 mode, the processor performs many of the MAC functions, including but not limited to: association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as Station (STA) and Access Point (AP) modes. In Bluetooth mode, the processor handles multiple tasks of the Bluetooth protocol stack.

7.2 Memory Subsystem

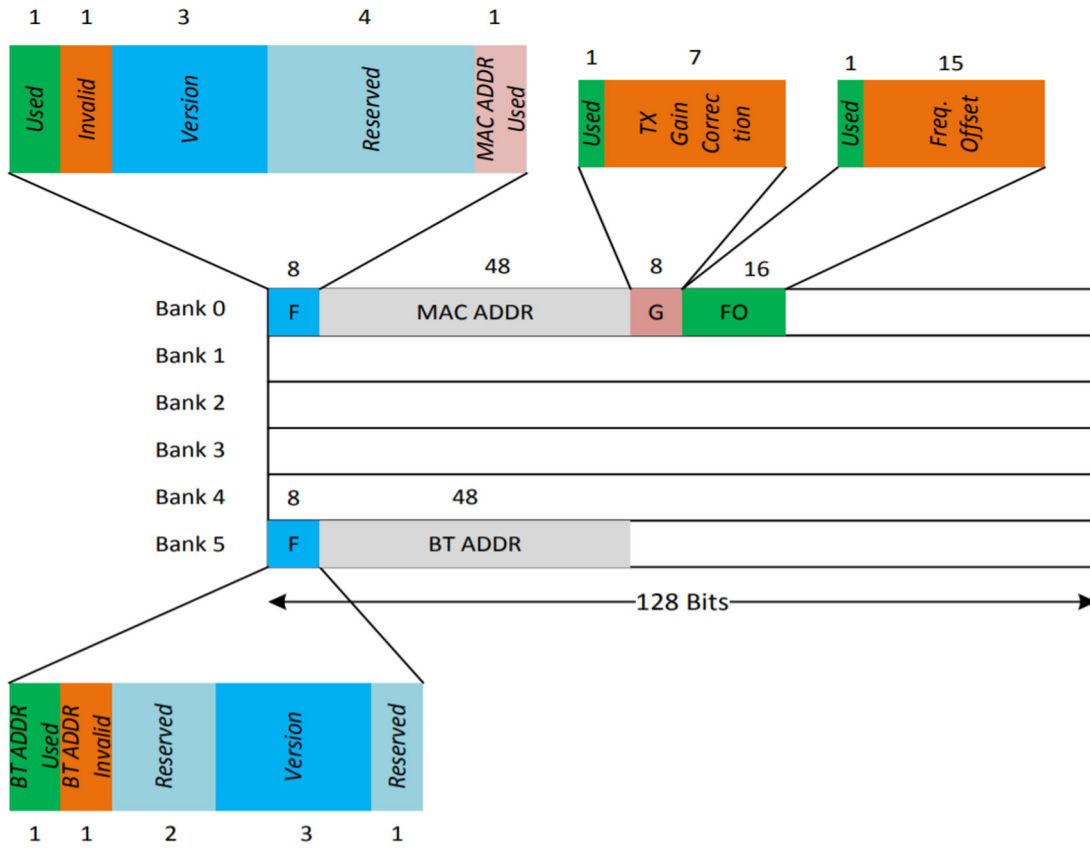
The APS3 core uses a 256 KB instruction/boot ROM (160 KB for IEEE 802.11 and 96 KB for Bluetooth) along with a 420 KB instruction RAM (128 KB for IEEE 802.11 and 292 KB for Bluetooth), and a 128 KB data RAM (64 KB for IEEE 802.11 and 64 KB for Bluetooth). In addition, the device uses a 160 KB shared/exchange RAM (128 KB for IEEE 802.11 and 32 KB for Bluetooth), accessible by the processor and MAC, which allows the processor to perform various data management tasks on the Tx and Rx data packets.

7.3 Nonvolatile Memory

The ATWINC3400-MR210CA module has 768 bits of nonvolatile eFuse memory that can be read by the CPU after device reset. This nonvolatile One-Time-Programmable (OTP) memory can be used to store customer-specific parameters, such as 802.11 MAC address and Bluetooth address; various calibration information such as Tx power, crystal frequency offset, and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. The bit map of the first and last banks is shown in the following figure. The purpose of the first 80 bits in bank 0 and the first 56 bits in bank 5 is fixed, and the remaining bits are general-purpose software dependent bits, reserved for future use. Currently, the Bluetooth address is derived from the Wi-Fi MAC address ($BT_ADDR=MAC_ADDR+1$). This eliminates the need to program the first 56 bits in bank 5. Since each bank and each bit can be programmed independently, this allows for several updates of the device parameters following the initial programming. For example, if the MAC address has to be changed, Bank 1 has to be programmed with the new MAC address along with the values of Tx gain correction and frequency offset if they are used and programmed in the Bank 0. The contents of Bank 0 have to be invalidated in this case by programming the Invalid bit in the Bank 0. This will allow the firmware to use the MAC address from Bank 1.

By default, ATWINC3400-MR210CA modules are programmed with the MAC address and the frequency offset bits of Bank 0.

Figure 7-1. ATWINC3400-MR210CA eFuse Bit Map



8. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY), and the radio.

8.1 MAC

The ATWINC3400-MR210CA module is designed to operate at low power, while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, and WPA2 CCMP-AES security requirements.

Control functions, which have real time requirements, are implemented using hardwired control logic modules. These logic modules offer real time response while maintaining configurability through the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon Tx control, interframe spacing, and so on), protocol timer module (responsible for the Network Access vector, back-off timing, timing synchronization function, and slot management), MAC Protocol Data Unit (MPDU) handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication), and Tx/Rx control Finite State Machine (FSM) (coordinates data movement between PHY and MAC interface, cipher engine, and the Direct Memory Access (DMA) interface to the Tx/Rx FIFOs).

The following are the characteristics of MAC functions implemented solely in software on the microprocessor:

- Functions with high memory requirements or complex data structures. Examples include association table management and power save queuing.
- Functions with low computational load or without critical real time requirements. Examples include authentication and association.
- Functions that require flexibility and upgradeability. Examples include beacon frame processing and QoS scheduling.

Features

The ATWINC3400-MR210CA MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/HCCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
 - Transmission and reception of aggregated MPDUs (A-MPDU)
 - Transmission and reception of aggregated MSDUs (A-MSDU)
 - Immediate block acknowledgment
 - Reduced Interframe Spacing (RIFS)
- IEEE 802.11i and WPA security with key management:

- WEP 64/128
- WPA-TKIP
- 128-bit WPA2 CCMP (AES)
- Advanced power management:
 - Standard IEEE 802.11 power save mode
- RTS-CTS and CTS-self support
- Either STA or AP mode in the infrastructure basic service set mode

8.2 PHY

The ATWINC3400-MR210CA module WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20 MHz bandwidth. The advanced algorithms are used to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as Fast Fourier Transform (FFT), filtering, Forward Error Correction (FEC) that is a Viterbi decoder, frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

Features

The IEEE 802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20 MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11 Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48, and 54 Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20 MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps
- IEEE 802.11n mixed mode operation
- Per packet Tx power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery and frame detection

8.3 Radio

This section presents information describing the properties and characteristics of the ATWINC3400-MR210CA and Wi-Fi radio transmit and receive performance capabilities of the device.

The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is guaranteed for room temperature of 25°C with a derating of 2-3 dB at boundary conditions.

Measurements were taken under typical conditions: VBATT=3.3V; VDDIO=3.3V; temperature: +25°C

Table 8-1. Features and Properties

Feature	Description
Part Number	ATWINC3400-MR210CA
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant
Host Interface	SPI
Dimension	22.4 x 14.7 x 2.0 mm

ATWINC3400-MR210CA

Feature	Description
Frequency Range	2.412GHz ~ 2.472GHz (2.4GHz ISM Band)
Number of Channels	11 for North America, and 13 for Europe and Japan
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM,16-QAM, QPSK, BPSK
Data Rate	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20 MHz, normal GI, 800 ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20 MHz, short GI, 400 ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Operating temperature	-40 to +85°C

9. Bluetooth Low Energy 4.0

The Bluetooth subsystem implements all the mission critical real-time functions. It encodes/decodes HCI packets, constructs baseband data packages, manages, and monitors the connection status, slot usage, data flow, routing, segmentation, and buffer control. The Bluetooth subsystem supports Bluetooth Low Energy modes of operation.

Supports the following advanced low energy applications:

- Smart energy
- Consumer wellness
- Home automation
- Security
- Proximity detection
- Entertainment
- Sports and Fitness
- Automotive

10. External Interfaces

10.1 Interfacing with the Host Microcontroller

This section describes about interfacing the ATWINC3400-MR210CA module with the host microcontroller. The interface comprises of a slave SPI and additional control signals, as shown in the following figure. For more information on SPI interface specification and timing, refer SPI Interface. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 10-1. Interfacing with Host Microcontroller

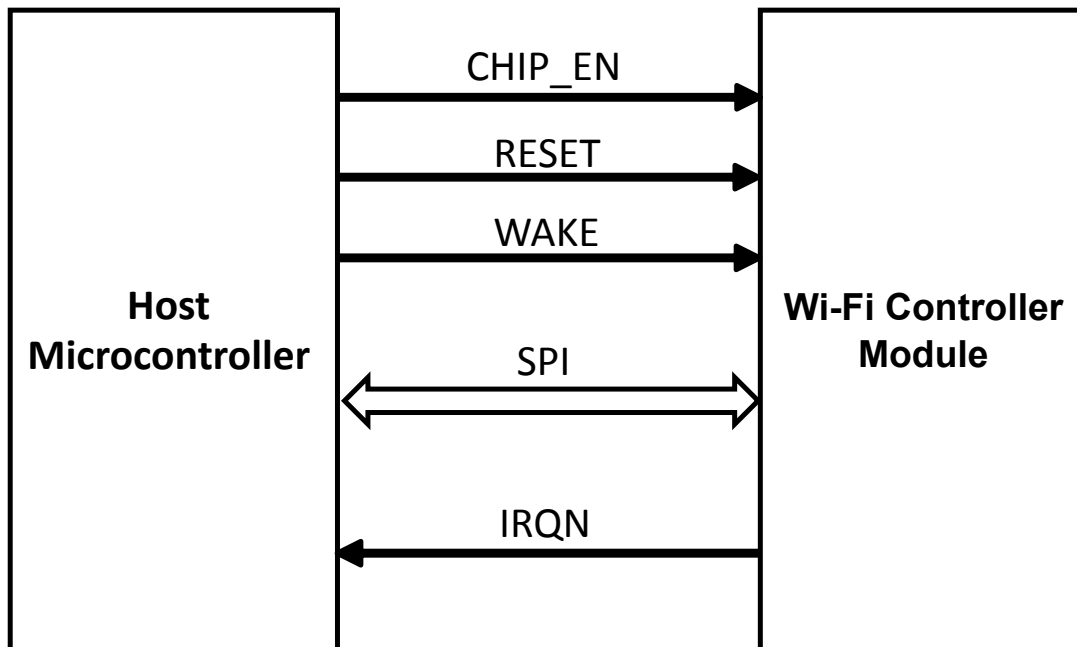


Table 10-1. Host Microcontroller Interface Pins

Pin Number	Function
4	RESET_N
11	WAKE
13	IRQ_N
22	CHIP_EN
16	SPI_SSN
15	SPI_MOSI
17	SPI_MISO
18	SPI_SCK

Related Links

[SPI Interface](#)

10.2 SPI Interface

10.2.1 Overview

The ATWINC3400-MR210CA has a Serial Peripheral Interface (SPI) that operates as an SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in the following table. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 10-2. SPI Interface Pin Mapping

Pin #	SPI function
10	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
15	MOSI(RXD): Serial Data Receive
18	SCK: Serial Clock
17	MISO(TXD): Serial Data Transmit

When the SPI is not selected, that is, when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO, and SCK pins of the ATWINC3400-MR210CA have internal programmable pull-up resistors. These resistors should be programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while the ATWINC3400-MR210CA is in the low-power sleep state, the current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

10.2.2 SPI Timing

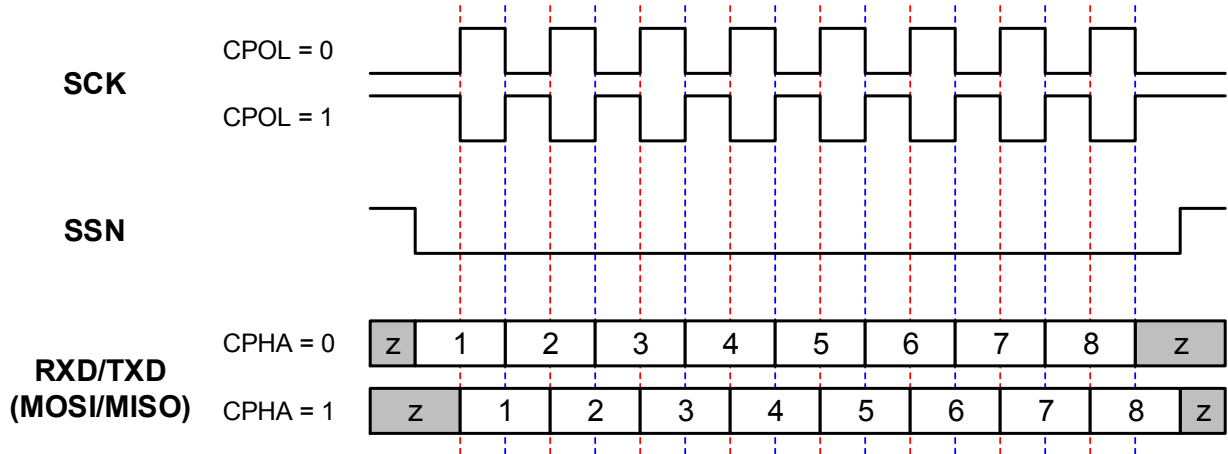
The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

Table 10-3. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Figure 10-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI timing is provided in the following figure and table.

Figure 10-3. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

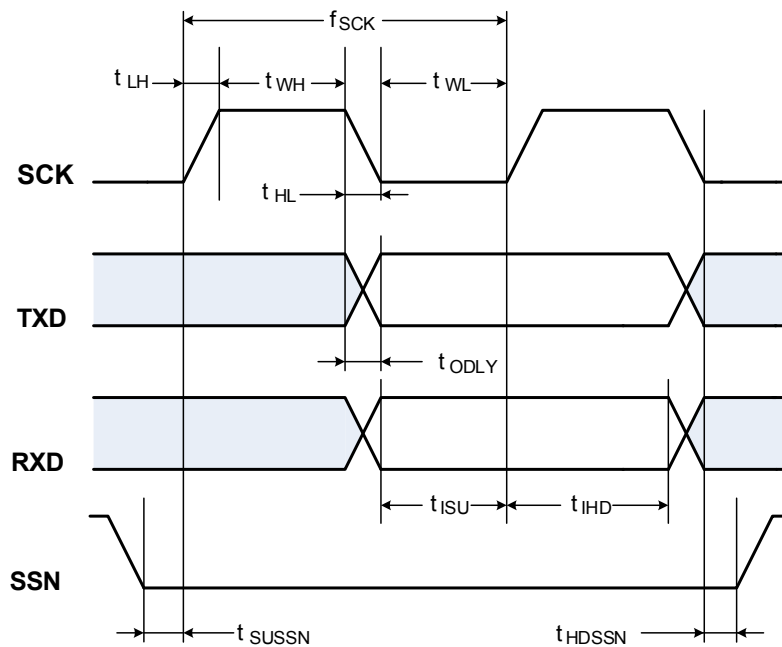


Table 10-4. SPI Slave Timing Parameters¹

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency ²	f_{SCK}	—	48	MHz
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay ³	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	

Parameter	Symbol	Min.	Max.	Units
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

Note:

1. Timing is applicable to all SPI modes
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout
3. Timing based on 15pF output loading

10.3 UART Interface

The ATWINC3400-MR210CA supports the Universal Asynchronous Receiver/Transmitter (UART) interface. This interface should be used for debug purposes only. The UART is available on pins 14 and 19. The UART is compatible with the RS-232 standard, and the ATWINC3400-MR210CA operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The default configuration for accessing the UART interface of ATWINC3400-MR210CA is mentioned below:

- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

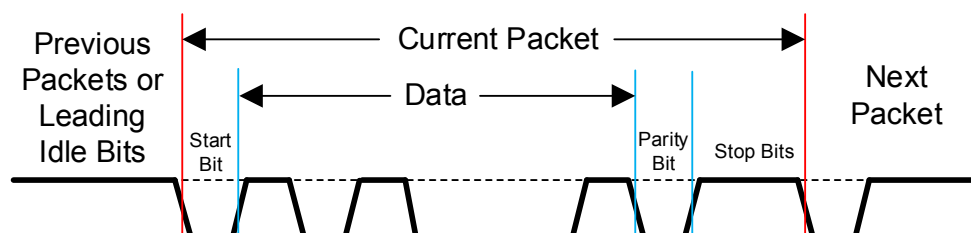
It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.



Important: UART2 supports RTS and CTS flow control. The UART RTS and UART CTS MUST be connected to the host MCU UART and enabled for the UART interface to be functional.

Figure 10-4. Example of UART RX of TX Packet

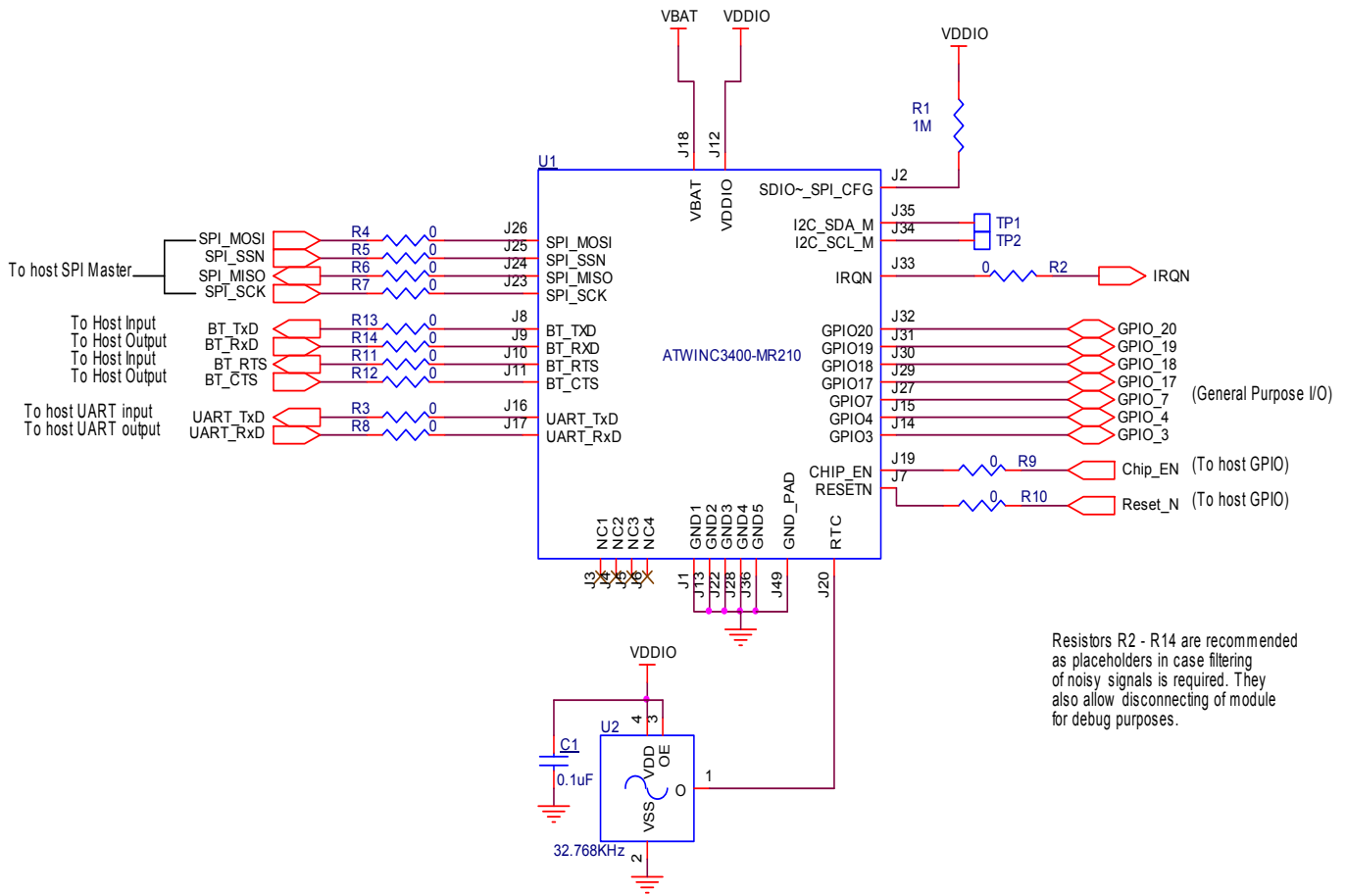


11. Application Reference Design

The ATWINC3400-MR210CA module application schematics for different supported host interfaces are shown in this section.

11.1 Host Interface - SPI

Figure 11-1. ATWINC3400-MR210CA Reference Schematic



Note: It is recommended to add test points for module pins J8, J9, J10, J11, J16 and J17 in the design.

The following table provides the reference Bill of Material (BoM) details for the ATWINC3400-MR210CA module with SPI as host interface.

Table 11-1. ATWINC3400-MR210CA Reference Bill of Materials for SPI Operation

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	U1	ATWINC3400-MR210CA	Wi-Fi/Bluetooth/BLE	Microchip Technology Inc.®	ATWINC3400-MR210CA	Custom

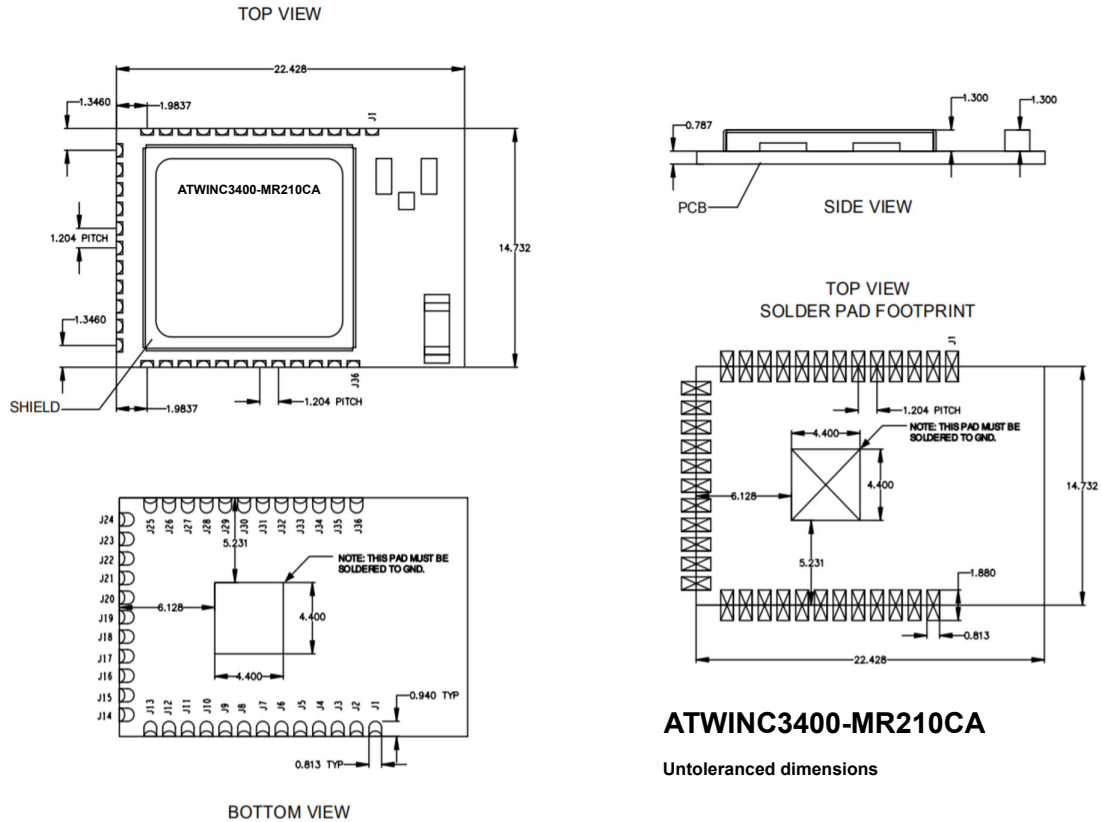
ATWINC3400-MR210CA

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number	Footprint
				Combo Module			
2	1	U2	ASH7KW-32.768KHZ-L-T	Oscillator, 32.768 kHz, +/-175 ppm, 1.2V - 5.5V, -40°C - +85°C	Abracon® Corporation	ASH7KW-32.768KHZ-L-T	OSCCC320X150X100-4N
3	1	R1	1M	RESISTOR, Thick Film, 1 MOhm, 0201	Panasonic	ERJ-1GEJ105C	RS0201
4	13	R2-R14	0	RESISTOR, Thick Film, 0 Ohm, 0201	Panasonic	ERJ-1GN0R00C	RS0201

12. Module Outline Drawings

The ATWINC3400-MR210CA module package details are outlined in the following figure.

Figure 12-1. ATWINC3400-MR210CA Footprint and Module Package Drawings - Top , Bottom and Side View



Note:

1. Dimensions are in mm.
2. It is recommended to have a 5x5 grid of GND vias solidly connecting the exposed GND paddle of the module to the ground plane on the inner/other layers of the host board. This will provide a good ground and thermal transfer for the ATWINC3400-MR210CA module.

13. Design Consideration

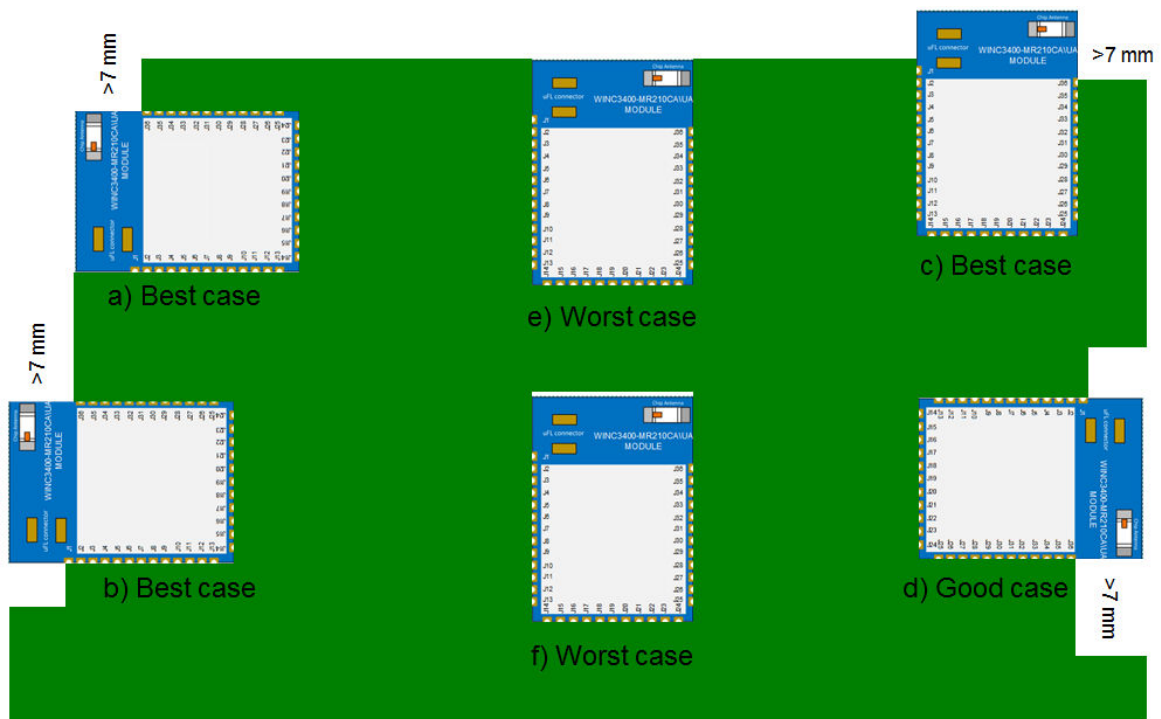
This section provides the guidelines on module placement and routing to achieve the best performance.

13.1 Module Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The module must be placed on the host board and the chip antenna area must not overlap with the host board. The following figure on placement reference shows the best, poor, and worst case module placements in the host board.

Figure 13-1. ATWINC3400-MR210CA Placement Example

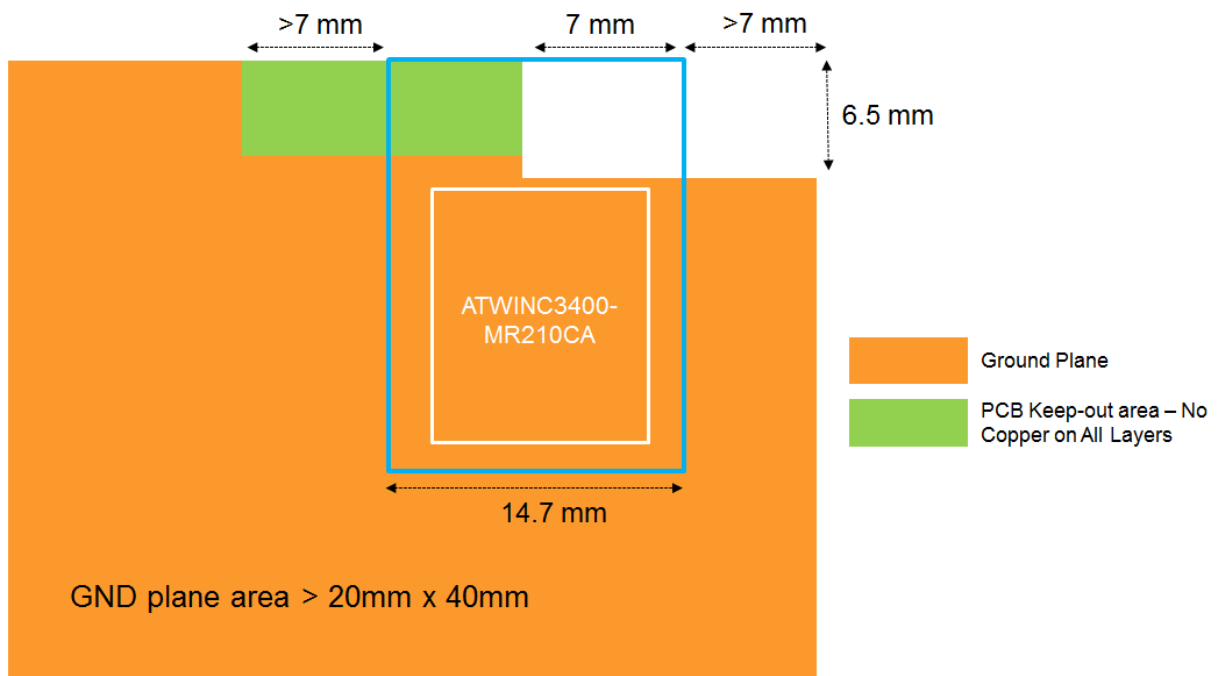


Caution: Do not place the module in the middle of the host board or far away from the host board edge.

- Follow the host board mechanical recommendation, ground plane and keep out recommendations as shown in the following figure. Module chip antenna is specifically tuned for this host board mechanical recommendation as shown in the following figure. The host PCB should have a thickness of 1.5 mm
 - Follow the module placement and keep out recommendation as shown in the following figure
 - Avoid routing any traces on the top layer of the host board which will be directly below the module area.
 - In keep out region, there should be no copper traces in all signal layers.
 - Avoid placing any components (like mechanical spacers, bump on and so on) on the host board closer to the chip antenna region.

- Place GND polygon pour below the module on the top layer of the host board. Avoid breaks in this GND plane, ensure continuous GND plane for better RF performance.
- GND polygon pour in the top layer of the host board should have a minimum area of 20 x 40 mm.
- Place sufficient GND vias on host board edge and below the module for better RF performance.
- It is recommended to have a 5x5 grid of GND vias solidly connecting the exposed GND paddle of the module to the ground plane of the host board. This will act as a good ground and thermal conduction path for the ATWINC3400-MR210CA module. The GND vias should have a minimum via hole size of 0.2 mm.
- Antenna on the module should not be placed in direct contact or close proximity to plastic casing/objects. Keep a minimum clearance of >7 mm in all directions around the chip antenna.

Figure 13-2. ATWINC3400-MR210CA Placement Reference



13.2 Antenna Performance

The ATWINC3400-MR210CA uses a chip antenna which is fed via matching network. The table below lists the technical specification of the chip antenna.

Table 13-1. Chip antenna specification

Parameter	Value
Peak gain	0.5 dBi
Operating frequency	2400 - 2500 MHz

Paramater	Value
Antenna P/N	2450AT18A100
Antenna vendor	Johanson Technology

14. Reflow Profile Information

This section provides the guidelines for the reflow process to get the module soldered to the customer's design.

14.1 Storage Condition

14.1.1 Moisture Barrier Bag Before Opening

A moisture barrier bag must be stored at a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product is 12 months from the date the bag is sealed.

14.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

14.2 Solder Paste

The SnAgCu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, no clean paste.

14.3 Stencil Design

The recommended stencil is laser-cut, stainless-steel type with thickness of 100 µm to 130 µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25 µm larger than the top is utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

14.4 Baking Conditions

This module is rated at MSL level 3. After the sealed bag is opened, no baking is required within 168 hours as long as the devices are held at ≤ 30°C/60% RH or stored at < 10% RH.

The module requires baking before mounting if:

- The sealed bag has been open for more than 168 hours
- The humidity indicator card reads more than 10%
- SIPs need to be baked for eight hours at 125°C

14.5 Soldering and Reflow Condition

Optimization of the reflow process is the most critical factor considered for lead-free soldering. The development of an optimal profile must account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensuring a successful lead-free assembly and achieves high yield and long-term solder joint reliability.

Temperature Profiling

Temperature profiling must be performed for all new board designs by attaching thermocouples at the solder joints, on the top surface of the larger components, and at multiple locations of the boards. This is to ensure that all components are heated to a temperature above the minimum reflow temperatures and the smaller components do not exceed the maximum temperature limit. The SnAgCu solder alloy melts at ~217°C, so the reflow temperature peak at joint level must be 15 to 20°C higher than melting temperature. The targeted solder joint temperature for the SnAgCu solder must be ~235°C. For larger or sophisticated boards with a large mix of components, it is also important to ensure that the temperature difference across the board is less than 10 degrees to minimize board warpage. The maximum temperature at the component body must not exceed the MSL3 qualification specification.

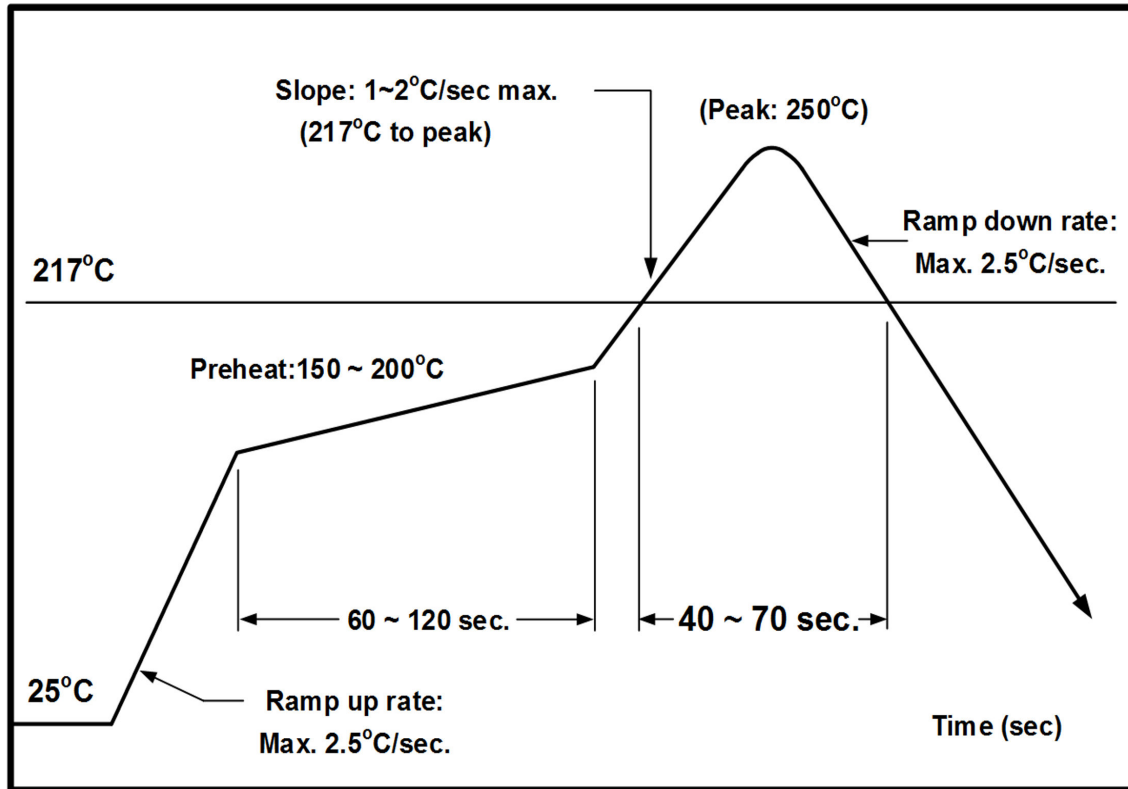
14.5.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere must be used for the lead-free assembly. The Nitrogen atmosphere is shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items must also be observed in the reflow process:

1. Some recommended pastes include:
 - NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu
 - SENJU N705-GRN3360-K2-V Type 3, no clean paste
2. Allowable reflow soldering iterations:
 - Three times based on the following reflow soldering profile (see, following figure).
3. Temperature profile:
 - Reflow soldering must be done according to the following temperature profile (see, following figure).
 - Peak temperature: 250°C

Figure 14-1. Solder Reflow Profile



Cleaning

The exposed ground paddle helps to self-align the module, avoiding pad misalignment. The use of no-clean solder pastes is recommended. As a result of reflow process, ensure to completely dry the no-clean paste fluxes. This may require longer reflow profiles and/or peak temperatures toward the high end of the process window as recommended by the solder paste vendor. It is believed that uncured flux residues can lead to corrosion and/or shorting in accelerated testing and possibly the field.

Rework

The rework removes the mounted SIP package and replaces it with a new unit. It is recommended that once an ATWINC3400-MR210CA module is removed and it must never be reused. During the rework process, the mounted module and PCB are heated partially, and the module is removed. It is recommended to heat-protect the proximity of the mounted parts and junctions and use the best nozzle for rework that is suited to the module size.

15. Module Assembly Considerations

The ATWINC3400-MR210CA module is assembled with an EMI shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a tin-plated steel (SPTE) and is not hermetically sealed. Solutions such as IPA and similar solvents can be used to clean this module. Cleaning solutions containing acid must never be used on the module.

The ATWINC3400-MR210CA module is manufactured without any conformal coating applied. It is the customer's responsibility if a conformal coating is specified and/or applied to this module.

16. Regulatory Approval

Regulatory Approvals received for ATWINC3400-MR210CA:

- United States/FCC ID: 2ADHKWINC3400
- Canada/ISED:
 - IC: 20266-ATWINC3400
 - HVIN: ATWINC3400-MR210CA
- Europe - CE (Approval pending)

16.1 United States

The ATWINC3400-MR210CA module has received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product, or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Verification or Declaration of Conformity) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

16.1.1 Labeling And User Information Requirements

The ATWINC3400-MR210CA module has been labeled with its own FCC ID number, and if the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label can use wording as follows:

For the ATWINC3400-MR210CA:

Contains Transmitter Module FCC ID: 2ADHKWINC3400

or

Contains FCC ID: 2ADHKWINC3400

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

A user's manual for the finished product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) <https://apps.fcc.gov/oetcf/kdb/index.cfm>

16.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

The antenna(s) used with this transmitter must be installed to provide a separation distance of at least 6.5 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

16.1.3 Helpful Web Sites

Federal Communications Commission (FCC): <http://www.fcc.gov>

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB): <https://apps.fcc.gov/oetcf/kdb/index.cfm>

16.2 Canada

The ATWINC3400-MR210CA module has been certified for use in Canada under Innovation, Science and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

16.2.1 Labeling and User Information Requirements

Label Requirements (from RSP-100 Issue 11, Section 3): The host device shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host product must be labeled to

display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:

For the ATWINC3400-MR210CA:

Contains IC: 20266-ATWINC3400

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device complies with Industry Canada license exempt RSS standard(s). Operation is subject to the following two conditions:

- (1) This device may not cause interference, and**
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- (1) l'appareil ne doit pas produire de brouillage, et**
- (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.**

Guidelines on Transmitter Antenna for License Exempt Radio Apparatus:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

16.2.2 RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The installation of the transmitter must ensure that the antenna has a separation distance of at least 6.5 cm from all persons or compliance must be demonstrated according to the ISED SAR procedures.

16.2.3 Helpful Web Sites

Innovation, Science and Economic Development Canada: <http://www.ic.gc.ca/>

16.3 Europe

Note: Pending for an approval.

The ATWINC3400-MR210CA module is a Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The ATWINC3400-MR210CA module has been tested to RED 2014/53/EU Essential Requirements for Health and Safety (Article (3.1(a)), Electromagnetic Compatibility (EMC) (Article 3.1(b)), and Radio (Article 3.2), which is summarized in the following European Compliance Testing table.

The ETSI provides guidance on modular devices in the “*Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment*” document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/203367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the testing listed in the following European Compliance Testing table the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified. When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

16.3.1 Labeling and User Information Requirements

The label on the final product that contains the ATWINC3400-MR210CA module must follow CE marking requirements.

Table 16-1. European Compliance Testing

Certification	Standards	Article	Laboratory	Report Number	Date
Safety	EN60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013	[3.1. (a)]	TUV Rheinland, Taiwan	10062655 001	30-Oct-2017
Health	EN300328 V2.1.1/EN62311:2008			50103733 001 50103734 001	30-Oct-2017
EMC	EN301489-1 V2.1.1 EN301489-1 V2.2.0	[3.1(b)]		10062417 001	30-Oct-2017
	EN301489-17 V3.1.1 EN301489-17 V3.2.0				
Radio	EN300328 V2.1.1	[3.2]	50103733 001 50103734 001	30-Oct-2017	

16.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1, when non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

The European Compliance Testing listed in the preceding table was performed using the integral chip antenna.

16.3.2.1 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type ATWINC3400-MR210CA is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity for this product is available at <http://www.microchip.com/design-centers/wireless-connectivity/>.

16.3.3 Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: <http://www.ecodocdb.dk/>.

Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU):
https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/rtte_en
- European Conference of Postal and Telecommunications Administrations (CEPT):
<http://www.cept.org>
- European Telecommunications Standards Institute (ETSI):
<http://www.etsi.org>
- The Radio Equipment Directive Compliance Association (REDCA):
<http://www.redca.eu/>

16.4 Other Regulatory Information

- For information about other countries' jurisdictions not covered here, refer to <http://www.microchip.com/design-centers/wireless-connectivity>
- Should other regulatory jurisdiction certification be required by the customer, or the customer needs to recertify the module for other reasons, contact Microchip for the required utilities and documentation

17. Reference Documentation

The following are the set of collaterals to ease integration and device ramp.

- Wi-Fi Network Controller Software Design Guide Application Note
- Integrated Serial Flash Memory Download Procedure Application Note
- Wi-Fi Network Controller Software Programming Guide Application Note
- ATWINC3400 XPro User Guide
- BLE Example Profiles Applications User Guide

Note:

For a complete listing of development-support tools and documentation, visit <http://www.microchip.com/wwwproducts/en/ATWINC3400> or refer to the customer support section on options to the nearest Microchip field representative.

18. Document Revision History

Rev A - 10/2017

Section	Changes
Document	Initial Release

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