SERVICE MANUAL FOR

8399

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MiTAC

8399 N/B Maintenance

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1. Engineer Hardware Specification

1.1 Introduction

The 8399 motherboard would support the AMD K8 62W Dublin (32 bit) with 256KB L2 cache/ Hammer (64 bit) with 1MB L2 cache with uPGA Package. This system is based on PCI architecture, which have standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0b. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as AC/Battery Power, Battery, WIRELESS LAN status, CD-ROM, HDD, NUM LOCK, CAP LOCK, and SCROLL LOCK status. It also equipped 6 USB2.0 ports.

The memory subsystem supports 0MB on board; Expandable up to 1024MB Expandable with combination of optional 128/256/512 MB memory 200-pin DDR 266/333/400 DRAM Memory Module x2, PC-2100/2700/3200 specification.

The “K8N800”chipset is a high performance, cost-effective and energy efficient solution for the implementation of desktop personal computer systems with 8 / 16-bit 800 / 600 / 400 / 200MHz HyperTransport. CPU host interface based on AMD K8 / ClawHammer. Processors. The K8N800 north bridge supports a high speed 8-bit 8x66 Mhz Quad Data Transfer interconnect (V-Link) to the VT8235 South Bridge. These chips also contain a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (double words) of post write buffers are included to allow for concurrent CPU and V-Link operation. For V-Link Host operation, forty-eight levels (double words) of post write buffers and sixteen levels (double words) of prefetch buffers are included for concurrent V-Link bus and DRAM / cache accesses. When combined, the V-Link host / Client controllers realize a

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Complete PCI sub-system and support enhanced PCI bus commands such as “ Master-Read-Line”, “memory-Read-Multiple” and “Memory-Write-Invalid” commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The VT8235CD “V-Link Client Controller” is a highly integrated PCI /LPC controller. Its internal bus structure is based on a 66 MHz PCI bus that provides 2x bandwidth compared to previous generation PCI bridge chips. The VT8235CD also provides a 533 MB/sec bandwidth Host / Client V-Link interface with V-Link-PCI and V-Link-LPC controllers. It supports six PCI slots of arbitration and decoding for all integrated functions and LPC bus.

To provide for the increasing number of multimedia applications, the AC97 CODEC VT1617/1617A is integrated onto the motherboard

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows XP and Windows 2000 to take full advantage of the hardware capabilities such as bus mastering IDE, Plug & Play, and Advance configuration and power interface(ACPI).

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 Hardware Specification(1)

CPU	AMD K8 62W Dublin (32 bit)/Hammer (64 bit) with uPGA Package
	Thermal Ceiling 62W TDP
Core Logic	VIA K8N800 + VT8235CD
L2 Cache	256KB for Dublin / 1MB for Hammer
System BIOS	Inside 256 KB Flash EPROM (Include System BIOS and VGA BIOS)
	ACPI 1.0b; DMI 2.3.1 compliant
	Plug & Play capability
OSD	Audio Volume Up/Down status, Brightness status, RF Antenna On/Off status, Display Status
Memory	0MB on board; Expandable up to 1024MB
	Expandable with combination of optional 128/256/512 MB memory
	200-pin DDR 333/400 DRAM Memory Module x2, PC-2700/3200 specification
ROM Driver	12.7mm Height
	CD / DVD Rom Drive
	Combo Drive
	Super Combo Drive
HDD	2.5” (9.5 mm height): 40/60/80 GB; ATA 100/133 Support
	Removable for Distributor
Display	15” XGA TFT Display; Resolution: 1024X768
Video Controller	VIA K8N800 integrated(64MB SMA)
Keyboard	19mm key pitch/ 3.0mm key stroke/ 307mm length
	Windows Logo Key x 1; Application Key x 1
Pointing Device	Glide pad with 2x buttons and 2 direction scroll button

1.2 Hardware Specification(2)

Continue to previous page

PCMCIA	Cardbus Controller: ENE CB1410
	one type II slots CardBus / no ZV port support/ no wakeup from S3
	Power switch: ENE CP-2211
Indicator	3 LEDs for Power/Battery/Charge status
	1 LED for Radio wave status Power LED (BTO: Wireless LAN only)
	5 LEDs for HDD Access, ODD Access , Num lock, Cap lock and Scroll Lock
Audio System	Sound Blaster Pro compatible
	AC97 V2.2 Codec
	Built-in Mono Microphone
	2X 2W Speakers
I/O Port	USB port (2.0, backward compatible with USB1.1) x 6
	RJ-11 port x 1
	RJ-45 port x 1
	DC input x 1
	VGA monitor port x1
	Audio-out x 1
	Mic-in x 1
	S/W Volume Control
	7-Pin S Video TV-Out x 1 (NTSC/PAL)
Communication	Built-in 56Kbps V.90 modem support ISN standard
	Built-in 10/100 M based-T LAN
	One Mini PCI slot and antenna reserved for wireless LAN

1.2 Hardware Specification(3)

Continue to previous page

AC Adapter	Universal AC adapter 90W ; Input: 100-240V, 50/60Hz AC (support power on charge)
Battery	6/8 cell (2000/2200mAH,3.7V) Li-ion smart battery
Dimensions	335*280*30(min) , 335x280x42 (max)
Weight	3.5kg (P)
Accessories	Power Cord, AC Adapter, RJ-11 Phone Cable (p),System Driver CD-Title
Architecture	Microsoft WHQL Designed for Windows XP
Options	128/256/512MB DDR RAM, AC Adapter w/o Power Cord, Battery, Notebook Carry Bag

1.3 System Hardware Parts

1.3.1 Processor

The AMD K8 Hammer processor family is designed to support performance desktop and workstation applications. It provides a high-performance HyperTransport. link to I/O, as well as a single 64-bit high-performance DDR memory controller.

- **Compatible with Existing 32-bit Code Base**
  - Including support for SSE, SSE2, MMXTM, 3DNow!TM, technology and all legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on-chip

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- **AMD x86-64 Technology**
  - AMD.s 64-bit x86 instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Eight new 64-bit integer registers (16 total)
  - Eight new 128-bit SSE/SSE2 registers (16 total)
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 72-bit DDR at 100, 133, 166 and 200MHz
- **HyperTransport. Technology to I/O Devices**
  - Two 8-bit links each support 1600 mega-transfers (MT) per second or 1.6 Gbytes/s in each direction
  - Can be configured as single 16-bit link supporting 1600 MT/s or 3.2 Gbytes/s in each direction
- **64-Kbyte 2-way Associative ECC-Protected L1 Data Cache**
  - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-way Associative Parity-Protected L1 Instruction Cache**
  - With advanced branch prediction
- **16-way Associative ECC-Protected L2 Cache**
  - Exclusive cache architecture.storage in addition to L1 caches

- 256 KB, 512 KB, and 1 MB options

- **Machine Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
  - Multiple low-power states
  - System Management Mode (SMM)
  - ACPI 2.0 compliant, including support for processor performance states
- **Electrical Interfaces**
  - HyperTransport. Technology: LVDS-like differential, unidirectional
  - DDR: SSTL_2 per JEDEC DDR specification
  - Clock, reset, and test signals also use DDR-like electrical specifications
- **Packaging**
  - 754-pin lidded micro PGA
  - 1.27-mm pin pitch
  - 29x29 row pin array
  - 40mm x 40mm organic substrate
  - Organic C4 die attach

1.3.2 K8N800 North Bridge

The "K8N800"chipset is a high performance, cost-effective and energy efficient solution for the implementation of mobile personal computer systems with 8 / 16-bit 800 / 600 / 400 / 200 MHz HyperTransport. CPU host interface based on AMD K8 / Claw Hammer processors.

- **Defines Highly Integrated Solutions for Performance PC Desktop Designs**
  - High performance North Bridge with HyperTransport. interface to AMD K8 CPU plus AGP 8x external bus to external Graphics Controller plus high-speed V-Link interface to South Bridge.
  - Combines with VIA VT8235CD V-Link South Bridge for integrated LAN, Audio, ATA133 IDE, and 6 USB 2.0 ports
  - 587 Ball Grid Array package with 35 x 35 mm body size, 1.27mm ball pitch
  - 1.5V core, 0.15 u process
- **High Performance HyperTransport CPU Interface**
  - Chipset support for AMD. K8 / ClawHammer. Processor
  - Processor interface via HyperTransport. Bus
  - Separate "transmit" and "receive" buses for no lost "bus turnaround" cycles
  - All transmit and receive signals use 2 pin low-voltage-swing differential signalling for high-reliability and high speed
  - 8 or 16-bit control / address / data transfer both directions

- 800 / 600 / 400 / 200 MHz clock rates with “Double Data Rate”-style operation for 1600/1200/800/400 MT/s in both directions simultaneously (total 6.4GB/sec using 16-bit transfer mode)
- Default 8-bit / 200 MHz operation on startup for high reliability with speedup to dual 16-bit, 800 MHz operation (6.4 GB/sec total bandwidth) under software control (transmit and receive may be different widths and / or speeds)

Full Featured Accelerated Graphics Port (AGP) 8x Controller

- Supports 533 MHz 8x, 266 MHz 4x, and 133 MHz 2x transfer modes for AD and SBA signaling
- AGP v3.0 compliant with 8x transfer mode
- Pseudo-synchronous with the host CPU bus with optimal skew control
- Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
- AGP pipelined split-transaction long-burst transfers up to 1GB/sec
- Eight level read request queue
- Four level posted-write request queue
- Thirty-two level (quadwords) read data FIFO (256 bytes)
- Sixteen level (quadwords) write data FIFO (128 bytes)
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Graphics Address Relocation Table (GART)

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- One level TLB structure
- Sixteen entry fully associative page table
- LRU replacement scheme
- Independent GART lookup control for host / AGP / PCI master accesses
- Windows 95 OSR-2 VXD and integrated Windows 98 / 2000 / XP mini port driver support

High Bandwidth 533 MB / Sec 8-bit V-Link Host Controller South Bridge Interface

- Supports 66 MHz V-Link Host interface with total bandwidth of 533 MB/sec
- Operates in 2x, 4x, and 8x modes
- Full duplex commands with separate command / strobe for 4x / 2x mode, half-duplex for 8x mode
- Request / Data split transaction
- Configurable outstanding transaction queue for Host to V-Link Client accesses
- Supports Defer / Defer-Reply transactions
- Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
- Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer Latency
- All V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow
- Highly efficient V-Link arbitration with minimum overhead

- All V-Link transactions have predictable cycle length with known command / data duration

Integrated Graphics / Video Accelerator

- Optimized Share Memory Architecture (SMA)
- 16 / 32 / 64 MB frame buffers using system memory
- Internal AGP 8x equivalent performance
- Separate 128-bit data paths between north bridge and graphics core for pixel data flow and texture/command access
- Graphics engine clock up to 200MHz decoupled form memory clock
- High quality DVD video playback
- Internal hardware VGA controller with true-color / high-color sprite for hardware cursor implementation
- 128-bit 2D graphics engine
- 128-bit 3D graphics engine
- Floating point triangle setup engine
- Microsoft DirectX texture compression
- 4.5M triangles/second setup engine
- 400M texels/second bilinear fill rate

- **Extensive Display Support**
  - CRT display interface with 24-bit true-color RAMDAC up to 300MHz pixel rate with gamma correction capability
  - DFP" flat panel interface supporting single-channel or dual-channel LVDS encoders
  - DVI" Flat Panel Monitor 12-bit DVI 1.0-compatible interface designed for use with external TMDS encoder
  - AGP 8x / 4x functions muxed on DFP/DVI pins for optional external graphics controller upgrade module
  - Dedicated 12-bit interface to TV Encoder for NTSC or PAL TV display (may be optionally configured as 12-bit DVI 1.0 interface to external TMDS encoder for driving a Flat Panel Monitor)
- **DuoView+ Dual Image Capability**
  - Direct Win98, WinME and WinXP multi-monitor, extended desktop support
  - Independent resolution and color depth for secondary desktop
  - Improved display flexibility with simultaneous LCD/CRT, CRT/DVI, CRT/TV, LCD/TV, DVI/TV operation capability
  - CRT, LCD or TV refresh rates are independently programmable to allow optimum image quality
  - Enables different images on different displays simultaneously for true multitasking
  - Full Media capabilities on all displays
  - Support for CRT resolutions up to 1920x1440 and panel resolutions up to 1600x1200
  - Automatic panel power sequencing and VESA DPMS CRT power-down

- ❖ Built-in reference voltage generator and monitor sense circuits
- ❖ I2C Serial Bus and DDC Monitor Communications for CRT Plug-and-Play configuration

❑ **Video Support**

- ❖ High quality 5-tap horizontal and 5-tap vertical scaler (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling filtering for horizontal and vertical down-scaling)
- ❖ Color space conversion
- ❖ Color enhancement (contrast, hue, saturation, brightness, and gamma correction)
- ❖ Color and chroma key support
- ❖ Hardware sub-picture blending
- ❖ Bob / weave de-interlacing mode and advanced de-interlacing to improve video quality
- ❖ Video gamma correction
- ❖ PAL / NTSC TV output capability using external TV encoder
- ❖ Support CCIR601 standard

❑ **MPEG-2/1 Video Decoder**

- ❖ MPEG-2 hardware slice layer, iDCT, and motion compensation for full speed DVD playback

❑ **2-D Hardware Acceleration Features**

- ❖ BitBLT 9bit block transfer) functions including alpha blts

- Text function
- Bresenham line drawing / style line function
- ROP3, 256 operation
- Color expansion
- Source and destination color keys
- Transparency mode
- Window clipping
- 8, 16, and 32 bpp mode acceleration

3-D Hardware Acceleration Features

- Microsoft DirectX 7.0 and 8.0 compatible
- OpenGL driver available
- Floating-point setup engine
- Triangle rate up to 4.5-million triangles per second and Pixel rate up to 400 million pixels per second for 2 texture, depth test and alpha blending
- 8K Texture Cache
- Microsoft DirectX Texture Compression (S3TC)
- Flat and Gouraud shading
- Hardware back-face culling

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- 16-bit, 32-bit Z test, and 24+8 Z+ Stencil test support
- Z-Bias support
- Stipple Test, Line-Pattern test, Text re-Transparence test, Alpha test support
- Edge anti-aliasing support
- Two textures per pass
- Tremendous Texture Format: 16/32 bpp ARGB, 1/2/4/8 bpp Luminance, 1/2/4/8 bpp Intensity, 1/2/4/8 bpp Paletized (ARGB) , YUV 422/420 format
- Texture sizes up to 2048x2048
- High quality texture filter modes: Nearest, Linear, Bi-linear, Tri-linear, Anisotropic
- LOD-Bias support
- Vertex Fog and Fog Talbe
- Specular Lighting
- Alpha Blending
- Bump mapping
- High quality dithering
- ROP2 support
- Internal full 32-bit ARGB format for high rendering quality

- ❖ System balance to achieve high performance

❑ **Advanced System Power Management**

- ❖ Power down of SDRAM (CKE)
- ❖ Independent clock stop controls for CPU, DDR SDRAM, VLINK interface, graphics engine (2D,3D, video, display) and on-chip AGP bus
- ❖ Suspend power plane for preservation of memory data
- ❖ Suspend-to-DRAM and self-refresh power down
- ❖ Low-leakage I/O pads
- ❖ ACPI 1.0B and PCI Bus Power Management 1.1 compliant

❑ **Full Software Support**

- ❖ Drivers for major operating system and APIs (windows 9x, Windows NT, Windows2000,Windows XP, Direct3D, DirectDraw and DirectShow, OpenGL ICD for Windows 9x, NT, 2000, and XP)
- ❖ Chipset and Video BIOS support (including all standard VESZA CRT display modes)

1.3.3 VIA VT8235CD BGA PCI-LPC/ISA South Bridge

The VT8235CD South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8235CD includes standard intelligent peripheral controllers:

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- IEEE 802.3 compliant 10 / 100 Mbps PCI bus master Ethernet MAC with standard MII interface to external PHYceiver.
- Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8235CD also supports the UltraDMA-133, 100, 66, and 33 standards to allow reliable data transfer at rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.
- Universal Serial Bus controller that is USB v2.0 / 1.1 and Universal HCI v2.0 / 1.1 compliant. The VT8235CD includes three root hubs with six function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.
- Keyboard controller with PS2 mouse support.
- Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.
- Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.
- Full System Management Bus (SMBus) interface.

- Integrated bus-mastering dual full-duplex direct-sound AC97-link-compatible sound system.
- Plug and Play controller that allows complete steer ability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigure ability of onboard peripherals for Windows family compliance.

The VT8235CD also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISADMA modes. Compliant with the PCI-2.2 specification, the VT8235CD supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (double words) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

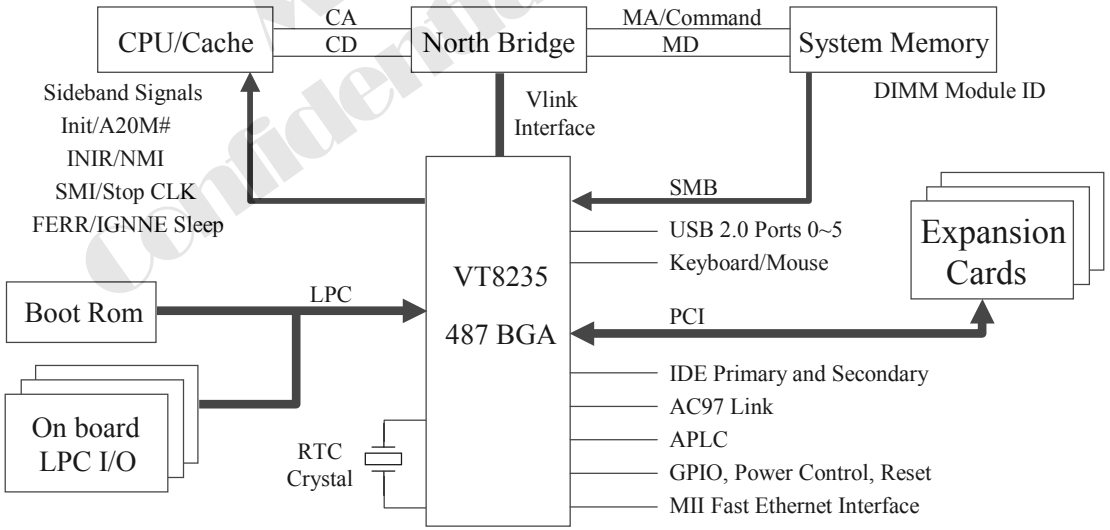

Figure 1. PC System Configuration Using the VT8233

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- **Inter-operable with VIA Host-to-V-Link Host Controller**
  - Combine with VT8754 (Apollo P4X333) for a complete 533 / 400 MHz FSB Pentium 4 system
  - Combine with VT8377 (Apollo KX400) for a complete 266 / 200 MHz FSB Athlon Socket-A system
  - May be used interchangeably with the VT8235CDLSout h Bridge in most board designs
- **High Bandwidth 533 MB/s 8-bit V-Link Client Controller**
  - Supports 66 MHz V-Link Client interface with peak bandwidth of 533 MB/sec
  - V-Link operates in 2x, 4x, and 8x modes
  - Full duplex commands with separate Strobe / Command
  - Request / Data split transaction
  - Configurable outstanding transaction queue for V-Link Client accesses
  - Auto Client Retry to eliminate V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency; all V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow.
  - Highly efficient V-Link arbitration with minimum overhead; all V-Link transactions have predictable cycle length with known Command / Data duration
  - Auto connect / reconnect capability and dynamic stop for minimum power consumption
  - Parity checking to insure correct data transfers

- **Integrated Peripheral Controllers**
  - Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability
  - Integrated USB 2.0 Controller with three root hubs and six function ports
  - Dual channel UltraDMA-133 / 100 / 66 / 33 master mode EIDE controller
  - AC-link interface for AC-97 audio codec and modem codec
  - HSP modem support
  - Integrated DirectSound compatible digital audio controller
  - LPC interface for Low Pin Count interface to Super-I/O or ROM
- **Integrated Legacy Functions**
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated DMA, timer, and interrupt controller
  - Serial IRQ for docking and non-docking applications
  - Fast reset and Gate A20 operation
- **Concurrent PCI Bus Controller**
  - 33 MHz operation

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- Supports up to six PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec (data sent to north bridge via high speed V-Link Interface)
- PCI master snoop ahead and snoop filtering
- Eight DW of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Four lines of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Delay transaction from PCI master accessing DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts

- ❖ PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

❑ **Fast Ethernet Controller**

- ❖ High performance PCI master interface with scatter / gather and bursting capability
- ❖ Standard MII interface to external PHYceiver
- ❖ 1 / 10 / 100 MHz full and half duplex operation
- ❖ Independent 2K byte FIFOs for receive and transmit
- ❖ Flexible dynamically loadable EEPROM algorithm
- ❖ Physical, Broadcast, and Multicast address filtering using hashing function
- ❖ Magic packet and wake-on-address filtering
- ❖ Software controllable power down

❑ **UltraDMA- 133/ 100 / 66 / 33 Master Mode EIDE Controller**

- ❖ Dual channel master mode hard disk controller supporting four Enhanced IDE devices
- ❖ Transfer rate up to 133MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-133 interface
- ❖ Increased reliability using UltraDMA-133/100/66 transfer protocols Thirty-two levels (double words) of prefetch and write buffers
- ❖ Dual DMA engine for concurrent dual channel operation

- ❖ Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
- ❖ Full scatter gather capability
- ❖ Support ATAPI compliant devices including DVD devices
- ❖ Support PCI native and ATA compatibility modes
- ❖ Complete software driver support

❑ **Direct Sound Ready AC97 Digital Audio Controller**

- ❖ AC-Link access to 4 CODECs (AC97 + AMC97 + MC97)
- ❖ Multi channel Audio
- ❖ Bus Master Scatter / Gather DMA
- ❖ Dedicated read and write channels supporting simultaneous stereo playback and record
- ❖ Dedicated read and write channels supporting simultaneous modem receive and transmit
- ❖ 1 stereo DirectSound channel with source / volume control / mixer
- ❖ 1 shared FM / SPDIF PCM read channel
- ❖ 1 dedicated channel supporting multi-channel audio
- ❖ 32-byte line-buffers for each SGD channel
- ❖ Programmable 8bit / 16bit mono / stereo PCM data format support
- ❖ AC97 2.1 compliant

- **System Management Bus Interface**
  - Host interface for processor communications
  - Slave interface for external SMBus masters
- **Universal Serial Bus Controller**
  - USB v2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compatible
  - USB v1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible
  - Eighteen level (double words) data FIFO with full scatter and gather capability
  - Three root hubs and six function ports
  - Integrated physical layer transceivers with optional over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support
- **Sophisticated PC2001-Compatible Mobile Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control
  - Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options,

suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up

- ❖ Multiple suspend power plane controls and suspend status indicators
- ❖ One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- ❖ Normal, doze, sleep, suspend and conserve modes
- ❖ Global and local device power control
- ❖ System event monitoring with two event classes
- ❖ Primary and secondary interrupt differentiation for individual channels
- ❖ Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
- ❖ 32 general purpose input ports and 32 output ports
- ❖ Multiple internal and external SMI sources for flexible power management models
- ❖ Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- ❖ Thermal alarm on external temperature sensing circuit
- ❖ I/O pad leakage control

❑ **Plug and Play Controller**

- ❖ PCI interrupts steerable to any interrupt channel
- ❖ Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, and audio

- ❖ Microsoft Windows XPTM, Windows NTTM, Windows 2000TM, Windows 98TM and plug and play BIOS compliant

- ❑ **Built-in NAND-tree pin scan test capability**
- ❑ **0.22um, 2.5V, low power CMOS process**
- ❑ **Single chip 27 x 27 mm, 1.0 mm ball pitch, 487 pin BGA**

1.3.4 System Frequency Synthesizer and DDR-SDRAM Buffer: ICS950403

The ICS950403 is a system clock synthesizer chip for AMD K8 based notebook systems with AMD, VIA or Ali chipset. This provides all clocks required for such a system. The ICS950403 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations. Serial programming I 2 C interface allows changing functions, stop clock programming and frequency selection.

- ❑ **Output Features**
  - ❖ 2 - Differential pair push-pull CPU clocks @ 3.3V
  - ❖ 8 - PCICLK (Including 1 free running) @ 3.3 V
  - ❖ 3 - Selectable PCICLK/HTTCLK @ 3.3V
  - ❖ 1 - HTTCLK @ 3.3V
  - ❖ 1 - 48MHz @ 3.3V fixed

- 1 - 24_48MHz @ 3.3V
- 3 - REF @ 3.3V, 14.318MHz

Features/Benefits

- Programmable output frequency
- Programmable output divider ratios
- Programmable output rise/fall time
- Programmable output skew
- Programmable spread percentage for EMI control
- Watchdog timer technology and RESET# output to reset system if system malfunction
- Programmable watch dog safe frequency
- Support I2C index read/write and block read/write operations
- Uses external 14.318MHz crystal
- Support Hyper Transport Technology (HTTCLK)
- 48-Pin 300mil SSOP

1.3.5 PC Card Interface Controller: ENE CB1410

The ENE CB1410 is a high-performance PCI-to-PC Card controller that supports a single PC Card socket compliant with the 1997 PC Card Standard. The ENE CB1410 provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The 1997 PC Card Standard retains the 16-bit PC Card specification defined in PCI Local Bus Specification and defines the new 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The ENE CB1410 supports both 16-bit and CardBus PC Cards, powered at 5 V or 3.3 V, as required.

The ENE CB1410 is compliant with the PCI Local Bus Specification, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers or CardBus PC Card bridging transactions. The ENE CB1410 is also compliant with the latest PCI Bus Power Management Interface Specification and PCI Bus Power Management Interface Specification for PCI to CardBus Bridges.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The ENE CB1410 internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The ENE CB1410 can also be programmed to accept fast posted writes to improve system-bus utilization.

Multiple system-interrupt signaling options are provided, including: parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features designed into the ENE CB1410, such as socket activity light-emitting diode (LED) outputs, are discussed in detail throughout the design specification.

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An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption while operating at PCI clock rates up to 33MHz. Several low-power modes enable the host power management system to further reduce power consumption.

- **The CB1410 Supports the Following Features**
  - 3V operation with 5V tolerant
  - 144-pin LQFP or 144-ball LFBGA package for CB1410 single slot Cardbus controller
- **Compliant with**
  - PCI Local Bus Specification, Revision 2.2
  - PCI Bus Power Management Interface Specification, Revision 1.1
  - PCI Mobile Design Guide, Version 1.1
  - Advanced Configuration and Power Interface Specification, Revision 1.0
  - PC99 System Design Guide
  - PC Card Standard 8.0
- **Interrupt Configuration**
  - Support parallel PCI interrupts
  - Support parallel IRQ and parallel PCI interrupts
  - Support serialized IRQ and parallel PCI interrupts
  - Support serialized IRQ and PCI interrupts

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- **Power Management Control Logic**
  - Support CLKRUN# protocol
  - Supports SUSPEND#
  - Support PCI PME# from D3, D2, D1 and D0
  - Support PCI PME# from D3 cold
  - Supports D3STATE#
- **Power Switch Interface**
  - Supports parallel 4 wire power switch interface.
- **Misc Control Logic**
  - Support CLKRUN# protocol
  - Support serial EEPROM interface
  - Support socket activity LED
  - Support 5 GPIOs and GPE#
  - Support standard Zoomed Video Port
  - Support SPKOUT, CAUDIO and RIOUT#
  - Support PCI LOCK

1.3.6 One-Slot PC Card Power Interface Switch: ENE CP-2211

CP-2211 is single Slot PCMCIA and CardBus power switch. It integrates control logic, low switching resistance MOSFET, over current alarm and over temperature auto shutdown circuits. It can deliver 3.3V or 5V to PC Card VCCOUT and 3.3V, 5V or 12V to PC Card VPPOUT. The output current is up to 1A for VCCOUT and 250mA for VPPOUT.

- Low Switching Resistance (100mΩ for VCC Switch)
- Over temperature auto shutdown
- 1A output current for VCCOUT
- 150mA output current for VPPOUT
- Only 3.3V is required for chip normal operation
- 12V is not required for 3.3V or 5V Output
- Break-Before-Make Switching
- 16-Pin SSOP Package

1.3.7 AC'97 Audio System: VIA VT1617/1617A

The VT1617/1617A is a high performance audio codec which complies with the AC'97 revision 2.3. It integrates Sample Rate Converters on all channels and can be adjusted in 1Hz increments. This chip supports 96KHz sampling rates, high-quality 96KHz S/PDIF output, stereo digital playback.

The 20bit, ΣΔADCs VT1617/1617A implements stereo recording and white noise removal to ensure the best quality of recording. It features 8-channel hardware-expansion for flexible 7.1-channel applications. It also contains a hardware down-mixing feature that allows the end users enjoy 6-channel audio with 2-channel or 4-channel speakers. The analog mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround sound effect for stereo media. The VT1617/1617A has a built-in quality headphone amplifier and a high-accuracy PLL for cost saving. This codec is designed with aggressive power management to achieve low power consumption; when used with a 3.3V analog supply, the owner consumption is further reduced.

- **AC'97 V2.3 Audio Codec**
  - Fully compliant with AC'97 Revision 2.3
- **High Audio Quality**
  - Support sampling rates up to 96KHz
  - Independent 20-bit ADC and 20-bit DAC
  - SNR (Signal to Noise Ratio) exceeds 95dB
  - Built-in 1Hz resolution VSR converter
- **Various Output Format**
  - Support 8-channel outputs
  - Hardware down-mixed 6-channel to 2-channel or 4-channel
  - Center and LFE channel swapping
  - Alternative Line-Level outputs at surround output

- 96KHz S/PDIF output
- Direct CD input to S/PDIF output

Added-on Functions

- Integrates headphone amplifier with mute
- Dual microphones supporting Karaoke mixing

Extension Control

- 4-bit 3D depth control
- Support EAPD control
- Supports GPIO pins control
- Selectable clock sources
- Driver support Magic 5.1

Convenient Design

- Flexible Jack-detect design
- Built-in accurate PLL for saving an external crystal
- Built-in Smart 5.1.

Power

- Low power consumption mode

- 3.3V or 5V analog, 3.3V digital power supply

❑ **Package**

- 48-Pin LQFP Package

1.3.8 System Flash Memory (BIOS)

❑ **2M bit Flash memory**

❑ **Flashed by 5V only**

❑ **User can upgrade the system BIOS in the future just running flash program.**

1.3.9 Memory System

❑ **64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs**

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 333Mb/s and 400Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V

8399 N/B Maintenance

- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6 μs (MT4VDDT864H, MT8VDDT1664HD), 7.8125 μs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2700, PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.3.10 LAN: VT6103L 10Base-T/100Base-TX Ethernet PHY

The VT6103L is a Physical Layer device for Ethernet 10BASE-T and 100BASE-TX using category 5 Unshielded, Type 1 Shielded, and Fiber Optic cables. This VLSI device is designed for easy implementation of 10 / 100 Mb/s Fast Ethernet LANs. It interfaces to a MAC through an MII interface ensuring interoperability between products from different vendors.

- **Product Features**
  - Single Chip 100Base-TX/10Base-T Physical Layer solution
  - Dual Speed – 100/10 Mbps
  - Half And Full Duplex
  - MII Interface to Ethernet Controller
  - MII Interface to Configuration & Status
  - Optional Repeater Interface
  - Auto Negotiation : 10/100, Full/Half Duplex
  - Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Standards
  - On Chip Wave Shaping – No External Filters Required
  - Adaptive Equalizer
  - Baseline Wander Correction
  - LED Outputs

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- Link Status
- Duplex status
- Speed Status
- Collision
- 48 Pin SSOP Package

1.4 Other Functions

1.4.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Wireless lan on/off	Wireless Lan on ->off
Fn + F2	Reserve	
Fn + F3	Volume down	Adjust Audio volume down
Fn + F4	Volume up	Adjust Audio volume up
Fn + F5	Display switch	LCD->CRT->LCD&CRT, TV-out will be not TV present. TV->CRT->TV&CRT, TV-out is connected.
Fn + F6	Brightness down	Adjust LCD panel backlight darkness.
Fn + F7	Brightness up	Adjust LCD panel backlight lightness.
Fn + F8	MAX brightness toggle	Toggle LCD brightness maximum or user setting
Fn + F9	Reserved	
Fn + F10	Battery Low warning beep toggle	Toggle to enable/mute the “Battery Low Warning” beep sound
Fn + F11	LCD panel toggle on/off	Toggle LCD panel on or off.
Fn + F12	System sleep	System sleep button function.

1.4.2 Power on/off/Suspend/Resume Button

1.4.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.4.2.2 ACPI Mode

At ACPI mode, power button behavior was set by windows power management control panel. You could set “standby” or “power off” to power button function. Continue pushing power button over 4 seconds will force system off at ACPI mode. There is no sleep button on this machine.

1.4.3 Lid Switch

System automatically provides a Keyboard cover state through PS2 to relative application when user closes the Keyboard cover.

1.4.4 LED Indicators

System has some status LED indicators to display system activity,.

1.4.4.1 Three LED Indicators on Display Housing/Cover:

From left to right that indicates, AC Power/Battery Power and Battery Charger

- **AC Power:**

  This LED lights green when AC powers to the notebook, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries.

- **Battery Power:**

  This LED lights green when Battery powers to the notebook, and flash (on 1second, off 1 second) when Suspend to DRAM is active using Battery power. The LED is off when the notebook is off or powered by AC power.

- **Battery Charge Status:**

  During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged. When battery charging error, it will flash orange light.

- **WLAN RF Status (BTO: Wireless LAN only):**

  This LED indicates WLAN RF module power status. User could use Fn+F1 to enable or disable RF.

1.4.4.2 Five LED Indicators above Front Side Housing:

From left to right that indicates CD, HDD, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.4.5 Fan Power on/off Management

l FAN is controlled by Embedded Controller Winbond W83L950D. Thermal with hardware monitor to sense CPU temperature and EC control fan on/off.

1.4.6 CMOS Battery

- CR2032 3V 220mAh lithium battery
- When AC in or system main battery inside, CMOS battery will consume no power
- AC or main battery not exists, CMOS battery life is at lest 10 years
- Battery was put in battery holder, can be replaced.

1.4.7 I/O Port

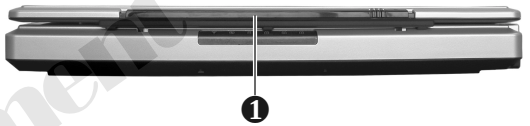
- One 3 pins AC power socket
- One CRT monitor
- One S-Video TV out (PAL/NTSC)
- Six USB 2.0 ports for all USB devices
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN
- Headphone out Jack
- Microphone Input Jack
- One Cardbus Sockets for one type II PC card extension

2. System View and Disassembly

2.1 System View

2.1.1 Front View

❶ Top Cover Latch

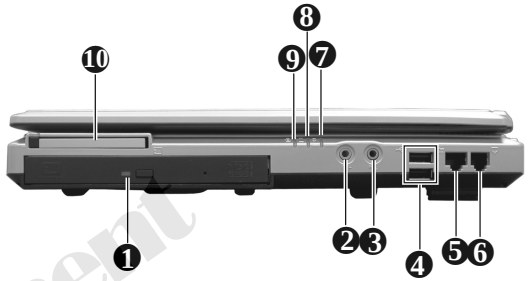


2.1.2 Left-side View

❶ Lock
❷ Ventilation Openings

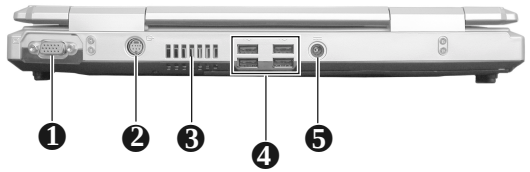
2.1.3 Right-side View

❶ CD/DVD driver
❷ Line out jack
❸ MIC in jack
❹ USB port *2
❺ RJ-45 connector
❻ RJ-11 connector
❼ AC Power Indicator
❽ Battery Power Indicator
❾ Battery Charge Indicator
❿ PC Card slot

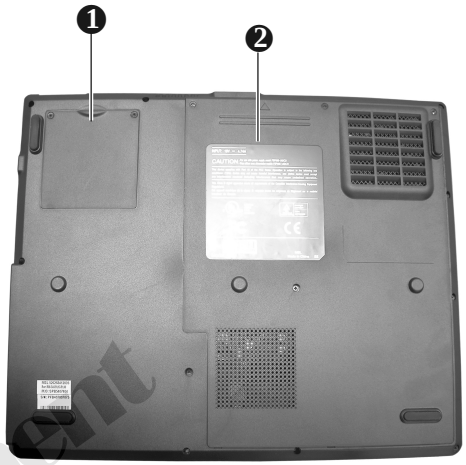


2.1.4 Rear View

❶ VGA port
❷ S-Video output connector
❸ Ventilation Openings
❹ USB port *4
❺ Power connector

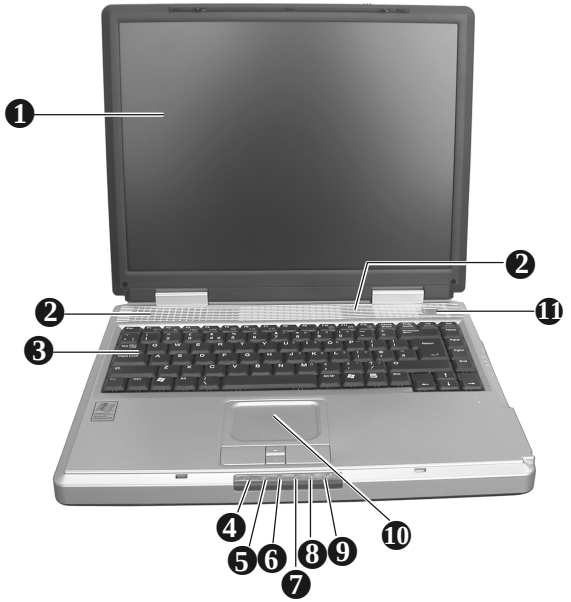


2.1.5 Bottom View



❶ Wireless Card cover
❷ CPU

2.1.6 Top-open View

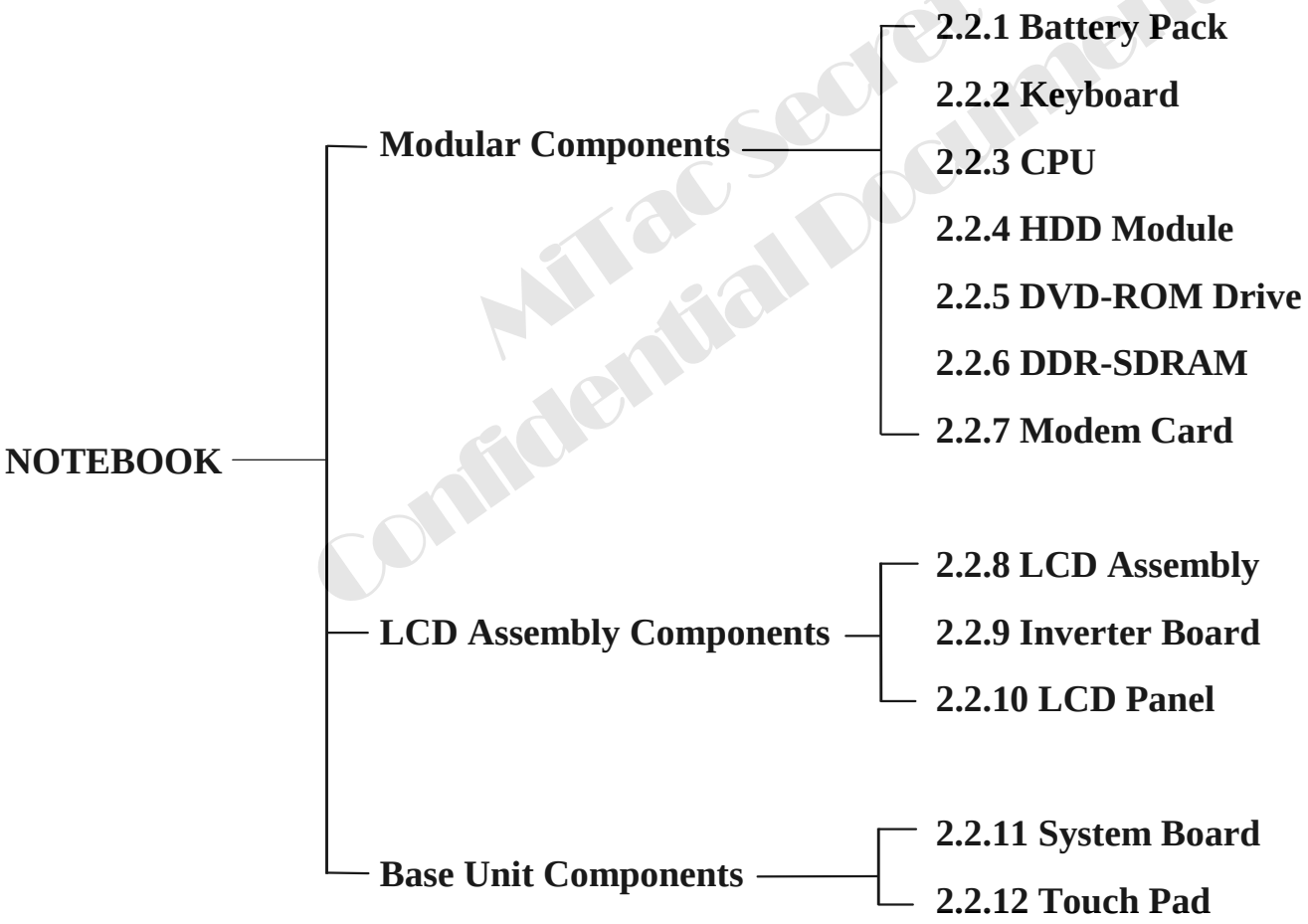


❶ LCD Screen
❷ Stereo set
❸ Keyboard
❹ Caps Lock
❺ Wireless Card Indicator
❻ CD/DVD-Rom Indicator
❼ HDD Indicator
❽ Num Lock
❾ Caps Lock
❿ Scroll Lock
⓫ Power Button

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Remove the four screws, then remove the CPU cover. (Figure 2-1)
3. Put up the battery pack, then free the battery pack. (Figure 2-2)

Figure 2-1 Remove the four screws

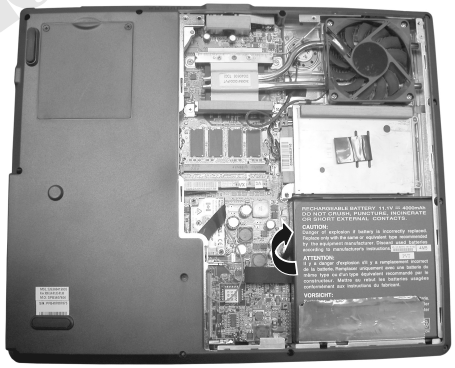


Figure 2-2 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Replace the CPU cover and secure the four screws.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Open the top cover.
3. Loosen the five latches locking the keyboard. (Figure 2-3)

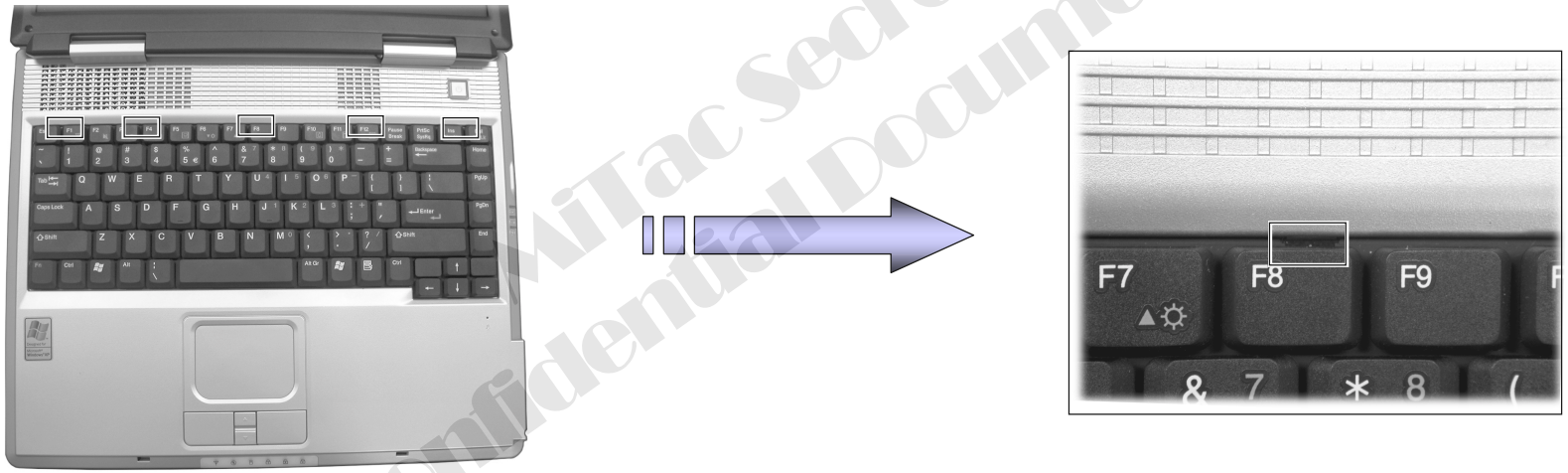


Figure 2-3 Loosen the five latches

4. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard. (Figure 2-4)

Figure 2-4 Lift up the keyboard and disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back.
2. Replace the keyboard into place and fasten the five latches.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Disconnect the fan's power cord from system board and remove five screws that secure the heatsink upon the CPU, Then free the heatsink. (Figure 2-5)
3. To remove the existing CPU, lift the socket arm up to the vertical position. (Figure 2-6)

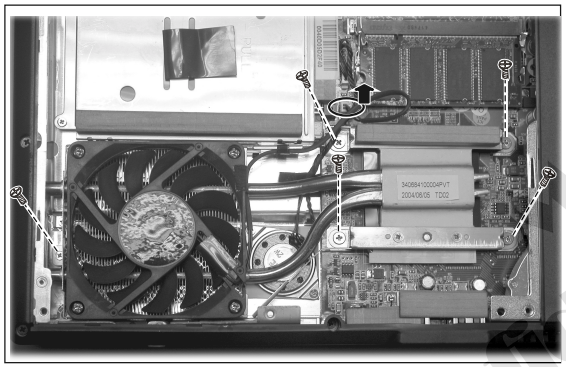


Figure 2-5 Free the heatsink

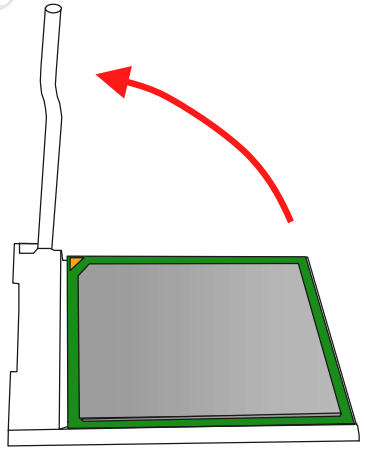


Figure 2-6 Disconnect the cable

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left.
2. Reconnect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with five screws.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the HDD module and slightly lift up HDD module. (Figure 2-7)
3. Remove four screws to separate the hard disk drive from the bracket, free the hard disk driver. (Figure 2-8)

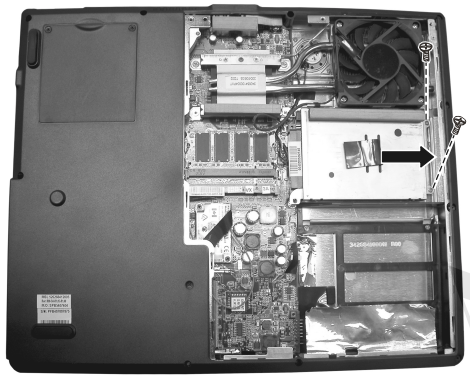


Figure 2-7 Remove HDD module

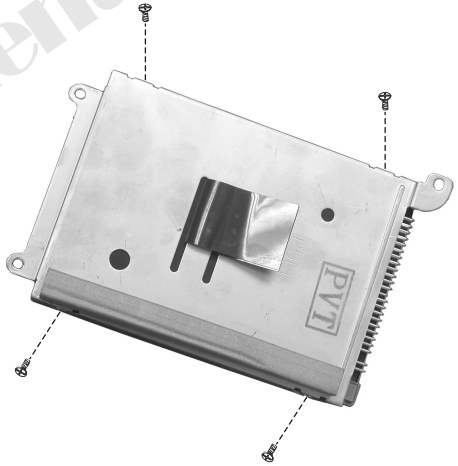


Figure 2-8 Free the HDD driver

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with two screws.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove one screw fastening the CD/DVD-ROM drive. (Figure 2-9)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out(❷). (Figure 2-9)

Figure 2-9 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Pull the retaining clips outwards (❶) and remove the DDR-SDRAM (❷). (Figure 2-10)

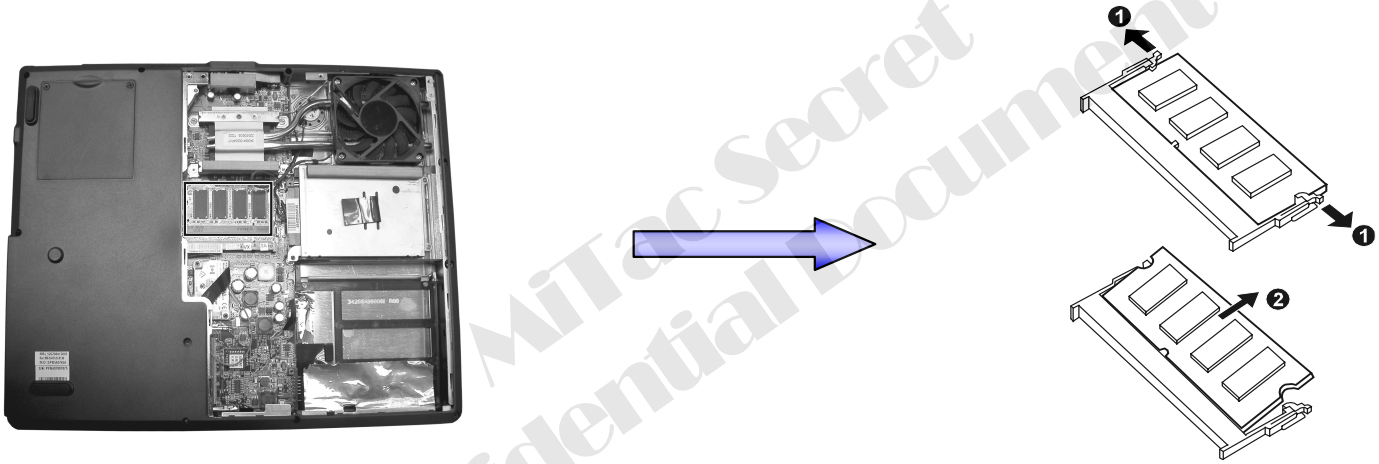


Figure 2-10 Remove the DDR-SDRAM

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the DDR into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.7 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the two screws. (Figure 2-11)
3. Disconnect the cable from the system board, Then free the modem card. (Figure 2-12)

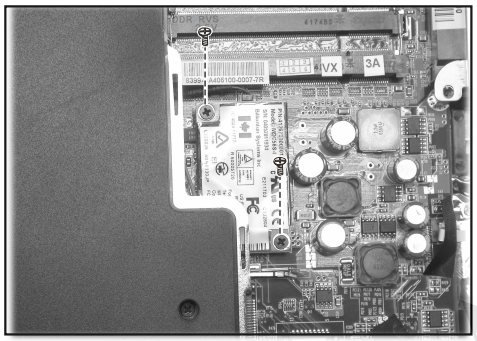


Figure 2-11 Remove the two screws

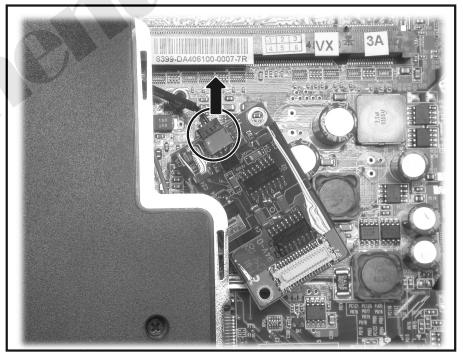


Figure 2-12 Disconnect the cable

Reassembly

1. Fit the modem card, Then reconnect the cable and secure with two screws.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.8 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.2.1 and 2.2.2 Disassembly)
2. Remove two hinge covers. (Figure 2-13)
3. Carefully put the notebook upside down. Remove the two screws fastening the wireless cover. (Figure 2-14)

Figure 2-13 Remove two hinge covers

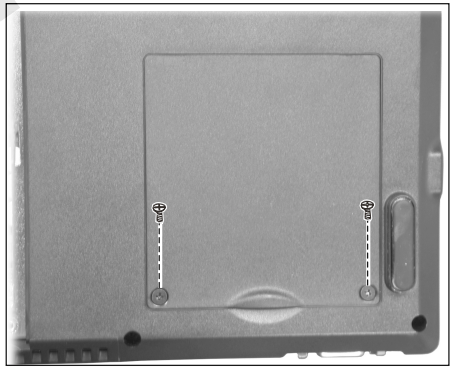


Figure 2-14 Remove the two screws

4. Disconnect the LCD cable from the system board and detach the antenna. (Figure 2-15)
5. Remove the four screws and put up the LCD assembly, then free the LCD assembly. (Figure 2-16)

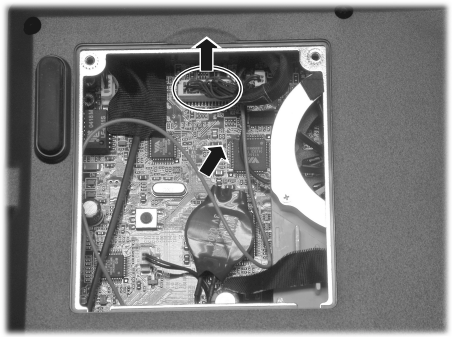


Figure 2-15 Disconnect the LCD cable

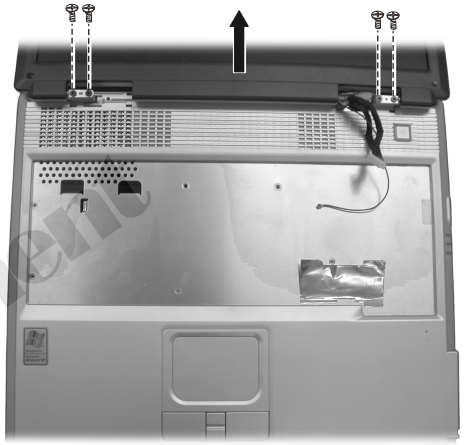


Figure 2-16 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws, then fit the antenna.
2. Reconnect the one cable to the system board, Then replace the wireless cover and secure two screws.
3. Replace the two hinge covers.
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.9 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove two screws and rubbers on the corners of the LCD panel. (Figure 2-17)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the one screw fastening the inverter board. (Figure 2-18)

Figure 2-17 Remove LCD cover

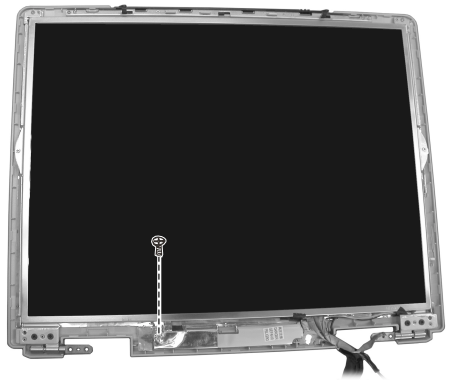


Figure 2-18 Remove the one screw

5. To remove the inverter board on the lower part of the LCD housing , disconnect two cables. (Figure 2-19)

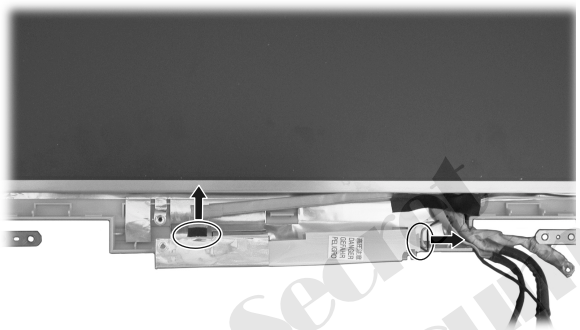


Figure 2-19 Remove the inverter board

Reassembly

1. Reconnect the two cables. Fit the inverter board back into place and secure with one screw.
2. Replace the LCD cover and secure with two screws and rubbers.
3. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.10 LCD Panel

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to sections 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove the LCD cover. (Refer for two steps 2,3 of section 2.2.9 Disassembly)
3. Remove the eight screws fastening the LCD panel and detach the cable, Then lift it up. (Figure 2-20)
4. Remove the five screws fastening the LCD brackets. (Figure 2-21)

Figure 2-20 Remove the eight screws and detach the cable

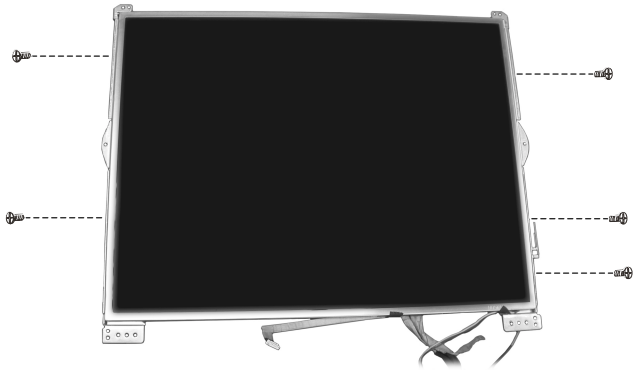


Figure 2-21 Remove the five screws

5. Disconnect the cable and free the LCD panel. (Figure 2-22)

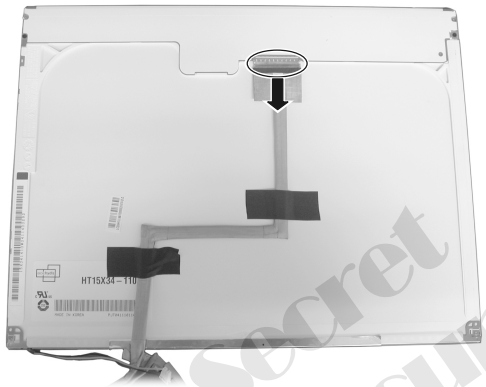


Figure 2-22 Free the LCD panel

Reassembly

1. Reconnect the cable, then replace the LCD brackets and secure with five screws.
2. Fit the LCD panel back into place and secure with eight screws, then reconnect the cable to the inverter board.
3. Replace the LCD cover and secure with two screws and rubbers. (Refer to section 2.2.9 Reassembly)
4. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
5. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM, modem card and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.8 Disassembly)
2. Remove the four screws. (Figure 2-23)
3. Remove the eleven screws and free the housing. (Figure 2-24)

Figure 2-23 Remove the four screws

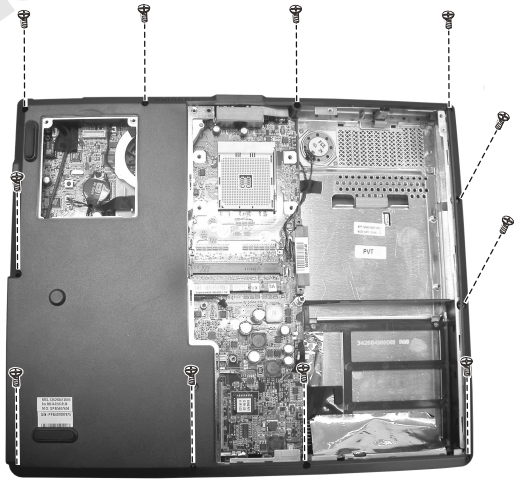


Figure 2-24 Remove the eleven screws

4. Remove the three screws and lift up the housing's shielding. (Figure 2-25)
5. Disconnect the speaker's cable and the touch pad's cable, Then remove the one screw and four hex nuts. Now you can lift up the system board. (Figure 2-26)

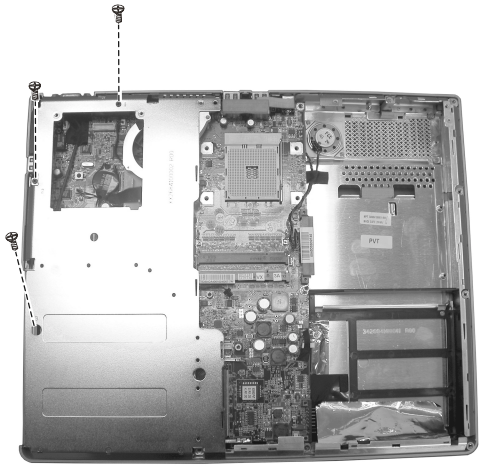


Figure 2-25 Remove the three screws

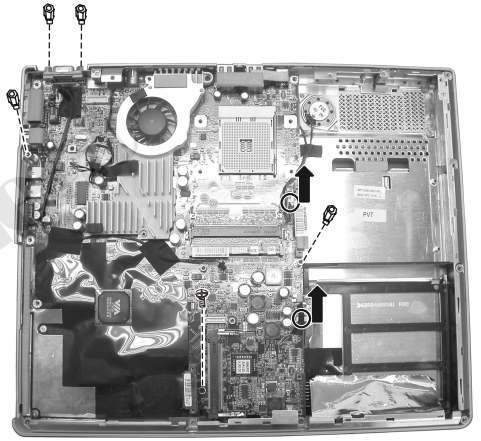


Figure 2-26 Free the system board

Reassembly

1. Replace the system board into the top cover and secure with one screw and four hex nuts.
2. Reconnect the touch pad's cable, the speaker's cable.
3. Replace the housing's shielding and secure with three screws.
4. Replace the housing and secure with fifteen screws.
5. Replace the LCD assembly, modem card, DDR-SDRAM, CD/DVD-ROM, HDD, CPU, keyboard and battery pack. (See sections 2.2.8, 2.2.6, 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.12 Touch Pad

Disassembly

1. Remove the system board. (See section 2.2.11 Disassembly)
2. Remove the two screws and disconnect the cable, then free the touch pad. (Figure 2-27)

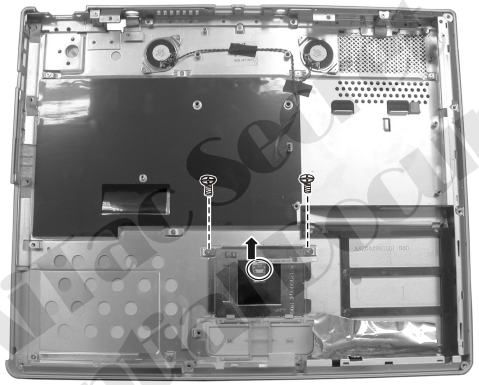


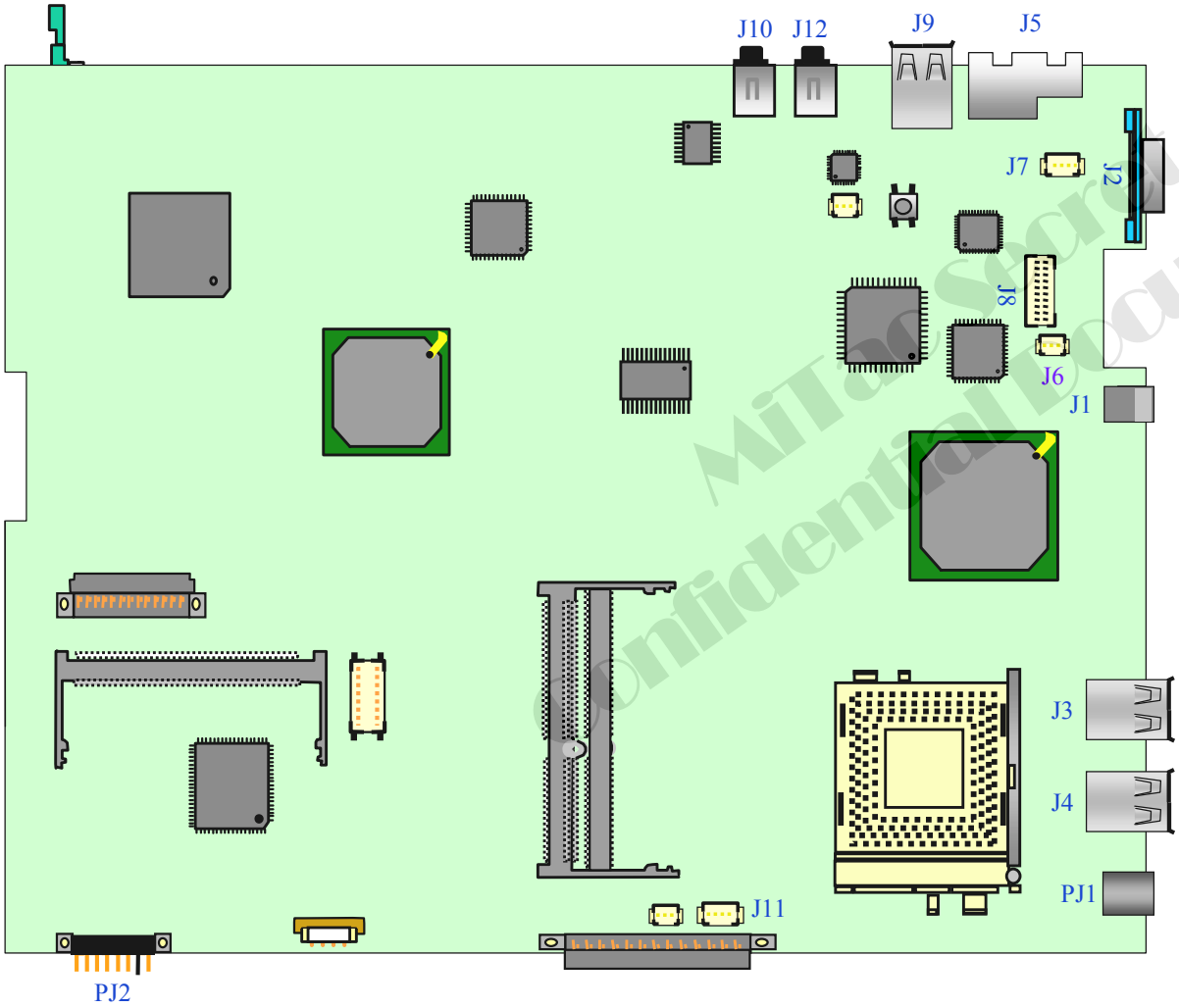
Figure 2-27 Free the touch pad

Reassembly

1. Replace the touch pad and reconnect the cable.
2. Replace the touch pad shielding and secure with two screws.
3. Reassemble the notebook. (See the previous sections Reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board – A(1)

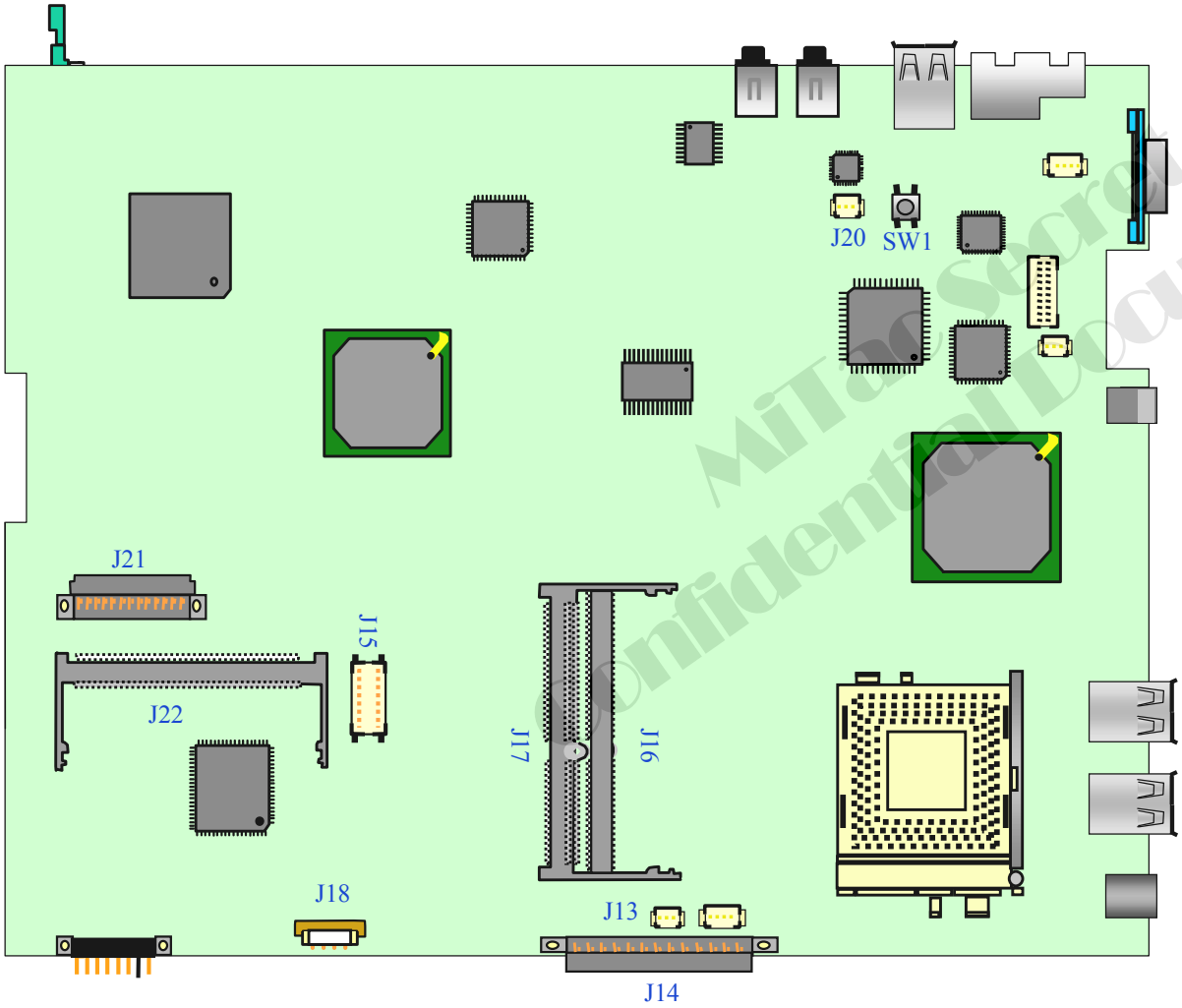


- PJ1 : AC Power Jack
- PJ2 : Battery Connector
- J1 : S-Video Port
- J2 : External VGA Connector
- J3, J4, J9 : USB Port Connector
- J5 : RJ11 & RJ45 Connector
- J6 : North Bridge Fan Connector
- J7 : MDC Jump Wire Connector
- J8 : LCD Connector
- J10 : Microphone Jack
- J11 : CPU Fan Connector
- J12 : Line Out Jack

------ To next page ------

3. Definition & Location of Connectors / Switches

3.1 Mother Board – A(2)



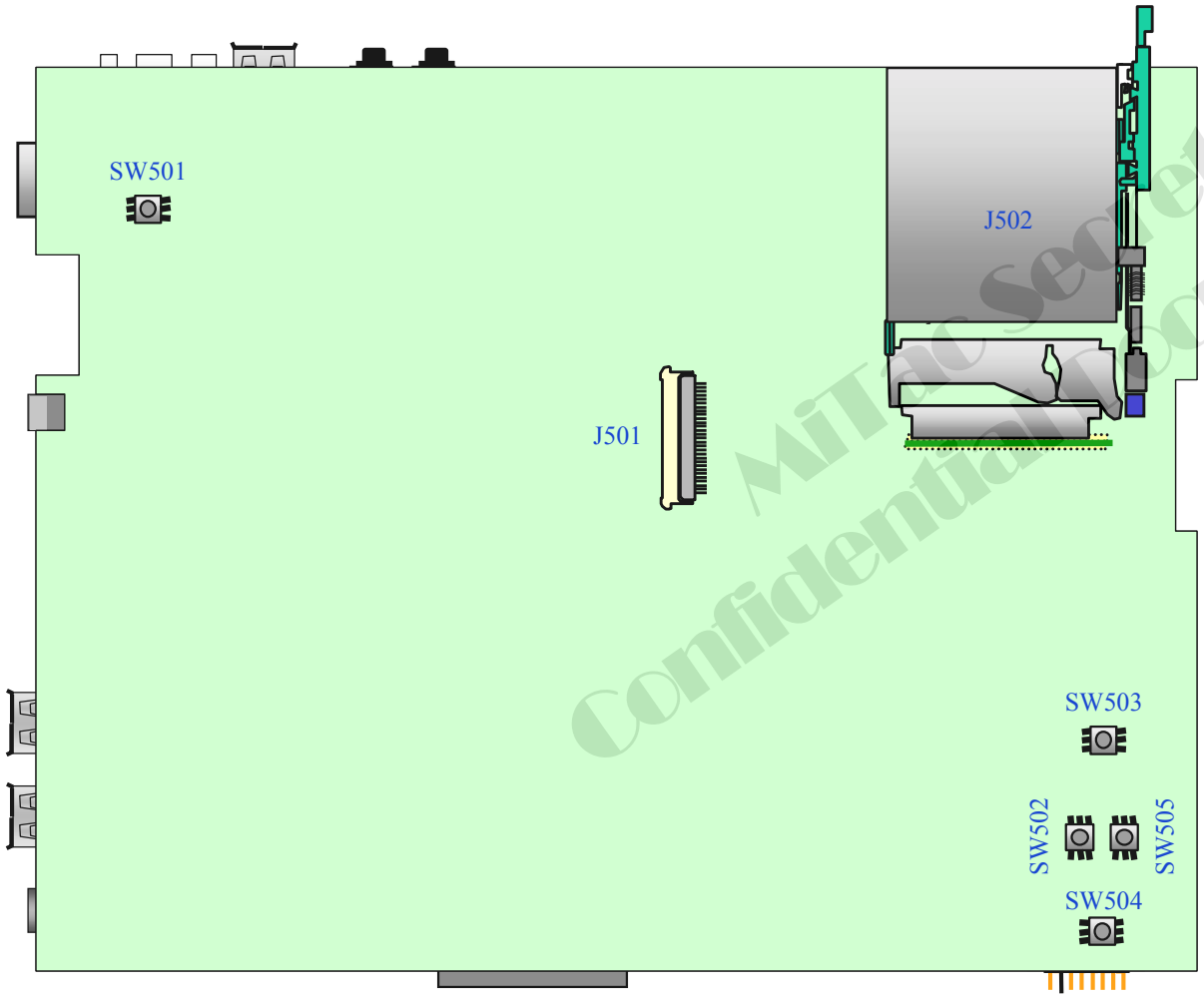
------ Continue to previous page ------

- J13 : Internal Speaker Connector
- J14 : Primary EIDE Connector
- J15 : MDC Board Connector
- J16,J17 : Extend DDR SDRAM Socket
- J18 : Touch-Pad Connector
- J20 : RTC Battery Connector
- J21 : Secondary IDE Connector
- J22 : Mini-PCI Socket

- SW1 : H8 Reset Button

3. Definition & Location of Connectors / Switches

3.2 Mother Board - B

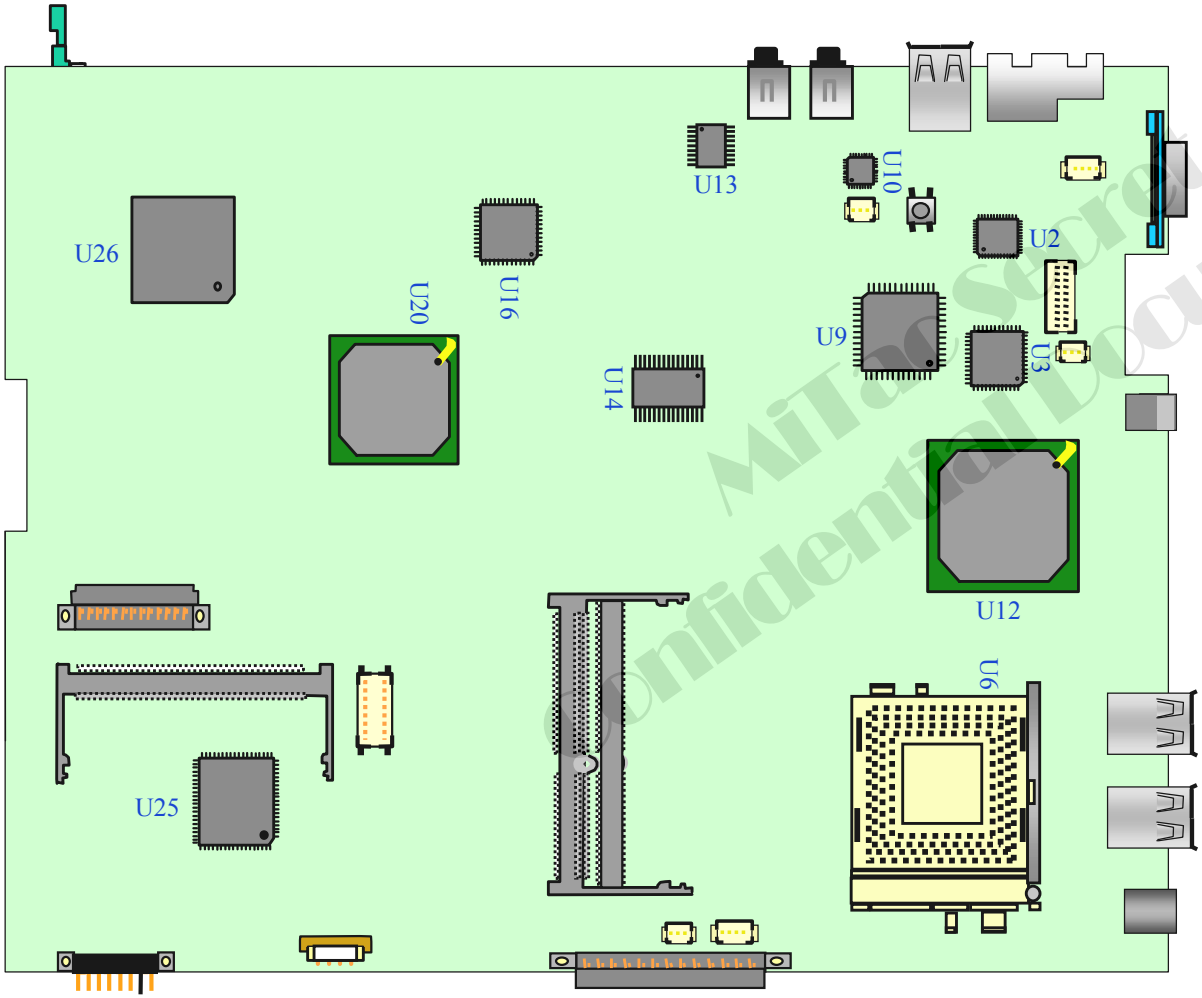


- J501 : Internal Keyboard Connector
- J502 : PCMCIA Card Socket

- SW501 : Power Button
- SW502 : Touch-Pad Up Button
- SW503 : Touch-Pad Right Button
- SW504 : Touch-Pad Left Button
- SW505 : Touch-Pad Down Button

4. Definition & Location of Major Components

4.1 Mother Board - A



- U2 : VT6103L LAN Controller
- U3 : TV Encoder(VIA_VT1622)
- U6 : AMD CPU Socket
- U9 : LVDS Encoder(VIA_VT1634)
- U10 : VT1617A Audio Codec
- U12 : VIA_K8N800 North Bridge
- U13 : G1428 Sounder Amplifier
- U14 : ICS950403 Clock Generator
- U16 : KBC (W83L950D)
- U20 : VIA_VT8235CD South Bridge
- U25 : LPC BIOS ROM
- U26 : CB1410 PCMCIA Controller

5. Pin Descriptions of Major Components

5.1 AMD Mobile Athlon 64(ClawHammer) Processor(1)

DDR SDRAM Memory Interface Pins

Signal Name	Type	Description
MEMCLK_H/L[7]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 0 for unbuffered DIMMs.1
MEMCLK_H/L[6]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 1 for unbuffered DIMMs.1
MEMCLK_H/L[5]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 0 for unbuffered DIMMs.1
MEMCLK_H/L[4]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 1 for unbuffered DIMMs.1
MEMCLK_H/L[3]	O-IOD	Differential DDR SDRAM clock to DIMM 3 for registered DIMMs.1
MEMCLK_H/L[2]	O-IOD	Differential DDRS DRAM clock to DIMM 2 for registered DIMMs.1
MEMCLK_H/L[1]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 1 for unbuffered DIMMs, or DIMM 1 for registered DIMMs.1
MEMCLK_H/L[0]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 0 for unbuffered DIMMs, or DIMM 0 for registered DIMMs.1
MEMCKEA MEMCKEB	O-IOS	Clock Enables to DIMMs. Used to gate clocks for power management functionality.1
MEMDQS[17:0]	B-IOS	DRAM Data Strobes synchronous with MEMDATA and MEMCHECK during DRAM read and writes.1
MEMDATA[63:0]	B-IOS	DRAM Interface Data Bus
MEMCHECK[7:0]	B-IOS	DRAM Interface ECC Check Bits
MEMCS_L[7:0]	O-IOS	DRAM Chip Selects 1
MEMRASA_L MEMRASB_L	O-IOS	DRAM Row Address Select. MEMRASA_L and MEMRASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMCASA_L MEMCASB_L	O-IOS	DRAM Column Address Select. MEMCASA_L and MEMCASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMWEA_L MEMWEB_L	O-IOS	DRAM Write Enable. MEMWEA_L and MEMWEB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMADDA[13:0] MEMADDB[13:0]	O-IOS	DRAM Column/Row Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes, the two copies are inverted from each other (except A[10] which is used for auto-precharge) to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1

DDR SDRAM Memory Interface Pins (Continued)

Signal Name	Type	Description
MEMBANKA[1:0] MEMBANKB[1:0]	O-IOS	DRAM Bank Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes the two copies are inverted from each other to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1
MEMRESET_L	O-IOS	DRAM Reset pin for Suspend-to-RAM power management mode. This pin is required for registered DIMMs only.
MEMVREF	VREF	DRAM Interface Voltage Reference 1
MEMZP	A	Compensation Resistor tied to VSS 1
MEMZN	A	Compensation Resistor tied to 2.5 V 1

Note: For connection details and proper resistor values, see the AMD Athlon™ 64 Processor Motherboard Design Guide, order# 24665.

HyperTransport™ Technology Pin Descriptions

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT	Link 0 Clock Input
L0_CTLIN_H/L[1:0]	I-HT	Link 0 Control Input 2
L0_CADIN_H/L[15:0]	I-HT	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT	Link 0 Clock Outputs
L0_CTLOUT_H/L[1:0]	O-HT	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT	Link 0 Command/Address/Data Outputs
L0_REF1	A	Compensation Resistor to VLDT 1
L0_REF0	A	Compensation Resistor to VSS 1

Note: 1.These pins are used in an alternating fashion to compensate R TT by internal comparison to 3/4 VLDT and 1/4 VLDTand compensate R ON by comparison to each other around 1/2 VLDT.
For proper resistor value, see theAMD Athlon™ 64 Processor Motherboard Design Guide, order# 24665.
2.The unused L0_CTLIN_H/L[1] pins must be properly terminated such that the true pin is pulled High and thecomplement is pulled Low. Refer to the AMD Athlon™ 64 Processor Motherboard Design Guide, order# 24665, for details.

5.1 AMD Mobile Athlon 64(ClawHammer) Processor(2)

Miscellaneous Pin Descriptions

Signal Name	Type	Description
RESET_L	I-IOS	System Reset
PWROK	I-IOS	Indicates that voltages and clocks have reached specified operation
LDTSTOP_L	I-IOS	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency.
VID[4:0]	O-IOS	Voltage ID to the regulator
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output, asserted at nominal temperature of 125 ℃.
COREFB_H/L	A	Differential feedback for VDD Power Supply
VDDIOFB_H/L	A	Differential feedback for VDDIO Power Supply
CORE_SENSE	A	VDD voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VTT_SENSE	A	VTT voltage monitor pin
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDD	S	Core power supply
VDDIO	S	DDR SDRAM I/O ring power supply
VLDT_A VLDT_B	S	HyperTransport™ I/O ring power supply for side A and side B of the package
VTT_A VTT_B	S	VTT regulator voltage for side A and side B of the die
VSS	S	Ground

Debug Pin Descriptions

Signal Name	Type	Description
DBREQ_L	I-IOS	Debug Request
DBRDY	O-IOS	Debug Ready

JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IOS	JTAG Clock
TMS	I-IOS	JTAG Mode Select
TRST_L	I-IOS	JTAG Reset
TDI	I-IOS	JTAG Data Input
TDO	O-IOS	JTAG Data Output

Clock Pin Descriptions

Signal Name	Type	Description
CLKIN_H/L	I-IOD	200-MHz PLL Reference Clock
FBCLKOUT_H/L	O-IOD	Core Clock PLL 200-MHz Feedback Clock

5.2 VIA K8N800 North Bridge(1)

AGP Bus Interface

Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GDS assertion for AGP-style transfers and with GFARME# assertion for PCI-style transfers.
GC#BE[3:0] (GCBE[3:0]# for 4x mode)	AC7 AD11 AF11 AD15	IO	**Command / Byte Enable.** (Interpreted as GC/BE# for AGP 2x/4x and GC#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn™t used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to io0000lt during the return of AGP read data. For PCI cycles, commands are driven with GFARME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	AC16	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH / GPIPE#**GDBIL**	AC5 AC4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Not**e: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GADSTB0F(GADSTB0 for 4x), **GADSTB0S**(GADSTB0# for 4x)	AE15 AF15	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x mode. For 8x transfer mode, GDS0 is interpreted as GDS0F (i1Firstl. strobe) and GDS0# as GDS0S (iSSecondl. strobe).

AGP Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GADSTB1F(GADSTB1 for 4x), **GADSTB1S**(GADSTB1# for 4x)	AE7 AF7	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode. For 8x transfer mode, GDS1 is interpreted as GDS1F (iSFirstle strobe) and GDS1# as GDS1S (iSSecondld strobe).
GFRAME(GFRAME# for 4x)	AC9	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GIRDY(GIRDY# for 4x)	AC10	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when the initiator is ready for data transfer.
GTRDY(GTRDY# for 4x)	AC14	IO	**Target Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when the target is ready for data transfer.
GDEVSEL(GDEVSEL# for 4x mode)	AC11	IO	**Device Select (PCI transactions only).** This signal is driven by the North Bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.

5.2 VIA K8N800 North Bridge(2)

AGP Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
AGP8XDT#	Y2	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode
GRBF(GRBF# for 4x)	AD6	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GWBF(GWBF# for 4x)	AC1	I	**Write Buffer Full.**
GSBA[7:0]# (GSBA[7:0] for 4x)	(see pin list)	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
GSBSTBF(GSBSTB for 4x), **GSBSTBS**(GSBSTB# for 4x)	AF1 AE1	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF (iBFirstlr strobe) and GSBSTBS (iBSecondl) strobe). These signals are interpreted as GSBSTB & GSBSTB# for AGP4x.
GST[2:0]	AB1 AA1 AA2	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (North Bridge logic) and inputs to the master (graphics controller).

AGP Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GSTOP(GSTOP# for 4x)	AC12	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
GREQ(GREQ# for 4x)	Y1	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT(GGNT# for 4x)	AA3	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR(GSERR# for 4x)	AC15	IO	**AGP System Error.**

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see isAdditional 12C InterfaceslÓo, and display pin description tables later in this document for more information).
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see isAdditional I2C Interfacesll and display pin description tables later in this document for more information).
Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.
Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)
Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn™t used in 8x mode).
Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

5.2 VIA K8N800 North Bridge(3)

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD7, **VAD6,** **VAD5**, **VAD**4, **VAD**3, **VAD**2, **VAD**1, **VAD0**	AF25 AD24 AF20 AE19 AE24 AF24 AD21 AD20	IO IO IO IO IO IO IO IO	**Address / Data Bus.** Also used to pass strap information from the South Bridge to the North Bridge (the actual straps are on the indicated South Bridge pin and that information is passed to the North Bridge at reset time via the VAD pins).
VPAR	AF19	IO	**Parity.**
VBE#	AE21	IO	**Byte Enable.**
UPCMD	AF26	I	**Command from Client (South Bridge) to Host (North Bridge).**
UPSTB	AE23	I	**Strobe from Client to Host.**
UPSTB#	AF23	I	**Complement Strobe from Client to Host.**
DNCMD	AD23	O	**Command from Host (North Bridge) to Client (South Bridge).**
DNSTB	AF22	O	**Strobe from Host to Client.**
DNSTB#	AD22	O	**Complement Strobe from Host to Client.**

SMB / I 2 C Interface

Signal Name	Pin #	I/O	Signal Description
SBPLCLK / GIRDY	AC10	I/O	**I 2 C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).**
SBPLDAT / GC#BE1	AF11	I/O	**I 2 C Serial Bus Data for Panel (Muxed on AGP Bus Pins).**
SBDDCCLK / GREQ	Y1	I/O	**I 2 C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).**
SBDDCDAT / GGNT	AA3	I/O	**I 2 C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).**
SPCLK[2:1]	C2, P2	IO	**Serial Port (SMB/I 2 C) Clocks.** Clocks for serial data transfer. SPCLK1 is typically used for I 2 C communications. SPCLK2 is typically used for CRT Display DDC communications.
SPDAT[2:1]	C1, P1	IO	**Serial Port (SMB/I 2 C) Data.** Data signals for serial data transfer. SPDAT1 is typically used for I 2 C communications. SPDAT2 is typically used for CRT Display DDC communications.

Dedicated Digital Video Port 0 (DVP0) – TMDS Interface

Signal Name	Pin #	I/O	Signal Description
DVP0D11/ TVD11 **DVP0D10**/ TVD10 **DVP0D9** / TVD9 **DVP0D8** / TVD8 **DVP0D7** / TVD7 **DVP0D6** / TVD6 **DVP0D5** / TVD5 **DVP0D4** / TVD4 **DVP0D3** / TVD3 **DVP0D2** / TVD2 **DVP0D1** / TVD1 **DVP0D0** / TVD0	M1 M3 M2 L1 M4 L3 L2 K1 L4 K3 K2 J1	O	**Digital Video Port 0 Data.** Default output drive is 8 mA. 16 mA may be selected via SR3D[6]=1. NOTE: DVP0D[6:0] are also used for power-up reset straps for the embedded graphics controller. Check the Strap Pin table for details.
DVP0HS / TVHS	N4	O	**Digital Video Port 0 Horizontal Sync.** Internally pulled down.
DVP0VS / TVVS	N3	O	**Digital Video Port 0 Vertical Sync.** Internally pulled down.
DVP0DE / TVDE	N1	O	**Digital Video Port 0 Data Enable.** Internally pulled down.
DVP0DET / TVCLKR	P4	I	**Digital Video Port 0 Display Detect.** If VGA register 3C5.12[5]=0, 3C5.1A[5] will read 1 if display is connected. Tie to GND if not used.
DVP0CLK / TVCLK	P3	O	**Digital Video Port 0 Clock.** Internally pulled down.

The terminology ie3C5.nnlg above refers to the VGA iGSequencerl. registers at I/O port 3C5 index "nn"

CRT Interface

Signal Name	Pin #	I/O	Signal Description
AR **AG** **AB**	B3 A3 A2	AO AO AO	**Analog Red.** Red output to CRT monitor. **Analog Green.** Green output to CRT monitor. **Analog Blue.** Blue output to CRT monitor.
RSET	C4	AI	**CRT Output Reference Resistor.** Tie to GNDRGB through an external 90.9 ±1% resistor to control the "RGB" RAMDAC full-scale current.
HSYNC	A1	O	**Horizontal Sync.** Digital output to CRT monitor.
VSYNC	B1	O	**Vertical Sync.** Digital output to CRT monitor.

5.2 VIA K8N800 North Bridge(4)

Dedicated Digital Video Port 0 (DVP0) - TV Encoder Interface

Signal Name	Pin #	I/O	Signal Description
TVD11 / DVP0D11 **TVD10** / DVP0D10 **TVD9** / DVP0D9 **TVD8** / DVP0D8 **TVD7** / DVP0D7 **TVD6** / DVP0D6 **TVD5** / DVP0D5 **TVD4** / DVP0D4 **TVD3** / DVP0D3 **TVD2** / DVP0D2 **TVD1** / DVP0D1 **TVD0** / DVP0D0	M1 M3 M2 L1 M4 L3 L2 K1 L4 K3 K2 J1	O	**TV Encoder 0 Data.** To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high. Note: One TV Encoder interface is supported through either DVP0 or GDVP1.
TVHS / DVP0HS	N4	O	**TV Encoder 0 Horizontal Sync.** Internally pulled down.
TVVS / DVP0VS	N3	O	**TV Encoder 0 Vertical Sync.** Internally pulled down.
TVDE / DVP0DE	N1	O	**TV Encoder 0 Display Enable.** Internally pulled down.
TVCLKR / DVP0DET	P4	I	**TV Encoder 0 Clock Return.** Input from TV encoder. Internally pulled down.
TVCLK / DVP0CLK	P3	O	**TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A or VT1622AM for driving a TV set.
I/O pads for the pins on this page are powered by VCCGFX (3.3V I/O).

AGP-Multiplexed Digital Video Port 1 (GDVP1) – TMDS Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
GDVP1D11	GC#BE3	AC7	O	**Data.**
GDVP1D10	GD26	AE6		
GDVP1D9	GD24	AF6		
GDVP1D8	GD30	AE4		
GDVP1D7	GD28	AF5		
GDVP1D6	GD29	AF4		
GDVP1D5	GSBA4#	AF2		
GDVP1D4	GD27	AD5		
GDVP1D3	GSBA5#	AD3		
GDVP1D2	GSBSTBS	AE1		
GDVP1D1	GSBSTBF	AF1		
GDVP1D0	GSBA2#	AD1		
GDVP1HS	GSBA3#	AD2	O	**Horizontal Sync.**
GDVP1VS	GSBA0#	AC2	O	**Vertical Sync.**
GDVP1DE	GSBA1#	AC3	O	**Data Enable.**
GDVP1DET	GD31	AD4	I	**Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a display is connected. Tie to GND if not used.
GDVP1CLK	GSBA6#	AE3	O	**Clock.**
GDVP1CLK#	GSBA7#	AF3	O	**Clock Complement.**

The GDVP1 Digital Video Port is supported through multiplexing its interface signal pins with AGP pins. GDVP1 can be configured as either a TMDS transmitter interface port or a TV Encoder interface port. (see the TMDS Transmitter Interface and TV Encoder Interface pin lists below for details).

Analog Power / Ground

Signal Name	Pin #	I/O	Signal Description
VCCATX	C22	P	**Analog Power for HT Transmit.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise.
GNDATX	C21	P	**Analog Ground for HT Transmit.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise.
VCCARX	E25	P	**Analog Power for HT Receive.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise.
GNDARX	E26	P	**Analog Ground for HT Receive.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise.

Reference Voltages

Signal Name	Pin #	I/O	Signal Description
VLVREF	AF21	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider (3K §Ù to 2.5V and 1K §Ù to ground). See Design Guide for details.
AGPVREF[1:0]	AC6, AC13	P	**AGP Voltage Reference.** 0.5 VCCQQ (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCCQQ (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details..

5.2 VIA K8N800 North Bridge(5)

AGP-Multiplexed Digital Video Port 1 (GDVP1) – TV Encoder

Signal Name	AGP Name	Pin #	I/O	Signal Description
GTVD11 / GDVP1D11, **GTVD10** / GDVP1D10, **GTVD9** / GDVP1D9, **GTVD8** / GDVP1D8, **GTVD7** / GDVP1D7, **GTVD6** / GDVP1D6, **GTVD5** / GDVP1D5, **GTVD4** / GDVP1D4, **GTVD3** / GDVP1D3, **GTVD2** / GDVP1D2, **GTVD1** / GDVP1D1, **GTVD0** / GDVP1D0	GC#BE3 GD26 GD24 GD30 GD28 GD29 GSBA4# GD27 GSBA5# GSBSTBS GSBSTBF GSBA2#	AC7 AE6 AF6 AE4 AF5 AF4 AF2 AD5 AD3 AE1 AF1 AD1	O	**Data.**
GTVHS / GDVP1HS	GSBA3#	AD2	O	**Horizontal Sync.** Internally pulled down.
GTVVS / GDVP1VS	GSBA0#	AC2	O	**Vertical Sync.** Internally pulled down.
GTVDE / GDVP1DE	GSBA1#	AC3	O	**Display Enable.** Internally pulled down.
GTVCLKR / GDVP1DET	GD31	AD4	I	**Clock In.** Input from TV encoder. Internally pulled down.
GTVCLK / GDVP1CLK	GSBA6#	AE3	O	**Clock Out.** Output to TV encoder. Internally pulled down.
GTVCLK# / GDVP1CLK#	GSBA7#	AF3	O	**Clock Out Complement.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1623 or VT1623M for driving a TV set.
I/O pads for the pins on this page are powered by VCC15AGP (1.5V I/O).

Flat Panel Power Control (Muxed with AGP)

Signal Name	AGP Name	Pin #	I/O	Signal Description
ENAVDD	GST1	AA1	IO	**Enable Panel VDD Power.**
ENAVEE	GST0	AA2	IO	**Enable Panel VEE Power.**
ENABLT	GST2	AB1	IO	**Enable Panel Back Light.**

Note: I/O pads for all pins on this page are powered by VCC15AGP (i.e., 1.5V I/O).

24-Bit / Dual 12-Bit Flat Panel Display Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD23 / FPD0D11, **FPD22 / FPD0D10,** **FPD21 / FPD0D09,** **FPD20 / FPD0D08,** **FPD19 / FPD0D07,** **FPD18 / FPD0D06,** **FPD17 / FPD0D05,** **FPD16 / FPD0D04,** **FPD15 / FPD0D03,** **FPD14 / FPD0D02,** **FPD13 / FPD0D01,** **FPD12 / FPD0D00,** **FPD11 / FPD1D1**1, **FPD10 / FPD1D1**0, **FPD09 / FPD1D0**9, **FPD08 / FPD1D0**8, **FPD07 / FPD1D0**7, **FPD06 / FPD1D0**6, **FPD05 / FPD1D0**5, **FPD04 / FPD1D0**4, **FPD03 / FPD1D0**3, **FPD02 / FPD1D0**2, **FPD01 / FPD1D0**1, **FPD00 / FPD1D00**	GD11 GD13 GD14 GD15 GC#BE2 GD16 GD17 GD18 GD23 GD20 GD22 GADSSTB1 F GD1 GD0 GD3 GD4 GD5 GD6 GD7 GADSTB0F GC#BE0 GADSTB0S GD10 GD12	AE13 AD12 AF12 AE12 AD11 AD10 AE10 AF10 AD8 AF9 AE9 AE7 AD18 AF18 AF17 AD17 AD16 AE16 AF16 AE15 AD15 AF15 AD13 AF13	O	**Flat Panel Data.** For 24-bit or dual 12-bit flat panel display modes. Two FPD interface modes, 24-bit and dual 12-bit, are supported. Strapping pin DVP0D4 is used to select the interface mode to the LVDS transmitter chip: Strap High (3C5.12[4]=1): 24-bit Strap Low (3C5.12[4]=0): Dual 12-bit In in24-bitl] mode, only one set of control pins is required. However, in dual 12-bit mode, the K8N800 Version CD provides two sets of control signals that are required for certain LVDS transmitter chips. In 24-bit mode, two operating modes are supported: 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=0 Double data rate: each rising & falling clock edge transmits a complete 24-bit pixel 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=1 Single data rate: each clock rising edge transmits a complete 24-bit pixel In dual 12-bit mode, 3C5.12[4]=0 & 3x5.88[2] = 1 Each rising and falling clock edge transmits half (12 bits) of two 24-bit pixels
FPHS	GFRAME	AC9	O	**Flat Panel Horizontal Sync.** 24-bit mode or port 0 of dual 12-bit mode.
FPVS	GDEVSEL	AC11	O	**Flat Panel Vertical Sync.** 24-bit mode or port 0 of dual 12-bit mode.
FPDE	GD19	AD9	O	**Flat Panel Data Enable.** 24-bit mode or port 0 of dual 12-bit mode
FPDET	GADSTB1S	AF7	I	**Flat Panel Detect.** 24-bit mode or port 0 of dual 12-bit mode
FPCLK	GD21	AF8	O	**Flat Panel Clock.** 24-bit mode or port 0 of dual 12-bit mode
FPCLK#	GWBF	AC1	O	**Flat Panel Clock Complement.** 24-bit mode or port 0 of dual 12-bit Mode.

5.2 VIA K8N800 North Bridge(6)

24-Bit / Dual 12-Bit Flat Panel Display Interface (Continued)

Signal Name	AGP Name	Pin #	I/O	Signal Description
FP1HS	GD9	AD14	O	**Flat Panel Horizontal Sync.** For port 1 in dual 12-bit mode.
FP1VS	GPAR	AC16	O	**Flat Panel Vertical Sync.** For port 1 in dual 12-bit mode.
FP1DE	GSERR	AC15	O	**Flat Panel Data Enable.** For port 1 in dual 12-bit mode.
FP1DET	GD8	AF14	I	**Flat Panel Detect.** For port 1 in dual 12-bit mode.
FP1CLK	GD2	AE18	O	**Flat Panel Clock.** For port 1 in dual 12-bit mode.
FP1CLK#	GSTOP	AC12	O	**Flat Panel Clock Complement.** For port 1 in dual 12-bit mode.

Compensation

Signal Name	Pin #	I/O	Signal Description
RPCOMP	D25	AI	**Host CPU P-Channel Compensation.** Connect 50 §Ù 1% resistor to GND.
RNCOMP	D26	AI	**Host CPU N-Channel Compensation.** Connect 50 §Ù 1% resistor to VCCHT.
RTCOMP	C26	AI	**Host CPU Compensation.** Connect 100 §Ù 1% resistor to VCCHT.
VLPCOMP	AD19	AI	**V-Link P-Channel Compensation.** Connect 360 §Ù 1% resistor to ground.
AGPNCOMP	W1	AI	**AGP N-Channel Compensation.** Connect 60.4 §Ù 1% resistor to VCCAGP.
AGPPCOMP	V1	AI	**AGP P-Channel Compensation.** Connect 60.4 §Ù 1% resistor to GND.

Clock, Reset, Power Control, General Purpose I/O, Interrupts and Test

Signal Name	Pin #	I/O	Signal Description
GCLK	A11	I	**AGP Clock.** 66 MHz clock for AGP logic.
DCLKI	D7	I	**Dot Clock (Pixel Clock) In.** For spread spectrum.
DCLKO	A7	O	**Dot Clock (Pixel Clock) Out.** For spread spectrum.
RESET#	AD25	I	**Reset.** Input from the South Bridge chip. 3.3V tolerant input. When asserted, this signal resets the chip and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options In addition, HTRST# is driven active to reset the K8 CPU.
PWROK	AE26	I	**Power OK.** Driven by South Bridge PWROK output from the power supply PWRGOOD input to the South Bridge.
SUSST#	AD26	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.
TESTIN	AC26	I	**Test In.** This pin is used for testing and must be left unconnected or tied high (4.7K §Ù to 2.5V) on all board designs.
BISTIN	D3	I	**Built-In-Self-Test In.** Reserved for test. Connect to GND for normal operation.
DEBUG	AC17	I	**Debug.** Reserved for test. Connect to ground for normal operation.
XIN	C6	I	**Reference Frequency In.** 14.31818 MHz.
INTA#	E7	O	**PCI Interrupt Output A.** Connect to the South Bridge.
GPOUT	D2	O	**General Purpose Output.**
GPO0	N2	O	**General Purpose Output.**

5.2 VIA K8N800 North Bridge(7)

Integrated Graphics Power and Ground

Signal Name	Pin #	I/O	Signal Description
VCCDAC	B2	P	**DAC Voltage.** 3.3V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDDAC	C3, D4	P	**DAC Ground.** Connect to main ground plane.
VCCRGB	A4	P	**Power for CRT RGB Outputs.** 3.3V ±5% connected via ferrite bead for isolation of digital switching noise
GNDRGB	B4	P	**Connection point for RGB Load Resistors.** Connect to main ground plane via ferrite bead for isolation of digital switching noise.
VCCPLL1	D5	P	**Power for Graphics Controller PLL1 ("E-Clock").** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDPLL1	C5	P	**Ground for Graphics Controller PLL1 ("E-Clock").** Connect to main ground plane via ferrite bead for isolation of digital switching noise.
VCCPLL2	A5	P	**Power for Graphics Controller PLL2 ("D-Clock").** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDPLL2	B5	P	**Ground for Graphics Controller PLL2 ("D-Clock").** Connect to main ground plane via ferrite bead for isolation of digital switching noise.
VCCPLL3	A6	P	**Power for Graphics Controller PLL3 ("LCD Clock").** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDPLL3	B6	P	**Ground for Graphics Controller PLL3 ("LCD Clock").** Connect to main ground plane via ferrite bead for isolation of digital switching noise.

5.3 VIA VT8235CD South Bridge(1)

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VD[7:0]	(see pin list)	IO	**Data Bus.** These pins are also used to send strap information to the chipset north bridge. At power up, VD7 reflects the state of a strap on SDCS3#, VD[6:4] reflect the state of straps on pins SDA[2:0], and VD[3:0] reflect the state of straps on pins Strap_VD3-0. The specific interpretation of these straps is north bridge chip design dependent.
VPAR	F24	IO	**Parity.** If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800, KT400). If VPAR is not implemented in the north bridge chip or is incompatible with the 8235CE (4x V-Link north bridges) connect this pin to an 8.2K pullup to 2.5V (Pro266, Pro266T, KT266, KT266A, KT333, P4X266, PN266, KN266, KM266, P4M266, P4N266). See app note AN222 for details.
VBE#	G24	IO	**Byte Enable.**
VCLK	L22	I	**V-Link Clock.**
UPCMD	K23	O	**Command from Client-to-Host.**
DNCMD	K25	I	**Command from Host-to-Client.**
UPSTB	J26	O	**Strobe from Client-to-Host.**
UPSTB#	J24	O	**Complement Strobe from Client-to-Host.**
DNSTB	K26	I	**Strobe from Host-to-Client.**
DNSTB#	H24	I	**Complement Strobe from Host-to-Client.**

CPU Interface

Signal Name	Pin #	I/O	Signal Description
A20M#	U26	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20).
FERR#	U24	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T24	OD	**Ignore Numeric Error.** This pin is connected to the CPU iPignore errorlr pin.
INIT#	R26	OD	**Initialization.** The VT8235 Version CE asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
INTR	T25	OD	**CPU Interrupt.** INTR is driven by the VT8235 Version CE to signal the CPU that an interrupt request is pending and needs service.
NMI	T26	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8235 Version CE generates an NMI when PCI bus SERR# is asserted.
SLP#	V26	OD	**Sleep.** Used to put the CPU to sleep.
SMI#	U25	OD	**System Management Interrupt.** SMI# is asserted by the VT8235 Version CE to the CPU in response to different Power-Management events.
STPCLK#	R24	OD	**Stop Clock.** STPCLK# is asserted by the VT8235 Version CE to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 §Ù pullup resistors to VCC_CMOS (see Design Guide).

5.3 VIA VT8235CD South Bridge(2)

Advanced Programmable Interrupt Controller (APIC) Interface

Signal Name	Pin #	I/O	Signal Description
APICD1	T23	O	**Internal APIC Data 1.** Function 0 Rx58[6] = 1
APICD0	R25	O	**Internal APIC Data 0.** Function 0 Rx58[6] = 1
APICCLK	U23	I	**APIC Clock.**

CPU Speed Control Interface

Signal Name	Pin #	I/O	Signal Description
VRDSLP / GPI29/ GPO29	AB9	OD	**Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selectsthe proper voltage for deep sleep mode. This pin performs the VRDPSLP function if Function 0 RxE5[3] = 0.
GHI# / **GPI22/ GPO22**	R22	OD	**CPU Speed Select.** Connected to the CPU voltage regulator, used to select high speed (L) or low speed (H). This pin performs the GHI# function if Function 0 RxE5[3] = 0.
DPSLP# / GPI23/ GPO23	P21	OD	**CPU Deep Sleep.** This pin performs the DPSLP# function if Device 17 Function 0RxE5[3]=0.
CPUMISS / GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ# / GPI6	AD10	I	**AGP Busy.** Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin.

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	(see pinlist)	IO	**Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME#assertion and data is driven or received in following cycles.
CBE[3:0]#	M3, L4, C1, E2	IO	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byteenables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	H2	IO	**Device Select.** The VT8235 Version CE asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235 Version CE-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	J1	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	J2	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	H1	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	K4	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
SERR#	C2	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 Version CE can be programmed to generate an NMI to the CPU.
PERR#	C3	_	**Parity Error.** PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except for a Special Cycle.
PAR	F4	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.

5.3 VIA VT8235CD South Bridge(3)

PCI Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
INTA# **INTB#** **INTC#** **INTD#** **INTE#** / GPI12, / GPO12, **INTF#** / GPI13, / GPO13, **INTG#** / GPI14, / GPO14, **INTH#** / GPI15, / GPO15	A4 B4 B5 C4 D4 E4 A3 B3	I	**PCI Interrupt Reques**t. The INTA# through INTD# pins are typically connected to thePCI bus INTA#-INTD# pins per the table below. INTE-H# are enabled by setting Device17, Function 0 Rx5B[1] = 1. BIOS settings must match the physical connection method. INTA# INTB# INTC# INTD# PCI Slot 1 INTA# NTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF# PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#
REQ5# / GPI7, **REQ4#,** **REQ3#,** **REQ2#,** **REQ1#,** **REQ0#**	R3 P3 D5 C5 B6 A5	I	**PCI Request.** These signals connect to the VT8235 Version CE from each PCI slot (oreach PCI master) to request the PCI bus. To use pin R3 as REQ5#, Function 0 RxE4 mustbe set to 1 otherwise this pin will function as General Purpose Input 7.
GNT5# / GPO7, **GNT4#,** **GNT3#,** **GNT2#,** **GNT1#,** **GNT0#**	R2 R4 E5 C6 D6 A6	O	**PCI Grant.** These signals are driven by the VT8235 Version CE to grant PCI access to aspecific PCI master. To use pin R2 as GNT5#, Function 0 RxE4 must be set to 1otherwise this pin will function as General Purpose Output 7.
PCIRST#	R1	O	**PCI Reset.** This signal is used to reset devices attached to the PCI bus.
PCICLK	R23	I	**PCI Clock.** This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AB7	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8235 Version CE drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 §Ù resistor if the function is not used. Refer to the ihPCI Mobile Design Guidelo and applicable VIA North Bridge Design Guide (KT400A, CLE266, or P4X400) for more details.

LAN Controller - Media Independent Interface (MII)

Signal Name	Pin #	I/O	PU	Signal Description
MCOL	B11	I	***PD***	**MII Collision Detect.** From the external PHY.
MCRS	A11	I	***PD***	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	A7	O	***PD***	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	B7	IO	***PD***	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	C9	I	***PD***	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	C7, A8, B8, C8	I	***PD***	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	D8	I	***PD***	**MII Receive Data Valid.**
MRXERR	D10	I	***PD***	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	C10	I	***PD***	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	A9, B9, B10, A10	O	***PD***	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	C11	O	***PD***	**MII Transmit Enable.** Signals that transmit is active from the MII port to the PHY.
MIIVCC	D9, E9, E10, E11	**Power**		**MII Interface Power.** 3.3V ±5%.
MIIVCC25	D12, E12	**Power**		**MII Suspend Power.** 2.5V ±5%.
RAMVCC	E7	**Power**		**Power For Internal LAN RAM.** 2.5V ±5%.
RAMGND	E6	**Power**		**Ground For Internal LAN RAM.**

5.3 VIA VT8235CD South Bridge(4)

Serial EEPROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
EECS#	**D11**	**O**		Serial EEPROM Chip Select.
EECK	**C12**	**O**		Serial EEPROM Clock.
EEDO	**B12**	**I**		Serial EEPROM Data Output. **Connect to EEPROM Data Out pin.**
EEDI	**A12**	**O**		Serial EEPROM Data Input. **Connect to EEPROM Data In pin.**

Low Pin Count (LPC) Interface

Signal Name	Pin #	I/O	PU	Signal Description
LFRM#	**AF6**	**IO**		LPC Frame.
LREQ#	**AE6**	**IO**		LPC DMA / Bus Master Request.
LAD[3-0]	**AD7, AE7, AF7, AD8**	**IO**	**PU**	LPC Address / Data.

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

System Management Bus (SMB) Interface (I 2 C Bus)

Signal Name	Pin #	I/O	Signal Description
SMBCK1	AC4	IO	**SMB / I 2 C Channel 1 Clock.**
SMBCK2 / GPI27 / GPO27	AC3	IO	**SMB / I 2 C Channel 2 Clock.** Rx95[2] = 0
SMBDT1	AB2	IO	**SMB / I 2 C Channel 1 Data.**
SMBDT2 / GPI26 / GPO26	AD1	IO	**SMB / I 2 C Channel 2 Data.** Rx95[2] = 0
SMBALRT#	AB1	I	**SMB Alert.** (enabled by System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. Connect to a 10K ohm pullup to VSUS33 if not used.

Universal Serial Bus 2.0 Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	E20	IO	**USB 2.0 Port 0 Data +**
USBP0Œ	D20	IO	**USB 2.0 Port 0 Data Œ**
USBP1+	A20	IO	**USB 2.0 Port 1 Data +**
USBP1Œ	B20	IO	**USB 2.0 Port 1 Data Œ**
USBP2+	E18	IO	**USB 2.0 Port 2 Data +**
USBP2Œ	D18	IO	**USB 2.0 Port 2 Data Œ**
USBP3+	A18	IO	**USB 2.0 Port 3 Data +**
USBP3Œ	B18	IO	**USB 2.0 Port 3 Data Œ**
USBP4+	D16	IO	**USB 2.0 Port 4 Data +**
USBP4Œ	E16	IO	**USB 2.0 Port 4 Data Œ**
USBP5+	A16	IO	**USB 2.0 Port 5 Data +**
USBP5Œ	B16	IO	**USB 2.0 Port 5 Data Œ**
USBCLK	E23	I	**USB 2.0 Clock.** 48MHz clock input for the USB interface
USBOC0#	C26	I	**USB 2.0 Port 0 Over Current Detect.** Port 0 is disabled if low.
USBOC1#	D24	I	**USB 2.0 Port 1 Over Current Detect.** Port 1 is disabled if low.
USBOC2#	B26	I	**USB 2.0 Port 2 Over Current Detect.** Port 2 is disabled if low.
USBOC3#	C25	I	**USB 2.0 Port 3 Over Current Detect.** Port 3 is disabled if low.
USBOC4#	B24	I	**USB 2.0 Port 4 Over Current Detect.** Port 4 is disabled if low.
USBOC5#	A24	I	**USB 2.0 Port 5 Over Current Detect.** Port 5 is disabled if low.
USBVCC	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Voltage.** 3.3V
USBGND	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Ground.**
VSUSUSB	C24	**Power**	**USB 2.0 Suspend Power.** 2.5V ±5%.
VCCUPLL	A23, B23	**Power**	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%.
GNDUPLL	C23, D23	**Power**	**USB 2.0 PLL Analog Ground.**

5.3 VIA VT8235CD South Bridge(5)

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY /PDDMARDY /PDSTROBE	Y22	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Read**y. Output flow control. The device mayassert DDMARDY to pause output transfers **Primary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY /SDDMARDY /SDSTROBE	AF17	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Read**y. Output flow control. The devicemay assert DDMARDY to pause output transfers **Secondary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR# /PHDMARDY /PHSTROBE	W26	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Read**y. Primary channel input flow contro**l.** Thehost may assert HDMARDY to pause input transfers **Primary Host Strob**e. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR# /SHDMARDY /SHSTROBE	AF23	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Read**y. Input flow control. The host mayassert HDMARDY to pause input transfers **Host Strobe** B. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# /PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# /SSTOP	AE23	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	Y23	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	AD17	I	**Secondary Device DMA Request.** Secondary channel DMA request

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
PDDACK#	Y24	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	AD23	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	AD24	I	**Primary Channel Interrupt Request.**
IRQ15	AE26	I	**Secondary Channel Interrupt Request.**
PDCS1#	V22	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	V23	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1# / strap	AF25	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector. Strap low (resistor to ground) to enable serial EEPROM interface via the MII bus (this disables the EExx pins). This pin has an internal pullup to default to serial EEPROM interface via the EExx pins.
SDCS3# / strap	AF26	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector. Strap information is communicated to the north bridge via VD[7].
PDA[2-0]	W24, V25, W23	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0] / strap	AE24, AC22, AF24	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VD[6:4].
PDD[15-0]	(see pin list)	IO	**Primary Disk Data.**
SDD[15-0]	(see pin list)	IO	**Secondary Disk Data.**

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ	AD9	I	**Serial IRQ.** This pin has an internal pull-up resistor.

5.3 VIA VT8235CD South Bridge(6)

AC97 Audio / Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST#	T3	O	**AC97 Reset.**
ACBTCK	T1	I	**AC97 Bit Clock.**
ACSYNC	T2	O	**AC97 Sync.**
ACSDO	U2	O	**AC97 Serial Data Out.**
ACSDIN0 (VSUS33)*f*	U3	I	**AC97 Serial Data In 0.**
ACSDIN1 (VSUS33)*f*	V2	I	**AC97 Serial Data In 1.**
ACSDIN2 / GPIO20 / PCS0#	U1	I	**AC97 Serial Data In 2.** RxE4[6]=0,E5[1]=0, PMIO Rx4C[20]=1
ACSDIN3 / GPIO21 / PCS1# / SLPBTN#	V3	I	**AC97 Serial Data In 3.** RxE4[6]=0,E5[2]=0, PMIO Rx4C[21]=1

Resets, Clocks, and Power Status

Signal Name	Pin #	I/O	Signal Description
PWRGD	**AC5**	**I**	**Power Good.** Connected to the Power Good signal on the Power Supply. Internal logic **powered by VBAT.**
PWROK#	**AF1**	**O**	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	**R1**	**O**	**PCI Reset.** Active low reset signal for the PCI bus. The VT8235 Version CE will assert this pin during power-up or from the control register.
OSC	**AB8**	**I**	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
RTCX1	**AE4**	**I**	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	**AF3**	**O**	**RTC Crystal Output**: 32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	**AE9**	**I**	**Test.**
TPO	**AF9**	**O**	**Test Pin Output.** Output pin for test mode.
NC	**(see pin list)**	**–**	**No Connect.** Do not connect.

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK / IRQ1	**W1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Clock.** From internal mouse controller. **Rx51[2]=0** Interrupt Request **1. Interrupt input 1.**
MSDT / IRQ12	**W2**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Data.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 1**2. Interrupt input 12.
KBCK / KA20G	**W3**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller Rx51[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	**V1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data.** From internal keyboard controller. Rx51[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / strap	**AF10**	**O**		**Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip. Strap high to enable LPC BIOS ROM.

Note: KBCK, KBDT, MSCK, and MSDT are powered by the VSUS33 suspend voltage plane.

Speaker

Signal Name	Pin #	I/O	PU	Signal Description
SPKR / strap	**AF8**	**O**		**Speaker.** Strap low to enable (high to disable) CPU frequency **strapping.**

5.3 VIA VT8235CD South Bridge(7)

General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 ***(VBAT)***	**AE2**	**I**	General Purpose Input 0. **Status on PMIO Rx20[0]**
GPI1 ***(VSUS33)***	**AC2**	**I**	General Purpose Input 1. **Status on PMIO Rx20[1]**
GPI2 / EXTSMI# ***(VSUS33)***	**AA1**	**I**	General Purpose Input 2. **Status on PMIO Rx20[4]**
GPI3 / RING# ***(VSUS33)***	**Y2**	**I**	General Purpose Input 3. **Status on PMIO Rx20[8]**
GPI4 / LID# ***(VSUS33)***	**AC1**	**I**	General Purpose Input 4. **Status on PMIO Rx20[11]**
GPI5 / BATLOW# ***(VSUS33)***	**V4**	**I**	General Purpose Input 5. **Status on PMIO Rx20[12]**
GPI6 / AGPBZ#	**AD10**	**I**	General Purpose Input 6. **Status on PMIO Rx20[5]**
GPI7 / REQ5#	**R3**	**I**	General Purpose Input 7. **RxE4[2] = 0**
GPI12 / GPO12 / INTE#	**D4**	**I**	General Purpose Input 12. **RxE4[4] = 0, 5B[1]=0**
GPI13 / GPO13 / INTF#	**E4**	**I**	General Purpose Input 13. **RxE4[4] = 0, 5B[1]=0**
GPI14 / GPO14 / INTG#	**A3**	**I**	General Purpose Input 14. **RxE4[4] = 0, 5B[1]=0**
GPI15 / GPO15 / INTH#	**B3**	**I**	General Purpose Input 15. **RxE4[4] = 0, 5B[1]=0**
GPI16 / INTRUDER# ***(VBAT)***	**AE1**	**I**	General Purpose Input 16. **Status on PMIO Rx20[6]**
GPI17 / CPUMISS	**Y1**	**I**	General Purpose Input 17. **Status on PMIO Rx20[5]**
GPI18 / THRM# / AOLGPI	**Y4**	**I**	General Purpose Input 18. **Rx8C[3] = 0**
GPI20 / GPO20 / ACSDIN2 / PCS0#	**U1**	**I**	**General Purpose Input 20.** RxE4[6]=1, E5[1]=0, **PMIO 4C[20] = 1**
GPI21 / GPO21 / ACSDIN3 / PCS1# / SLPBTN#	**V3**	**I**	**General Purpose Input 21.** RxE4[6]=1, E5[2]=0 PMIO 4C[21] = 1
GPI22 / GPO22 / GHI#	**R22**	**I**	**General Purpose Input 22.** RxE5[3] = 1, PMIO 4C[22] = 1
GPI23 / GPO23 / DPSLP#	**P21**	**I**	**General Purpose Input 23.** RxE5[3] = 1, PMIO 4C[23] = 1

General Purpose Inputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPI26 / GPO26 / SMBDT2 ***(VSUS33)***	**AD1**	**I**	**General Purpose Input 26.** Rx95[2] = 1, 95[3] = 0
GPI27 / GPO27 / SMBCK2 ***(VSUS33)***	**AC3**	**I**	**General Purpose Input 27.** Rx95[2] = 1, 95[3] = 0
GPI28 / GPO28	**AC8**	**I**	**General Purpose Input 28.** RxE5[3] = 1, PMIO 4C[28] = 1
GPI29 / GPO29 / VRDSLP	**AB9**	**I**	**General Purpose Input 29.** RxE5[3] = 1, PMIO 4C[29] = 1

Note: Register references above are Device 17 Function 0 unless indicated otherwise.
Note: Default pin function is underlined in the signal name column above.
Note: Input pin status for the above GPI pins 31-0 is also available on PMIO Rx4B-48[31-0]
Note: See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx4C. General purpose input pins 20-31 are shared with OD (open drain) general

Programmable Chip Selects

Signal Name	Pin #	I/O	Signal Description
PCS0# / GPIO20 / ACSDIN2	**U1**	**O**	Programmable Chip Select 0. **RxE4[6]=1, E5[1]=1**
PCS1# / GPIO21 / ACSDIN3 / SLPBTN#	**V3**	**O**	Programmable Chip Select 1. **RxE4[6]=1, E5[2]=1**

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General Purpose Outputs

Signal Name	Pin #	I/O	Signal Description
GPO0 ***(VSUS33)***	**AA3**	**O**	General Purpose Output 0.
GPO1 / SUSA# ***(VSUS33)***	**AA2**	**O**	General Purpose Output 1. **Rx94[2] = 1**
GPO2 / SUSB# ***(VSUS33)***	**AD3**	**O**	General Purpose Output 2. **Rx94[3] = 1**
GPO3 / SUSST1# ***(VSUS33)***	**Y3**	**O**	General Purpose Output 3. **Rx94[4] = 1**
GPO4 / SUSCLK ***(VSUS33)***	**AB3**	**O**	General Purpose Output 4. **Rx95[1] = 1**
GPO5 / CPUSTP#	**AC7**	**O**	General Purpose Output 5. **RxE4[0] = 1**
GPO6 / PCISTP#	**AD6**	**O**	General Purpose Output 6. **RxE4[1] = 1**
GPO7 / GNT5#	**R2**	**O**	General Purpose Output 7. **RxE4[2] = 0**
GPO12 / GPI12 / INTE#	**D4**	**O**	General Purpose Output 12. **RxE4[4]=1, 5B[1]=0**
GPO13 / GPI13 / INTF#	**E4**	**O**	General Purpose Output 13. **RxE4[4]=1, 5B[1]=0**
GPO14 / GPI14 / INTG#	**A3**	**O**	General Purpose Output 14. **RxE4[4]=1, 5B[1]=0**
GPO15 / GPI15 / INTH#	**B3**	**O**	General Purpose Output 15. **RxE4[4]=1, 5B[1]=0**
GPO20 / GPI20 / ACSDIN2 / PCS0#	**U1**	**OD**	General Purpose Output 20. **RxE4[6]=1, E5[1]=0**
GPO21 / GPI21 / ACSDIN3 / PCS1# /SLPBTN#	**V3**	**OD**	General Purpose Output 21. **RxE4[6]=1, E5[2]=0**
GPO22 / GPI22 / GHI#	**R22**	**OD**	General Purpose Output 22. **RxE5[3]=1, PMIO 4C[22]=1**
GPO23 / GPI23 / DPSLP#	**P21**	**OD**	General Purpose Output 23. **RxE5[3]=1, PMIO 4C[23]=1**
GPO26 / GPI26 / SMBDT2 ***(VSUS33f)***	**AD1**	**OD**	General Purpose Output 26. **Rx95[2] = 1, 95[3] = 1**
GPO27 / GPI27 / SMBCK2 ***(VSUS33f)***	**AC3**	**OD**	General Purpose Output 27. **Rx95[2] = 1, 95[3] = 1**

General Purpose Outputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPO28 / GPI28	**AC8**	**OD**	General Purpose Output 28. **RxE5[3] = 1, PMIO 4C[28]=1**
GPO29 / GPI29 / VRDSLP	**AB9**	**OD**	General Purpose Output 29. **RxE5[3] = 1, PMIO 4C[29]=1**

Note: The output state for each of the above general purpose outputs is selectable via Power Management I/O registers Rx4C-48
Note: Default pin functions are underlined in the table above.

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	**AD2**	**I**	**Power Button.** Used by the Power Management subsystem to monitor an external **system on/off button or switch. Internal logic powered by VSUS33.**
SLPBTN# / GPIO21/ ACSDIN3 / PCS1#	**V3**	**I**	**Sleep Button.** Used by the Power Management subsystem to monitor an external sleepbutton or switch. RxE4[6] = 1, 80[6] = 1, E5[2] = 0 and PMIO Rx4C[21] = 1
RSMRST#	**AD4**	**I**	**Resume Reset.** Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT.
EXTSMI# / GPI2	**AA1**	**IOD**	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VSUS33 if not used) (3.3V only)
PME#	**W4**	**I**	**Power Management Event.** (10K PU to VSUS33 if not used)
SMBALRT#	**AB1**	**I**	**SMB Aler**t. When programmed to allow it (SMB I/O Rx8[3]=1), assertion generates an IRQ, SMI, or power management event. (10K PU to VSUS33 if not used)

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Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
LID# / GPI4	**AC1**	**I**	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. (10K PU to VSUS33 if not used)
INTRUDER# / GPI16	**AE1**	**I**	**Intrusion Indicator.** The value of this bit may be read at PMIO Rx20[6]
THRM# / GPI18/ AOLGPI	**Y4**	**I**	**Thermal Alarm Monitor.** Rx8C[3] = 1. Rising or falling edges (selectable by PMIORx2C[6]) may be detected to set status at PMIO Rx20[10]. Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#) to automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-4]).
RING# / GPI3	**Y2**	**I**	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VSUS33 if not used)
BATLOW# / GPI5	**V4**	**I**	**Battery Low Indicator.** (10K PU to VSUS33 if not used) (3.3V only)
CPUSTP# / GPO5	**AC7**	**O**	**CPU Clock Stop** (RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP# / GPO6	**AD6**	**O**	**PCI Clock Stop** (RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.
SUSA# / GPO1	**AA2**	**O**	**Suspend Plane A Control** (Rx94[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VSUS33 if not used)
SUSB# / GPO2	**AD3**	**O**	**Suspend Plane B Control** (Rx94[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VSUS33 if not used)
SUSC#	**AF2**	**O**	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry. (10K PU to VSUS33 if not used)

Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
SUSST1# / GPO3	**Y3**	**O**	**Suspend Status 1** (Rx94[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VSUS33.
SUSCLK	**AB3**	**O**	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., KT400A, CLE266, or P4X400) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS / GPI17	**Y1**	**I**	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AOLGPI / GPI18/ THRM#	**Y4**	**I**	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pinmay be used as AOLGPI, GPI18 and THRM# all at the same time.

Strap Pins for VT8235 Version CE Configuration

Signal Name	Pin #	Function	Description	Note
Strap_AUTO	**AE10**	**Auto Reboot**	L: Enable Auto Reboot **H: Disable Auto Reboot (Default)**	
SPKR	**AF8**	**CPU Frequency Strapping**	L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping (Default)	
KBCS#	**AF10**	**Internal Keyboard** Controller	L: Disable internal KBC H: Enable internal KBC (Default)	
SDCS1#	**AF25**	Eliminate External LAN EEPROM	L: Enable. Use external EEPROM (Default) H: Disable. Do not use external EEPROM	

5.3 VIA VT8235CD South Bridge(10)

Power and Ground

Signal Name	Pin #	I/O	Signal Description
VSUS33	AA4, AB4-6	P	**Suspend Power.** 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the ihsoft-offlÉD state is not implemented, then this pin can be connected to VCC33. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCK1/2, SMBDT1/2, GPO0, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO3, SUSCLK / GPO4, GPI1, GPI2 / EXTSMI#, GPI3 / RING#, GPI4 / LID, GPI5 / BATLOW#, GPI6 / PME#, SMBALRT#
VSUS25	T4, U4	P	**Suspend Power.** 2.5V ±5%.
VSUSUSB	C24	P	**USB Suspend Power.** 2.5V ±5%.
VBAT	AF4	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VLVREF	H22	P	**V-Link Voltage Reference.** 0.9V ±5% for 4x transfers and 0.625V ±5% for 8x transfers.
VLCOMP	J22	AI	**V-Link Compensation.**
VCCVK	(see pin list)	P	**V-Link Compensation Circuit Voltage.** 2.5V ±5%
MIIVCC	D9, E9-11	P	**LAN MII Power.** 3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY). Connect to VCC33 through a ferrite bead.
MIIVCC25	D12. E12	P	**LAN MII Suspend Power.** 2.5V ±5%.
LANVCC	E7	P	**LAN Power.** 2.5V ±5%. Power for LAN. Connect to VCC through a ferrite bead.
LANGND	E6	P	**LAN Ground.** Connect to GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.** 3.3V ±5%. Power for USB differential outputs (USBP0+, P0Œ, P1+, P1Œ, P2+, P2Œ, P3+, P3Œ, P4+, P4Œ, P5+, P5Œ). Connect to VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.
VCCUPLL	A23, B23	P	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%. Connect to VCC through a ferrite bead.
GNDUPLL	C23, D23	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	T22	P	**PLL Analog Power.** 2.5V ±5%. Connect to VCC through a ferrite bead.
PLLGND	U22	P	**PLL Analog Ground.** Connect to GND through a ferrite bead.

Power and Ground（Continued）

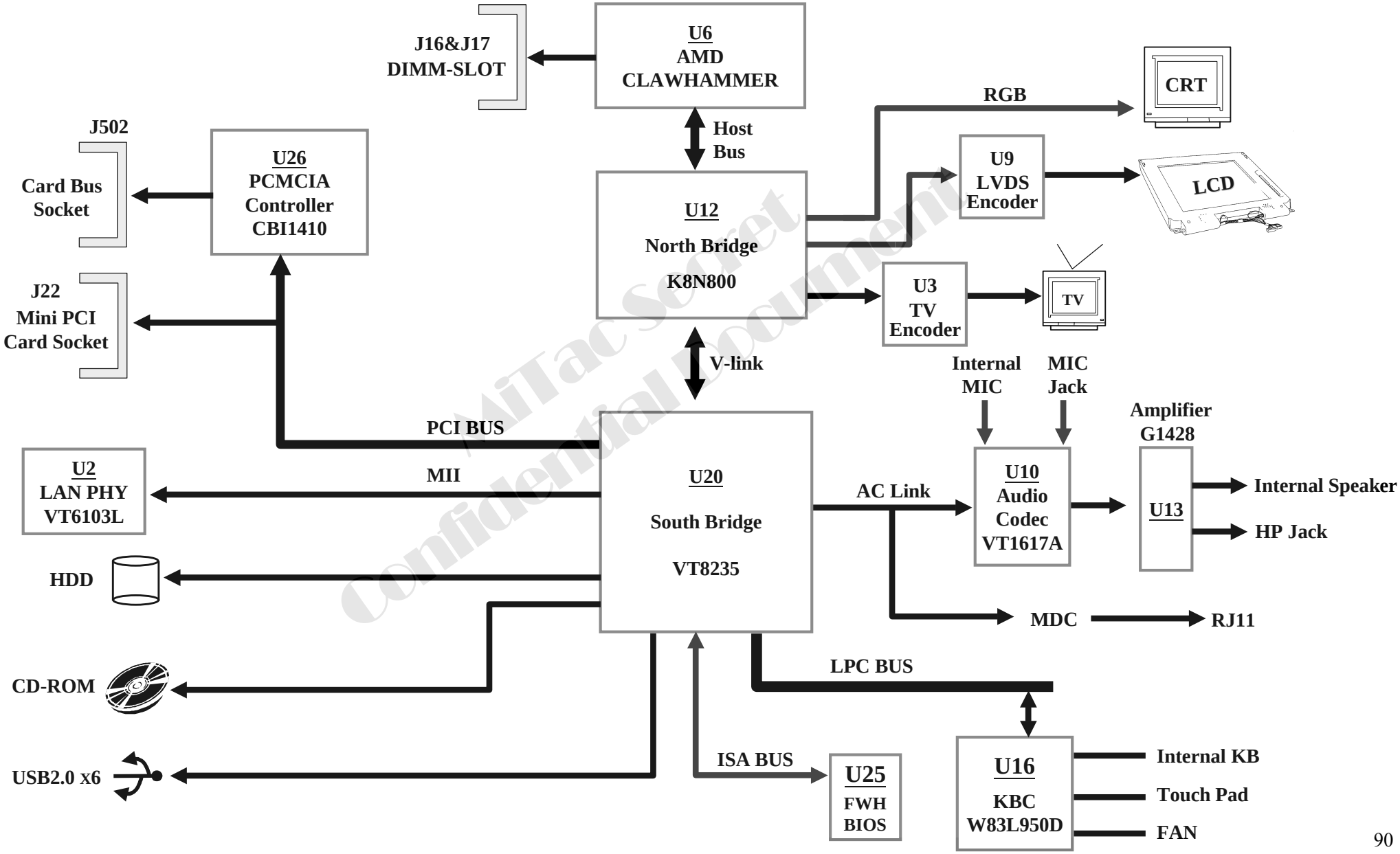
Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)	P	I/O Power. **3.3V ±5%**
VCC	(see pin list)	P	Core Power. **2.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.**
GND	(see pin list)	P	**Ground.** Connect to primary motherboard ground plane.

Strap Pins for North Bridge Configuration

Signal Name	Pin #	Function	Description	Note
SDCS3#	AF26	NB Configuration	SDCS3# signal state is reflected on signal pinVD[7] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA2	AE24	NB Configuration	SDA2 signal state is reflected on signal pinVD[6] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA1	AC22	NB Configuration	SDA1 signal state is reflected on signal pinVD[5] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA0	AF24	NB Configuration	SDA0 signal states is reflected on signal pinsVD[4] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD3	AC6	NB Configuration	Strap_VD3 signal state is reflected on signal pinVD[3] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD2	AD5	NB Configuration	Strap_VD2 signal state is reflected on signal pinVD[2] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD1	AE5	NB Configuration	Strap_VD1 signal state is reflected on signal pin, VD[1] during power up for North Bridge configuration.	**Check the North Bridge DS for details**
Strap_VD0	AF5	NB Configuration	Strap_VD0 signal state is reflected on signalpin, VD[0] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**

Note: Internal Pullups are present on pins KBCK, KBDT, MSCK, MSDT, SERIRQ, LAD[3:0]
Internal Pulldowns are present on all LAN pins

6. System Block Diagram



7. Maintenance Diagnostics

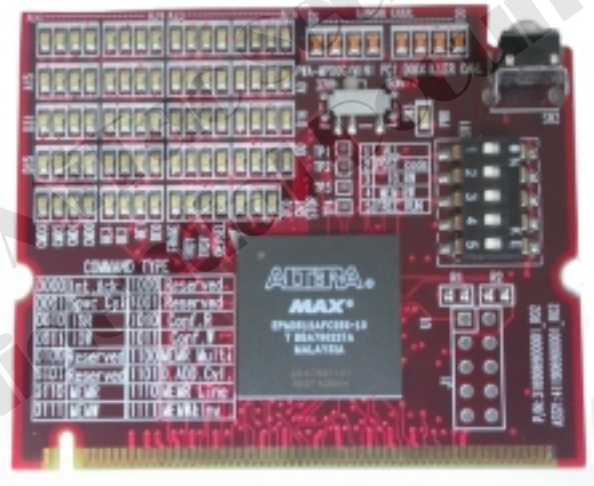
7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port by the debug card plug at MINI PCI slot.

7.2 Diagnostic Tool for Mini PCI Slot

The Mini PCI DOG killer card is a single-step debug tool which utilizes Mini PCI interface (Type III A) and is able to hold a PCI bus cycle so that address, data and control bus states on PCI bus can be inspected. Especially, the tool can help an engineer trace address/data bus for BIOS read cycles as soon as power on and debug open or short circuit problems easily. Usually, this sort of problem will make a PC motherboard fail to boot.



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

7.3 Error Codes-1

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
10H	Some Type Of Long Reset
11H	Turn off FASTA20 for POST
12H	Signal Power On Reset
13H	Initialize the Chipset
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1
16H	user register configure through CMOS
17H	Size Memory
18H	Dispatch To RAM Test
19H	checksum the ROM
1AH	Reset PIC's
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter
1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Test Keyboard
21H	Test Keyboard Controller
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Int Vectors

POST (HEX)	DESCRIPTION
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Going To Initialize Video
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter
2FH	Signon messages displayed
30H	special init of keyboard ctrl
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful
38H	Update OUTPUT port
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	test for RTC ticking
3CH	initialize the hardware vectors
3DH	Search and Init the Mouse

7.3 Error Codes-2

Following is a list of error codes in sequent display on the debug board.

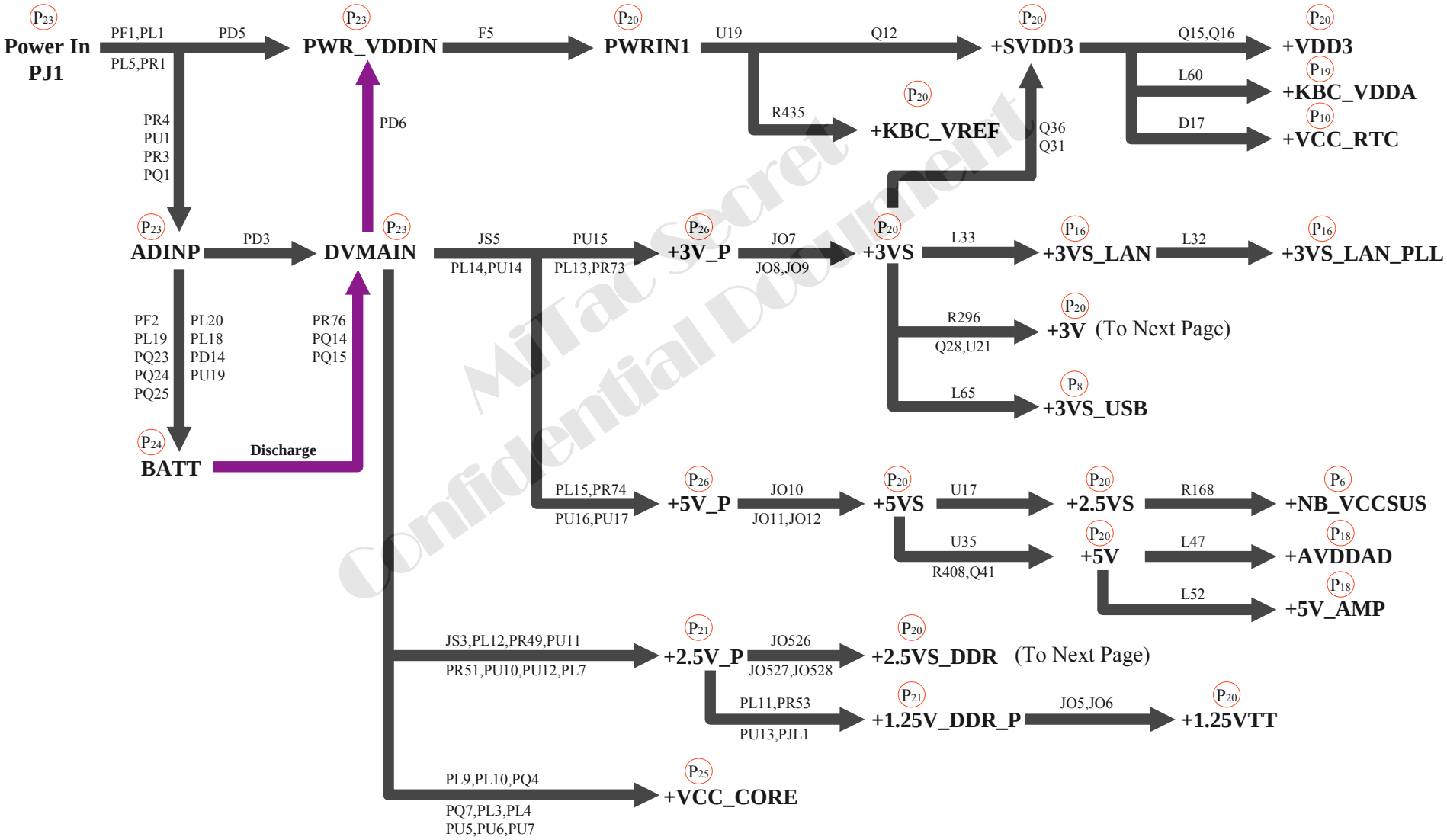
POST (HEX)	DESCRIPTION
3EH	Update NUMLOCK status
3FH	special init of COMM and LPT ports
40H	Configure the COMM and LPT ports
41H	Initialize the floppies
42H	Initialize the hard disk
43H	Initialize option ROMs
44H	OEM's init of power management
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM functions before boot
48H	Dispatch To Op. Sys. Boot
49H	Jump Into Bootstrap Code

8. Trouble Shooting

- 8.1 Base Work Condition
- 8.2 No Power
- 8.3 Battery Can not Be Charged
- 8.4 No Display
- 8.5 External Monitor No Display
- 8.7 Keyboard/Touch Pad Test Error
- 8.6 Memory Test Error
- 8.8 USB Port Test Error
- 8.9 Hard Disk Driver Test Error
- 8.10 CD-ROM Driver Test Error
- 8.11 Audio Failure
- 8.12 LAN Test Error
- 8.13 Modem Test Error
- 8.14 Mini PCI Test Error
- 8.15 CardBus & Reader Test Error
- 8.16 TV Encoder Test Error

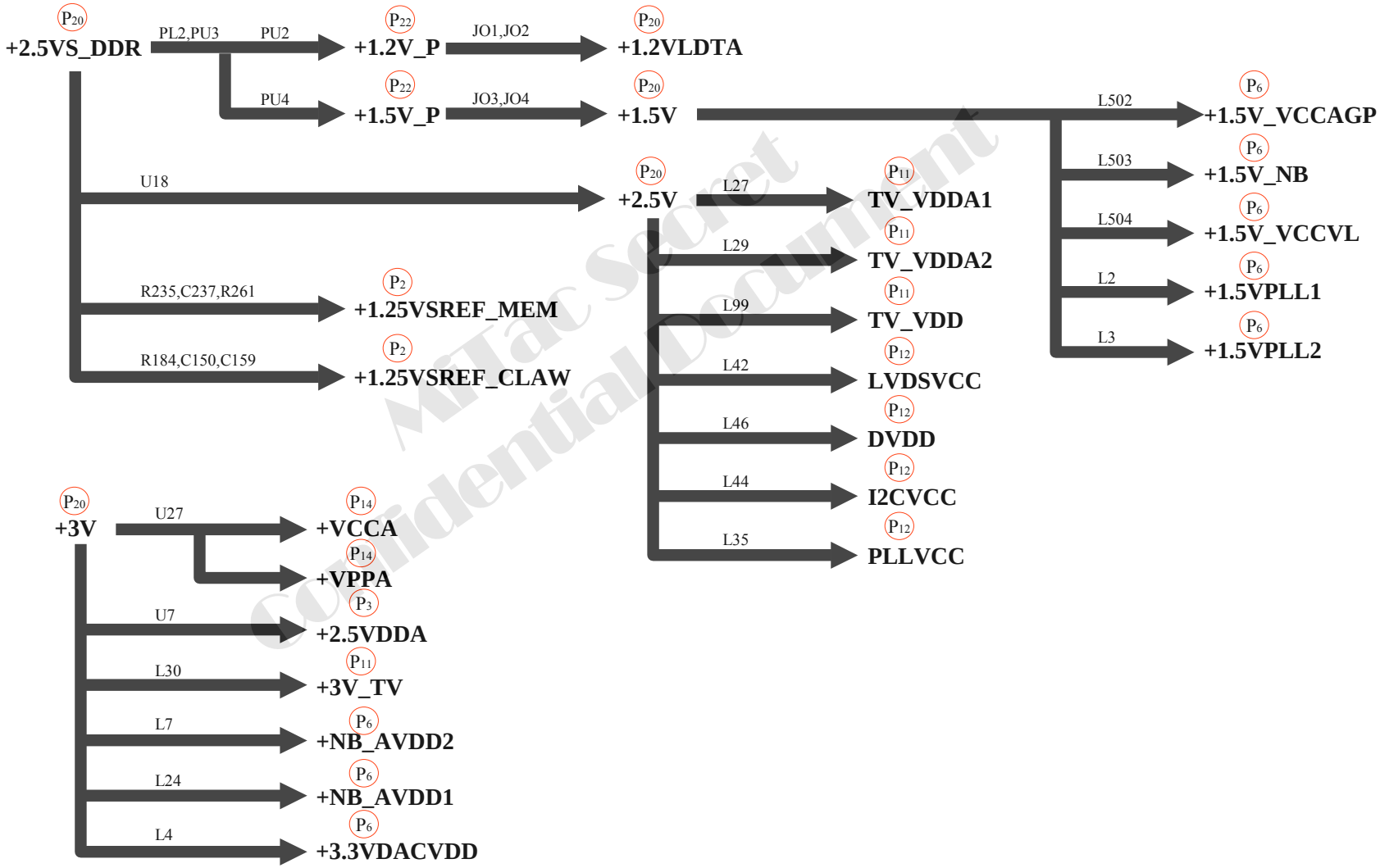
8.1 Base Work Condition(1)

System Voltage Check



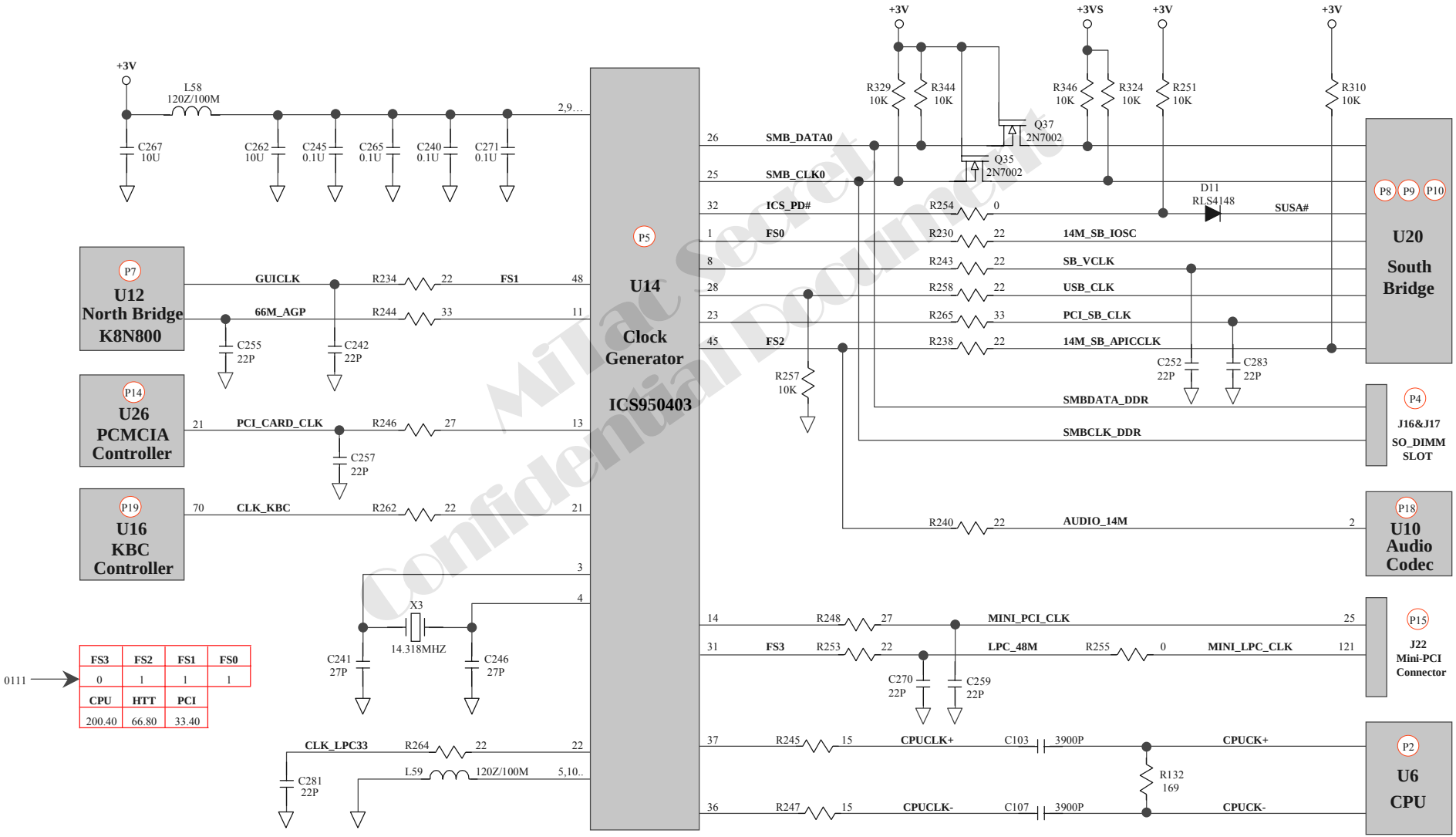
8.1 Base Work Condition(2)

System Voltage Check



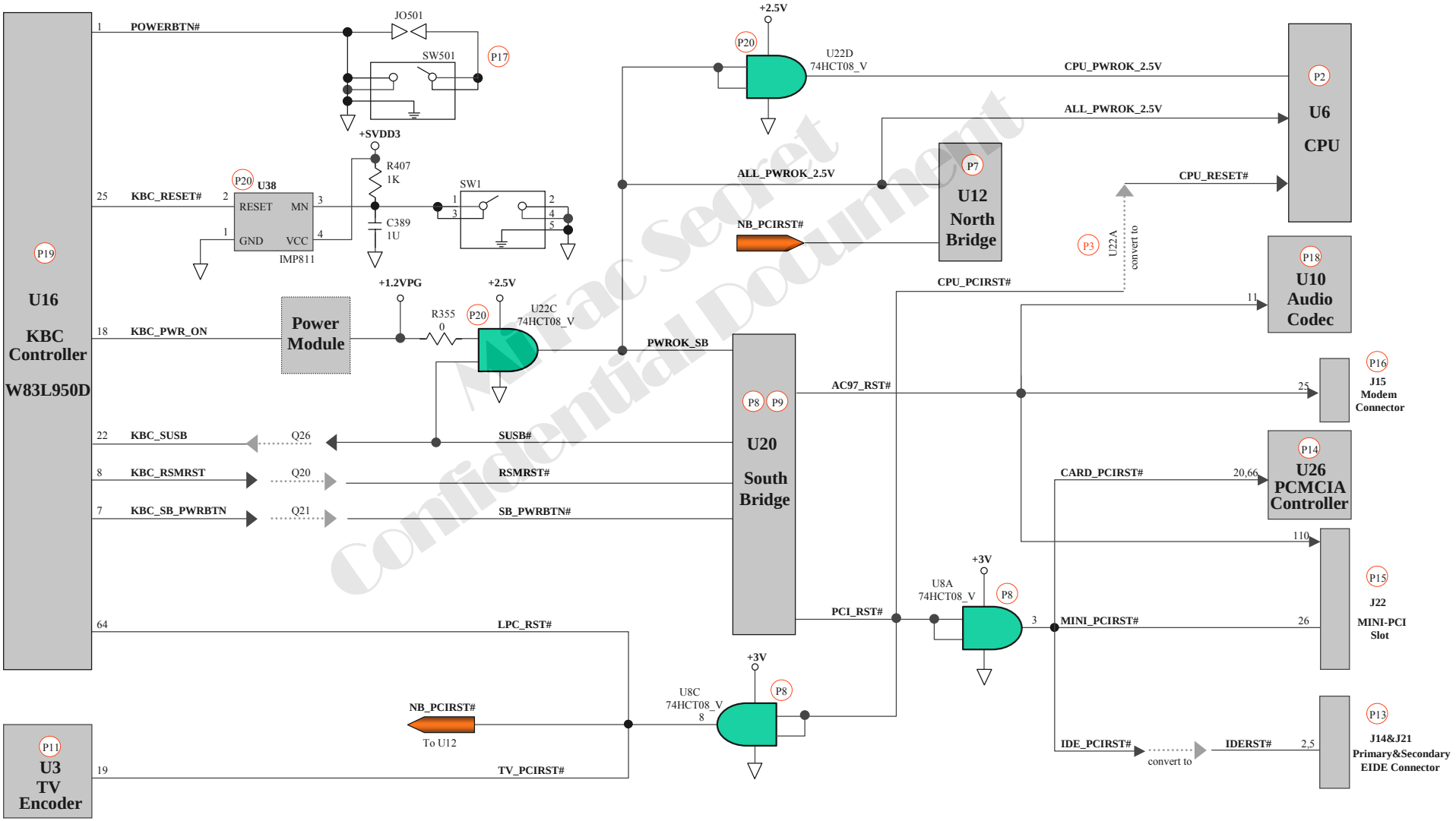
8.1 Base Work Condition(3)

System Clock Check



8.1 Base Work Condition(4)

System Reset Check



*1: No power definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No display definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

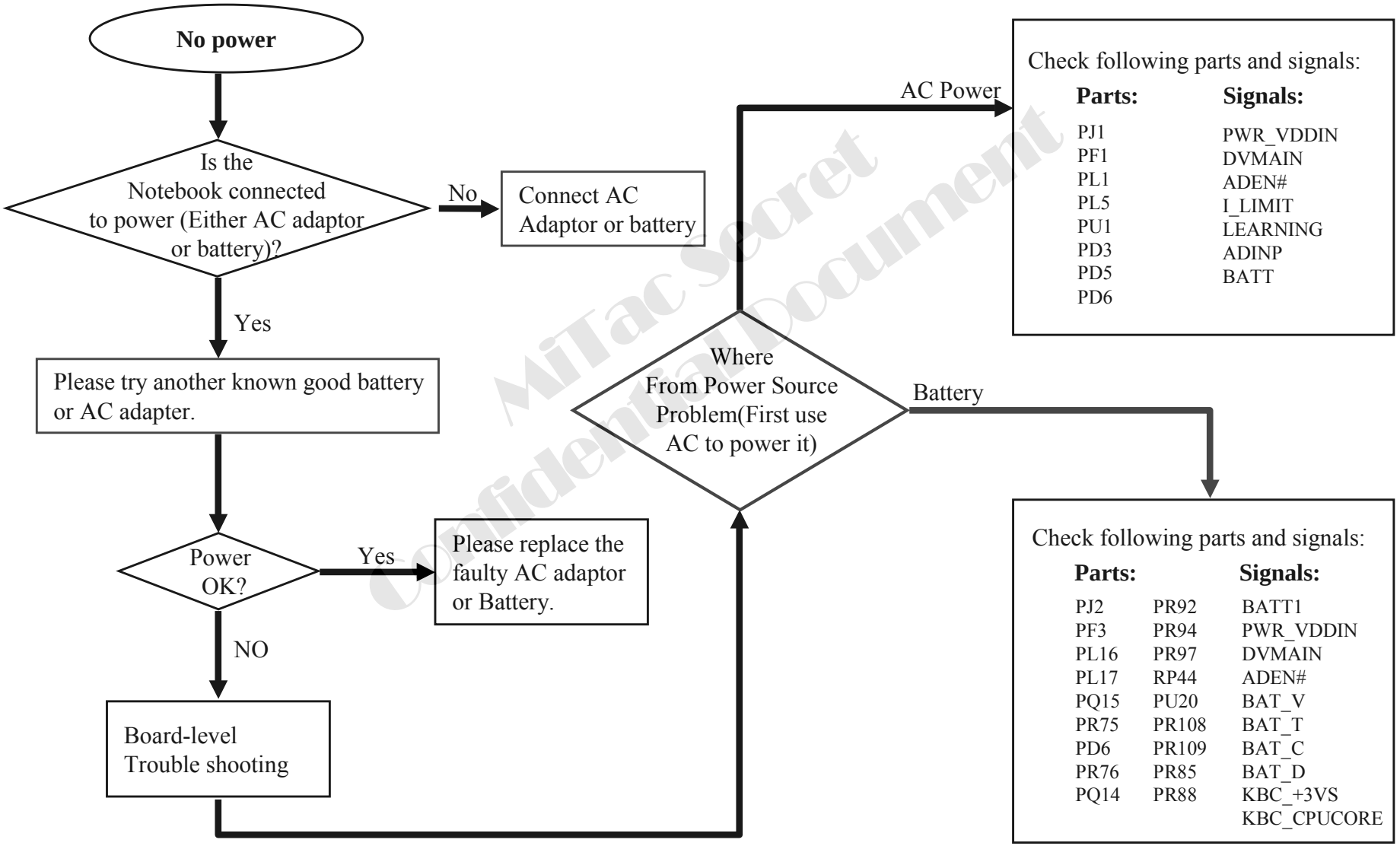
Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

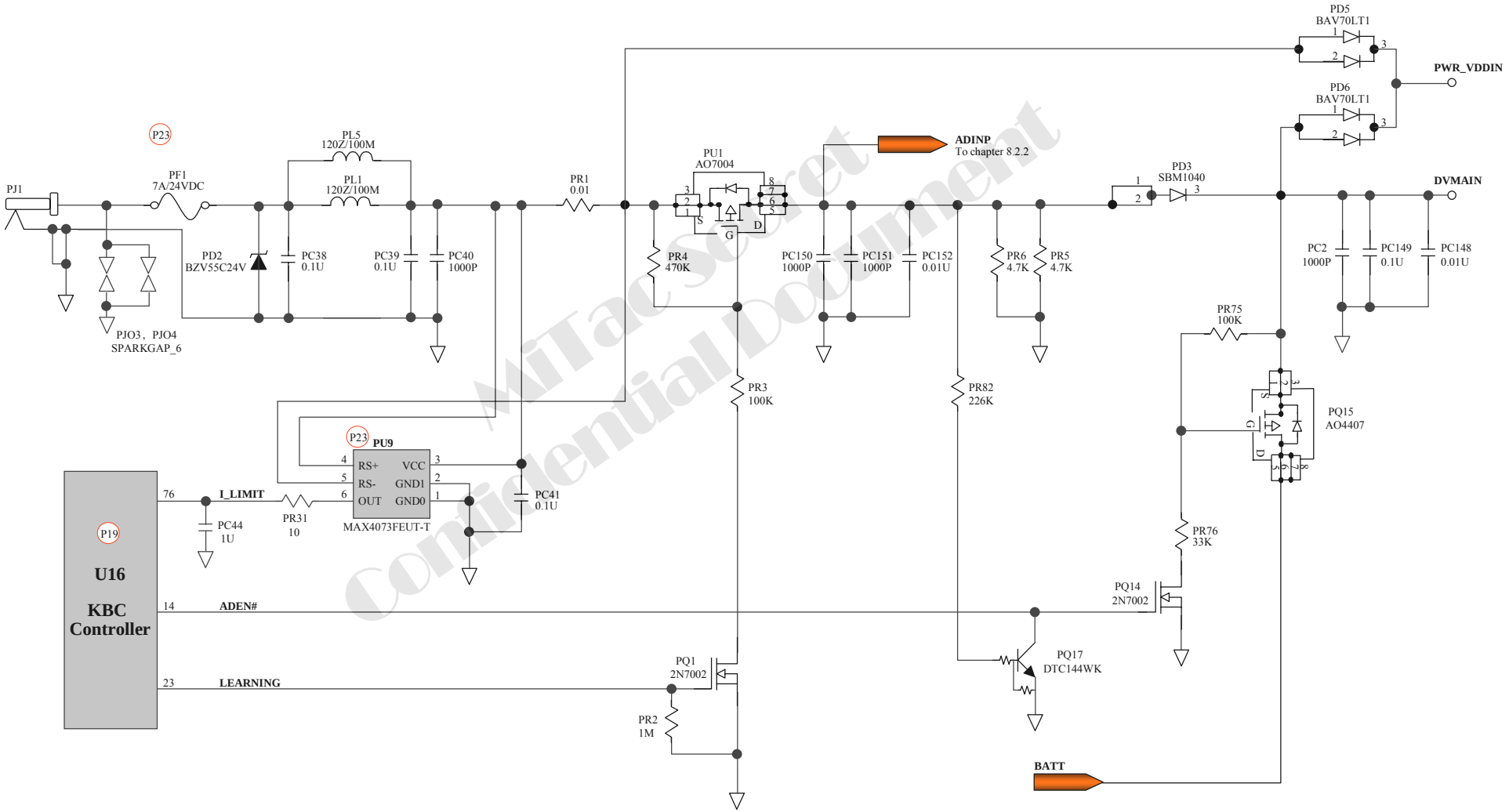
8.2 No Power(1)

When power button is pressed ,nothing happens ,power indicator does not light up.



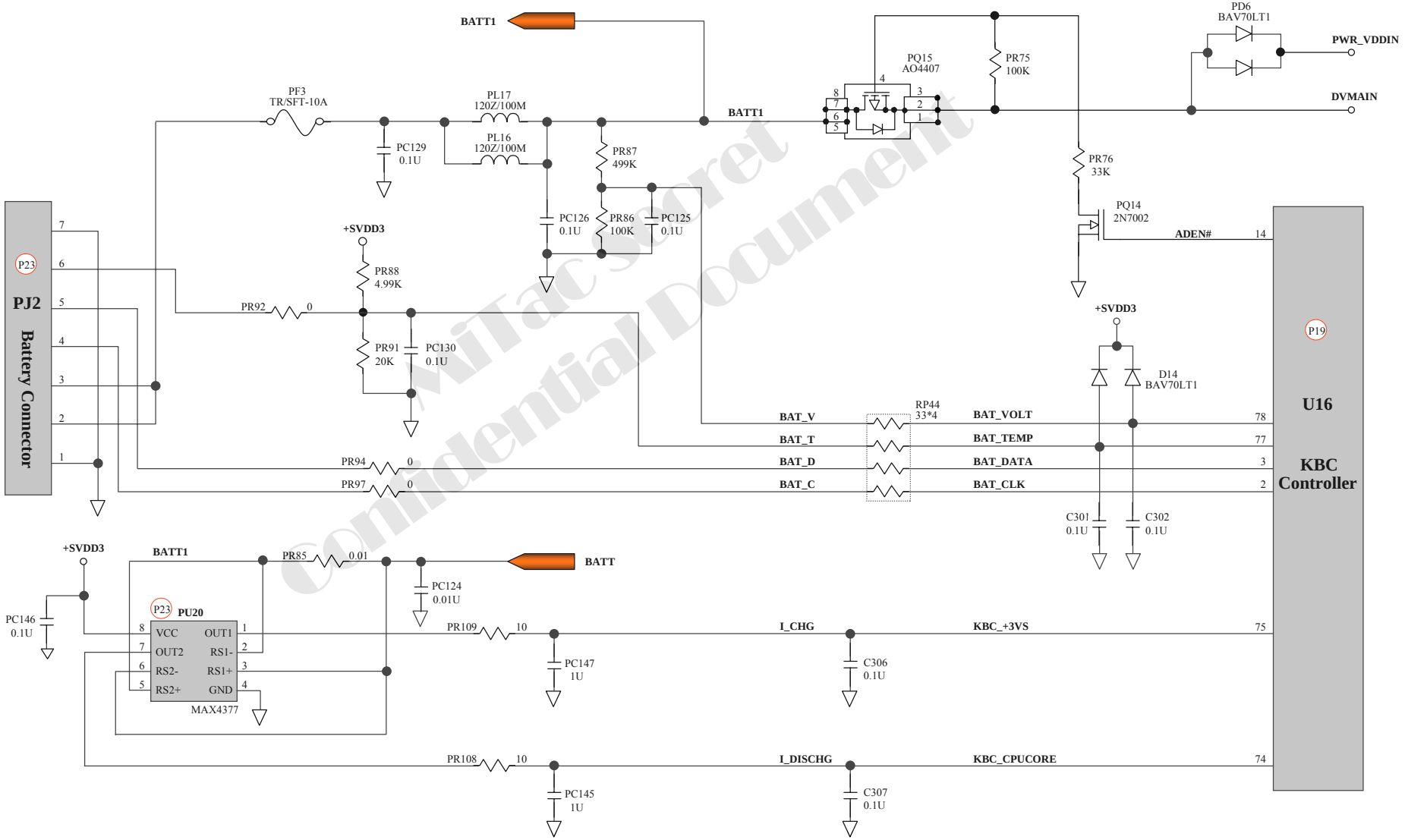
8.2 No Power(2)

When power button is pressed ,nothing happens ,power indicator does not light up.



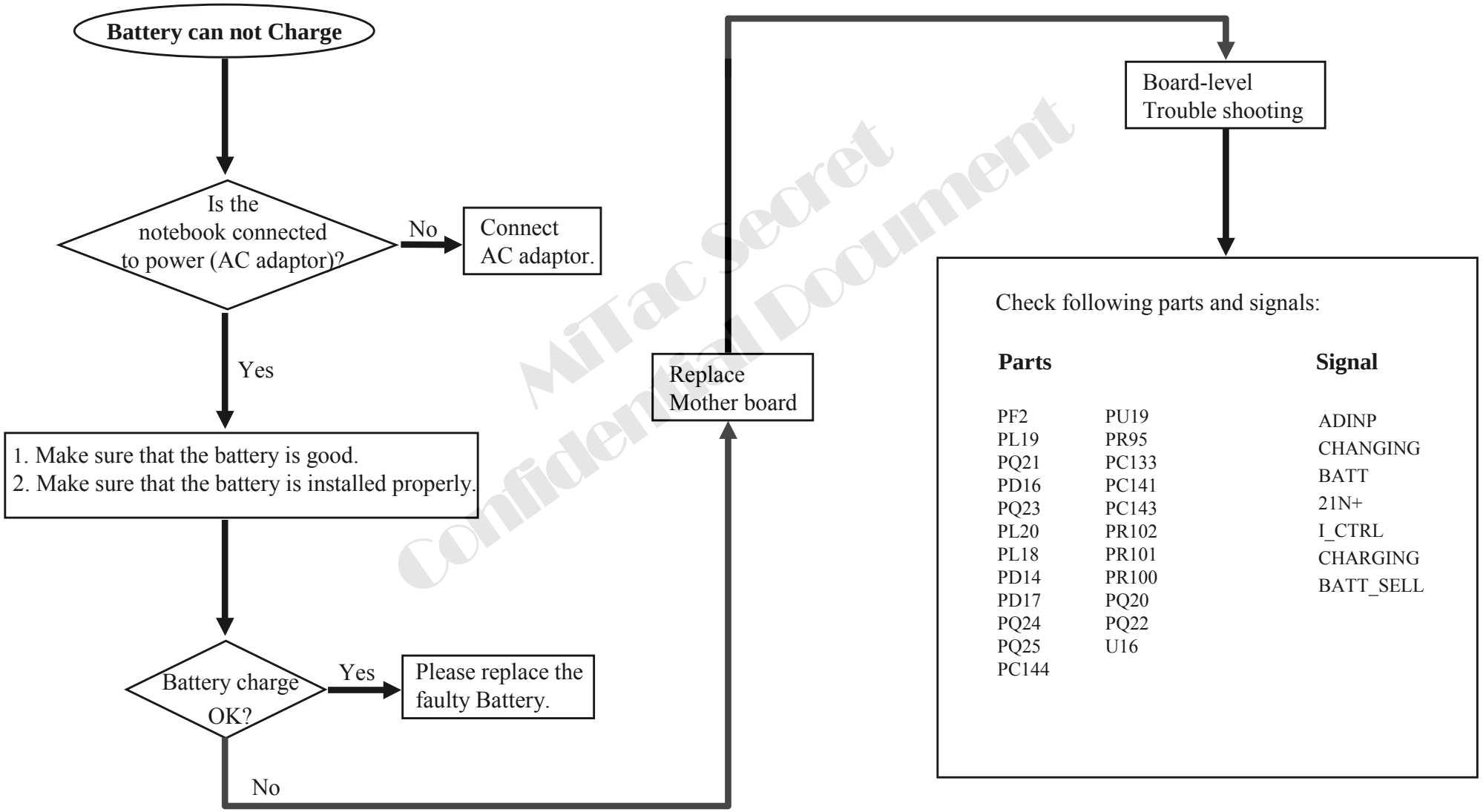
8.2 No Power(3)

When power button is pressed ,nothing happens ,power indicator does not light up.



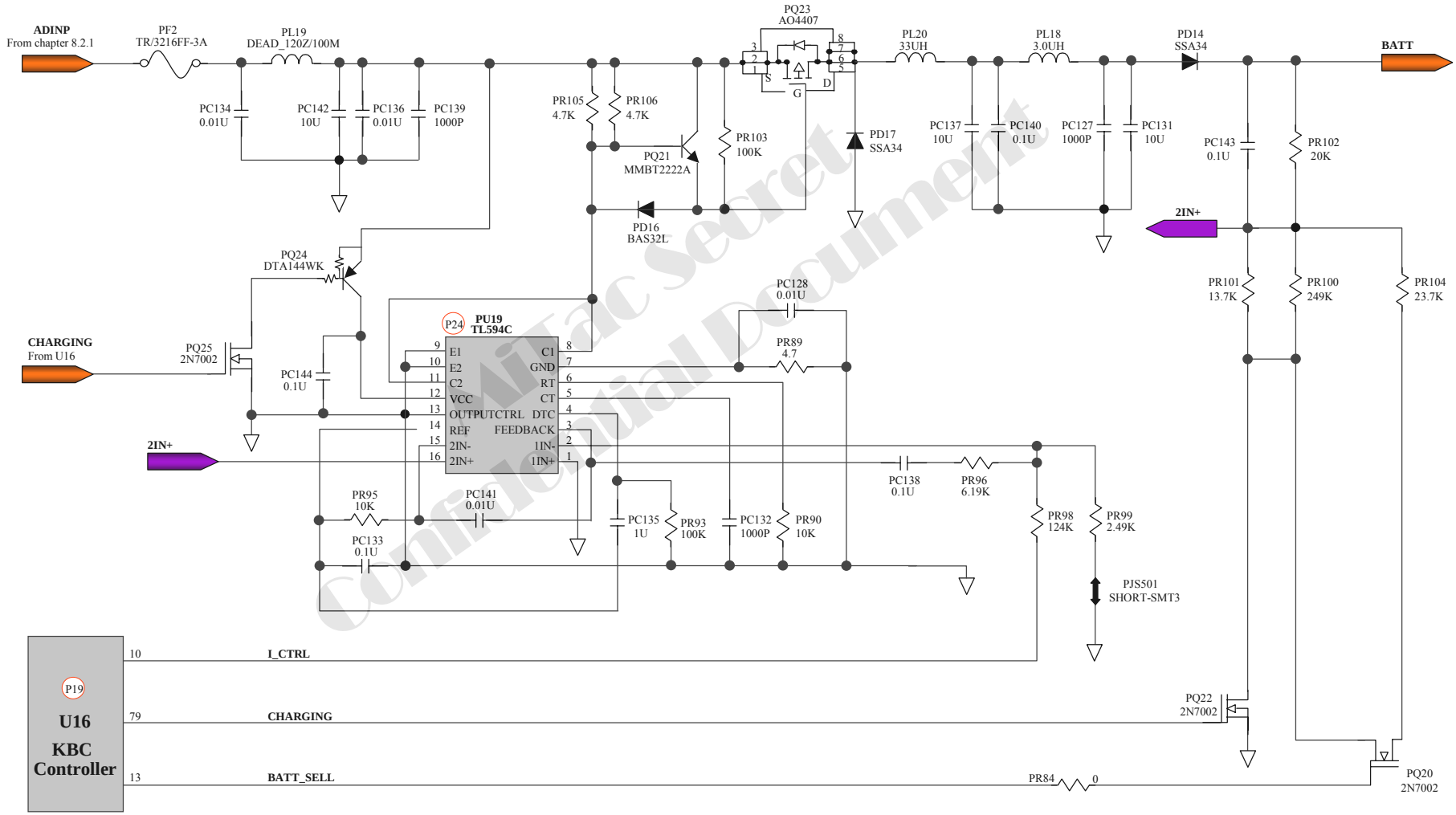
8.3 Battery Can not Be Charged(1)

When the battery is installed but the battery status indicate LED display abnormal.



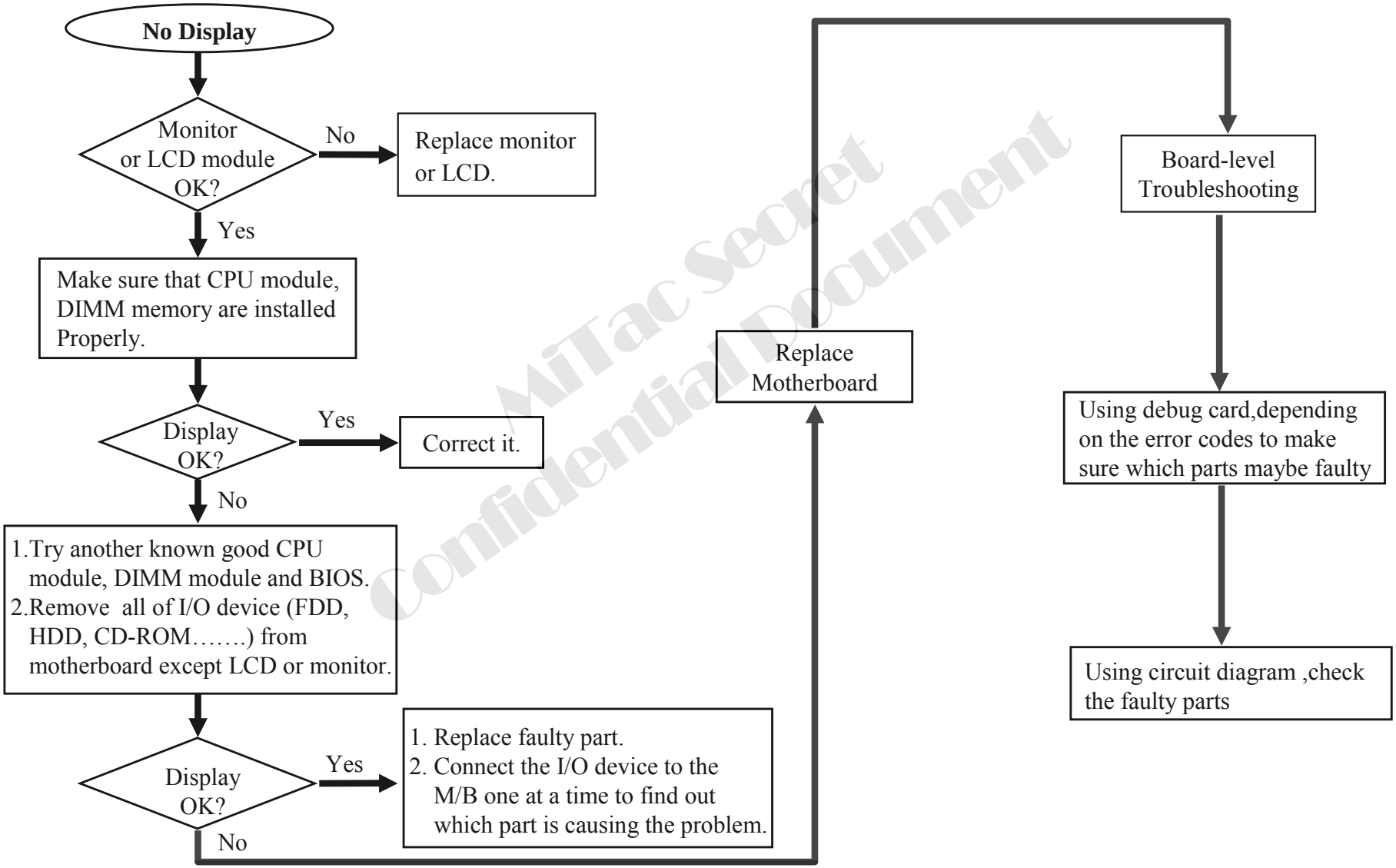
8.3 Battery Can not Be Charged(2)

When the battery is installed but the battery status indicate LED display abnormal.



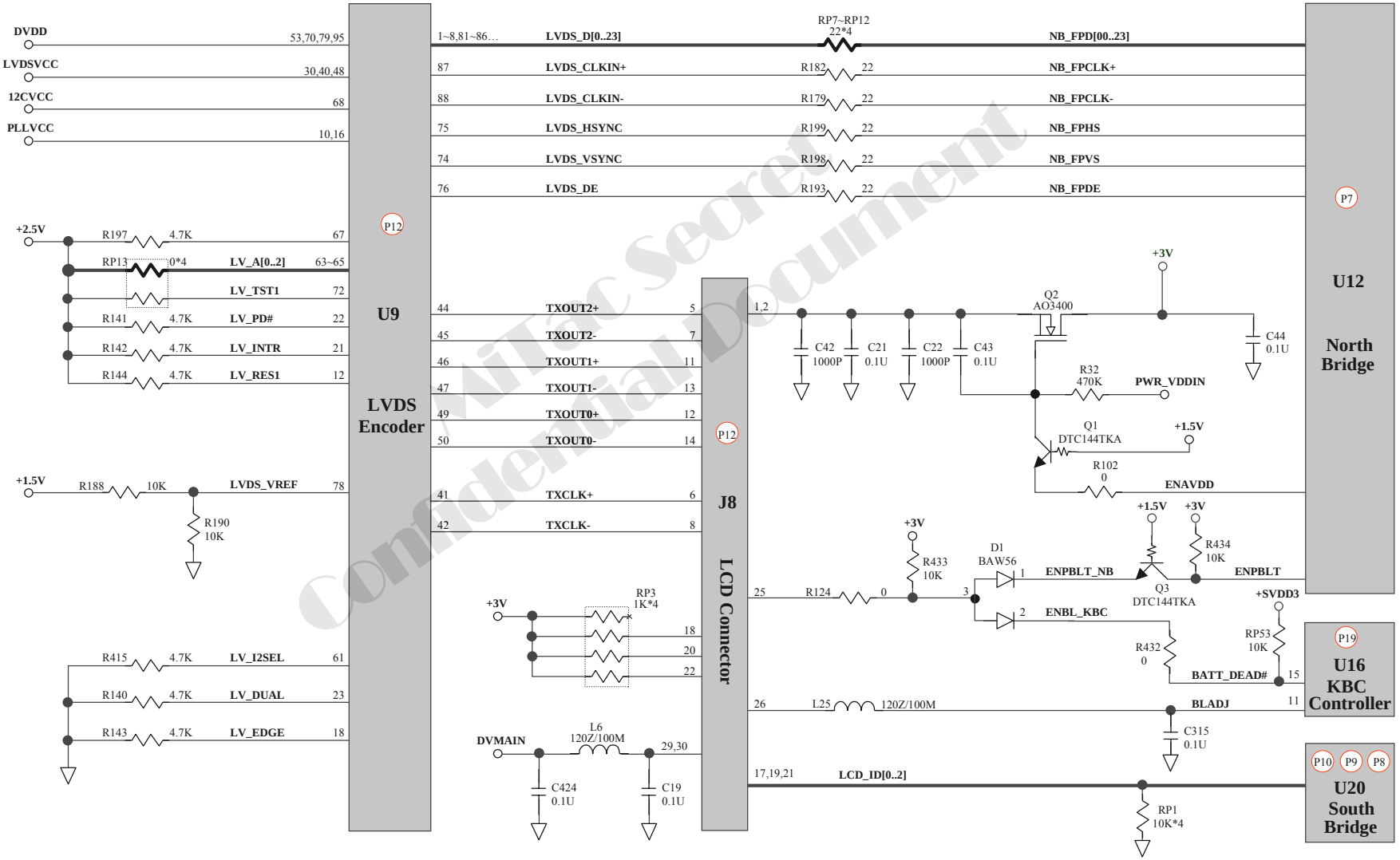
8.4 No Display(1)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



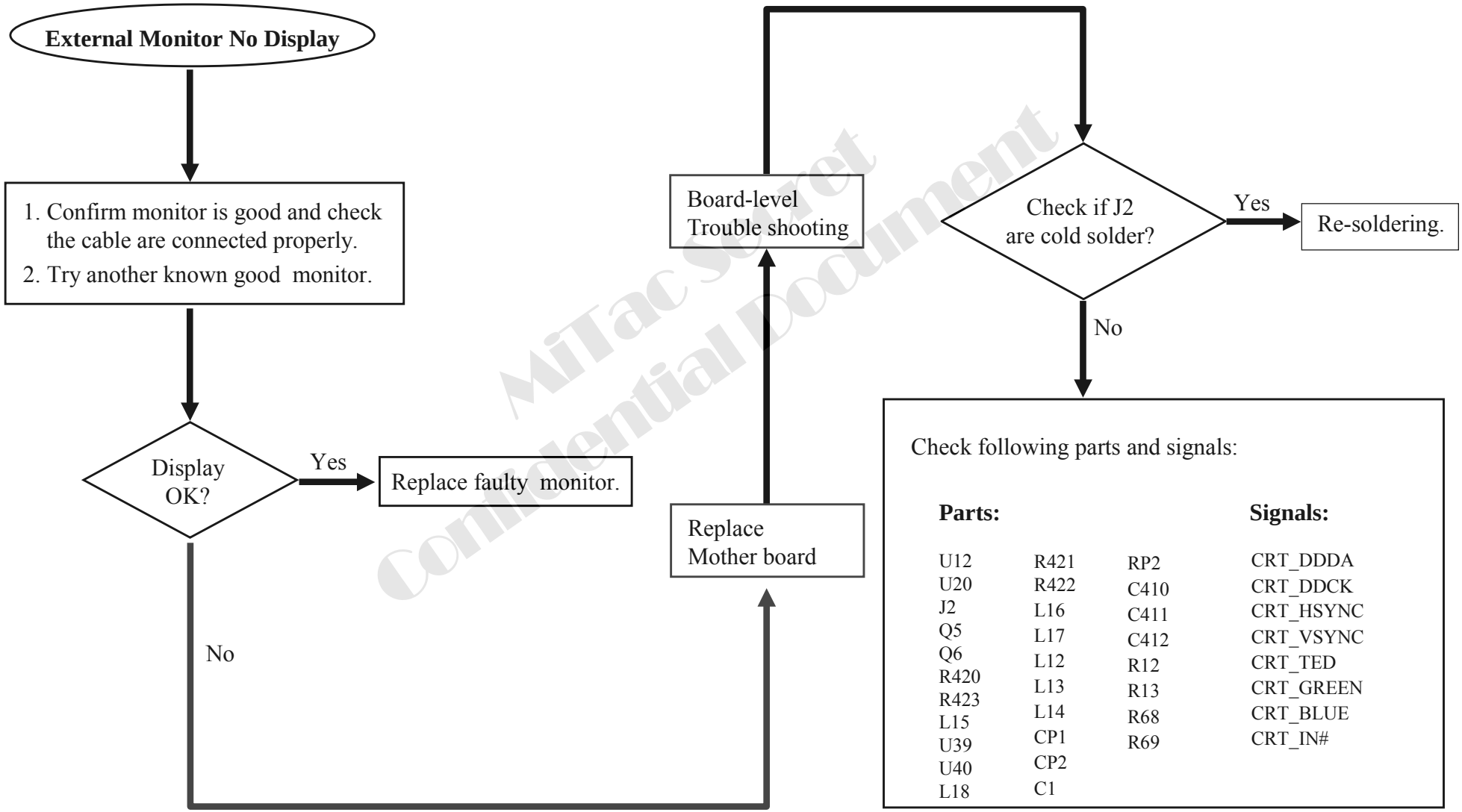
8.4 No Display(2)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



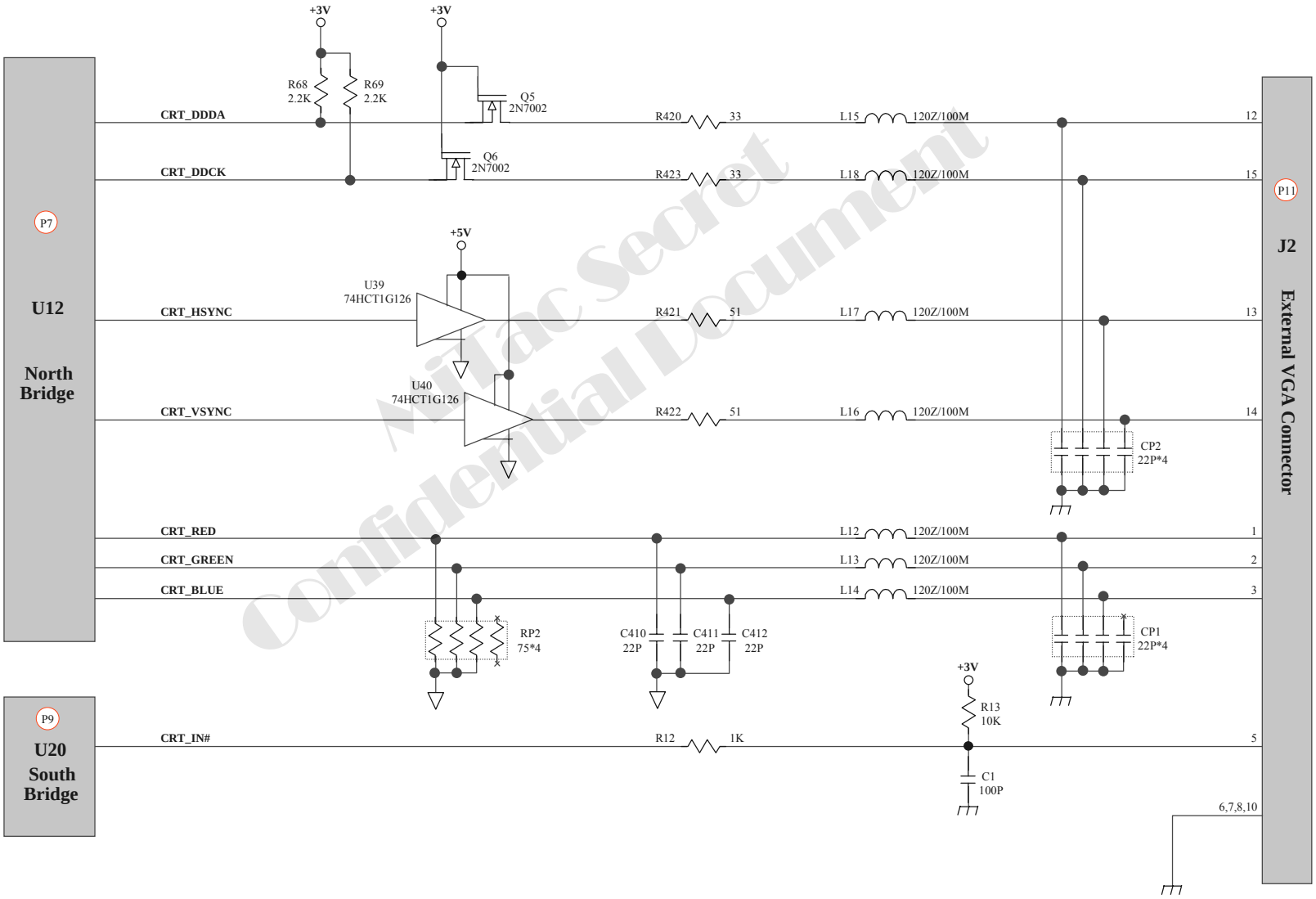
8.5 External Monitor No Display(1)

There is no display or picture abnormal on CRT monitor, but LCD can normally display.



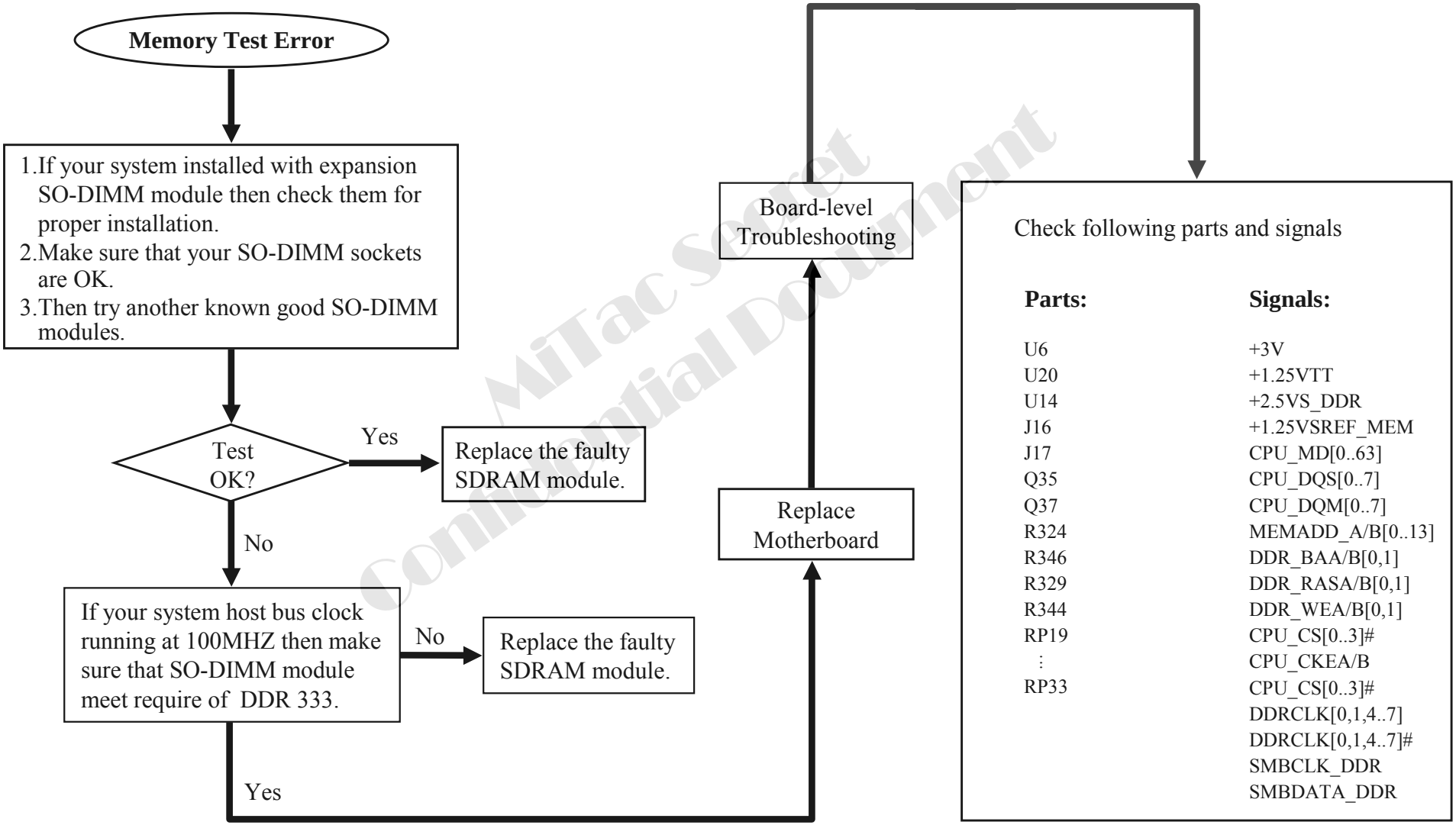
8.5 External Monitor No Display(2)

There is no display or picture abnormal on CRT monitor, but LCD can normally display.



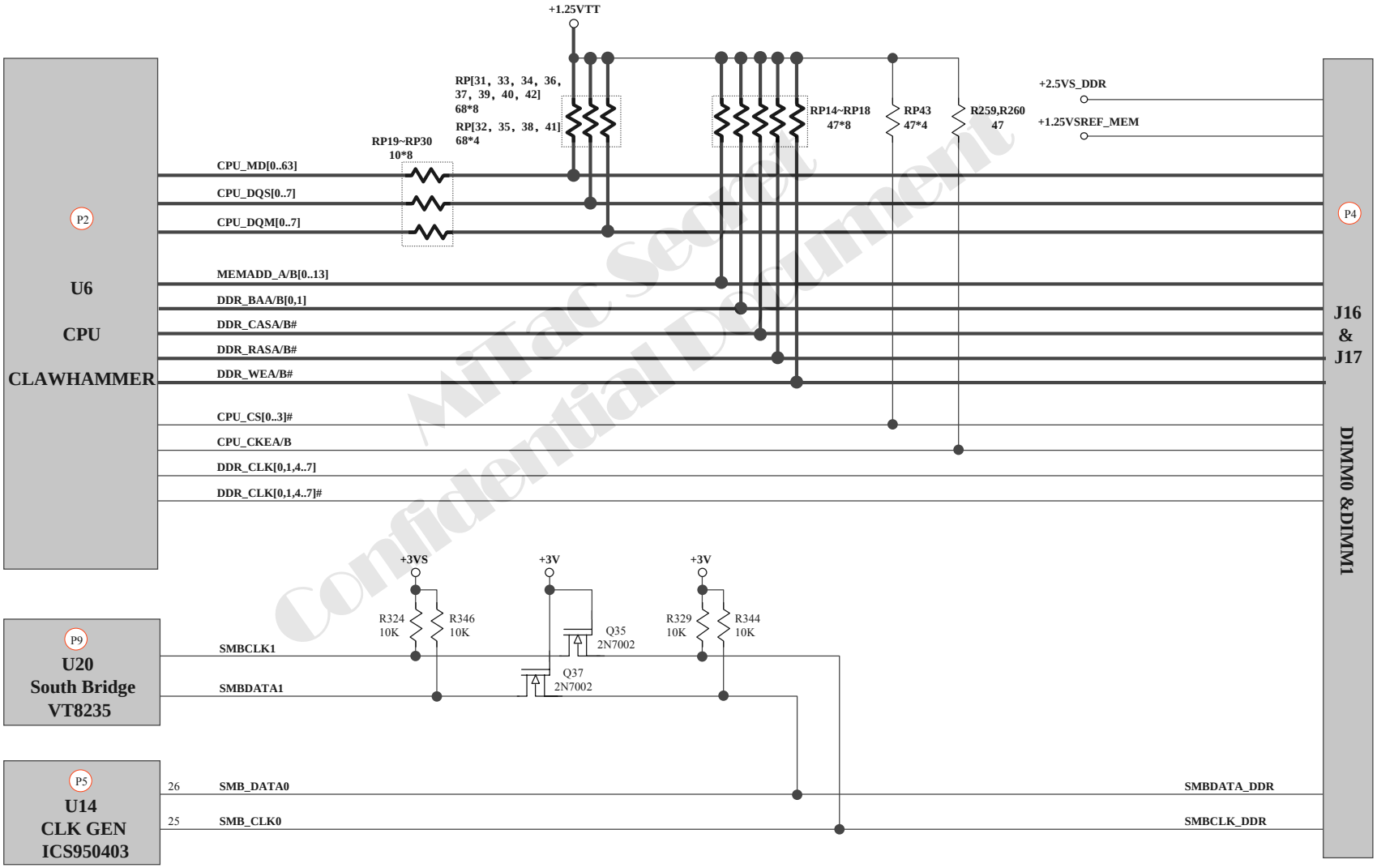
8.6 Memory Test Error(1)

Either on board or extend SDRAM is failure or system hangs up.



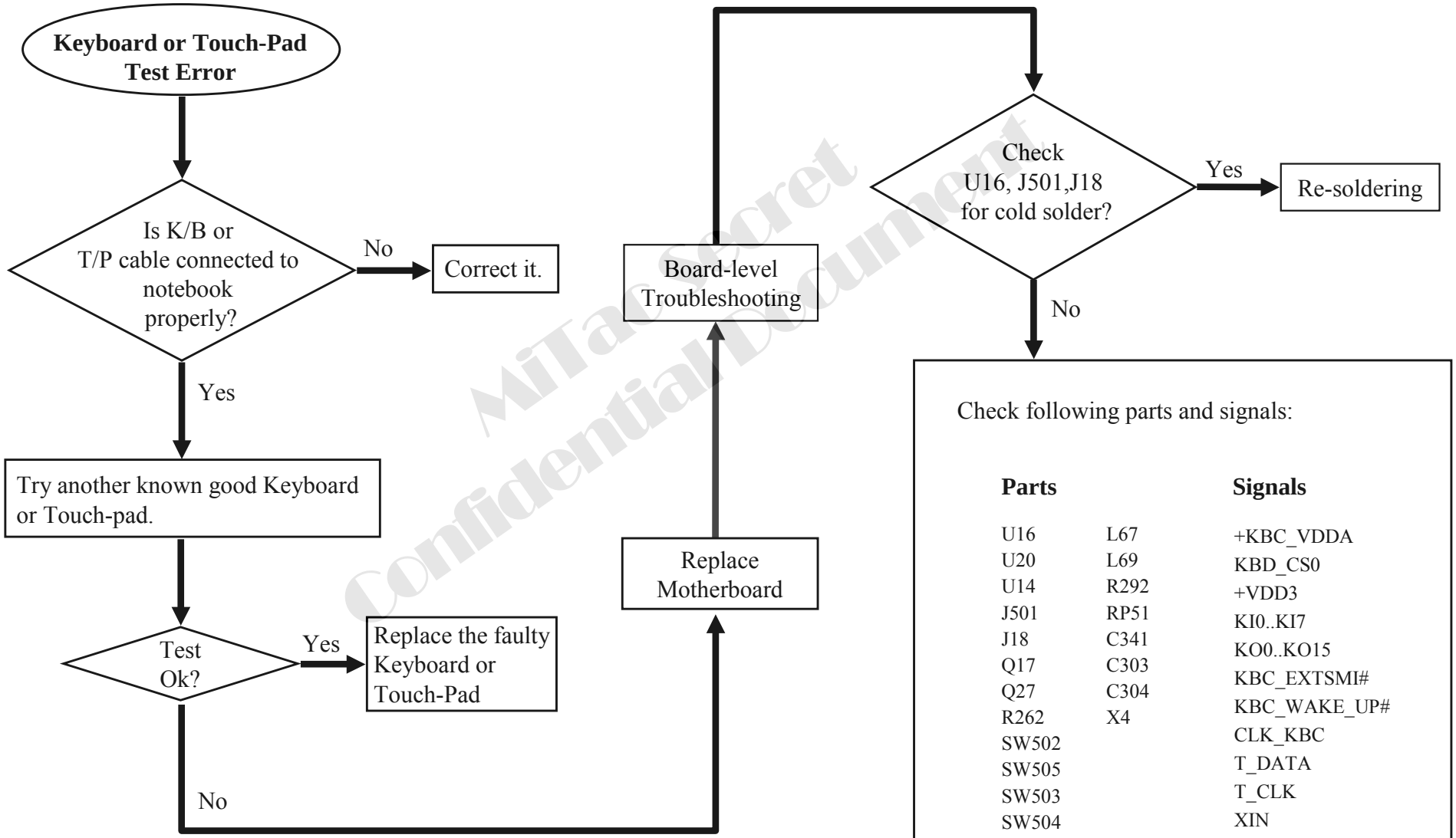
8.6 Memory Test Error(2)

Either on board or extend SDRAM is failure or system hangs up.



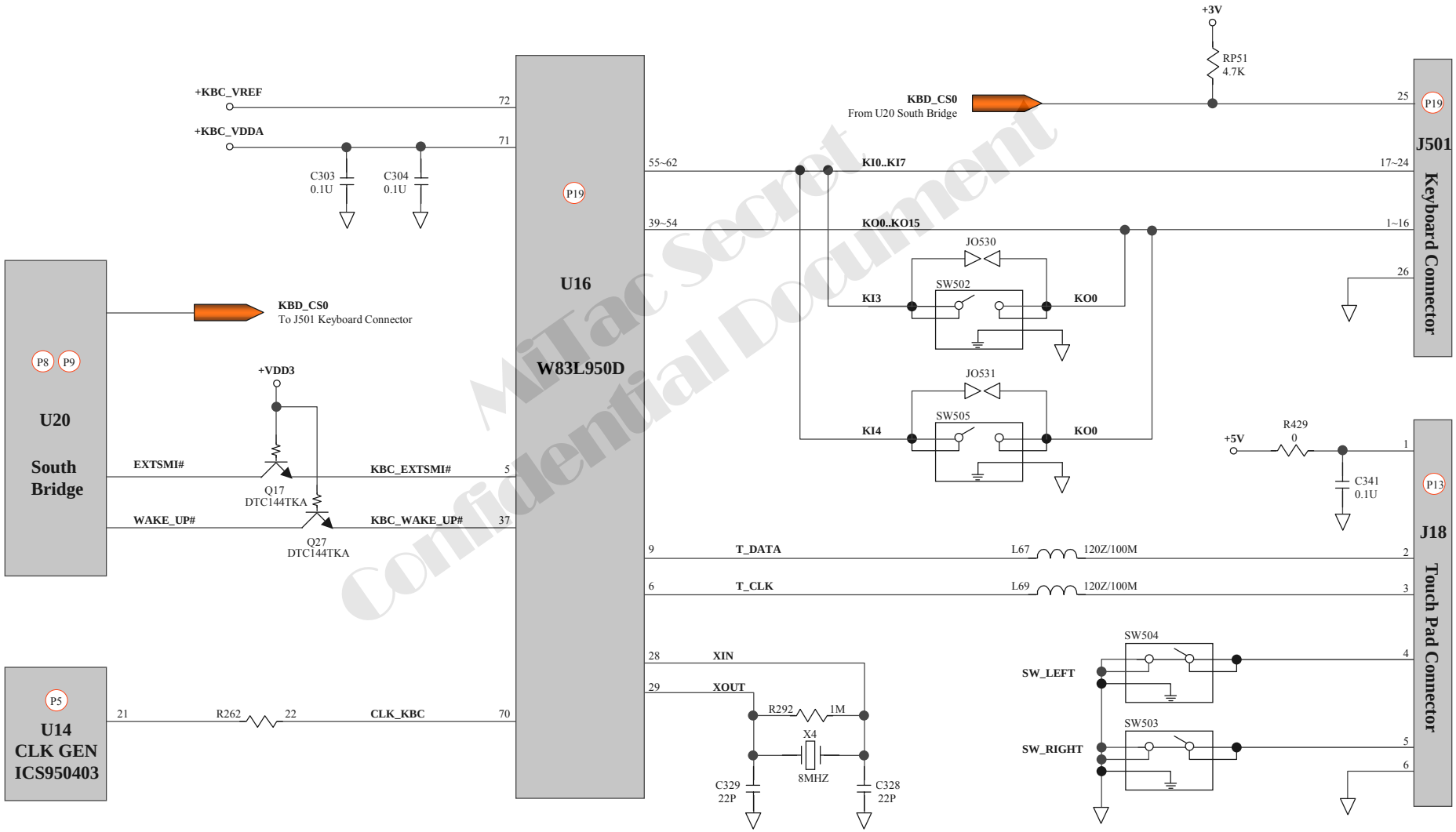
8.7 Keyboard/Touch Pad Test Error(1)

Error message of keyboard or touch-pad failure is shown or any key does not work.



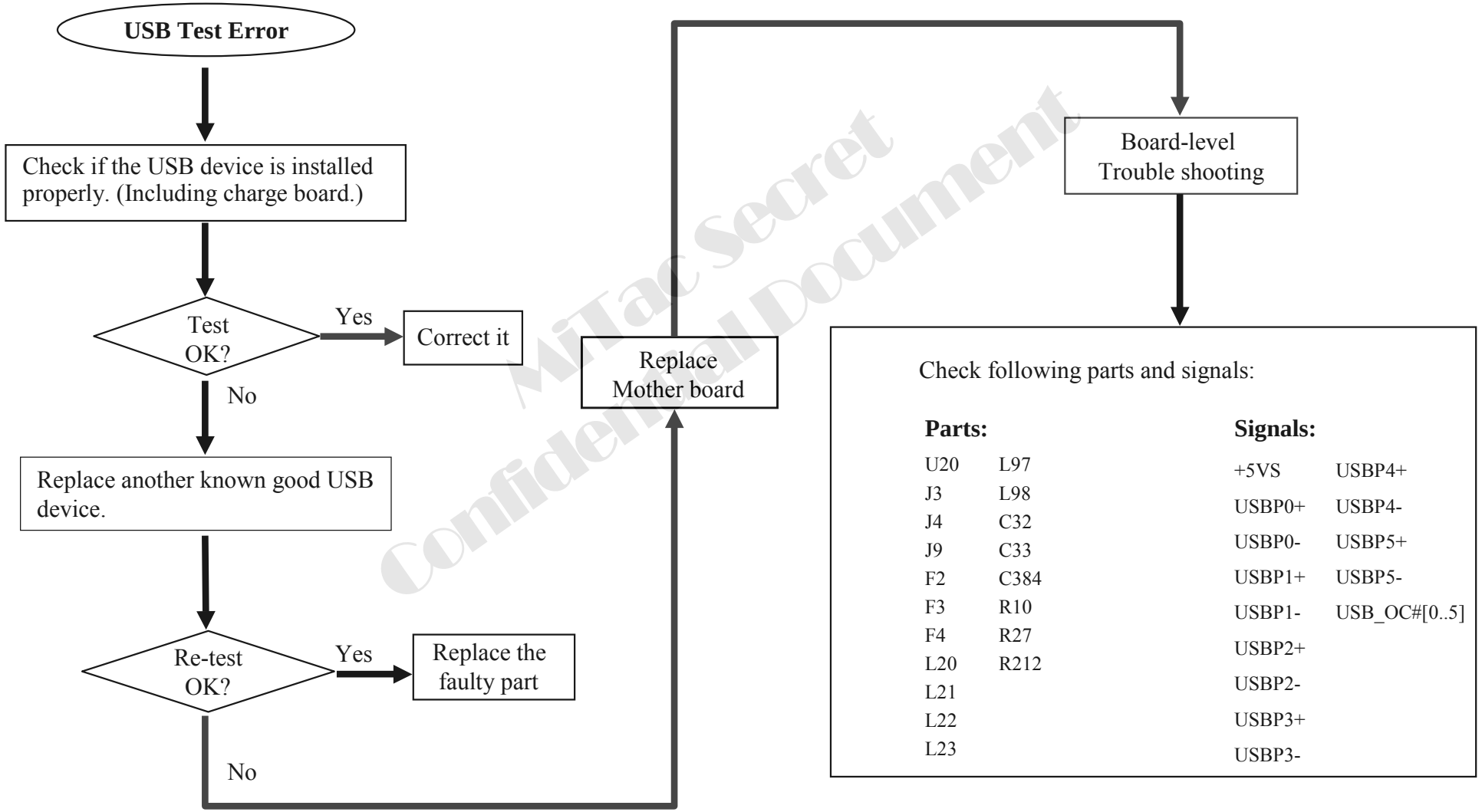
8.7 Keyboard/Touch Pad Test Error(2)

Error message of keyboard or touch-pad failure is shown or any key does not work.



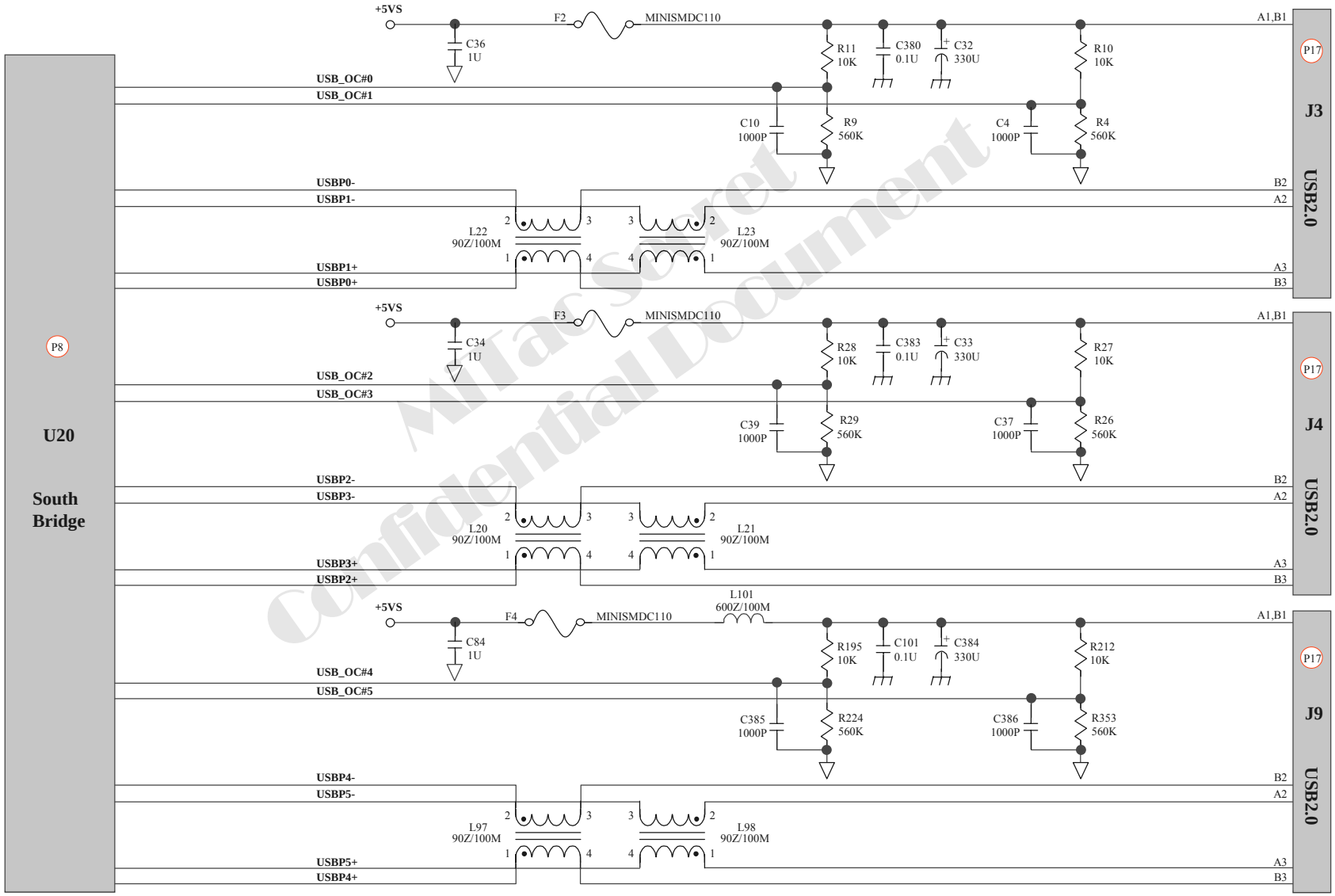
8.8 USB Port Test Error(1)

An error occurs when a USB I/O device is installed.



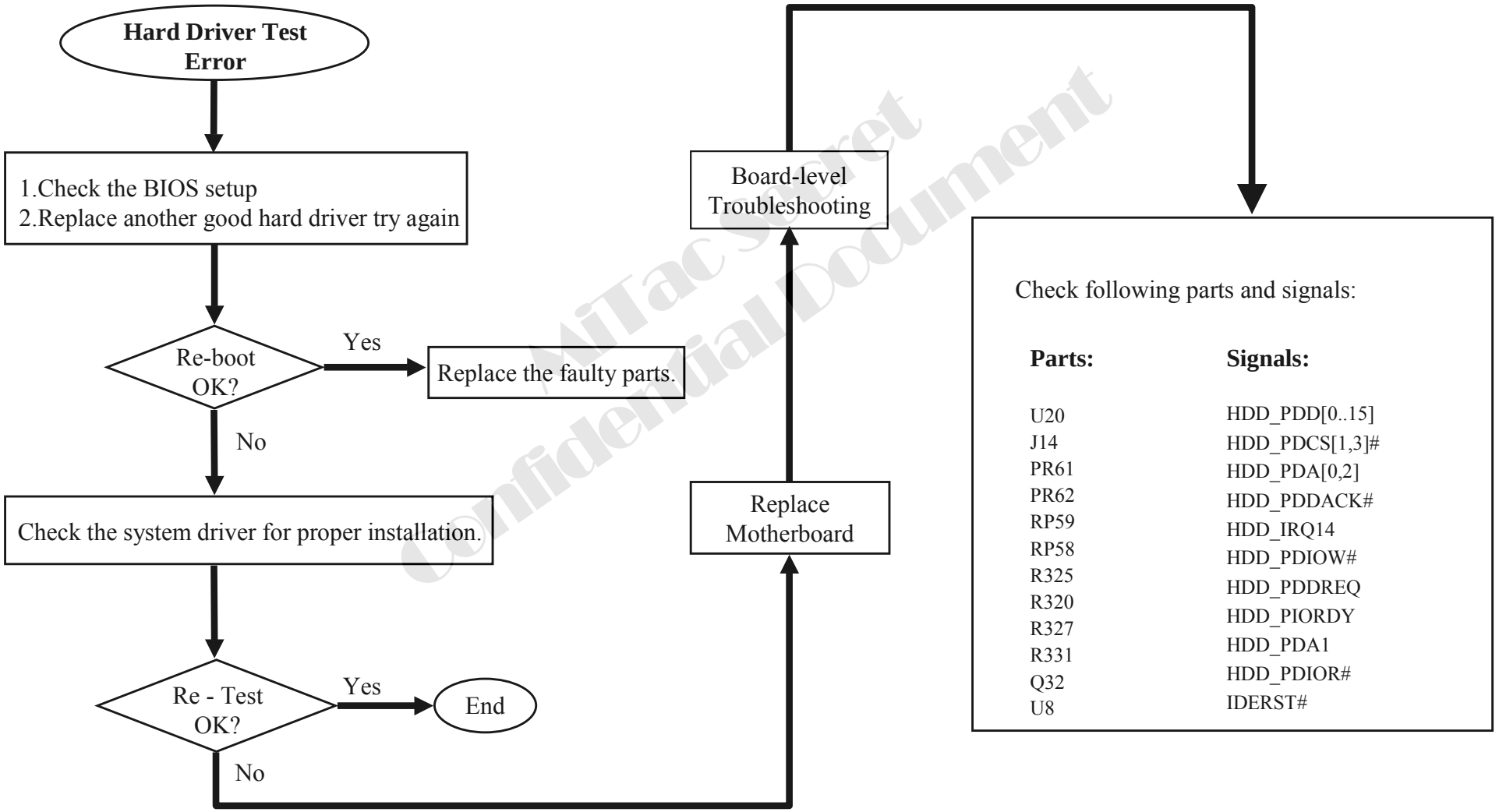
8.8 USB Port Test Error(2)

An error occurs when a USB I/O device is installed.



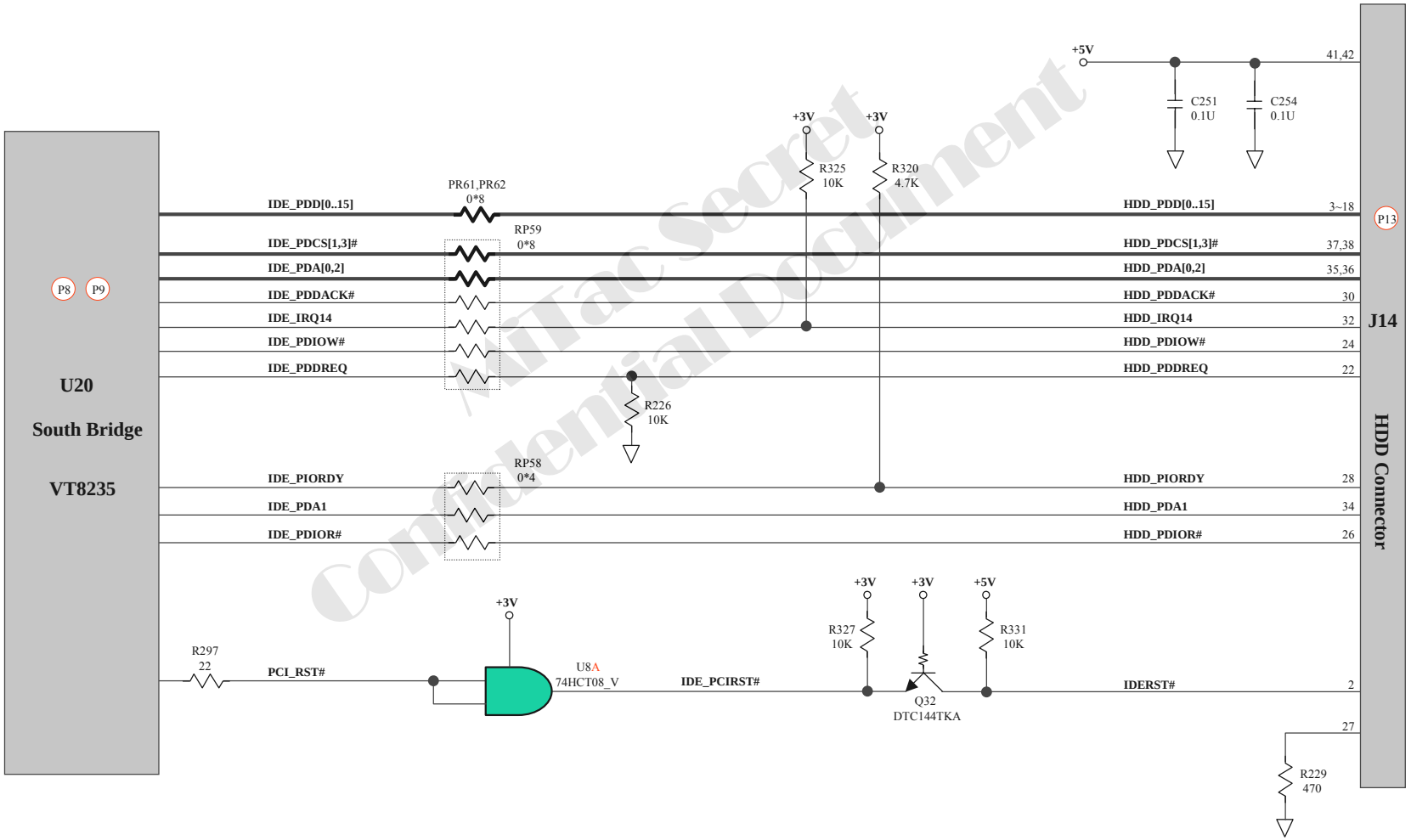
8.9 Hard Disk Driver Test Error(1)

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



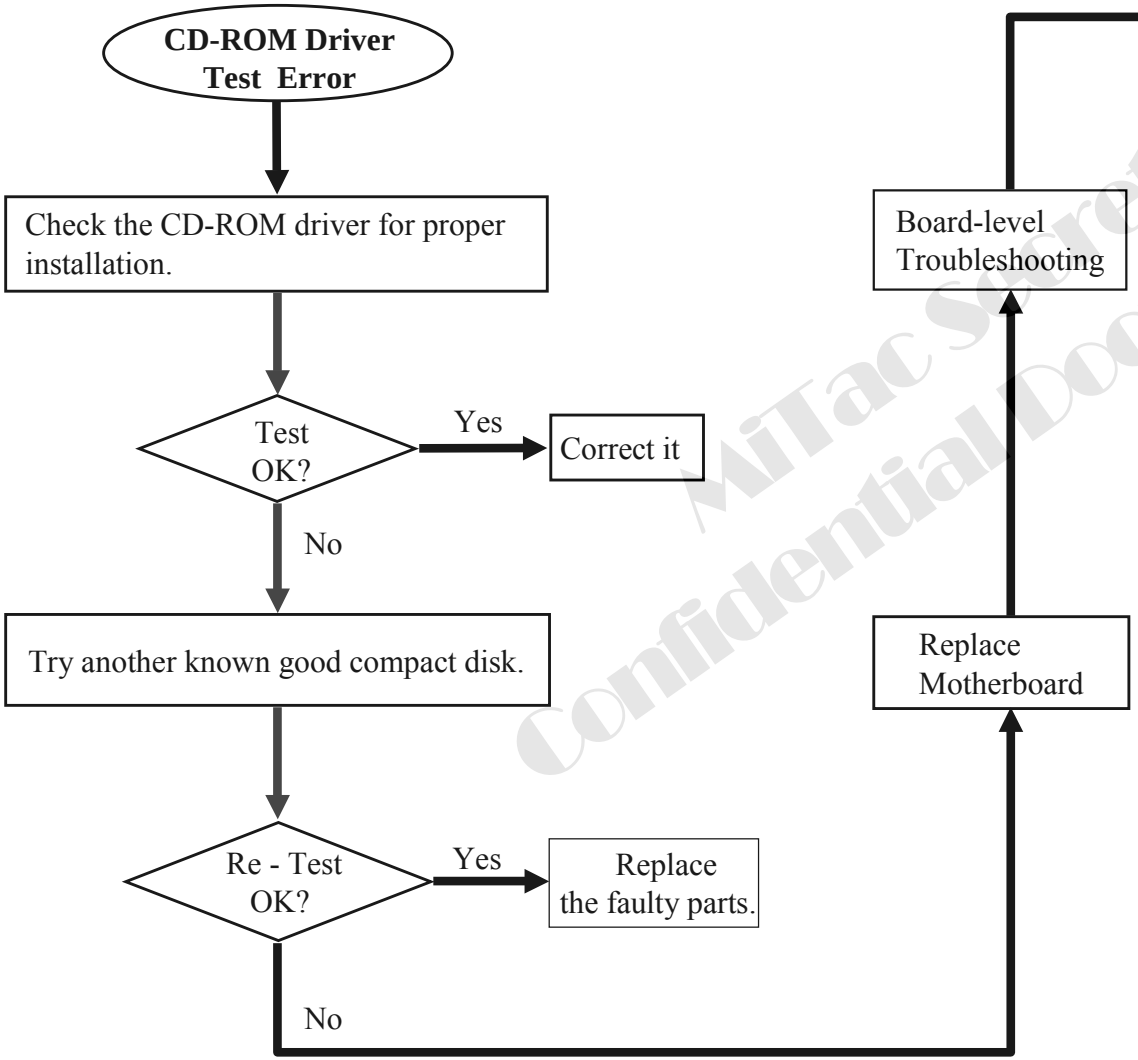
8.9 Hard Disk Driver Test Error(2)

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.10 CD-ROM Driver Test Error(1)

CD-ROM driver can't run normally,maybe an error message is shown when reading data from CD-ROM.

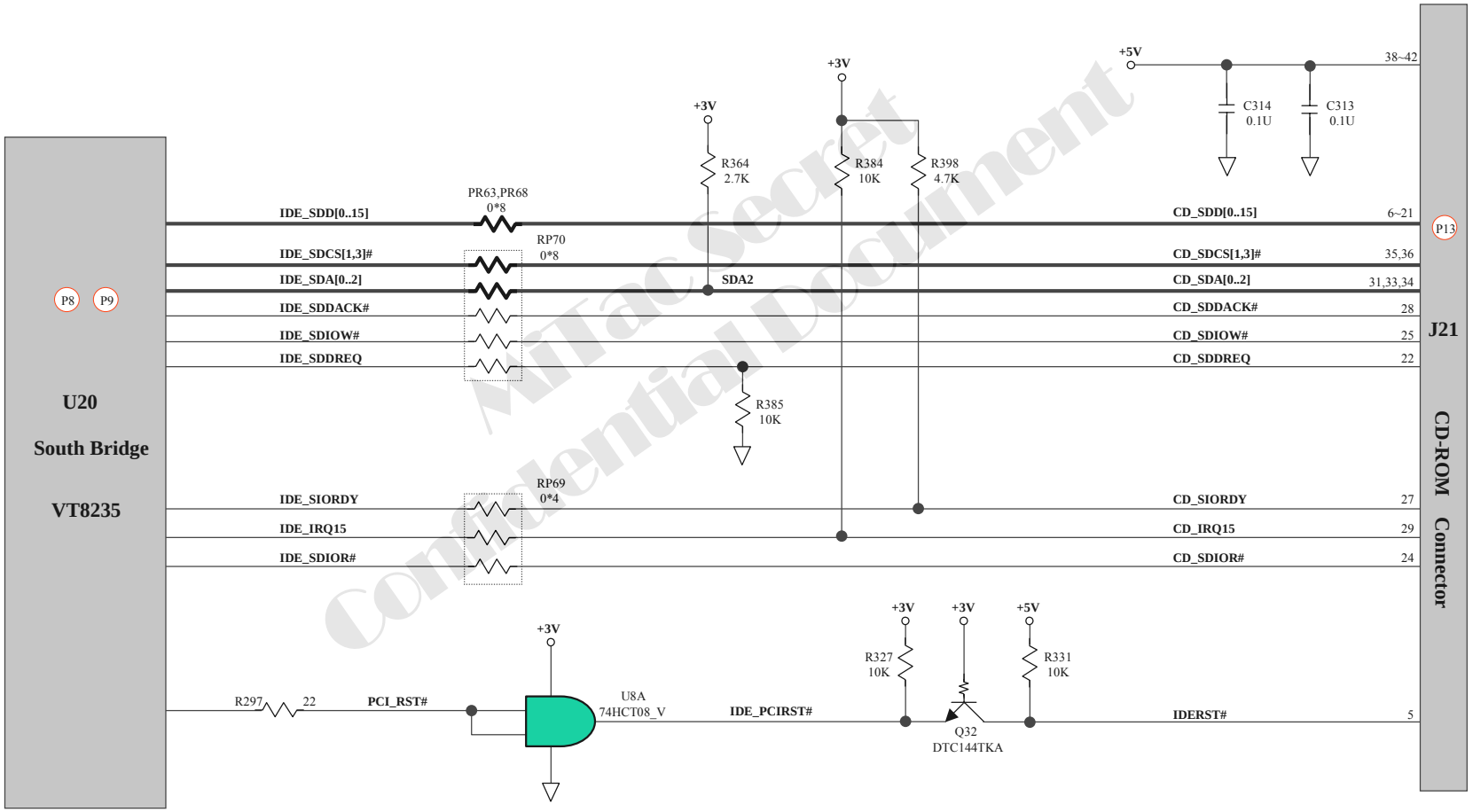


Check following parts and signals:

Parts:	Signals:
U20	CD_SDD[0..15]
J21	CD_SDCS[1,3]#
PR63	CD_SDA[0..2]
PR68	CD_SDDACK#
RP69	CD_SDIOW#
RP70	CD_SDDREQ
R384	CD_SIORDY
R398	CD_IRQ15
R327	CD_SDIOR#
R331	PCI_RST#
Q32	
U8	

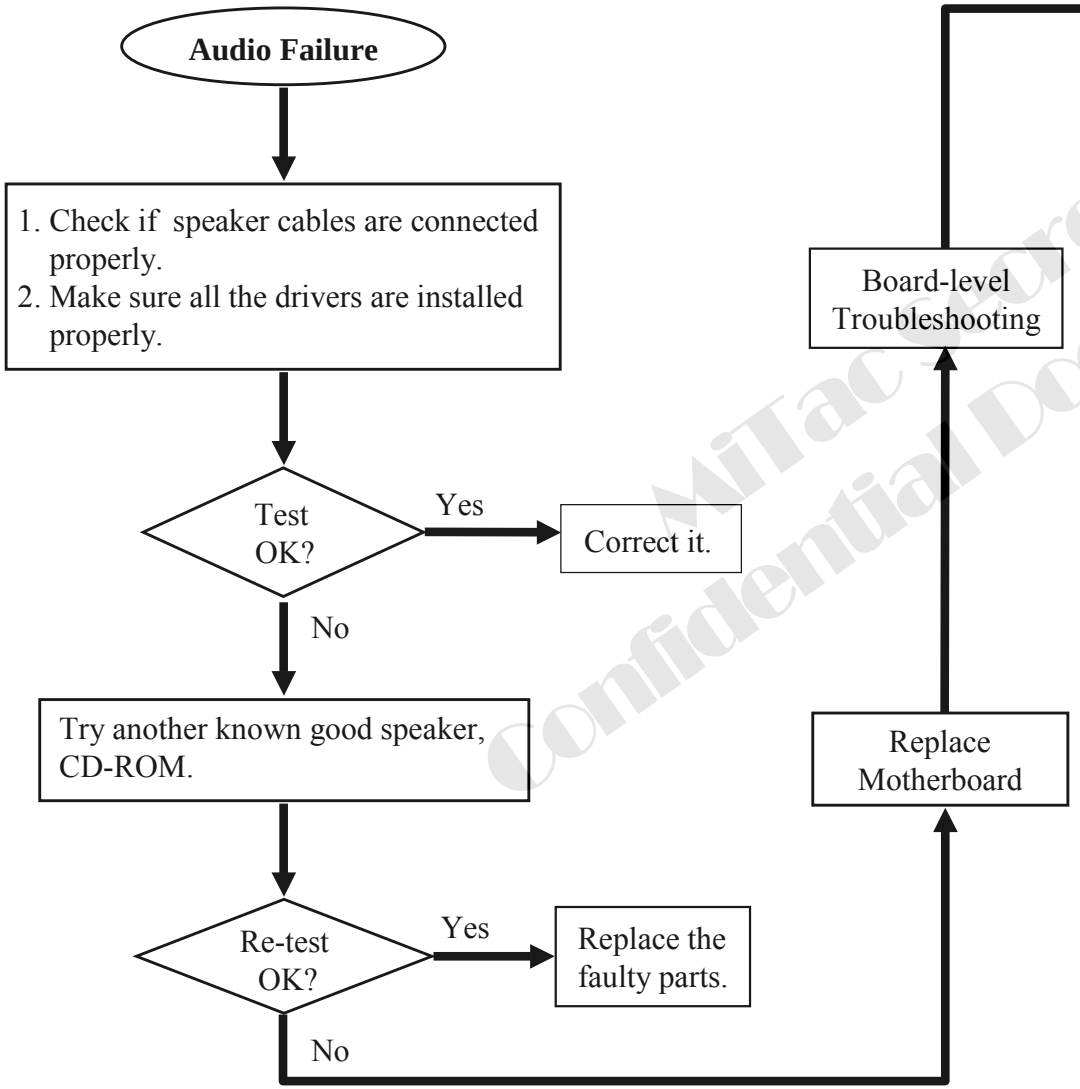
8.10 CD-ROM Driver Test Error(2)

CD-ROM driver can't run normally,maybe an error message is shown when reading data from CD-ROM.



8.11 Audio Failure(1)

There is trouble with the sound from speaker or completely no sound.

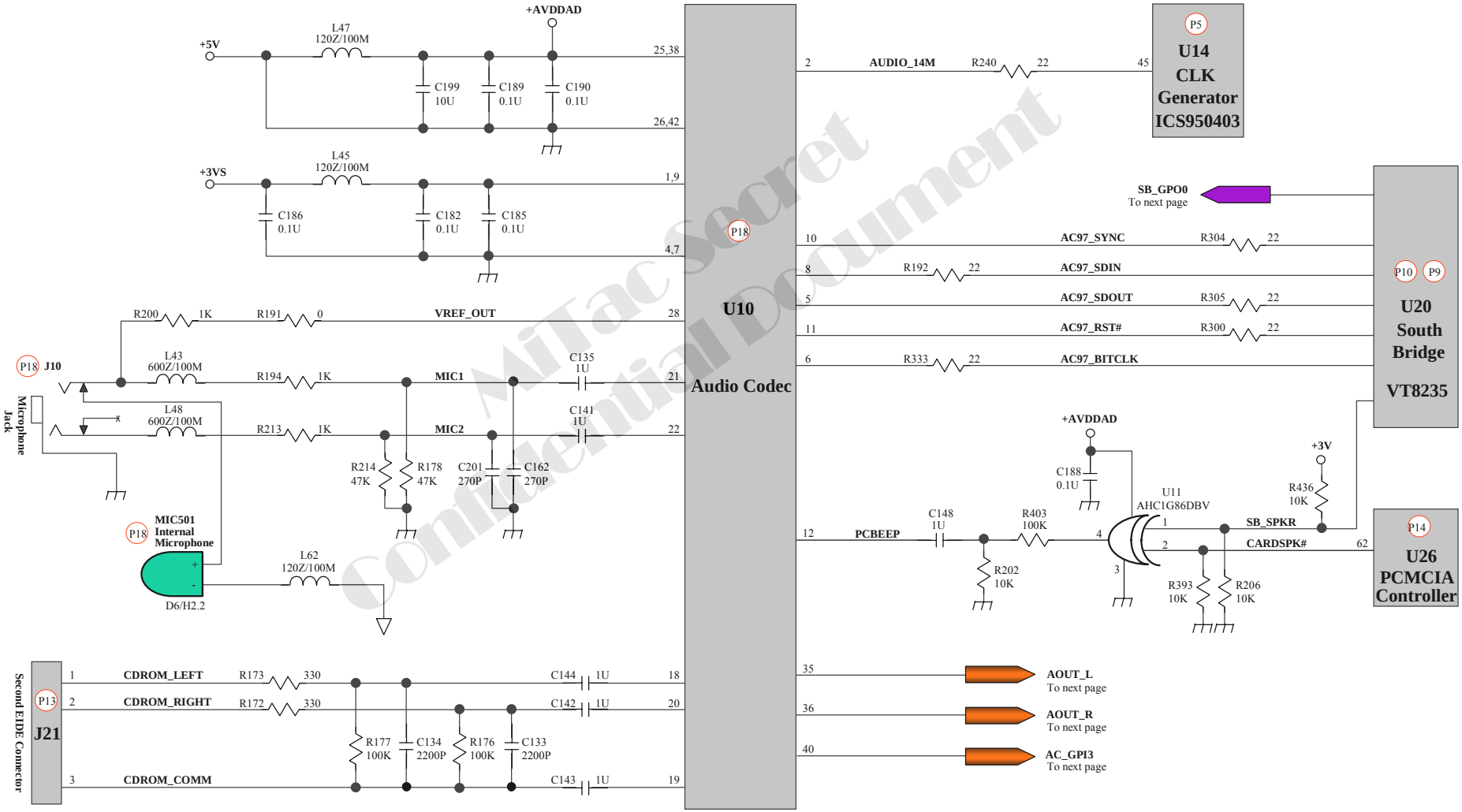


Check following parts and signals:

Parts:		**Signals:**	
U10	C148	+AVDDAD	AOUT_R
U14	R403	VREF_OUT	AC_GPI3
U26	U11	MIC1	TP534
U13	L52	MIC2	+5V_AMP
J13	R205	CDROM_LEFT	SHUTDOWN
J21	Q13	CDROM_RIGHT	SPKR_ROUT+
L45	C235	CDROM_ROMM	SPKR_ROUT-
L47	J12	AUDIO_14M	SPKR_LOUT+
L48	L39	AC97_SYNC	SPKR_LOUT-
L43	L41	AC97_SDIN	HP_SENSE
R200	L50	AC97_SDOUT	
R191	L51	AC97_RST#	
R194	L53	AC97_BITCLK	
R213	⋮	SB_SPKR	
L62	L56	CARDSPK#	
R172		AOUT_L	
R173			

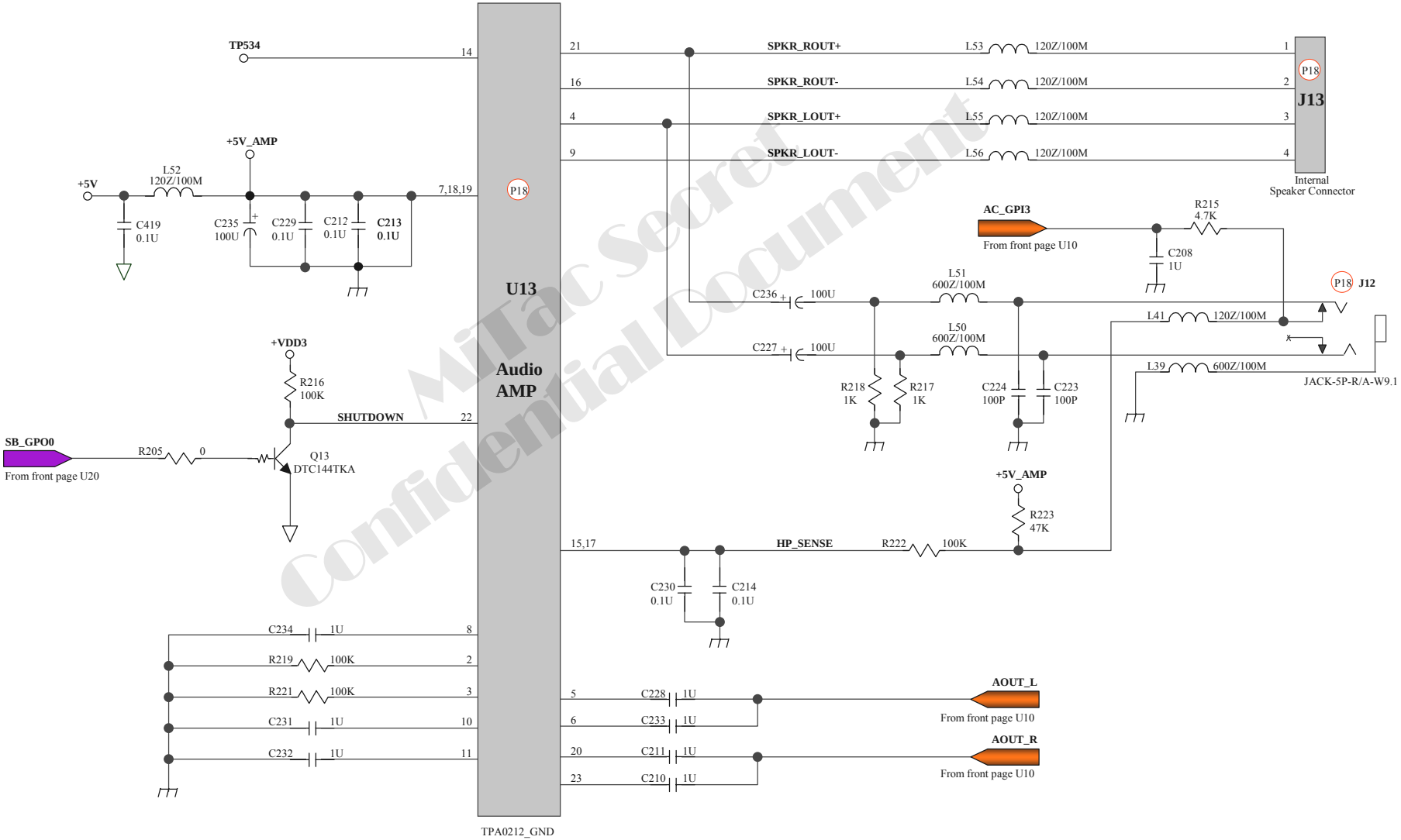
8.11 Audio Failure(2)--Audio In

There is trouble with the sound from speaker or completely no sound



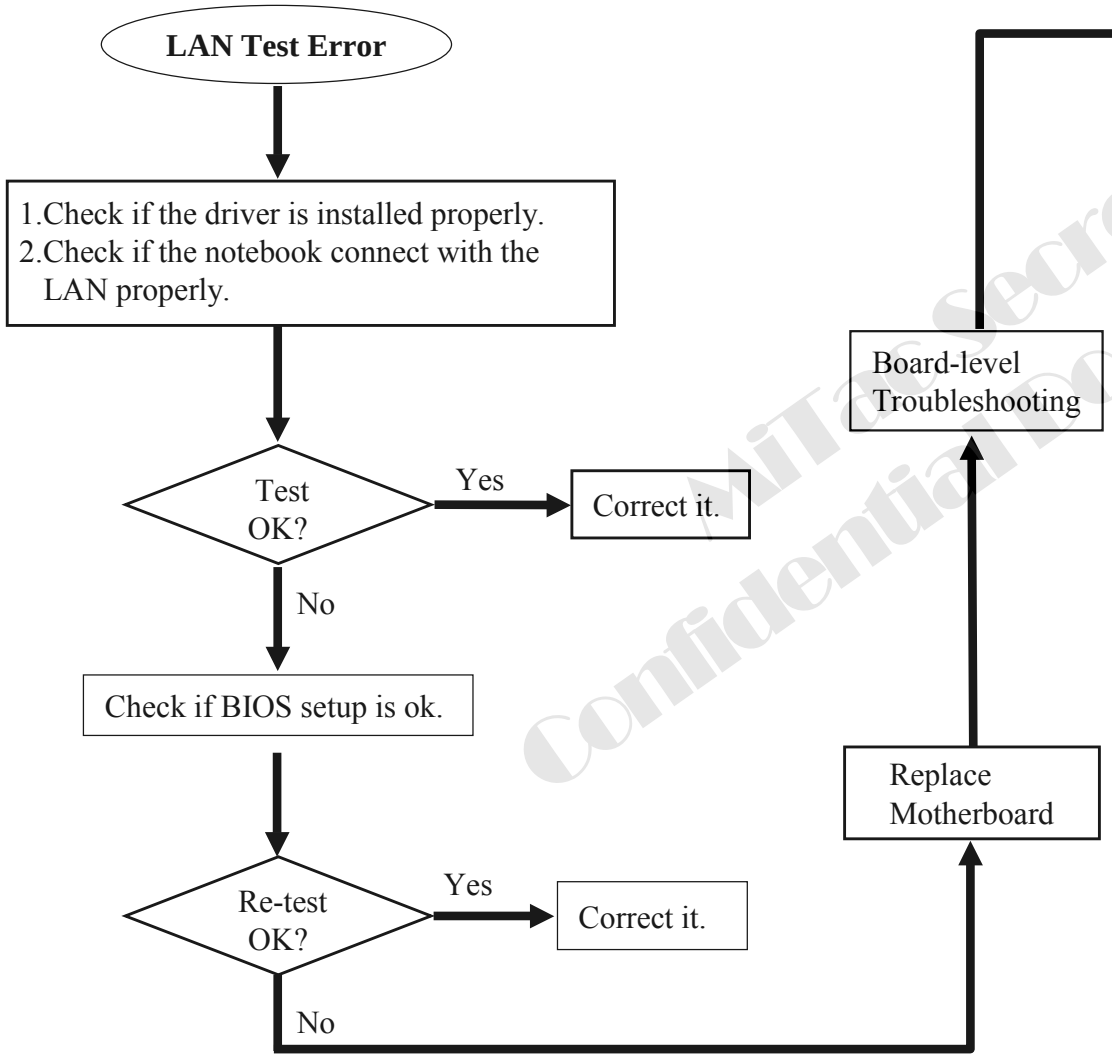
8.11 Audio Failure(3)--Audio Out

There is trouble with the sound from speaker or completely no sound



8.12 LAN Test Error(1)

An error occurs when a LAN device is installed.

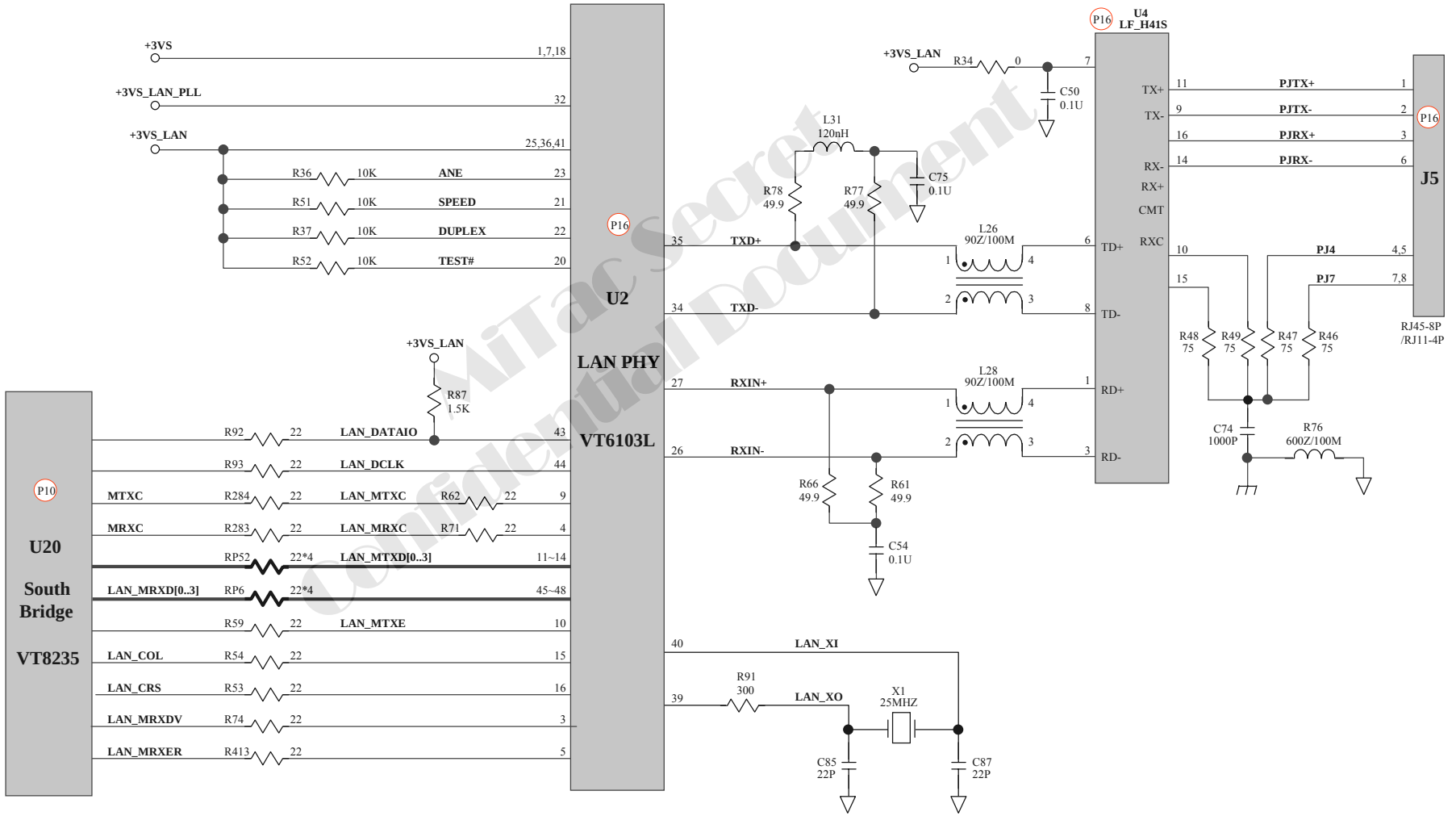


Check following parts and signals:

Parts:		Signals:	
U2	R283	+3VS	LAN_MTXD[0..3]
U4	R284	+3VS_LAN_PLL	LAN_MRXD[0..3]
U20	RP52	+3VS_LAN	LAN_MTXE
J5	RP6	TXD+	LAN_COL
L26	R59	TXD-	LAN_CRS
L28	R54	RXIN+	LAN_MRXDV
X1	R53	RXIN-	LAN_MRXER
R36	R74	PJTX+	LAN_XI
R51	R413	PJTX-	LAN_XO
R37	R46	PJRX+	
R52	⋮	PJRX-	
R34	R49	LAN_DATAIO	
R87	C85	LAN_DCLK	
R92	C87	LAN_MTXC	
R93	C74	LAN_MRXC	

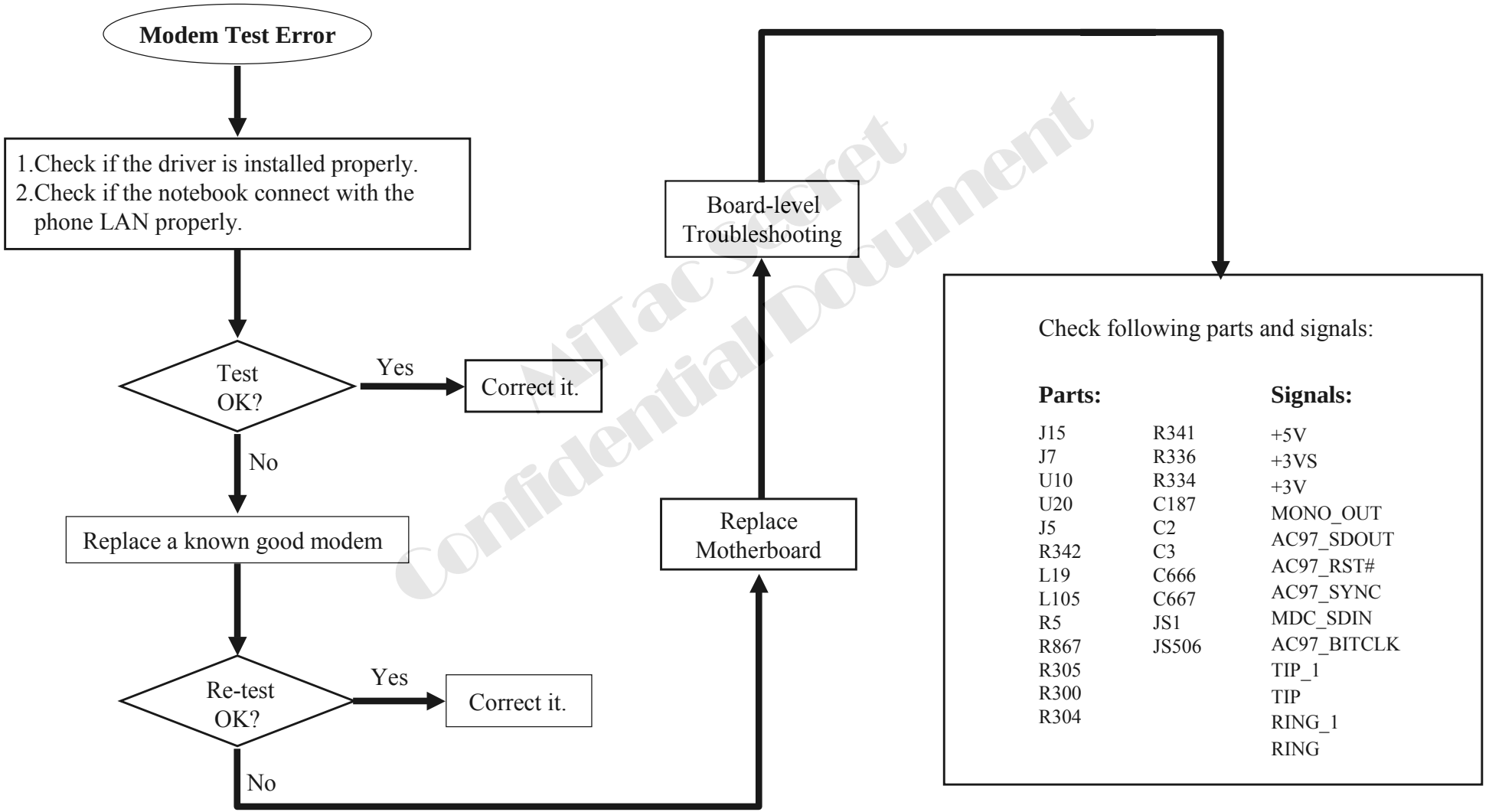
8.12 LAN Test Error(2)

An error occurs when a LAN device is installed.



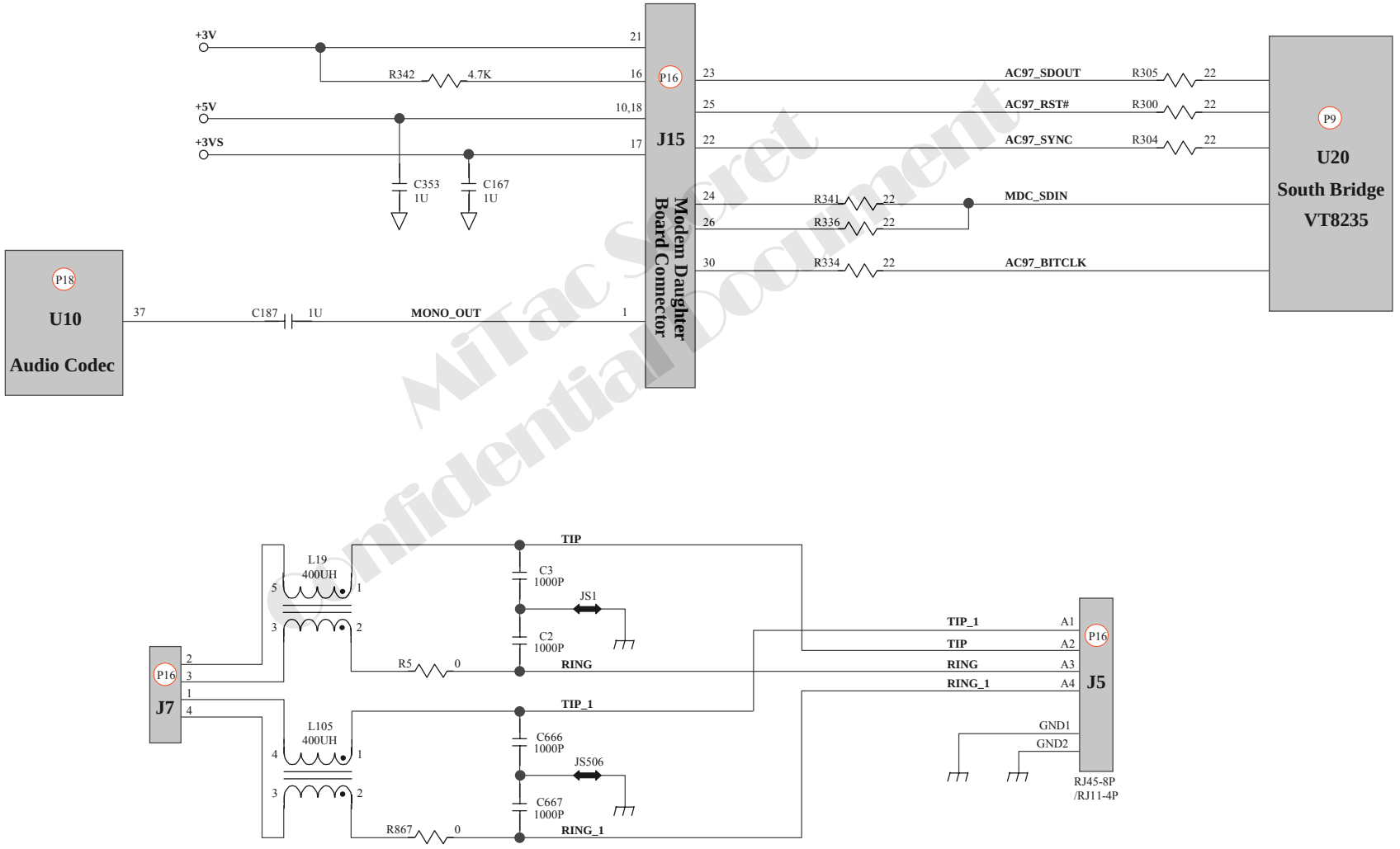
8.13 Modem Test Error(1)

An error occurs when run the modem



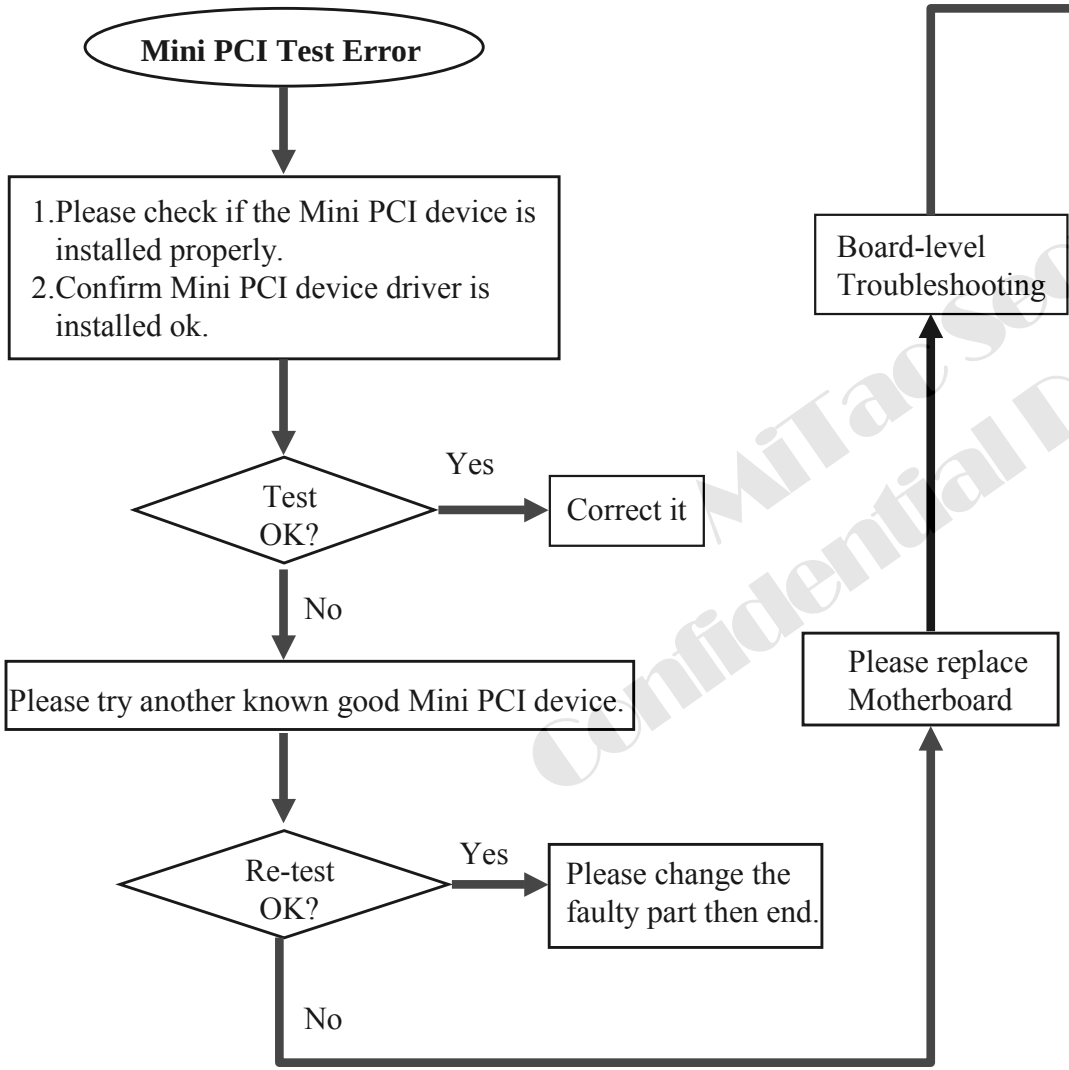
8.13 Modem Test Error(2)

An error occurs when run the modem



8.14 Mini PCI Test Error(1)

An error message is shown after Mini PCI device is installed or the Mini PCI device does't work.

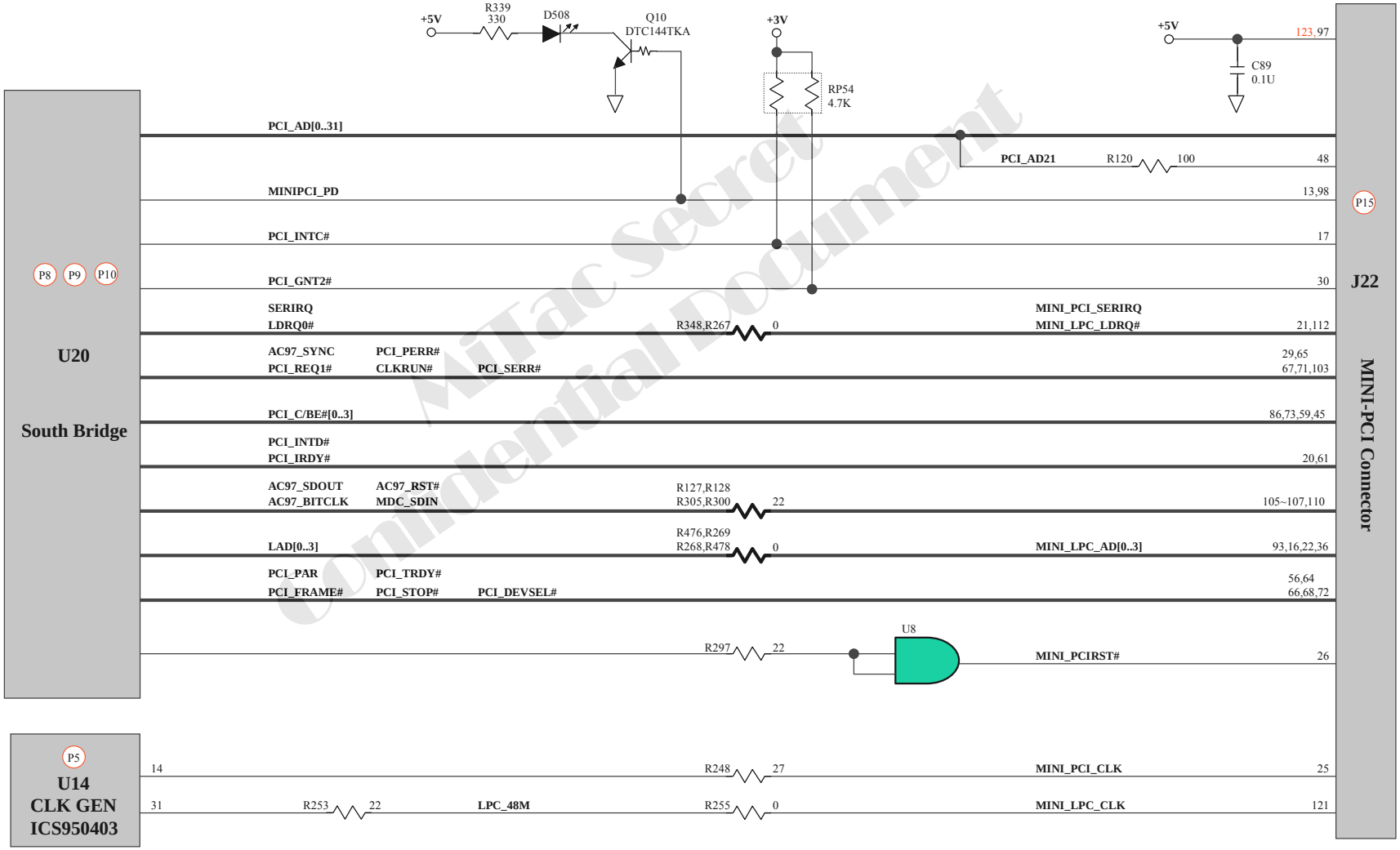


Check following parts and signals:

Parts:	Signals	
U20	PCI_AD[0..31]	AC97_BITCLK
U14	PCI_C/BE# [0..3]	MDC_SDIN
J22	MINIPCI_PD	LAD[0..3]
Q10	PCI_INTC#	PCI_PAR
U8	PCI_GNT2#	PCI_TRDY#
R248	SERIRQ	PCI_FRAME#
R255	LDRQ0#	PCI_STOP#
R297	AC97_SYNC	PCI_DEVSEL#
R348	PCI_PERR#	MINI_PCIRST#
R267	PCI_REQ1#	MINI_PCI_CLK
R127	CLKRUN#	MINI_LPC_CLK
R128	PCI_SERR	
R300	PCI_INTD#	
R305	PCI_IRDY#	
R268	AC97_SDOUT	
R476	AC97_RST#	
R478		

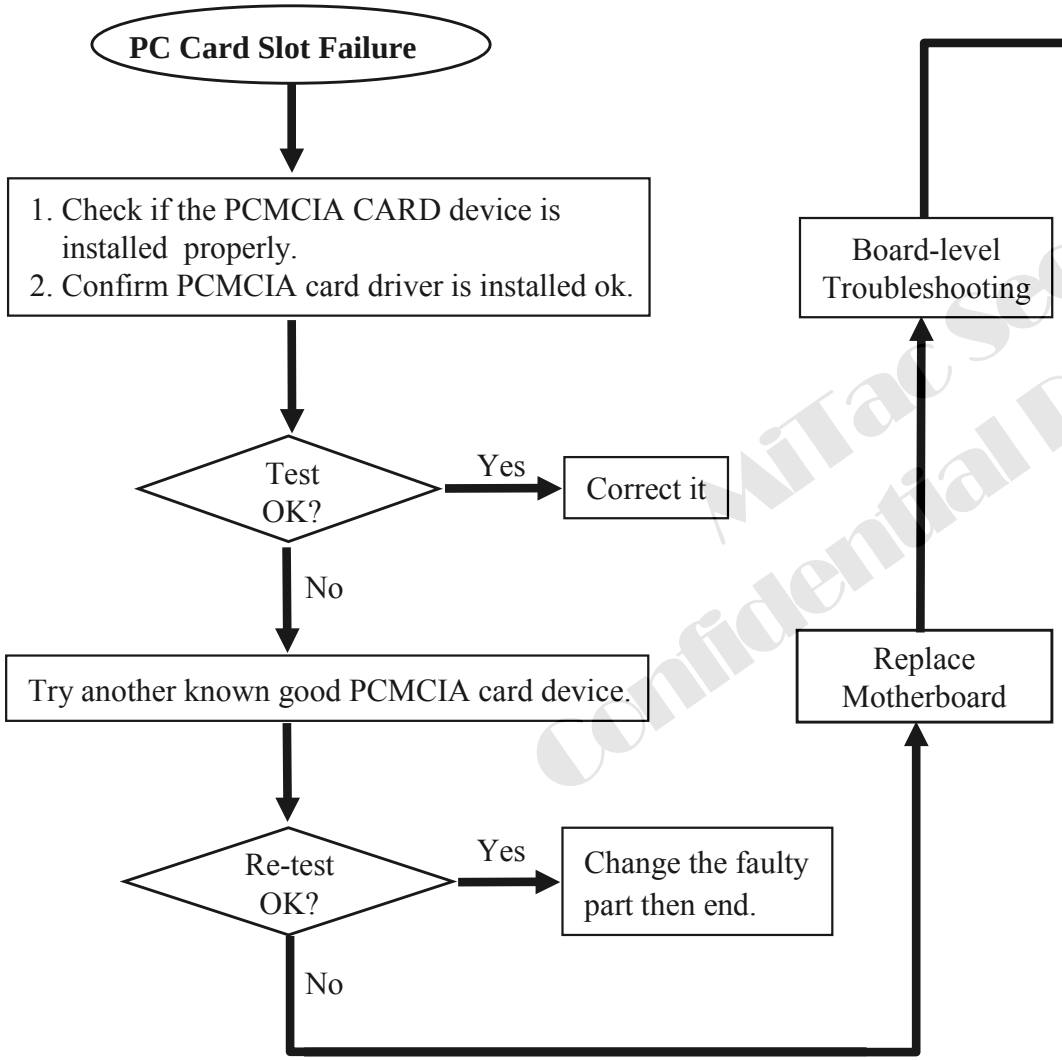
8.14 Mini PCI Test Error(2)

An error message is shown after Mini PCI device is installed or the Mini PCI device does't work.



8.15 CardBus & Reader Test Error(1)

An error occurs when a PC card device is installed.

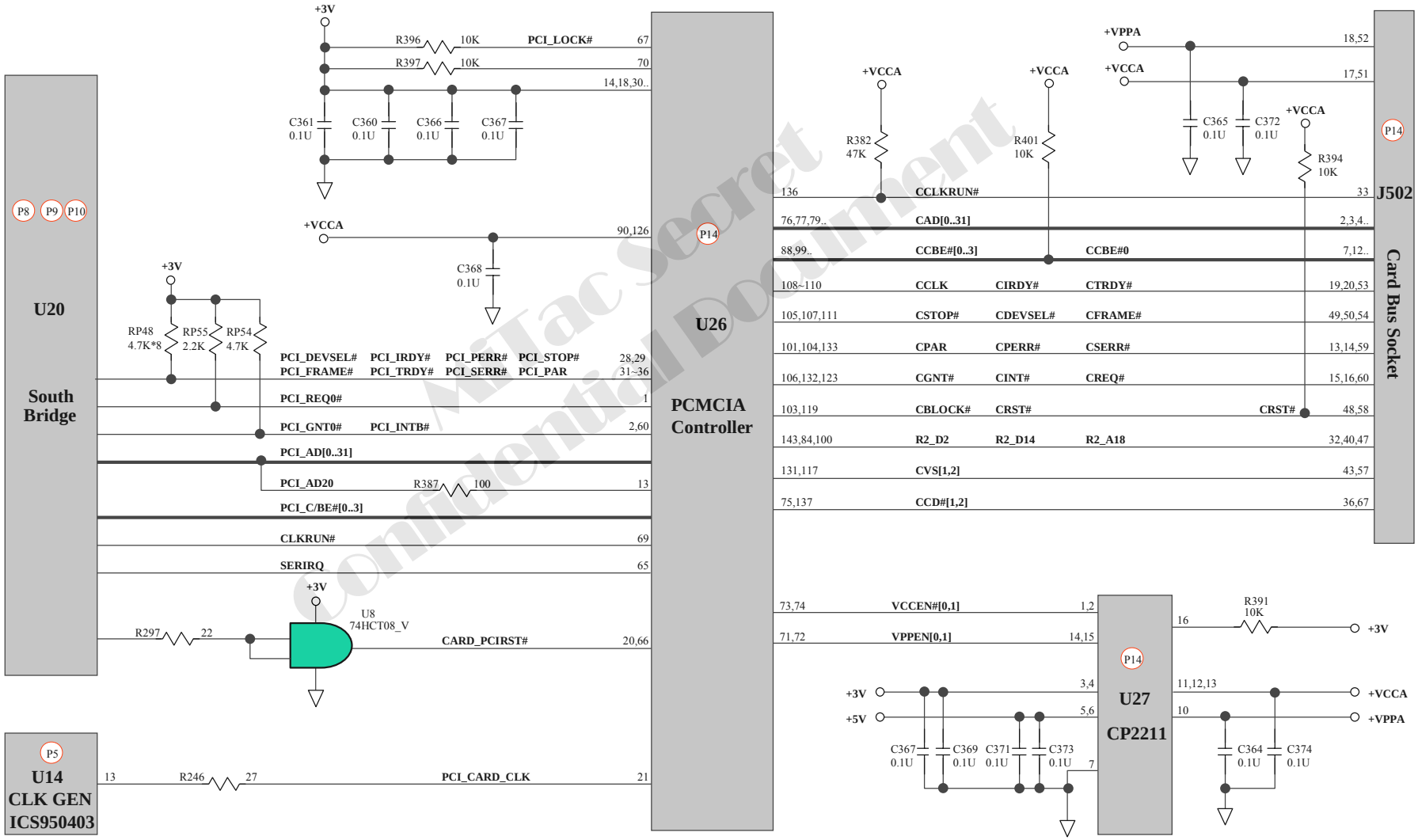


Check following parts and signals:

Parts:	Signals	
U20	+VCCA	CGNT#
U26	+VPPA	CINT#
U14	CCLKRUN#	CREQ#
J502	CAD[0..31]	CBLOCK#
U27	CCBE#[0..3]	CRST#
R396	CCLK	R2_D2
R397	CIRDY#	R2_D14
RP48	CTRDY#	R2_A18
RP54	CSTOP#	CVS[1,2]
RP55	CDEVSEL#	CCD#[1,2]
R297	CFRAME#	CARD_PCIRST#
U8	CPAR	PCI_CARD_CLK
R246	CPERR#	
R382	CSERR#	
R391		

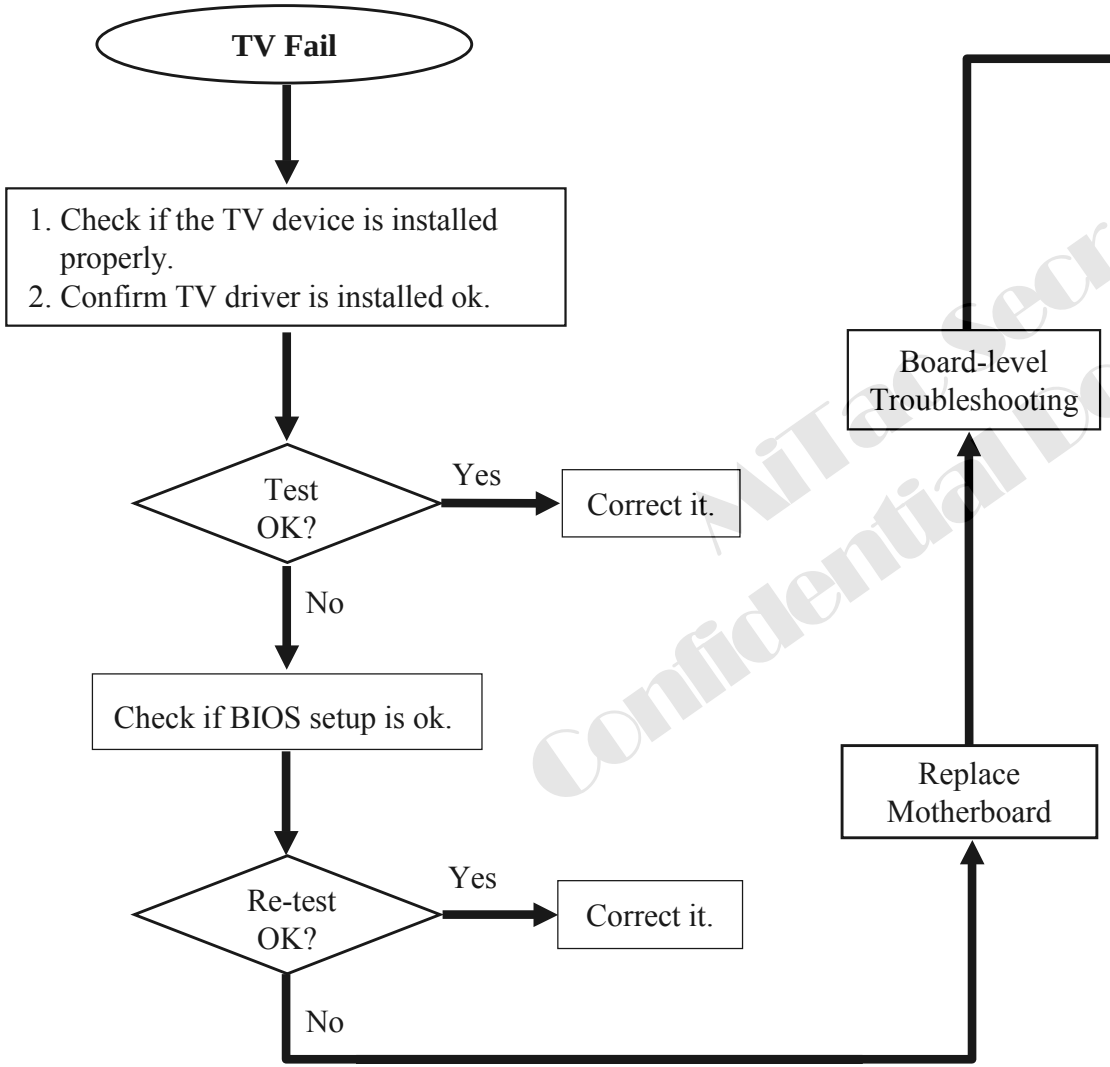
8.15 CardBus & Reader Test Error(2)

An error occurs when a PC card device is installed.



8.16 TV Encoder Test Error(1)

An error occurs when using the computer as TV.



Check following parts and signals:

Parts:

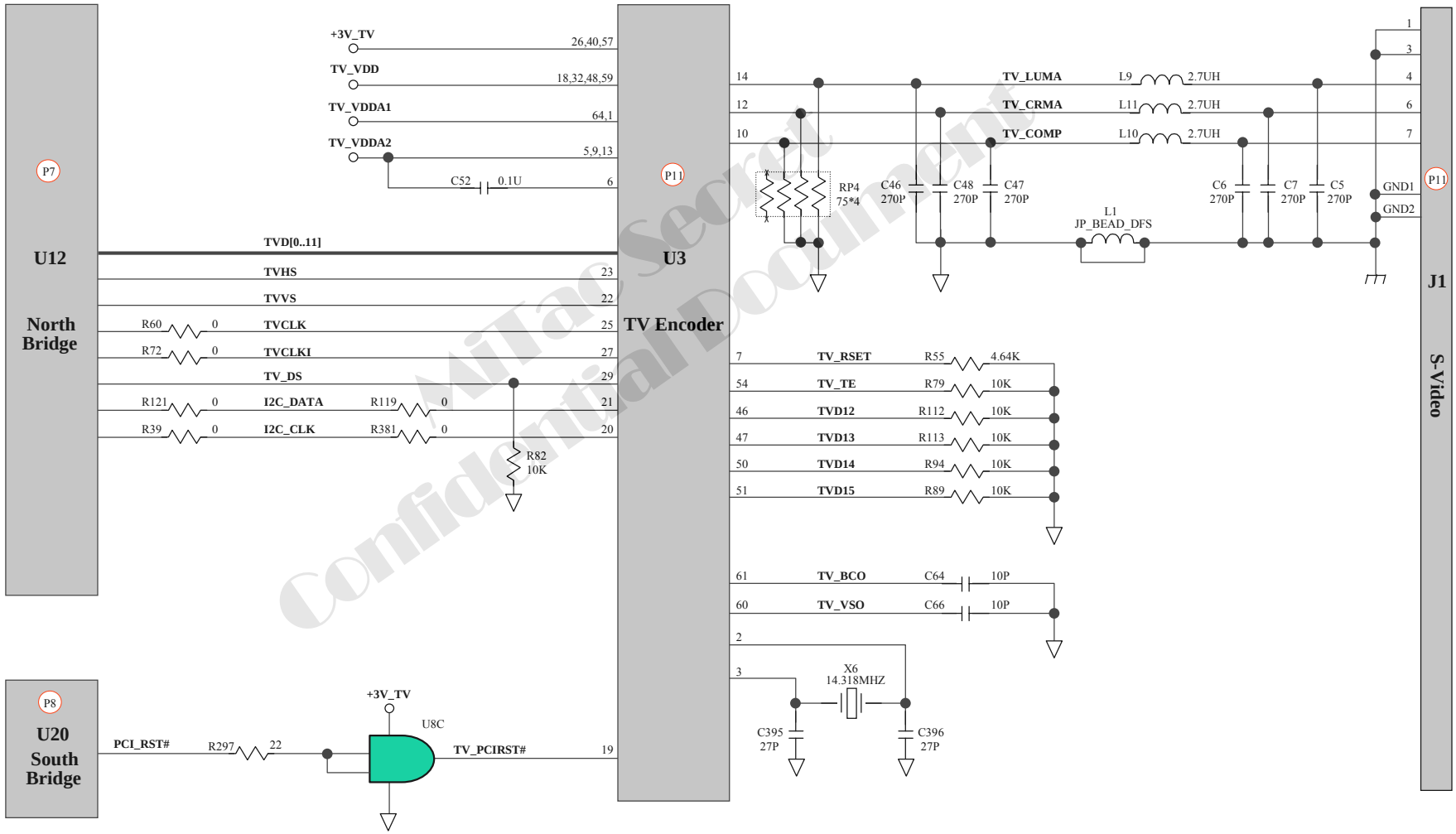
U3	R55
U12	R79
U20	R112
J1	R113
C52	R94
R119	R89
R381	RP4
X6	C46
C395	C47
C396	C48
R297	C64
U8	C66
L9	C5
L10	C6
L11	C7
L1	

Signals

TV_VDD	TV_DS
TV_VDDA1	I2C_DATA
TV_VDDA2	I2C_CLK
TV_LUMA	
TV_CRMA	
TV_COMP	
TV_PCIRST#	
TVD[0..15]	
TVHS	
TVVS	
TVCLK	
TVCLK1	

8.16 TV Encoder Test Error(2)

An error occurs when using the computer as TV.



9. Spare Part List(1)

Part Number	Description	Location(S)
221679920001	CARTON;NON-BRAND,8640C	
221679950001	PARTITION;IN CARTON,8640C	
221679950002	CARD BOARD;TOP/BTM,PALLET,8640C	
221679950003	CARD BOARD;FRAME,PALLET,8640C	
221679950004	PARTITION;PALLET,8640C	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222678500002	PE BUBBLE BAG;BATTERY,280*170,MS	
224670830002	PALLET;1250*1080*130,7521N	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
225682900001	CONDUCTIVE TAPE;DC,M/B,8599	
227675400003	EPE PAD;K/B,8355	
227682900001	END CAP;R,8599	
227682900002	END CAP;L,8599	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000433	LABEL;BLANK,11*5MM,COMMON	

Part Number	Description	Location(S)
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242669600005	LABEL;LOT NUMBER,RACE	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242684100001	LABEL;AGENCY-GLOBAL,8399	
242684100002	LABEL;BATT 11.1V/4AH,LI,PANA,839	
245600010007	FLOW CARD;M/B,WHITE	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R431
271002100301	RES;10 ,1/10W,5% ,0805,SMT	PR17,PR28
271002331301	RES;330 ,1/10W,5% ,0805,SMT	FR3,FR4,R14,R15
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR5,PR6
271035012711	RES;.012,1W,1%,2010,LR2010,IRC,S	PR73
271044060301	RES;.006 ,1.5W,5% ,2512,SMT	
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR1,PR85
271045127102	RES;.012,1W,1%,2512,SMT	PR74
271046068101	RES;.006 ,1.5W ,1% ,2512,SMT;PWR	RM4
271061000002	RES;0 ,1/16W,0402,SMT	R102,R105,R119,R121,R129,R134
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R120,R181,R184,R235,R24,R261,I
271061102105	RES;1K ,1/16W,1% ,0402,SMT	R12,R166,R217,R218
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R1,R194,R200,R213,R288,R296,R
271061103102	RES;10K ,1/16W,1% ,0402,SMT	R10,R11,R195,R212,R27,R28

9. Spare Part List(2)

Part Number	Description	Location(S)
271061103501	RES;10K ,1/16W,5% ,0402,SMT	R112,R113,R117,R13,R145,R146,I
271061104501	RES;100K ,1/16W,5% ,0402,SMT	R176,R177,R216,R219,R221,R222
271061105501	RES;1M ,1/16W,5% ,0402,SMT	R292
271061106501	RES;10M ,1/16W,5% ,0402,SMT	R345
271061121501	RES;120 ,1/16W,5% ,0402,SMT	R183,R186,R207,R208,R209,R210
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R87
271061203102	RES;20K ,1/16W,1% ,0402,SMT	R289
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R127,R128,R179,R182,R192,R193
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R68,R69
271061300131	RES;300 ,1/16W,5% ,0402,SMT	R91
271061302101	RES;3K ,1/16W,1% ,0402,SMT	R170,R448
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R241,R244,R265,R420,R423
271061331304	RES;330 ,1/16W,5% ,0402,SMT	R154,R172,R173,R225,R227,R228
271061361101	RES;360 ,1/16W,1% ,0402,SMT	R165,R315,R350,R445
271061401101	RES;402,1/16W,1%.0402,SMT	R450
271061464112	RES;4.64K ,1/16W,1% ,0402,SMT	R55
271061470501	RES;47 ,1/16W,5% ,0402,SMT	R259,R260
271061471501	RES;470 ,1/16W,5% ,0402,SMT	R229,R323
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R108,R109,R110,R111,R130,R137
271061473501	RES;47K ,1/16W,5% ,0402,SMT	R178,R214,R223,R382,R386
271061474501	RES;470K ,1/16W,5% ,0402,SMT	R123,R211,R32
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R101,R107,R61,R66,R77,R78
271061512102	RES;5.1K ,1/16W,1% ,0402,SMT	R67
271061562501	RES;5.6K ,1/16W,5% ,0402,SMT	R328,R356
271061564101	RES;560K ,1/16W,1% ,0402,SMT	R224,R26,R29,R353,R4,R9

Part Number	Description	Location(S)
271061604011	RES;60.4 ,1/16W,1% ,0402,SMT	R81,R90
271061619211	RES;6.19K,1/16W,1% ,0402,SMT	R287
271061649212	RES;6.49K,1/16W,1% ,0402,SMT	R70
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R131,R135,R138,R139,R148,R150
271061753101	RES;75,1/16W,1%,0402,SMT	R46,R47,R48,R49
271061821101	RES;820 ,1/16W,1% ,0402,SMT	R114,R118
271061822501	RES;8.2K ,1/16W,5% ,0402,SMT	R290,R411
271061900101	RES;90.9,1/16W,1%.0402,SMT	R14
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L36,L37,L57,PR10,PR12,PR13,PR
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R42,X38
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR108,PR109,PR18,PR31,PR34,P
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R13,R17,R18,R35,R36
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR37,PR52
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR16,PR62,PR90,PR95
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR22,R376,R433
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1,R37,R38
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R2,R3
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR103,PR3,PR57,PR72,PR75,PR9
271071104701	RES;100K ,1/16W,.1%,0603,SMT	PR86
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR2,PR49,PR56,R303
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R16,R39
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR21,PR69
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R156

9. Spare Part List(3)

Part Number	Description	Location(S)
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR98
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R14A
271071137271	RES;13.7K,1/16W,.1%,0603,SMT	PR101
271071143112	RES;14K,1/16W,1%,0603,SMT	PR15
271071151103	RES;15 ,1/16W,1% ,0603,SMT	R245,R247
271071169011	RES;169 ,1/16W,1% ,0603,SMT	R132
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR60
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR61,PR68,PR9,PR91
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR102
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR66,PR67
271071220101	RES;22 ,1/16W,1% ,0603,SMT	R168
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R41
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR82
271071228301	RES;2.2 ,1/16W,5% ,0603,SMT	PR48,PR65,PR70
271071243211	RES;24.3K,1/16W,1% ,0603,SMT	PR104
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR99
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR100
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R246,R248
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R366,R367,R372,R373,R374,R375
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071302101	RES;3K ,1/16W,1% ,0603,SMT	PR30,PR33
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R157,R169
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R2
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR76

Part Number	Description	Location(S)
271071348111	RES;3.48K,1/16W,1% ,0603,SMT	PR29
271071348812	RES;34.8 ,1/16W,1%,0603,SMT	R174,R180
271071402111	RES;4.02K,1/16W,1% ,0603,SMT	PR50
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071442113	RES;44.2 ,1/16W,1% ,0603,SMT	R100,R30
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR105,PR106
271071473101	RES;47K ,1/16W,1% ,0603,SMT	PR11
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR4
271071478301	RES;4.7 ,1/16W,5% ,0603,SMT	PR89
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR32,PR88
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR87
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R19,R25
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R421,R422
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR96
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR59
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
271071806812	RES;80.6 ,1/16W,1% ,0603,SMT	R151
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R256,R388
271071866111	RES;8.66K,1/16W,1% ,0603,SMT	PR51
271071887111	RES;8.87K,1/16W,1% ,0603,SMT	R133
271071909101	RES;9.09K,1/16W,1% ,0603,SMT	PR8
271072383011	RES;383 ,1/10W,1% ,0603,SMT	R319,R352
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4,R5,R9

9. Spare Part List(4)

Part Number	Description	Location(S)
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP59,RP61,RP62,RP63,RP68,RP7
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP19,RP21,RP22,RP24,RP25,RP2
271571470301	RP;47*8 ,16P ,1/16W,5% ,1606,SM	RP14,RP15,RP16,RP17,RP18
271571680302	RP; 68*8 ,16P,1/16W,5% ,1606,SM	RP31,RP33,RP34,RP36,RP37,RP3
271586026101	RES;.02 ,2W,1%,2512,SMT	PR107
271591000701	RP;0*4,8P,1/16W,.1%,0804,SMT	RP13,RP58,RP69
271591220301	RP;22*4,8P,1/16W,5%,0804,SMT	RP10,RP11,RP12,RP52,RP6,RP7,I
271591470301	RP;47*4,8P,1/16W,5%,0804,SMT	RP43
271591471301	RP;470*4,8P,1/16W,5%,0804,SMT	RP72,RP73
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP20,RP23,RP26,RP29
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP3
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP1,RP45,RP57
271611153301	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	RP46,RP49,RP50
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP44
271611680301	RP;68*4 ,8P ,1/16W,5% ,0612,SMT	RP32,RP35,RP38,RP41
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP2,RP4
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP47,RP53,RP56,RP60,RP66,RP6
271621222301	RP;2.2K*8,10P,1/16W,5% ,1206,SMT	RP55
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP48,RP51,RP54,RP64,RP65,RP7
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC145,PC147,PC44
272001106702	CAP;10U,6.3V,+- 20%,0805,X5R,SMT	C115,C125,C126,C127,C128,C132
272001106703	CAP;10U,10V,+80-20%,0805,Y5V,SMT	C100,C105,C12,C120,C158,C164,(
272001475403	CAP;4.7U,10V,10%,0805,X5R,SMT	C122,C140,C202,C204,C243,C260
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C342,C351,C421,C96
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PC135,PC23,PC33

Part Number	Description	Location(S)
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C420
272005104401	CAP;.1U ,CR,50V,10%,0805,X7R,IN	PC19,PC34
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC111,PC80,PC93
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V	C17,C18
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,	PC10,PC110,PC13,PC3,PC6,PC68
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	PC103,PC70
272011475401	CAP;4.7U ,10%,10V ,1206,X7R,SMT	C41
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,S	C14A,C14B
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	PC48
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,S	PC97
272023106002	CAP;10U,25V,M,1210,T2.8MM,X5R,SM	PC131,PC137,PC142
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC11
272023106502	CAP;10U,25V,M,1210,T2.5MM,X5R,SM	PC24,PC30,PC43,PC49,PC5,PC51
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272030102301	CAP;100P,3KV,5%,1808,NPO,SMT,PWR	C20
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C2,C3,C666,C667,C74
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C10,C4
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C311,C375
272071225401	CAP;2.2U ,CR,6.3V ,10%,0603,X5R,	C282,C336
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C12,C17,C6
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C339,PC138
272072104702	CAP;.1U ,16V,+80-20%,0603,Y5V,S	PC20,PC22,PC28,PC31,PC47,PC6
272072224402	CAP;.22U ,16V ,10%,0603,X7R,SMT	C108,C131,C136,C15,C156,C16,C
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C116,C117,C402,C403,C404,C405

9. Spare Part List(5)

Part Number	Description	Location(S)
272072473402	CAP;.047U,16V ,10%,0603,X7R,SMT	C266
272072683404	CAP;.068U ,16V ,10%,0603,X7R,SMT	C16
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C355,C356
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C9
272073392401	CAP;3900P,50V,10%,0603,X7R,SMT	C103,C107
272073472301	CAP;4700P,CR,50V ,5% ,0603,X7R,S	C15A
272075102402	CAP;1000P,CR,50V,10%,0603,X7R,IN	PC105,PC109,PC75,PC92
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC1,PC123,PC127,PC132,PC139,
272075102501	CAP;1000P,CR,50V ,20%,0603,X7R,S	PC108
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	PC21,PC36,PC84
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C11,C13,C3,C8
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC102,PC116,PC117,PC128,PC14
272075103403	CAP;.01U ,50V,10%,0603,X7R,SMT	PC90
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R S	C15,C16,C35,C37,C39
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	PC119,PC124,PC134,PC136,PC14
272075103706	CAP; 0.1U CR 50V +80-20% 0603 Y	C28,C30,C31,C32,C33,C34
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C344,C425,PC107,PC113,PC118,P
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC104,PC98
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C85,C87
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C5
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C133,C134
272075223702	CAP; 0.22U CR 50V +80-20% 0603	C29,C40,C41
272075330401	CAP;33P ,CR,50V ,10%,0603,X7R,S	PC32
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	PC100,PC101
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C36

Part Number	Description	Location(S)
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7	C19
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,S	PC37
272075822401	CAP;8200P,CR,50V,10%,X7R,0603,SM	PC106
272102100401	CAP;10P ,50V ,+-10%,0402,NPO,SM	C321,C64,C66
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SM	C102,C104,C106,C124,C13,C130,
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y	C110,C111,C118,C121,C135,C141
272102224701	CAP;.22U ,10V ,+80-20%,0402,Y5V,	C137,C225,C264,C278
272102334701	CAP;.33U ,CR,10V ,+80-20%,0402,Y	C139
272105059401	CAP;5P ,50V,+-10%,0402,SMT	C283
272105101401	CAP;100P ,50V ,5%,0402,COG,SMT	C1,C223,C224
272105101402	CAP;100P ,50V ,+ -10%,0402,NPO,S	C114,C129,C206,C261
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SM	C10,C138,C180,C22,C250,C37,C3
272105102501	CAP;1000P,50V ,+/-20%,0402,X7R,S	C123
272105103402	CAP;.01U ,CR,25V ,10%,0402,X7R,S	C150,C152
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C112,C119,C154,C175,C179,C25,
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C101,C109,C113,C155,C169,C173
272105220402	CAP;22P ,50V ,+ -10%,0402,NPO,S	C242,C249,C252,C255,C257,C259
272105221403	CAP;220P ,CR,50V ,10%,0402,X7R,S	C406
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,S	C99
272105270303	CAP;27P ,50V ,5%,0402,COG,SMT	C241,C246,C395,C396
272105271403	CAP;270P ,50V,+-10%,0402,X7R,SMT	C162,C172,C174,C201,C357,C378
272105332402	CAP;3300P,50V,10%,0402,SMT	C80
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PC35,PC64
272431227503	CAP;150U ,POLY,6.3V,20%,7243,SMT	PC7,PC77,PC9
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C227,C235,C236

9. Spare Part List(6)

Part Number	Description	Location(S)
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP1,CP2
272990100301	CAP;10P,3000V,+- 5%,NPO,SMT	C19
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L52
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L100,L101,L43,L48,L50,L501,L5
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L10,L11,L12,L13,L14,L15,L16,L1
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L38,L39,L40,L49,L57,R124
273000130062	INDUCTOR;120nH,10%,0603,SMT	L31
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L2,L24,L27,L29,L3,L30,L32,L33,
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L58,PL1,PL10,PL11,PL12,PL14,P
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L20,L21,L22,L23,L26,L28,L97,L9
273000500092	CHOKE COIL;2.2UH ,20%,16A,3.5MM	PL7
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;	L105,L19
273000990018	INDUCTOR;10uH,CDRH125,SUMIDA,SMT	PL13,PL15
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	PL20
273000990127	INDUCTOR;IHLP5050CE-01-0.68uH,VI	PL3,PL4
273000990186	INDUCTOR;3.0UH,30%,CDRH6D28,H2.8	PL18
273001050028	XSFORMER;10/100 BASE,LF-H41S,SMT	U4
273001050127	XFMR;CI8.5,30T/2150T,300mH,SMT,o	T1
274011431414	XTAL;14.318MHZ,32PF,50PPM,8*4.5,	X3,X6
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X5
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,	U1
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U11
282607408001	IC;74HCT08PW,2-INPUT AND GATE,TS	U22,U8
282607408002	IC;SN74HCT08PW,2-INPUT AND GATE,	
282674112601	IC;74HCT1G126GW,NON-INVERTING BU	U39,U40

Part Number	Description	Location(S)
282674112602	IC;SN74AHCT1G126DCK,NON-INVERTIN	
282674244004	IC;74HCT244D,OCT TRI-ST BUF,SOIC	U23,U24
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	IC6
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	U15
283480404001	IC;FLASH,256K*8-70,PLCC32,A29002	
284500781001	IC;G781,TEMPERATURE MTR,SO8	U5
284501617005	IC;VT1617A,AUDIO CODEC,TQFP,48P	U10
284501622003	IC;VT1622AM,TV ENCODER,PQFP,64P,	U3
284506103009	IC;VT6103L,LAN-PHY,LQFP,48P,SMT	U2
284508235007	IC;VT8235,0340CD,SOUTH BRIDGE,BG	U20
284508800006	IC;VIA K8N800CE,N.B.,BGA578,SMT	U12
284516310001	IC;VT1631,LVDS TRANSMITTER,TQFP,	U9
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,8	
284595040301	IC;ICS950403,TIMING CTL HUB FOR	U14
286101428001	IC;G1428,AMPLIFIER,TSSOP,24P,SMT	U13
286104073001	IC;MAX4073F,I-SENSE AMP,SOT23,6P	PU9
286300338001	IC;SC338,FET CTRL,SC,MSOP-10	PU3
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU19
286301410002	IC;CB1410Q_B0,PCI/CARDBUS,LQFP,1	U26
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	IC7
286301470001	IC;SC1470,PWM CTRL,TSSOP,14P,SMT	PU11
286302211006	IC;CP2211,POWER DISTRI SW,REV.C1	U27
286302996001	IC;G2996,DDR,GMT,SOP8FD,SMT	PU13
286303107001	IC;AMS3107C,3.3V,1%,VOL REGULATO	U19
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU14

9. Spare Part List(7)

Part Number	Description	Location(S)
286304377001	IC; MAX4377F,I-SENSEAMP ,MSOP8,S	PU20
286306207001	IC;ISL6207CB,PWM DRIVER,SO8,SMT	PU5,PU7
286306559002	IC;ISL6559,MULTI-PHASE PWM CTL,S	PU6
286308800007	IC;AME8800DEFT,VOL REG.,SOT89,3P	U17
286308804002	IC;AME8804AEEY,ADJ,0.3A,LDO,SOT2	U7
286329513001	IC;AMS2951CS-3.3,3.3V,150MA VLOT	U28
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V	U38
286387506001	IC;S-875061EUP VOLT DETECTOR S	IC5
288100014010	DIODE;SS14,40V,1A,SMA,VISHAY	PD11
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D12,PD16
288100034004	DIODE;SSA34,40V,3A,SMA	PD14,PD17,PD7,PD8
288100054002	DIODE;BAT54C,SCHOTTKY DIODE,SOT2	D17
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D1
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD3,ZD4
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,	PD12
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D14,PD5,PD6
288101040006	DIODE;SBM1040,10A,SCHOTTKY,POWER	PD3
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D11
288105524003	DIODE;BZV55-C24,ZENER,5%,SOD-80,	PD2
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SM	D3
288111544001	DIODE; 1SR-154-400 400V 1.0A	D4
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q8
288200144008	TRANS;DTA144EKA,PNP,SMT	Q8
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q20
288200416001	TRANS;AOB416,30V/110A,.0065OHM,N	PQ2,PQ5

Part Number	Description	Location(S)
288200420001	TRANS;AOB420,30V/110A,.010OHM,N-	PQ4,PQ7
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323	SD2
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ21
288202237002	TRANS;MUN2237T1,NPN,SOT-23,SMT,O	PQ17,Q26,Q31
288202240001	TRANS;MUN2240T1,NPN,SOT-23,ON	Q1,Q10,Q13,Q16,Q17,Q22,Q23,Q
288203400001	TRANS;AO3400,N-MOSFET,SOT-23	Q2
288203403001	TRANS;AO3403,P-MOSFET,SOT-23,ALP	Q11,Q9
288203413001	TRANS;AO3413,P-MOSFET,SOT-23	Q15,Q36
288204403008	TRANS;AO4403,P-MOSFET,46mOHM (VG	U21,U35
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SM	PQ15,PQ23,PU1
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,	Q10,Q14
288204410010	TRANS;AO4410,N-MOSFET,ID=18A,0.0	PU10
288204422001	TRANS;AO4422,24mOHM,N-MOSFET,SOI	PU12,PU17,PU2,PU4,U18
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU16
288204912001	TRANS;AO4912,24mOHM ,SMT	PU15
288221371002	TRANS;MUN2137T1,PNP,SMT,ON	PQ24
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	Q18,Q19,Q21,Q29,Q35,Q37,Q5,Q
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ1,PQ10,PQ11,PQ12,PQ13,PQ1
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000000708	CON;BATTERY,7P,FM,2.5MM,BTG-07AR	CON1
291000013016	CON;HDR,MA,15P*2,1MM,H4.25,ST,SM	J8
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	
291000020222	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J11,J20,J6
291000020415	CON;HDR,MA,4P*1,1.25MM,ST,SMT,38	J13,J7
291000143011	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J15

9. Spare Part List(8)

Part Number	Description	Location(S)
291000150606	CON;FPC/FFC,6P,0.5MM,R/A,SMT	J18
291000152614	CON;FPC/FFC,26P,1MM,H=2.0,R/A,SM	J501
291000611255	MINIPCI SOCKET;124P,0.8MM,H=9.2,	J22
291000616807	CON;PCMCIA CARD,68P,929100000140	J502
291000617542	IC SOCKET;AMD K8 BGA-PGA754-SKT,	U6
291000622010	DIMM SOCKET; DDR,200P,REVERSE TY	J16
291000622011	DIMM SOCKET; DDR,200P,H=9.2mm,SM	J17
291000810818	CON;PHONE JACK,12P,R/A,RJ45,RJ11	J5
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D501,D502,D503,D504,D505,D50
294011200200	LED;GREEN/RED,H0.8,W1.9,19-22SRV	D510
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F2,F3,F4
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMI	PF2
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF3
295000010154	FUSE;FAST,1.25A,63V,1206,SMT,043	F1
295000100004	FUSE;FAST,1A,63V,1206,THIN FILM	F5
297030100015	SW;TOGGLE,SPST,5V/1mA,4P,SMT,TAI	SW506
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW1,SW501,SW502,SW503,SW50
310111103013	THERMISTOR;10K,1%,RA,DISK,103AT-	RT2
310111103025	THERMISTOR;10K,1%,RA,DISK,103AT-	
310111103031	THERMISTOR;10K,1%,150MM,BN35-3H1	
312272263511	EC;22U,25V,20%,RA,8*10.5,105℃,O	PC112,PC115,PC27,PC52,PC54,P
312273361501	EC;330U ,6.3V ,RA,M,6.3*7,+105C	C32,C33,C384
312276806151	EC;680U ,6.3V,20%,D10,105'C,OS-C	PC114
312278206151	EC;820U ,4V,+-20%,100*10.5,SP.OS	PC82,PC94

Part Number	Description	Location(S)
312278206161	EC;820U ,2.5V,+-20%,8X12.5,OS-CO	PC25,PC29,PC53,PC58
314100250502	XTAL;25MHZ,30PPM,20PF,49S,11.5*3	X1
314149800402	XTAL;8MHZ,30PPM,HC-49/S,6B080002	X4
316678100001	PCB;PWA-INVERTER BD (DA-1A10-A);	R0C
316684100001	PCB;PWA-8399-M BD	R02
316684500001	PCB;PWA-Tarzan/BATT ,PR AND GA	
323768410001	DDR SODIMM MODULE;256MB,PC3200,7	
324180786803	IC;CPU,AMD-Athlon 64 3200+,OPGA,	
331000000303	CON HOLDER;PCMCIA,331000000071,A	
331000007038	CON;BAT,7P,2.5mm,OCT,tBTD-007001	PJ2
331000008091	CON;USB,MA,ST,4P*2,SMT,1-1470748	J3,J4,J9
331000050004	CON;CD-ROM,50P,0.8MM,H-10.4,R/A,	J21
331030044021	CON;HDR,FM,22P*2,2.0MM,SMT,C1783	J14
331678100001	CONNECTOR;7 PIN,1.25mm,SMT,ACES,	J1
331720015071	CON;D,FM,15P,2.29,R/A,SUYIN	J2
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J10
331840005014	CON;STEREO JACK,5P,R/A,28MF60-05	J12
331870007010	CON;MINI DIN,7P,R/A,W/GROUND,030	J1
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	PJ1
332110020097	WIRE;#20,UL1007,74MM,BLACK,YIYI;	CN6
332110020175	WIRE;#20,UL1007,L=103MM,RED, PWR	CN10
332110020176	WIRE;#20,UL1007,70.5MM,BLACK,YIY	VL-VL
332110026097	WIRE;#26,UL1007,55MM,BLACK,PRC	CN8
332110026155	WIRE;26#,UL1061,L=115MM,YELLOW,	CN9
332810000212	PWR CORD;125V/7A,2P,BLACK, AMERI	

9. Spare Part List(9)

Part Number	Description	Location(S)
333020000008	SHRINK TUBE;600V,125℃,Φ2.5mm,L	
333025000004	SHRINK TUBE;300V,125,I.D=2.5,T=0	
333050000120	SHRINK TUBE;600V,105'C,D0.8*9MM,	
335152000044	CFM-BAT;FUSE THERMAL 98'C	
335152000085	FUSE; 128 DC-7A/50V 139℃only UC	F2
335152000094	FUSE;LR4-900,POLY SWITCH	
335152000100	FUSE; THERMAL,SF91E-1/94℃,10A/2	
338536010006	BATTERY;LI,3.6V/2.0AH,18650,PANA	
339115000046	MICROPHONE;-62dB+-2dB,D6.0*H2.7,	MIC501
340682900001	HOUSING ASSY;LCD,8599	
340682900002	COVER ASSY;LCD,8599	
340682900003	HINGE;R,8599	
340682900004	HINGE;L,8599	
340682900005	HINGE;R,SZS,8599	
340682900006	HINGE;L,SZS,8599	
340682900009	BRACKET ASSY;TOUCH-PAD,8599	
340682900010	SPEAKER ASSY; 28*4.3,2W,FENG-CHI	
340682900011	SPEAKER ASSY; 28*4.3,2W,VECO,859	
340682900015	HOUSING ASSY;BOTTOM,8599	
340682900017	COVER ASSY;CPU,8599	
340682900018	COVER ASSY;MINIPCI,8599	
340682900021	SHIELDING ASSY;HDD,8599	
340682900022	DVD+RW BEZEL ASSY;SDW-041,8599	
340684100001	COVER ASSY;TOP,8399	
340684100003	SHIELDING ASSY;BOTTOM,8399	

Part Number	Description	Location(S)
340684100004	HEATSINK ASSY;CPU,K8 HAMMER,MPT,	
340684100005	HEATSINK ASSY;CPU,K8 HAMMER,AVC,	
340684100006	HAETSINK ASSY;SYSTEM,M/B,MPT,839	
340684100007	HAETSINK ASSY;SYSTEM,M/B,AVC,839	
341675300008	STANDOFF;CPU,8080	MTG501,MTG502
341682900003	BRACKET;LCD,R,8599	
341682900004	BRACKET;LCD,L,8599	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342503200003	CONTACT PLATE;W4L18T0.15,7521/GR	
342503400005	CONTACT PLATE;W5L24T0.13,7170LI,	
342503400005	CONTACT PLATE;W5L24T0.13,7170LI,	
342673100024	CONTACT PLATE;W5L62T0.13 ,1/3T,8	
342682900009	BRACKET;ROM,8599	
342682900010	CONTACT PLATE;W5L28T0.15MM,BATTE	
344503100304	DUMMY;D18L65,BATT ASSY,7521C	
344672300025	DUMMY CARD;PCMCIA,MANGUSTA	
344682900012	COVER;HINGE,8599	
344682900016	COVER;BATTERY,8599	
344682900017	HOUSING;BATTERY,8599	
345668900016	SPONGE;BIOS BATT,M722	
345675400023	RUBBER;DOWN LCD,8355	
345682900005	SPONGE;DUAL DDR,M/B,8599	
345682900006	SPONGE;SPSPEND SWITCH,M/B,8599	
345682900009	SPONGE;HINGE COVER,8599	
346502800004	INSULATOR;BATT ASSY,BATT+,BATT-,	

9. Spare Part List(10)

Part Number	Description	Location(S)
346503100001	INSULATOR;BATT ASSY,THERMAL FUSE	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346673420003	MYLAR;15*10*0.8,8640P	
346677300001	INSULATOR;FIBER,UL94V-0,D=17.5mm	
346678600005	INSULATOR;FIBER,UL94V-0,64X15,T=	
346682900007	NYLON;BATTERY PULL,8599	
346682900009	AL-FOIL;T/P BRACKET,8599	
346682900010	AL-FOIL;T/P SWITCH,MB,8599	
346682900013	SPONGE;M/B,8599	
346682900014	INSULATOR;AL-FOIL,INVERTER,8599	
346684100002	INSULATOR;CARD BUS,8399	
346684100003	INSULATOR;SOUTH BRIDGE,8399	
346684100004	TUBE;M/B,FOR ANTENNA,8399	
346684400002	INSULATOR;RIBRE,63*15*0.25MM,BAT	
347104030012	GASKET;1,04,030,012	
347104030030	GASKET;1,04,030,030	
347104045125	GASKET;1,04,045,125	
347105020090	GASKET;1,05,020,090	
347105060030	GASKET;1,05,060,030	
347105060060	GASKET;1,05,060,060	
347108010012	GASKET;1,08,010,012	
347108080090	GASKET;1,08,080,090	
347108150024	GASKET;1,08,150,024	

Part Number	Description	Location(S)
347110020025	GASKET;1,10,020,025	
347110035035	GASKET;1,10,035,035	
347110040012	GASKET;1,10,040,012	
347110080025	GASKET;1,10,080,025	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102611001	SPC-SCREW;M2.6L10,NIB,K-HD,NY	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010414	SPC-SCREW;M3L4,KHD,NIW/NLK,D5.3,	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	
371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,N	
371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,N	
371102010610	SCREW;M2L6,K-HD(+),t0.75,NIB	
371102610308	SCREW;M2.6L3,D3.5,t=0.5,K-HD,NIW	
371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	
371102610607	SCREW;M2.6L6,K-HEAD(+),NIB	
373101712351	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
377102650901	S-STANDOFF;M2.6DP3.5H9L1.1,NIW	MTG3,MTG4
377102651002	S-STANDOFF;M2.6DP5H12.5L4,NIW,NY	

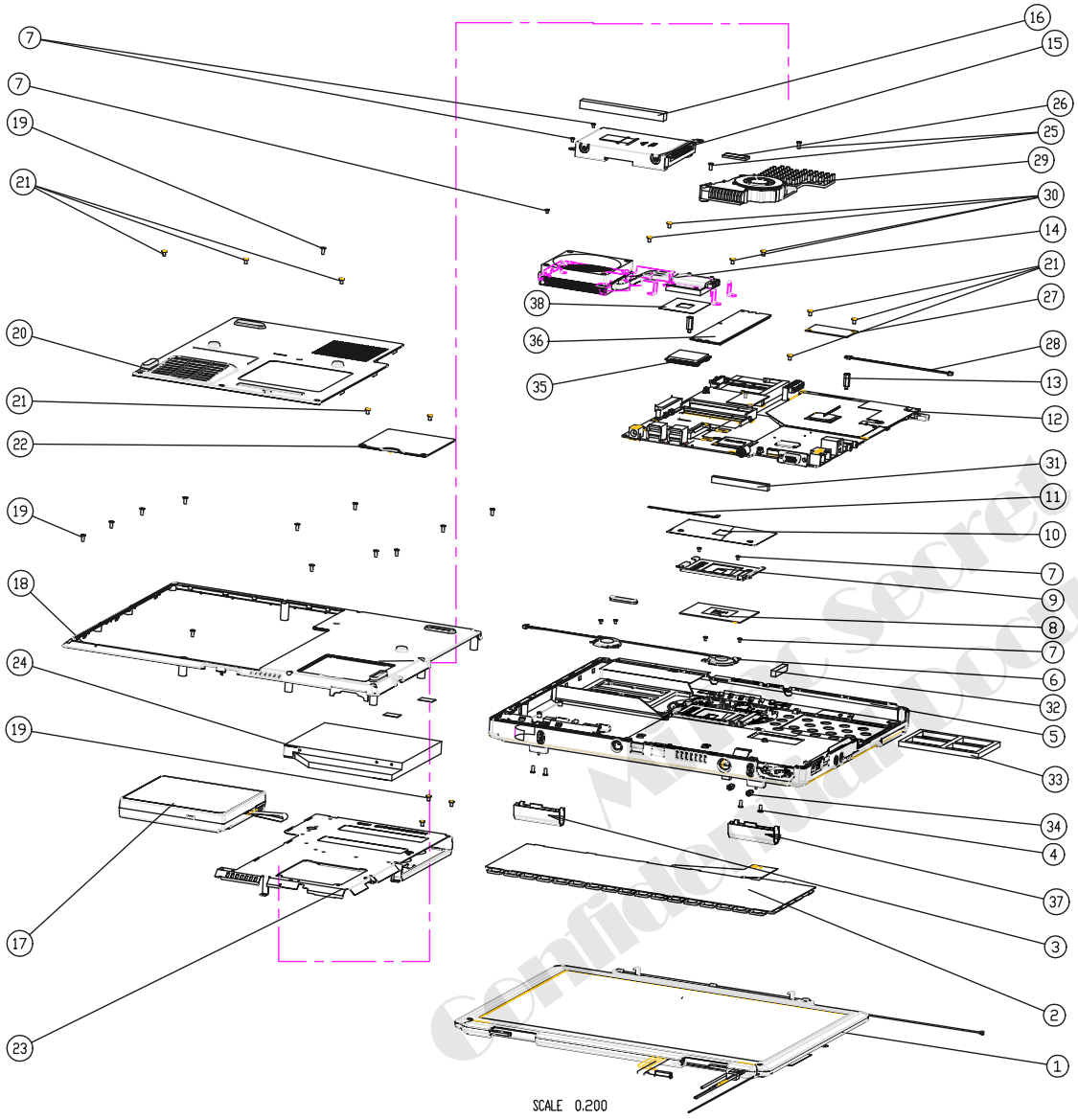
9. Spare Part List(11)

Part Number	Description	Location(S)
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
411678100001	PWA;PWA-INVERTER BD,DA-1A10-A,PW	
411678100002	PWA;PWA-INVERTER BD,SMT,DA-1A10-	
411684110001	PWA;PWA-8399-MAX,MOTHER BD	
411684110002	PWA;PWA-8399-MAX,MOTHER BD,T/U	
411684110003	PWA;PWA-8399-MAX,MOTHER BD,SMT	
411684430001	PWA;PWA-BATT,PCB BD,LI,4.0Ah,BL4	
411684430002	PWA;PWA-BATT,PCB BD,SMT,4.0Ah,BL	
412681400001	PCB ASSY;WIRELESS LAN CARD,MINI	
412684100001	CFM-Medion; PCB ASSY;FAX MODEM 5	
412684110001	FAX MODEM KIT;Creatix,8399-MAX I	
413000020433	LCD;LTN150XB- L03,15",XGA,SAMSUN	
416268411001	LT PF;15",XGA,SAMSUNG,8399-MAX I	
421675400012	WIRE ASSY;BIOS,BATTERY,8355	
421682900001	WIRE ASSY;LTN150XB-L03,8599	
421682900011	WIRE ASSY;LTN150XB-L03,GREATLAND	
421684100003	WIRE ASSY,MDC-MODEM,4-4PIN,8399	
421684100005	WIRE ASSY;ANTENNA,WHA-YU,8399	
421684110001	ANTENNA OPTION;8399 ID1	
422682900001	FFC ASSY;TOUCH-PAD,TENN-RICH,859	
422682900002	FFC ASSY;TOUCH-PAD,HONG-FU,8599	
422682900003	FFC ASSY;TOUCH-PAD,CEI,8599	
431684110001	CASE KIT;Creaxtix,8399-MAX	
441684110001	LCD ASSY;15",XGA,SAMSUNG,8399 ID	
441684400003	BATT ASSY;11.1V,4.0Ah,LI,BL-424	

Part Number	Description	Location(S)
441684400006	CONTACT PLATE ASSY;PTC,S-TUBE,BL	
441684400010	CONTACT PLATE ASSY;W5L45T0.13,FU	
441684430003	BATT ASSY;11.1V,4.0Ah,LI,CASE CL	
441684430004	BATT ASSY;11.1V,4.0Ah,LI,CORE PA	
442678800002	CFM Medion AC ADPT ASSY;19V,4.74	
442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PU	
451682900001	HDD ME KIT;8599	
451682900002	LCD ME KIT;15",XGA,SAMSUNG,8599	
451682900005	ROM ME KIT;8599	
451684110002	HOUSING KIT;8399 ID1	
451684110004	LABEL KIT;N-B,8399	
461677400001	PACKING KIT;DA-1A05-A;PWR	
461682900002	PACKING KIT;COMPACT,N-B,8599	
481684100002	F/W ASSY;KBD CTRL,8399	U16
481684110001	F/W ASSY;SYS/VGA BIOS,8399-MAX	U25
523405320072	HDD DRIVE,40GB,2.5",IC25N040ATMR	
523430061910	DVD+RW DRIVE;SDW-041,QSI	
523468290001	DVD+RW ASSY;SDW-041,8599	
523468290004	HDD ASSY;Hitachi,IC25N040ATMR04,	
526268411004	LTXNX;8399/5SHE/40N/1UIX/B2X2A/X	
531020237940	KBD;88,UI,K011818G1,8599	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	

9. Spare Part List(12)

Part Number	Description	Location(S)
624200010140	LABEL;5*20,BLANK,COMMON	
		P/N:526268411004



ITEM	PART NO	PART NAME	Q'TY	TYPE	MARK
38	340684100012	INSULATOR KIT;CPU,8399	1	part	
37	340684100015	COVER ASSY;HINGE R,8399	1	part	
36	323768410003	DDR SODIMM MODULE ;256MB,PC3200,MICRON	1	part	OPTION
35	324180786803	IC;CPU,AMD-Athlon 64 3200+,ΩPGA,62W,754	1	part	OPTION
34	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	2	part	
33	344672300025	DUMMY CARD;PCMCIA,MANGUSTA	1	part	
32	347105060040	GASKET;1,05,060,040	1	part	
31	347105060060	GASKET;1,05,060,060	1	part	
30	370103010414	SPC-SCREW;M3L4,KHD,NIW/NLK,D5.3,t0.8	4	part	
29	340684100006	HAETSINK ASSY;SYSTEM,M/B,MPT,8399	1	asm	OPTION
28	421684100001	WIRE ASSY,MDC-MODEM,4-2PIN,8399	1	asm	
27	412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-I,MANGUST	1	asm	
26	347110020025	GASKET;1,10,020,025	1	part	
25	370102611001	SPC-SCREW;M2.6L10,NIB,NY	2	part	
24	523468411008	DVD COMBO ASSY;KME UJDA760,8399 ID1	1	asm	OPTION
23	340684100003	SHIELDING ASSY;BOTTOM,8399	1	asm	
22	340682900018	COVER ASSY;MINIPCI,8599	1	asm	
21	371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	8	part	
20	340684100016	COVER ASSY;CPU,8399	1	asm	
19	371102610607	SCREW;M2.6L6,K-HEAD(+),NIB	16	part	
18	340682900015	HOUSING ASSY;BOTTOM,8599	1	asm	
17	441684400012	BATT ASS'Y;11.1V,4.0Ah,LI,BL-4240G0116/	1	asm	OPTION
16	347108080090	GASKET;1,08,080,090	1	part	
15	523468411006	HDD ASSY;40G,FUJITSU,MHS2040AT,8399	1	asm	OPTION
14	340684100005	HEATSINK ASSY;CPU,K8,AVC,8399	1	asm	OPTION
13	377102651002	S-STANDOFF;M2.6DP5H12.5L4,NIW,NYLOK	2	part	
12	411684100001	PWA;PWA-8399,MOTHER BD	1	asm	
11	422682900001	FFC ASSY;TOUCH-PAD,TENN-RICH,8599	1	asm	OPTION
10	346682900009	AL-FOIL;T/P BRACKET,8599	1	part	
9	340682900009	BRACKET ASSY;TOUCH-PAD,8599	1	asm	
8	442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PUM1950	1	part	
7	371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,NIW	9	part	
6	340682900010	SPEAKER ASSY; 28*4.3,2W,FENG-CHIUN,8599	1	asm	OPTION
5	340684100001	COVER ASSY;TOP,8399	1	asm	
4	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	4	part	
3	344682900012	COVER;HINGE,8599	1	part	
2	531020237940	KBD;88,UI,K080818G1,8599	1	part	OPTION
1	441684110002	LCD ASSY;15",XGA,HYDIS,8399	1	asm	OPTION

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /
					/ /

RANGE \ TOL±	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	31-May-04	MATERIAL	SEE NOTES	TREATMENT	REMARK
UNIT	MM	SCALE	0.2	DRAWING NAME	LTXXNON;8399ID1/T5M3/0C04D/1XUIA/1X
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 526268412002 R00A

MiTAC Technology Corp.

model name8399_MAIN_ASSY

file nameDRW_8399_MAIN_ASSY

MODEL : 8399 Revision 03

REVISION	TAPEOUT DAY	HISTORY
R00	2003/01/03	DESIGN FOR EVT
R02		1.Add AMS2951 for KBC_VREF to solve battery not accuracy issue.
R03	2004/05/20	1.Connect CPU AF_18 to VDDIO ba se on Errata 108. 2.Change LDTSTOP pull high resistor location. 3.Add level shift circuit for ENPBLT from K8N800. 4.Add R436 pull high resistor for VT8235CD hardwar e strap pin SPKR. 5.Change R287 from 6.19K to 5.6K for USB2.0 eye pattern fail issue . 6.Remove AMS2951 but add a MOSFET between AMS3107 and +SVDD3 for cost issue.

Contexts

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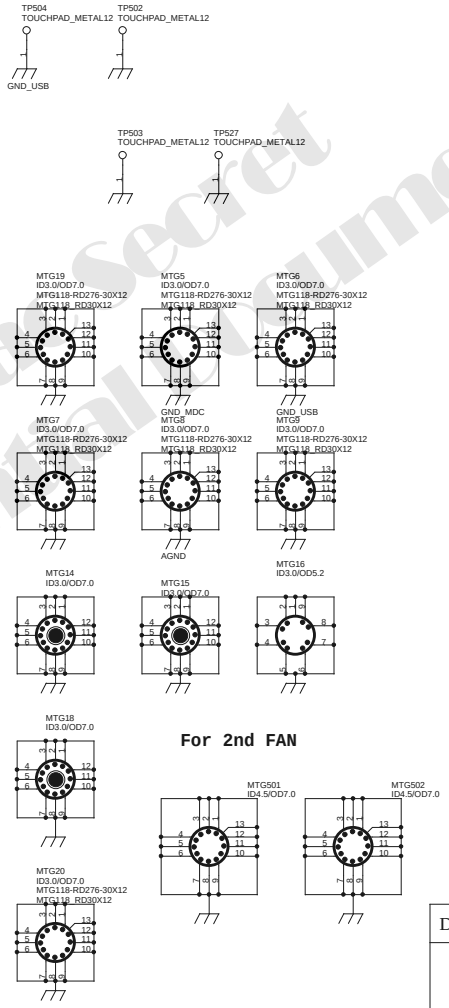

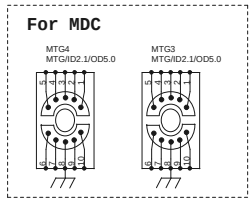

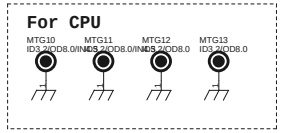

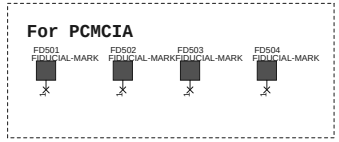

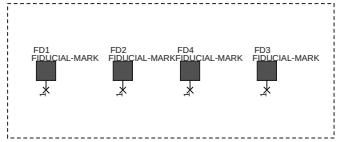

DRAWN	DESIGN	CHECK	ISSUES

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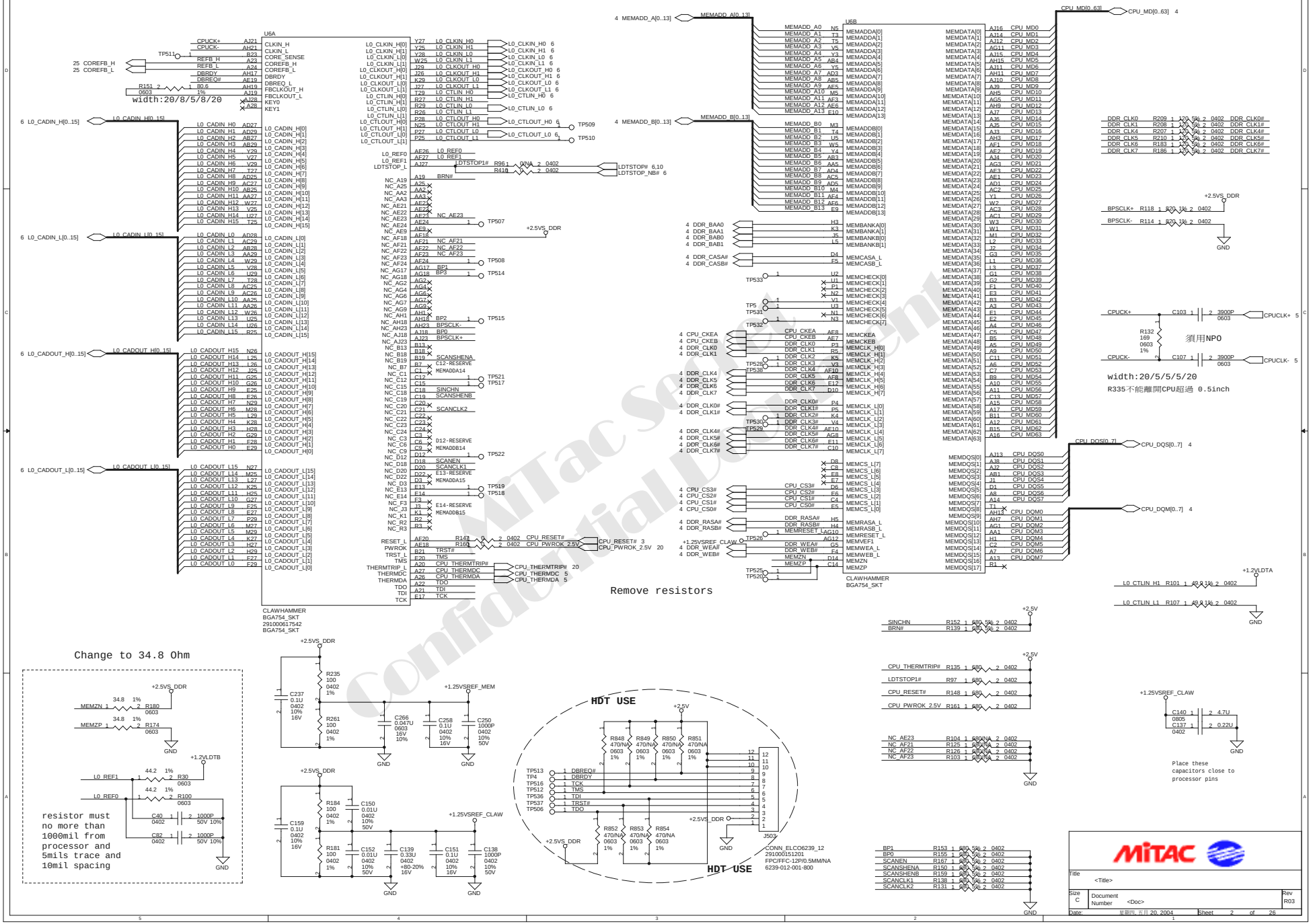
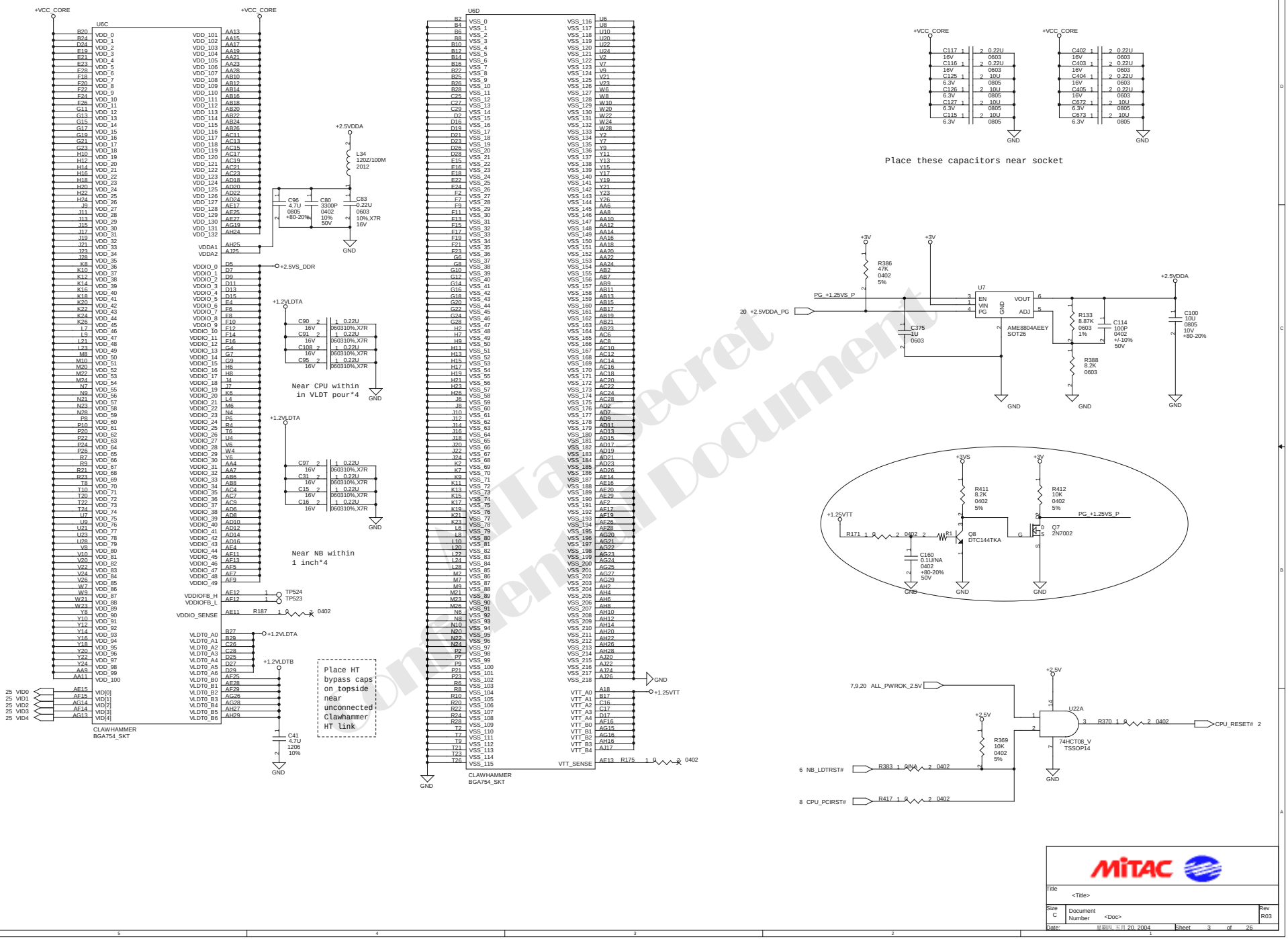
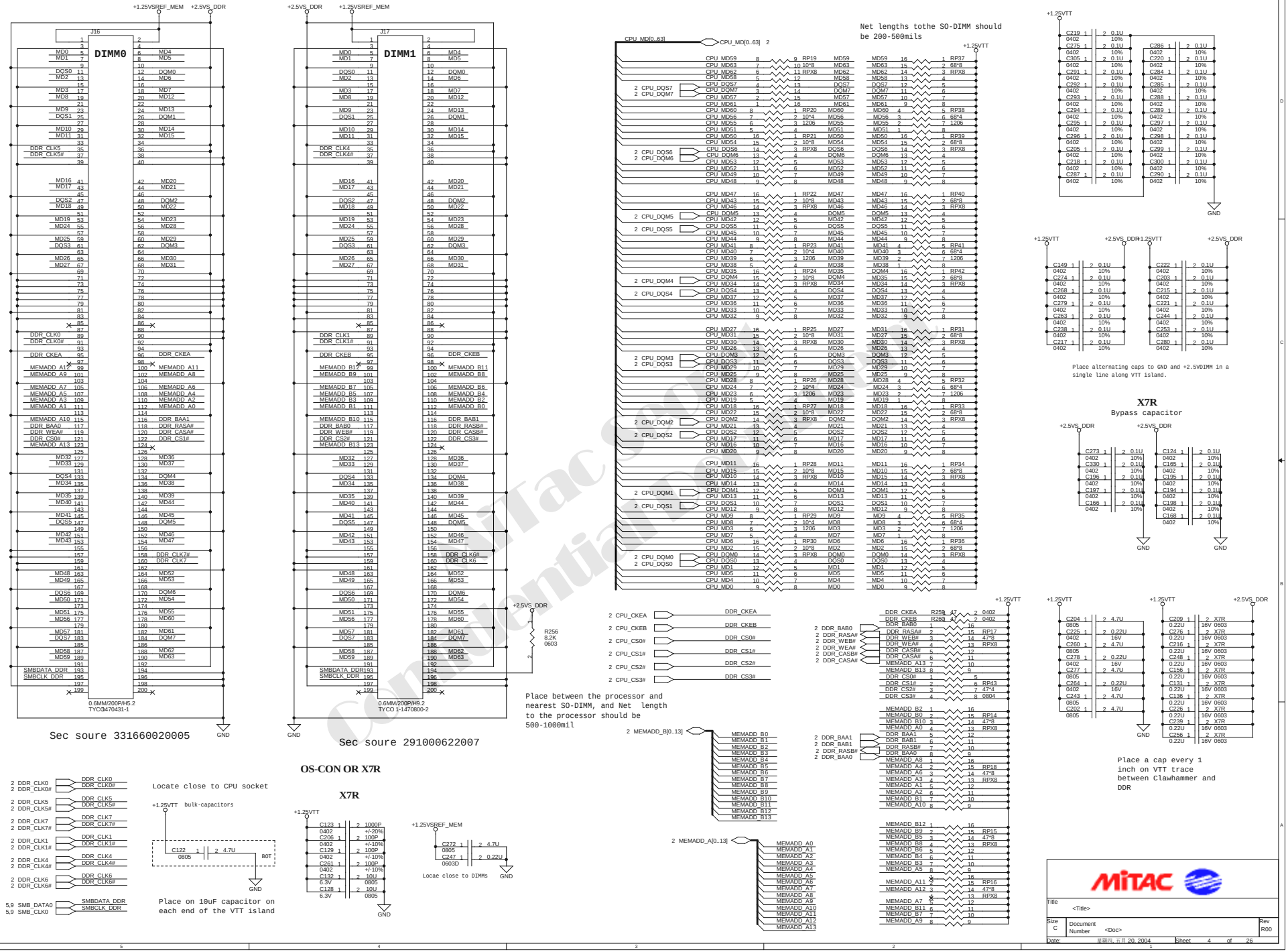
ClawHammer-HT&DDR(1/2)



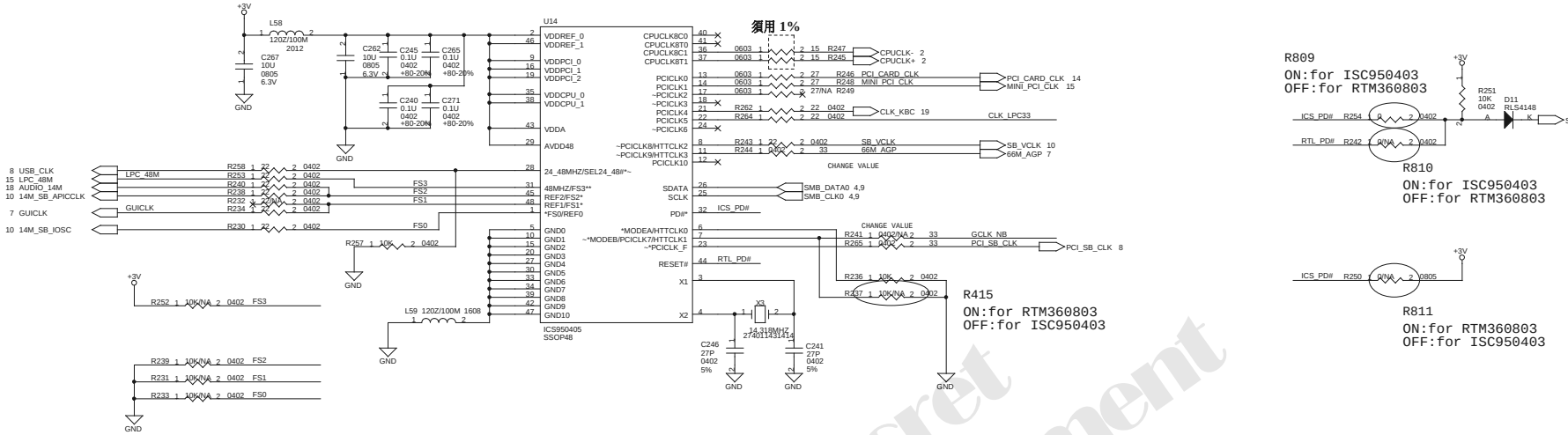
ClawHammer-Power plane(2/2)



DIMM-SLOT & Termination



CLOCK GENERATOR(ICS950405)

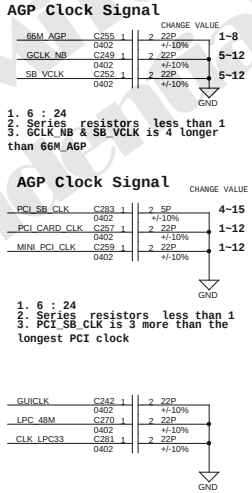


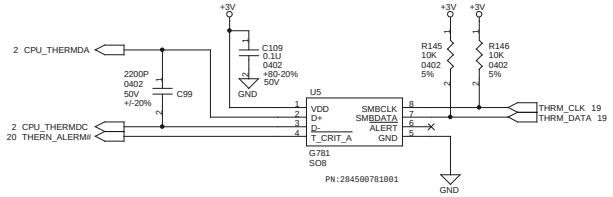
MODE FUNCTIONALITY TABLES

MODE A	MODE B	Pin6	Pin7	Pin8	Pin11
0	0	66MHZ	66MHZ	66MHZ	33MHZ
0	1	MODE A INPUT ONLY	66MHZ	66MHZ	66MHZ
1	0	33MHZ	33MHZ	33MHZ	33MHZ
1	1	MODE A INPUT ONLY	33MHZ	33MHZ	33MHZ

MODE C Pin23	Pin24
0	PCICLK6
1	PCI_STOP#

FS3	FS2	FS1	FS0	CPU Mhz	HTT Mhz	PCI Mhz	
0	0	0	0	100.90	67.27	33.63	
0	0	0	1	133.90	66.95	33.48	
0	0	1	0	168.00	67.20	33.60	
0	0	1	1	202.00	67.33	33.67	
0	1	0	0	100.20	66.80	33.40	
0	1	0	1	133.50	66.75	33.38	
0	1	1	0	166.70	67.68	33.34	
0	1	1	1	200.40	66.80	33.40	
1	0	0	0	150.00	60.00	33.00	DEFAULT
1	0	0	1	180.00	60.00	33.00	
1	0	1	0	210.00	70.00	35.00	
1	0	1	1	240.00	60.00	30.00	
1	1	0	0	270.00	67.50	33.75	
1	1	0	1	233.33	66.67	33.33	
1	1	1	0	266.67	66.67	33.33	
1	1	1	1	300.00	75.00	37.50	





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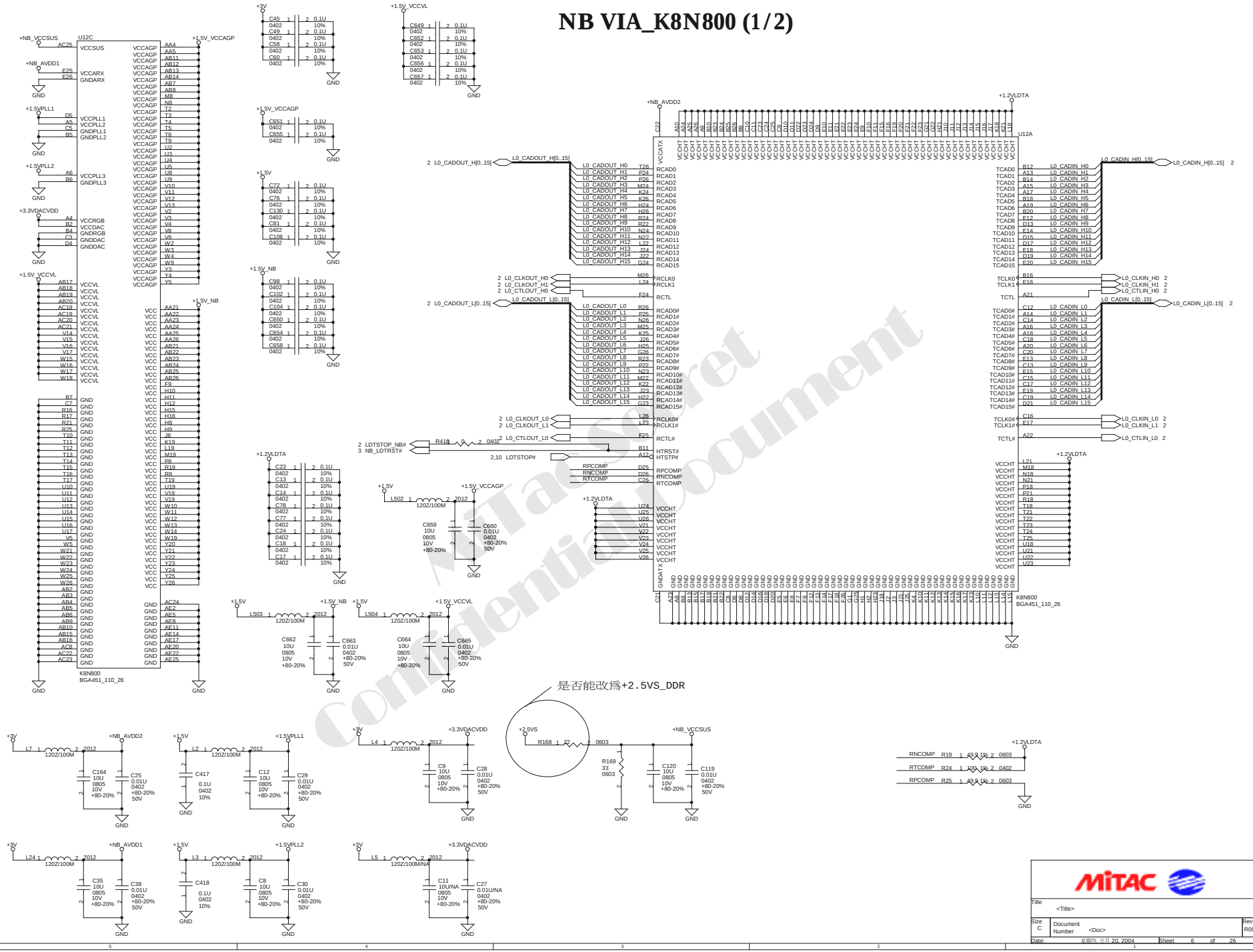
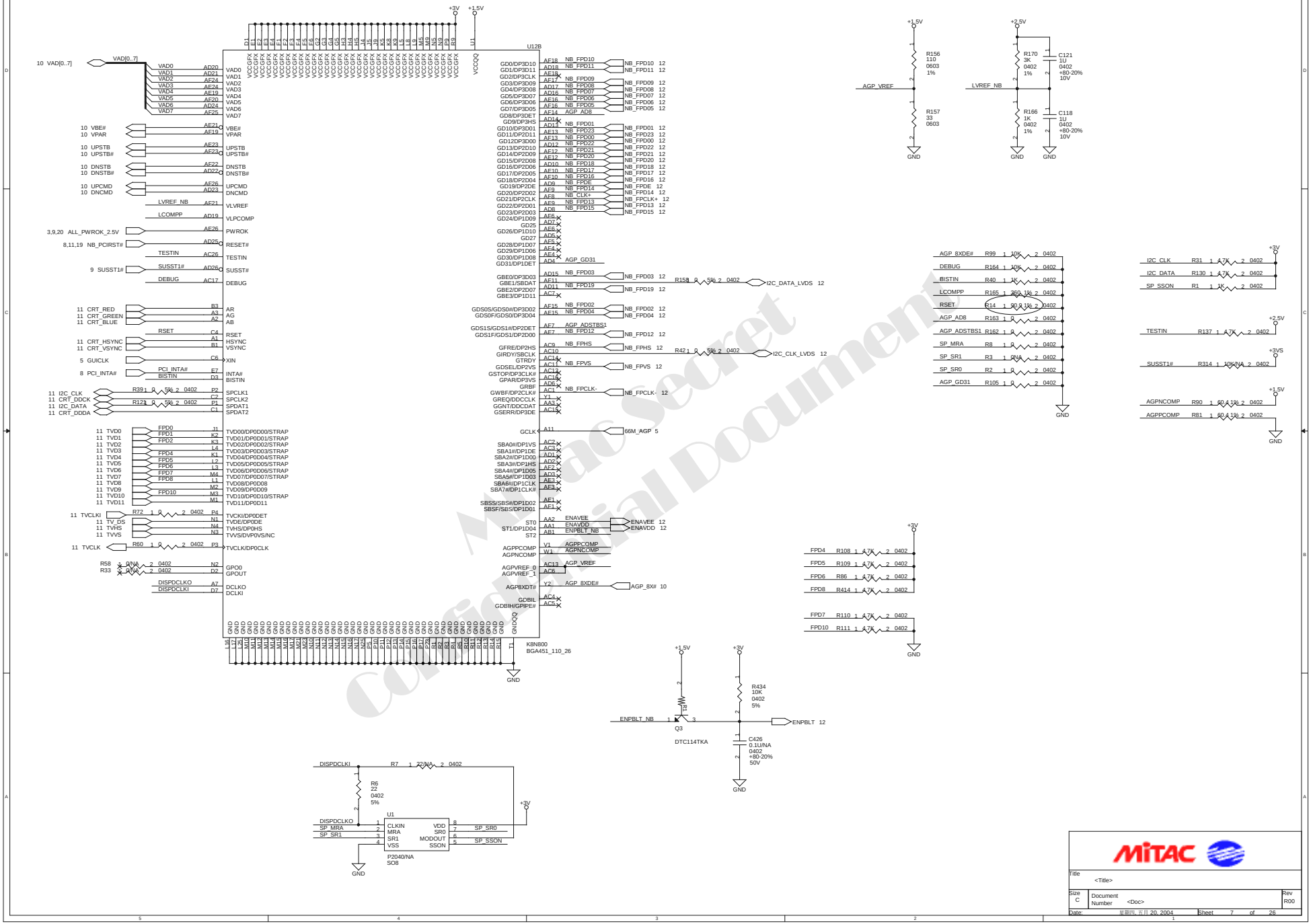
NB VIA_K8N800 (1/2)



NB VIA_K8N800 (2/2)



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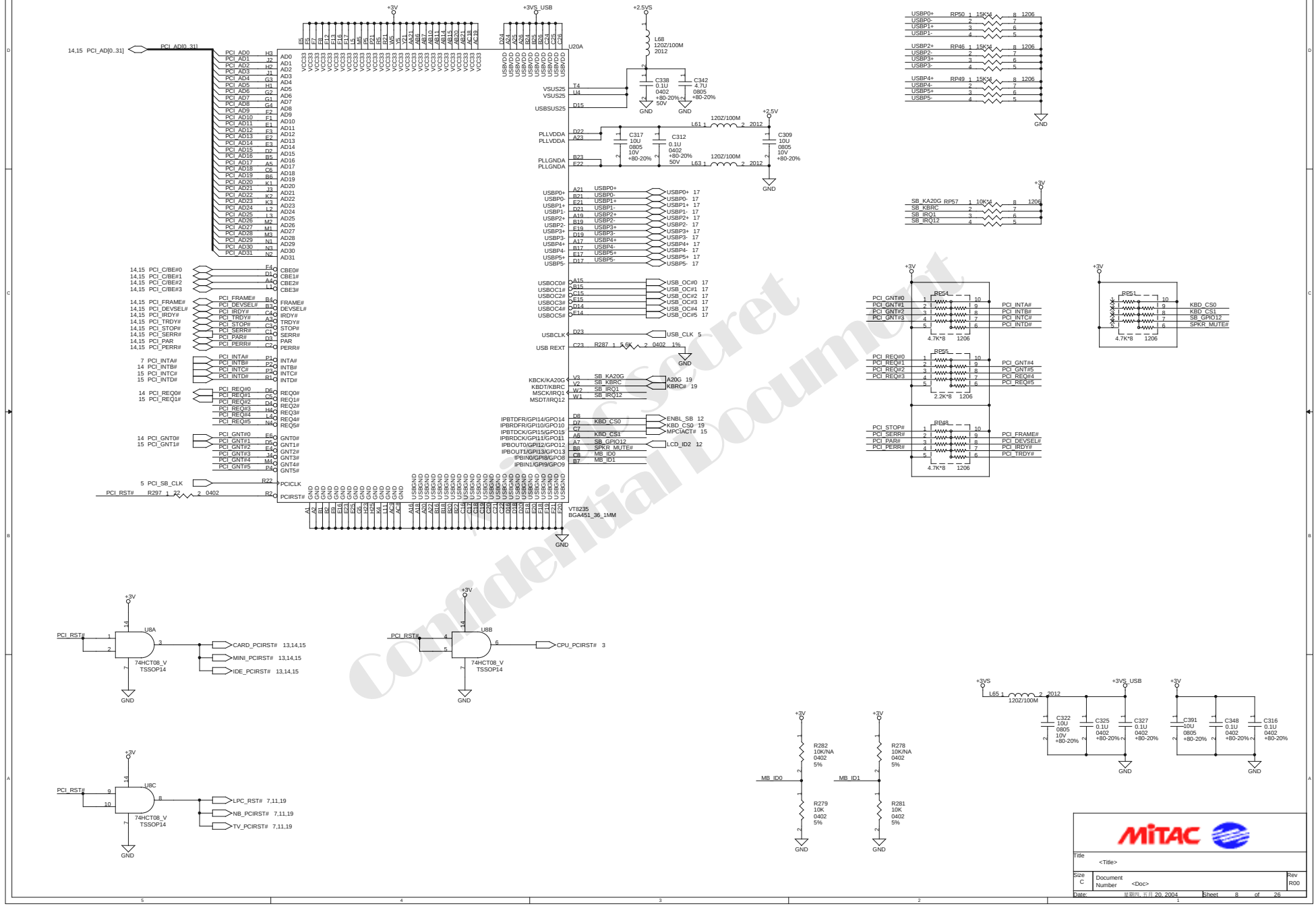
SB VIA_VT8235CD (1/3)



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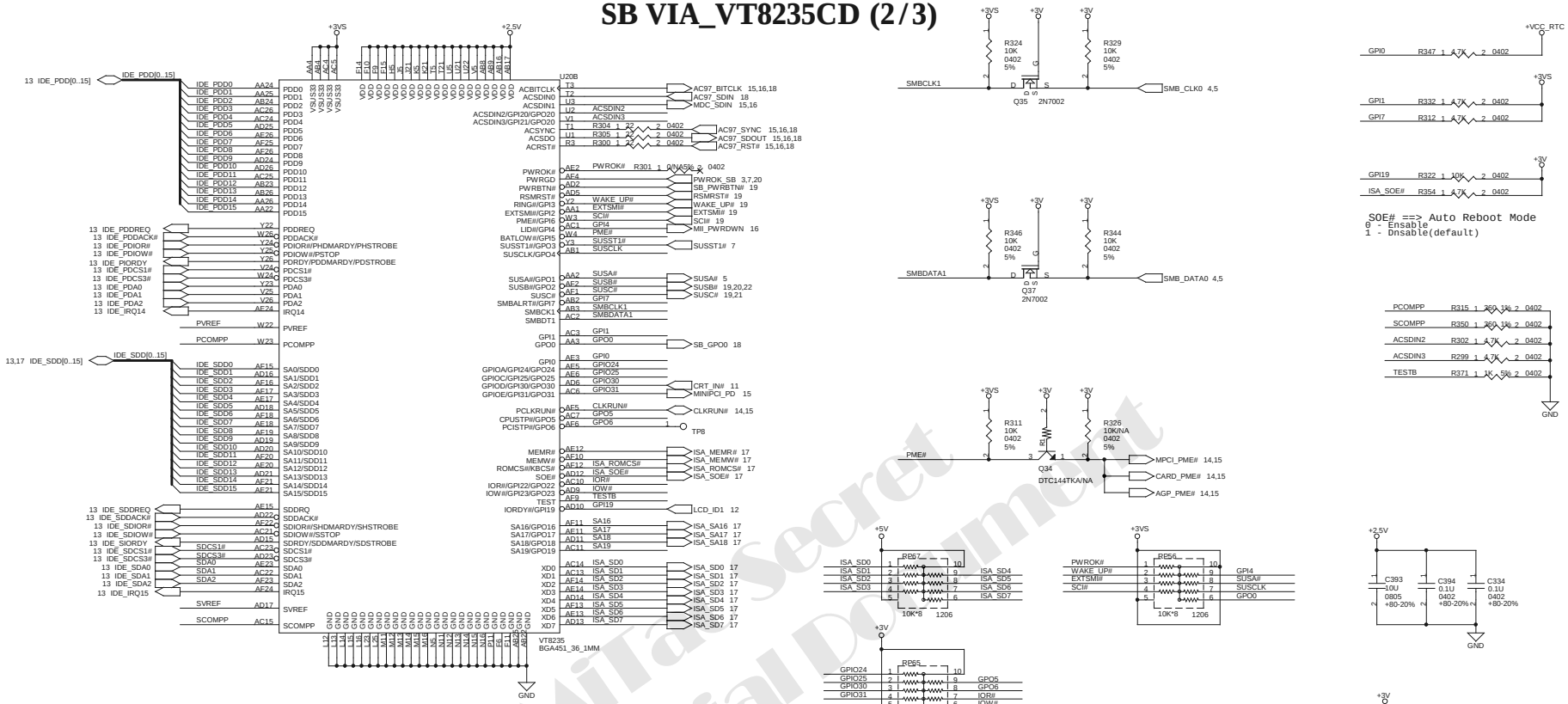
SB VIA_VT8235CD (2/3)



			PINOUT
GPI0	VCC_RTC	RESERVE	AE3
GPI1	+3VS	RESERVE	AC3
GPI2	+3VS	EXTSMI#	AA1
GPI3	+3VS	VAKE_UP#	Y2
GPI4	+3VS	MI_PWRDWN	AC1
GPI5	+3VS	PME#	W4
GPI6	+3V	SCI#	A8
GPI7	+3V	RESERVE	N4
GPI16	VCC_RTC	RESERVE	AD3
GPI17	+3V	LCD_ID0	Y1
GPI18	+3V	THRM#	Y4
GPI19	+3V	LCD_ID1	AD10
GPO0	+3VS	RESERVE	AA3
GPO1	+3VS	SUSA#	AA2
GPO2	+3VS	SUSB#	AF2
GPO3	+3VS	SB_SUSST#	Y3
GPO4	+3VS	RESERVE	AB1
GPO5	+3V	RESERVE	AC7
GPO6	+3V	RESERVE	AF6
GPO7	+3V	SB_SLP#	P4
GPO16		SEE STRAP TABLE	AF11
GPO17		SEE STRAP TABLE	AE11
GPO18		SEE STRAP TABLE	AD11
GPO19		SEE STRAP TABLE	AC11
GPIO8	+3V	MB_ID0	C8
GPIO9	+3V	MB_ID1	B7
GPIO10	+3V	KBD_CS0	D7
GPIO11	+3V	KBD_CS1	A6
GPIO12	+3V	RESERVE	A7
GPIO13	+3V	RESERVE	B8
GPIO14	+3V	ENBL_SB	D8
GPIO15	+3V	MPCIACT#	C7
GPIO20	+3V	RESERVE	U2
GPIO21	+3V	RESERVE	V1
GPIO22	+3V	SB_GHI#	R24
GPIO23	+3V	RESERVE	P26
GPIO24	+3V	SPKR_MUTE#	AE5
GPIO25	+3V	RESERVE	AE6
GPIO26	+3VS	RESERVE	AD1
GPIO27	+3VS	RESERVE	AE1
GPIO28	+3V	AGP_BX#	P25
GPIO29	+3V	RESERVE	P24
GPIO30	+3V	CRT_IN#	AD6
GPIO31	+3V	MINIPCI_PD	AC6

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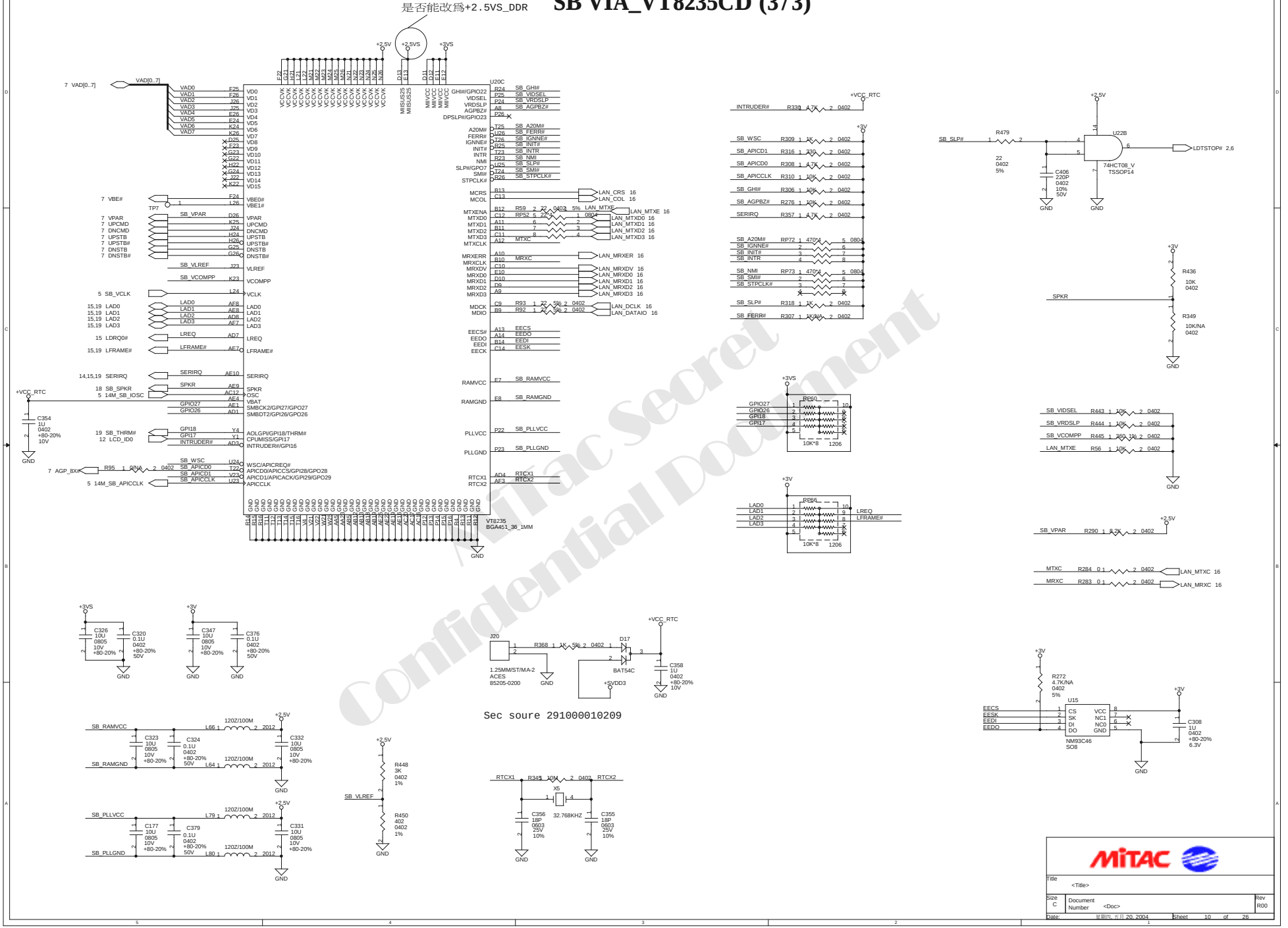
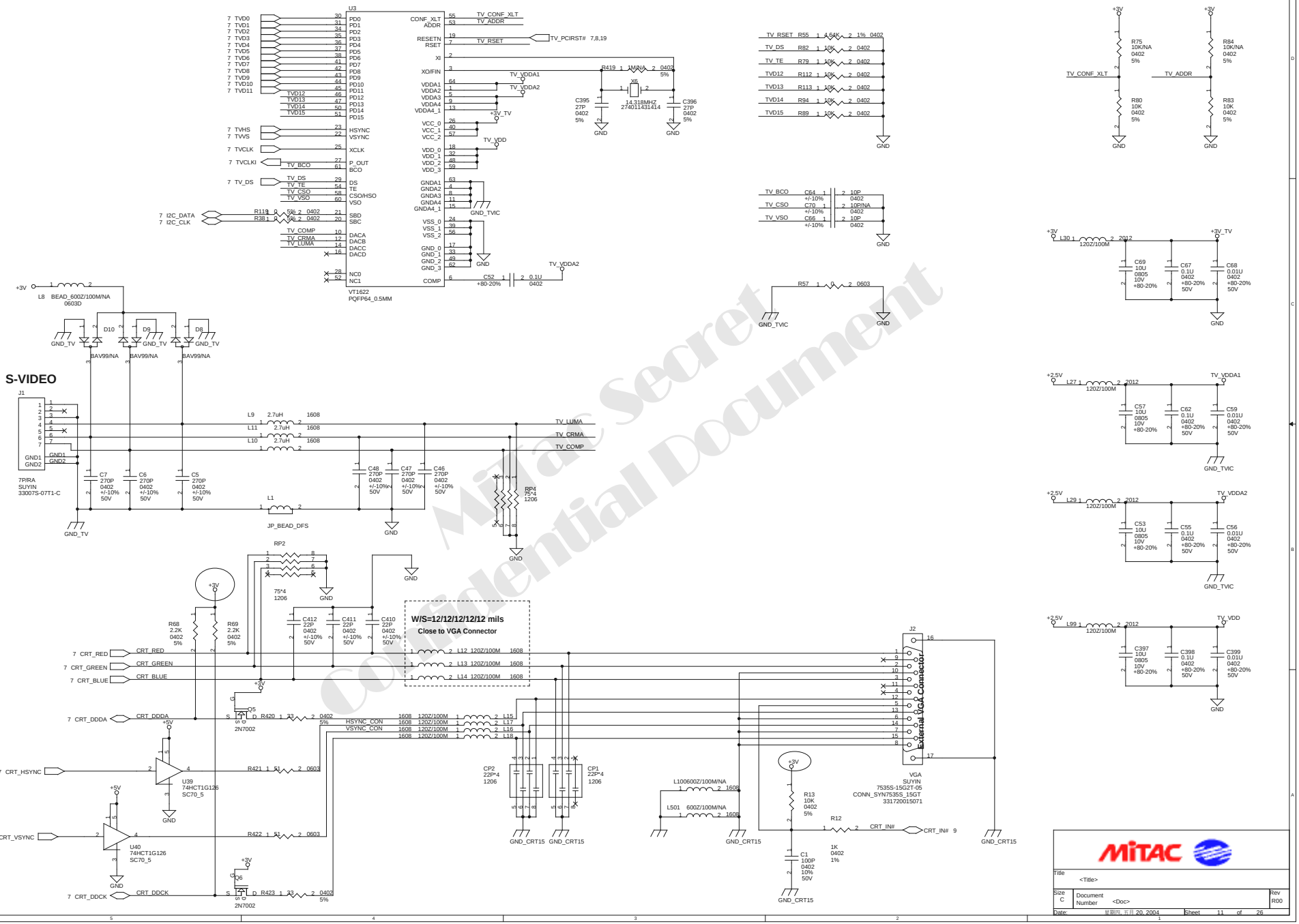
SB VIA_VT8235CD (3/3)

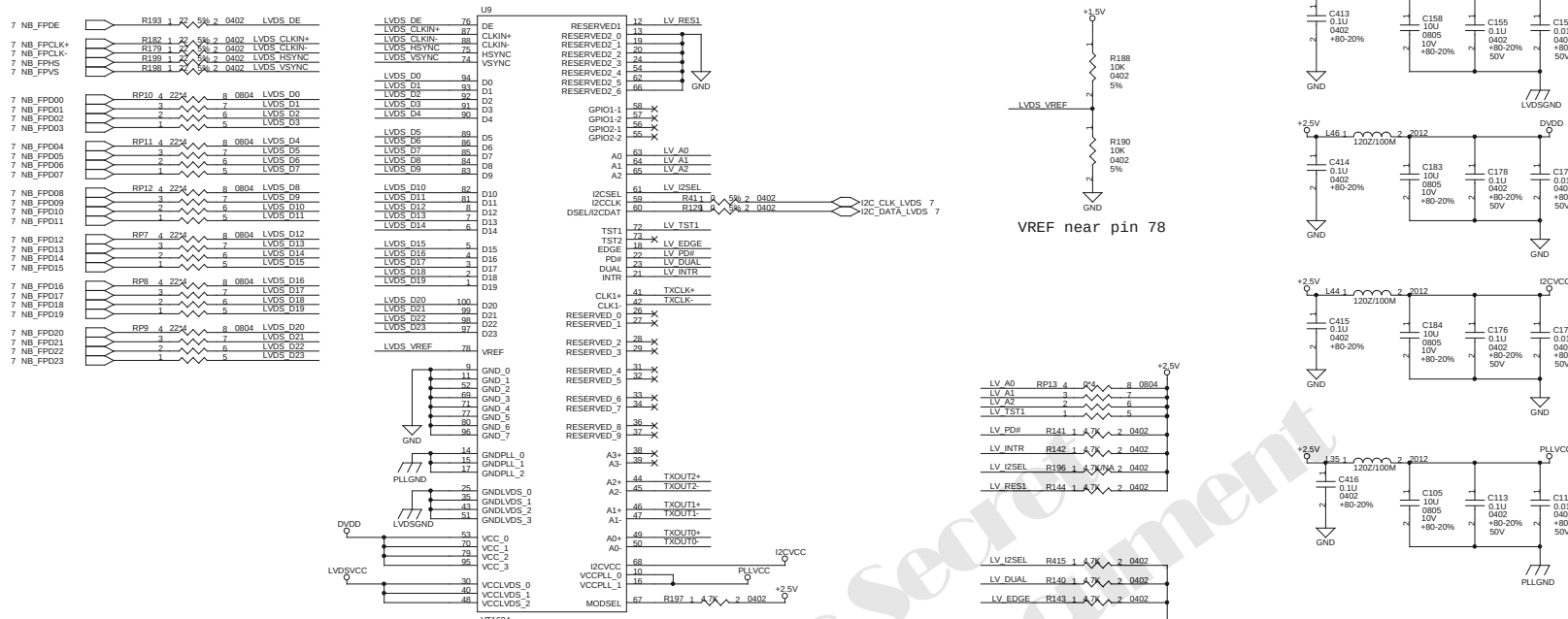
是否能改爲+2.5VS_DDR



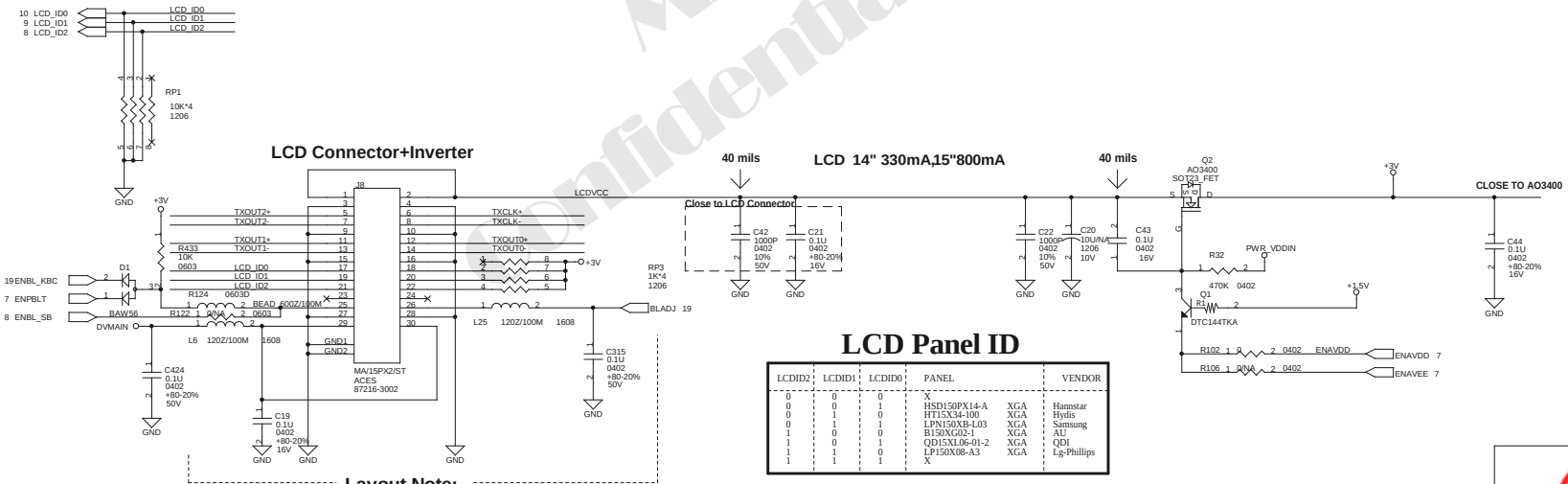
TV Encoder(VIA_VT1622)



LVDS Encoder(VIA_VT1634)



	DUAL (pin23)
For one channel panel	Low Remove R10 Install R8
For two channel panel	High Remove R8 Install R10



LCD Panel ID

LCDID2	LCDID1	LCDID0	PANEL		VENDOR
0	0	0	X		
0	0	1	HSD150PX14-A	XGA	Hannstar
0	1	0	HT15X34-100	XGA	Hydis
0	1	1	LPN150XB-L03	XGA	Samsung
1	0	0	B150XG02-1	XGA	AU
1	0	1	QD15XL06-01-2	XGA	QDI
1	1	0	LP150X08-A3	XGA	Lg-Phillips
1	1	1	X		

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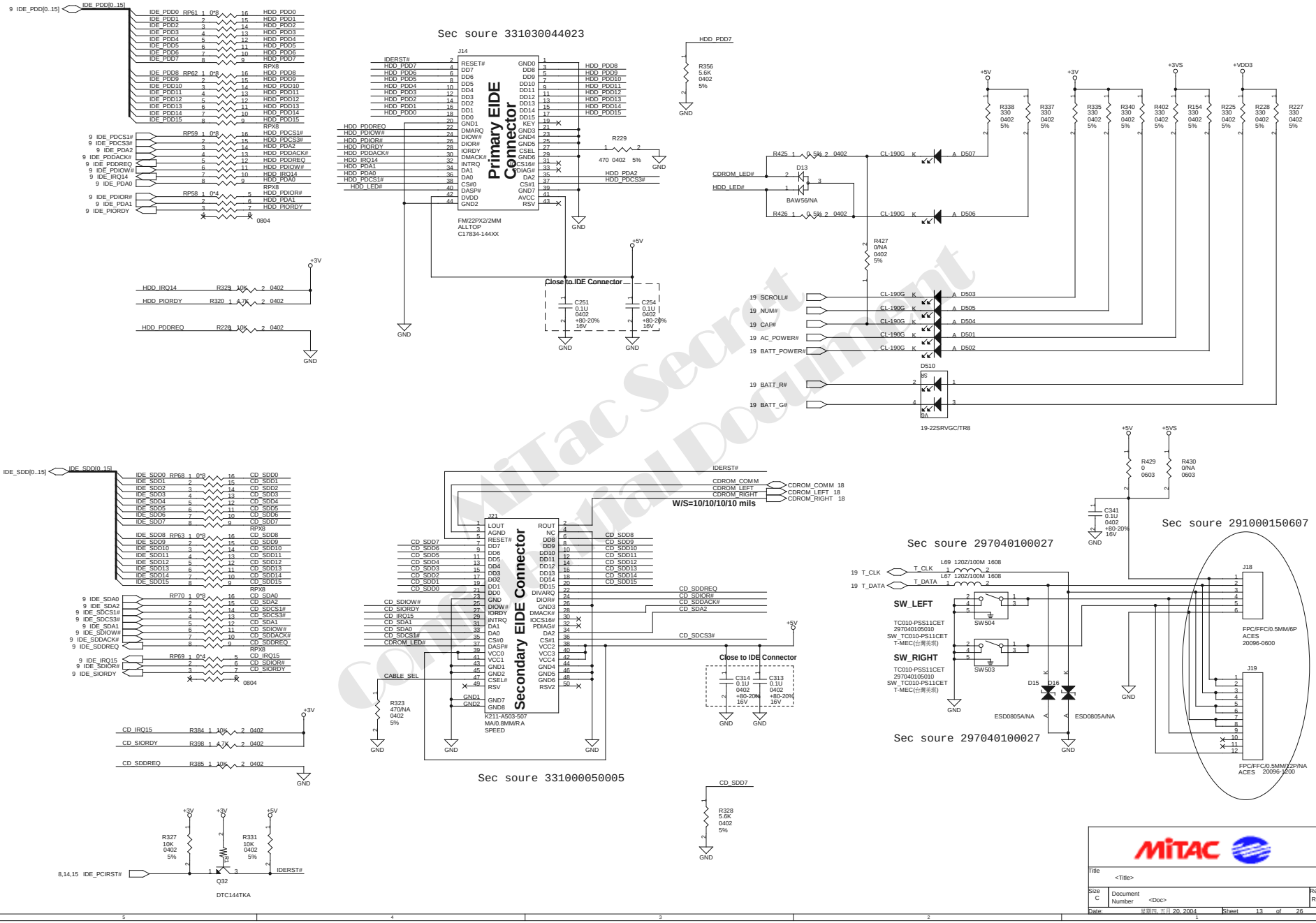
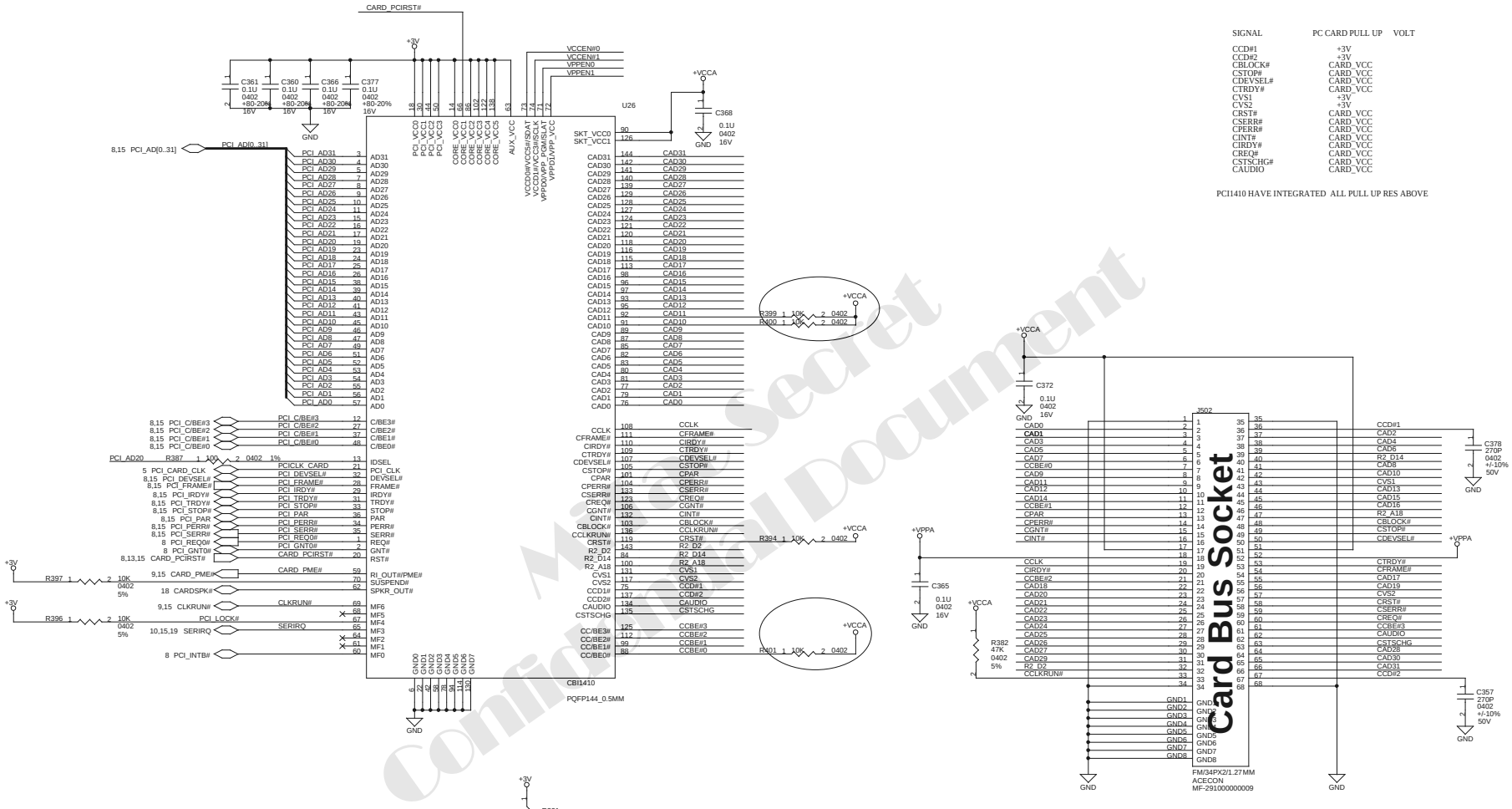
HDD & CD_ROM Conntor



AD20
PCI_INTB#

REQ0#/GNT0#

PCMCIA CONTROLLER & CARDBUS SCOKET



SIGNAL	PC CARD PULL UP	VOLT
CCD#1	+3V	
CCD#2	+3V	
CBLOCK#	CARD_VCC	
CSTOP#	CARD_VCC	
CDEVSEL#	CARD_VCC	
CTRDY#	CARD_VCC	
CVS1	+3V	
CVS2	+3V	
CRST#	CARD_VCC	
CSERR#	CARD_VCC	
CPERR#	CARD_VCC	
CINT#	CARD_VCC	
CIRDY#	CARD_VCC	
CREQ#	CARD_VCC	
CSTSCHG#	CARD_VCC	
CAUDIO	CARD_VCC	

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE

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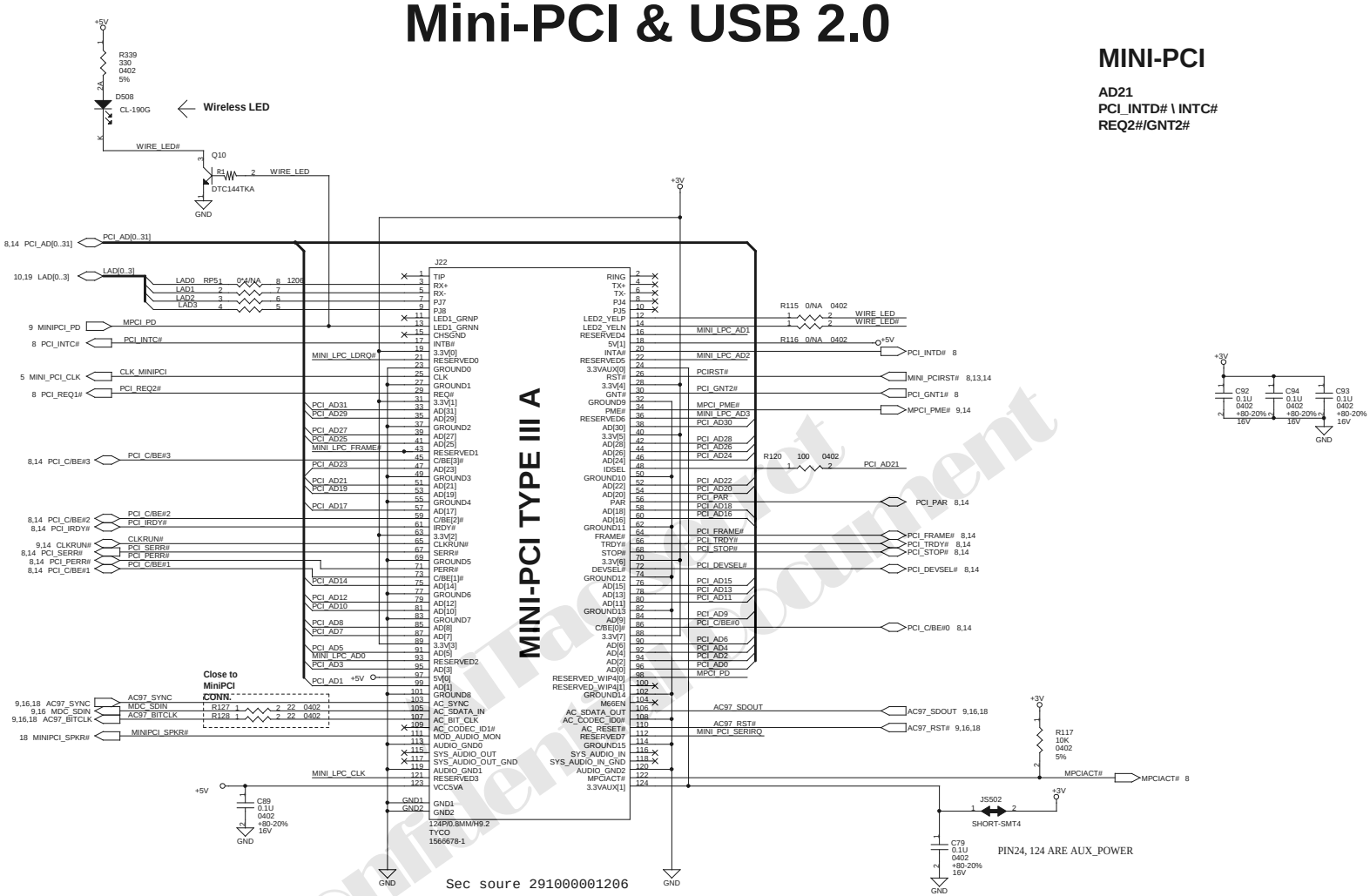
Mini-PCI & USB 2.0

MINI-PCI

AD21
PCI_INTD# \ INTC#
REQ2#/GNT2#



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LAN PHY (VT6103L) & MDC

Layout Note:

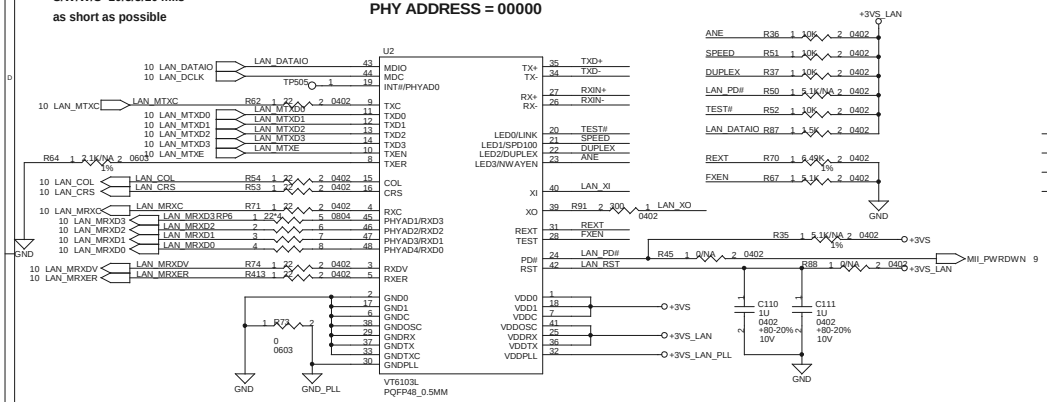
二組各自平行走線尋長

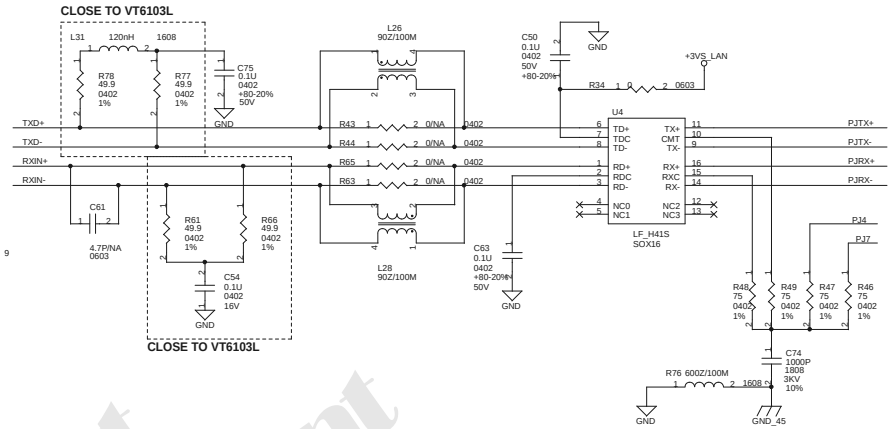
二組中間須包地線, EX: GND SHIELDING

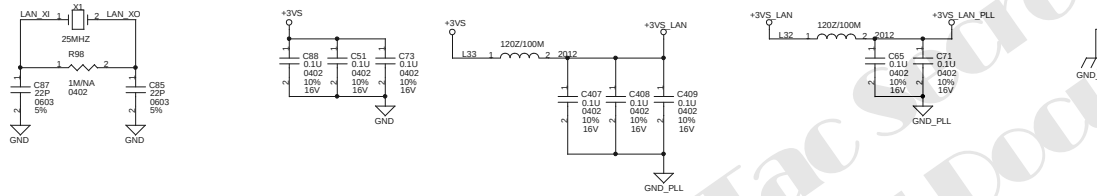
S/W/W/S=10/8/8/10 mils

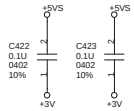
as short as possible

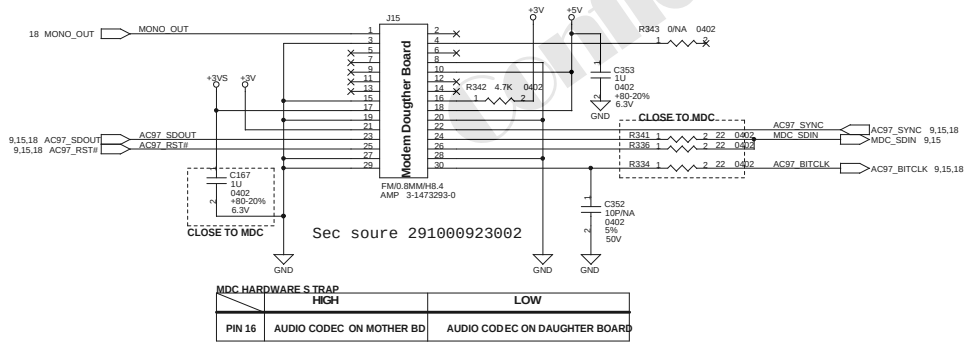
PHY ADDRESS = 00000









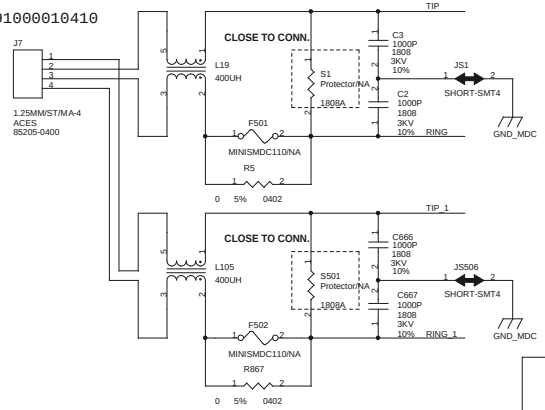


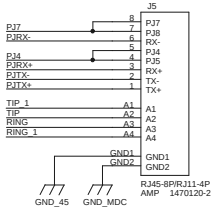
Sec soure 291000923002

MDC HARDWARE S TRAP

	HIGH	LOW
PIN 16	AUDIO CODEC ON MOTHER BD	AUDIO CODEC ON DAUGHTER BOARD

Sec soure 291000010410





Sec soure 291000810819

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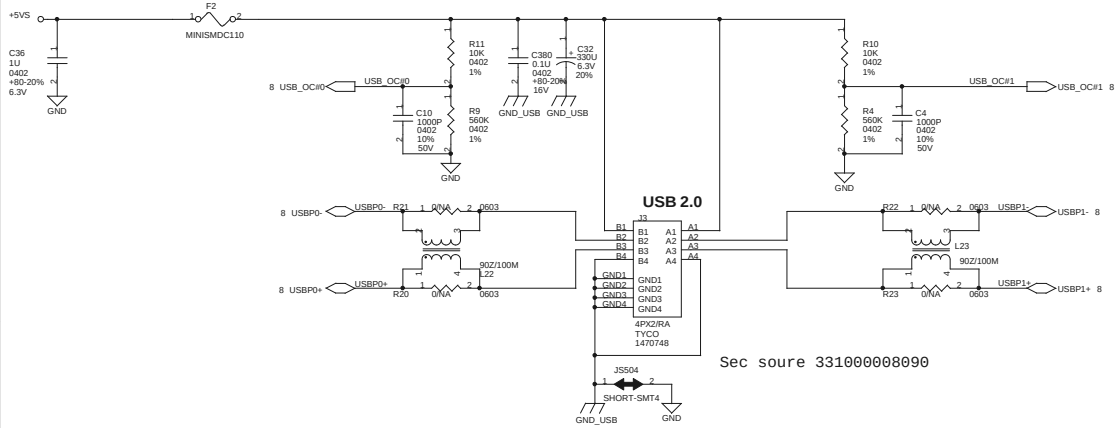
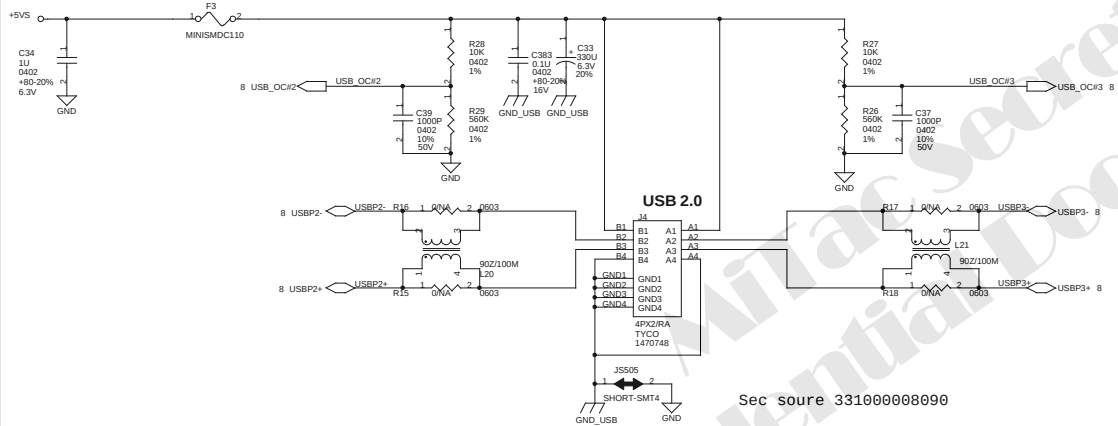
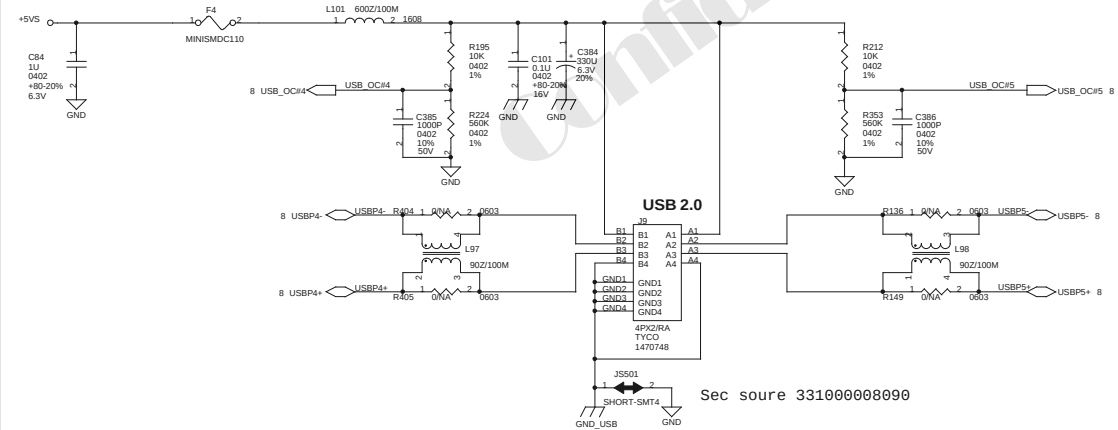
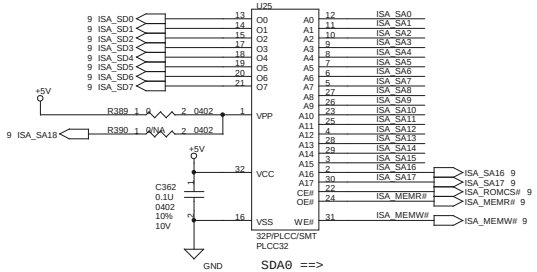
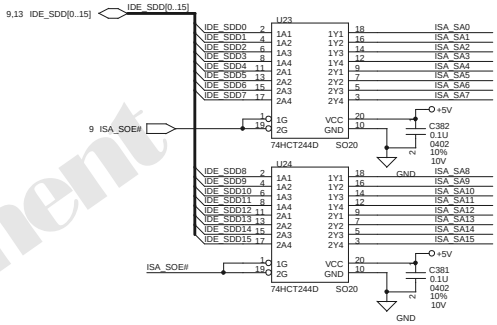
USB2.0 & Flash ROM

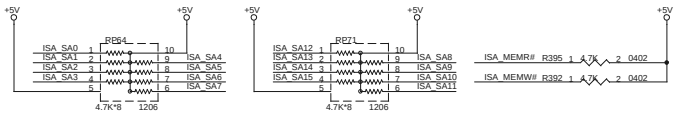












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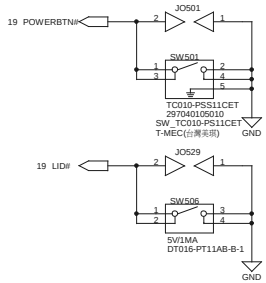

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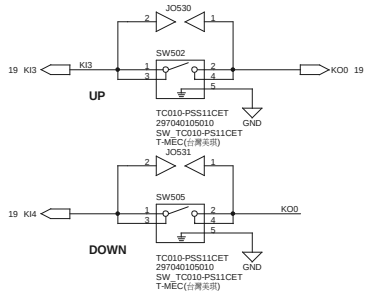

Sec soure 297030105003

Sec soure 297040100027

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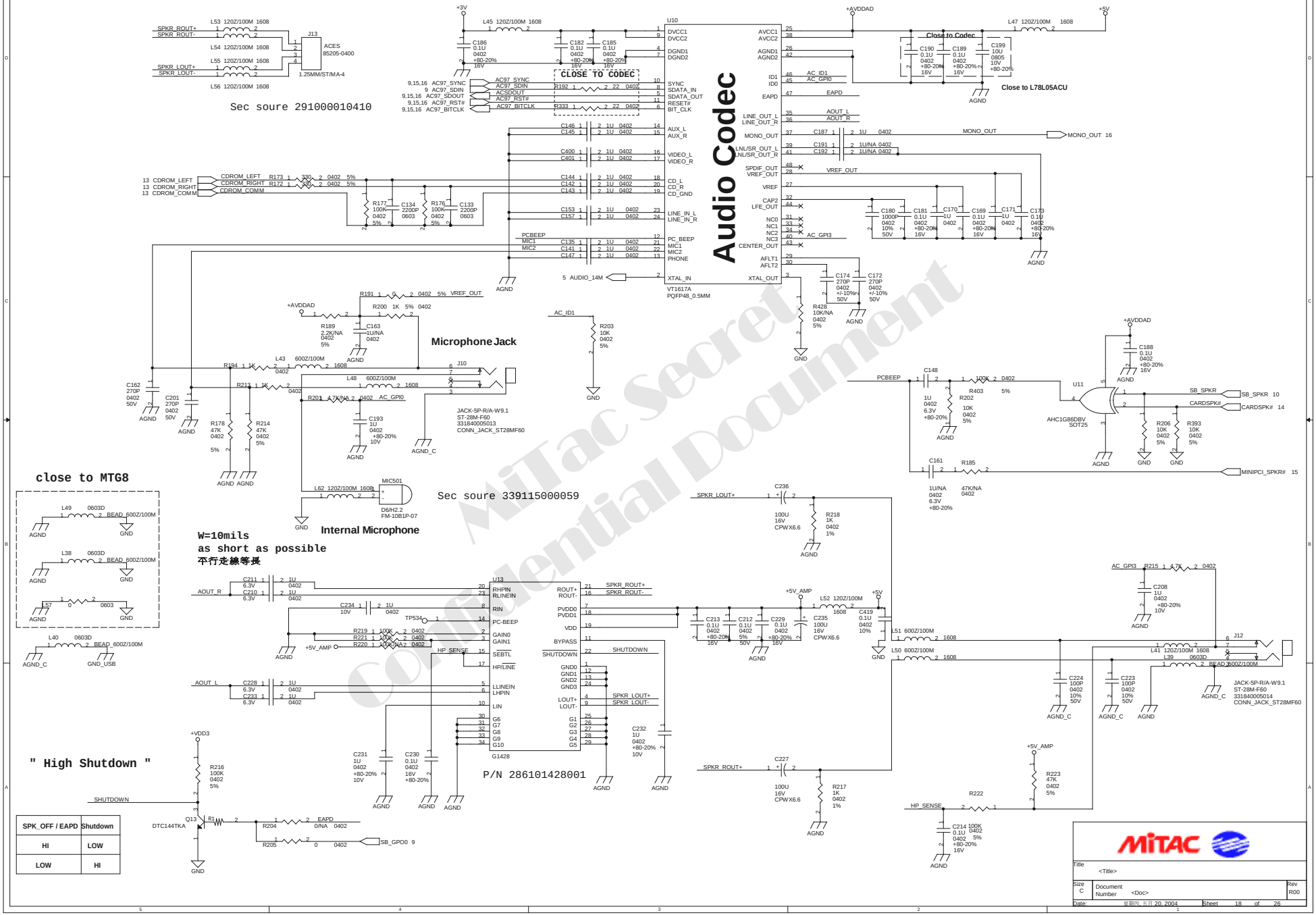
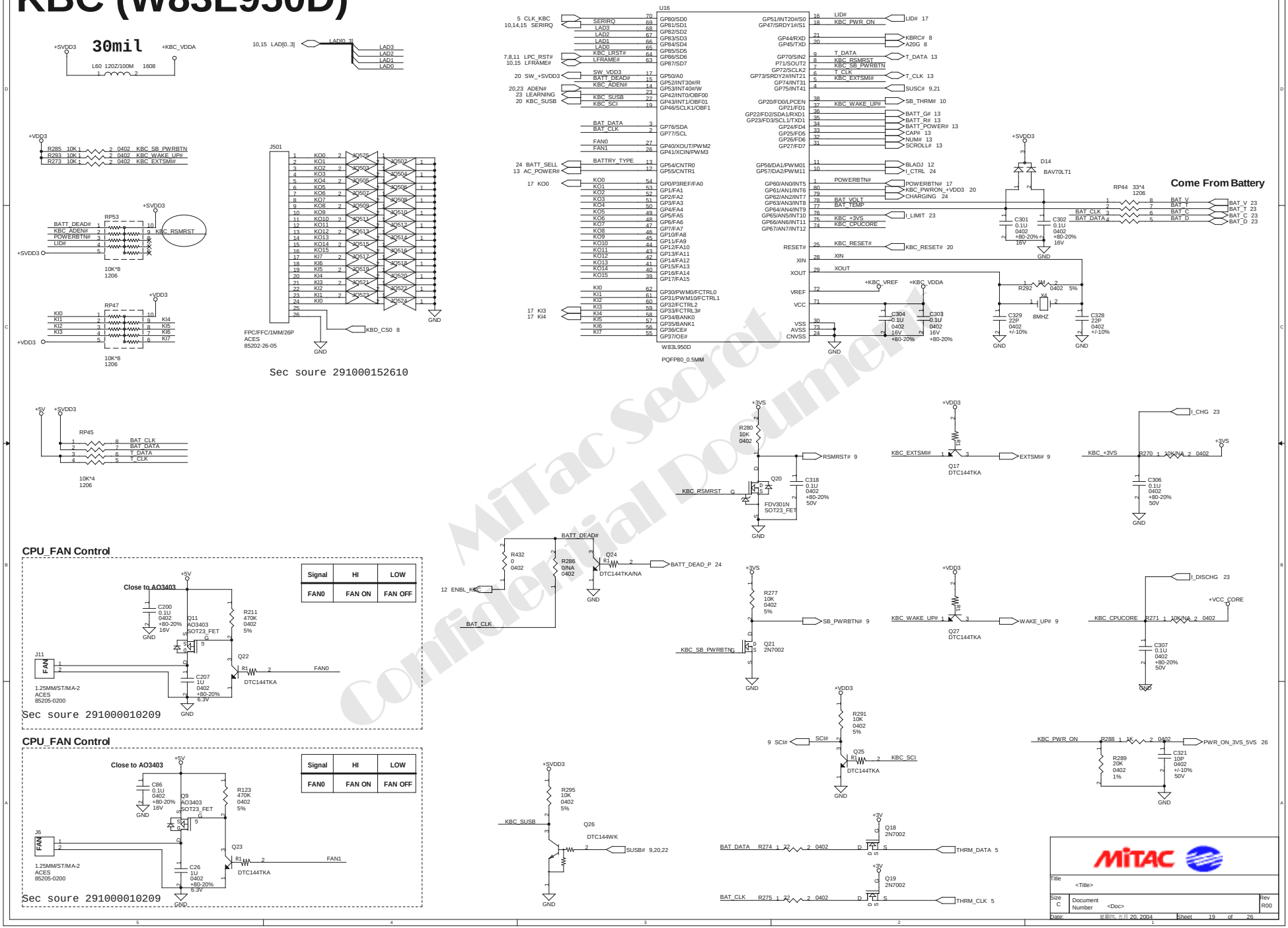
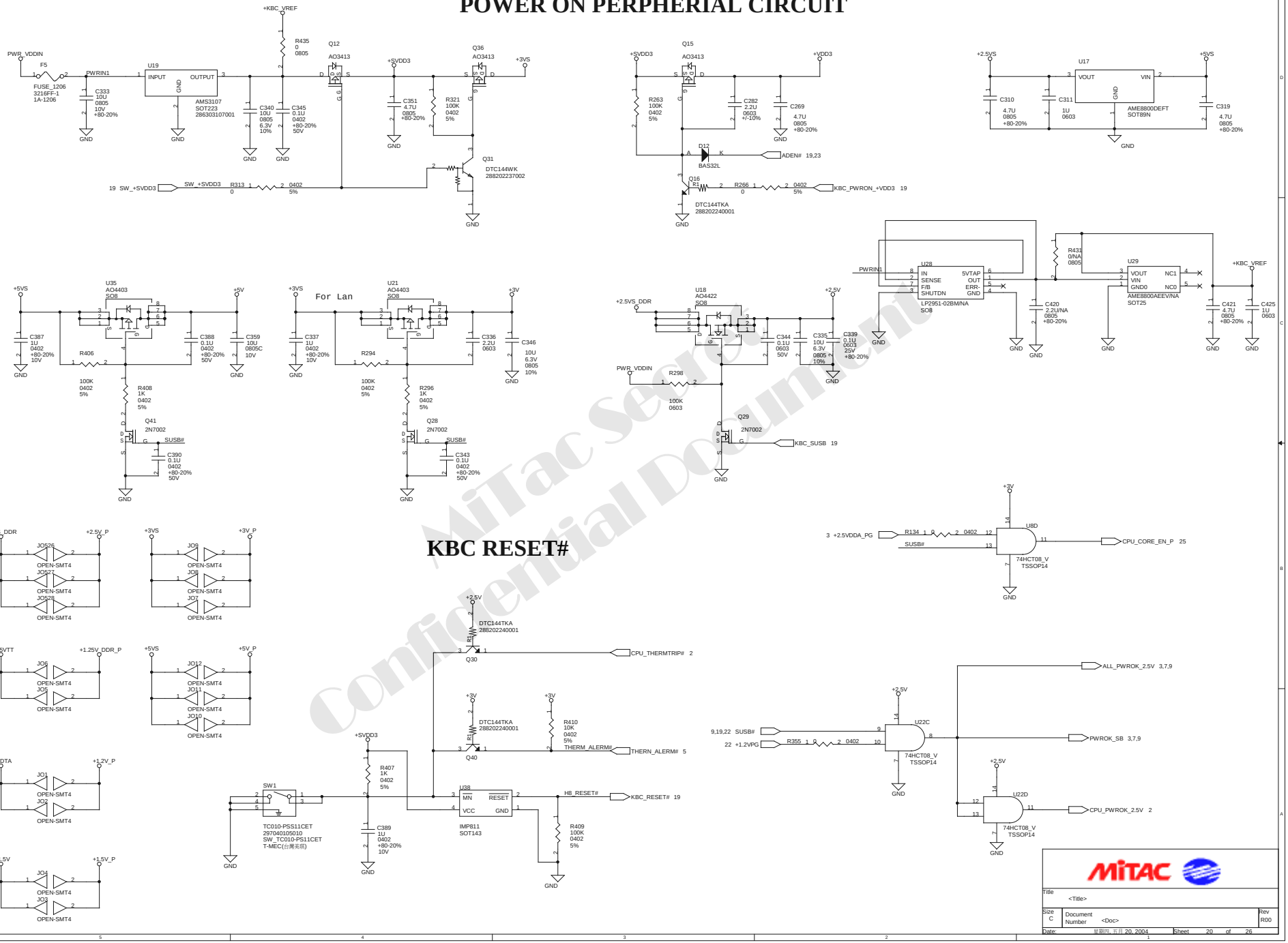
Audio CODEC(VT1617A)



KBC (W83L950D)



POWER ON PERPHERIAL CIRCUIT



KBC RESET#

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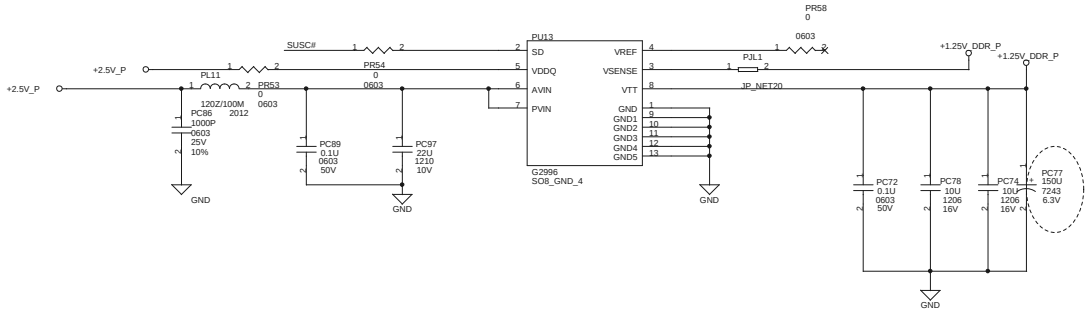
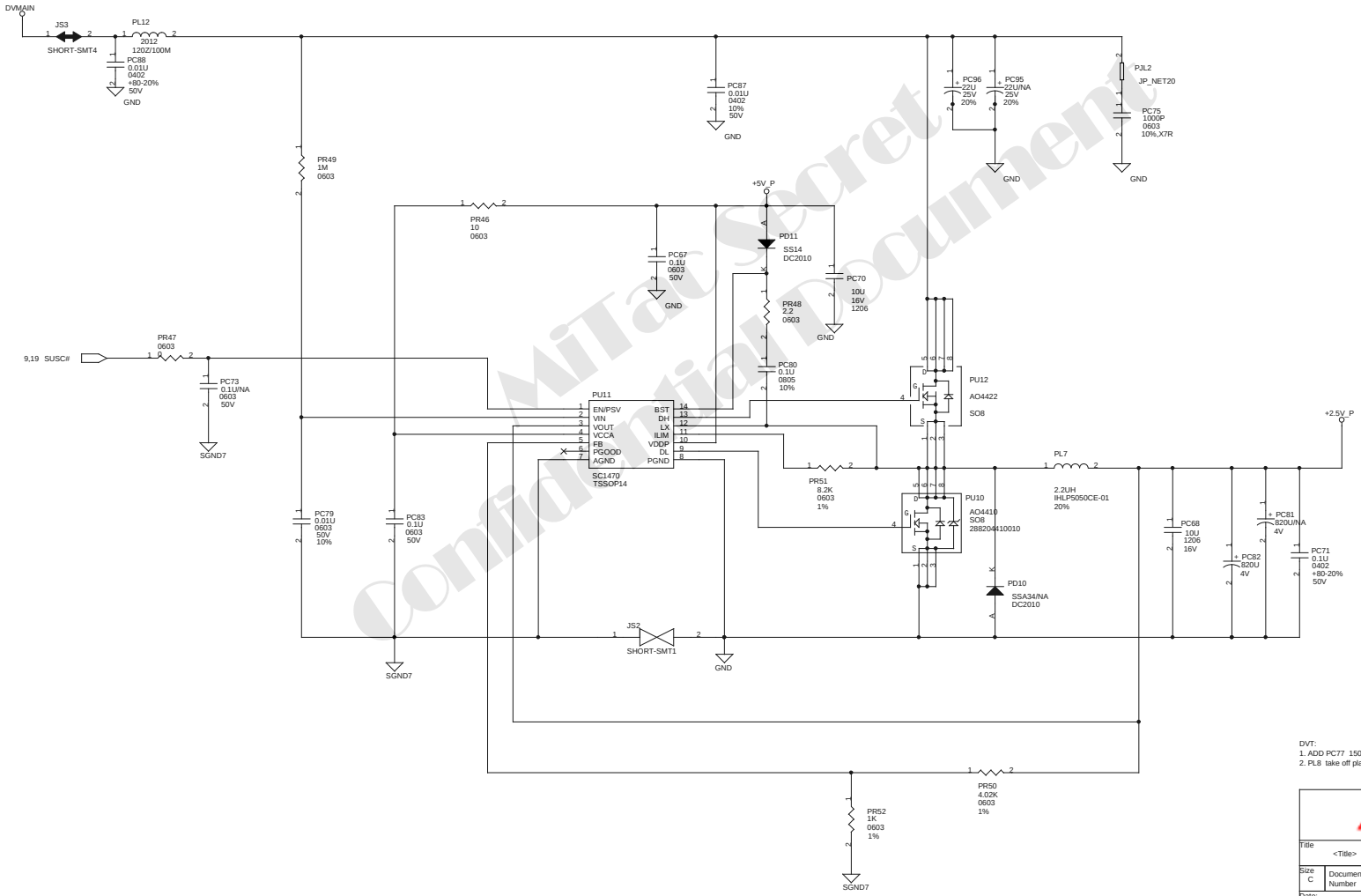
+1.25V



+2.5V_P



DVT:
1. ADD PC77 150U/6.3V
2. PL8 take off placement

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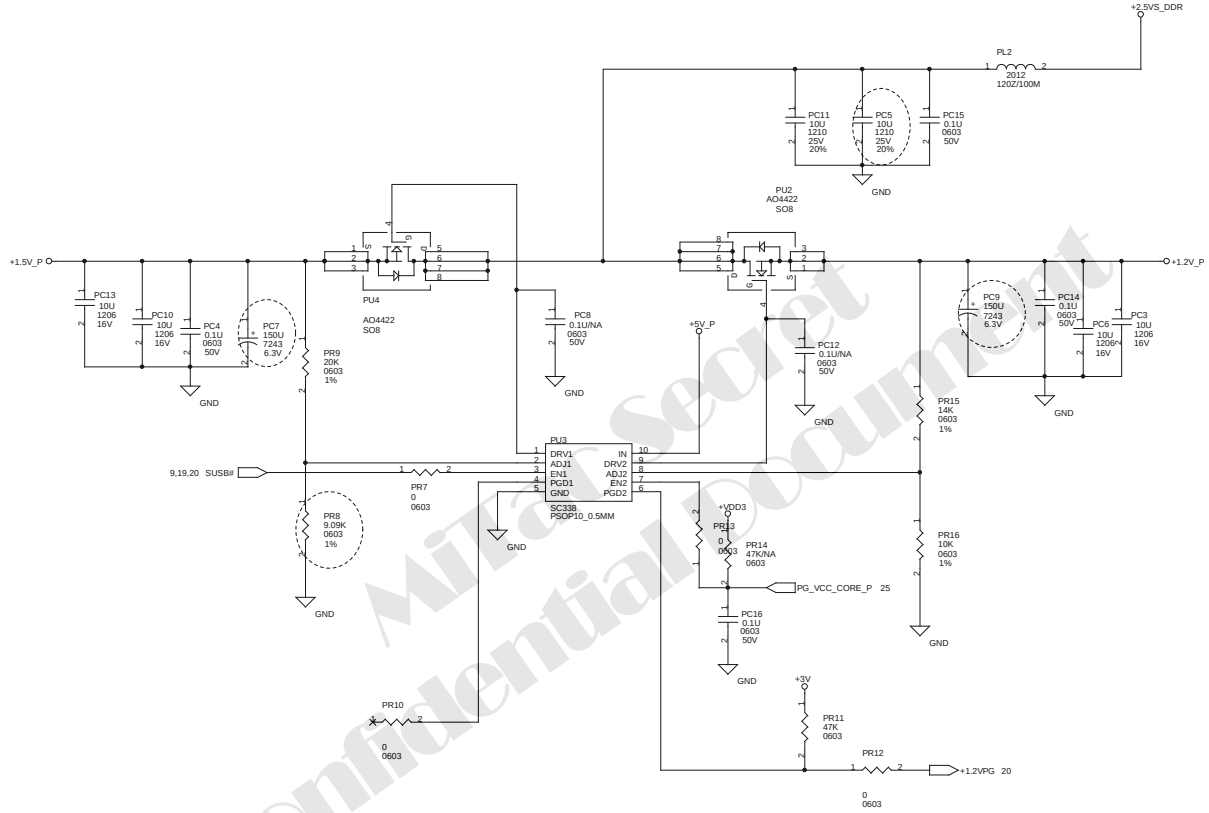

DVT:
1. ADD PC7.PC9 150U/6.3V
2. ADD PC5 10U/25V change from 272023106701 to 272023106502
3. PR8 change from 10Kto 9.09 for H/W +1.57V

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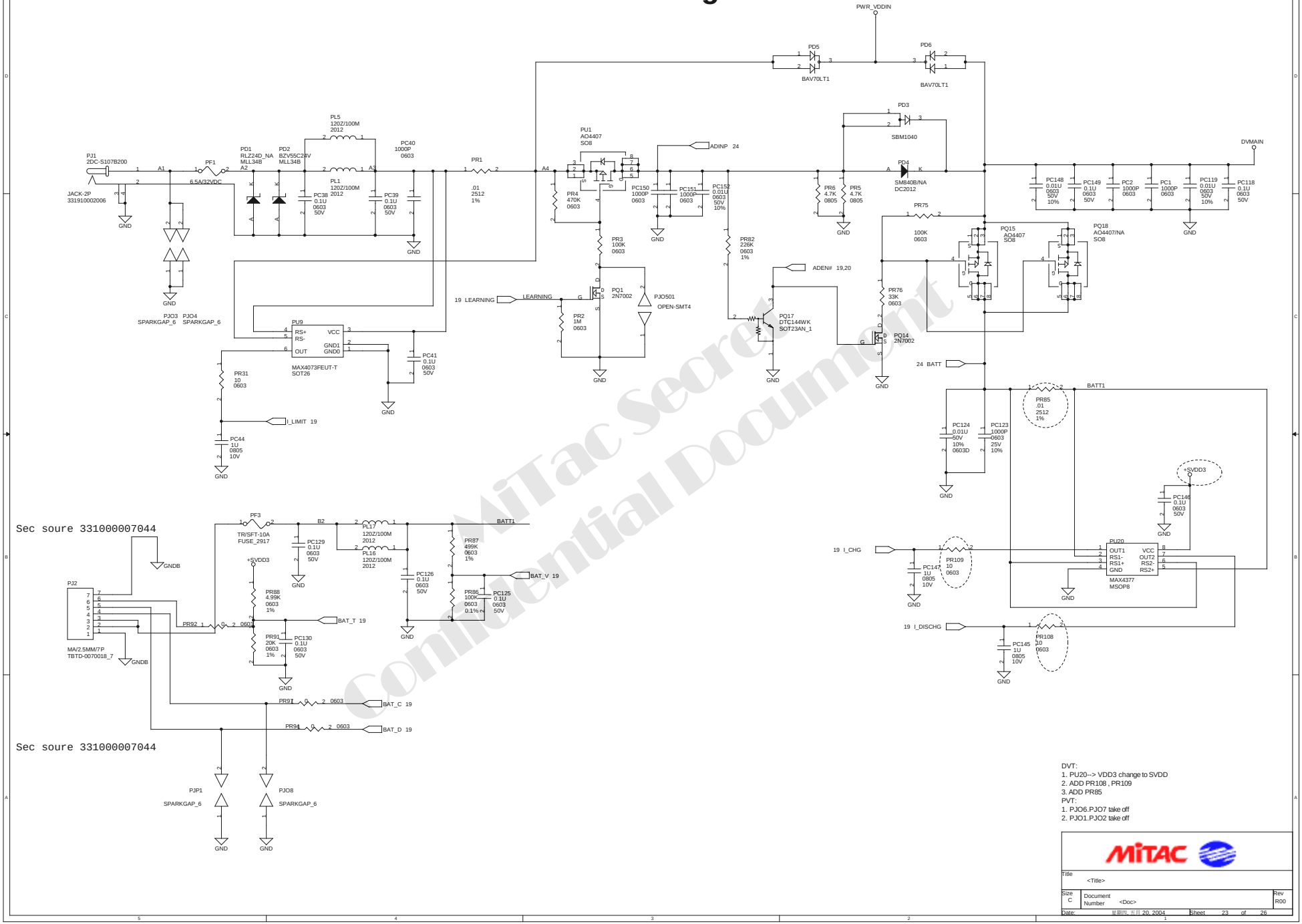
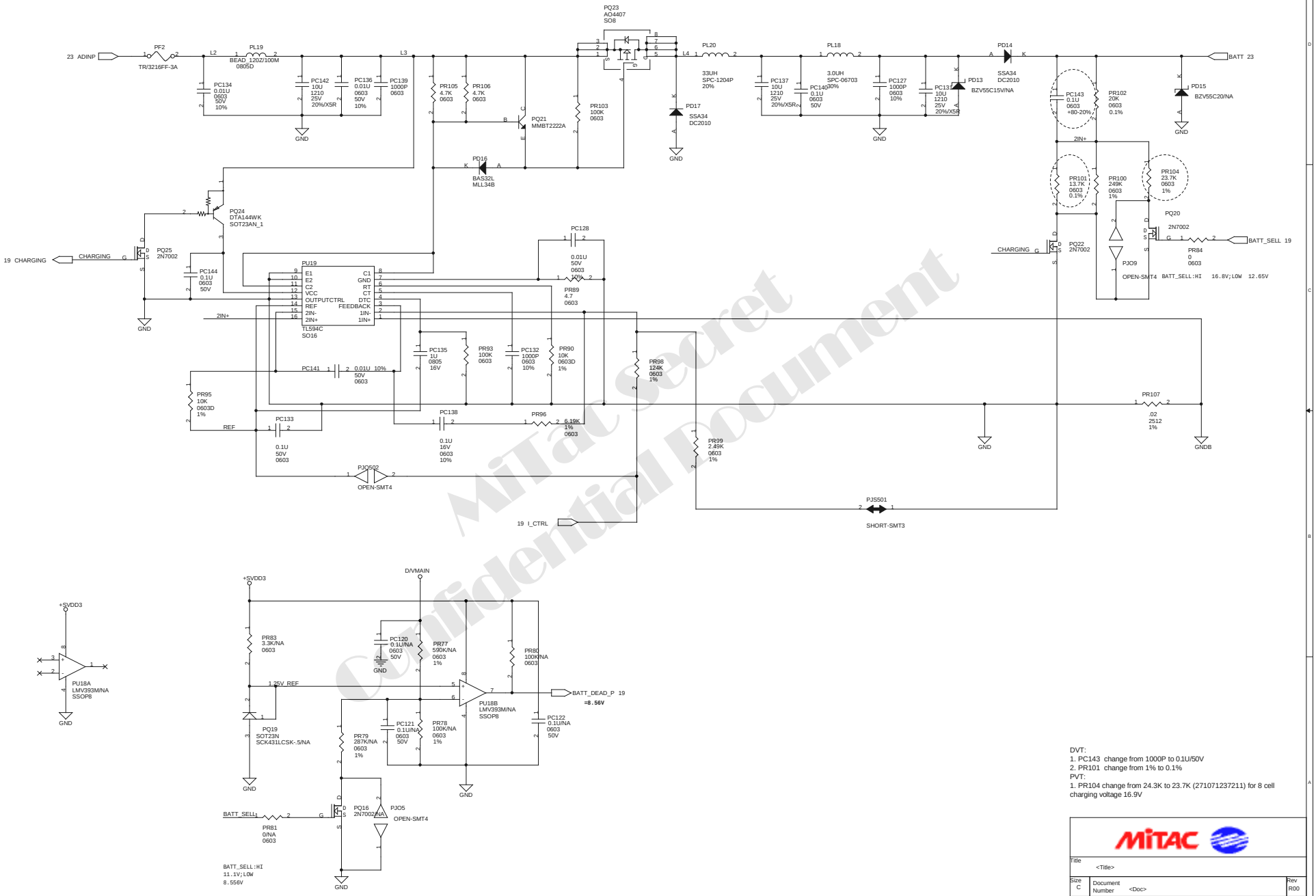
ADPIN & Dischrage



CHARGING



DVT:
1. PC143 change from 1000P to 0.1U/50V
2. PR101 change from 1% to 0.1%
PVT:
1. PR104 change from 24.3K to 23.7K (271071237211) for 8 cell charging voltage 16.9V

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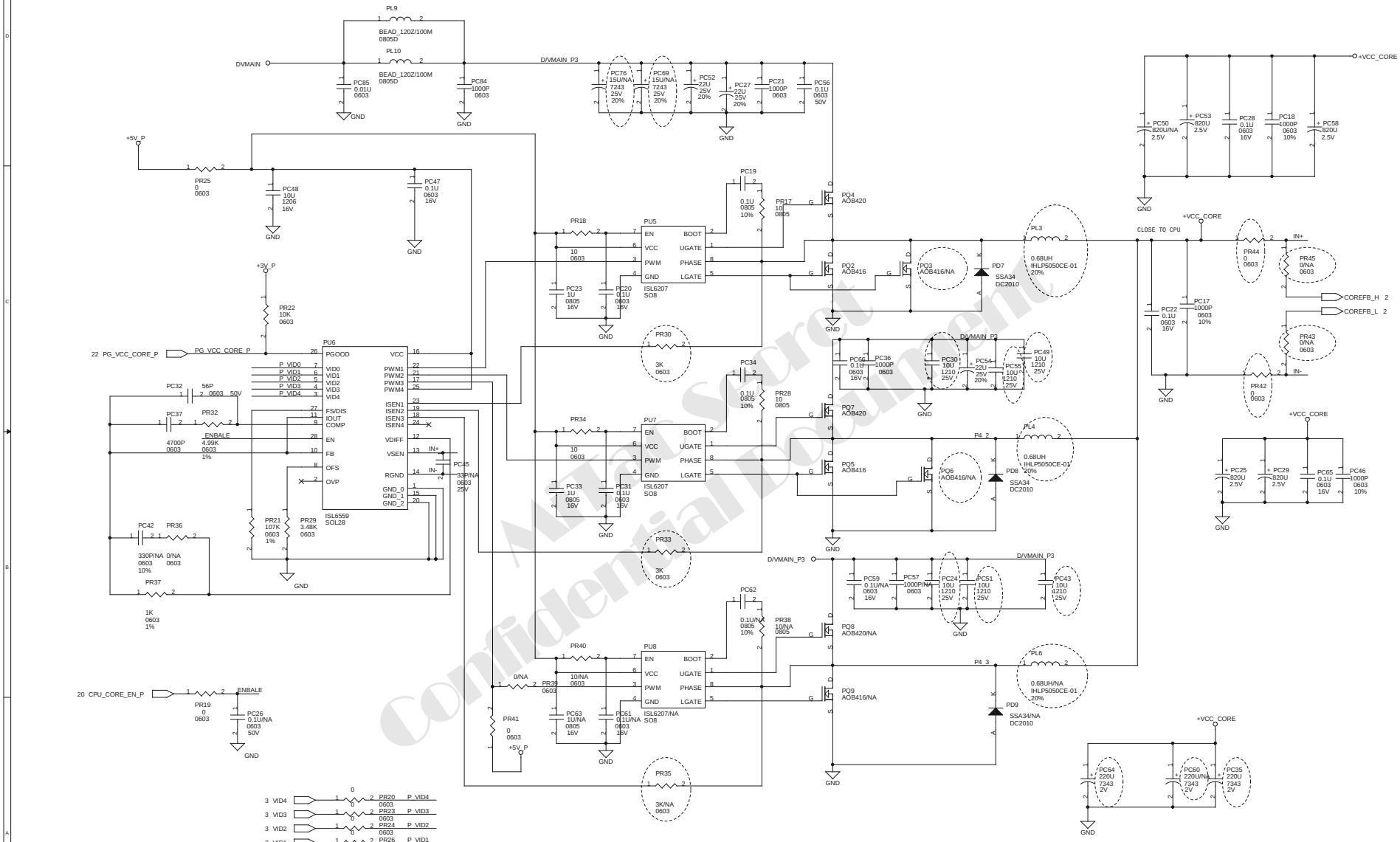
VCC_CORE



DVT:
1. PL3.PL4.PL6 change to 273000990127
2. ADD PR44.PR42 , PR43.PR45 N/A
3. PR30.PR33.PR35 change from 2K to 3K , for one low-side mos O.C.P
4.PQ3.PQ6 /NA
5.ADD input cap PC76.PC69.PC30.PC55.PC49.PC24.PC51.PC43
6.ADD output cap PC64.PC60.PC35
7.PC24.PC30.PC43.PC49.PC51.PC55 change from 272023106701 to 272023106502
PVT:
1. PC69.PC76.PC60 N/A

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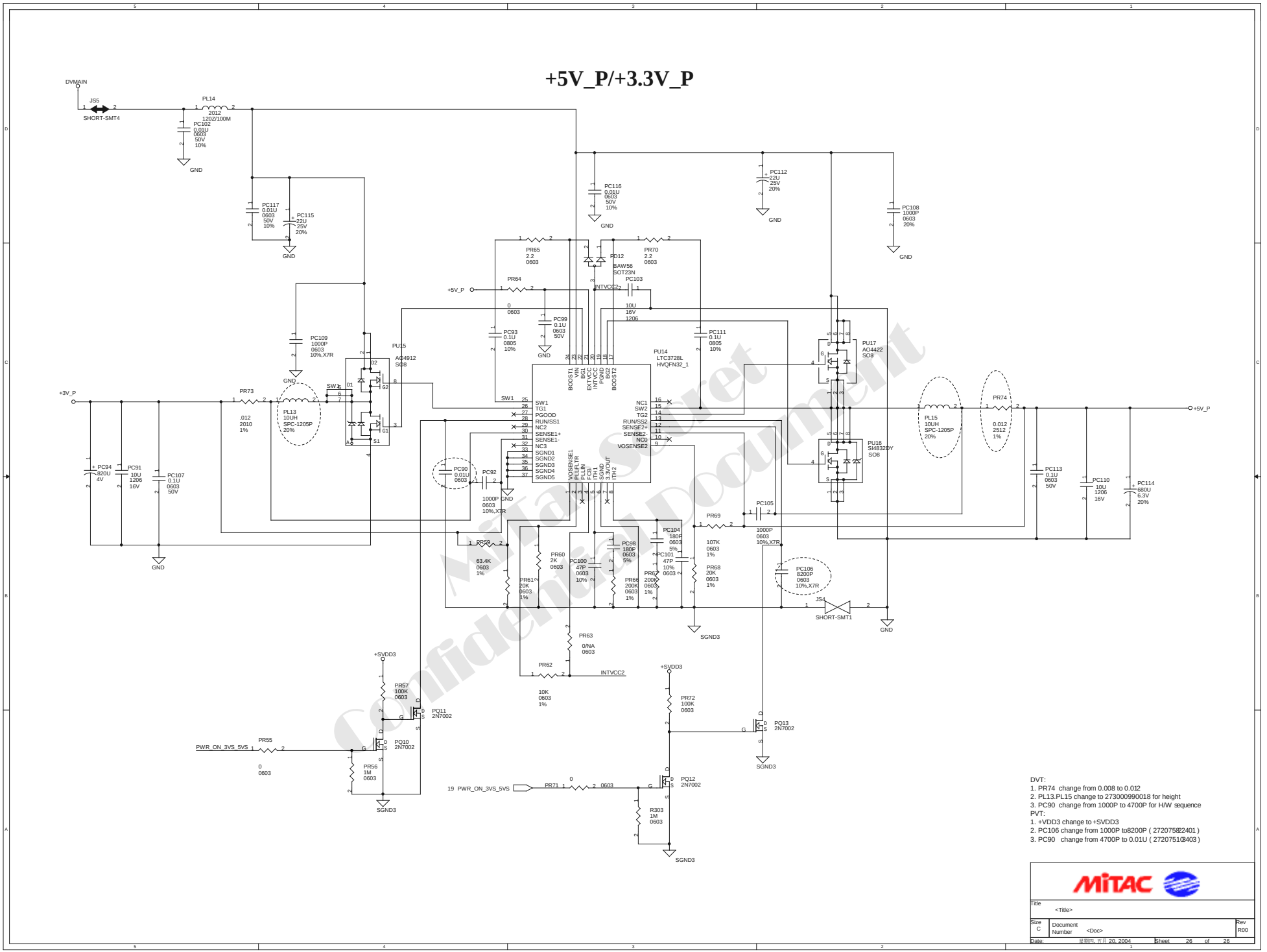

REFERENCE MATERIAL

AMD Athlon 64 CLAWHAMMER Processor	AMD, INC.
“VIA K8N800 North Bridge”	VIA, INC.
“VIA VT8235 South Bridge”	VIA, INC.
H8/W83L950D	WINBOND, LTD.
System Explode View	Technology Corp / MiTAC
8399 Hardware Specification	Technology Corp / MiTAC

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