Power Draw

Note:

- Multi-Tech Systems, Inc. recommends that you incorporate a 10% buffer into the power source when determining product load.
- Transmit power measured with MTXDOT-NA1-xxx transmitting to a MultiConnect Conduit with an MTAC-LORA-915 accessory card installed.
- Power measurements are similar for MTXDOT-EU1-xxx models. Some 868 MHz sub-band frequencies do not support maximum TXP power of 20.
- Idle current measured with the xDot joined with Conduit, but idle without data transferring.
- Transmit power measured while transferring data packets using spread factor 9. Packet size limited to 53 bytes. The Conduit was set to receive packets from and send back to the xDot. A script was run to send the packet 100 times with either 10 or 53 bytes of data, with an average measurement taken during that time.
- For Inrush charge, recorded the highest observed value from five separate measurements.

Voltage USB = 5v	Standby Mode Current, (Sleep = 0 Deep Sleep)	Stop Mode Current, (Sleep = 1)	Idle current Average	Spreading Factor Setting	Packet Size (# Bytes)
LDO = 3.3	1.9uA	2.2uA	11.1mA	DR1 - SF9BW125	10
LDO = 3.3	1.9uA	2.2uA	11.1mA	DR1 - SF9BW125	53

Voltage USB = 5v	Average Current (Amps) at Low Transmit Power Setting (TXP 2)	Average Current (Amps) at Default Transmit Power Setting (TXP 11)	Average Current (Amps) at Maximum Transmit Power Setting (TXP 20)	Total Inrush Charge measured in MilliCoulombs	Total Inrush Charge DURATION during Powerup (INRUSH Duration)
LDO = 3.3	0.013	0.017	0.018	0.132mC	153uS
LDO = 3.3	0.017	0.024	0.025	0.132mC	147uS

Measuring the Power Draw

To measure the power draw on an xDot developer board:

1. Flash the latest AT command firmware on the xDot.
2. Unplug the xDot from the computer and then reconnect it.
3. Connect current meter across JP30 on the developer board.
4. Set wake pin to wake, **AT+WP=6**.
5. Set wake mode to interrupt, **AT+WM=1**.
6. Put the xDot to sleep, **AT+SLEEP=0|1**.
7. Put jumper across JP5.

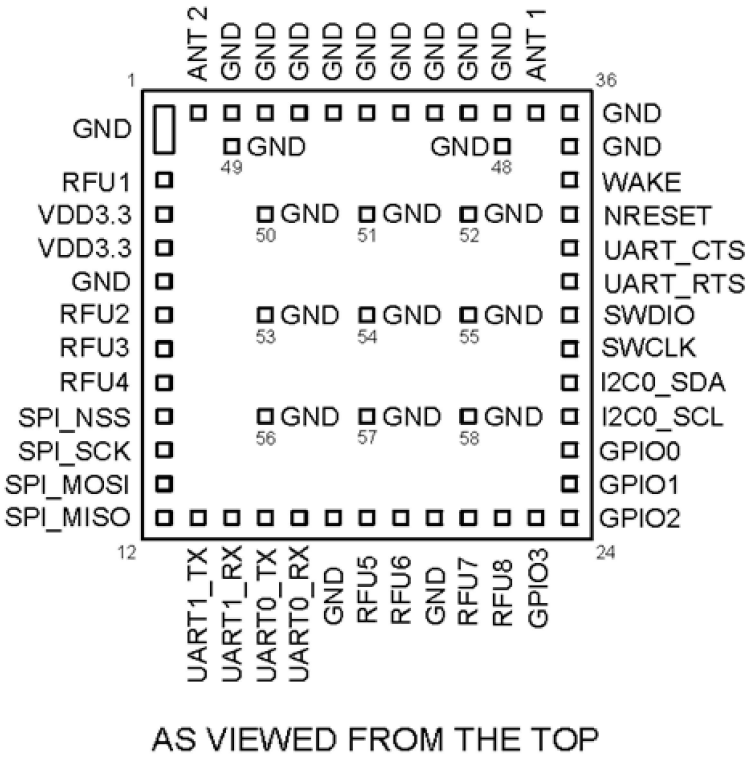
   Note: After this step, AT command and debug ports no longer work.

8. Measure current draw.
9. Press the **S2** button on the developer board to wake the xDot

Electrical Characteristics

Signal	Description	Min	Max
Vin Low	Input low level	--	0.3 * VDD
Vin High	Input high level	0.45 * VDD +0.6	--
Vout Low	Output low level	--	.4
Vout High	Output high level	0.4	--
VCC	Standard operating voltage	2.4	3.6
ICC	Operating current (mA) @5V	--	135
	Operating current (mA) @3.3V	--	200

xDot and Processor Pin Information



AS VIEWED FROM THE TOP

Pin Information

Note:

- Using the mbed platform expands your pin functionality options.
- Pins are on a 0.07 inch grid, and are 0.028 inches square (except for upper left)
- The xDot is 0.045 x 0.045, board is 0.93 x 0.93

48QFN	xDot Pin	Pin Name	SW Name	Function Description	Processor Pin Alt1	Processor Pin Alt2
25	9	PB12	SPI2_NSS	GPIO / SPI	TIM10_CH1/ I2C2_SMBA/ SPI2_NSS/ I2S2_WS/ USART3_CK/ LCD_SEG12	ADC_IN18/ COMP1_INP/ VLCDRAIL2
26	10	PB13	SPI2_SCK	GPIO / SPI	TIM9_CH1/ SPI2_SCK/ I2S2_CK/ USART3_CTS/ LCD_SEG13	ADC_IN19/ COMP1_INP
28	11	PB15	SPI2_MOSI	GPIO / SPI	TIM11_CH1/ SPI2_MOSI/ I2S2_SD/ LCD_SEG15	ADC_IN21/ COMP1_INP/ RTC_REFIN
27	12	PB14	SPI2_MISO	GPIO / SPI	TIM9_CH2/ SPI2_MISO/ USART3_RTS/ LCD_SEG14	ADC_IN20/ COMP1_INP
30	13	PA9	UART1_TX	GPIO / UART	USART1_TX/ LCD_COM1	-
31	14	PA10	UART1_RX	GPIO / UART	USART1_RX/ LCD_COM2	-
12	15	PA2	UART2_TX	Debug UART		
13	16	PA3	UART2_RX	Debug UART		
20	23	PB2	GPIO3	GPIO	BOOT1	VLCDRAIL1/ ADCIN0b
18	24	PB0	GPIO2	GPIO	TIM3_CH3/ LCD_SEG5	ADC_IN8/ COMP1_INP/ OPAMP2_VOUT/ VLCDRAIL3/ VREF_OUT
15	25	PA5	GPIO1	GPIO	TIM2_CH1_ETR/ SPI1_SCK	ADC_IN5/ DAC_OUT2/ COMP1_INP
14	26	PA4	GPIO0	GPIO	SPI1_NSS/ SPI3_NSS/ I2S3_WS/ USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
45	27	PB8	I2C1_SCL	GPIO / I2C	TIM4_CH3/ TIM10_CH1/ I2C1_SCL/ LCD_SEG16	-

48QFN	xDot Pin	Pin Name	SW Name	Function Description	Processor Pin Alt1	Processor Pin Alt2
46	28	PB9	I2C1_SDA	GPIO / I2C	TIM4_CH4/ TIM11_CH1/ I2C1_SDA/ LCD_COM3	-
37	29	PA14		MBED SWCLK	JTCK-SWCLK	-
34	30	PA13		MBED SWDIO	JTMS-SWDIO	-
33	31	PA12	UART1_RTS	GPIO / UART	USART1_RTS/ SPI1_MOSI	USB_DP
32	32	PA11	UART1_CTS	GPIO / UART	USART1_CTS/ SPI1_MISO	USB_DM
7	33	NRST		NRESET	-	-
10	34	PA0-WKUP1	WAKE	GPIO / WAKE	TIM2_CH1_ETR/ TIM5_CH1/ USART2_CTS	WKUP1/ RTC_TAMP2/ ADC_IN0/ COMP1_INP
	37			ANT1		
	47			RFU (ANT2)		
8,23,35 ,47,49	1, 5, 17, 20,35, 36, 38, 39, 40, 41, 42, 43, 44, 45, 46, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58	VSS		GND		
	2, 6, 7, 8, 18, 19, 21, 22			Reserved		
16		PA6	LORA_DIO0	LORA Radio		
17		PA7	LORA_DIO1	LORA Radio		
29		PA8	LORA_DIO2	LORA Radio		
42		PB6	LORA_DIO3	LORA Radio		
43		PB7	LORA_DIO4	LORA Radio		
40		PB4	LORA_MISO	LORA Radio		
41		PB5	LORA_MOSI	LORA Radio		

48QFN	xDot Pin	Pin Name	SW Name	Function Description	Processor Pin Alt1	Processor Pin Alt2
38		PA15	LORA_NSS	LORA Radio		
11		PA1	LORA_RESET	LORA Radio		
39		PB3	LORA_SCK	LORA Radio		
22		PB11	SE_CLK	Secure Element		
19		PB1	SE_CTRL	Secure Element		
21		PB10	SE_IO	Secure Element		
2		PC13-WKUP2	SE_RESET	Secure Element		
44		BOOT0		Boot0	-	-
3		PC14-OSC32_IN(4)		RTC_CLK	-	OSC32_IN
4		PC15-OSC32_OUT		RTC_CLK	-	OSC32_OUT
5		PH0-OSC_IN(5)		Main 24M	-	OSC_IN
6		PH1-OSC_OUT(5)		Main 24M	-	OSC_OUT

Pull-Up/Down

48QFN	xDot Pin	Pin Name	SW Name	PU/PD
7	33	NRST		10k PU
38		PA15	LORA_NSS	100k PU
19		PB1	SE_CTRL	10k PU
44		BOOT0		10k PD

xDot Pinout Design Notes

Refer to the mechanical drawing for your model for pin locations.

- All pins that go to connectors are directly connected to the processor.
- Refer to Pin Information table for pull up and pull down information.

xDots allow you to program pins depending on your application:

- **Serial:** Available out of the box. See Serial Pinout Notes for details.
- **mbed:** Designed with the STM32L151CCU6 48-pin processor, this option provides the most flexibility. For more information about processor capabilities, see the processor datasheet.

Serial Pinout Notes

Out of the box, these pins are available for serial applications. Refer to the mechanical drawing for your model for pin locations.

- 18 PTA1 UART1_CTS
- 19 PTA2 UART1_RTS
- 36 PTC3 UART1_RX
- 37 PTC4 UART1_TX

Serial Settings

When creating a serial connection with the device on the developer board, open communications software (such as TeraTerm, Putty, or Minicom), and use the following settings:

- Baud rate = 115,200
- Data bits = 8
- Parity = N
- Stop bits = 1
- Flow control = Off

LoRa

Throughput Rates

Theoretical maximum speeds for LoRa mode with ACKs off are:

- Using spreading factor 7 at 125kHz, the throughput rate is 5470 bps (5.47 kbps).
- Using spreading factor 7 at 500kHz the receiving throughput rate is 21900 bps (21.9 kbps).

Note: Data rates in the LoRaWAN specification vary by geographic region.

Range

Variables effecting the range include TX power, antenna gain, RX sensitivity, fade margin, earth's curvature. Use the following formula to calculate the maximum range:

$$Range_{Miles} = 10^{\left(\frac{TxPower + Antenna\ gain\ total - RX\ Sensitivity - Fade\ Margin - 36.56}{20} - LOG_{10}(F_{MHz})\right.}$$

The following table provides example settings and the theoretical maximum range based on these settings.

Example	18dB Transmit Power for 915 MHz Models	Units	Example 14dB Transmit Power for 868MHz Models
Frequency	915	MHz	868
TX Power	19	dBm	14
TX Antenna Gain	3	dB	3
RX Sensitivity[1]	-120	dBm	-120
RX Antenna Gain	3	dB	3
Fade Margin[2]	30	dB	30
Distance	8.14	Miles	5.41
Distance	13.08	Km	8.70

[1]RX Sensitivity is set to a conservative -120dBm, but can vary from -117 to -137dBm.

[2]Fade Margin is set at the worst case of 30dB. Fade margin is an allowance a system designer includes to account for unknown variables. The higher the fade margin, the better the overall link quality will be. With a fade margin set to zero, the link budget is still valid, but only in LOS conditions, which is not practical for most designs. The amount of fade margin to include in a calculation depends on the environment in which you will deploy the system. A fade margin of 12 dBm is good, but a better number would be 20 to 30 dBm.

Chapter 5 Antennas

Antenna System

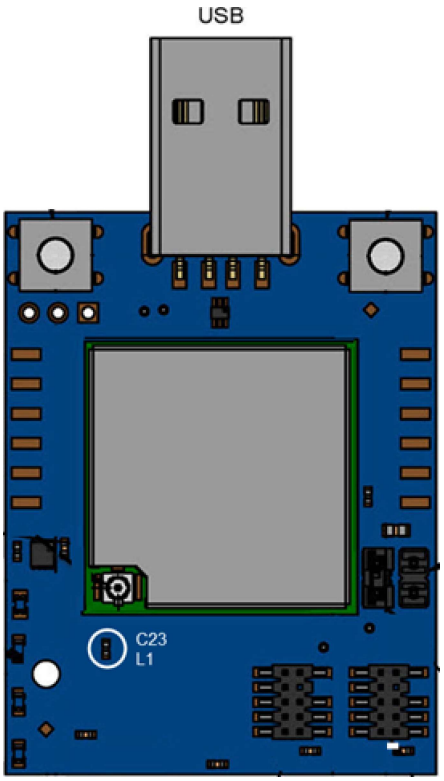
The LoRa antenna performance depends on the implementation and antenna design. The integration of the antenna system into the product is a critical part of the design process; therefore, it is essential to consider it early so the performance is not compromised. If changes are made to the device's certified antenna system, then recertification will be required.

This radio transmitter has been tested with both the Pulse and Ethertronics antennas listed below. If you follow our design guidelines, you do not need to re-certify your design. The antenna you use must maintain the same specifications. It must be of the same type, with similar in-band and out-of-band radiation patterns. Antennas having a greater gain than the maximum gain indicated for the listed type, are strictly prohibited for use with this device.

U.FL and Trace Antenna Options

If using U.FL or trace antennas, note the following:

- **For a simple trace to RF antennas:** Routing must follow standard RF design rules and practices for stripline/miscrostrip for a 50 ohm impedance line. Use the developer board schematics for a reference circuit for the a trace antenna.
- **For U.FL antennas:** The antenna and cable combination in your design cannot exceed the performance of the SMA antenna as listed in the next topic.
- The xDot Developer Board includes an Ethertronics M620710-1K chip antenna, which by default connects the xDot to the chip antenna. Only one antenna, either U.FL or chip, may be used at a time. To use the xDot’s U.FL connector, remove resistor C23 and L1, marked on the following image, to disconnect the chip antenna.



Pulse Electronics Antenna

Manufacturer:	Pulse Electronics
Description:	868-915 MHz RP-SMA Antenna, 8"
Model Number:	W1063
MultiTech Part Number:	45009830L

MultiTech ordering information:

Ordering Part Number	Quantity
AN868-915A-1HRA	1
AN868-915A-10HRA	10
AN868-915A-50HRA	50

Antenna Specifications

Category	Description
Frequency Range	868-928 MHz
Impedance	50 Ohms
VSWR	≤ 2.0
Gain	3.0 dBi
Radiation	Omni

Category	Description
Polarization	Vertical

RSMA-to-U.FL Coaxial Cables

Coaxial Cable Specifications

Optional antenna cables can be ordered from MultiTech

Cable Type	Coaxial Cable
Attenuation	<1.0db
Connector Impedance	50 ohm
Maximum Cable Length	16" (40 cm)

Ordering Information

Part Number	Description
CARSMA-UFL-1	RSMA-to-UFL Coax Cable (Single Pack)
CARSMA-UFL-10	RSMA-to-UFL Coax Cable (Ten Pack)
CARSMA-UFL-100	RSMA-to-UFL Coax Cable (One Hundred Pack)

Ethertronics Chip Antenna

This is the developer board's default antenna.

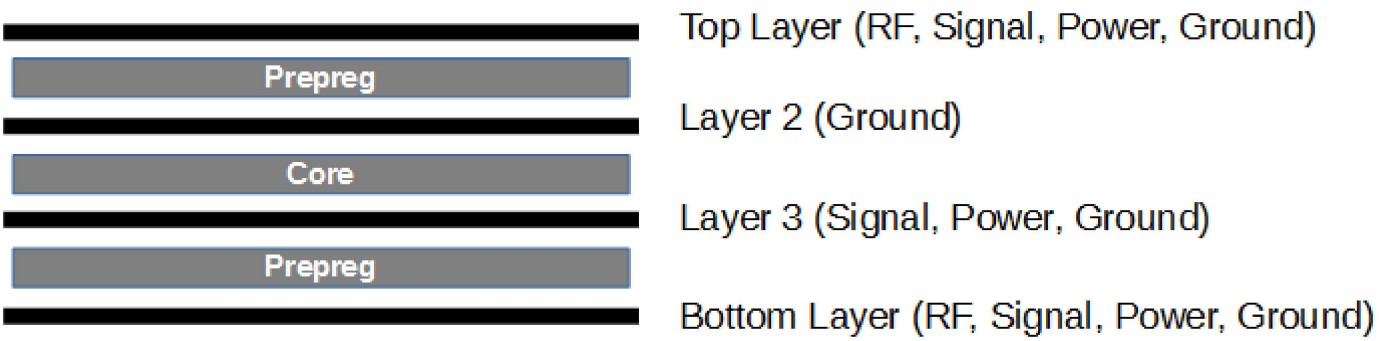
Manufacturer:	Ethertronics
Description:	915MHz Chip RF Antenna 902MHz ~ 928MHz 2.56dB Solder Surface Mount
Model Number:	M620710-1K
Datasheet:	http://www.ethertronics.com/files/2914/0652/9246/2-Savvi_M620710_ISM__6x2.pdf

Antenna Specifications

Category	Description
Electrical Specifications	
Frequency Range	902—928 MHz
Peak Gain	2.56 dBi
VSWR	2:6:1 max
Impedance	50 ohms unbalanced
Average Efficiency	58%
Power Handling	0.5 Watt cw
Polarization	Linear
Mechanical Specifications	
Mounting	Surface Mount
Size	6.00 x 2.00 x 1.1mm

Stackup Information

Developer Board Layer Stackup



Stackup Table

Part Number: 10000952L
PDF Date: Friday, August 12, 2016 01:42:30 PM

MULTITECH

Stackup S02

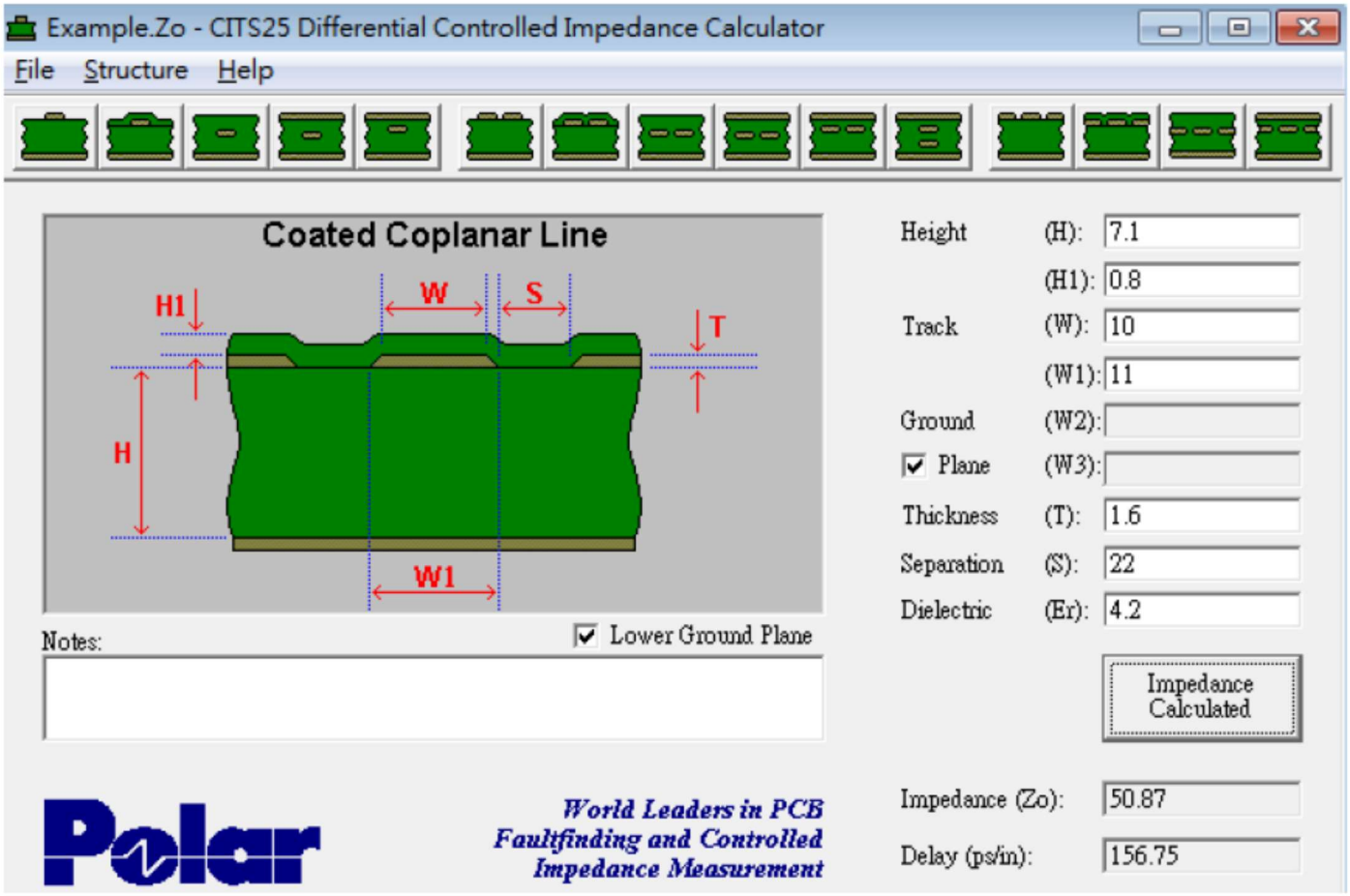
PCB Fabricator: APCB-Taiwan
Soldermask Type: DSR-220TL 06BL (Blue)
Surface Finish: High Temp. OSP
Stackup Notes: White Silkscreen Blue Soldermask

Created/Modified: 07-10-2012 / 12-31-2015
Measured Thickness:

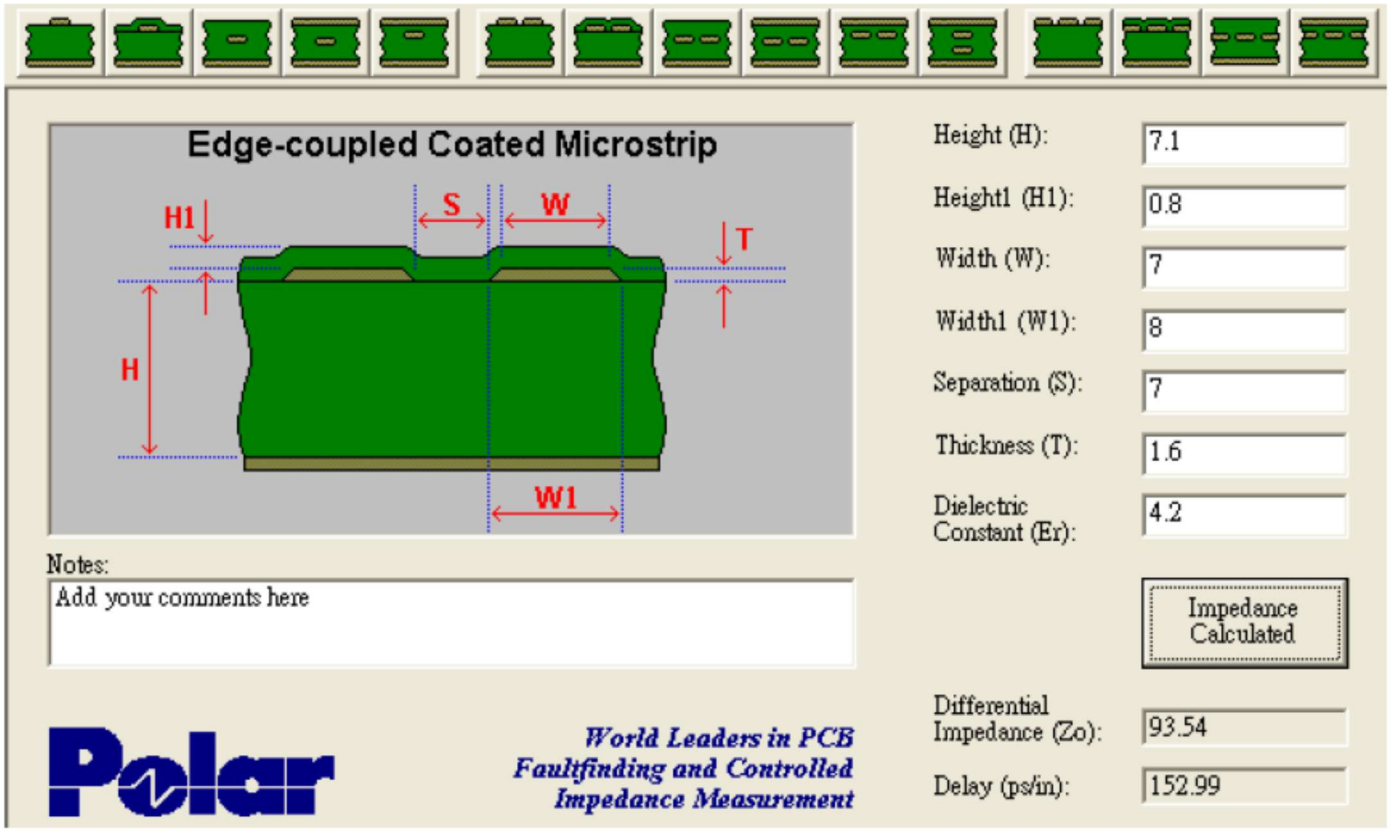
Layer	Layer Type	Construction	Dk	T (mils)	W (mils)	D (mils)	Z_o (ohms)	Z_{min}/Z_{max} (ohms)	Z_{diff} (ohms)
1	Signal	0.5 oz. Copper	—	1.6/–	11/– 8/–	22/– 7/–	50±10%/–	45/55	90±10%/–
.	Prepreg (TU-72P-1MHz)	7628 (43%)	4.2	7.1	—	—	—	—	—
2	Plane	1 oz. Copper	—	1.4/–	—	—	—	—	—
.	Core (TU-722-1MHz)	5x7628	4.63	39	—	—	—	—	—
3	Signal	1 oz. Copper	—	1.4/–					
.	Prepreg (TU-72P-1MHz)	7628 (43%)	4.2	7.1	—	—	—	—	—
4	Signal	0.5 oz. Copper	—	1.6/–	8/–	7/–			90±10%/–

Impedance

Polar trial balance (L1 refer to L2) impedance 50.87 ohms, using 11 mil tracs, 22mil space.



Polar trial balance (L1 refer to L2/L4 refer to L3) impedance 93.54 ohms, using 8 mil tracs, 7mil space.



Chip Antenna Design Guidelines

When designing antenna placement for the chip antenna, note the following:

- The antenna's long side must be along the edge of the ground plane.
- Remove the ground plane from all layers below the antenna.
- The distance from the antenna to the enclosure or plastic cover should be greater than 1.5 mm.

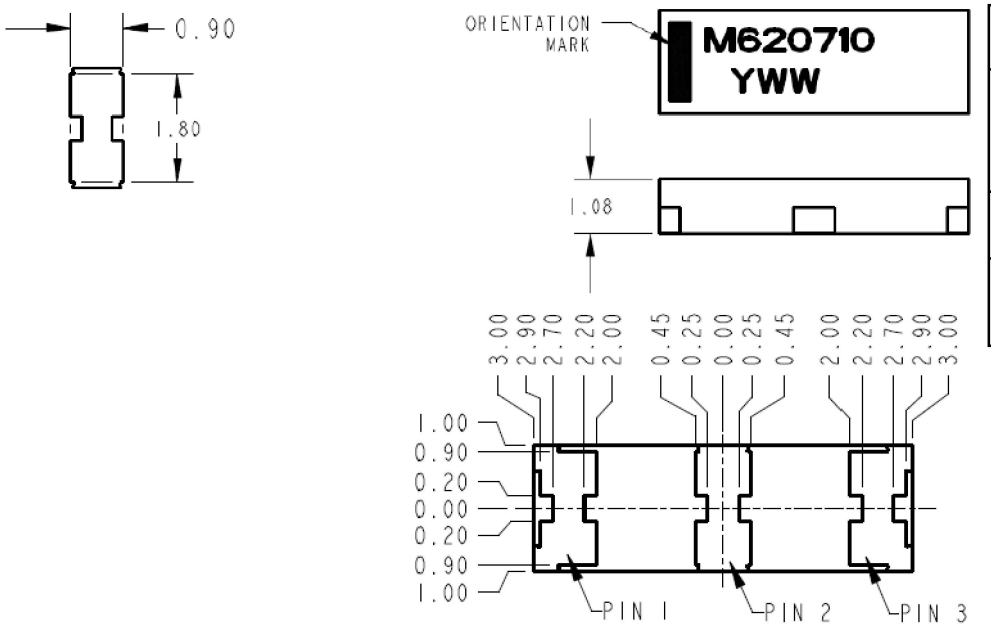
The distance from the antenna to relatively large perturbations, such as a shield or large components, depends on the height of surrounding components. It should not be less than 1.5mm.

We recommend a distance equal to or greater than 10mm from the end of the antenna to either end of the PCB distance. Performance is better from larger distances.

Use the recommended land pattern shown in the figures below. Land patterns are composed of a 50 ohm line connected to each antenna feed point. Ground clearance around and under the antenna as shown in the PCB layout is recommended to maximize antenna performance.

Antenna Pad Layout

Antenna Pad Layout



Pin	Description
1	ISM Feed/ Minor Matching Circuit Connection
2	Dummy Pad
3	Matching Circuit Connection

PCB Layout

PCB Layout