Micro Developer Board LEDs

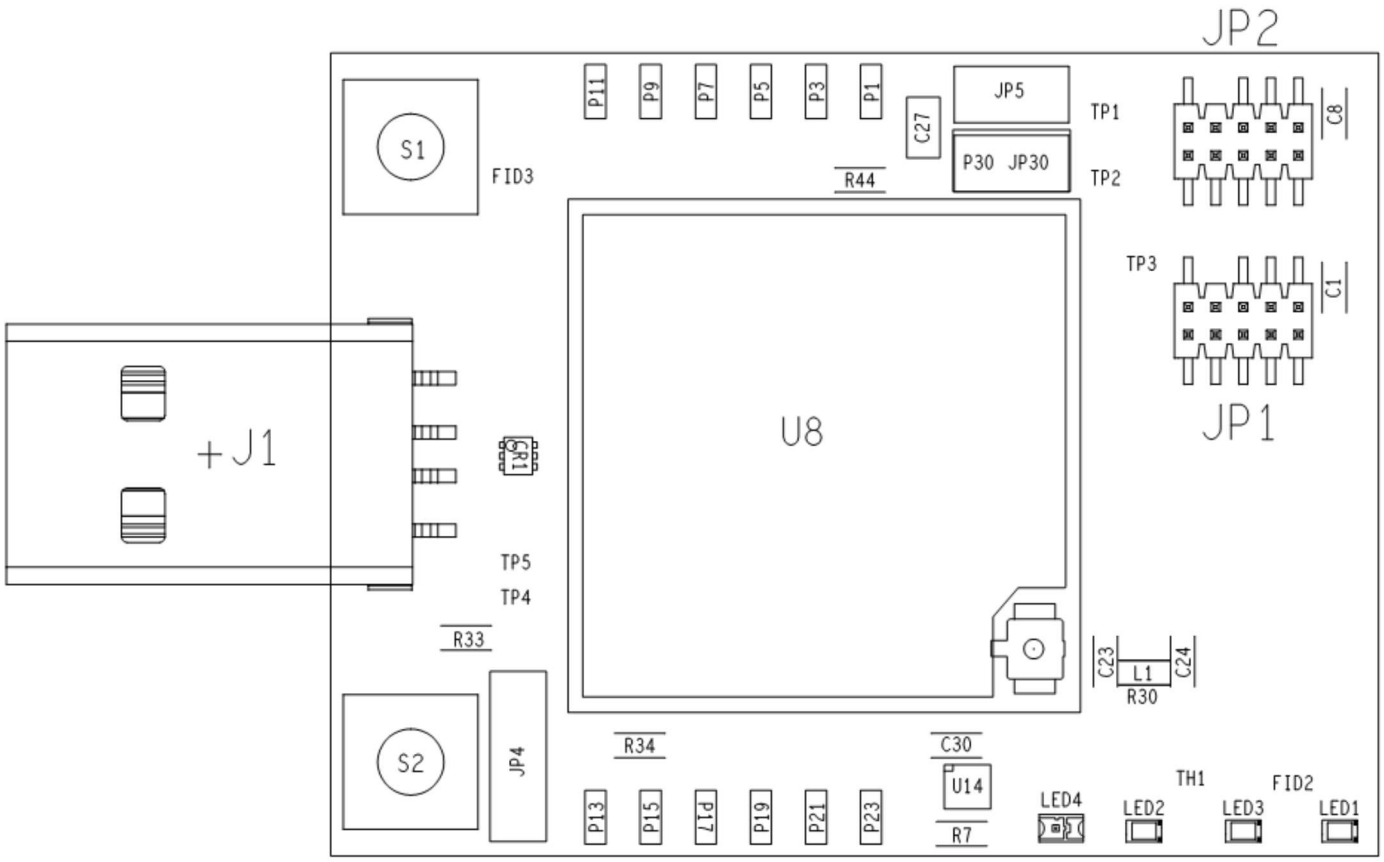
LED	Description
LED1	User-definable LED.
LED3/SDA	Programming Status.
LED2/PWR	Power, blue light when the board has power.
LED4/PROXY	LED for the proximity sensor, which is next to it (labeled U14 on the top assembly diagram).

Chapter 11 Developer Board Schematics

Assembly Diagrams and Schematics

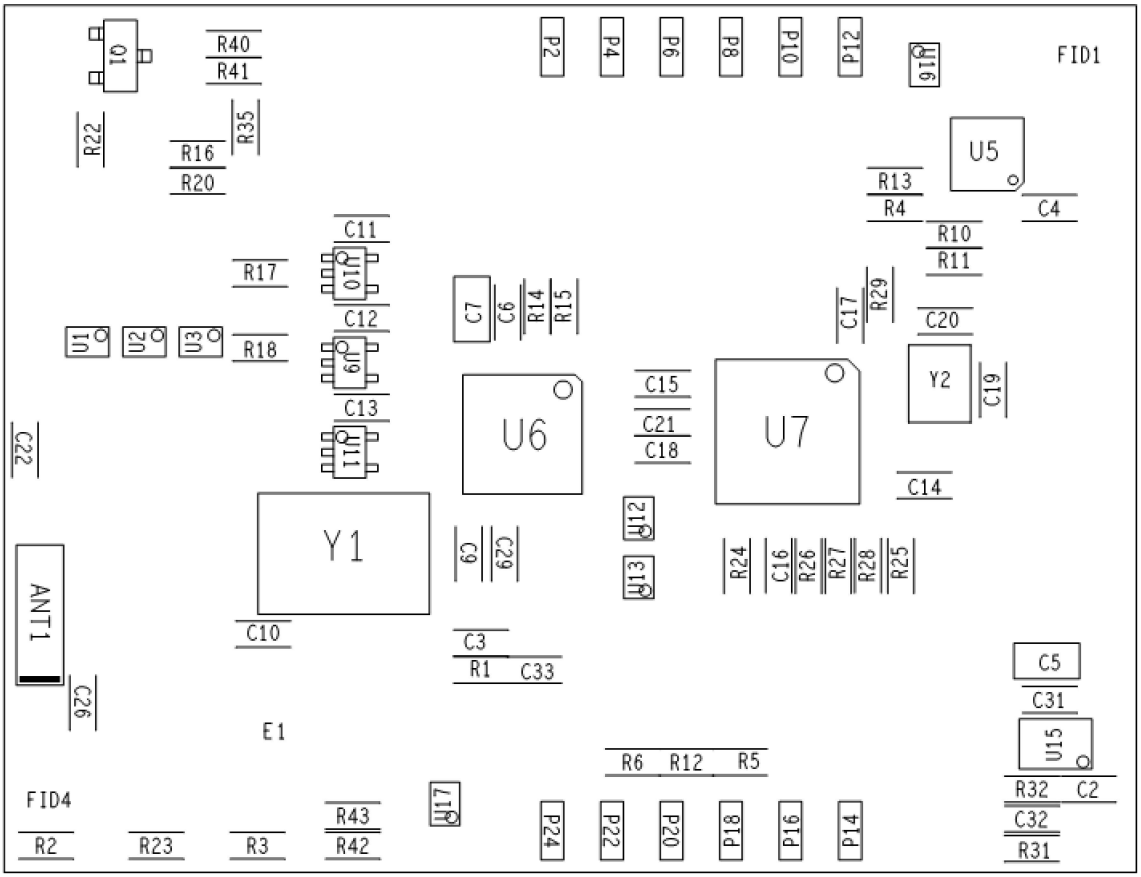
Assembly Diagrams

Top

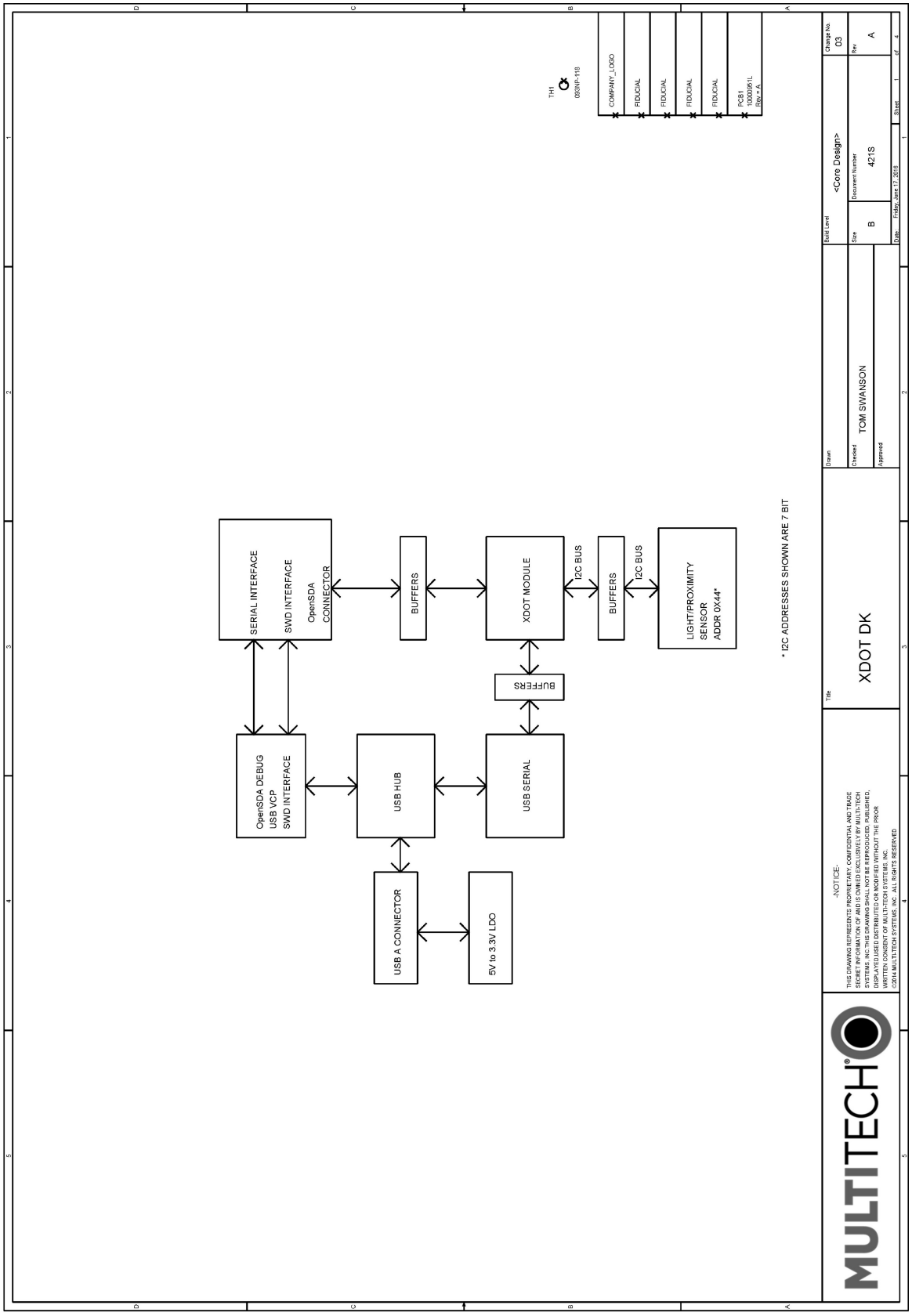


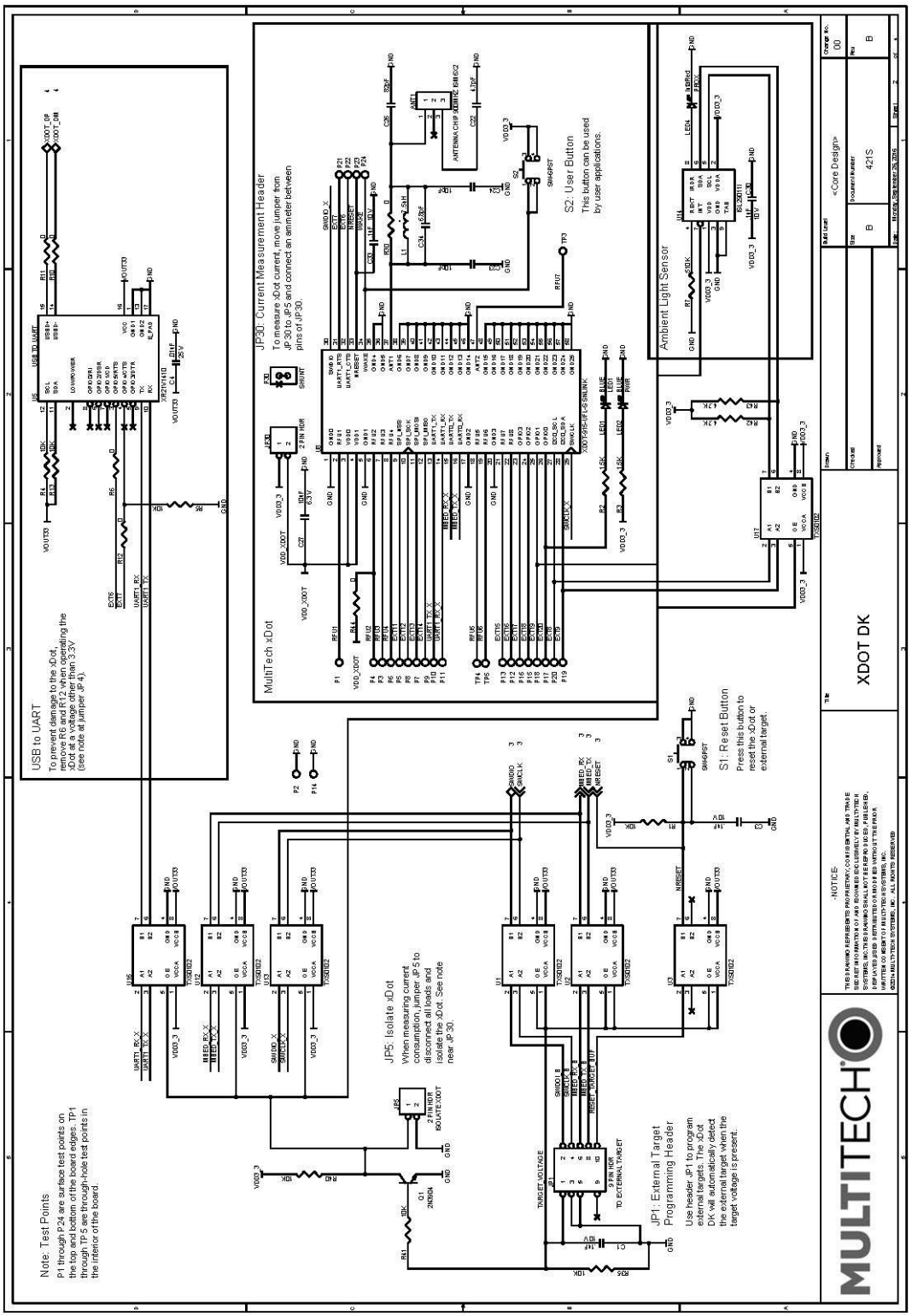
R30 SITS ON L1
C34 SITS ON L1

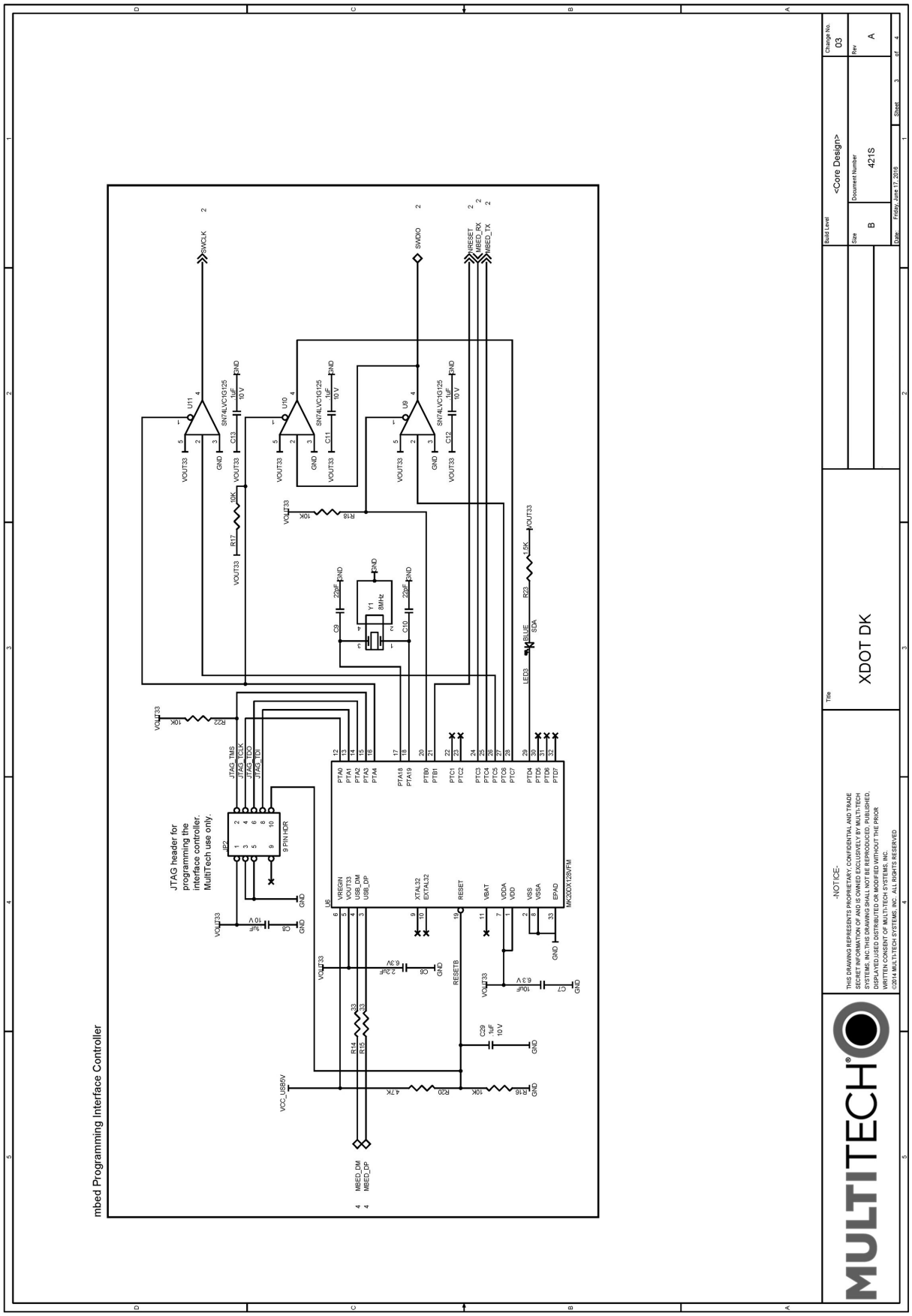
Bottom


J1
R40
R41
R22
R35
R16
R20
P2
P4
P6
P8
P10
P12
J16
FID1
U5
R13
R4
C4
R10
R11
C11
J10
R17
C12
C7
C6
R14
R15
C17
R29
C20
U1
U2
U3
R18
J9
C13
U6
C15
C21
C18
U7
Y2
C19
C22
J11
C14
Y1
J12
J13
C9
C29
R24
C16
R26
R27
R28
R25
ANT1
C10
C3
R1
C33
C5
C31
C26
E1
U15
R6
R12
R5
FID4
J17
R32
C2
C32
R43
R2
R23
R3
R42
P24
P22
P20
P18
P16
P14
R31

Schematics


SERIAL INTERFACE
SWD INTERFACE
OpenSDA CONNECTOR
BUFFERS
XDOT MODULE
I2C BUS
BUFFERS
I2C BUS
LIGHT/PROXIMITY SENSOR ADDR 0X44*
BUFFERS
OpenSDA DEBUG
USB VCP
SWD INTERFACE
USB HUB
USB SERIAL
USB A CONNECTOR
5V to 3.3V LDO
* I2C ADDRESSES SHOWN ARE 7 BIT
COMPANY_LOGO
FIDUCIAL
FIDUCIAL
FIDUCIAL
FIDUCIAL
PCB1
TH1
093NP-118
MULTITECH
XDOT DK
TOM SWANSON
<Core Design>
421S
Change No. 03
Rev A
Size B
Friday, June 17, 2016
Sheet 1 of 4


USB to UART
To prevent damage to the xDot, remove R5 and R12 when operating the xDot at voltages other than 3.3V (see note at jumper JP 4).
JP30: Current Measurement Header
To measure xDot current, move jumper from JP 30 to JP5 and connect an ammeter between pins of JP30.
MultiTech xDot
S2: User Button
This button can be used by user applications.
Ambient Light Sensor
S1: Reset Button
Press this button to reset the xDot or external target.
JP5: Isolate xDot
When measuring current consumption, jumper JP 5 to disconnect all loads and isolate the xDot. See note near JP 30.
JP1: External Target Programming Header
Use header JP1 to program external targets. The xDot DK will automatically detect the external target when the target voltage is present.
Note: Test Points
P1 through P24 are surface test points on the top and bottom of the board edges. TP1 through TP 5 are through-hole test points in the interior of the board.
XDOT DK
MULTITECH


mbed Programming Interface Controller
JTAG header for programming the interface controller. MultiTech use only.
XDOT DK
<Core Design>
MULTITECH
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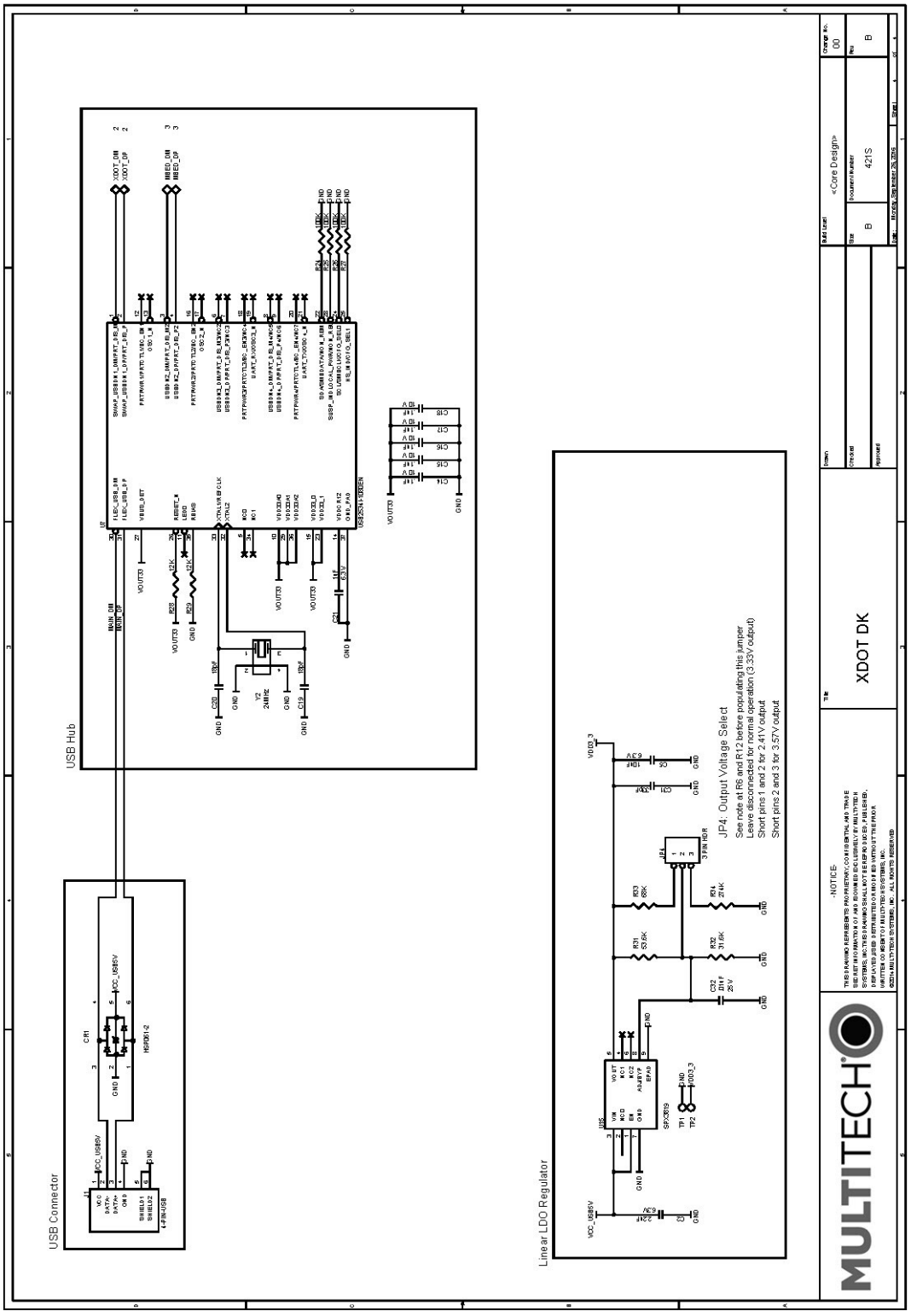

USB Hub
USB Connector
Linear LDO Regulator
JP4: Output Voltage Select
See note at R6 and R12 before populating this jumper
Leave disconnected for normal operation (3.33V output)
Short pins 1 and 2 for 2.41V output
Short pins 2 and 3 for 3.57V output
XDOT DK
«Core Design»
421S
MULTITECH

Chapter 12 Design Considerations

Noise Suppression Design

Adhere to engineering noise-suppression practices when designing a printed circuit board (PCB). Noise suppression is essential to the proper operation and performance of the modem and surrounding equipment.

Any OEM board design must consider both on-board and off-board generated noise that can affect digital signal processing. Both on-board and off-board generated noise that is coupled on-board can affect interface signal levels and quality. Noise in frequency ranges that affect modem performance is of particular concern.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is equally important. This type of noise can affect the operation of surrounding equipment. Most local government agencies have certification requirements that must be met for use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, and so on) component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

Other aspects of proper noise-suppression engineering practices are beyond the scope of this guide. Consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes.

PC Board Layout Guideline

In a 4-layer design, provide adequate ground plane covering the entire board. In 4-layer designs, power and ground are typically on the inner layers. Ensure that all power and ground traces are 0.05 inches wide.

The recommended hole size for the device pins is 0.036 in. +/-0.003 in. in diameter. Use spacers to hold the device vertically in place during the wave solder process.

Electromagnetic Interference

The following guidelines are offered specifically to help minimize EMI generation. Some of these guidelines are the same as, or similar to, the general guidelines. To minimize the contribution of device-based design to EMI, you must understand the major sources of EMI and how to reduce them to acceptable levels.

- Keep traces carrying high frequency signals as short as possible.
- Provide a good ground plane or grid. In some cases, a multilayer board may be required with full layers for ground and power distribution.
- Decouple power from ground with decoupling capacitors as close to the device's power pins as possible.
- Eliminate ground loops, which are unexpected current return paths to the power source and ground.
- Decouple the telephone line cables at the telephone line jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines; however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
- Decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.

- Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
- Locate cables and connectors to avoid coupling from high frequency circuits.
- Lay out the highest frequency signal traces next to the ground grid.
- If using a multilayer board design, make no cuts in the ground or power planes and be sure the ground plane covers all traces.
- Minimize the number of through-hole connections on traces carrying high frequency signals.
- Avoid right angle turns on high frequency traces. Forty-five degree corners are good; however, radius turns are better.
- On 2-layer boards with no ground grid, provide a shadow ground trace on the opposite side of the board to traces carrying high frequency signals. This will be effective as a high frequency ground return if it is three times the width of the signal traces.
- Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.

Electrostatic Discharge Control

Handle all electronic devices with precautions to avoid damage due to the static charge accumulation.

See the ANSI/ESD Association Standard (ANSI/ESD S20.20-1999) – a document “for the Development of an Electrostatic Discharge Control for Protection of Electrical and Electronic Parts, Assemblies and Equipment.” This document covers ESD Control Program Administrative Requirements, ESD Training, ESD Control Program Plan Technical Requirements (grounding/bonding systems, personnel grooming, protected areas, packaging, marking, equipment, and handling), and Sensitivity Testing.

MultiTech strives to follow these recommendations. Input protection circuitry is incorporated in MultiTech devices to minimize the effect of static buildup. Take precautions to avoid exposure to electrostatic discharge during handling.

MultiTech uses and recommends that others use anti-static boxes that create a faraday cage (packaging designed to exclude electromagnetic fields). MultiTech recommends that you use our packaging when returning a product and when you ship your products to your customers.

Chapter 13 Mounting xDots and Programming External Targets

Mounting the Device on Your Board

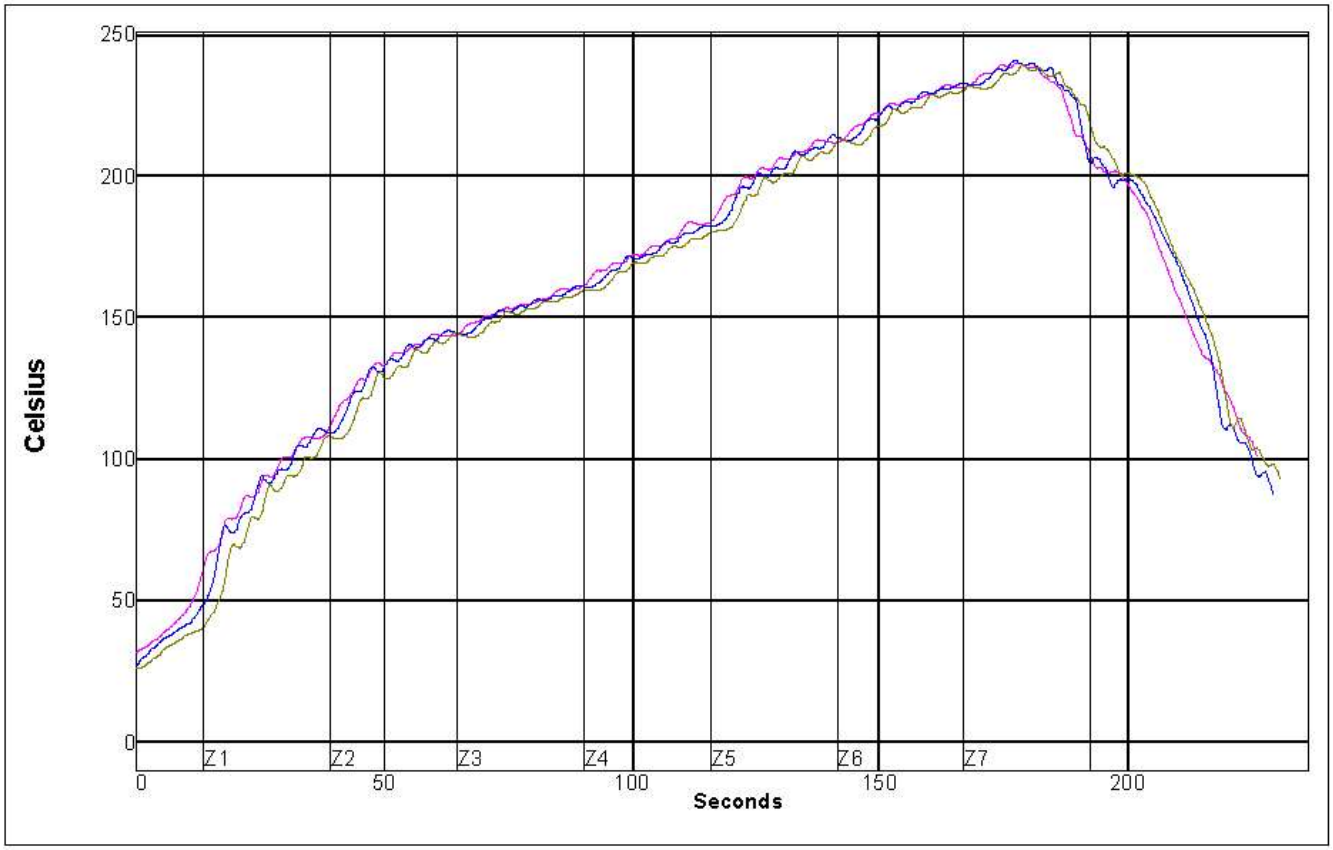
A footprint diagram is included on the xDot Mechanical Diagram.

Solder Profile

Solder Paste: SAC NC 254

Note: Calculate slope over 120 seconds

Name	Low Limit	High Limit	Units
Max Rising Slope (Target=1.0)	0	2	Degrees/Second
Max Falling Slope	-2	-0.1	Degrees/Second
Soak Time 150-170C	15	45	Seconds
Peak Temperature	235	250	Degrees Celsius
Total Time Above 218C	30	90	Seconds



Setpoints (Celsius)

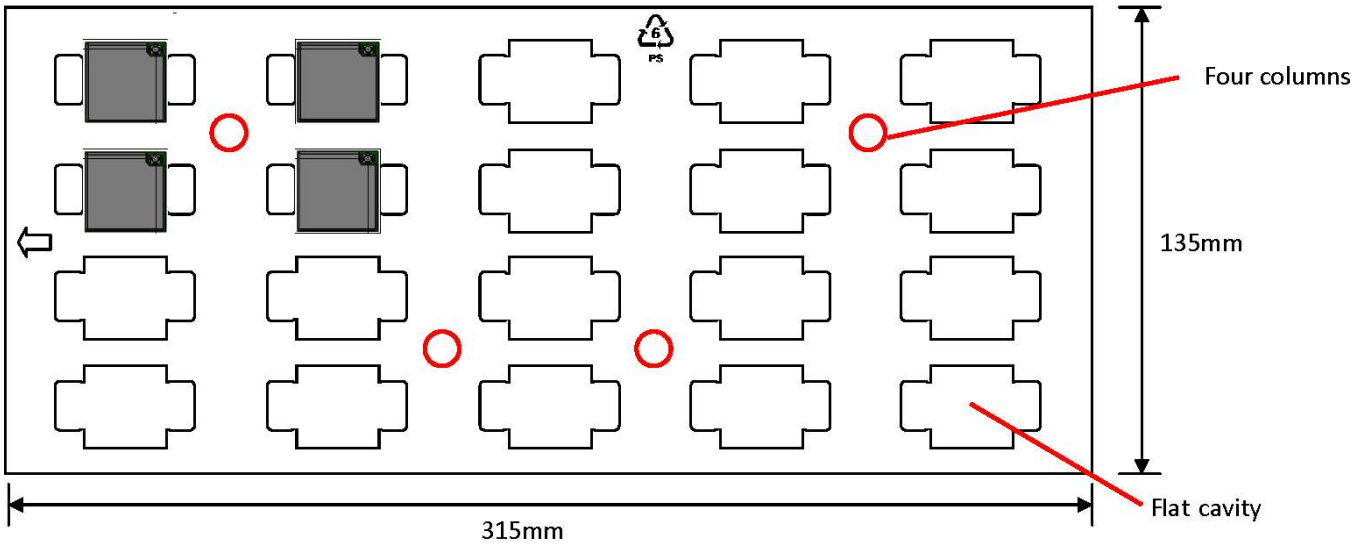
Zone	1	2	3	4	5	6	7
Top	130	160	170	190	230	245	255
Bottom	130	160	170	190	230	245	255
Conveyer Speed		32.0 inch/minute					

		Max Rising Slope		Max Falling Slope		Soak Time 150-170C		Peak Temp		Total Time /218C	
TC	Position	Slope	PWI	Slope	PWI	Time	PWI	Temp	PWI	Time	PWI
1	<TC2>	1.38	38%	-0.63	45%	28.82	-8%	240.22	-30%	43.61	-55%
2	<TC3>	1.38	38%	-0.75	32%	26.75	-22%	241.21	-17%	43.66	-54%
3	<TC4>	1.38	38%	-0.70	36%	29.47	-4%	239.56	-39%	43.29	-56%
Delta		0.00		0.12		2.72		1.65		0.37	

xDot Packing

xDots ship on 20 piece trays, which you can use for pick and place handling.

Warning: Maximum temperature for these trays is 65° C.

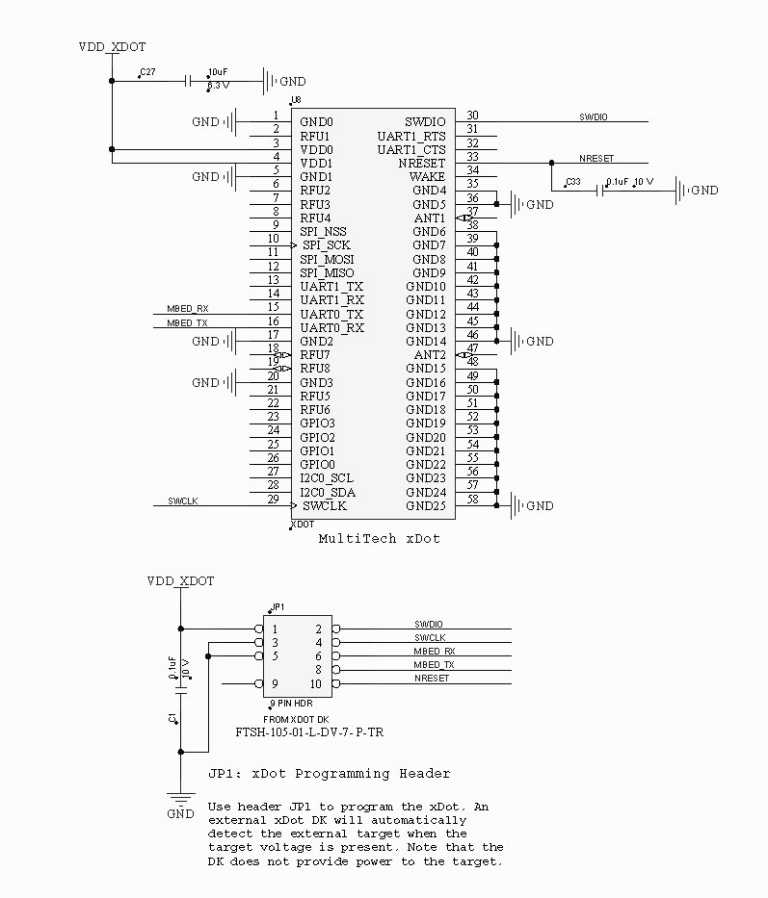


Programming External Targets

You can use the xDot developer board to program external targets. To do this:

1. Connect header JP1 to your target board with a 9-position ribbon cable.[1]
2. Apply power to your target board.

3. When the xDot developer board detects a target voltage on Pin 1 of header JP1, it redirects the mbed programming interface to the external target. You can use the mbed programming environment as normal to program and debug the external target.



[1]MultiTech recommends the Samtec FFSD-05-D-06.00-01-N ribbon cable.

JTAG/SWD Connector

The developer board uses an unshrouded 10-pin header.

Suitable connector headers include:

- Harwin: M50-3500542
- Mouser: 855-M50-3500542
- Samtec shrouded header: FTSH-105-01-F-D-K

The Samtec FTSH-105 header dimensions are 0.25"x 0.188" (6.35mm x 4.78mm).

Ensure that you connect your cable correctly, typically by matching the "1" marked on the board to the cable's red stripe.

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