

Data Sheet: JN5142

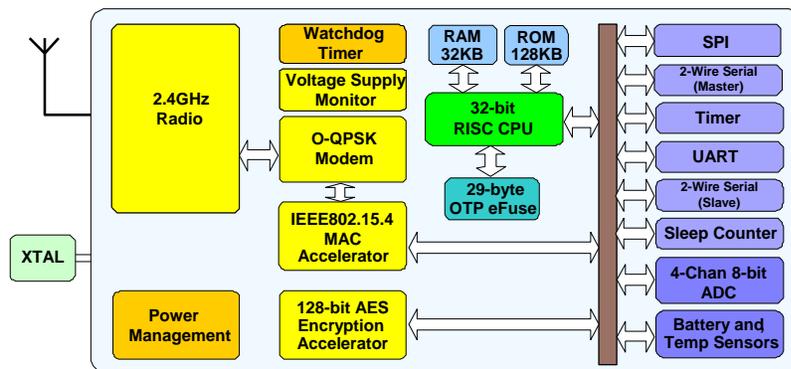
IEEE802.15.4 Wireless Microcontroller

Overview

The JN5142 is an ultra low power, high performance wireless microcontroller suitable for Remote Control, IEEE802.15.4 and Active RFID applications. There is also a ROM variant that supports JenNet-IP Smart Devices. The JN5142 features an enhanced 32-bit RISC processor offering high coding efficiency through variable width instructions, a multi-stage instruction pipeline and low power operation with programmable clock speeds. It also includes a 2.4GHz IEEE802.15.4 compliant transceiver, 128KB of ROM, 32KB of RAM, and a comprehensive mix of analogue and digital peripherals. The operating current is below 18mA, allowing operation direct from a coin cell.

The peripherals support a wide range of applications. They include a 2-wire serial interface, which operates as either master or slave, a two channel ADC with battery and temperature sensors. A large switch matrix of up to 81 elements can be supported for remote control applications. The best in class radio current and a 0.5µA sleep timer give excellent battery life.

Block Diagram



Benefits

- Single chip optimized for simple applications
- Very low current solution for long battery life – over 10 yrs
- RF4CE in ROM
- Variant for JenNet-IP Smart Devices
- Highly featured 32-bit RISC CPU for high performance and low power
- System BOM is low in component count and cost
- Flexible sensor interfacing options

Applications

- Robust and secure low power wireless applications using RF4CE
- Remote Control
- Toys and gaming peripherals
- Active RFID tags
- Point-to-point or star networks using IEEE802.15.4
- Energy harvesting, for example self powered light switch
- Smart Lighting Networks
- Building Automation

Features: Transceiver

- 2.4GHz IEEE802.15.4 compliant
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- Integrated ultra low power sleep oscillator – 0.5µA
- 2.0V to 3.6V battery operation
- Deep sleep current 0.12µA (Wake-up from IO)
- 0.5µA sleep with timer (1.5µA with RAM held)
- <\$0.50 external component cost
- Rx current 16.5mA
- Tx current 14.8mA
- Receiver sensitivity -95dBm
- Transmit power 2.5dBm

Features: Microcontroller

- 32-bit RISC CPU, 1 to 32MHz clock speed
- Low power operation
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- 128KB ROM and 32KB RAM for bootloaded program code
- RF4CE or JenNet-IP software in ROM
- Master/Slave I2C interface.
- 3xPWM and Application timer/counter
- UART
- SPI port with 3 selects
- Supply Voltage Monitor with 8 programmable thresholds
- 2- to 4-input 8-bit ADC, comparator
- Battery and temperature sensors
- Watchdog timer and Power-on-Reset (with brown-out) circuit
- Up to 18 DIO

Industrial temp -40°C to +125°C
6x6mm 40-lead Punched QFN
 Lead-free and RoHS compliant

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1 Introduction

The JN5142 is an IEEE802.15.4 wireless microcontroller that provides a fully integrated solution for applications using the IEEE802.15.4 standard in the 2.4 - 2.5GHz ISM frequency band [1], including RF4CE. A ROM variant provides support for JenNet-IP “Smart Device” applications such as lighting and building automation.

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimise this complexity, NXP provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN5142. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, it is not necessary to provide the register details of the JN5142 in the datasheet.

The device includes a Wireless Transceiver, RISC CPU, on chip memory and an extensive range of peripherals.

1.1 Wireless Transceiver

The Wireless Transceiver comprises a 2.45GHz radio, a modem, a baseband controller and a security coprocessor. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realised very easily. Appendix B.4, describes a complete reference design including Printed Circuit Board (PCB) design and Bill Of Materials (BOM).

The security coprocessor provides hardware-based 128-bit AES-CCM* modes as specified by the IEEE802.15.4 2006 standard. Specifically this includes encryption and authentication covered by the MIC –32/-64/-128, ENC and ENC-MIC –32/-64/-128 modes of operation.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 (2006) MAC and PHY functionality under the control of a protocol stack. Applications incorporating IEEE802.15.4 functionality can be developed rapidly by combining user-developed application software with a protocol stack library.

1.2 RISC CPU and Memory

A 32-bit RISC CPU allows software to be run on-chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN5142 has a unified memory architecture, code memory, data memory, peripheral devices and I/O ports are organised within the same linear address space. The device contains 128kbytes of ROM, 32kbytes of RAM and a 29-byte One Time Programmable (OTP) eFuse memory.

1.3 Peripherals

The following peripherals are available on chip:

- Master SPI port with three select outputs
- UART with support for hardware or software flow control
- One programmable Timer/Counter which supports Pulse Width Modulation (PWM) and capture/compare, plus three PWM timers which support PWM and Timer modes only.
- Two programmable Sleep Timers and a Tick Timer
- Two-wire serial interface (compatible with SMBus and I²C) supporting master and slave operation
- Eighteen digital I/O lines (multiplexed with peripherals such as timers and UARTs)
- 8-bit, Analogue to Digital converter with up to four input channels
- Programmable analogue comparator
- Internal temperature sensor and battery monitor
- Two low power pulse counters
- Random number generator
- Watchdog Timer and Supply Voltage Monitor
- JTAG hardware debug port

User applications access the peripherals using the Integrated Peripherals API. This allows applications to use a tested and easily understood view of the peripherals allowing rapid system development.

1.4 Block Diagram

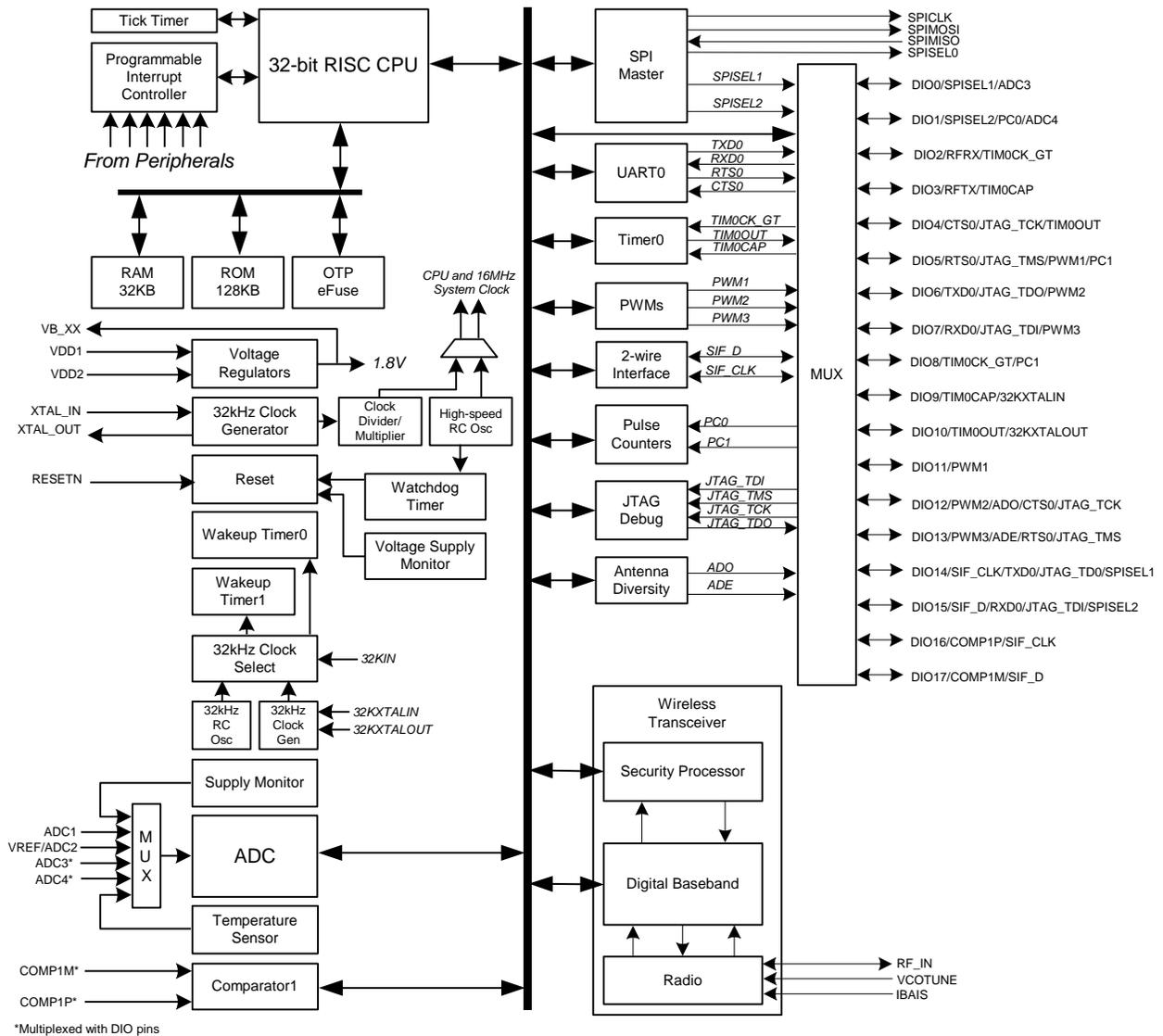


Figure 1: JN5142 Block Diagram

2 Pin Configurations

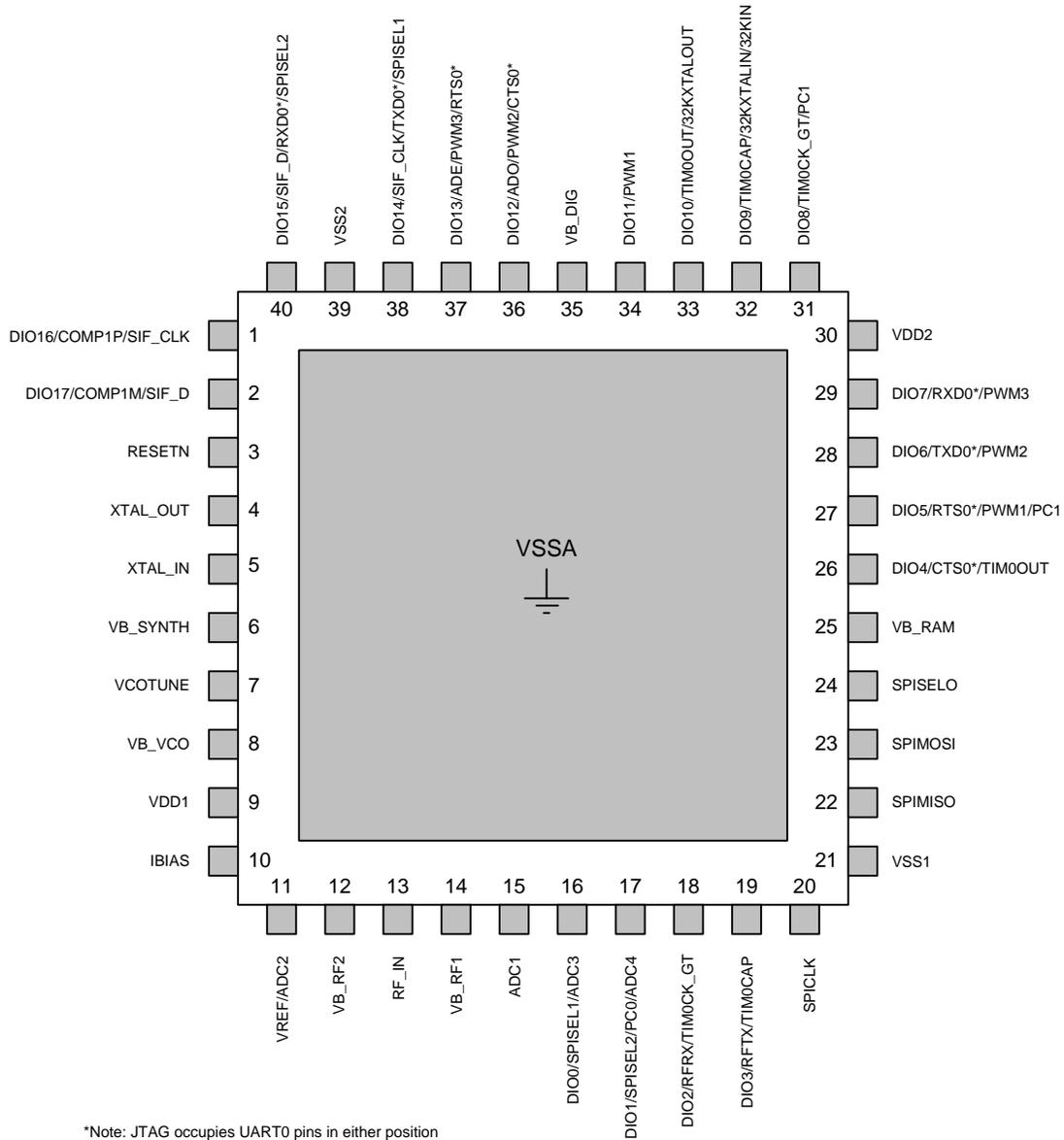


Figure 2: 40-pin QFN Configuration (top view)



Note: Please refer to Appendix B.4 JN5142 Module Reference Design for important applications information regarding the connection of the PADDLE to the PCB.

2.1 Pin Assignment

Pin No	Power supplies					Signal Type	Description
6, 8, 12, 14, 25, 35	VB_SYNTH, VB_VCO, VB_RF2, VB_RF1, VB_RAM, VB_DIG					1.8V	Regulated supply voltage
9, 30	VDD1, VDD2					3.3V	Supplies: VDD1 for analogue, VDD2 for digital
21, 39, Paddle	VSS1, VSS2, VSSA					0V	Grounds (see appendix A.2 for paddle details)
General							
3	RESETN					CMOS	Reset input
4,5	XTAL_OUT, XTAL_IN					1.8V	System crystal oscillator
Radio							
7	VCOTUNE					1.8V	VCO tuning RC network
10	IBIAS					1.8V	Bias current control
13	RF_IN					1.8V	RF antenna
Analogue Peripheral I/O							
15, 16, 17	ADC1, ADC3, ADC4					3.3V	ADC inputs
11	VREF/ADC2					1.8V	Analogue peripheral reference voltage or ADC input 2
1, 2	COMP1P, COMP1M					3.3V	Comparator 1 inputs
Digital Peripheral I/O							
	Primary	Alternate Functions					
20	SPICLK					CMOS	SPI Clock Output
22	SPIMISO					CMOS	SPI Master In Slave Out Input
23	SPIMOSI					CMOS	SPI Master Out Slave In Output
24	SPISEL0					CMOS	SPI Slave Select Output 0
16	DIO0	SPISEL1	ADC3			CMOS	DIO0, SPI Slave Select Output 1 or ADC input 3
17	DIO1	SPISEL2	ADC4	PC0		CMOS	DIO1, SPI Slave Select Output 2, ADC input 4 or Pulse Counter 0 Input
18	DIO2	TIM0CK_GT	RFRX			CMOS	DIO2, Timer0 Clock/Gate Input or Radio Receive Control Output
19	DIO3	TIM0CAP	RFTX			CMOS	DIO3, Timer0 Capture Input or Radio Transmit Control Output
26	DIO4	CTS0	JTAG_TCK	TIM0OUT		CMOS	DIO4, UART 0 Clear To Send Input, JTAG CLK or Timer0 PWM Output
27	DIO5	RTS0	JTAG_TMS	PWM1	PC1	CMOS	DIO5, UART 0 Request To Send Output, JTAG Mode Select, PWM1 Output or Pulse Counter 1 Input
28	DIO6	TXD0	JTAG_TDO	PWM2		CMOS	DIO6, UART 0 Transmit Data Output, JTAG Data Output or PWM2 Output
29	DIO7	RXD0	JTAG_TDI	PWM3		CMOS	DIO7, UART 0 Receive Data Input, JTAG Data Input or PWM 3 Output
31	DIO8	TIM0CK_GT	PC1			CMOS	DIO8, Timer0 Clock/Gate Input or Pulse Counter1 Input
32	DIO9	TIM0CAP	32KXTALIN			CMOS	DIO9, Timer0 Capture Input or 32K External Crystal Input

Digital Peripheral I/O							
	Primary	Alternate Functions					
33	DIO10	TIM0OUT	32KXTALOUT			CMOS	DIO10, Timer0 PWM Output or 32K External Crystal Output
34	DIO11	PWM1				CMOS	DIO11 or PWM1 Output
36	DIO12	PWM2	CTS0	JTAG_TCK	ADO	CMOS	DIO12, PWM2 Output, UART 0 Clear To Send Input, JTAG CLK or Antenna Diversity Odd
37	DIO13	PWM3	RTS0	JTAG_TMS	ADE	CMOS	DIO13, PWM3 Output, UART 0 Request To Send Output, JTAG Mode Select or Antenna Diversity Even
38	DIO14	SIF_CLK	TXD0	JTAG_TDO	SPISEL1	CMOS	DIO14, Serial Interface Clock, UART 0 Transmit Data Output, JTAG Data Output or SPI Slave Select Output 1
40	DIO15	SIF_D	RXD0	JTAG_TDI	SPISEL2	CMOS	DIO15, Serial Interface Data, UART 0 Receive Data Input, JTAG Data Input or SPI Slave Select Output 2
1	DIO16	COMP1P	SIF_CLK			CMOS	DIO16, Comparator Positive Input or Serial Interface clock
2	DIO17	COMP1M	SIF_D			CMOS	DIO17, Comparator Negative Input or Serial Interface Data



The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5142 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

2.2 Pin Descriptions

2.2.1 Power Supplies

The device is powered from the VDD1 and VDD2 pins, each being decoupled with a 100nF ceramic capacitor. VDD1 is the power supply to the analogue circuitry; it should be decoupled to ground. VDD2 is the power supply for the digital circuitry; and should also be decoupled to ground. In addition, a common 10 μ F tantalum capacitor is required for low frequencies. Decoupling pins for the internal 1.8V regulators are provided which each require a 100nF capacitor located as close to the device as practical. VB_SYNTN, VB_RAM and VB_DIG require only a 100nF capacitor. VB_RF and VB_RF2 should be connected together as close to the device as practical, and require one 100nF capacitor and one 47pF capacitor. The pin VB_VCO requires a 10nF capacitor. Refer to B.4.1 for schematic diagram.

VSSA, VSS1, VSS2 are the ground pins.

Users are strongly discouraged from connecting their own circuits to the 1.8v regulated supply pins, as the regulators have been optimised to supply only enough current for the internal circuits.

2.2.2 Reset

RESETN is an active low reset input pin that is connected to a 300k Ω internal pull-up resistor. It may be pulled low by an external circuit. Refer to Section 6.2 for more details.

2.2.3 32MHz Oscillator

A crystal is connected between XTALIN and XTALOUT to form the reference oscillator, which drives the system clock. A capacitor to analogue ground is required on each of these pins. Refer to Section 5.1 for more details. The 32MHz reference frequency is divided down to 16MHz and this is used as the system clock throughout the device.

2.2.4 Radio

The radio is a single ended design, requiring a capacitor and just two inductors to match to 50 Ω microstrip line to the RF_IN pin.

An external resistor (43k Ω) is required between IBIAS and analogue ground to set various bias currents and references within the radio.

2.2.5 Analogue Peripherals

The ADC requires a reference voltage to use as part of its operation. It can use either an internal reference voltage or an external reference connected to VREF. This voltage is referenced to analogue ground and the performance of the analogue peripherals is dependent on the quality of this reference.

There are four ADC inputs and a pair of comparator inputs. ADC1 has a designated input pin but ADC2 uses the same pin as VREF, invalidating its use as an ADC pin when an external reference voltage is required. The remaining 2 ADC channels are shared with the digital I/Os DIO0 and DIO1 and connect to pins 16 and 17. When these two ADC channels are selected, the corresponding DIOs must be configured as Inputs with their pull-ups disabled. Similarly, the comparator shares pins 1 and 2 with DIO16 and DIO17, so when the comparator is selected these pins must be configured as Inputs with their pull-ups disabled. The analogue I/O pins on the JN5142 can have signals applied up to 0.3v higher than VDD1. A schematic view of the analogue I/O cell is shown in Figure 3. Figure 4 demonstrates a special case, where a digital I/O pin doubles as an input to analogue devices. This applies to ADC3, ADC4, COMP1P and COMP1M.

In reset, sleep and deep sleep, the analogue peripherals are all off. In sleep, the comparator may optionally be used as a wakeup source.

Unused ADC and comparator inputs should not be left unconnected, for example connected to analogue ground.

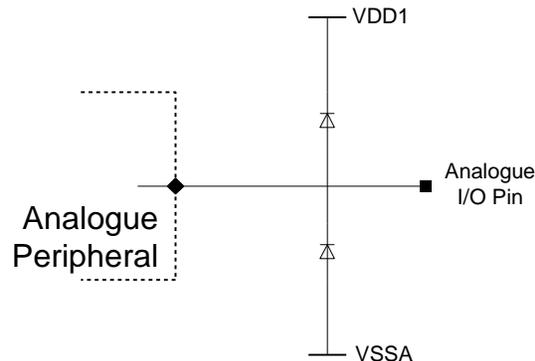


Figure 3: Analogue I/O Cell

2.2.6 Digital Input/Output

Most digital I/O pins on the JN5142 can have signals applied up to 2V higher than VDD2 (with the exception of DIOs 0, 1, 9, 10, 15, 16 and 17, which are 3V tolerant) are therefore TTL-compatible with VDD2 > 3V. For other DC properties of these pins see Section 19.2.3.

When used in their primary function all Digital Input/Output pins are bi-directional and are connected to weak internal pull up resistors (40kΩ nominal) that can be disabled. When used in their secondary function (selected when the appropriate peripheral block is enabled through software library calls) then their direction is fixed by the function. The pull up resistor is enabled or disabled independently of the function and direction; the default state from reset is enabled.

A schematic view of the digital I/O cell is in Figure 4. The dotted lines through resistor R_{ESD} represent a path that exists only on DIO0, DIO1, DIO15, DIO16 and DIO17 which are also inputs to the ADC (ADC3, ADC4) and Comparator (COMP1P, COMP1M) respectively. To use these DIO pins for their analogue functions, the DIO must be set as an Input with its pull-up resistor, R_{PU} , disabled.

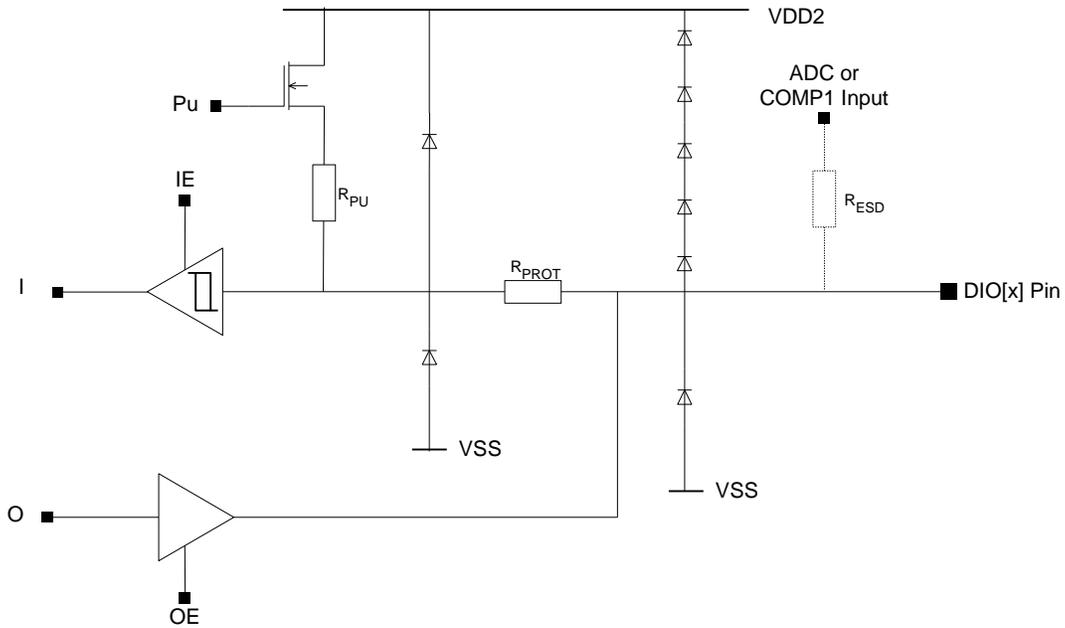


Figure 4: DIO Pin Equivalent Schematic

In reset, the digital peripherals are all off and the DIO pins are set as high-impedance inputs. During sleep and deep sleep, the DIO pins retain both their input/output state and output level that was set as sleep commences. If the DIO pins were enabled as inputs and the interrupts were enabled then these pins may be used to wake up the JN5142 from sleep.

3 CPU

The CPU of the JN5142 is a 32-bit load and store RISC processor. It has been architected for three key requirements:

- Low power consumption for battery powered applications
- High performance to implement a wireless protocol at the same time as complex applications
- Efficient coding of high-level languages such as C provided with the Software Developers Kit

It features a linear 32-bit logical address space with unified memory architecture, accessing both code and data in the same address space. Registers for peripheral units, such as the timers, UART and the baseband processor are also mapped into this space.

The CPU has access to a block of 15 32-bit General-Purpose (GP) registers together with a small number of special purpose registers which are used to store processor state and control interrupt handling. The contents of any GP register can be loaded from or stored to memory, while arithmetic and logical operations, shift and rotate operations, and signed and unsigned comparisons can be performed either between two registers and stored in a third, or between registers and a constant carried in the instruction. Operations between general or special-purpose registers execute in one cycle while those that access memory require a further cycle to allow the memory to respond.

The instruction set manipulates 8, 16 and 32-bit data; this means that programs can use objects of these sizes very efficiently. Manipulation of 32-bit quantities is particularly useful for protocols and high-end applications allowing algorithms to be implemented in fewer instructions than on smaller word-size processors, and to execute in fewer clock cycles. In addition, the CPU supports hardware Multiply that can be used to efficiently implement algorithms needed by Digital Signal Processing applications.

The instruction set is designed for the efficient implementation of high-level languages such as C. Access to fields in complex data structures is very efficient due to the provision of several addressing modes, together with the ability to be able to use any of the GP registers to contain the address of objects. Subroutine parameter passing is also made more efficient by using GP registers rather than pushing objects onto the stack. The recommended programming method for the JN5142 is by using C, which is supported by a software developer kit comprising a C compiler, linker and debugger.

The CPU architecture also contains features that make the processor suitable for embedded, real-time applications. In some applications, it may be necessary to use a real-time operating system to allow multiple tasks to run on the processor. To provide protection for device-wide resources being altered by one task and affecting another, the processor can run in either supervisor or user mode, the former allowing access to all processor registers, while the latter only allows the GP registers to be manipulated. Supervisor mode is entered on reset or interrupt; tasks starting up would normally run in user mode in a RTOS environment.

Embedded applications require efficient handling of external hardware events. Exception processing (including reset and interrupt handling) is enhanced by the inclusion of a number of special-purpose registers into which the PC and status register contents are copied as part of the operation of the exception hardware. This means that the essential registers for exception handling are stored in one cycle, rather than the slower method of pushing them onto the processor stack. The PC is also loaded with the vector address for the exception that occurred, allowing the handler to start executing in the next cycle.

To improve power consumption a number of power-saving modes are implemented in the JN5142, described more fully in Section 18. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on an interrupt it will wake up to service the request. Additionally, it is possible under software control, to set the speed of the CPU to 1, 2, 4, 8, 16 or 32MHz. This feature can be used to trade-off processing power against current consumption.

4 Memory Organisation

This section describes the different memories found within the JN5142. The device contains ROM, RAM, OTP eFuse memory, the wireless transceiver and peripherals all within the same linear address space.

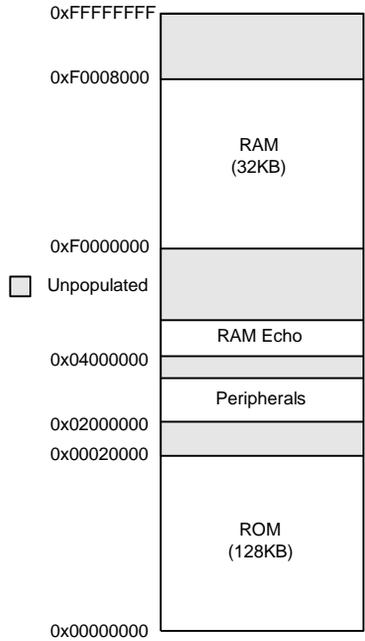


Figure 5: JN5142 Memory Map

4.1 ROM

The ROM is 128k bytes in size, and can be accessed by the processor in a single CPU clock cycle. The ROM contents include bootloader to allow external Flash memory contents to be bootloaded into RAM at runtime, a default interrupt vector table, an interrupt manager, IEEE802.15.4 MAC and APIs for interfacing on-chip peripherals. The operation of the boot loader is described in detail in Application Note [9]. The interrupt manager routes interrupt calls to the application’s soft interrupt vector table contained within RAM. Section 7 contains further information regarding the handling of interrupts. ROM contents are shown in Figure 6.

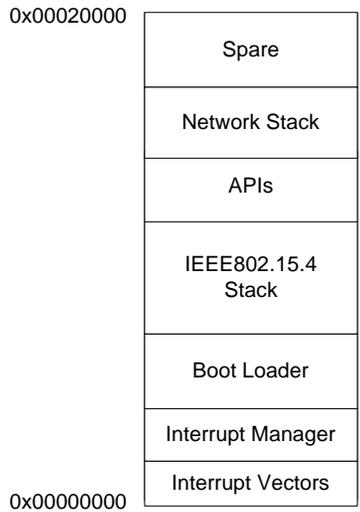


Figure 6: Typical ROM Contents

4.2 RAM

The JN5142 contains 32KBytes of high speed RAM. It can be used for both code and data storage and is accessed by the CPU in a single clock cycle. At reset, a boot loader controls the loading of segments of code and data from an external memory connected to the SPI port, into RAM. Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are un-powered. Typical RAM contents are shown in Figure 7.

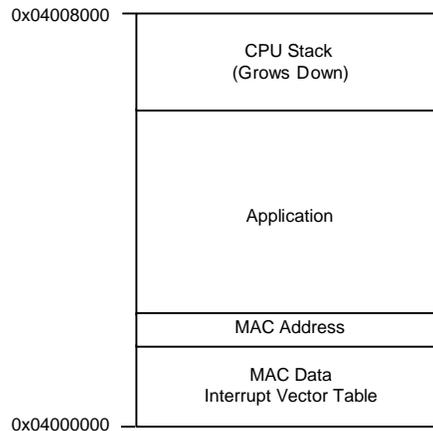


Figure 7: Typical RAM Contents

4.3 OTP eFuse Memory

The JN5142 contains a total of 29bytes of eFuse memory; this is a One Time Programmable (OTP) memory that can be used to support a 40-bit MAC ID (For a 64-bit MAC ID, the 24 bit company ID, OUI, can be stored in the external memory) and a 128-bit AES security key. A limited number of bits are available for customer use for storage of configuration information; configuration of these is made through use of software APIs.

For further information on how to program and use the eFuse memory, please contact technical support via the on-line tech-support system.

Alternatively, NXP can provide an eFuse programming service for customers that wish to use the eFuse but do not wish to undertake this for themselves. For further details of this service, please contact your local NXP sales office.

4.4 External Memory

An external memory with an SPI interface may be used to provide storage for program code and data for the device when external power is removed. The memory is connected to the SPI interface using select line SPISEL0; this select line is dedicated to the external memory interface and is not available for use with other external devices. See Figure 8 for connection details.

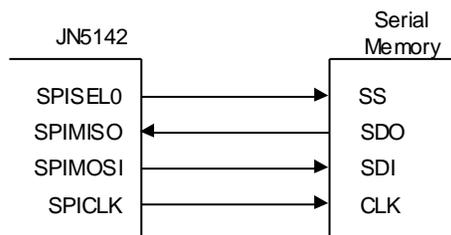


Figure 8: Connecting External Serial Memory

At reset, the contents of this memory are copied into RAM by the software boot loader. The Flash and EEPROM memory devices that are supported as standard through the JN5142 bootloader are given in Table 1. NXP recommends that where possible one of these devices should be selected.

Manufacturer	Part Number	Size	Type
Micron (Numonyx)	M25P10A	1 Mbit	Flash
	M25P05A	512 kbit	Flash
Winbond	W25X20B	2 Mbit	Flash
	W25X10B	1 Mbit	Flash
Microchip	25AA080	8 kbit	EEPROM
	25AA160	16 kbit	EEPROM
	25AA320	32 kbit	EEPROM

Table 1: Supported Flash and EEPROM Memories

Applications wishing to use an alternate Flash memory device should refer to Application Note [2]. This application note provides guidance on developing an interface to an alternate device.

4.4.1 External Memory Encryption

The contents of the external serial memory may be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in eFuse.

When bootloading program code from external serial memory, the JN5142 automatically accesses the encryption key to execute the decryption process. User program code does not need to handle any of the decryption process; it is transparent.

With encryption enabled, the time taken to boot code from external flash is increased.

4.5 Peripherals

All peripherals have their registers mapped into the memory space. Access to these registers requires 3 clock cycles. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see [5].

4.6 Unused Memory Addresses

Any attempt to access an unpopulated memory area will result in a bus error exception (interrupt) being generated.

5 System Clocks

Two system clocks are used to provide timing references into the on-chip subsystems of the JN5142. A 16MHz clock, generated by a crystal-controlled 32MHz oscillator, is used by the transceiver, processor, memory and digital and analogue peripherals. A 32kHz clock is used by the sleep timer and is generated by one of two on-chip oscillators or can be supplied externally.

5.1 16MHz System Clock

The 16MHz system clock is used by the digital and analogue peripherals and the transceiver. A scaled version (1,2,4,8,16 or 32MHz) of this clock is also used by the processor and memories. For most operations it is necessary to source this clock from the 32MHz oscillator.

Crystal oscillators are generally slow to start. Hence to provide a faster start-up following a sleep cycle a fast RC oscillator is provided that can be used as the source for the 16MHz system clock. The oscillator starts very quickly and can run at 27MHz or 32MHz (calibrated), giving system clock speeds of either 13.5MHz or 16MHz. Using the oscillator at 27MHz scales down the speed of the processor and any peripherals in use. For the SPI interface this causes no functional issues as the generated SPI clock is slightly slower and is used to clock the external SPI slave. Use of the radio or UART is not possible when using the high-speed RC oscillator, as even after calibration there is a +/- 7.5% tolerance. Additionally, timers should be used with care as the exact frequency will not be known.

On wake-up from sleep, the JN5142 uses the Fast RC oscillator. It can then either:

- Automatically switch over to use the 32MHz clock source when it has started up.
- Continue to use the fast RC oscillator until software triggers the switch-over to the 32MHz clock source, for example when the radio is required.
- Continue to use the RC oscillator until the device goes back into one of the sleep modes.

Compared to the JN5148, the use of the fast RC Oscillator at wake-up means, there is no need to wait for the 32MHz crystal oscillator to start, if it is necessary to download code from the external memory. Consequently, in this situation, application code will start executing earlier, with a typical improvement of 550µsec.

5.1.1 32MHz Oscillator

The JN5142 contains the necessary on chip components to build a 32MHz reference oscillator with the addition of an external crystal resonator and two tuning capacitors. The schematic of these components are shown in Figure 9. The two capacitors, C1 and C2, should typically be 15pF and use a COG dielectric. Due to the small size of these capacitors, it is important to keep the traces to the external components as short as possible. The on chip transconductance amplifier is compensated for temperature variation, and is self-biasing by means of the internal resistor R1. This oscillator provides the frequency reference for the radio and therefore it is essential that the reference PCB layout and BOM are carefully followed. The electrical specification of the oscillator can be found in Section 19.3.10. Please refer to Appendix B for development support with the crystal oscillator circuit.

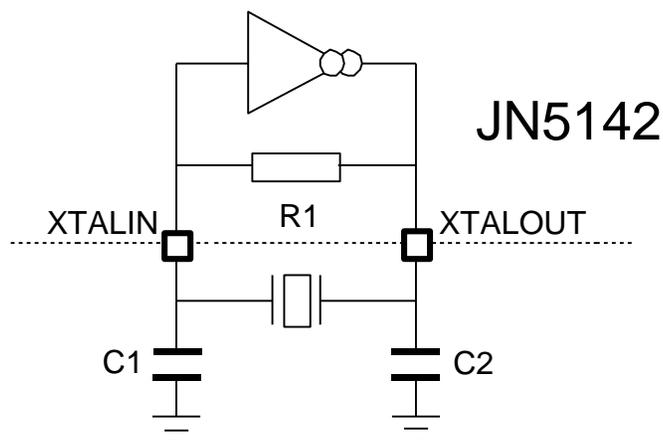


Figure 9: 32MHz Crystal Oscillator Connections

5.1.2 High-Speed RC Oscillator

An on-chip High-Speed RC oscillator is provided, capable of running at either 27MHz typical or 32MHz typical once calibrated, using the software API function. No external components are required for this oscillator. The electrical specification of the oscillator can be found in Section 19.3.11.

5.2 32kHz System Clock

The 32kHz system clock is used for timing the length of a sleep period (see Section 18). The clock can be selected from one of three sources through the application software:

- 32kHz RC Oscillator
- 32kHz Crystal Oscillator
- 32kHz External Clock

Upon a chip reset or power-up the JN5142 defaults to using the internal 32kHz RC Oscillator. If another clock source is selected then it will remain in use for all 32kHz timing until a chip reset is performed.

5.2.1 32kHz RC Oscillator

The internal 32kHz RC oscillator requires no external components. The internal timing components of the oscillator have a wide tolerance due to manufacturing process variation and so the oscillator runs nominally at 32kHz $\pm 30\%$. To make this useful as a timing source for accurate wakeup from sleep, a frequency calibration factor derived from the more accurate 16MHz clock may be applied. The calibration factor is derived through software, details can be found in Section 11.3.1. Software must check that the 32kHz RC oscillator is running before using it. For detailed electrical specifications, see Section 19.3.8.

5.2.2 32kHz Crystal Oscillator

In order to obtain more accurate sleep periods, the JN5142 contains the necessary on-chip components to build a 32kHz oscillator with the addition of an external 32.768kHz crystal and two tuning capacitors. The crystal should be connected between 32KXTALIN and 32KXTALOUT (DIO9 and DIO10), with two equal capacitors to ground, one on each pin. Due to the small size of the capacitors, it is important to keep the traces to the external components as short as possible.

The electrical specification of the oscillator can be found in Section 19.3.9. The oscillator cell is flexible and can operate with a range of commonly available 32.768kHz crystals with load capacitances from 6 to 12.5pF. However, the maximum ESR of the crystal and the supply current are both functions of the actual crystal used, see Appendix B.1 for more details.

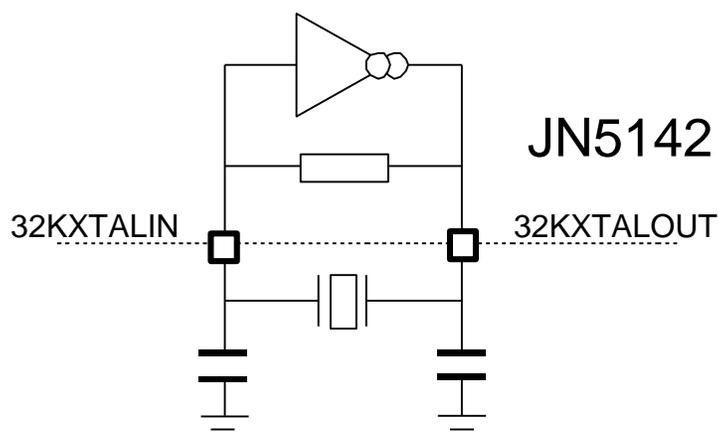


Figure 10: 32kHz Crystal Oscillator Connections

5.2.3 32kHz External Clock

An externally supplied 32kHz reference clock on the 32KIN input (DIO9) may be provided to the JN5142. This would allow the 32kHz system clock to be sourced from a very stable external oscillator module, allowing more accurate sleep cycle timings compared to the internal RC oscillator. (See Section 19.2.3, DIO9 is a 3V tolerant input)

6 Reset

A system reset initialises the device to a pre-defined state and forces the CPU to start program execution from the reset vector. The reset process that the JN5142 goes through is as follows.

When power is first applied or when the external reset is released, the High-Speed RC oscillator and 32MHz crystal oscillator are activated. After a short wait period (13µsec approx) while the High-Speed RC starts up, and so long as the supply voltage satisfies the default Supply Voltage Monitor (SVM) threshold (2.0V+0.045V hysteresis), the internal 1.8V regulators are turned on to power the processor and peripheral logic. This is followed by a further wait (again 13µsec approx) before the eFuse SVM threshold is read and applied. After a brief pause (approx 2.5µsec) the SVM is checked again with the new threshold and if successful, the internal reset is removed from the CPU and peripheral logic and the CPU starts to run code beginning at the reset vector, consisting of initialisation code and the resident boot loader. [9] Section 19.3.1 provides detailed electrical data and timing.

The JN5142 has five sources of reset:

- Internal Power-on / Brown-out Reset (BOR)
- External Reset
- Software Reset
- Watchdog timer
- Supply Voltage detect



Note: When the device exits a reset condition, device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, then the device must be held in reset until the operating conditions are met. (See Section 19.3)

6.1 Internal Power-On / Brown-out Reset (BOR)

For the majority of applications the internal power-on reset is capable of generating the required reset signal. When power is applied to the device, the power-on reset circuit monitors the rise of the VDD supply. When the VDD reaches the specified threshold, the reset signal is generated. This signal is held internally until the power supply and oscillator stabilisation time has elapsed, when the internal reset signal is then removed and the CPU is allowed to run.

The BOR circuit has the ability to reject spikes on the VDD rail to avoid false triggering of the reset module. Typically for a negative going square pulse of duration 1µs, the voltage must fall to 1.2v before a reset is generated. Similarly for a triangular wave pulse of 10µs width, the voltage must fall to 1.3v before causing a reset. The exact characteristics are complex and these are only examples.

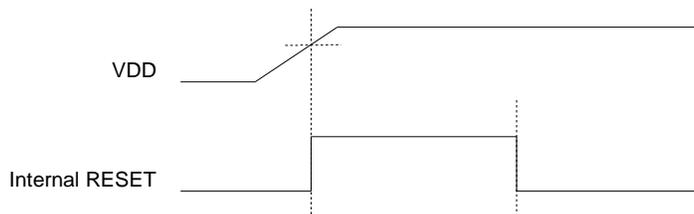


Figure 11: Internal Power-on Reset

When the supply drops below the power on reset 'falling' threshold, it will re-trigger the reset. If necessary, use of the external reset circuit show in Figure 12 is suggested.

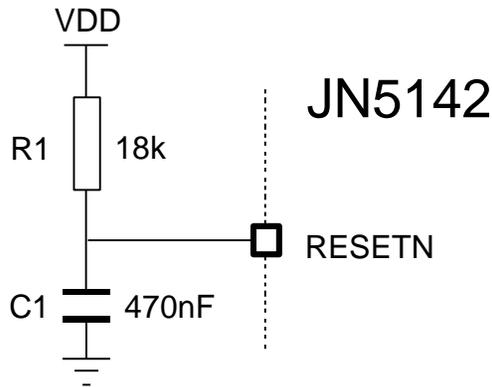


Figure 12: External Reset Generation

The external resistor and capacitor provide a simple reset operation when connected to the RESETN pin.

6.2 External Reset

An external reset is generated by a low level on the RESETN pin. Reset pulses longer than the minimum pulse width will generate a reset during active or sleep modes. Shorter pulses are not guaranteed to generate a reset. The JN5142 is held in reset while the RESETN pin is low. When the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the internal reset process starts.

The JN5142 has an internal 300k Ω pull-up resistor connect to the RESETN pin. The pin is an input for an external reset only.

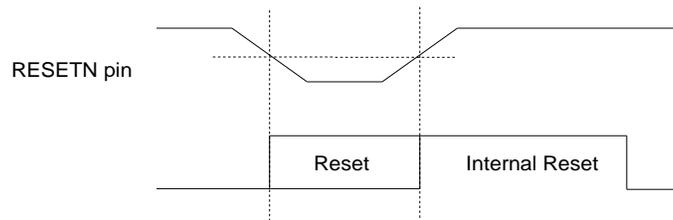


Figure 13: External Reset

6.3 Software Reset

A system reset can be triggered at any time through software control, causing a full chip reset and invalidating the RAM contents. For example this can be executed within a user's application upon detection of a system failure.

6.4 Supply Voltage Monitor (SVM)

An internal Supply Voltage Monitor (SVM) is used to monitor the supply voltage to the JN5142; this can be used whilst the device is awake or is in CPU doze mode. Dips in the supply voltage below a variable threshold can be detected and can be used to cause the JN5142 to perform a chip reset. Equally, dips in the supply voltage can be detected and used to cause an interrupt to the processor, when the voltage either drops below the threshold or rises above it.

The supply voltage detect is enabled by default from power-up and can extend the reset during power-up. This will keep the CPU in reset until the voltage exceeds the SVM threshold voltage. The threshold voltage is configurable to 1.95V, 2.0V, 2.1V, 2.2V, 2.3V, 2.4V, 2.7V and 3.0V and is controllable by software. From power-up the threshold is

set by eFuse settings and the default chip configuration is for the 2.3V threshold. It is recommended that the threshold is set so that, as a minimum, the chip is held in reset until the voltage reaches the level required by the external memory device on the SPI interface.

6.5 Watchdog Timer

A watchdog timer is provided to guard against software lockups. It operates by counting cycles of the high-speed RC system clock. A pre-scaler is provided to allow the expiry period to be set between typically 8ms and 16.4 seconds (dependent on high-speed RC accuracy: +30%, -15%). Failure to restart the watchdog timer within the pre-configured timer period will cause a chip reset to be performed. A status bit is set if the watchdog was triggered so that the software can differentiate watchdog initiated resets from other resets, and can perform any required recovery once it restarts.

After power up, reset, start from deep sleep or start from sleep, the watchdog is always enabled with the largest timeout period and will commence counting as if it had just been restarted. Under software control the watchdog can be disabled. If it is enabled, the user must regularly restart the watchdog timer to stop it from expiring and causing a reset. The watchdog runs continuously, even during doze, however the watchdog does not operate during sleep or deep sleep, or when the hardware debugger has taken control of the CPU. It will recommence automatically if enabled once the debugger un-stalls the CPU.

7 Interrupt System

The interrupt system on the JN5142 is a hardware-vector interrupt system. The JN5142 provides several interrupt sources, some associated with CPU operations (CPU exceptions) and others which are used by hardware in the device. When an interrupt occurs, the CPU stops executing the current program and loads its program counter with a fixed hardware address specific to that interrupt. The interrupt handler or interrupt service routine is stored at this location and is run on the next CPU cycle. Execution of interrupt service routines is always performed in supervisor mode. Interrupt sources and their vector locations are listed in Table 2 below:

Interrupt Source	Vector Location	Interrupt Definition
Bus error	0x08	Typically cause by an attempt to access an invalid address or a disabled peripheral
Tick timer	0x0e	Tick timer interrupt asserted
Alignment error	0x14	Load/store address to non-naturally-aligned location
Illegal instruction	0x1a	Attempt to execute an unrecognised instruction
Hardware interrupt	0x20	interrupt asserted
System call	0x26	System call initiated by b.sys instruction
Trap	0x2c	caused by the b.trap instruction or the debug unit
Reset	0x38	Caused by software or hardware reset.
Stack Overflow	0x3e	Stack overflow

Table 2: Interrupt Vectors

7.1 System Calls

The b.trap and b.sys instructions allow processor exceptions to be generated by software.

A system call exception will be generated when the b.sys instruction is executed. This exception can, for example, be used to enable a task to switch the processor into supervisor mode when a real time operating system is in use. (See Section 3 for further details.)

The b.trap instruction is commonly used for trapping errors and for debugging.

7.2 Processor Exceptions

7.2.1 Bus Error

A bus error exception is generated when software attempts to access a memory address that does not exist, or is not populated with memory or peripheral registers or when writing to ROM.

7.2.2 Alignment

Alignment exceptions are generated when software attempts to access objects that are not aligned to natural word boundaries. 16-bit objects must be stored on even byte boundaries, while 32-bit objects must be stored on quad byte boundaries. For instance, attempting to read a 16-bit object from address 0xFFF1 will trigger an alignment exception as will a read of a 32-bit object from 0xFFF1, 0xFFF2 or 0xFFF3. Examples of legal 32-bit object addresses are 0xFFF0, 0xFFF4, 0xFFF8 etc.

7.2.3 Illegal Instruction

If the CPU reads an unrecognised instruction from memory as part of its instruction fetch, it will cause an illegal instruction exception.

7.2.4 Stack Overflow

When enabled, a stack overflow exception occurs if the stack pointer reaches a programmable location.

7.3 Hardware Interrupts

Hardware interrupts generated from the transceiver, analogue or digital peripherals and DIO pins are individually masked using the Programmable Interrupt Controller (PIC). Management of interrupts is provided in the peripherals library [5]. For details of the interrupts generated from each peripheral see the respective section in this datasheet.

Interrupts can be used to wake the JN5142 from sleep. The peripherals, baseband controller, security coprocessor and PIC are powered down during sleep but the DIO interrupts and optionally the pulse counters, wake-up timers and analogue comparator interrupts remain powered to bring the JN5142 out of sleep.

Prioritised external interrupt handling (i.e., interrupts from hardware peripherals) is provided to enable an application to control an events priority to provide for deterministic program execution.

The priority Interrupt controller provides 15 levels of prioritised interrupts. The priority level of all interrupts can be set, with value 0 being used to indicate that the source can never produce an external interrupt, 1 for the lowest priority source(s) and 15 for the highest priority source(s). Note that multiple interrupt sources can be assigned the same priority level if desired.

If while processing an interrupt, a new event occurs at the same or lower priority level, a new external interrupt will not be triggered. However, if a new higher priority event occurs, the external interrupt will again be asserted, interrupting the current interrupt service routine.

Once the interrupt service routine is complete, lower priority events can be serviced.

8.1.1 Radio External Components

In order to realise the full performance of the radio it is essential that the reference PCB layout and BOM are carefully followed. See Appendix B.4.

The radio is powered from a number of internal 1.8V regulators fed from the analogue supply VDD1, in order to provide good noise isolation between the digital logic of the JN5142 and the analogue blocks. These regulators are also controlled by the baseband controller and protocol software to minimise power consumption. Decoupling for internal regulators is required as described in Section 2.2.1.

For single ended antennas or connectors, a balun is not required, however a matching network is needed.

The RF matching network requires three external components and the IBIAS pin requires one external component as shown in schematic in B.4.1. These components are critical and should be placed close to the JN5142 pins and analogue ground as defined in Table 13. Specifically, the output of the network comprising L2, C1 and L1 is designed to present an accurate match to a 50 ohm resistive network as well as provide a DC path to the final output stage or antenna. Users wishing to match to other active devices such as amplifiers should design their networks to match to 50 ohms at the output of L1

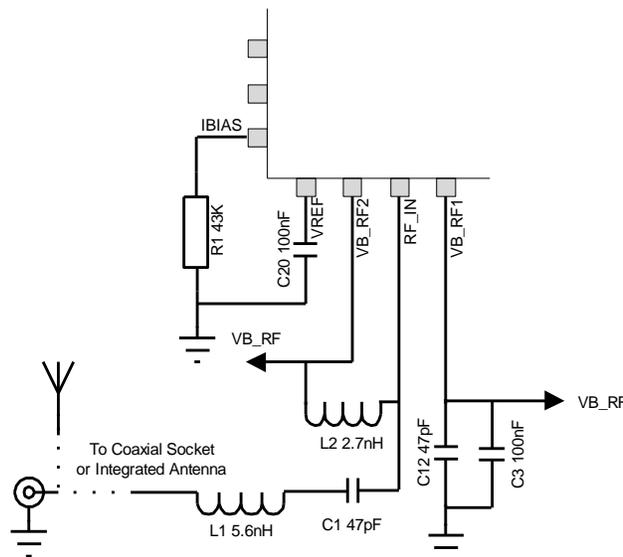


Figure 15: External Radio Components

8.1.2 Antenna Diversity

Support is provided for antenna diversity. Antenna diversity is a technique that maximises the performance of an antenna system. It allows the radio to switch between two antennas that have very low correlation between their received signals. Typically, this is achieved by spacing two antennas around 0.25 wavelengths apart or by using two orthogonal polarisations. So, if a packet is transmitted and no acknowledgement is received, the radio system can switch to the other antenna for the retry, with a different probability of success.

The JN5142 provides an output (ADO) on DIO12 that is asserted on odd numbered retries and optionally its complement (ADE) on DIO13, that can be used to control an antenna switch; this enables antenna diversity to be implemented easily (see Figure 16 and Figure 17).

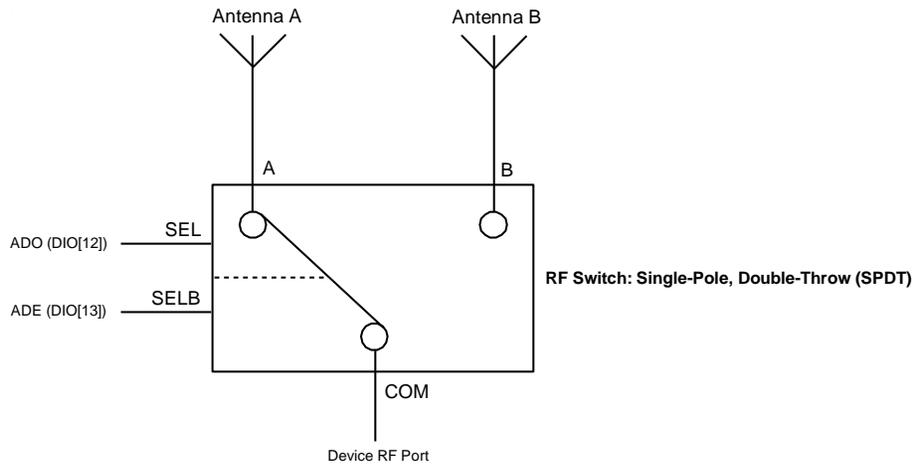


Figure 16: Simple Antenna Diversity Implementation using External RF Switch

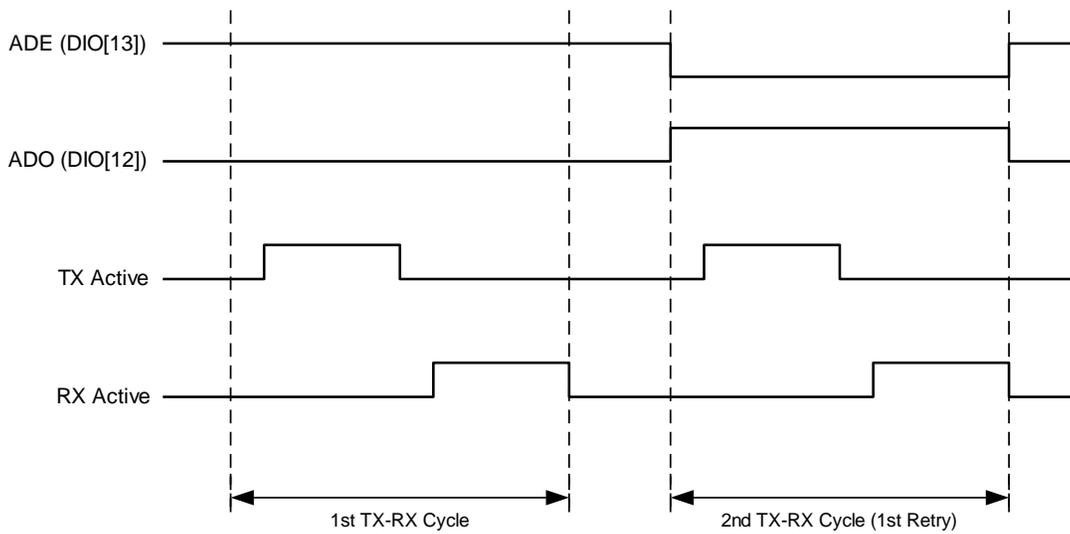


Figure 17: Antenna Diversity ADO Signal for TX with Acknowledgement

If two DIO pins cannot be spared, DIO13 can be configured to be a normal DIO pin, and the inverse of ADO generated with an inverter on the PCB.

8.2 Modem

The modem performs all the necessary modulation and spreading functions required for digital transmission and reception of data at 250kbps in the 2450MHz radio frequency band in compliance with the IEEE802.15.4 standard.

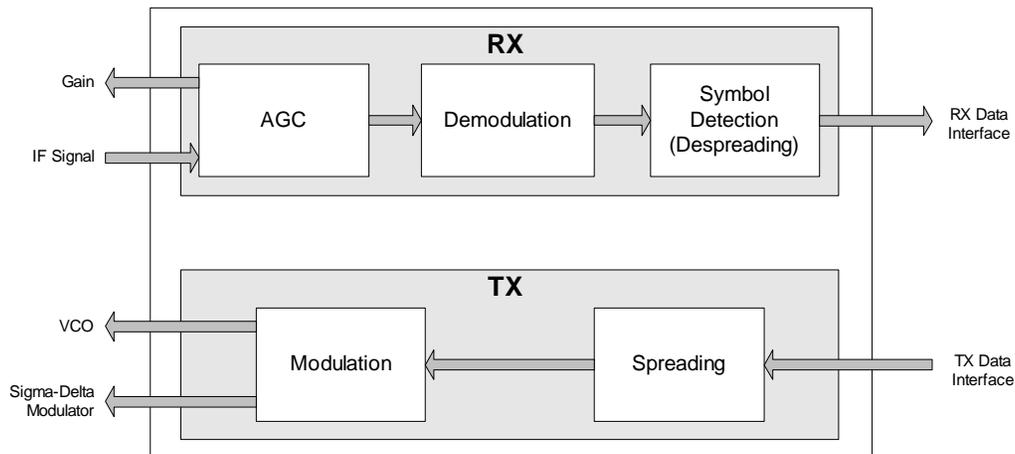


Figure 18: Modem Architecture

Features provided to support network channel selection algorithms include Energy Detection (ED), Link Quality Indication (LQI) and fully programmable Clear Channel Assessment (CCA).

The Modem provides a digital Receive Signal Strength Indication (RSSI) that facilitates the implementation of the IEEE 802.15.4 ED function and LQI function.

The ED and LQI are both related to receiver power in the same way, as shown in Figure 19. LQI is associated with a received packet, whereas ED is an indication of signal power on air at a particular moment.

The CCA capability of the Modem supports all modes of operation defined in the IEEE 802.15.4 standard, namely Energy above ED threshold, Carrier Sense and Carrier Sense and/or energy above ED threshold.

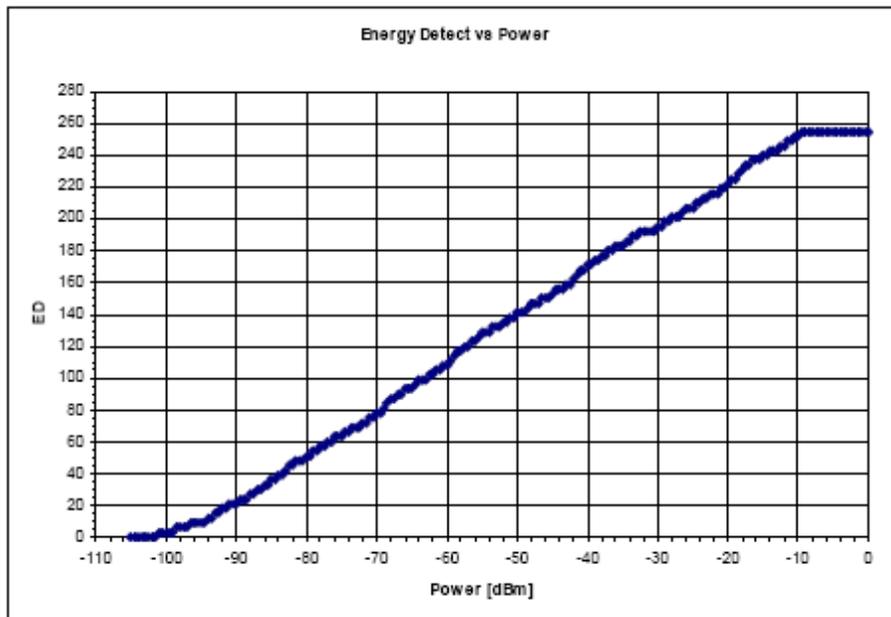


Figure 19: Energy Detect Value vs Receive Power Level

8.3 Baseband Processor

The baseband processor provides all time-critical functions of the IEEE802.15.4 MAC layer. Dedicated hardware guarantees air interface timing is precise. The MAC layer hardware/software partitioning, enables software to implement the sequencing of events required by the protocol and to schedule timed events with millisecond resolution, and the hardware to implement specific events with microsecond timing resolution. The protocol software layer performs the higher-layer aspects of the protocol, sending management and data messages between endpoint and coordinator nodes, using the services provided by the baseband processor.

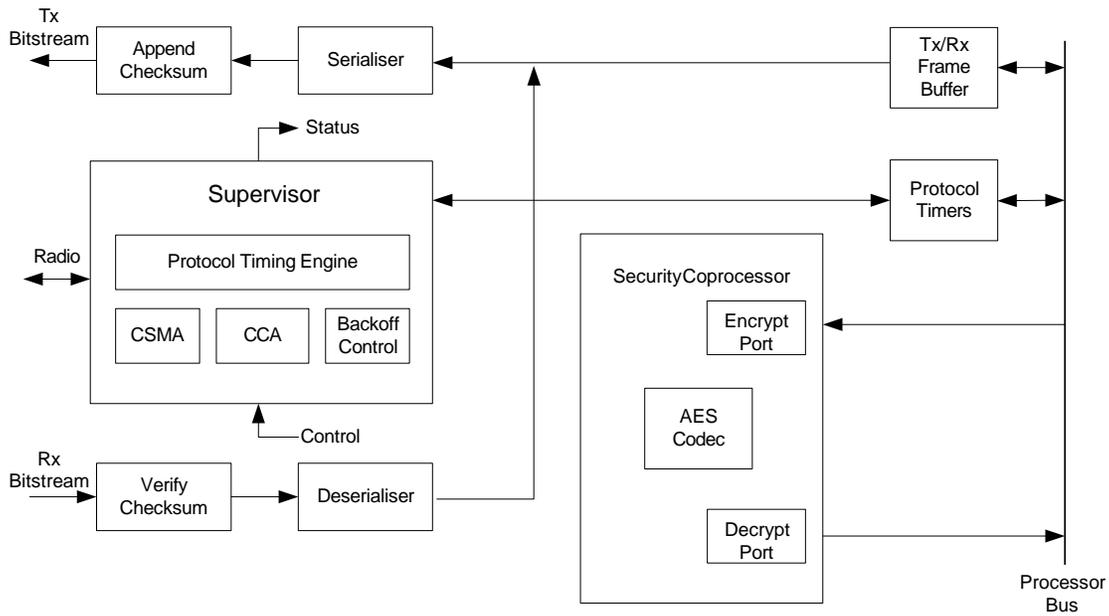


Figure 20: Baseband Processor

8.3.1 Transmit

A transmission is performed by software writing the data to be transferred into the Tx/Rx Frame Buffer, together with parameters such as the destination address and the number of retries allowed, and programming one of the protocol timers to indicate the time at which the frame is to be sent. This time will be determined by the software tracking the higher-layer aspects of the protocol such as superframe timing and slot boundaries. Once the packet is prepared and protocol timer set, the supervisor block controls the transmission. When the scheduled time arrives, the supervisor controls the sequencing of the radio and modem to perform the type of transmission required. It can perform all the algorithms required by IEEE802.15.4 such as CSMA/CA without processor intervention including retries and random backoffs.

When the transmission begins, the header of the frame is constructed from the parameters programmed by the software and sent with the frame data through the serialiser to the Modem. At the same time, the radio is prepared for transmission. During the passage of the bitstream to the modem, it passes through a CRC checksum generator that calculates the checksum on-the-fly, and appends it to the end of the frame.

8.3.2 Reception

During reception, the radio is set to receive on a particular channel. On receipt of data from the modem, the frame is directed into the Tx/Rx Frame Buffer where both header and frame data can be read by the protocol software. An interrupt may be provided on receipt of the frame header. As the frame data is being received from the modem it is passed through a checksum generator; at the end of the reception the checksum result is compared with the checksum at the end of the message to ensure that the data has been received correctly. An interrupt may be provided to indicate successful packet reception. During reception, the modem determines the Link Quality, which is made available at the end of the reception as part of the requirements of IEEE802.15.4.

8.3.3 Auto Acknowledge

Part of the protocol allows for transmitted frames to be acknowledged by the destination sending an acknowledge packet within a very short window after the transmitted frame has been received. The JN5142 baseband processor can automatically construct and send the acknowledgement packet without processor intervention and hence avoid the protocol software being involved in time-critical processing within the acknowledge sequence. The JN5142 baseband processor can also request an acknowledge for packets being transmitted and handle the reception of acknowledged packets without processor intervention.

8.3.4 Beacon Generation

In beaconing networks, the baseband processor can automatically generate and send beacon frames; the repetition rate of the beacons is programmed by the CPU, and the baseband then constructs the beacon contents from data delivered by the CPU. The baseband processor schedules the beacons and transmits them without CPU intervention.

8.3.5 Security

The transmission and reception of secured frames using the Advanced Encryption Standard (AES) algorithm is handled by the security coprocessor and the stack software. The application software must provide the appropriate encrypt/decrypt keys for the transmission or reception. On transmission, the key can be programmed at the same time as the rest of the frame data and setup information.

8.4 Security Coprocessor

The security coprocessor is available to the application software to perform encryption/decryption operations. A hardware implementation of the encryption engine significantly speeds up the processing of the encrypted packets over a pure software implementation. The AES library for the JN5142 provides operations that utilise the encryption engine in the device and allow the contents of memory buffers to be transformed. Information such as the type of security operation to be performed and the encrypt/decrypt key to be used must also be provided.

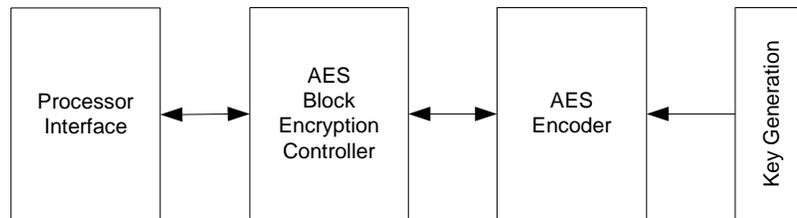


Figure 21: Security Coprocessor Architecture

9 Digital Input/Output

There are 18 Digital I/O (DIO) pins, which can be configured as either an input or an output, and each has a selectable internal pull-up resistor. Most DIO pins are multiplexed with alternate peripheral features of the device, see Section 2.1. Once a peripheral is enabled it takes precedence over the device pins. Refer to the individual module Sections for a full description of the alternate peripherals functions. Following a reset (and whilst the reset input is held low), all peripherals are off and the DIO pins are configured as inputs with the internal pull-ups turned on.

When a peripheral is not enabled, the DIO pins associated with it can be used as digital inputs or outputs. Each pin can be controlled individually by setting the direction and then reading or writing to the pin.

The individual pull-up resistors, R_{PU} , can also be enabled or disabled as needed and the setting is held through sleep cycles. The pull-ups are generally configured once after reset depending on the external components and functionality. For instance, outputs should generally have the pull-ups disabled. An input that is always driven should also have the pull-up disabled.

When configured as an input each pin can be used to generate an interrupt upon a change of state (selectable transition either from low to high or high to low); the interrupt can be enabled or disabled. When the device is sleeping, these interrupts become events that can be used to wake the device up. Equally the status of the interrupt may be read. See Section 18 for further details on sleep and wakeup.

The state of all DIO pins can be read, irrespective of whether the DIO is configured as an input or an output.

Throughout a sleep cycle the direction of the DIO, and the state of the outputs, is held. This is based on the resultant of the GPIO Data/Direction registers and the effect of any enabled peripherals at the point of entering sleep. Following a wake-up these directions and output values are maintained under control of the GPIO data/direction registers. Any peripherals enabled before the sleep cycle are not automatically re-enabled, this must be done through software after the wake-up.

For example, if DIO0 is configured to be SPISEL1 then it becomes an output. The output value is controlled by the SPI functional block. If the device then enters a sleep cycle, the DIO will remain an output and hold the value being output when entering sleep. After wake-up the DIO will still be an output with the same value but controlled from the GPIO Data/Direction registers. It can be altered with the software functions that adjust the DIO, or the application may re-configure it to be SPISEL1.

Unused DIO pins are recommended to be set as inputs with the pull-up enabled.

Two DIO pins can optionally be used to provide control signals for RF circuitry (e.g. switches and PA) in high power range extenders.

DIO3/RFTX is asserted when the radio is in the transmit state and similarly, DIO2/RFRX is asserted when the radio is in the receiver state.

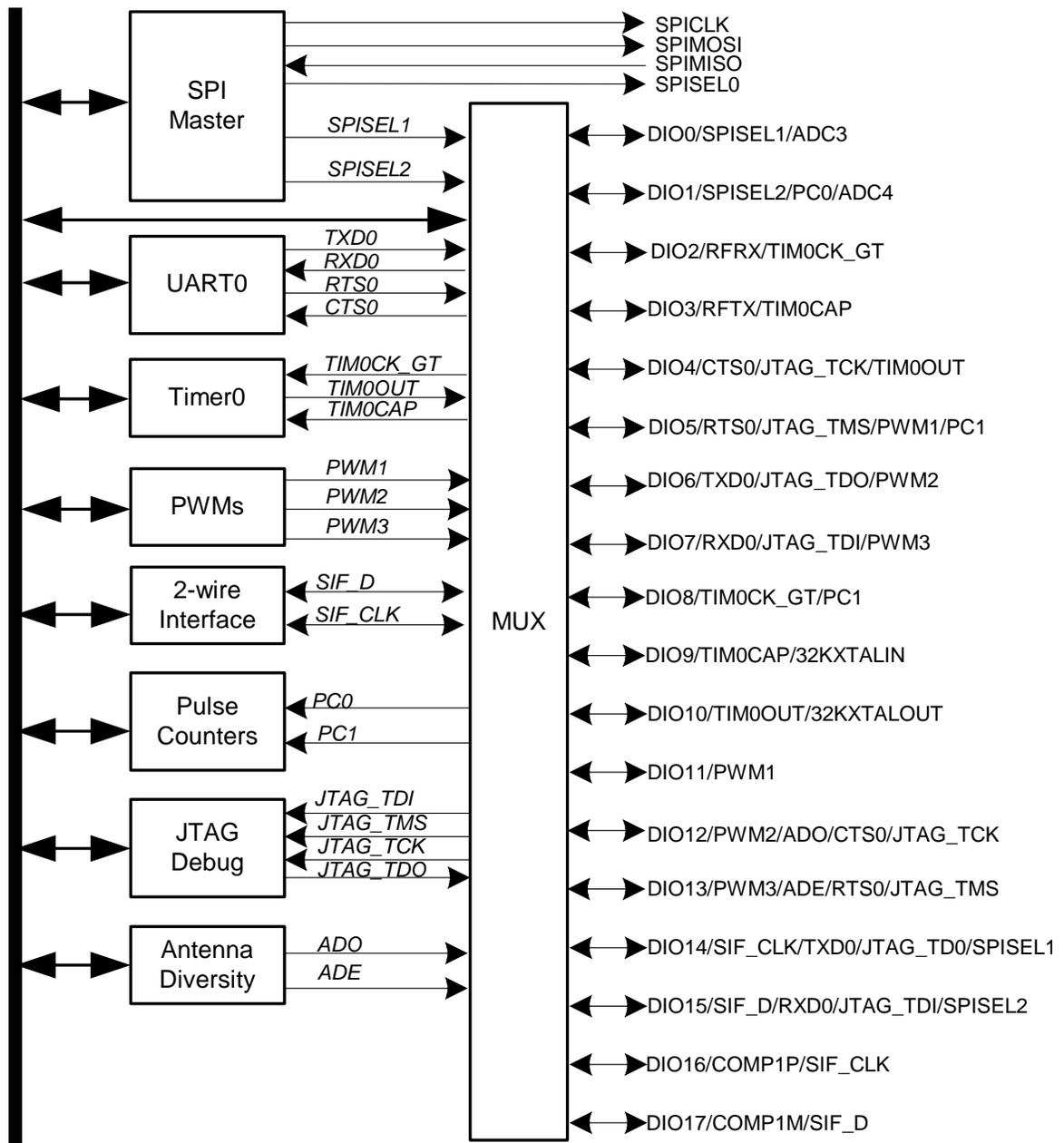


Figure 22: DIO Block Diagram

10 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the JN5142 and peripheral devices. The JN5142 operates as a master on the SPI bus and all other devices connected to the SPI are expected to be slave devices under the control of the JN5142 CPU. The SPI includes the following features:

- Full-duplex, three-wire synchronous data transfer
- Programmable bit rates (up to 16Mbit/s)
- Programmable transaction size up to 32-bits
- Standard SPI modes 0,1,2 and 3
- Manual or Automatic slave select generation (up to 3 slaves)
- Maskable transaction complete interrupt
- LSB First or MSB First Data Transfer
- Supports delayed read edges

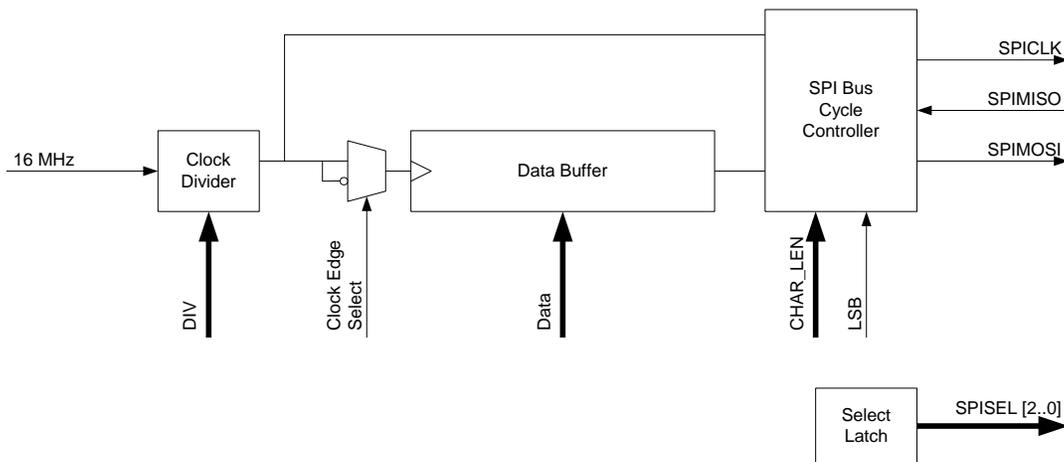


Figure 23: SPI Block Diagram

The SPI bus employs a simple shift register data transfer scheme. Data is clocked out of and into the active devices in a first-in, first-out fashion allowing SPI devices to transmit and receive data simultaneously.

There are three dedicated pins SPICLK, SPIMOSI, SPIMISO that are shared across all devices on the bus. Master-Out-Slave-In or Master-In-Slave-Out data transfer is relative to the clock signal SPICLK generated by the JN5142.

The JN5142 provides three slave selects, SPISEL0 to SPISEL2 to allow three SPI peripherals on the bus. SPISEL0 is a dedicated pin; this is generally connected to a serial Flash/EEPROM memory holding application code that is downloaded to internal RAM via software from reset. SPISEL1 is accessed, depending upon the configuration, on DIO0 or DIO14. SPISEL2 is accessed on DIO1 or DIO15. This is enabled under software control. The following table details which DIO are used for the SPISEL signals depending upon the configuration.

Signal	DIO Assignment	
	Standard pins	Alternative pins
SPISEL1	16	38
SPISEL2	17	40

Table 3: SPISEL IO

The interface can transfer from 1 to 32-bits without software intervention and can keep the slave select lines asserted between transfers when required, to enable longer transfers to be performed.

When the device reset is active, the three outputs SPISEL, SPICLK and SPI_MOSI are tri-stated and SPI_MISO is set to be an input. The pull-up resistors associated with all four pins will be active at this time.

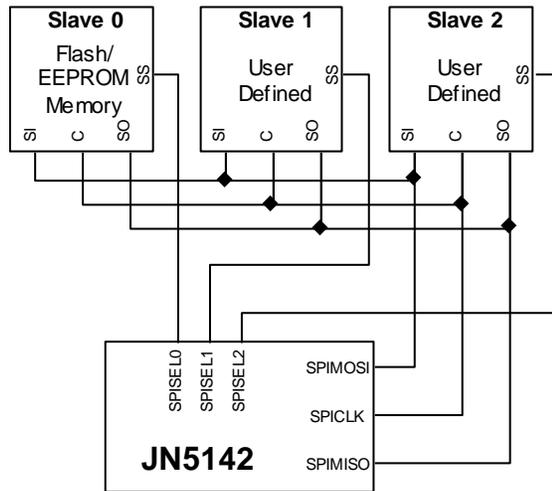


Figure 24: Typical JN5142 SPI Peripheral Connection

The data transfer rate on the SPI bus is determined by the SPICLK signal. The JN5142 supports transfers at selectable data rates from 16MHz to 125kHz selected by a clock divider. Both SPICLK clock phase and polarity are configurable. The clock phase determines which edge of SPICLK is used by the JN5142 to present new data on the SPIMOSI line; the opposite edge will be used to read data from the SPIMISO line. The interface should be configured appropriately for the SPI slave being accessed.

SPICLK		Mode	Description
Polarity (CPOL)	Phase (CPHA)		
0	0	0	SPICLK is low when idle – the first edge is positive. Valid data is output on SPIMOSI before the first clock and changes every negative edge. SPIMISO is sampled every positive edge.
0	1	1	SPICLK is low when idle – the first edge is positive. Valid data is output on SPIMOSI every positive edge. SPIMISO is sampled every negative edge.
1	0	2	SPICLK is high when idle – the first edge is negative. Valid data is output on SPIMOSI before the first clock edge and is changed every positive edge. SPIMISO is sampled every negative edge.
1	1	3	SPICLK is high when idle – the first edge is negative. Valid data is output on SPIMOSI every negative edge. SPIMISO is sampled every positive edge.

Table 4: SPI Configurations

If more than one SPISEL line is to be used in a system they must be used in numerical order starting from SPISEL0. A SPISEL line can be automatically de-asserted between transactions if required, or it may stay asserted over a number of transactions. For devices such as memories where a large amount of data can be received by the master by continually providing SPICLK transitions, the ability for the select line to stay asserted is an advantage since it keeps the slave enabled over the whole of the transfer.

A transaction commences with the SPI bus being set to the correct configuration, and then the slave device is selected. Upon commencement of transmission (1 to 32 bits) data is placed in the FIFO data buffer and clocked out, at the same time generating the corresponding SPICLK transitions. Since the transfer is full-duplex, the same number of data bits is being received from the slave as it transmits. The data that is received during this transmission can be read (1 to 32 bits). If the master simply needs to provide a number of SPICLK transitions to allow data to be

sent from a slave, it should perform transmit using dummy data. An interrupt can be generated when the transaction has completed or alternatively the interface can be polled.

If a slave device wishes to signal the JN5142 indicating that it has data to provide, it may be connected to one of the DIO pins that can be enabled as an interrupt.

Figure 25 shows a complex SPI transfer, reading data from a FLASH device, that can be achieved using the SPI master interface. The slave select line must stay low for many separate SPI accesses, and therefore manual slave select mode must be used. The required slave select can then be asserted (active low) at the start of the transfer. A sequence 8 and 32 bit transfers can be used to issue the command and address to the FLASH device and then to read data back. Finally, the slave select can be deselected to end the transaction.

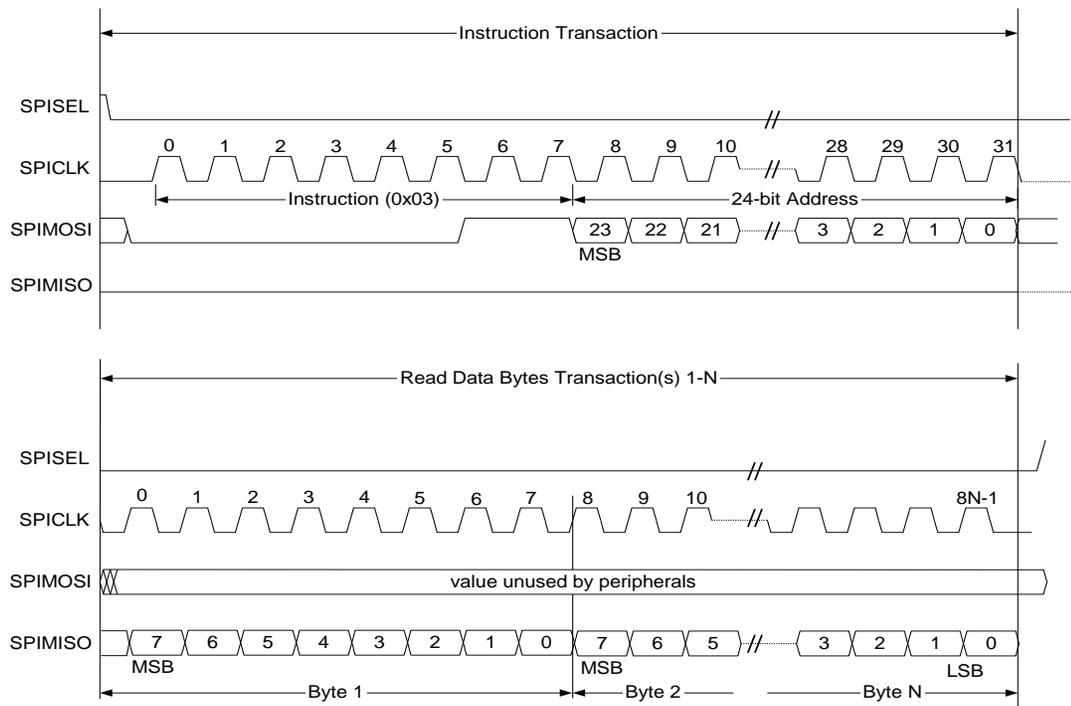


Figure 25: Example SPI Waveforms – Reading from FLASH Device using Mode 0

11 Timers

11.1 Peripheral Timer/Counters

A general-purpose timer/counter unit, Timer0, is available that can be configured to operate in one of five possible modes. This has:

- 5-bit prescaler, divides system clock by $2^{\text{prescale value}}$ as the clock to the timer (prescaler range is 0 to 16)
- Clocked from internal system clock (16MHz)
- 16-bit counter, 16-bit Rise and Fall (period) registers
- Timer: can generate interrupts off Rise and Fall counts. Can be gated by external signal
- Counter: counts number of transitions on external event signal. Can use low-high, high-low or both transitions
- PWM/Single pulse: outputs repeating Pulse Width Modulation signal or a single pulse. Can set period and mark-space ratio
- Capture: measures times between transitions of an applied signal
- Delta-Sigma: Return-To-Zero (RTZ) and Non-Return-to-Zero (NRZ) modes
- Timer usage of external IO can be controlled on a pin by pin basis

Three further timers are also available that support the same functionality but have no Counter or Capture mode. Additionally, is not possible to gate these three timers with an external signal.

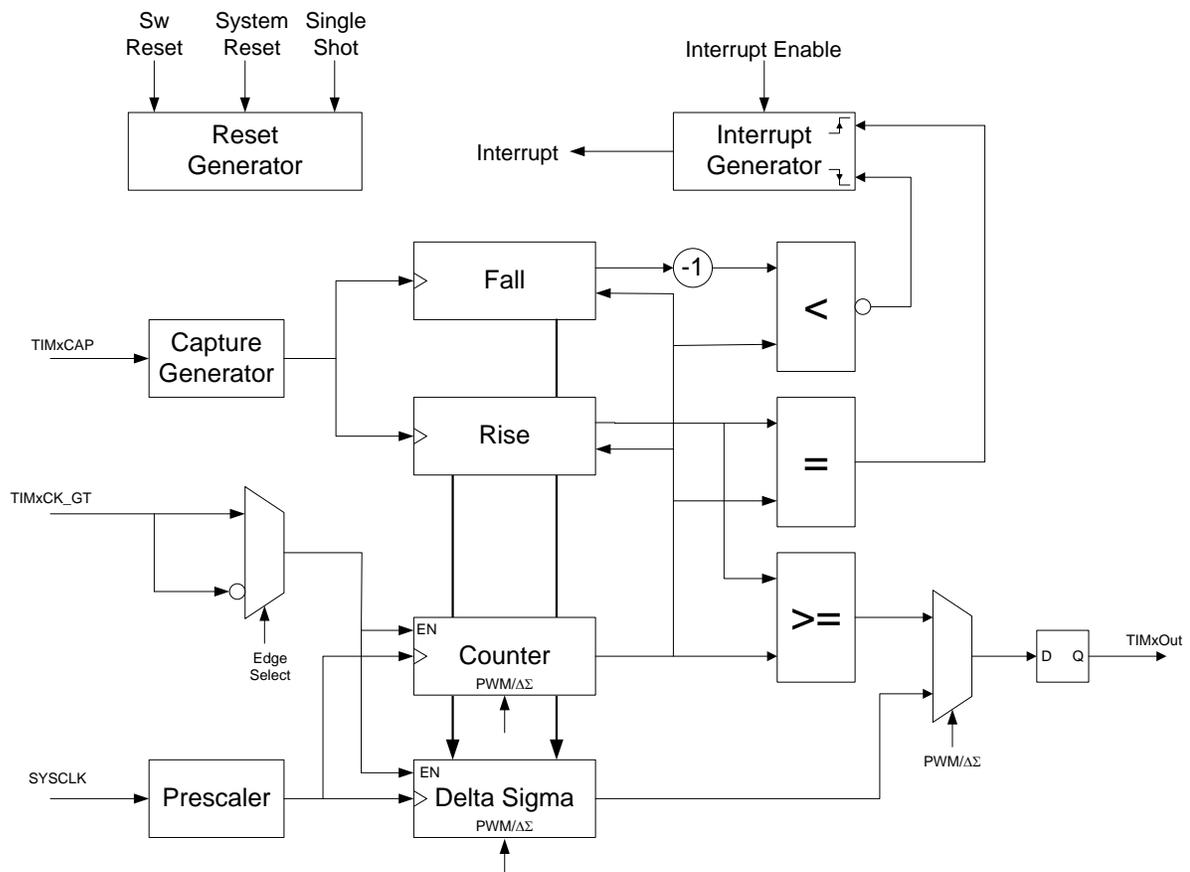


Figure 26: Timer Unit Block Diagram

The clock source for the Timer0 unit is fed from the 16MHz system clock. This clock passes to a 5-bit prescaler where a value of 0 leaves the clock unmodified and other values divide it by 2^{prescale} value. For example, a prescale value of 2 applied to the 16MHz system clock source results in a timer clock of 4MHz.

The counter is optionally gated by a signal on the clock/gate input (TIM0CK_GT). If the gate function is selected, then the counter is frozen when the clock/gate input is high.

An interrupt can be generated whenever the counter is equal to the value in either of the High or Low registers.

The internal Output Enable (OE) signal enables or disables the timer output.

Timer0 can be accessed, depending upon the configuration, on DIO8 to DIO10 or DIO2 to DIO4. PWM1,2,3 can be accessed on DIO11 to DIO13 or DIO5 to DIO7. This is enabled under software control. Timer0 can be assigned to its alternative location without moving the PWMs, and vice-versa. The following table details which DIO are used for the PWM depending upon the configuration.

Signal	DIO Assignment	
	Standard pins	Alternative pins
TIM0CK_GT	31	18
TIM0CAP	32	19
TIM0OUT	33	26
PWM1	34	27
PWM2	36	28
PWM3	37	29

Table 5: Timer and PWM IO

If operating in timer mode it is not necessary to use any of the DIO pins, allowing the standard DIO functionality to be available to the application.

11.1.1 Pulse Width Modulation Mode

Pulse Width Modulation (PWM) mode, as used by PWM timers 1,2 and 3 and optionally by Timer0, allows the user to specify an overall cycle time and pulse length within the cycle. The pulse can be generated either as a single shot or as a train of pulses with a repetition rate determined by the cycle time.

In this mode, the cycle time and low periods of the PWM output signal can be set by the values of two independent 16-bit registers (Fall and Rise). The counter increments and its output is compared to the 16-bit Rise and Fall registers. When the counter is equal to the Rise register, the PWM output is set to high; when the counter reaches the Fall value, the output returns to low. In continuous mode, when the counter reaches the Fall value, it will reset and the cycle repeats. The PWM waveform is available on PWM1,2,3 or TIM0OUT when the output driver is enabled.

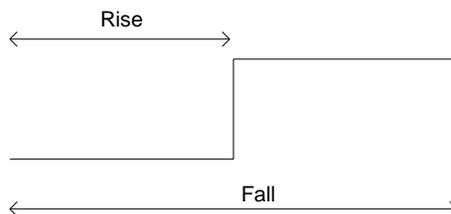


Figure 27: PWM Output Timings

11.1.2 Capture Mode

The capture mode can be used to measure the time between transitions of a signal applied to the capture input (TIM0CAP). When the capture is started, on the next low-to-high transition of the captured signal, the count value is stored in the Rise register, and on the following high-to-low transition, the counter value is stored in the Fall register. The pulse width is the difference in counts in the two registers multiplied by the period of the prescaled clock. Upon reading the capture registers the counter is stopped. The values in the High and Low registers will be updated whenever there is a corresponding transition on the capture input, and the value stored will be relative to when the

mode was started. Therefore, if multiple pulses are seen on TIM0CAP before the counter is stopped only the last pulse width will be stored.

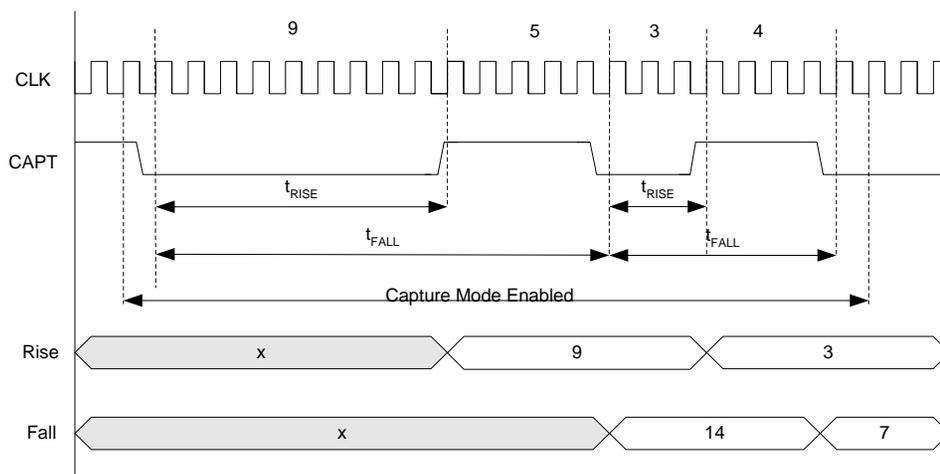


Figure 28: Capture Mode

11.1.3 Counter/Timer Mode

The counter/timer can be used to generate interrupts, based on the timers or event counting, for software to use. As a timer the clock source is from the system clock, prescaled if required. The timer period is programmed into the Fall register and the Fall register match interrupt enabled. The timer is started as either a single-shot or a repeating timer, and generates an interrupt when the counter reaches the Fall register value.

When used to count external events on TIM0CK_GT the clock source is selected from the input pin and the number of events programmed into the Fall register. The Fall register match interrupt is enabled and the counter started, usually in single shot mode. An interrupt is generated when the programmed number of transitions is seen on the input pin. The transitions counted can be configured to be rising, falling or both rising and falling edges.

Edges on the event signal must be at least 100nsec apart, i.e. pulses must be wider than 100nsec.

11.1.4 Delta-Sigma Mode

A separate delta-sigma mode is available, allowing a low speed delta-sigma DAC to be implemented with up to 16-bit resolution. This requires that a resistor-capacitor network is placed between the output DIO pin and digital ground. A stream of pulses with digital voltage levels is generated which is integrated by the RC network to give an analogue voltage. A conversion time is defined in terms of a number of clock cycles. The width of the pulses generated is the period of a clock cycle. The number of pulses output in the cycle, together with the integrator RC values, will determine the resulting analogue voltage. For example, generating approximately half the number of pulses that make up a complete conversion period will produce a voltage on the RC output of $VDD1/2$, provided the RC time constant is chosen correctly. During a conversion, the pulses will be pseudo-randomly dispersed throughout the cycle in order to produce a steady voltage on the output of the RC network.

The output signal is asserted for the number of clock periods defined in the High register, with the total period being 2^{16} cycles. For the same value in the High register, the pattern of pulses on subsequent cycles is different, due to the pseudo-random distribution.

The delta-sigma converter output can operate in a Return-To-Zero (RTZ) or a Non-Return-to-Zero (NRZ) mode. The NRZ mode will allow several pulses to be output next to each other. The RTZ mode ensures that each pulse is separated from the next by at least one period. This improves linearity if the rise and fall times of the output are different to one another. Essentially, the output signal is low on every other output clock period, and the conversion cycle time is twice the NRZ cycle time i.e. 2^{17} clocks. The integrated output will only reach half $VDD2$ in RTZ mode, since even at full scale only half the cycle contains pulses. Figure 29 and Figure 30 illustrate the difference between RTZ and NRZ for the same programmed number of pulses.

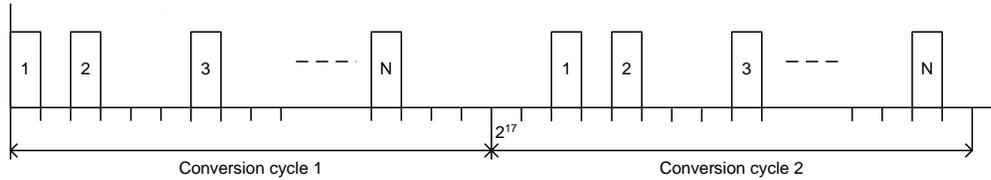


Figure 29: Return To Zero Mode in Operation

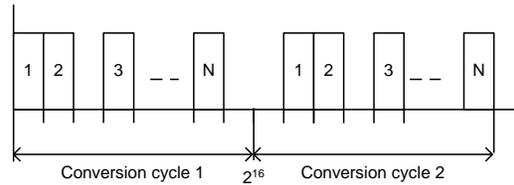


Figure 30: Non-Return to Zero Mode

11.1.5 Example Timer/Counter Application

Figure 31 shows an application of the JN5142 timers to provide closed loop speed control. Timer 0 is configured in PWM mode to provide a variable mark-space ratio switching waveform to the gate of the NFET. This in turn controls the power in the DC motor.

Timer 1 is configured to count the rising edge events on the clk/gate pin over a constant period. This converts the tacho pulse stream output into a count proportional to the motor speed. This value is then used by the application software executing the control algorithm.

If required for other functionality, then the unused IO associated with the timers could be used as general purpose DIO.

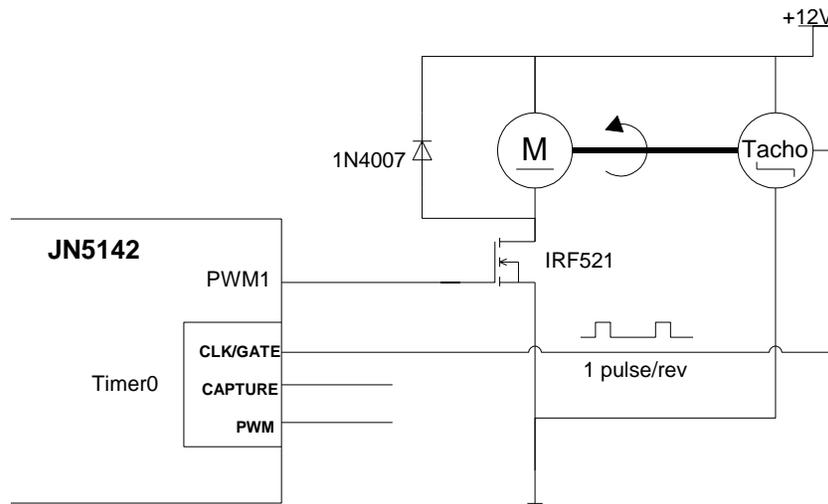


Figure 31: Closed Loop PWM Speed Control Using JN5142 Timers

11.2 Tick Timer

The JN5142 contains a hardware timer that can be used for generating timing interrupts to software. It may be used to implement regular events such as ticks for software timers or an operating system, as a high-precision timing reference or can be used to implement system monitor timeouts as used in a watchdog timer. Features include:

- 32-bit counter

- 28-bit match value
- Maskable timer interrupt
- Single-shot, Restartable or Continuous modes of operation

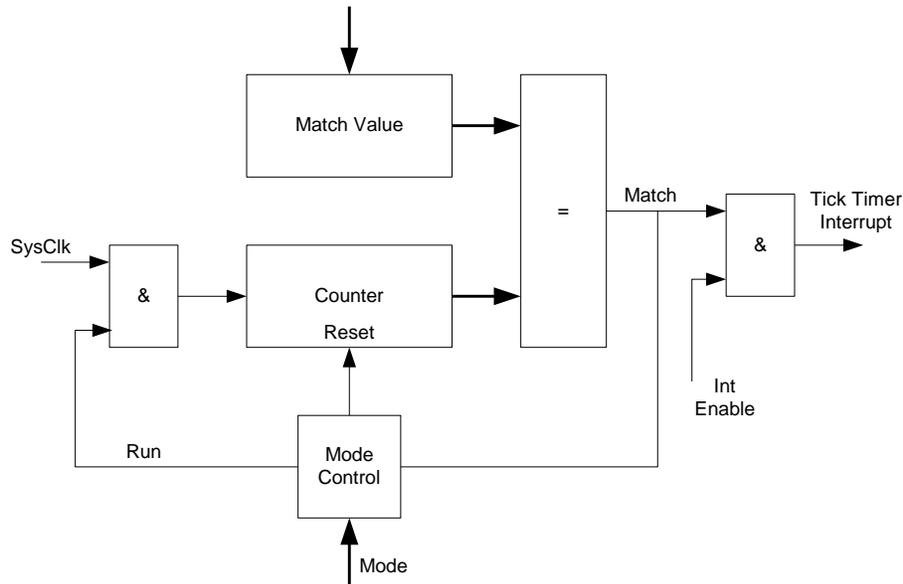


Figure 32: Tick Timer

The Tick Timer is clocked from a continuous 16MHz clock, which is fed to a 32-bit wide resettable up-counter, gated by a signal from the mode control block. A match register allows comparison between the counter and a programmed value. The match value, measured in 16MHz clock cycles is programmed through software, in the range 0 to 0x0FFFFFFF. The output of the comparison can be used to generate an interrupt if the interrupt is enabled and used in controlling the counter in the different modes. Upon configuring the timer mode, the counter is also reset.

If the mode is programmed as single shot, the counter begins to count from zero until the match value is reached. The match signal will be generated which will cause an interrupt if enabled, and the counter will stop counting. The counter is restarted by reprogramming the mode.

If the mode is programmed as restartable, the operation of the counter is the same as for the single shot mode, except that when the match value is reached the counter is reset and begins counting from zero. An interrupt will be generated when the match value is reached if it is enabled.

Continuous mode operation is similar to restartable, except that when the match value is reached, the counter is not reset but continues to count. An interrupt will be generated when the match value is reached if enabled.

11.3 Wakeup Timers

Two 35-bit wakeup timers are available in the JN5142 driven from the 32kHz internal clock. They may run during sleep periods when the majority of the rest of the device is powered down, to time sleep periods or other long period timings that may be required by the application. The wakeup timers do not run during deep sleep and may optionally be disabled in sleep mode through software control. When a wakeup timer expires it typically generates an interrupt, if the device is asleep then the interrupt may be used as an event to end the sleep period. See Section 18 for further details on how they are used during sleep periods. Features include:

- 35-bit down-counter
- Optionally runs during sleep periods
- Clocked by 32kHz system clock; either 32kHz RC oscillator, 32kHz XTAL oscillator or 32kHz clock input

A wakeup timer consists of a 35-bit down counter clocked from the selected 32 kHz clock. An interrupt or wakeup event can be generated when the counter reaches zero. On reaching zero the counter will continue to count down until stopped, which allows the latency in responding to the interrupt to be measured. If an interrupt or wakeup event is required, the timer interrupt should be enabled before loading the count value for the period. Once the count value is loaded and counter started, the counter begins to count down; the counter can be stopped at any time through software control. The counter will remain at the value it contained when the timer was stopped and no interrupt will be generated. The status of the timers can be read to indicate if the timers are running and/or have expired; this is useful when the timer interrupts are masked. This operation will reset any expired status flags.

11.3.1 RC Oscillator Calibration

The RC oscillator that can be used to time sleep periods is designed to require very little power to operate and be self-contained, requiring no external timing components and hence is lower cost. As a consequence of using on-chip resistors and capacitors, the inherent absolute accuracy and temperature coefficient is lower than that of a crystal oscillator, but once calibrated the accuracy approaches that of a crystal oscillator. Sleep time periods should be as close to the desired time as possible in order to allow the device to wake up in time for important events, for example beacon transmissions in the IEEE802.15.4 protocol. If the sleep time is accurate, the device can be programmed to wake up very close to the calculated time of the event and so keep current consumption to a minimum. If the sleep time is less accurate, it will be necessary to wake up earlier in order to be certain the event will be captured. If the device wakes earlier, it will be awake for longer and so reduce battery life.

In order to allow sleep time periods to be as close to the desired length as possible, the true frequency of the RC oscillator needs to be determined to better than the initial 30% accuracy. The calibration factor can then be used to calculate the true number of nominal 32kHz periods needed to make up a particular sleep time. A calibration reference counter, clocked from the 16MHz system clock, is provided to allow comparisons to be made between the 32kHz RC clock and the 16MHz system clock when the JN5142 is awake.

Wakeup timer0 counts for a set number of 32kHz clock periods during which time the reference counter runs. When the wakeup timer reaches zero the reference counter is stopped, allowing software to read the number of 16MHz clock ticks generated during the time represented by the number of 32kHz ticks programmed in the wakeup timer. The true period of the 32kHz clock can thus be determined and used when programming a wakeup timer to achieve a better accuracy and hence more accurate sleep periods

For a RC oscillator running at exactly 32,000Hz the value returned by the calibration procedure should be 10000, for a calibration period of twenty 32,000Hz clock periods. If the oscillator is running faster than 32,000Hz the count will be less than 10000, if running slower the value will be higher. For a calibration count of 9000, indicating that the RC oscillator period is running at approximately 35kHz, to time for a period of 2 seconds the timer should be loaded with 71,111 $((10000/9000) \times (32000 \times 2))$ rather than 64000.

12 Pulse Counters

Two 16-bit counters are provided that can increment during all modes of operation (including sleep). The first, PC0, increments from pulses received on DIO1. The other pulse counter, PC1, can also be accessed on DIO5 or DIO8 depending upon the configuration. This is enabled under software control. The pulses can be de-bounced using the 32kHz clock to guard against false counting on slow or noisy edges. Increments occur from a configurable rising or falling edge on the respective DIO input.

Each counter has an associated 16-bit reference that is loaded by the user. An interrupt (and wakeup event if asleep) may be generated when a counter reaches its pre-configured reference value. The two counters may optionally be cascaded together to provide a single 32-bit counter, linked to DIO1. The counters do not saturate at 65535, but naturally roll-over to 0. Additionally, the pulse counting continues when the reference value is reached without software interaction so that pulses are not missed even if there is a long delay before an interrupt is serviced or during the wakeup process.

The system can work with signals up to 100kHz, with no debounce, or from 5.3kHz to 1.7kHz with debounce. When using debounce the 32kHz clock must be active, so for minimum sleep currents the debounce mode should not be used.

13 Serial Communications

The JN5142 has a Universal Asynchronous Receiver/Transmitter (UART) serial communication interface. It provides similar operating features to the industry standard 16550A device operating in FIFO mode. The interface performs serial-to-parallel conversion on incoming serial data and parallel-to-serial conversion on outgoing data from the CPU to external devices. In both directions, a 16-byte deep FIFO buffer allows the CPU to read and write multiple characters on each transaction. This means that the CPU is freed from handling data on a character-by-character basis, with the associated high processor overhead. The UART has the following features:

- Emulates behaviour of industry standard NS16450 and NS16550A UARTs
- 16 byte transmit and receive FIFO buffers reduce interrupts to CPU, with direct access to fill levels of each
- Adds/deletes standard start, stop and parity communication bits to or from the serial data
- Independently controlled transmit, receive, status and data sent interrupts
- Optional modem flow control signals CTS and RTS
- Fully programmable data formats: baud rate, start, stop and parity settings
- False start bit detection, parity, framing and FIFO overrun error detect and break indication
- Internal diagnostic capabilities: loop-back controls for communications link fault isolation
- Flow control by software or automatically by hardware

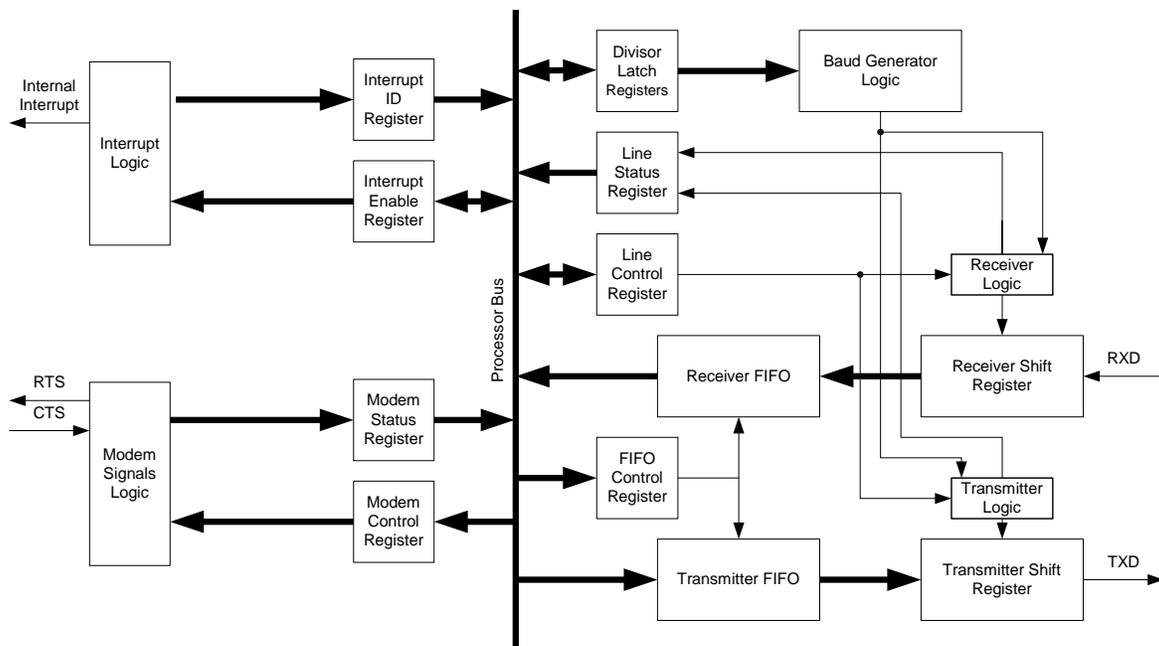


Figure 33: UART Block Diagram

The serial interface contains programmable fields that can be used to set number of data bits (5, 6, 7 or 8), even, odd, set-at-1, set-at-0 or no-parity detection and generation of single or multiple stop bit, (for 5 bit data, multiple is 1.5 stop bits; for 6, 7 or 8 data bits, multiple is 2 bits).

The baud rate is programmable up to 1Mbps, standard baud rates such as 4800, 9600, 19.2k, 38.4k etc. can be configured.

For applications requiring hardware flow control, two control signals are provided: Clear-To-Send (CTS) and Request-To-Send (RTS). CTS is an indication sent by an external device to the UART that it is ready to receive data. RTS is an indication sent by the UART to the external device that it is ready to receive data. RTS is controlled from software, while the value of CTS can be read. Monitoring and control of CTS and RTS is a software activity, normally performed as part of interrupt processing. The signals do not control parts of the UART hardware, but simply indicate to software the state of the UART external interface. Alternatively, the Automatic Flow Control mode can be set

where the hardware controls the value of the generated RTS (negated if the receive FIFO fill level is greater than a programmable threshold of 8, 11, 13 or 15 bytes), and only transmits data when the incoming CTS is asserted.

Software can read characters, one byte at a time, from the Receive FIFO and can also write to the Transmit FIFO, one byte at a time. The Transmit and Receive FIFOs can be cleared and reset independently of each other. The status of the transmitter can be checked to see if it is empty, and if there is a character being transmitted. The status of the receiver can also be checked, indicating if conditions such as parity error, framing error or break indication have occurred. It also shows if an overrun error occurred (receive buffer full and another character arrives) and if there is data held in the receive FIFO.

The UART is accessed, depending upon the configuration, on DIO4 to DIO7 or DIO12 to DIO15. This is enabled under software control. The following table details which DIO are used for the UART depending upon the configuration.

Signal	DIO Assignment	
	Standard pins	Alternative pins
CTS0	26	36
RTS0	27	37
TXD0	28	38
RXD0	29	40

Table 6: UART IO

If CTS and RTS are not required on the device's external pins, then they may be disabled, this allows the DIOx function to be used for other purposes.

Note: With the automatic flow control threshold set to 15, the hardware flow control within the UART block negates RTS when the receive FIFO is about to become full. In some instances it has been observed that remote devices that are transmitting data do not respond quickly enough to the de-asserted CTS and continue to transmit data. In these instances the data will be lost in a receive FIFO overflow.

13.1 Interrupts

Interrupt generation can be controlled for the UART block, and is divided into four categories:

- Received Data Available: Is set when data in the Rx FIFO queue reaches a particular level (the trigger level can be configured as 1, 4, 8 or 14) or if no character has been received for 4 character times.
- Transmit FIFO Empty: set when the last character from the Tx FIFO is read and starts to be transmitted.
- Receiver Line Status: set when one of the following occur (1) Parity Error - the character at the head of the receive FIFO has been received with a parity error, (2) Overrun Error - the Rx FIFO is full and another character has been received at the Receiver shift register, (3) Framing Error - the character at the head of the receive FIFO does not have a valid stop bit and (4) Break Interrupt – occurs when the RxD line has been held low for an entire character.
- Modem Status: Generated when the CTS (Clear To Send) input control line changes.

13.2 UART Application

The following example shows the UART connected to a 9-pin connector compatible with a PC. As the JN5142 device pins do not provide the RS232 line voltage, a level shifter is used.

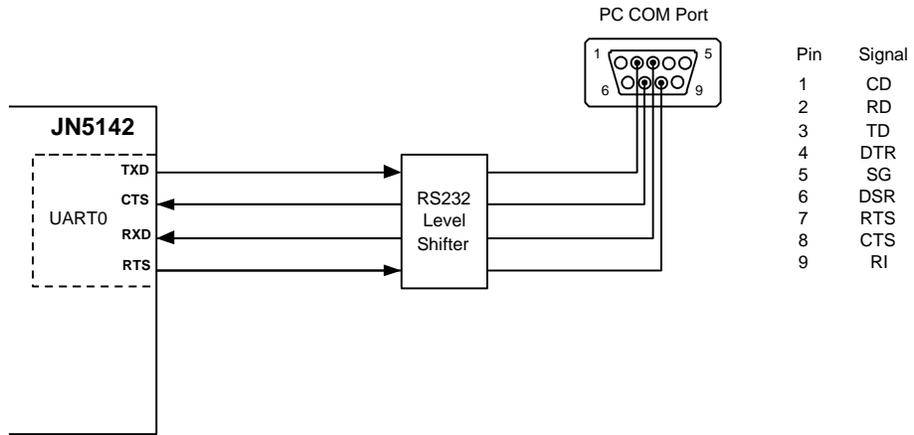


Figure 34: JN5142 Serial Communication Link

14 JTAG Debug Interface

The JN5142 includes an IEEE1149.1 compliant JTAG port for the sole purpose of software code debug with the Software Development Kit. The JTAG interface is disabled by default and is enabled under software control. Therefore, debugging is only possible if enabled by the application. Once enabled, the application executes as normal until the external debugger controller initiates debug activity.

The Debugger supports breakpoints and watchpoints based on four comparisons between any of program counter, load/store effective address and load/store data. There is the ability to chain the comparisons together. There is also the ability, under debugger control to perform the following commands: go, stop, reset, step over/into/out/next, run to cursor and breakpoints. In addition, under control of the debugger, it is possible to:

- Read and write registers on the wishbone bus
- Read ROM and RAM, and write to RAM
- Read and write CPU internal registers

The Debugger interface is accessed, depending upon the configuration, through the standard or alternative pins used for UART0. This is enabled under software control and is dealt with in [4]. The following table details which DIO are used for the JTAG interface depending upon the configuration.

Signal	DIO Assignment	
	Standard pins	Alternative pins
clock (TCK)	26	36
control (TMS)	27	37
data out (TDO)	28	38
data in (TDI)	29	40

Table 7: Hardware Debugger IO

If doze mode is active when debugging is started, the processor will be woken and then respond to debugger commands. It is not possible to wake the device from sleep using the debug interface and debugging is not available while the device is sleeping.

When using the debug interface, program execution is halted, and control of the CPU is handed to the debugger. The watchdog, tick timer and the timers described in Section 11 are stalled while the debugger is in control of the CPU.

When control is handed from the CPU to the debugger or back a small number of CPU clock cycles are taken flushing or reloading the CPU pipeline. Because of this, when a program is halted by the debugger and then restarted again, a small number of tick timer cycles will elapse.

It is possible to prevent all hardware debugging by blowing the relevant Efuse bit. For further information on how to program the eFuse, please contact technical support via the on-line tech-support system.

The JTAG interface does not support boundary scan testing. It is recommended that the JN5142 is not connected as part of the board scan chain.

15 Two-Wire Serial Interface (I²C)

The JN5142 includes industry standard I²C two-wire synchronous Serial Interface operates as a Master (MSIF) or Slave (SSIF) that provides a simple and efficient method of data exchange between devices. The system uses a serial data line (SIF_D) and a serial clock line (SIF_CLK) to perform bi-directional data transfers and includes the following features:

Common to both master and slave:

- Compatible with both I²C and SMBus peripherals
- Support for 7 and 10-bit addressing modes
- Optional pulse suppression on signal inputs

Master only:

- Multi-master operation
- Software programmable clock frequency
- Clock stretching and wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Bus busy detection

Slave only:

- Programmable slave address
- Simple byte level transfer protocol
- Write data flow control with optional clock stretching or acknowledge mechanism
- Read data preloaded or provided as required

The Serial Interface is accessed, depending upon the configuration, DIO14 and DIO15 or DIO16 and DIO17. This is enabled under software control. The following table details which DIO are used for the Serial Interface depending upon the configuration.

Signal	DIO Assignment	
	Standard pins	Alternative pins
SIF_CLK	38	1
SIF_D	40	2

Table 8: Two-Wire Serial Interface IO

15.1 Connecting Devices

The clock and data lines, SIF_D and SIF_CLK, are alternate functions of DIO15 and DIO14 respectively. The serial interface function of these pins is selected when the interface is enabled. They are both bi-directional lines, connected internally to the positive supply voltage via weak (45k Ω) programmable pull-up resistors. However, it is recommended that external 4.7k Ω pull-ups be used for reliable operation at high bus speeds, as shown in Figure 35. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. The number of devices connected to the bus is solely dependent on the bus capacitance limit of 400pF.

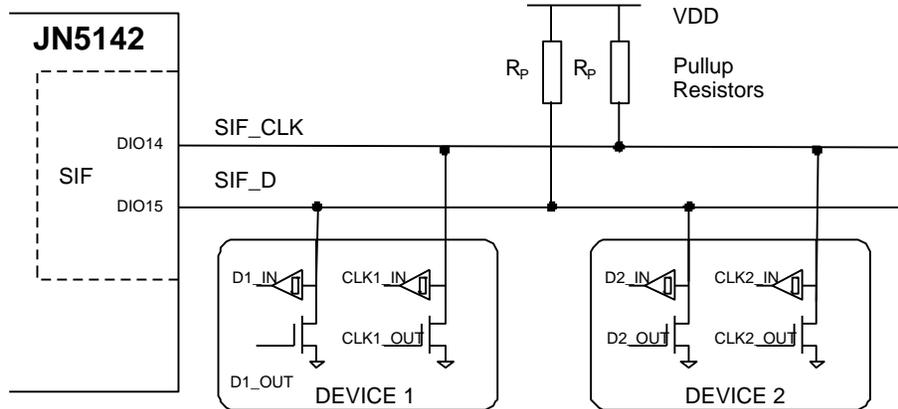


Figure 35: Connection Details

15.2 Clock Stretching

Slave devices can use clock stretching to slow down the transfer bit rate. After the master has driven SIF_CLK low, the slave can drive SIF_CLK low for the required period and then release it. If the slave's SIF_CLK low period is greater than the master's low period the resulting SIF_CLK bus signal low period is stretched thus inserting wait states.

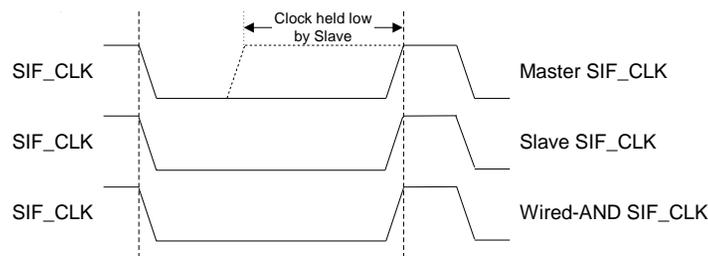


Figure 36: Clock Stretching

15.3 Master Two-wire Serial Interface

When operating as a master device, it provides the clock signal and a prescale register determines the clock rate, allowing operation up to 400kbit/s.

Data transfer is controlled from the processor bus interface at a byte level, with the processor responsible for indicating when start, stop, read, write and acknowledge control should be generated. Write data written into a transmit buffer will be written out across the two-wire interface when indicated, and read data received on the interface is made available in a receive buffer. Indication of when a particular transfer has completed may be indicated by means of an interrupt or by polling a status bit.

The first byte of data transferred by the device after a start bit is the slave address. The JN5142 supports both 7-bit and 10-bit slave addresses by generating either one or two address transfers. Only the slave with a matching address will respond by returning an acknowledge bit.

The master interface provides a true multi-master bus including collision detection and arbitration that prevents data corruption. If two or more masters simultaneously try to control the bus, a clock synchronization procedure determines the bus clock. Because of the wired-AND connection of the interface, a high-to-low transition on the bus affects all connected devices. This means a high-to-low transition on the SIF_CLK line causes all concerned devices to count off their low period. Once the clock input of a device has gone low, it will hold the SIF_CLK line in that state until the clock high state is reached when it releases the SIF_CLK line. Due to the wired-AND connection, the SIF_CLK line will therefore be held low by the device with the longest low period, and held high by the device with the shortest high period.

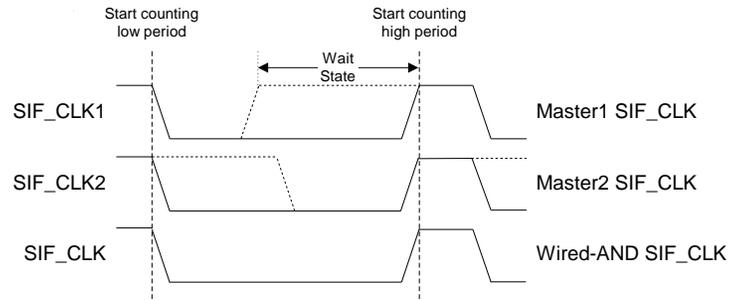


Figure 37: Multi-Master Clock Synchronisation

After each transfer has completed, the status of the device must be checked to ensure that the data has been acknowledged correctly, and that there has been no loss of arbitration. (N.B. Loss of arbitration may occur at any point during the transfer, including data cycles). An interrupt will be generated when arbitration has been lost.

15.4 Slave Two-wire Serial Interface

When operating as a slave device, the interface does not provide a clock signal, although it may drive the clock signal low if it is required to apply clock stretching.

Only transfers whose address matches the value programmed into the interface's address register are accepted. The interface allows both 7 and 10 bit addresses to be programmed, but only responds with an acknowledge to a single address. Addresses defined as "reserved" will not be responded to, and should not be programmed into the address register. A list of reserved addresses is shown in Table 9.

Address	Name	Behaviour
0000 000	General Call/Start Byte	Ignored
0000 001	CBUS address	Ignored
0000 010	Reserved	Ignored
0000 011	Reserved	Ignored
0000 1XX	Hs-mode master code	Ignored
1111 1XX	Reserved	Ignored
1111 0XX	10-bit address	Only responded to if 10 bit address set in address register

Table 9 : List of two-wire serial interface reserved addresses

Data transfer is controlled from the processor bus interface at a byte level, with the processor responsible for taking write data from a receive buffer and providing read data to a transmit buffer when indicated. A series of interrupt status bits are provided to control the flow of data.

For writes, in to the slave interface, it is important that data is taken from the receive buffer by the processor before the next byte of data arrives. To enable this, the interface may be configured to work in two possible backoff modes:

- Not Acknowledge mode – where the interface returns a Not Acknowledge (NACK) to the master if more data is received before the previous data has been taken. This will lead to the termination of the current data transfer.
- Clock Stretching mode – where the interface holds the clock line low until the previous data has been taken. This will occur after transfer of the next data but before issuing an acknowledge

For reads, from the slave interface, the data may be preloaded into the transmit buffer when it is empty (i.e. at the start of day, or when the last data has been read), or fetched each time a read transfer is requested. When using data preload, read data in the buffer must be replenished following a data write, as the transmit and received data is contained in a shared buffer. The interface will hold the bus using clock stretching when the transmit buffer is empty.

Interrupts may be triggered when:

- Data Buffer read data is required – a byte of data to be read should be provided to avoid the interface from clock stretching
- Data Buffer read data has been taken – this indicates when the next data may be preloaded into the data buffer
- Data Buffer write data is available – a byte of data should be taken from the data buffer to avoid data backoff as defined above
- The last data in a transfer has completed – i.e. the end of a burst of data, when a Stop or Restart is seen
- A protocol error has been spotted on the interface

16 Random Number Generator

A random number generator is provided which creates a 16-bit random number each time it is invoked. Consecutive calls can be made to build up any length of random number required. Each call takes approximately 0.25msec to complete. Alternatively, continuous generation mode can be used where a new number is generated approximately every 0.25msec. In either mode of operation an interrupt can be generated to indicate when the number is available, or a status bit can be polled.

The random bits are generated by sampling the state of the 32MHz clock every 32kHz system clock edge. As these clocks are asynchronous to each other, each sampled bit is unpredictable and hence random.

17 Analogue Peripherals

The JN5142 contains a number of analogue peripherals allowing the direct connection of a wide range of external sensors and switches.

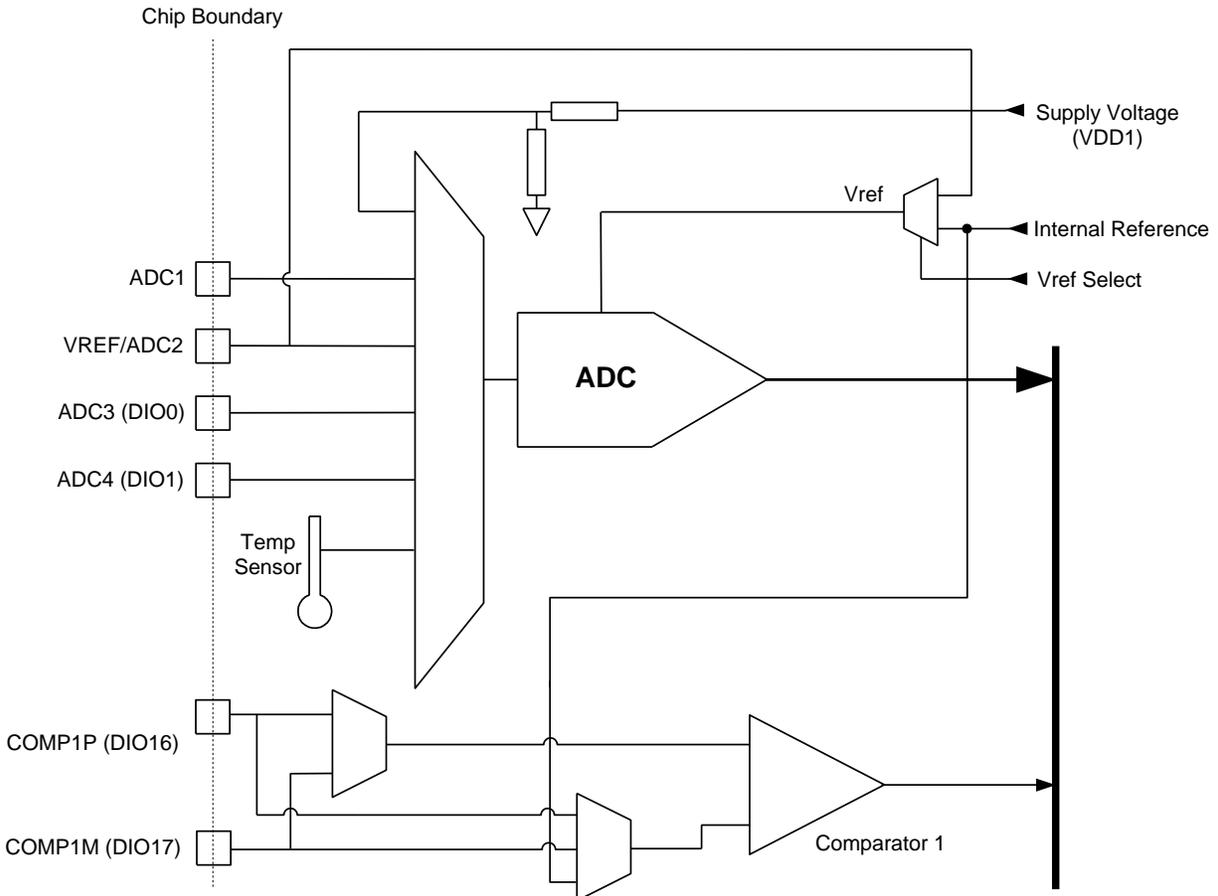


Figure 38: Analogue Peripherals

In order to provide good isolation from digital noise, the analogue peripherals and radio are powered by the radio regulator, which is supplied from the analogue supply VDD1 and referenced to analogue ground VSSA.

A reference signal Vref for the ADC can be selected between an internal bandgap reference or an external voltage reference supplied to the VREF pin. ADC input 2 cannot be used if an external reference is required as this uses the same pin as VREF. Note also that ADC3 and ADC4 use the same pins as DIO0/SPISEL1 and DIO1/SPISEL2 respectively. These pins can only be used for the ADC if they are not required for their alternative functions. Similarly, the comparator inputs are shared with DIO16/SIF_CLK and DIO17/SIF_D. If used for their analogue functions, these DIOs must be put into a passive state by setting them to Inputs with their pull-ups disabled.

The ADC is clocked from a common clock source derived from the 16MHz clock

17.1 Analogue to Digital Converter

The 8-bit analogue to digital converter (ADC) uses a successive approximation design to perform high accuracy conversions as typically required in wireless sensor network applications. It has six multiplexed single-ended input channels: four available externally, one connected to an internal temperature sensor, and one connected to an internal supply monitoring circuit.

17.1.1 Operation

The input range of the ADC can be set between 0V to either the reference voltage or twice the reference voltage. The reference can be either taken from the internal voltage reference or from the external voltage applied to the VREF pin. For example, an external reference of 1.2V supplied to VREF may be used to set the ADC range between 0V and 2.4V.

VREF	Gain Setting	Maximum Input Range	Supply Voltage Range (VDD)
1.2V	0	1.2V	2.2V - 3.6V
1.6V	0	1.6V	2.2V - 3.6V
1.2V	1	2.4V	2.6V - 3.6V
1.6V	1	3.2V	3.4V - 3.6V

Table 10: ADC Maximum Input Range

The input clock to the ADC is 16MHz and can be divided down to 2MHz, 1MHz, 500kHz and 250kHz. During an ADC conversion the selected input channel is sampled for a fixed period and then held. This sampling period is defined as a number of ADC clock periods and can be programmed to 2, 4, 6 or 8. The conversion rate is $((3 \times \text{Sample period}) + 10)$ clock periods. For example for 500kHz conversion with sample period of 2 will be $(3 \times 2) + 10 = 16$ clock periods, 32µsecs or 31.25kHz. The ADC can be operated in either a single conversion mode or alternatively a new conversion can be started as soon as the previous one has completed, to give continuous conversions.

If the source resistance of the input voltage is 1kΩ or less, then the default sampling time of 2 clocks should be used. The input to the ADC can be modelled as a resistor of 5kΩ(typ) and 10kΩ (max) to represent the on-resistance of the switches and the sampling capacitor 8pF. The sampling time required can then be calculated, by adding the sensor source resistance to the switch resistance, multiplying by the capacitance giving a time constant. Assuming normal exponential RC charging, the number of time constants required to give an acceptable error can be calculated, 6 time constants gives an error of 0.25%, so for 8-bit accuracy 7 time constants should be the target. For a source with zero resistance, 7 time constants is 560 nsecs, hence the smallest sampling window of 2 clock periods can be used.

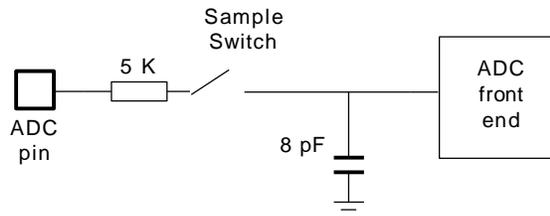


Figure 39: ADC Input Equivalent Circuit

The ADC sampling period, input range and mode (single shot or continuous) are controlled through software.

When the ADC conversion is complete, an interrupt is generated. Alternatively the conversion status can be polled. When operating in continuous mode, it is recommended that the interrupt is used to signal the end of a conversion, since conversion times may range from 8 to 136 µsecs. Polling over this period would be wasteful of processor bandwidth.

To facilitate averaging of the ADC values, which is a common practice in microcontrollers, a dedicated accumulator has been added, the user can define the accumulation to occur over 2,4,8 or 16 samples. The end of conversion interrupt can be modified to occur at the end of the chosen accumulation period, alternatively polling can still be used. Software can then be used to apply the appropriate rounding and shifting to generate the average value, as well as setting up the accumulation function.

For detailed electrical specifications, see Section 19.3.6.

17.1.2 Supply Monitor

The internal supply monitor allows the voltage on the analogue supply pin VDD1 to be measured. This is achieved with a potential divider that reduces the voltage by a factor of 0.666, allowing it to fall inside the input range of the ADC when set with an input range twice the internal voltage reference. The resistor chain that performs the voltage reduction is disabled until the measurement is made to avoid a continuous drain on the supply.

17.1.3 Temperature Sensor

The on chip temperature sensor can be used either to provide an absolute measure of the device temperature or to detect changes in the ambient temperature. In common with most on chip temperature sensors, it is not trimmed and so the absolute accuracy variation is large; the user may wish to calibrate the sensor prior to use. The sensor forces a constant current through a forward biased diode to provide a voltage output proportional to the chip die temperature which can then be measured using the ADC. The measured voltage has a linear relationship to temperature as described in Section 19.3.12.

Because this sensor is on chip, any measurements taken must account for the thermal time constants. For example, if the device just came out of sleep mode the user application should wait until the temperature has stabilised before taking a measurement.

17.2 Comparator

The JN5142 contains one analogue comparator, COMP1, that is designed to have true rail-to-rail inputs and operate over the full voltage range of the analogue supply VDD1. The hysteresis level can be set to a nominal value of 0mV, 10mV, 20mV or 40mV. The source of the negative input signal for the comparator can be set to the internal voltage reference, the negative external pin (COMP1M, which uses the same pin as DIO17) or the positive external pin (COMP1P, on the same pin as DIO16). The source of the positive input signal can be COMP1P or COMP1M. DIO16 and DIO17 cannot be used if the external comparator inputs are needed. The comparator output is routed to an internal register and can be polled, or can be used to generate interrupts. The comparator can be disabled to reduce power consumption.

The comparator also has a low power mode where the response time of the comparator is slower than the normal mode, but the current required is greatly reduced, these figures are specified in Section 19.3.7. It is the only mode that may be used during sleep, where a transition through the threshold will wake the device. The wakeup action and the configuration for which edge of the comparator output will be active are controlled through software. In sleep mode the negative input signal source, must be configured to be driven from the external pins.

18 Power Management and Sleep Modes

18.1 Operating Modes

Three operating modes are provided in the JN5142 that enable the system power consumption to be controlled carefully to maximise battery life.

- Active Processing Mode
- Sleep Mode
- Deep Sleep Mode

The variation in power consumption of the three modes is a result of having a series of power domains within the chip that may be controllably powered on or off.

18.1.1 Power Domains

The JN5142 has the following power domains:

- **VDD Supply Domain:** supplies the wake-up timers and controller, DIO blocks, Comparator, SVM and BOR plus Fast RC, 32kHz RC and crystal oscillators. This domain is driven from the external supply (battery) and is always powered. The wake-up timers and controller, and the 32kHz RC and crystal oscillators may be powered on or off in sleep mode through software control.
- **Digital Logic Domain:** supplies the digital peripherals, CPU, ROM, Baseband controller, Modem and Encryption processor. It is powered off during sleep mode.
- **RAM Domain:** supplies the RAM during sleep mode to retain the memory contents. It may be powered on or off for sleep mode through software control.
- **Radio Domain:** supplies the radio interface, ADCs and temperature sensor. It is powered during transmit and receive and when the analogue peripherals are enabled. It is controlled by the baseband processor and is powered off during sleep mode.

The current consumption figures for the different modes of operation of the device is given in Section 19.2.2.

18.2 Active Processing Mode

Active processing mode in the JN5142 is where all of the application processing takes place. By default, the CPU will execute at the selected clock speed executing application firmware. All of the peripherals are available to the application, as are options to actively enable or disable them to control power consumption; see specific peripheral sections for details.

Whilst in Active processing mode there is the option to doze the CPU but keep the rest of the chip active; this is particularly useful for radio transmit and receive operations, where the CPU operation is not required therefore saving power.

18.2.1 CPU Doze

Whilst in doze mode, CPU operation is stopped but the chip remains powered and the digital peripherals continue to run. Doze mode is entered through software and is terminated by any interrupt request. Once the interrupt service routine has been executed, normal program execution resumes. Doze mode uses more power than sleep and deep sleep modes but requires less time to restart and can therefore be used as a low power alternative to an idle loop.

Whilst in CPU doze the current associated with the CPU is not consumed, therefore the basic device current is reduced as shown in the figures in Section 19.2.2.1.

18.3 Sleep Mode

The JN5142 enters sleep mode through software control. In this mode most of the internal chip functions are shutdown to save power, however the state of DIO pins are retained, including the output values and pull-up enables, and this therefore preserves any interface to the outside world.

When entering into sleep mode, there is an option to retain the RAM contents throughout the sleep period. If the wakeup timers are not to be used for a wakeup event and the application does not require them to run continually, then power can be saved by switching off the 32kHz oscillator if selected as the 32kHz system clock through software control. The oscillator will be restarted when a wakeup event occurs.

Whilst in sleep mode one of four possible events can cause a wakeup to occur: transitions on DIO inputs, expiry of wakeup timers, pulse counters maturing or comparator events. If any of these events occur, and the relevant interrupt is enabled, then an interrupt is generated that will cause a wakeup from sleep. It is possible for multiple wakeup sources to trigger an event at the same instant and only one of them will be accountable for the wakeup period. It is therefore necessary in software to remove all other pending wakeup events prior to requesting entry back into sleep mode; otherwise, the device will re-awaken immediately.

When wakeup occurs, a similar sequence of events to the reset process described in Section 6.1 happens, including the checking of the supply voltage by the Brown Out Detector 6.4. The High-Speed RC oscillator is started up, once stable the power to CPU system is enabled and the reset is removed. Software determines that this is a reset from sleep and so commences with the wakeup process. If RAM contents were held through sleep, wakeup is quicker as the application program does not have to be reloaded from Flash memory. See Section 19.3.4 for wake-up timings.

18.3.1 Wakeup Timer Event

The JN5142 contains two 35-bit wakeup timers that are counters clocked from the 32kHz oscillator, and can be programmed to generate a wake-up event. Following a wakeup event, the timers continue to run. These timers are described in Section 11.3.

Timer events can be generated from both of the two timers; one is intended for use by the 802.15.4 protocol, the other being available for use by the Application running on the CPU. These timers are available to run at any time, even during sleep mode.

18.3.2 DIO Event

Any DIO pin when used as an input has the capability, by detecting a transition, to generate a wake-up event. Once this feature has been enabled the type of transition can be specified (rising or falling edge). Even when groups of DIO lines are configured as alternative functions such as the UARTs or Timers etc, any input line in the group can still be used to provide a wakeup event. This means that an external device communicating over the UART can wakeup a sleeping device by asserting its RTS signal pin (which is the CTS input of the JN5142).

18.3.3 Comparator Event

The comparator can generate a wakeup interrupt when a change in the relative levels of the positive and negative inputs occurs. The ability to wakeup when continuously monitoring analogue signals is useful in ultra-low power applications. For example, the JN5142 can remain in sleep mode until the voltage drops below a threshold and then be woken up to deal with the alarm condition.

18.3.4 Pulse Counter

The JN5142 contains two 16 bit pulse counters that can be programmed to generate a wake-up event. Following the wakeup event the counters will continue to operate and therefore no pulse will be missed during the wake-up process. These counters are described in Section 12.

To minimise sleep current it is possible to disable the 32K RC oscillator and still use the pulse counters to cause a wake-up event, provided debounce mode is not required.

18.4 Deep Sleep Mode

Deep sleep mode gives the lowest power consumption. All switchable power domains are off and certain functions in the VDD supply power domain, including the 32kHz oscillator are stopped. This mode can be exited by a power down, a hardware reset on the RESETN pin, or a DIO event. The DIO event in this mode causes a chip reset to occur.

19 Electrical Characteristics

19.1 Maximum Ratings

Exceeding these conditions may result in damage to the device.

Parameter		Min	Max
Device supply voltage VDD1, VDD2		-0.3V	3.6V
Supply voltage at voltage regulator bypass pins VB_XXX		-0.3V	1.98V
Voltage on analogue pins XTALOUT, XTALIN, VCOTUNE, RF_IN.		-0.3V	VB_XXX + 0.3V
Voltage on analogue pins VREF, ADC1, IBIAS		-0.3V	VDD1 + 0.3V
Voltage on 5v tolerant digital pins SPICLK, SPIMOSI, SPIMISO, SPISEL0, DIO2-8 & DIO11-14, RESETN		-0.3V	Lower of (VDD2 + 2V) and 5.5V
Voltage on 3v tolerant digital pins DIO0, DIO1, DIO9, DIO10, DIO15-17		-0.3V	VDD2 + 0.3V
Storage temperature		-40°C	150°C
Reflow soldering temperature according to IPC/JEDEC J-STD-020C			260°C
ESD rating	Human Body Model ¹		2.0kV
	Charged Device Model ² (Exception XTALOUT 350V)		500V

1) Testing for Human Body Model discharge is performed as specified in JEDEC Standard JESD22-A114.

2) Testing for Charged Device Model discharge is performed as specified in JEDEC Standard JESD22-C101.

19.2 DC Electrical Characteristics

19.2.1 Operating Conditions

Supply	Min	Max
VDD1, VDD2	2.0V	3.6V
Standard Ambient temperature range	-40°C	85°C
Extended Ambient temperature range	-40°C	125°C

In the following sections typical is defined as 25°C and VDD1,2 =3V

Most parameter values cover the extended temperature range up to 125 °C, where this is not the case, two values are given, the value in *italics* type face is for standard temperature range up to 85°C and the value in **bold** is for the extended range.

19.2.2 DC Current Consumption

VDD = 2.0 to 3.6V, -40 to +125° C

19.2.2.1 Active Processing

Mode:	Min	Typ	Max	Unit	Notes
CPU processing 32,16,8,4,2 or 1MHz		2100 + 220/MHz		µA	SPI, GPIOs enabled. When in CPU doze the current related to CPU speed is not consumed.
Radio transmit		14.8		mA	CPU in software doze – radio transmitting
Radio receive		16.5		mA	CPU in software doze – radio in receive mode
The following current figures should be added to those above if the feature is being used					
ADC		655		µA	Temperature sensor and battery measurements require ADC
Comparator		73/0.8		µA	Normal/low-power
UART		90		µA	For each UART
Timer		30		µA	For each Timer
2-wire serial interface (I ² C)		70		µA	

19.2.2.2 Sleep Mode

Mode:	Min	Typ	Max	Unit	Notes
Sleep mode with I/O wakeup		0.12		µA	Waiting on I/O event
Sleep mode with I/O and RC Oscillator timer wakeup – measured at 25°C		0.73		µA	As above, but also waiting on timer event. If both wakeup timers are enabled then add another 0.05µA
32kHz crystal oscillator		1.5		µA	As alternative sleep timer
The following current figures should be added to those above if the feature is being used					
RAM retention– measured at 25°C		0.7		µA	For full 32KB retained
Comparator (low-power mode)		0.8		µA	Reduced response time

19.2.2.3 Deep Sleep Mode

Mode:	Min	Typ	Max	Unit	Notes
Deep sleep mode– measured at 25°C		100		nA	Waiting on chip RESET or I/O event

19.2.3 I/O Characteristics

VDD = 2.0 to 3.6V, -40 to +125° C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Internal DIO pullup resistors	22 26 39 45	33 40 61 71	48, 51 59, 63 93, 97 109, 113	kΩ	VDD2 = 3.6V VDD2 = 3.0V VDD2 = 2.2V VDD2 = 2.0V
Internal RESETN pullup resistor	158 189 287 338	231 287 450 531	335, 353 425, 448 680, 705 803, 825	kΩ	VDD2 = 3.6V VDD2 = 3.0V VDD2 = 2.2V VDD2 = 2.0V
Digital I/O High Input (DIO0,1, 9,10, 15 - 17) (Remaining digital pins)	VDD2 x 0.7 VDD2 x 0.7		VDD2 Lower of (VDD2 + 2V) and 5.5V	V	
Digital I/O low Input	-0.3		VDD2 x 0.27	V	
Digital I/O input hysteresis	140	230	310	mV	
DIO High O/P (2.7-3.6V)	VDD2 x 0.8		VDD2	V	With 4mA load
DIO Low O/P (2.7-3.6V)	0		0.4	V	With 4mA load
DIO High O/P (2.2-2.7V)	VDD2 x 0.8		VDD2	V	With 3mA load
DIO Low O/P (2.2-2.7V)	0		0.4	V	With 3mA load
DIO High O/P (2.0-2.2V)	VDD2 x 0.8		VDD2	V	With 2.5mA load
DIO Low O/P (2.0-2.2V)	0		0.4	V	With 2.5mA load
Current sink/source capability		4 3 2.5		mA	VDD2 = 2.7V to 3.6V VDD2 = 2.2V to 2.7V VDD2 = 2.0V to 2.2V
I _{IL} - Input Leakage Current			15, 50	nA	V _{cc} = 3.6V, pin low
I _{IH} - Input Leakage Current			15, 50	nA	V _{cc} = 3.6V, pin high

19.3 AC Characteristics

19.3.1 Reset and Supply Voltage Monitor

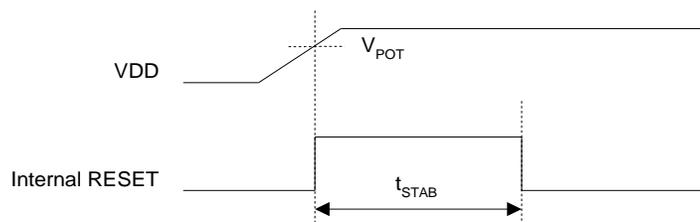


Figure 40: Internal Power-on Reset without Showing Brown-Out

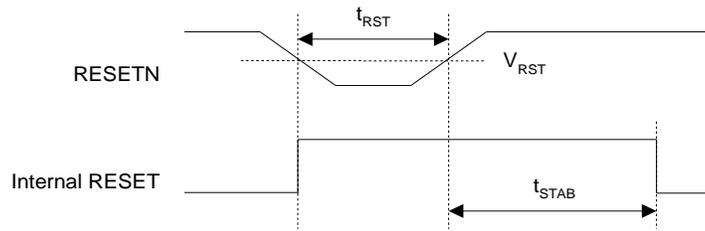


Figure 41: Externally Applied Reset

VDD = 2.0 to 3.6V, -40 to +125° C

Parameter	Min	Typ	Max	Unit	Notes
External Reset pulse width to initiate reset sequence (t_{RST})	1			μs	Assumes internal pullup resistor value of 100K worst case and ~5pF external capacitance
External Reset threshold voltage (V_{RST})	$V_{DD} \times 0.7$			V	Minimum voltage to avoid being reset
Internal Power-on Reset threshold voltage (V_{POT}) Rise/fall time > 10mS		1.47 1.42		V	Rising Falling
Spike Rejection Square wave pulse 1us Triangular wave pulse 10us		1.2 1.3		V	Depth of pulse to trigger reset
Reset stabilisation time (t_{STAB})		45		μs	Note 1
Supply Voltage Monitor Threshold Voltage (V_{TH})	1.88 1.92 2.03 2.12 2.22 2.31 2.60 2.89	1.96 2.00 2.11 2.21 2.31 2.41 2.71 3.01	2.02 2.06 2.17 2.28 2.38 2.48 2.79 3.10	V	Configurable threshold with 8 levels
Supply Voltage Monitor Hysteresis (V_{HYS})		43 46 50 57 63 70 85 100		mV	Corresponding to the 8 threshold levels

¹ Time from release of reset to start of executing ROM code. Loading program from Flash occurs in addition to this.

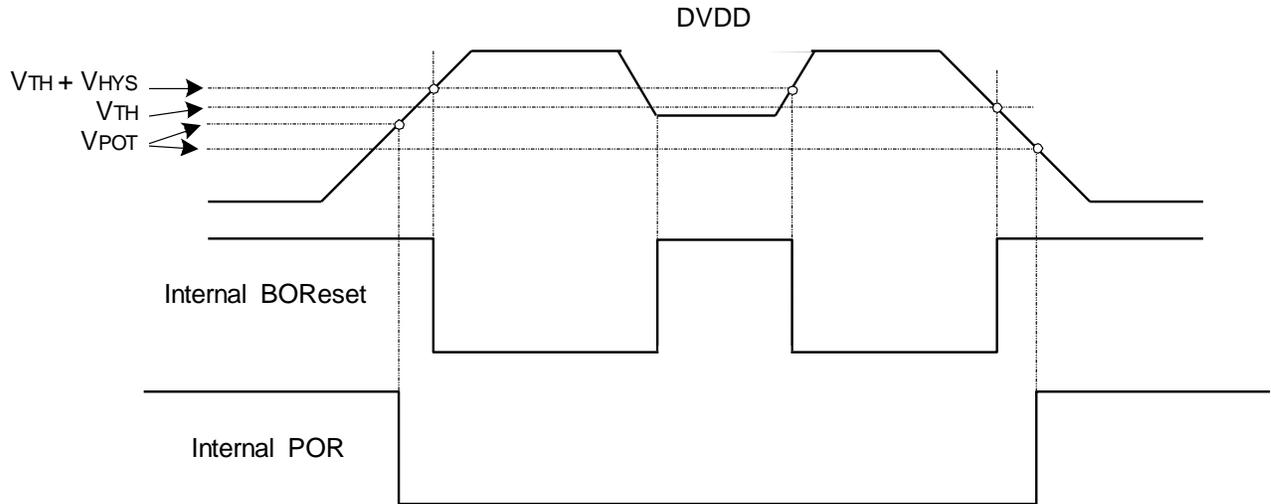


Figure 42: Power-on Reset Followed By Brown-out Detect

19.3.2 SPI Master Timing

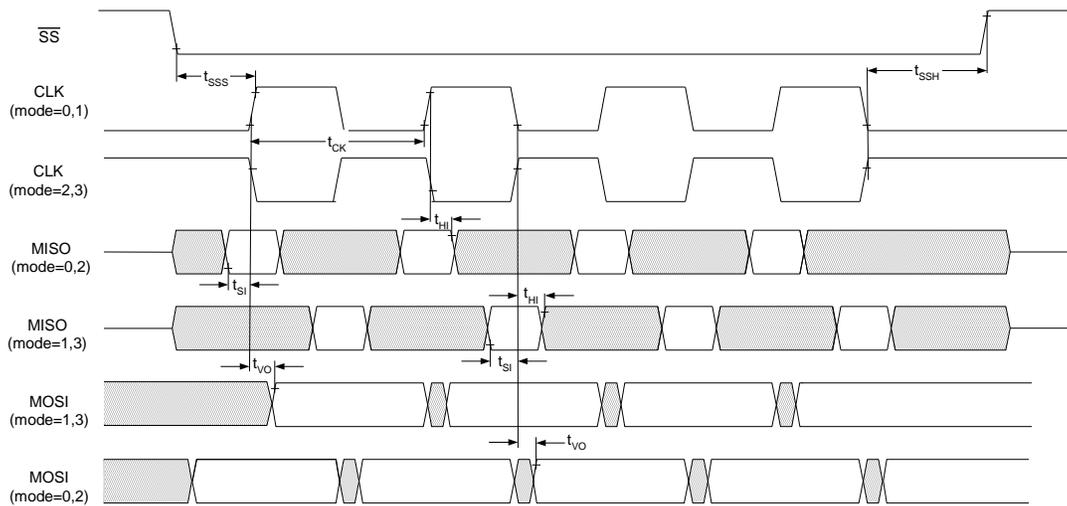


Figure 43: SPI Timing (Master)

Parameter	Symbol	Min	Max	Unit
Clock period	t_{CK}	62.5	-	ns
Data setup time	t_{SI}	16.7 @ 3.3V 18.2 @ 2.7V 21.0 @ 2.0V	-	ns
Data hold time	t_{HI}	0	-	ns
Data invalid period	t_{VO}	-	15	ns
Select set-up period	t_{SSS}	60	-	ns
Select hold period	t_{SSH}	30 (SPICLK = 16MHz) 0 (SPICLK < 16MHz, mode=0 or 2) 60 (SPICLK < 16MHz, mode=1 or 3)	-	ns

19.3.3 Two-wire Serial Interface

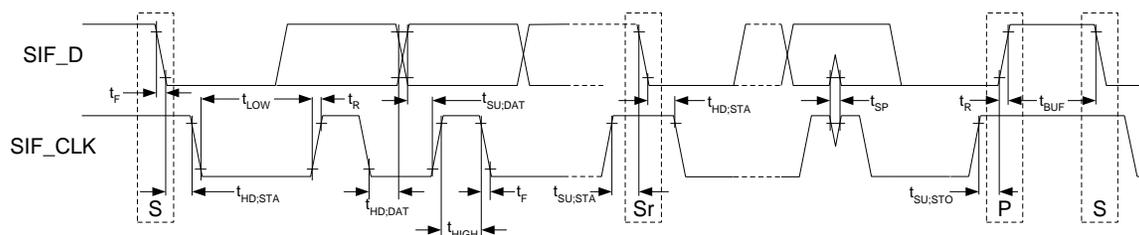


Figure 44: Two-wire Serial Interface Timing

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SIF_CLK clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4	-	0.6	-	μs
LOW period of the SIF_CLK clock	t_{LOW}	4.7	-	1.3	-	μs
HIGH period of the SIF_CLK clock	t_{HIGH}	4	-	0.6	-	μs
Set-up time for repeated START condition	$t_{SU:STA}$	4.7	-	0.6	-	μs
Data setup time SIF_D	$t_{SU:DAT}$	0.25	-	0.1	-	μs
Rise Time SIF_D and SIF_CLK	t_R	-	1000	$20+0.1C_b$	300	ns
Fall Time SIF_D and SIF_CLK	t_F	-	300	$20+0.1C_b$	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4	-	0.6	-	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	μs
Pulse width of spikes that will be suppressed by input filters (Note 1)	t_{SP}	-	60	-	60	ns
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nl}	0.1VDD	-	0.1VDD	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nh}	0.2VDD	-	0.2VDD	-	V

Note 1: This figure indicates the pulse width that is guaranteed to be suppressed. Pulse with widths up to 125nsec may also get suppressed.

19.3.4 Wakeup and Boot Load Timings

Parameter	Min	Typ	Max	Unit	Notes
Time for crystal to stabilise ready to run CPU		0.74		ms	Reached oscillator amplitude threshold
Time for crystal to stabilise ready for radio activity		1.0		ms	
Wake up from Deep Sleep or from Sleep (memory not held)		$0.05 + 0.5^*$ program size in KBytes		ms	Assumes SPI clock to external Flash is 16MHz
Wake up from Sleep (memory held)		45		μs	Start-up runs from High-Speed RC oscillator
Wake up from CPU Doze mode		0.2		μs	

19.3.5 Bandgap Reference

VDD = 2.0 to 3.6V, -40 to +125°C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Voltage	<i>1.156</i> , 1.154	1.192	1.216	V	
DC power supply rejection		58		dB	at 25°C
Temperature coefficient		-30 +35 -60 +5		ppm/°C	20 to 85°C -40°C to 20°C 20 to 125 °C -40°C to 85°C
Point of inflexion		+15		°C	

19.3.6 Analogue to Digital Converters

VDD = 3.0V, VREF = 1.2V, -40 to +125°C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Resolution			8	bits	500kHz Clock
Current consumption		655		µA	
Integral nonlinearity		± 1 , 1.2		LSB	
Differential nonlinearity	-0.5		+0.5	LSB	Guaranteed monotonic
Offset error		-10 -20		mV	0 to Vref range 0 to 2Vref range
Gain error		+10 +20		mV	0 to Vref range 0 to 2Vref range
Internal clock		0.25,0.5 or 1.0		MHz	16MHz input clock, $\div 16,32$ or 64
No. internal clock periods to sample input		2, 4, 6 or 8			Programmable
Conversion time	16		136	µs	Programmable
Input voltage range	0.04		Vref or 2*Vref	V	Switchable. Refer to 17.1.1
Vref (Internal)	See Section 19.3.5				
Vref (External)	1.15	1.2	1.6	V	Allowable range into VREF pin
Input capacitance		8		pF	In series with 5K ohms

19.3.7 Comparator

VDD = 2.0 to 3.6V -40 to +125°C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Analogue response time (normal)		85	125, 130	ns	+/- 250mV overdrive 10pF load
Total response time (normal) including delay to Interrupt controller			105 + 125, 130	ns	Digital delay can be up to a max. of two 16MHz clock periods
Analogue response time (low power)		2.4	2.8	µs	+/- 250mV overdrive No digital delay
Hysteresis	4 12 28	10 20 40	16, 17 26, 29 50, 55	mV	Programmable in 3 steps and zero
Vref (Internal)	See Section 19.3.5			V	
Common Mode input range	0		Vdd	V	
Current (normal mode)	54	73	102, 110	µA	
Current (low power mode)		0.8	1.1, 1.2	µA	

19.3.8 32kHz RC Oscillator

VDD = 2.0 to 3.6V, -40 to +125 °C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Current consumption of cell and counter logic		680 600 500	830, 930 750, 850 650, 710	nA	3.6V 3.0V 2.0V
32kHz clock native accuracy	-30%	32kHz	+30%		Typical is at 3.0V 25°C
Calibrated 32kHz accuracy		±250		ppm	For a 1 second sleep period calibrating over 20 x 32kHz clock periods
Variation with temperature		-0.010		%/°C	
Variation with VDD2		-1.8		%/V	

19.3.9 32kHz Crystal Oscillator

VDD = 2.0 to 3.6V, -40 to +125°C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Current consumption of cell and counter logic		1.5	1.75, 2.0	µA	This is sensitive to the ESR of the crystal, Vdd and total capacitance at each pin
Start – up time		0.8		s	Assuming xtal with ESR of less than 40kohms and CL= 9pF External caps = 15pF (Vdd/2mV pk-pk) see Appendix B
Input capacitance		1.4		pF	Bondpad and package
Transconductance		17		µA/V	
External Capacitors (CL=9pF)		15		pF	Total external capacitance needs to be 2*CL, allowing for stray capacitance from chip, package and PCB
Amplitude at Xout		Vdd-0.2		Vp-p	

19.3.10 32MHz Crystal Oscillator

VDD = 2.0 to 3.6V, -40 to +125°C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Current consumption	300	375	450, 500	µA	Excluding bandgap ref.
Start – up time		0.74		ms	Assuming xtal with ESR of less than 40ohms and CL= 9pF External caps = 15pF see Appendix B
Input capacitance		1.4		pF	Bondpad and package
Transconductance	3.65, 3.55	4.30	5.16	mA/V	
DC voltages, XTALIN/XTALOUT	390/425 375/405	425/465	470/520	mV	
External Capacitors (CL=9pF)		15		pF	Total external capacitance needs to be 2*CL, allowing for stray capacitance from chip, package and PCB
Amplitude detect threshold		320		mVp-p	Threshold detection accessible via API

19.3.11 High-Speed RC Oscillator

VDD = 2.0 to 3.6V, -40 to +125°C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Current consumption of cell	81	145	250, 275	µA	
Clock native accuracy	-20%	27MHz	+26%		
Calibrated centre frequency accuracy	-7%	32.1MHz	+7.5%		
Variation with temperature	-0.035 , <i>-0.025</i>		-0.015 , <i>0.010</i>	%/°C	
Variation with VDD2	-0.65	-0.35	-0.2, +0.1	%/V	
Startup time			2.4	us	

19.3.12 Temperature Sensor

VDD = 2.0 to 3.6V, -40 to +125°C, *italic* +85 °C **Bold** +125 °C

Parameter	Min	Typ	Max	Unit	Notes
Operating Range	-40	-	125	°C	
Sensor Gain	-1.44	-1.55	-1.66	mV/°C	
Accuracy	-	-	±10	°C	
Non-linearity	-	-	2.5, 3.5	°C	
Output Voltage	630 , 570		855	mV	Includes absolute variation due to manufacturing & temp
Typical Voltage		745		mV	Typical at 3.0V 25°C
Resolution	0.154	0.182	0.209	°C/LSB	0 to Vref ADC I/P Range

19.3.13 Radio Transceiver

This JN5142 meets all the requirements of the IEEE802.15.4 standard over 2.0 - 3.6V and offers the following improved RF characteristics. All RF characteristics are measured single ended.

This part also meets the following regulatory body approvals, when used with NXP's Module Reference Designs. Compliant with FCC part 15, rules, IC Canada, ETSI ETS 300-328 and Japan ARIB STD-T66



The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5142 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

Parameter	Min	Typical	Max	Notes
RF Port Characteristics				
Type				Single Ended
Impedance ¹		50ohm		2.4-2.5GHz
Frequency range	2.400 GHz		2.485GHz	
ESD levels (pin 17)		2KV (HBM) 500v (CDM)		

1) With external matching inductors and assuming PCB layout as in Appendix B.4.

Radio Parameters: 2.0-3.6V, +25°C

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity	-92	-95		dBm	Nominal for 1% PER, as per 802.15.4 Section 6.5.3.3
Maximum input signal		+10		dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection (-1/+1 ch) [CW Interferer]		19/34 [27/49]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Alternate channel rejection (-2/+2 ch) [CW Interferer]		40/45 [54/54]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		48		dBc	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		52		dBc	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 8dB lower. (Note1)
Spurious emissions (RX)		-61	<-70 -58	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		40		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm. Available through Hardware API
Transmitter Characteristics					
Transmit power	+0.5	+2.5		dBm	
Output power control range		-35		dB	In three 12dB steps (Note3)
Spurious emissions (TX)		-40	<-70 <-70	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to 12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz
EVM [Offset]		10 [2.0]	15	%	At maximum output power
Transmit Power Spectral Density		-38	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, Section 6.5.3.1

Radio Parameters: 2.0-3.6V, -40°C

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity	-93.5	-96.5		dBm	Nominal for 1% PER, as per 802.15.4 Section 6.5.3.3
Maximum input signal		+10		dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection (-1/+1 ch) [CW Interferer]		19/34 [TBC]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Alternate channel rejection (-2/+2 ch) [CW Interferer]		40/45 [TBC]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		47		dBc	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		49		dBc	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 8dB lower. (Note1)
Spurious emissions (RX)		-60	<-70 -57	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		39		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm. Available through Hardware API
Transmitter Characteristics					
Transmit power	+0.75	+2.75		dBm	
Output power control range		-35		dB	In three 12dB steps (Note3)
Spurious emissions (TX)		-40	<-70 <-70	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to 12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz
EVM [Offset]		9 [2.0]	15	%	At maximum output power
Transmit Power Spectral Density		-38	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, Section 6.5.3.1

Radio Parameters: 2.0-3.6V, +85°C

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity	-90	-93		dBm	Nominal for 1% PER, as per 802.15.4 Section 6.5.3.3
Maximum input signal		+5		dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection (-1/+1 ch) [CW Interferer]		19/34 [TBC]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Alternate channel rejection (-2/+2 ch) [CW Interferer]		40/45 [TBC]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		49		dBc	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		53		dBc	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 8dB lower. (Note1)
Spurious emissions (RX)		-62	<-70 -59	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		41		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm. Available through Hardware API
Transmitter Characteristics					
Transmit power	-0.2	+1.8		dBm	
Output power control range		-35		dB	In three 12dB steps (Note3)
Spurious emissions (TX)		-38	<-70 <-70	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to 12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz
EVM [Offset]		10 [2.0]	15	%	At maximum output power
Transmit Power Spectral Density		-38	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, Section 6.5.3.1

Radio Parameters: 2.0-3.6V, +125°C

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity	-88	-91		dBm	Nominal for 1% PER, as per 802.15.4 Section 6.5.3.3
Maximum input signal		0		dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection (-1/+1 ch) [CW Interferer]		20/34 [TBC]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Alternate channel rejection (-2/+2 ch) [CW Interferer]		40/45 [TBC]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		49		dBc	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		53		dBc	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 8dB lower. (Note1)
Spurious emissions (RX)		-64	<-70 -61	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		41		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm. Available through Hardware API
Transmitter Characteristics					
Transmit power	-0.8	+1.2		dBm	
Output power control range		-35		dB	In three 12dB steps (Note3)
Spurious emissions (TX)		-37	<-70 <-70	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to 12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz
EVM [Offset]		10 [3.0]	15	%	At maximum output power
Transmit Power Spectral Density		-38	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, Section 6.5.3.1

Note1: Blocker rejection is defined as the value, when 1% PER is seen with the wanted signal 3dB above sensitivity, as per 802.15.4 Section 6.5.3.4

Note2: Channels 11,17,24 low/high values reversed.

Note3: Up to an extra 2.5dB of attenuation is available if required.

Appendix A Mechanical and Ordering Information

A.1 SOT618-1 HVQFN40 40-pin QFN Package Drawing

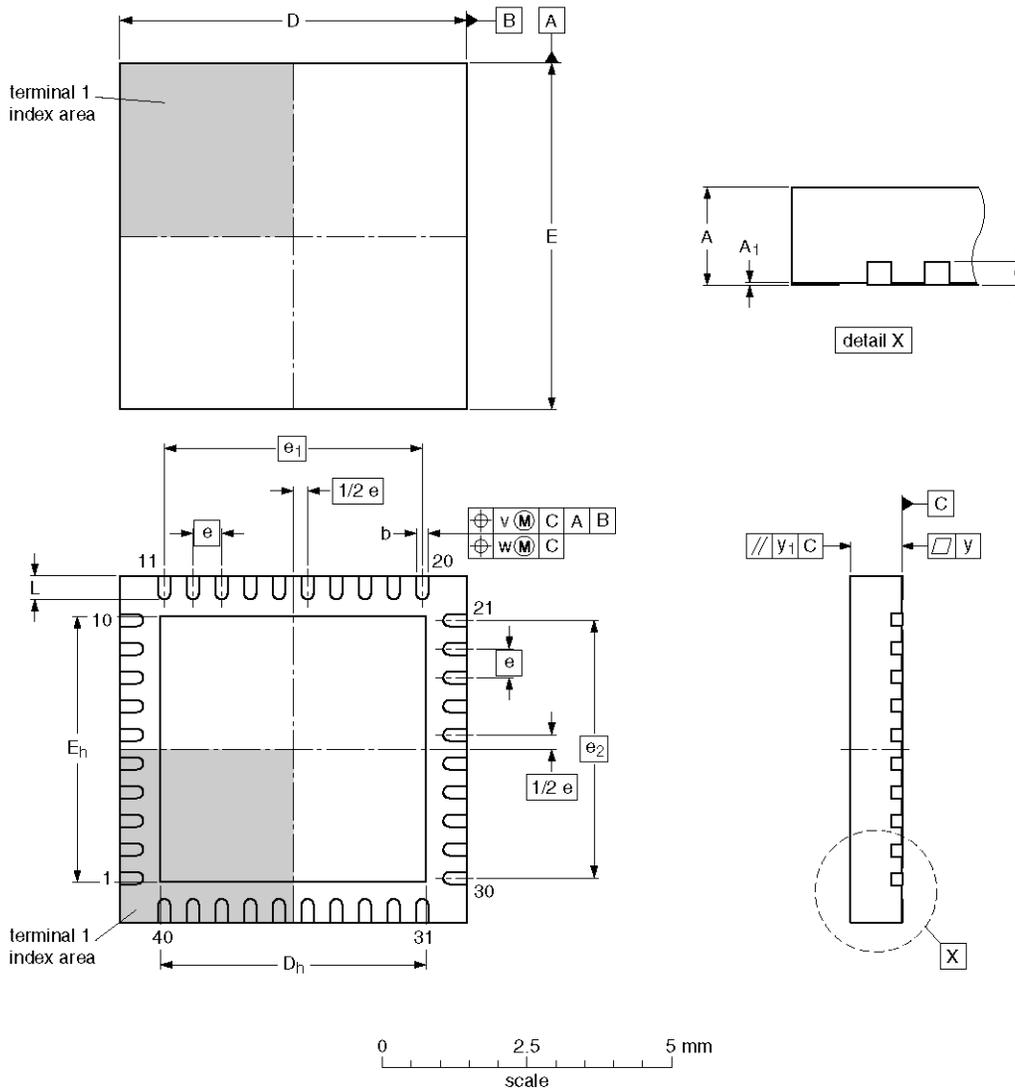


Figure 45: 40-pin QFN Package Drawings

UNIT	A max.	A1	b	c	D	Dh	E	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.75 4.45	6.1 5.9	4.75 4.45	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

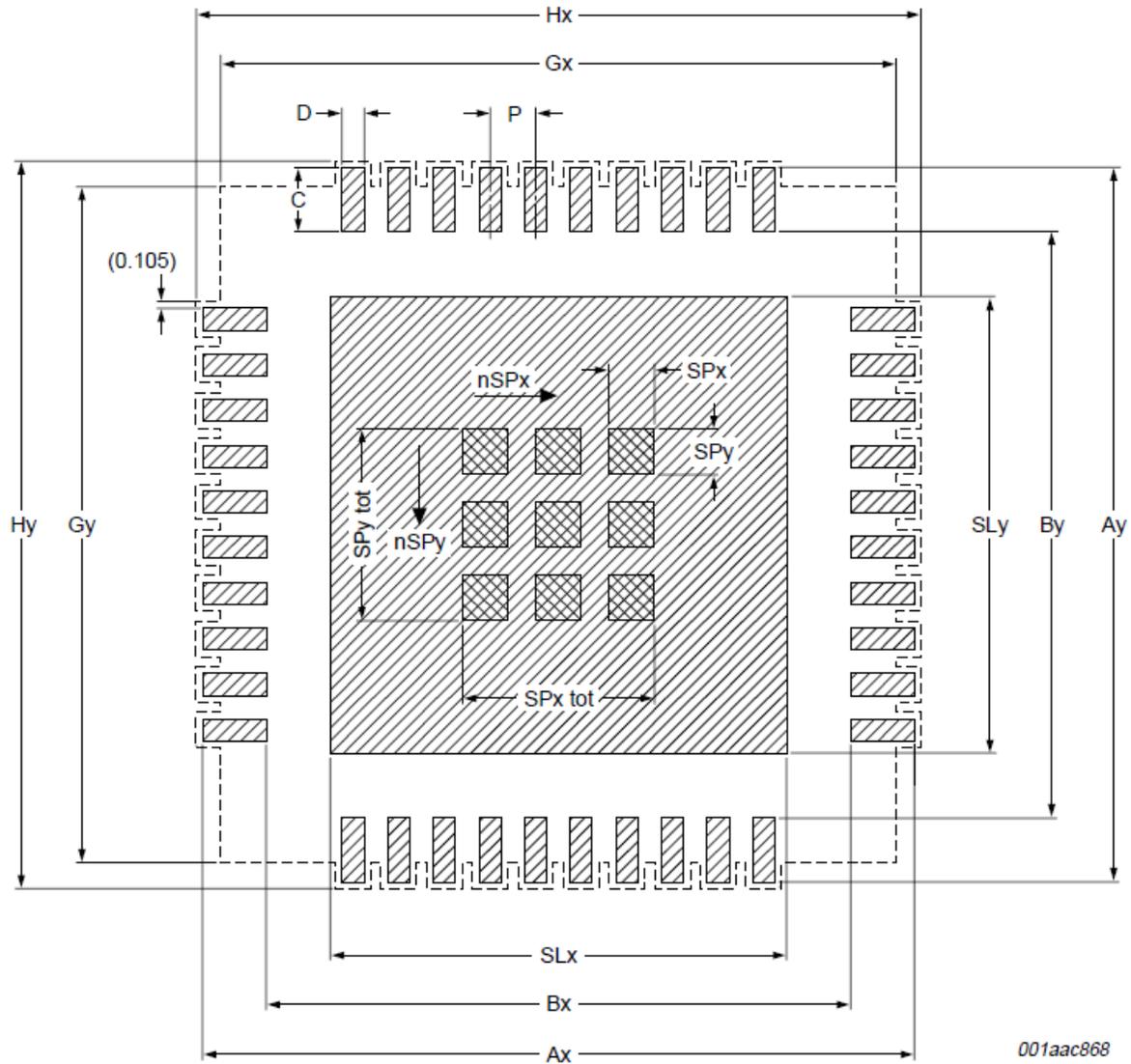
Table 11: Package Dimensions



Plastic or metal protrusions of 0.075 mm maximum per side are not included.

A.2 Footprint information

Information for reflow soldering. All dimensions are given in the table underneath.



-  solder land
-  solder paste deposit
-  solder land plus solder paste

Figure 46: PCB Decal

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	7.000	7.000	5.200	5.200	0.900	0.290	4.100	4.100	2.400	2.400	0.600	0.600	6.300	6.300	7.250	7.250

Table 12: Footprint Dimensions



The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5142 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

A.3 Ordering Information

The standard qualification for the JN5142 is extended industrial temperature range: -40°C to +125°C, packaged in a 40-pin QFN package.

Ordering code format:

JN5142N / XXX

XXX: ROM Variant:

001 IEEE802.15.4, RF4CE and Active RFID

J01 JenNet-IP

The device is available in two different reel quantities

- Tape mounted 4000 devices on a 330mm reel
- Tape mounted 1000 devices on a 180mm reel

Order Codes:

Part Number	Ordering Code	Description
JN5142-001	JN5142N/001	JN5142 microcontroller with 001 ROM
JN5142-J01	JN5142N/J01	JN5142 microcontroller with J01 ROM

The Standard Supply Multiple (SSM) for Engineering Samples or Prototypes is 50 units with a maximum of 250 units. If the quantity of Engineering Samples or Prototypes ordered is less than a reel quantity, then these will be shipped in tape form only, with no reel and will not be dry packaged in a moisture sensitive environment.

The SSM for Production status devices is one reel, all reels are dry packaged in a moisture barrier bag see A.5.3.

A.4 Device Package Marking

The diagram below shows the package markings for JN5142. The package on the left along with the legend information below it, shows the general format of package marking. The package on the right shows the specific markings for a JN5142 device, with revision B ROM software, that came from assembly build number 01 and was manufactured week 25 of 2011.

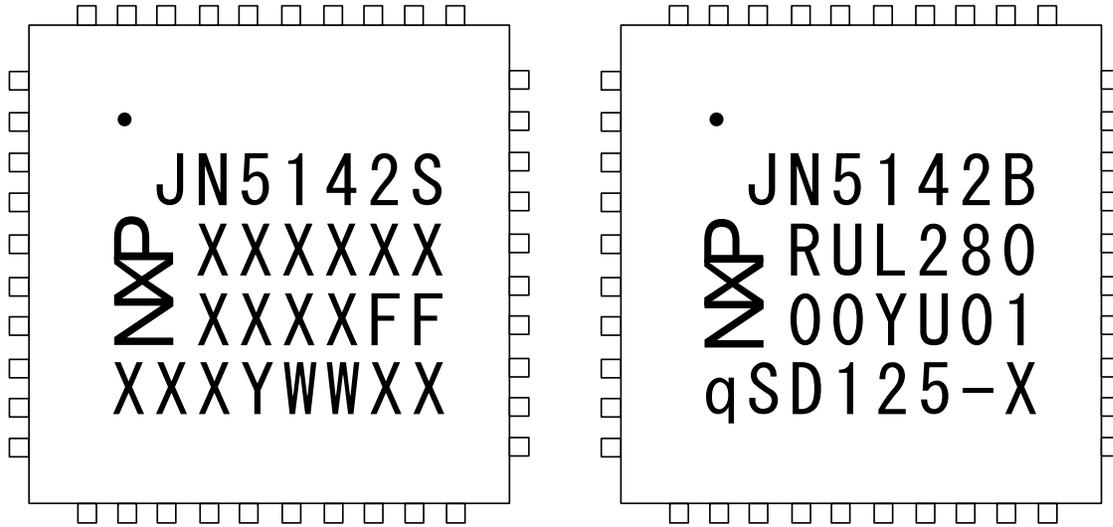


Figure 47: Device Package Marking

Legend:

JN	Family part code
XXXX	4 digit part number
S	Software ROM identifier letter
FF	2 digit assembly build number
Y	1 digit year number
WW	2 digit week number

Network Stack	Ordering Code	Part Marking
IEEE802.15.4 & RF4CE	JN5142N/001	JN5142B
JenNet-IP	JN5142N/J01	JN5142C

A.5 Tape and Reel Information

A.5.1 Tape Orientation and Dimensions

The general orientation of the 40QFN package in the tape is as shown in Figure 48.

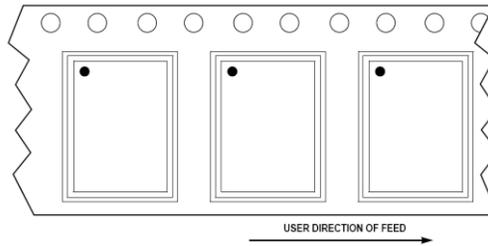
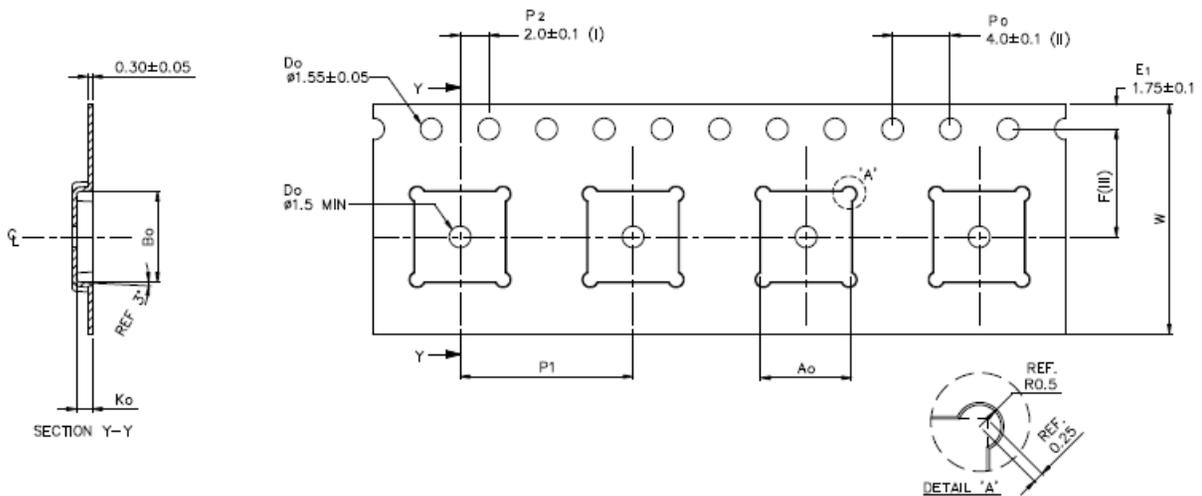


Figure 48: Tape and Reel Orientation

Figure 49 shows the detailed dimensions of the tape used for 6x6mm 40QFN devices.



Reference	Dimensions (mm)
A _o	6.30 ±0.10
B _o	6.30 ±0.10
K _o	1.10 ±0.10
F	7.500 ±0.10
P1	12.0 ±0.10
W	16.00 +0.30/-0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket
- (II) Cumulative tolerance of 10 sprocket holes is ±0.20mm
- (III) Measured from centreline of sprocket hole to centreline of pocket
- (IV) Other material available

Figure 49: Tape Dimensions

A.5.3 Reel Information: 330mm Reel

Surface Resistivity	Between $10e^9$ – $10e^{11}$ Ohms Square
Material	High Impact Polystyrene with Antistatic Additive

All dimensions and tolerances are fully compliant with EIA-481-B and are specified in millimetres.
 3 window design to allow adequate labelling space.

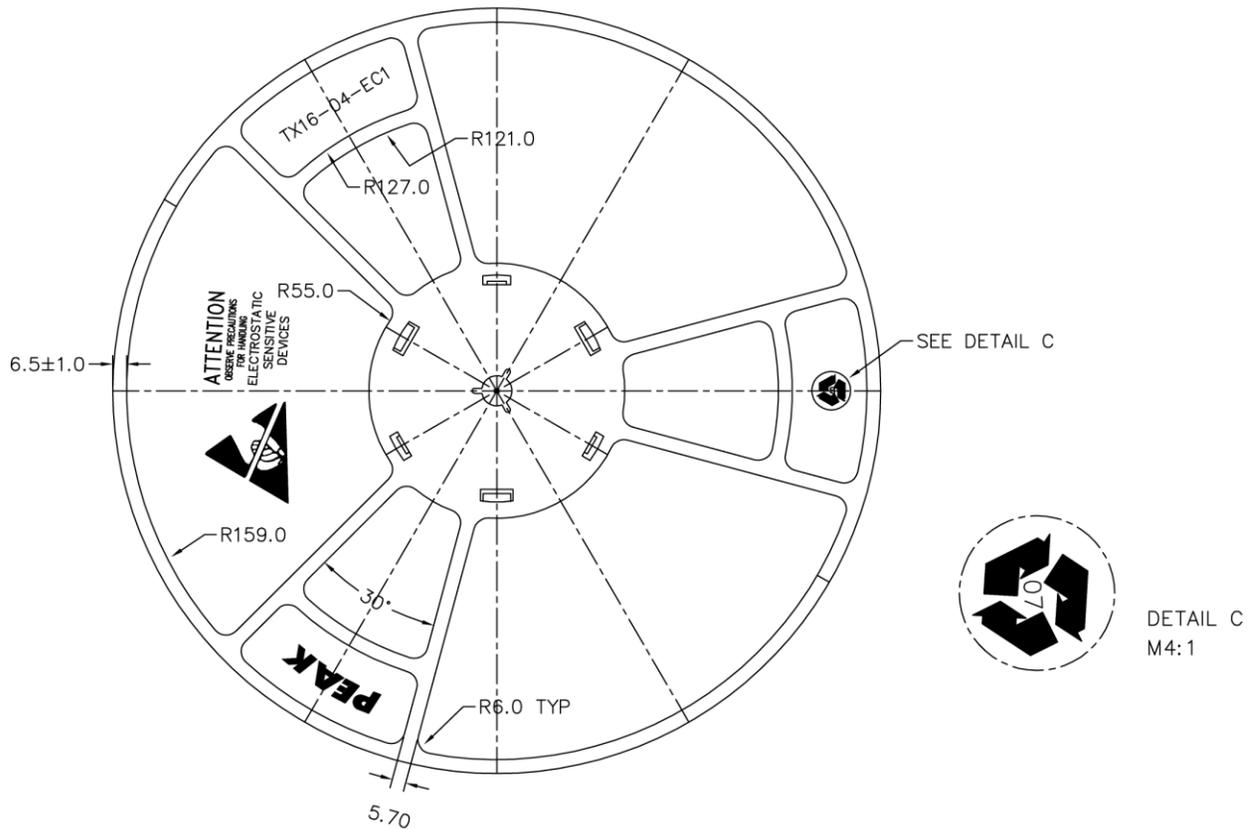


Figure 51: 330mm Reel Dimensions

A.5.4 Dry Pack Requirement for Moisture Sensitive Material

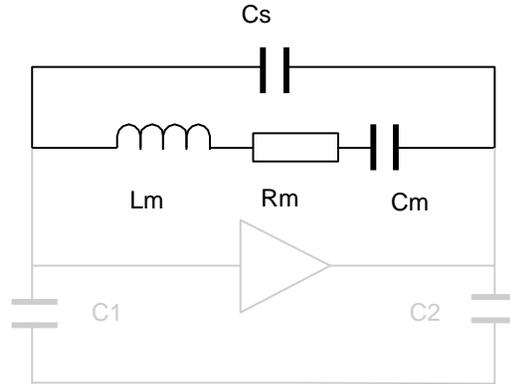
Moisture sensitive material, as classified by JEDEC standard J-STD-033, must be dry packed. The 56 lead QFN package is MSL2A/260°C, and is dried before sealing in a moisture barrier bag (MBB) with desiccant bag weighing at 67.5 grams of activated clay and a humidity indicator card (HIC) meeting MIL-L-8835 specification. The MBB has a moisture-sensitivity caution label to indicate the moisture-sensitive classification of the enclosed devices.

Appendix B Development Support

B.1 Crystal Oscillators

This Section covers some of the general background to crystal oscillators, to help the user make informed decisions concerning the choice of crystal and the associated capacitors.

B.1.1 Crystal Equivalent Circuit



Where C_m is the motional capacitance

L_m is the motional inductance. This together with C_m defines the oscillation frequency (series)

R_m is the equivalent series resistance (ESR).

C_s is the shunt or package capacitance and this is a parasitic

B.1.2 Crystal Load Capacitance

The crystal load capacitance is the total capacitance seen at the crystal pins, from all sources. As the load capacitance (CL) affects the oscillation frequency by a process known as 'pulling', crystal manufacturers specify the frequency for a given load capacitance only. A typical pulling coefficient is 15ppm/pF, to put this into context the maximum frequency error in the IEEE802.15.4 specification is +/-40ppm for the transmitted signal. Therefore, it is important for resonance at 32MHz exactly, that the specified load capacitance is provided.

The load capacitance can be calculated using:

$$CL = \frac{C_{T1} \times C_{T2}}{C_{T1} + C_{T2}}$$

Total capacitance

$$C_{T1} = C_1 + C_{1P} + C_{1in}$$

Where C_1 is the capacitor component

C_{1P} is the PCB parasitic capacitance. With the recommended layout this is about 1.6pF

C_{1in} is the on-chip parasitic capacitance and is about 1.4pF typically.

Similarly for C_{T2}

Hence for a 9pF load capacitance, and a tight layout the external capacitors should be 15pF

B.1.3 Crystal ESR and Required Transconductance

The resistor in the crystal equivalent circuit represents the energy lost. To maintain oscillation, power must be supplied by the amplifier, but how much? Firstly, the Pi connected capacitors C_1 and C_2 with C_S from the crystal, apply an impedance transformation to R_m , when viewed from the amplifier. This new value is given by:

$$\hat{R}_m = R_m \left(\frac{C_S + C_L}{C_L} \right)^2$$

The amplifier is a transconductance amplifier, which takes a voltage and produces an output current. The amplifier together with the capacitors C_1 and C_2 , form a circuit, which provides a negative resistance, when viewed from the crystal. The value of which is given by:

$$R_{NEG} = \frac{g_m}{C_{T1} \times C_{T2} \times \omega^2}$$

Where g_m is the transconductance

ω is the frequency in rad/s

Derivations of these formulas can be easily found in textbooks.

In order to give quick and reliable oscillator start-up, a common rule of thumb is to set the amplifier negative resistance to be a minimum of 4 times the effective crystal resistance. This gives

$$\frac{g_m}{C_{T1} \times C_{T2} \times \omega^2} \geq 4R_m \left(\frac{C_S + C_L}{C_L} \right)^2$$

This can be used to give an equation for the required transconductance.

$$g_m \geq \frac{4R_m \times \omega^2 [C_S(C_{T1} + C_{T2}) + C_{T1} \times C_{T2}]^2}{C_{T1} \times C_{T2}}$$

Example: Using typical 32MHz crystal parameters of $R_m = 40\Omega$, $C_S = 1\text{pF}$ and $C_{T1} = C_{T2} = 18\text{pF}$ (for a load capacitance of 9pF), the equation above gives the required transconductance (g_m) as 2.59mA/V. The JN5142 has a typical value for transconductance of 4.3mA/V

The example and equation illustrate the trade-off that exists between the load capacitance and crystal ESR. For example, a crystal with a higher load capacitance can be used, but the value of max. ESR that can be tolerated is reduced. Also note, that the circuit sensitivity to external capacitance [C_1 , C_2] is a square law.

Meeting the criteria for start-up is only one aspect of the way these parameters affect performance, they also affect the time taken during start-up to reach a given, (or full), amplitude. Unfortunately, there is no simple mathematical model for this, but the trend is the same. Therefore, both a larger load capacitance and larger crystal ESR will give a longer start-up time, which has the disadvantages of reduced battery life and increased latency.

B.2 32MHz Oscillator

The JN5142 contains the necessary on-chip components to build a 32 MHz reference oscillator with the addition of an external crystal resonator, two tuning capacitors. The schematic of these components are shown in Figure 52. The two capacitors, C1 and C2, will typically be 15pF \pm 5% and use a COG dielectric. For a detailed specification of the crystal required and factors affecting C1 and C2 see Appendix B.1. As with all crystal oscillators the PCB layout is especially important, both to keep parasitic capacitors to a minimum and to reduce the possibility of PCB noise being coupled into the oscillator.

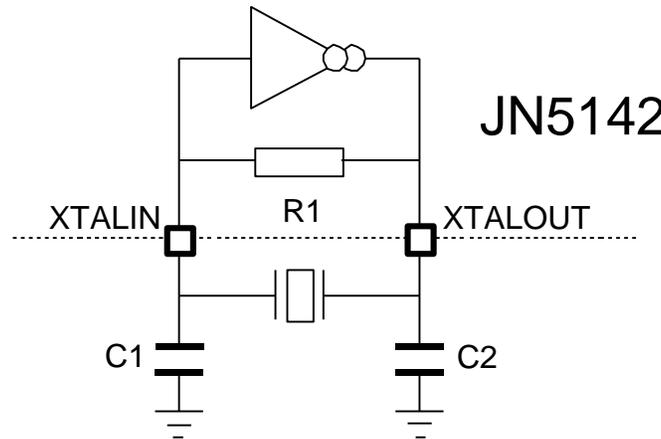


Figure 52: Crystal Oscillator Connections

The clock generated by this oscillator provides the reference for most of the JN5142 subsystems, including the transceiver, processor, memory and digital and analogue peripherals.

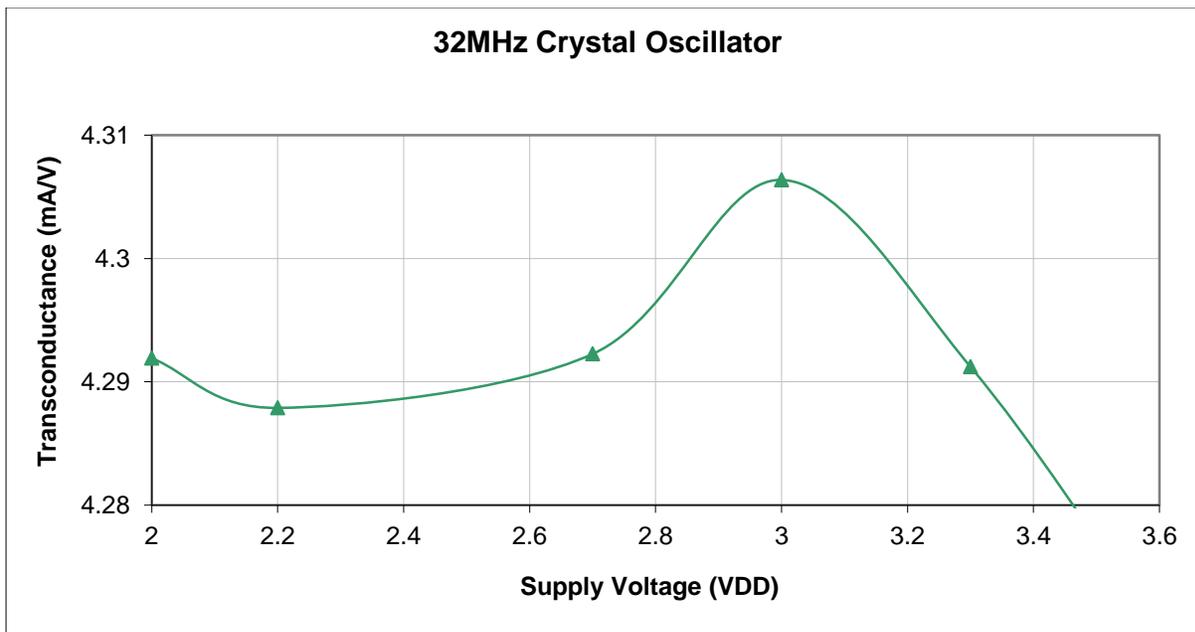
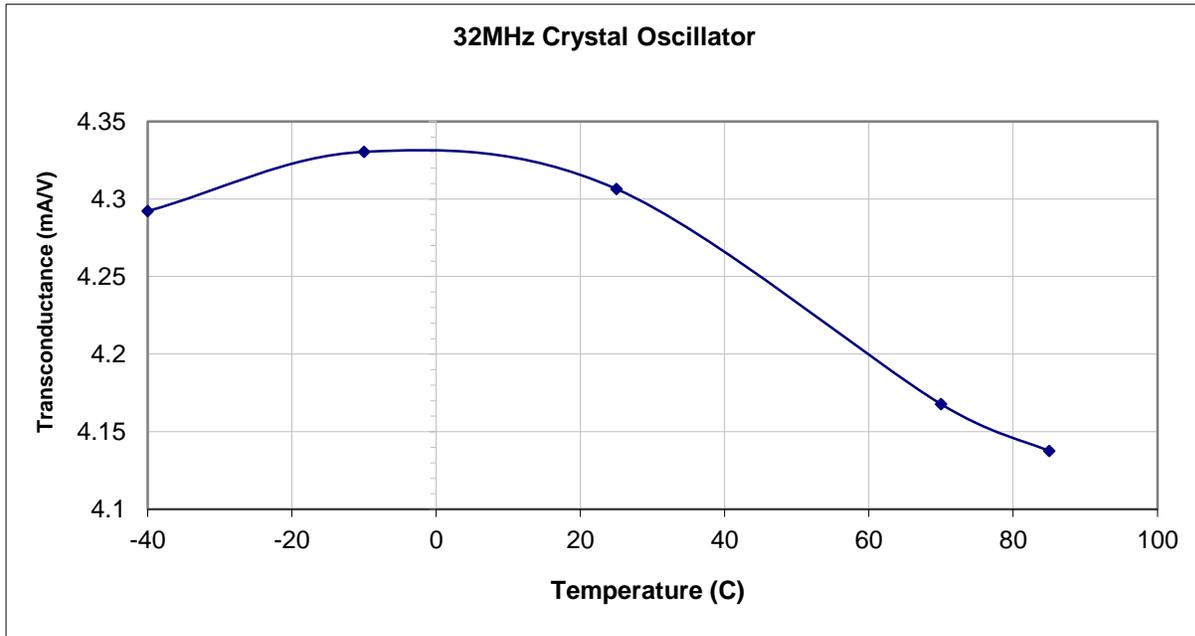
32MHz Crystal Requirements

Parameter	Min	Typ	Max	Notes
Crystal Frequency		32MHz		
Crystal Tolerance			40ppm	Including temperature and ageing
Crystal ESR Range (Rm)	10 Ω		60 Ω	See below for more details
Crystal Load Capacitance Range (CL)	6pF	9pF	12pF	See below for more details
Not all Combinations of Crystal Load Capacitance and ESR are Valid				
Recommended Crystal	Load Capacitance 9pF and max ESR 40 Ω			
External Capacitors (C1 & C2) For recommended Crystal		15pF		CL = 9pF, total external capacitance needs to be 2*CL, allowing for stray capacitance from chip, package and PCB

As is stated above, not all combinations of crystal load capacitance and ESR are valid, and as explained in Appendix B.1.3 there is a trade-off that exists between the load capacitance and crystal ESR to achieve reliable performance.

For this reason, we recommend that for a 9pF load capacitance crystals be specified with a maximum ESR of 40 ohms. For lower load capacitances the recommended maximum ESR rises, for example, $CL=7\text{pF}$ the max ESR is 61 ohms. For the lower cost crystals in the large HC49 package, a load capacitance of 9 or 10pF is widely available and the max ESR of 30 ohms specified by many manufacturers is acceptable. Also available in this package style, are crystals with a load capacitance of 12pF, but in this case the max ESR required is 25 ohms or better.

Below is measurement data showing the variation of the crystal oscillator amplifier transconductance with temperature and supply voltage, notice how small the variation is. Circuit techniques have been used to apply compensation, such that the user need only design for nominal conditions.



B.3 32kHz Oscillator

In order to obtain more accurate sleep periods, the JN5142 contains the necessary on-chip components to build an optional 32kHz oscillator with the addition of an external 32.768kHz crystal and two tuning capacitors. The crystal should be connected between XTAL32K_IN and XTAL32K_OUT (DIO9 and DIO10), with two equal capacitors to ground, one on each pin. The schematic of these components are shown in Figure 53. The two capacitors, C1 and C2, will typically be in the range 10 to 22pF \pm 5% and use a COG dielectric. As with all crystal oscillators the PCB layout is especially important, both to keep parasitic capacitors to a minimum and to reduce the possibility of PCB noise being coupled into the oscillator.

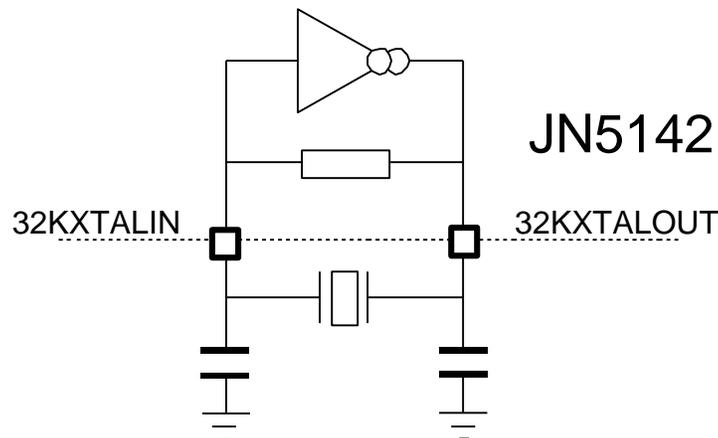


Figure 53: 32kHz Crystal Oscillator Connections

The electrical specification of the oscillator can be found in 19.3.9. The oscillator cell is flexible and can operate with a range of commonly available 32kHz crystals with load capacitances from 6 to 12.5p, and ESR up to 80K Ω . It achieves this by using automatic gain control (AGC), which senses the signal swing. As explained in Appendix B.1.3 there is a trade-off that exists between the load capacitance and crystal ESR to achieve reliable performance. The use of an AGC function allows a wider range of crystal load capacitors and ESR's to be accommodated than would otherwise be possible. However, this benefit does mean the supply current varies with the supply voltage (VDD), value of the total capacitance at each pin, and the crystal ESR. This is described in the table and graphs below.

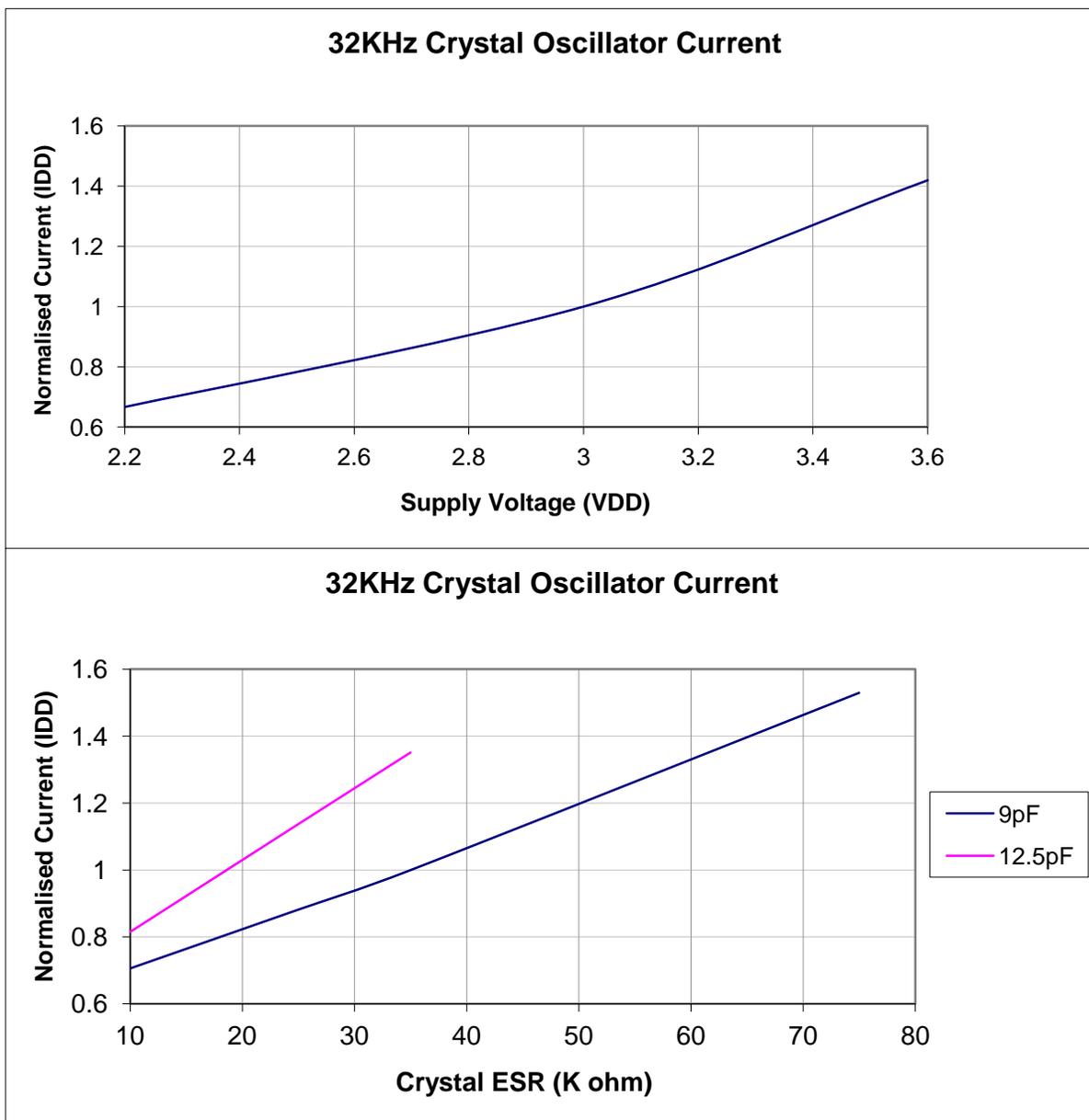
32kHz Crystal Requirements

Parameter	Min	Typ	Max	Notes
Crystal Frequency		32kHz		
Supply Current		1.6 μ A		Vdd=3v, temp=25 C, load cap =9pF, Rm=25K
Supply Current Temp. Coeff.		0.1%/C		Vdd=3v
Crystal ESR Range (Rm)	10K Ω	25K Ω	80K Ω	See below for more details
Crystal Load Capacitance Range (CL)	6pF	9pF	12.5pF	See below for more details
Not all Combinations of Crystal Load Capacitance and ESR are Valid				

Three examples of typical crystals are given, each with the value of external capacitors to use, plus the likely supply current and start-up time that can be expected. Also given is the maximum recommended ESR based on the start-up criteria given in Appendix B.1.3. The values of the external capacitors can be calculated using the equation in Appendix B.1.2 .

Load Capacitance	Ext Capacitors	Current	Start-up Time	Max ESR
9pF	15pF	1.6μA	0.8Sec	70KΩ
6pF	9pF	1.4μA	0.6sec	80KΩ
12.5pF	22pF	2.4μA	1.1sec	35KΩ

Below is measurement data showing the variation of the crystal oscillator supply current with voltage and with crystal ESR, for two load capacitances.



B.4 JN5142 Module Reference Designs

For customers wishing to integrate the JN5142 device directly into their system, NXP provide a range of Module Reference Designs, covering standard and high-power modules fitted with different Antennae

To ensure the correct performance, it is strongly recommended that where possible the design details provided by the reference designs, are used in their exact form for all end designs, this includes component values, pad dimensions, track layouts etc. In order to minimise all risks, it is recommended that the entire layout of the appropriate reference module, if possible, be replicated in the end design.

For full details, see [6]. Please contact technical support via the on-line tech-support system. (www.jennic.com/support)

B.4.1 Schematic Diagram

A schematic diagram of the JN5142 PCB antenna reference module is shown in

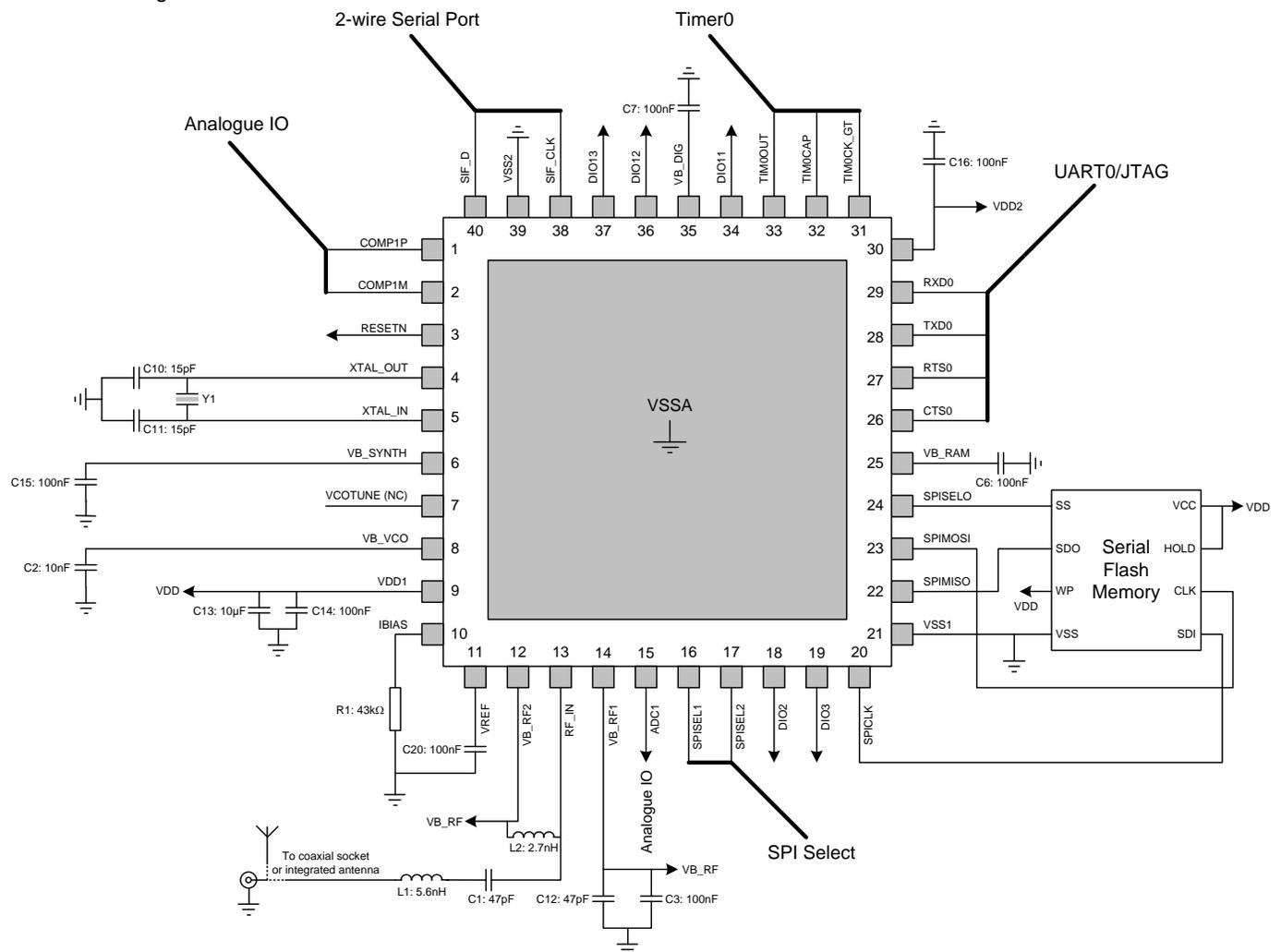


Figure 54. Details of component values and PCB layout constraints can be found in Table 13.

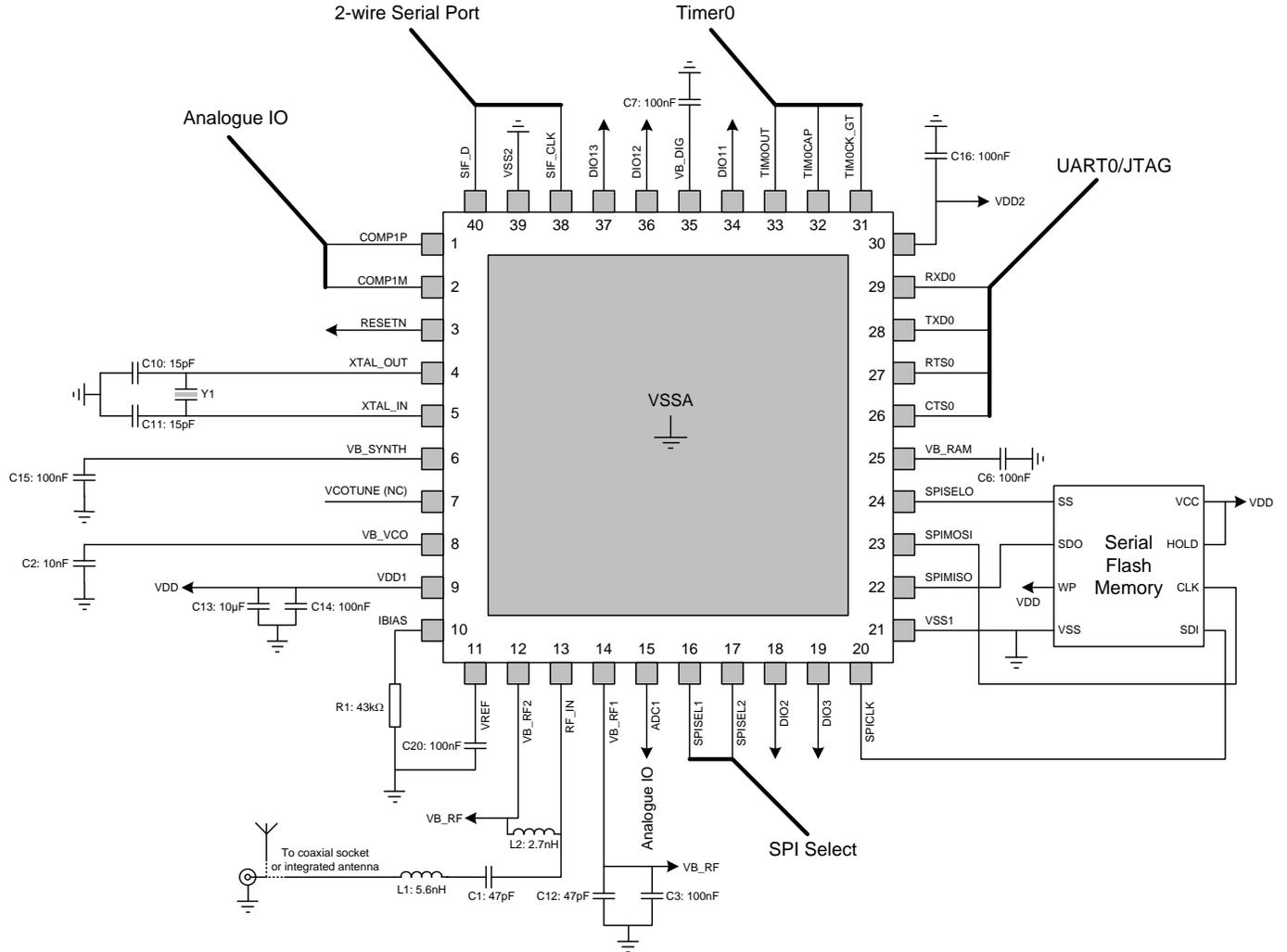


Figure 54: JN5142 Printed Antenna Reference Module Schematic Diagram

Component Designator	Value/Type	Function	PCB Layout Constraints
C13	10 μ F	Power source decoupling	
C14	100nF	Analogue Power decoupling	Adjacent to U1 pin 9
C16	100nF	Digital power decoupling	Adjacent to U1 pin 30
C15	100nF	VB Synth decoupling	Less than 5mm from U1 pin 6
C2	10nF	VB VCO decoupling	Less than 5mm from U1 pin 8
C3	100nF	VB RF decoupling	Less than 5mm from U1 pin 12 and U1 pin 14
C12	47pF	VB RF decoupling	Less than 5mm from U1 pin 12 and U1 pin 14
C6	100nF	VB RAM decoupling	Less than 5mm from U1 pin 25
C7	100nF	VB Dig decoupling	Less than 5mm from U1 pin 35
R1	43k	I Bias Resistor	Less than 5mm from U1 pin 10
C20	100nF	Vref decoupling (optional)	Less than 5mm from U1 pin 11
U2	1Mbit	Serial Flash Memory (Micron M25P10)	
Y1	32MHz	Crystal (AEL X32M000000S039 or Epson Toyocom X1E000021016700) (CL = 9pF, Max ESR 40R)	
C10	15pF +/-5% COG	Crystal Load Capacitor	Adjacent to pin 4 and Y1 pin 1
C11	15pF +/-5% COG	Crystal Load Capacitor	Adjacent to pin 5 and Y1 pin 3
C1	47pF	AC Coupling Phycomp 2238-869-15479	Must be copied directly from the reference design.
L1	5.6nH	RF Matching Inductor MuRata LQP15MN5N6B02	
L2	2.7nH	Load Inductor MuRata LQP15MN2N7B02	

Table 13: JN5142 Printed Antenna Reference Module Components and PCB Layout Constraints

The paddle should be connected directly to ground. Any pads that require connection to ground should do so by connecting directly to the paddle.

B.4.2 PCB Design and Reflow Profile

PCB and land pattern designs are key to the reliability of any electronic circuit design.

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) defines a number of standards for electronic devices. One of these is the "Surface Mount Design and Land Pattern Standard" IPC-SM-782 [3], commonly referred to as "IPC782". This specification defines the physical packaging characteristics and land patterns for a range of surface mounted devices. IPC782 is also a useful reference document for general surface mount design techniques, containing sections on design requirements, reliability and testability. NXP strongly recommends that this be referred to when designing the PCB.

NXP also provide application note AN10366, "HVQFN application information" [7] which describes the reflow soldering process. The suggested reflow profile, from that application note, is shown in Figure 55. The specific paste manufacturers guidelines on peak flow temperature, soak times, time above liquidus and ramp rates should also be referenced.

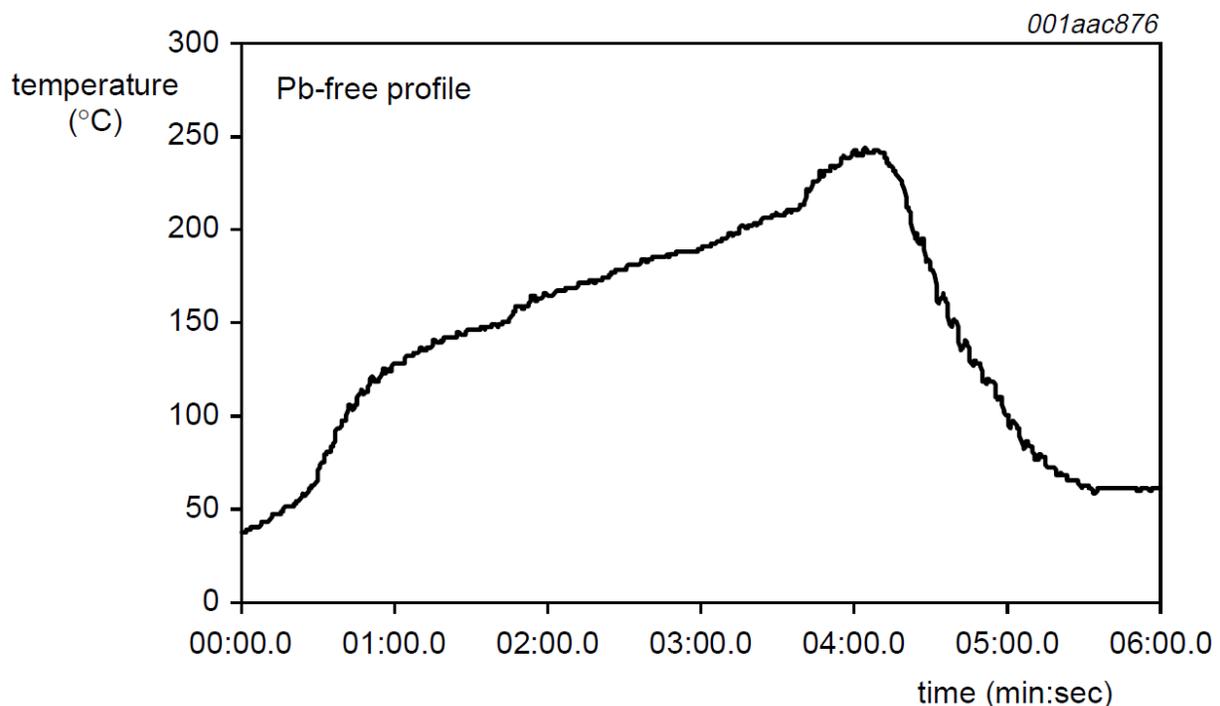


Figure 55: Recommended Reflow Profile for Lead-free Solder Paste (SNAgCu) or PPF Lead Frame

B.4.3 Moisture Sensitivity Level (MSL)

If there is moisture trapped inside a package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may cause damage to the inside of the package (delamination), and it may result in a cracked semiconductor package body (the popcorn effect). A package's MSL depends on the package characteristics and on the temperature it is exposed to during reflow soldering. This is explained in more detail in [8].

Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package.

Related Documents

- [1] IEEE Std 802.15.4-2006 IEEE Standard for Information Technology – Part 15.4 Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs).
- [2] JN-AN-1038 Programming Flash devices not supported by the JN51xx ROM-based bootloader
- [3] IPC-SM-782 Surface Mount Design and Land Pattern Standard
- [4] JN-AN-1118 JN514x Application Debugging
- [5] JN-UG-3066 JN51xx Integrated Peripherals API Reference Manual
- [6] JN-RD-6032 Standard Module Reference Design
- [7] http://www.nxp.com/documents/mounting_and_soldering/HVQFN_mounting.pdf
- [8] http://www.nxp.com/documents/mounting_and_soldering/AN10365.pdf
- [9] JN-AN-1003 Boot Loader Operation

RoHS Compliance

JN5142 devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS) and of the China RoHS (SJ/T11363 – 2006) requirements which came into force on 1st March 2007.

Status Information

The status of this Data Sheet is. **Preliminary**

NXP Low Power RF products progress according to the following format:

Advance

The Data Sheet shows the specification of a product in planning or in development.

The functionality and electrical performance specifications are target values of the design and may be used as a guide to the final specification. Integrated circuits are identified with an Rx suffix, for example JN5142R1.

NXP reserves the right to make changes to the product specification at anytime without notice.

Preliminary

The Data Sheet shows the specification of a product that is commercially available, but is not yet fully qualified.

The functionality of the product is final. The electrical performance specifications are target values and may be used as a guide to the final specification. Integrated circuits are identified with an Rx suffix, for example JN5142R1.

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Production

This is the production Data Sheet for the product.

All functional and electrical performance specifications, where included, including min and max values are derived from detailed product characterization.

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Version Control

Version	Notes
0.4	26/10/10 – First issue, released as Advance Information
1.0	22/12/11 - Major revision including the electrical parameters and appendix A

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