UM10922

ZigBee PRO and IEEE802.15.4 JN5169-001-M00 module

Rev. 1.1 — 15 September 2015 **User manual**

Document information

Info	Content
Keywords	JN5169, Zigbee, module
Abstract	JN5169-001-M00 module user manual

Revision history

Rev	Date	Description
1.1	20150915	removed M06 module
1.0	20150629	Initial version

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. General description

The JN5169-001-M00 module family provides designers with a ready-made component that provides a fully integrated solution for applications, using the IEEE802.15.4 standard in the 2.4 GHz - 2.5 GHz ISM frequency band, including ZigBee Smart Energy and Home Automation and can be quickly and easily included in product designs. The module integrates all of the RF components required, removing the need to perform expensive RF design and test. Products can be designed by simply connecting sensors and switches to the module IO pins. The module uses NXP's single chip IEEE802.15.4 wireless microcontroller, allowing designers to make use of the extensive chip development support material. Hence, this module allows designers to bring wireless applications to market in the minimum time with significantly reduced development effort and cost.

JN5169-001-M00 module has FCC modular approval. it is also CE compliant and subject to a Notified Body Opinion.

1.1 FCC identification

Table 1. FCC identification

Module name	Description	FCCID
JN5169-001-M00	Standard power, integrated antenna	XXMJN5169M0

1.2 Regulatory approvals

The JN5169-001-M00 has been tested against the requirements of the following European standards.

- Radio EN 300 328 v 1.8.1
- EMC, EN 301 489-17 v 2.2.1, EN 62479 2010, EN 301 489-1 v 1.9.2
- Basic Safety Assessment (BSA) EN 60950-1:2006

A Notified Body statement of opinion for this standard is available on request.

Additionally, the module has received FCC "Modular Approval", in compliance with CFR 47 FCC part 15 regulations and in accordance to FCC public notice DA00-1407. The modular approval notice and test report are available on request.

2. Features and benefits

2.1 Benefits

- Microminiature module solutions
- Ready to use in products
- Minimises product development time
- No RF test required for systems
- Compliant with:
  - FCC 47CFR Part 15C
  - ETSI EN 300-328 V1.8.1

- EN 301-489-17 V2.2.1
- EN60950-1-2006
- Temperature range: −40 °C to +85 °C
- Lead-free and RoHS compliant

2.2 Features: module

- 2.4GHz IEEE 802.15.4, ZigBee Smart Energy and Home Automation compatible
- Integral antenna
- 16 mm × 30 mm PCB size
- TX power 8.5 dBm/10 dBm
- Receiver sensitivity –96.5 dBm
- TX current 25.7 mA at 10 dBm
- TX current 23.5 mA at 8.5 dBm
- RX current 17.8 mA at maximum input level 10 dBm
- RX current 16.7 mA at maximum input level 0 dBm
- 2.0 V/3.6 V operation

2.3 Features: microcontroller

- 32-bit RISC CPU; 1 MHz to 32 MHz clock speed
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- 512 kB Flash
- 32 kB RAM
- 4 kB EEPROM
- Data EEPROM with guaranteed 100 k write operations
- ZigBee PRO stack with Home Automation and Smart Energy profiles
- 2-wire I^2C-bus compatible serial interface; can operate as either master or slave
- 5 × PWM (4 timers, 1 timer/counter)
- 2 low-power sleep counters
- 2 UARTs
- SPI-bus Master and Slave port, 3 selects
- Supply voltage monitor with 8 programmable thresholds
- 6-input 10-bit ADC, comparator
- Battery and temperature sensors
- Watchdog and Supply Voltage Monitor (SVM)
- Up to 20 Digital IO (DIO) pins

3. Applications

- Robust and secure low-power wireless applications
- ZigBee Smart Energy networks
- ZigBee Home Automation networks
- Toys and gaming peripherals
- Energy harvesting - for example, self-powered light switch

4. Overview

The JN5169-001-M00 is an ultra-low power, high performance surface mount module targeted at IEEE 802.15.4, ZigBee Smart Energy and Home Automation networking applications, enabling users to realize products with minimum time to market and at the lowest cost. It removes the need for expensive and lengthy development of custom RF board designs and test suites. The module uses NXP's JN5169 wireless microcontroller to provide a comprehensive solution with large memory, high CPU and radio performance and all RF components included. All that is required to develop and manufacture wireless control or sensing products is to connect a power supply and peripherals such as switches, actuators and sensors, considerably simplifying product development.

The module includes an integrated antenna.

5. Marking

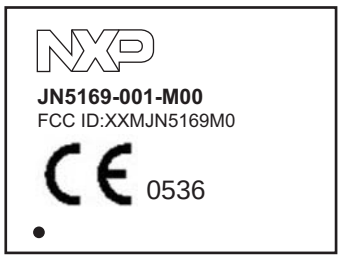


Fig 1. JN5169-001-M00 package marking (top view)

Table 2. Marking code

Line number	Marking code
Line 1	NXP Logo: B&W outline logo
Line 2	part ID: JN5169-001-M00
Line 3	FCC ID: XXMJN5169M0
Line 4	European notified body number

The JN5169-001-M00 module meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS) and of the Chinese RoHS requirements SJ/T11363-2006 which came into force on 1st March 2007.

6. Block diagram

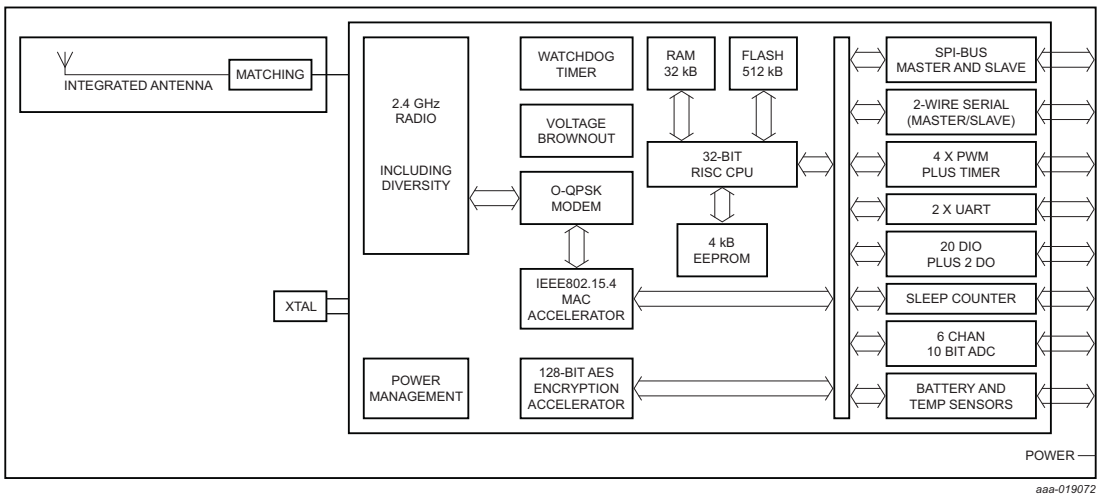
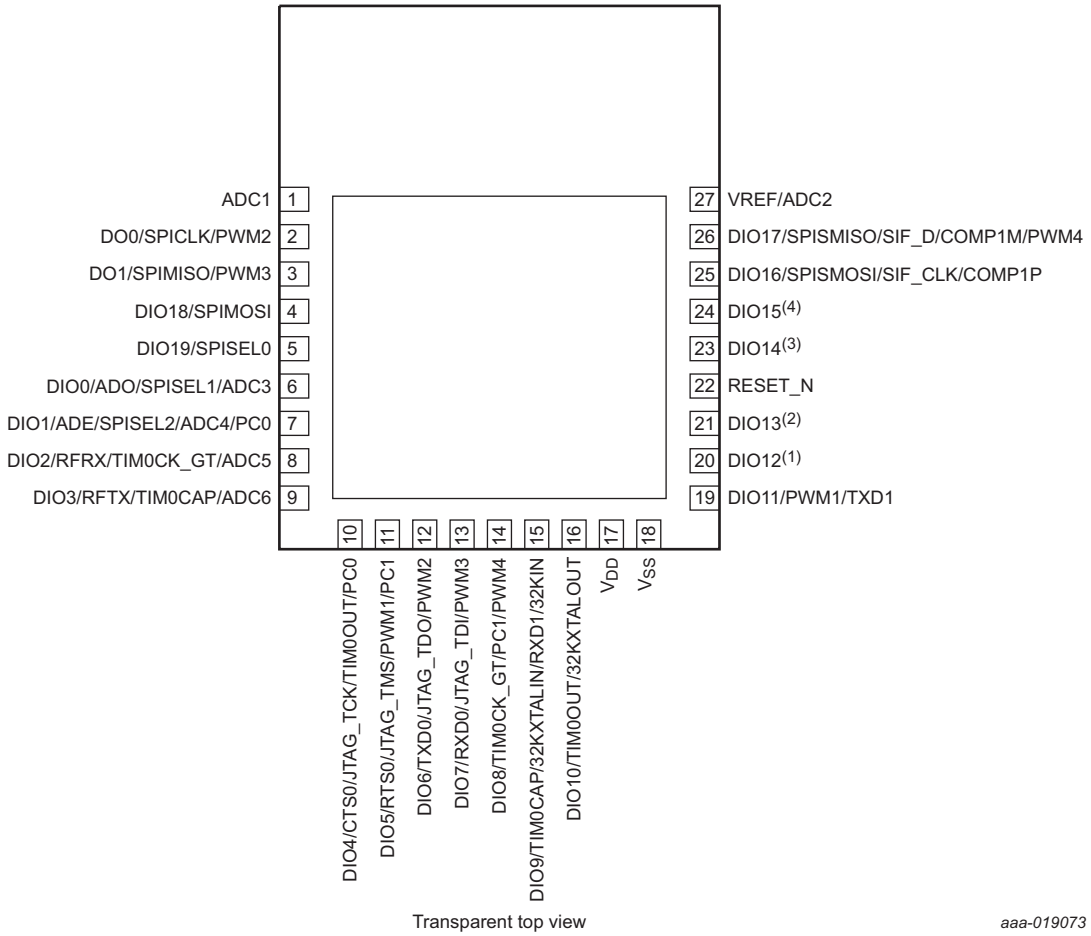


Fig 2. Block diagram

7. Pinning information

7.1 Pinning



(1) Multi-function: DIO12/PWM2/CTS0/JTAG_TCK/ADO/SPISMOSI.

(2) Multi-function: DIO13/PWM3/RTS0/JTAG_TMS/ADE/SPISMISO.

(3) Multi-function: DIO14/SIF_CLK/TXD0/TXD1/JTAG_TDO/SPISEL1/SPISSEL.

(4) Multi-function: DIO15/SIF_D/RXD0/RXD1/JTAG_TDI/SPISEL2/SPISCLK.

Fig 3. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
ADC1	1	I	**ADC1 —** ADC input
DO0/SPICLK/PWM2[2]	2	O	**DO0 —** DO0
			SPICLK — SPI-bus master clock output
			PWM2 — PWM2 output

Table 3. Pin description *…continued*

Symbol	Pin	Type[1]	Description
DO1/SPIMISO/PWM3[3]	3	I/O	**DO1 —** DO1
			SPIMISO — SPI-bus Master In, Slave Out input
			PWM3 — PWM3 output
DIO18/SPIMOSI	4	I/O	**DIO18 —** DIO18
			SPIMOSI — SPI-bus Master Out Slave In output
DIO19/SPISEL0	5	I/O	**DIO19 —** DIO19
			SPISEL0 — SPI-bus Master Select Output 0
DIO0/ADO/SPISEL1/ADC3	6	I/O	**DIO0 —** DIO0
			ADO — antenna diversity odd output
			SPISEL1 — SPI-bus master select output 1
			ADC3 — ADC input: ADC3
DIO1/ADE/SPISEL2/ADC4/PC0	7	I/O	**DIO1 —** DIO1
			ADE — antenna diversity even output
			SPISEL2 — SPI-bus master select output 2
			ADC4 — ADC input: ADC4
			PC0 — pulse counter 0 input
DIO2/RFRX/TIM0CK_GT/ADC5	8	I/O	**DIO2 —** DIO2
			RFRX — radio receives control output
			TIM0CK_GT — timer0 clock/gate input
			ADC5 — ADC input: ADC5
DIO3/RFTX/TIM0CAP/ADC6	9	I/O	**DIO3 —** DIO3
			RFTX — radio transmit control output
			TIM0CAP — timer0 capture input
			ADC6 — ADC input: ADC6
DIO4/CTS0/JTAG_TCK/TIM0OUT/PC0	10	I/O	**DIO4 —** DIO4
			CTS0 — UART 0 clear to send input
			JTAG_TCK — JTAG CLK input
			TIM0OUT — timer0 PWM output
			PC0 — pulse counter 0 input
DIO5/RTS0/JTAG_TMS/PWM1/PC1	11	I/O	**DIO5 —** DIO5
			RTS0 — UART 0 request to send output
			JTAG_TMS — JTAG mode select input
			PWM1 — PWM1 output
			PC1 — pulse counter 1 input
DIO6/TXD0/JTAG_TDO/PWM2	12	I/O	**DIO6 —** DIO6
			TXD0 — UART 0 transmit data output
			JTAG_TDO — JTAG data output
			PWM2 — PWM2 data output

Table 3. Pin description *…continued*

Symbol	Pin	Type[1]	Description
DIO7/RXD0/JTAG_TDI/PWM3	13	I/O	**DIO7 —** DIO7
			RXD0 — UART 0 receive data input
			JTAG_TDI — JTAG data input
			PWM3 — PWM 3 data output
DIO8/TIM0CK_GT/PC1/PWM4	14	I/O	**DIO8 —** DIO8
			TIM0CK_GT — timer0 clock/gate input
			PC1 — pulse counter1 input
			PWM4 — PWM 4 output
DIO9/TIM0CAP/32KXTALIN/RXD1/32KIN	15	I/O	**DIO9 —** DIO9
			TIM0CAP — Timer0 Capture input
			32KXTALIN — 32 kHz External Crystal input
			RXD1 — UART1 Receive Data input
			32KIN — 32 kHz External clock input
DIO10/TIM0OUT/32KXTALOUT	16	I/O	**DIO10 —** DIO10
			TIM0OUT — Timer0 PWM Output
			32KXTALOUT — 32 kHz External Crystal output
V_{DD}	17	P	**V_{DD} —** supply voltage
V_{SS}	18	GND	ground
DIO11/PWM1/TXD1	19	I/O	**DIO11 —** DIO11
			PWM1 — PWM1 output
			TXD1 — UART1 Transmit Data output
DIO12[4]	20	I/O	**DIO12 —** DIO12
			PWM2 — PWM2 output
			CTS0 — UART0 clear to send input
			JTAG_TCK — JTAG CLK input
			ADO — antenna diversity odd output
			SPISMOSI — SPI-bus slave Master Out, Slave In input
DIO13[5]	21	I/O	**DIO13 —** DIO13
			PWM3 — PWM3 output
			RTS0 — UART0 request to send output
			JTAG_TMS — JTAG mode select input
			ADE — antenna diversity even output
			SPISMISO — SPI-bus slave master in slave out output
RESET_N	22	I	**RESET_N —** reset input
DIO14[6]	23	I/O	**DIO14 —** DIO14
			SIF_CLK — serial interface clock
			TXD0 — UART 0 transmit data output
			TXD1 — UART 1 transmit data output
			JTAG_TDO — JTAG data output
			SPISEL1 — SPI-bus master select output 1
			SPISSEL — SPI-bus slave select input

Table 3. Pin description *…continued*

Symbol	Pin	Type[1]	Description
DIO15[7]	24	I/O	**DIO15 —** DIO15
			SIF_D — serial interface data
			RXD0 — UART 0 receive data input
			RXD1 — UART 1 receive data input
			JTAG_TDI — JTAG data input
			SPISEL2 — SPI-bus master select output 2
			SPISCLK — SPI-bus slave clock input
DIO16/SPISMOSI/SIF_CLK/COMP1P	25	I/O	**DIO16 —** DIO16
			COMP1P — comparator positive input
			SIF_CLK — Serial Interface clock
			SPISMOSI — SPI-bus Slave Master Out Slave In input
DIO17/SPISMISO/SIF_D/COMP1M	26	I/O	**DIO17 —** DIO17
			COMP1M — COMP1M; comparator negative input
			SIF_D — Serial Interface Data
			SPISMISO — SPI-bus Slave Master In Slave Out output
			PWM4 — PWM 4 output
VREF/ADC2	27	P	**VREF —** analog peripheral reference voltage
		I	**ADC2 —** ADC input 2

[1] P = power supply; G = ground; I = input, O = output; I/O = input/output.

[2] JTAG programming mode: must be left floating high during reset to avoid entering JTAG programming mode.

[3] UART programming mode: leave pin floating high during reset to avoid entering UART programming mode or hold it low to program.

[4] Multi-function: DIO12/PWM2/CTS0/JTAG_TCK/ADO/SPISMOSI.

[5] Multi-function: DIO13/PWM3/RTS0/JTAG_TMS/ADE/SPISMISO.

[6] Multi-function: DIO14/SIF_CLK/TXD0/TXD1/JTAG_TDO/SPISEL1/SPISSEL.

[7] Multi-function: DIO15/SIF_D/RXD0/RXD1/JTAG_TDI/SPISEL2/SPISCLK.

8. Functional description

8.1 JN5169 single chip wireless microcontroller

The JN5169-001-M00 is constructed around the JN5169-001 single chip wireless microcontroller, which includes the radio system, a 32-bit RISC CPU, Flash, RAM and EEPROM memory and a range of analogue and digital peripherals.

The chip is described fully in JN5169 Wireless Microcontroller Datasheet (see Ref. 2).

8.2 Peripherals

Table 4. Peripherals

Peripherals	JN5169-001-M00	JN5169-001-M06	Notes
Master SPI-bus port	3 selects	3 selects	250 kHz - 16 MHz
Slave SPI-bus port	1	1	250 kHz - 4 MHz
UART	2	2	16550 compatible

Table 4. Peripherals

Peripherals	JN5169-001-M00	JN5169-001-M06	Notes
Two-wire serial I/F (compatible with SMbus and I^2C-bus)	1	1	Up to 400kHz
PWM			16 MHz clock
timer	4	4	
timer/counter	1	1	
Programmable Sleep Timers	2	2	32 kHz clock
Digital IO lines (multiplexed with UARTs, timers and SPI-bus selects)	20	18	DIO2 and DIO3 are not available on JN5169-001-M06 modules
Analog-to-Digital converter	4	4	10-bit, up to 100 ks/s
Programmable analogue comparator	1	1	ultra low power mode for sleep
Internal temperature sensor	1	1	
Internal battery sensor	1	1	

The performance of all peripherals is defined in the JN5169 Wireless Microcontroller Datasheet (see Ref. 2).

NXP supplies all the development tools and networking stacks needed to enable end-product development to occur quickly and efficiently. These are all freely available from the NXP Wireless Connectivity TechZone (see Ref. 3). A range of evaluation/developer kits is also available, allowing products to be quickly bread boarded. Efficient development of software applications is enabled by the provision of a complete, unlimited, software developer kit. Together with the available libraries for the IEEE802.15.4 MAC and ZigBee PRO network stacks, this package provides everything required to develop application code and to trial it with hardware representative of the final module.

The module can be user programmed both in development and in production using software supplied by NXP. Access to the on-chip peripherals, MAC and network stack software is provided through specific APIs. This information is available on the NXP support website, together with many example applications, user guides, reference manuals and application notes.

9. Limiting values

Table 5. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+3.6	V
V_{VREF}	voltage on pin VREF		–0.3	V_{DDA} + 0.3V	V
V_{ADC1}	voltage on pin ADC1		–0.3	V_{DDA} + 0.3V	V

Table 5. Limiting values *…continued*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IO(dig)}$	digital input/output voltage		–0.3	V_{DDD} + 0.3V	V
T_{stg}	storage temperature		–40	+150	°C
V_{ESD}	electrostatic discharge voltage	according to ETSI EN 301 489-17 2012 V2.2.1 and ETSI EN 301 489-1 2011 V1.9.2	-	4	kV

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	[1]	2	3.6	V
T_{amb}	ambient temperature	standard range	–40	+85	°C

[1] To reach the maximum TX power, 2.8 V is the minimum.

11. Characteristics

11.1 DC current

Table 7. Active processing

V_{DD} = 2 V to 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	M00				
		radio in receive mode; maximum input level at 10 dBm	-	17.8	-	mA
		radio in receive mode; maximum input level at 0 dBm	-	16.7	-	mA
		radio in transmit mode 10 dBm [1]	-	25.7	-	mA
		radio in transmit mode 8.5 dBm [1]	-	23.5	-	mA

[1] To reach the maximum TX power, 2.8 V is the minimum.

Table 8. Sleep mode

V_{DD} = 2 V to 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(IO)}$	input/output supply current	in sleep mode; with I/O wake-up; T_{amb} = 25 °C [1]	-	0.10	-	µA
		in sleep mode; with I/O and RC oscillator timer wake-up; T_{amb} = 25 °C	-	0.73	-	µA

[1] Waiting on I/O event.

Table 9. Deep sleep mode

V_{DD} = 2 V to 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	deep sleep mode; measured at 25 °C [1]	-	50	-	nA

[1] Waiting on chip RESET or I/O event.

11.2 AC characteristics

11.2.1 Radio transceiver

These modules meet all the requirements of the IEEE802.15.4 standard over 2.0 V to 3.6 V and offers the improved RF characteristics shown in Table 10. All RF characteristics are measured single ended.

Table 10. RF port characteristics

Single-ended; Impedance = 50 Ω[1]; V_{DD} = 2 V to 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{range}	frequency range		2.4	-	2.485	GHz

[1] With external matching inductors and assuming PCB layout.

Table 11. Radio transceiver characteristics

V_{DD} = 2 V to 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
S_{RX}	receiver sensitivity	nominal for 1 % PER, as per 802.15.4	-	–96.5	-	dBm
$P_{i(RX)(max)}$	maximum receiver input power	1 % PER, measured as sensitivity; supply current at 14.7 mA	-	10	-	dBm
		1 % PER, measured as sensitivity; supply current at 13 mA	-	0	-	dBm
$RSSI_{(min)}$	minimum received signal strength indicator		-	–95	-	dBm
$RSSI_{(max)}$	maximum received signal strength indicator		-	–10	-	dBm
Transmitter						
P_o	output power	I_{DD} = 23.3 mA [1]	-	10	-	dBm
		I_{DD} = 19.6 mA [1]	-	8.5	-	dBm
$P_{o(cr)}$	control range output power	in 6 major steps and then 4 fine steps [2]	-	–42	-	dB

[1] To reach the maximum TX power, 2.8 V is the minimum on V_{DDA}.

[2] Up to an extra 2.5 dB of attenuation is available if required.

12. Federal Communication Commission Statement

- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules see Ref. 4. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment

does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

- OEM integrators instructions
  - The OEM integrators are responsible for ensuring that the end-user has no manual instructions to remove or install module
  - The module is limited to installation in mobile or fixed applications, according to CFR 47 Part 2.1091(b)
  - Separate approval is required for all other operating configurations, including portable configurations with respect to CFR 47 Part 2.1093 and different antenna configurations
- User guide mandatory statements
  - User's instructions of the host device must contain the following statements in addition to operation instructions:

    * “This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

    (1) This device may not cause harmful interference, and

    (2) This device must accept any interference received, including interference that may cause undesired operation”

    * “Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment”
- FCC RF Exposure requirements
  - User's instructions of the host device must contain the following instructions in addition to operation instructions:

    * The antenna used with this module must be installed to provide a separation distance of at least 20 cm from all persons, and must not transmit simultaneously with any other antenna or transmitter

12.1 FCC end product labelling

The final ‘end product’ should be labelled in a visible area with the following:

“Contains TX FCC ID: XXMJN5169M0”.

13. Footprint information for reflow soldering

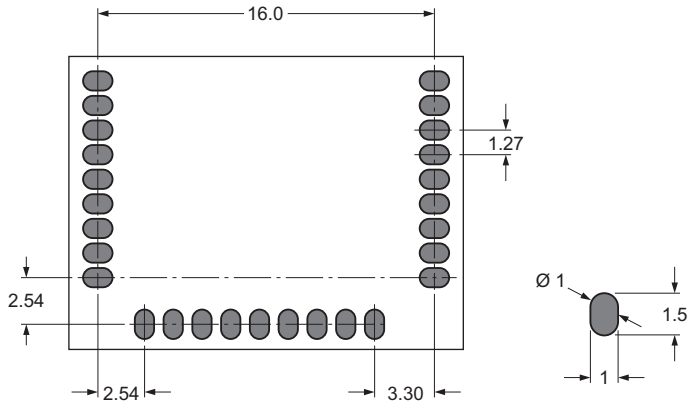


Fig 4. Module PCB footprint

14. Package outline

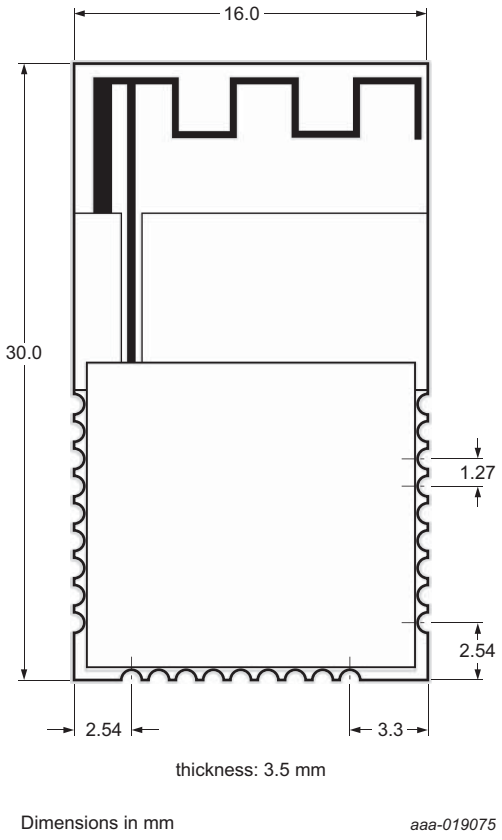


Fig 5. Package outline JN5169-001-M00

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
API	Application Program Interface
ADC	Analog to Digital Converter
FCC	Federal Communication Commission
IO	Input Output
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PER	Packet Error Rate
PWM	Pulse Width Modulation
R&TTE	Radio and Telecommunications Terminal Equipment
RF	Radio Frequency
RISC	Reduce Instruction Set Computing
RSSI	Receive Signal Strength Indicator
RTS	Request-To-Send
SPI	Serial Peripheral Interface
SVM	Supply Voltage Monitor
SYNTH	SYNTHesizer
UART	Universal Asynchronous Receiver/Transmitter

16. References

[1] **IEEE Std 802.15.4-2011 —** IEEE Std 802.15.4-2011 IEEE Standard for Information Technology.

[2] **JN5169 —** JN5169 wireless microcontroller datasheet.

[3] **Wireless Connectivity TechZone —** http://www.nxp.com/techzones/wireless-connectivity

[4] **Part 15 of the FCC Rules —**

http://www.ecfr.gov/cgi-bin/text-idx?SID=d01e00935bfcb0d53b914e7c8e63f383&node=47:1.0.1.1.16&rgn=div5

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