Bluespark Technical Overview

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Bluespark is a battery operated GPS receiver that transmits the NMEA data to a remote host using the Bluetooth protocol.

The schematic is divided in to four sections:
Page 1. GPS RF front end and Receiver.
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Page 4. Power supplies and logic translation.

GPS RF front end and Receiver.

GPS signals on 1575.42 MHz are picked up by the dielectric patch antenna (P1) and amplified by the LNA, Q4, whose bias is controlled/switched by Q1.
Q3-A and Q3-B form a high side comparator sensing the voltage across R38 when current is drawn by an external antenna applied to J2. Q2-A and Q2-B buffer the comparator output and switch pin diode D10 on while switching Q1 off, thus selecting the external antenna while shutting off the LNA and hence the internal antenna.
Note that the external antenna is applied after the on board LNA and assumes an active gain in the order of 18-30dB. (3V source, 5-20mA operating current)
Q14 provides the processor with a level translated, active low flag to indicate that an external antenna is applied.

U6 is a low noise 2.8V regulator providing power to the RF section and is controlled via the RFPC0 line from the processor when using trickle mode.
Q15 and Q6 are also controlled from this line and switch off power to the external antenna when in trickle mode in order to conserve battery power.

Signals from the selected source (either int. or ext. antenna) are presented to FL2, a SAW filter on 1575.42MHz to remove out of band signals before being input to U4, the SiRF RF IC.
The GPS TCXO, Y5, and resonant circuit C96, L7 provide a clean, stable oscillator source.
The SiRF RF IC uses a superheterodyne principle with a VCO local oscillator on 1565.97MHz and an IF of 9.45MHz.
2 bit sign and magnitude data is sent to the SiRF processor while RF power and AGC control signals are received.

GPS processor and flash memory.

The GPS processor is based on the ARM7 CPU and runs a 1.8V core with 3.3V I/O.
It is a true system on a chip and contains at least the following functions:
1Mbit SRAM, Boot ROM, Real Time Clock, GPS DSP, Battery backed SRAM, Beacon DSP, SPI bus, I/O unit and Dual UARTs.
Refering to page 2 of the schematic, U10 is a voltage monitor providing an active low reset to the processor if the 3V SiRF Vcc drops below 2.8V. D6 provides a non-return charging path (when the GPS is active) for the 3V MS Li-Ion battery (BT1) which supplies the RTC and BBSRAM via U18, a 1.8V regulator, when main batteries/ext power is absent. When either

the internal batteries or the external power source is available, an alternative path is provided via D1 and DC_IN.
Q7-A provides a level translated active low flag to the processor when external power is available thus allowing mode switching and the benefits of full power GPS to be realised.
SIRF_TX and SIRF_RX are the main UART outputs (non-inverted TTL, 57600,8N1) carrying the NMEA data.

Bluetooth transceiver/processor and flash memory.

U3 is the BlueCore 2 single chip Bluetooth system incorporating 2.4GHz transmit/receive and baseband functions.
Data originating from the GPS is presented to BC_RX, the BC2 UART input, for processing and eventual transmission as RF. Timing for all processor and RF synthesis is provided by the 16MHz crystal Y1.

When transmitting, the outgoing balanced RF is first matched and converted to 50 ohm single ended by inductors L2, L3 and balun Y2. Filter Y3 provides harmonic and spurious output rejection before signals are passed to the chip antenna. Note that DC is provided to the push-pull output section of the BC2 via the balun.

In receive, the reverse order of operation applies – signals from the 50 ohm chip antenna are first filtered (out of of band signals) then translated to a balanced input, under control of the internal T/R switch.

U5 is a 4Mbit 1.8V flash memory that directly interfaces with the BC2.
Q13-A and Q13-B buffer and translate the PIO ports to provide LED indicators for low battery (DS1, Red) and Bluetooth status (DS2, Blue).

Power supplies and logic translation.

3 x AAA cells provide the main (int) power and this supply goes via the reverse battery protection device, Q5, to the 3V switching regulator, U13. Low battery status is monitored by U9 which outputs an active low to both the SiRF and BC2 processors, via D5, when level drops below 3.2V.

J3 is the external 5V DC input socket. D2 provides reverse polarity protection while U11, a precision shunt regulator, conducts if the supply goes over 5.7V, saturating Q16 and shutting off Q17. This open circuit over voltage protection serves to protect U13 but is not intended to duplicate the full automotive load dump already provided in the 12V to 5V cigarette adaptor.

When the On/Off switch, S3, is pressed, Q9 turns on and provides an enable to U13, the 3V switchmode regulator. This provides power to U7, which outputs 1.8V to the BC2. The BC2 then outputs a logic high to PWR_ON, switching on Q8-A and effectively latching the power switch on.
If the BC2 is already powered on then pushing the switch S3 again will turn on Q8-B, providing the BC2 with a logic high on PWR_OFF and initiating the power down sequence.

Q18 and Q19 allow the BC2 to control the 3V GPS supply, saving power when the Bluetooth link is lost or yet to be acquired.

Q10-A and Q10-B provide inversion (2 stages), buffering and level translation for the SIRF_TX to BC_RX data path, with a tap mid way to the flash/program adaptor plug, J1. Similarly, Q11-A and Q11-B provide the same for the BC_TX to SIRF_RX data path.

Q12-A and Q12-B provide translation from the BC2 GPIO to allow the SiRF processor to be reflashed. A tap between these devices also goes to J1.

J1 is a diagnostic/test connector accessing most of the control and monitoring points needed to flash either the GPS or Bluetooth functions (even simultaneously).